LTC1326

Micropower Precision Triple Supply Monitor

FEATURES

- **Simultaneously Monitors 5V, 3.3V and Adjustable Inputs**
- **Guaranteed Threshold Accuracy: ±0.75%**
- Low Supply Current: 20µA
- Internal Reset Time Delay: 200ms
- Manual Pushbutton Reset Input
- Active Low and Active High Reset Outputs
- Active Low "Soft" Reset Output
- Power Supply Glitch Immunity
- Guaranteed $\overline{\text{RESET}}$ for $V_{CC3} \geq 1V$
- 8-Pin SO and MSOP Packages

APPLICATIONS

- Desktop Computers
- Notebook Computers
- Intelligent Instruments
- Portable Battery-Powered Equipment

DESCRIPTION

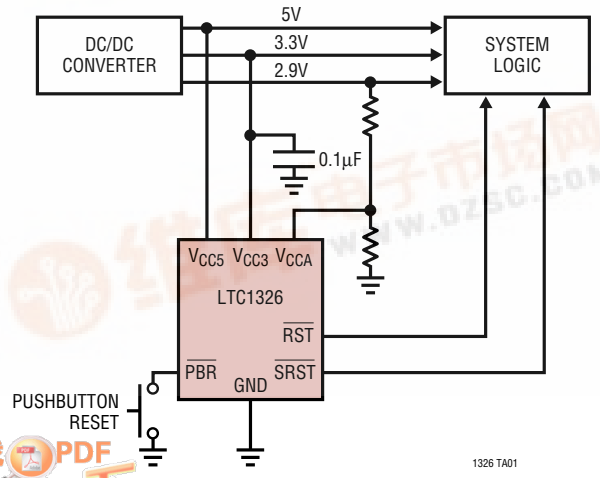
The LTC®1326 is a triple supply monitor intended for systems with multiple supply voltages. It provides micropower operation, small size and high accuracy supply monitoring.

Tight 0.75% threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The 20µA typical supply current makes the LTC1326 ideal for power-conscious systems.

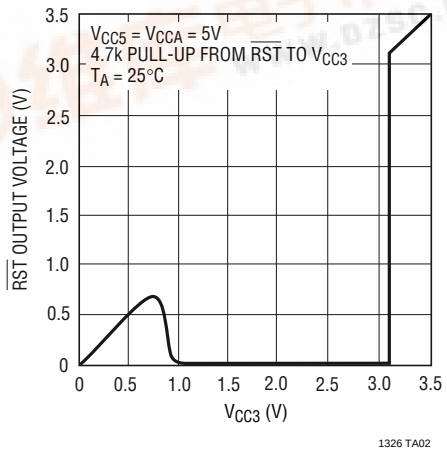
The $\overline{\text{RST}}$ output is guaranteed to be in the correct state for V_{CC3} down to 1V. The LTC1326 may also be configured to monitor any one or two V_{CC} inputs instead of three, depending on system requirements.

A manual pushbutton reset input provides the ability to generate a very narrow "soft" reset pulse (100µs typ) or a 200ms reset pulse equivalent to a power-on reset. Both $\overline{\text{SRST}}$ and $\overline{\text{RST}}$ outputs are open-drain and can be OR-tied with other reset sources.

TYPICAL APPLICATION



$\overline{\text{RST}}$ Output Voltage vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

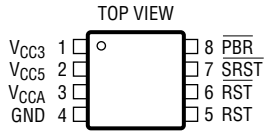
(Notes 1, 2)

Terminal Voltage

V_{CC3}, V_{CC5}, V_{CCA} ..... –0.5V to 7V
$\overline{RST}$, $\overline{SRST}$ ..... –0.5V to 7V
$\overline{RST}$ ..... –0.5V to V_{CC3} + 0.3V
$\overline{PBR}$ ..... –7V to 7V

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

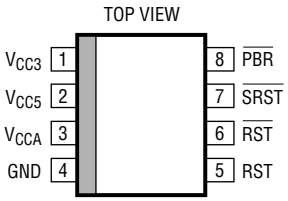
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LTC1326CMS8
MS8 PART NUMBER
LTBA



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1326CS8
S8 PART NUMBER
1326

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC3} = 3.3V, V_{CC5} = 5V, V_{CCA} = V_{CC3}, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT3}	Reset Threshold V_{CC3}		●	3.094	3.118	3.143	V
V_{RT5}	Reset Threshold V_{CC5}		●	4.687	4.725	4.762	V
V_{RTA}	Reset Threshold V_{CCA}		●	0.992	1.000	1.007	V
V_{CC}	V_{CC3} Operating Voltage	$\overline{RST}$ in Correct Logic State	●	1		7	V
I_{VCC3}	V_{CC3} Supply Current	$\overline{PBR}$ = V_{CC3}	●		20	40	µA
I_{VCC5}	V_{CC5} Input Current	V_{CC5} = 5V	●		2.8	5	µA
I_{VCCA}	V_{CCA} Input Current	V_{CCA} = 1V	●	–5	0	5	nA
t_{RST}	Reset Pulse Width	$\overline{RST}$ Low with 10kΩ Pull-Up to V_{CC3}	●	140	200	280	ms
t_{SRST}	Soft Reset Pulse Width	$\overline{SRST}$ Low with 10kΩ Pull-Up to V_{CC3}	●	50	100	200	µs
t_{UV}	V_{CC} Undervoltage Detect to $\overline{RST}$	V_{CC5}, V_{CC3} or V_{CCA} Less Than Reset Threshold V_{RT} by More Than 1%			13		µs
I_{PBR}	$\overline{PBR}$ Pull-Up Current	$\overline{PBR}$ = 0V	●	3	7	10	µA
V_{IL}	$\overline{PBR}$, $\overline{RST}$ Input Low Voltage		●			0.8	V
V_{IH}	$\overline{PBR}$, $\overline{RST}$ Input High Voltage		●	2			V
t_{PW}	$\overline{PBR}$ Min Pulse Width		●	40			ns
t_{DB}	$\overline{PBR}$ Debounce	Deassertion of $\overline{PBR}$ Input to $\overline{SRST}$ Output ($\overline{PBR}$ Pulse Width = 1µs)	●		20	35	ms
t_{PB}	$\overline{PBR}$ Assertion Time to Reset	$\overline{PBR}$ Held Less Than V_{IL}	●	1.4	2.0	2.8	s

ELECTRICAL CHARACTERISTICS

V_{CC3} = 3.3V, V_{CC5} = 5V, V_{CCA} = V_{CC3}, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	$\overline{RST}$ Output Voltage Low	I_{SINK} = 5mA I_{SINK} = 100µA, V_{CC3} = 1V	● ●		0.15 0.05	0.4 0.4	V V
	$\overline{SRST}$ Output Voltage Low	I_{SINK} = 2.5mA	●		0.15	0.4	V
	RST Output Voltage Low	I_{SINK} = 2.5mA	●		0.15	0.4	V
V_{OH}	$\overline{RST}$ Output Voltage High (Note 3)	I_{SOURCE} = 1µA	●	V_{CC3} – 1			V
	$\overline{SRST}$ Output Voltage High (Note 3)	I_{SOURCE} = 1µA	●	V_{CC3} – 1			V
	RST Output Voltage High	I_{SOURCE} = 600µA	●	V_{CC3} – 1			V
t_{PHL}	Prop Delay $\overline{RST}$ to RST High Input to Low Output	C_{RST} = 20pF			25		ns
t_{PLH}	Prop Delay $\overline{RST}$ to RST Low Input to High Output	C_{RST} = 20pF			45		ns
V_{OVR}	V_{CC5} Reset Override Voltage	Override V_{CC5} Ability to Assert $\overline{RST}$ (Note 4)			V_{CC3} ±0.025		V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

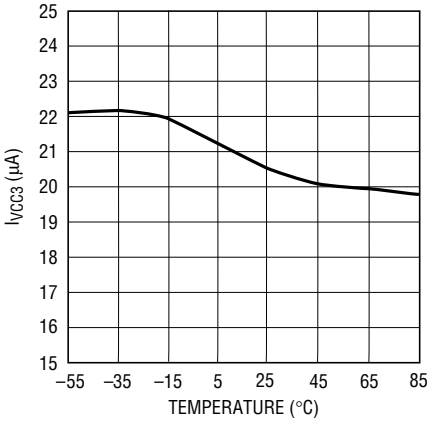
Note 2: All voltage values are with respect to GND.

Note 3: The output pins $\overline{SRST}$ and $\overline{RST}$ have weak internal pull-ups to V_{CC3} of 6µA typ. However, external pull-up resistors may be used when faster rise times are required.

Note 4: The V_{CC5} reset override voltage is valid for an operating range less than approximately 4.15V. Above this point the override is turned off and the V_{CC5} pin functions normally.

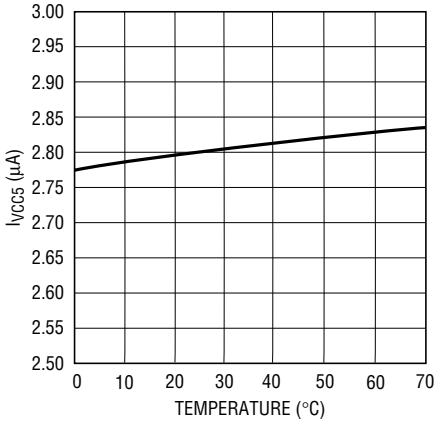
TYPICAL PERFORMANCE CHARACTERISTICS

I_{VCC3} vs Temperature



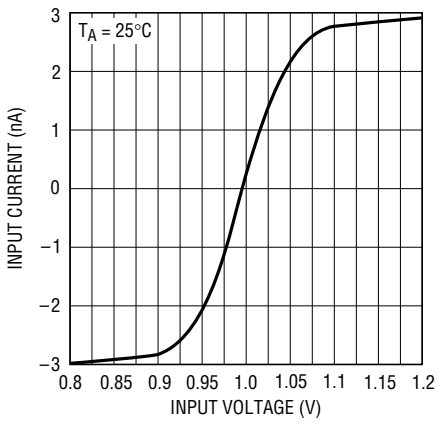
1326 G01

I_{VCC5} vs Temperature



1326 G02

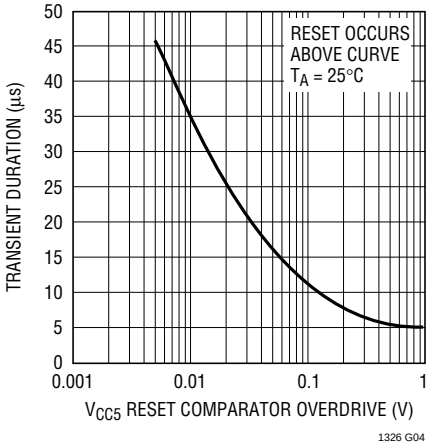
V_{CCA} Input Current vs Input Voltage



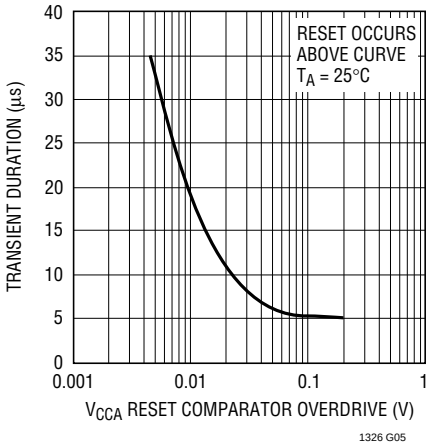
1236 G06

TYPICAL PERFORMANCE CHARACTERISTICS

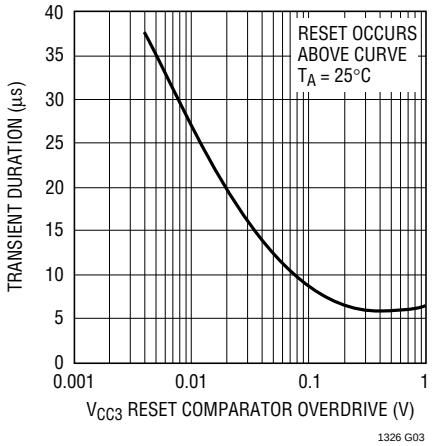
V_{CC5} Transient Immunity



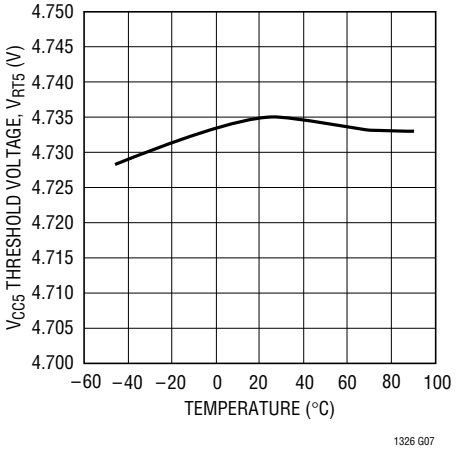
V_{CCA} Transient Immunity



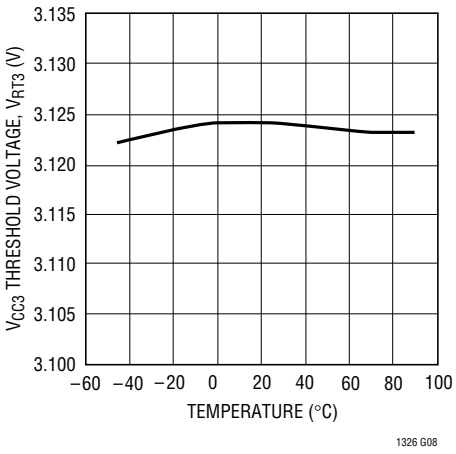
V_{CC3} Transient Immunity



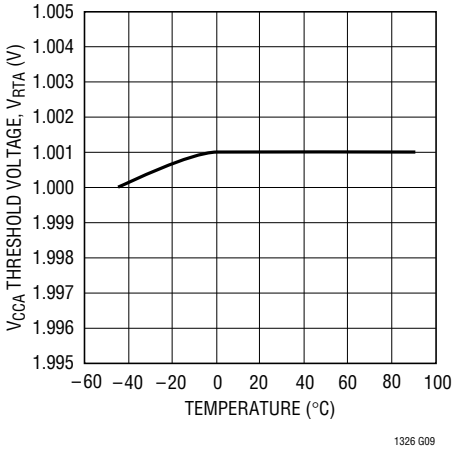
V_{CC5} Threshold Voltage vs Temperature



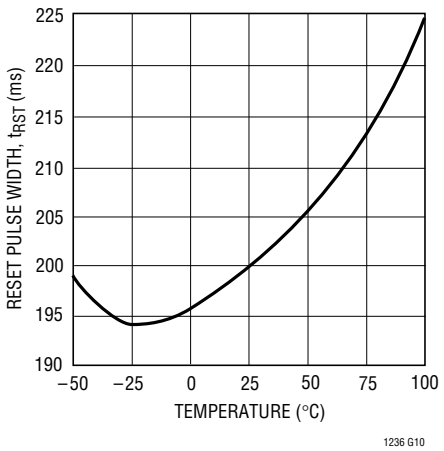
V_{CC3} Threshold Voltage vs Temperature



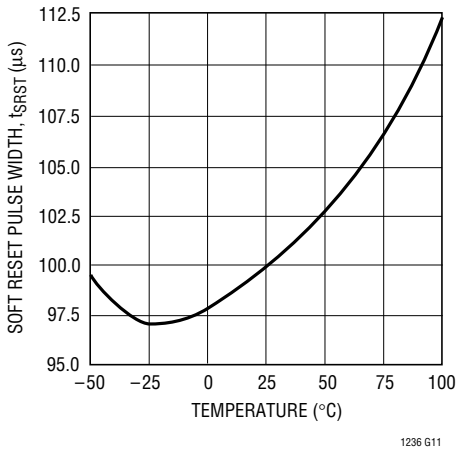
V_{CCA} Threshold Voltage vs Temperature



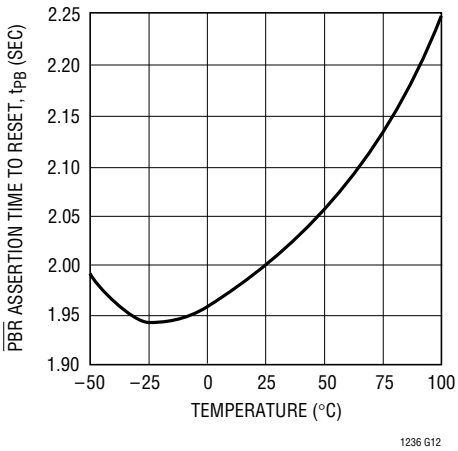
Reset Pulse Width vs Temperature



"Soft" Reset Pulse Width vs Temperature



$\overline{PBR}$ Assertion Time to Reset vs Temperature



PIN FUNCTIONS

V_{CC3} (Pin 1): 3.3V Sense Input and Power Supply Pin for the IC. At least 1V must be applied to this pin for the $\overline{RST}$ to be in its guaranteed state. Bypass to ground with ≥0.1µF ceramic capacitor.

V_{CC5} (Pin 2): 5V Sense Input.

V_{CCA} (Pin 3): 1V Sense, High Impedance Input. If unused it can be tied to either V_{CC3} or V_{CC5}.

GND (Pin 4): Ground.

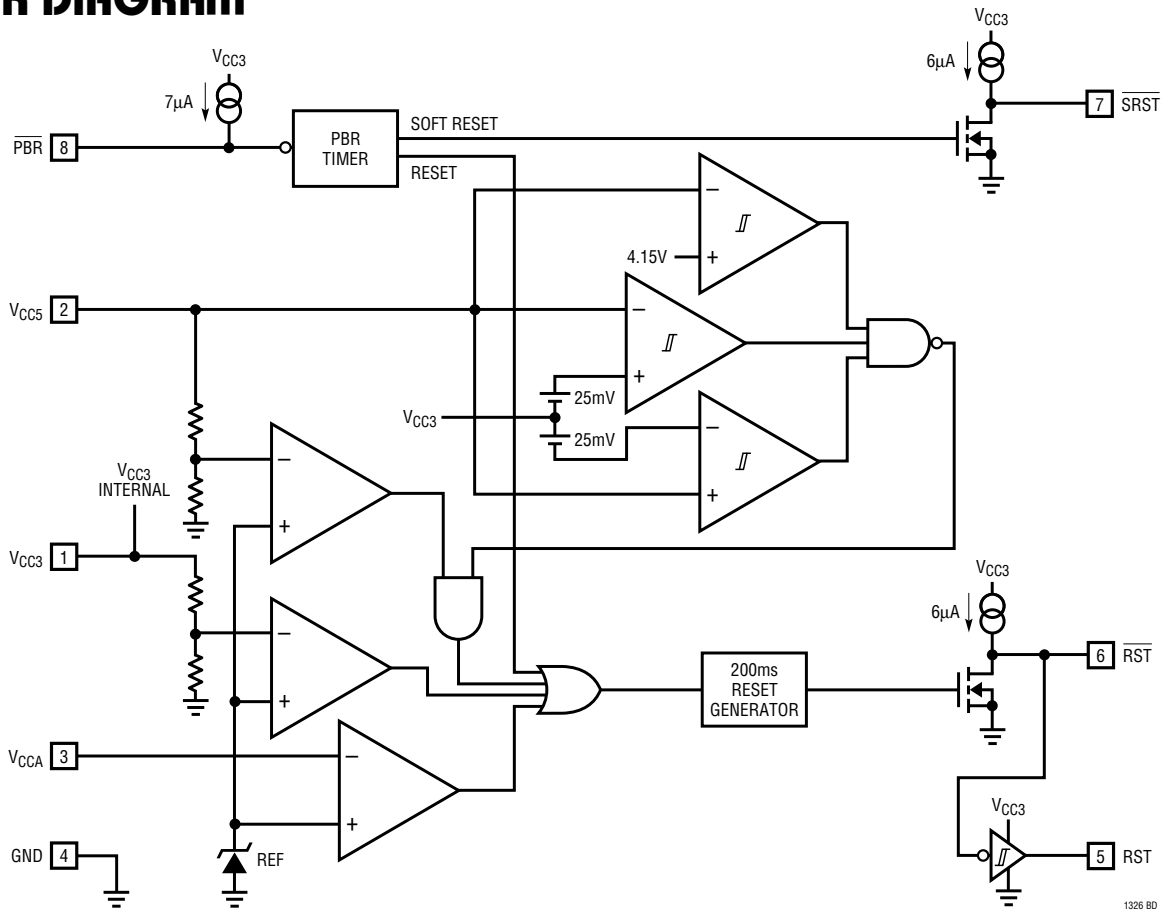
RST (Pin 5): Reset Logic Output. Active high CMOS logic output, drives high to V_{CC3}, buffered compliment of $\overline{RST}$. An external pull-down on the $\overline{RST}$ pin will drive this pin high.

$\overline{RST}$ (Pin 6): Reset Logic Output. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted when one or more of the supplies are below trip thresholds and held for 200ms after all supplies become valid. Also asserted after $\overline{PBR}$ is held low for more than 2 seconds and for an additional 200ms after $\overline{PBR}$ is released.

$\overline{SRST}$ (Pin 7): "Soft" Reset. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted for 100µs after $\overline{PBR}$ is held low for less than 2 seconds and released.

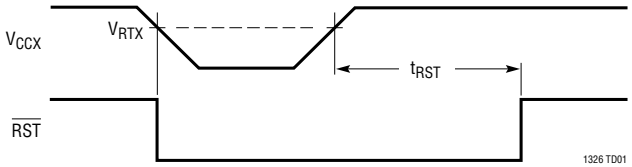
$\overline{PBR}$ (Pin 8): Pushbutton Reset. Active low logic input with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. When asserted for less than 2 seconds, outputs a soft reset 100µs pulse on the $\overline{SRST}$ pin. When $\overline{PBR}$ is asserted for greater than 2 seconds, the $\overline{RST}$ output is forced low and remains low until 200ms after $\overline{PBR}$ is released.

BLOCK DIAGRAM

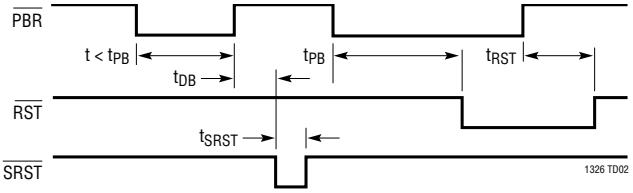


TIMING DIAGRAMS

V_{CC} Monitor Timing



Pushbutton Reset Function Timing



APPLICATIONS INFORMATION

Operation

The LTC1326 is a micropower, high accuracy triple supply monitoring circuit. The part has two basic functions: generation of a reset when power supplies are out of range, and generation of reset or a "soft" reset when the $\overline{PBR}$ is pulled low.

Supply Monitoring

All three V_{CC} inputs must be above predetermined thresholds for 200ms before the reset output is released. The LTC1326 will assert reset during power-up, power-down and brownout conditions on any one or more of the V_{CC} inputs (assumes $V_{CC3} \geq 1V$).

On power-up, before V_{CC3} reaches 1V, $\overline{RST}$ is pulled to a logic low of 0.4V or less. As long as any one of the V_{CC} inputs is below its predetermined threshold, $\overline{RST}$ will stay a logic low. Once all of the V_{CC} inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after 200ms. $\overline{RST}$ outputs the inverted state of what is seen on $\overline{RST}$.

$\overline{RST}$ is reasserted whenever any one of the V_{CC} inputs drops below its predetermined threshold and remains asserted until 200ms after all of the V_{CC} inputs are above their thresholds.

On power-down, once any of the V_{CC} inputs drop below its threshold, $\overline{RST}$ is held at a logic low. A logic low of 0.4V is guaranteed until V_{CC3} drops below 1V.

The three precision voltage comparators internal to the LTC1326 have response times that are typically 13µs. This slow response time helps prevent mistriggering due to transients on each of the V_{CC} inputs. The part's ability to suppress transients can be improved by bypassing each of the V_{CC} inputs with a 0.1µF capacitor to ground.

Pushbutton Reset

The LTC1326 provides a pushbutton reset input pin. The $\overline{PBR}$ input has an internal pull-up current source to V_{CC3}. If the $\overline{PBR}$ pin is not used it can be left floating.

When the $\overline{PBR}$ is pulled low for less than t_{PB} (≈2 sec), a narrow (100µs typ) soft reset pulse is generated on the $\overline{SRST}$ output pin after the button is released. The pushbutton circuitry contains an internal debounce counter which delays the output of the soft reset pulse by typically 20ms. This pin can be OR-tied to the $\overline{RST}$ pin and issue what is called a "soft" reset. The $\overline{SRST}$ thereby resets the microprocessor without interrupting the DRAM refresh cycle. In this manner DRAM information remains undisturbed. Alternatively, $\overline{SRST}$ may be monitored by the processor to initiate a software-controlled reset.

When the $\overline{PBR}$ pin is held low for longer than t_{PB} (≈2 sec), a standard reset is generated. Once the 2 second period has elapsed, a reset signal is produced by the pushbutton logic, thereby clearing the reset counter. Once the button is released, the reset counter begins counting the reset period (200ms nominal). Consequently, the reset outputs remain asserted for approximately 200ms after the button is released.

During a supply induced reset condition, the ability of the $\overline{PBR}$ pin to force a soft reset condition on the $\overline{SRST}$ pin is disabled. In other words $\overline{SRST}$ will remain high. If the $\overline{PBR}$ pin is held low, both during and after a supply induced reset (low $\overline{RST}$), the $\overline{RST}$ pin will remain low until 200ms after the $\overline{PBR}$ goes high.

APPLICATIONS INFORMATION

Dual and Single Supply Monitor Operation

The V_{CC3}, V_{CC5} and V_{CCA} inputs may be individually disabled by the following techniques which allows the LTC1326 to be used as a dual or single supply monitor.

The V_{CCA} pin, if unused, can be tied to either V_{CC3} or V_{CC5}. This is an obvious solution since the trip points for V_{CC3} and V_{CC5} will always be greater than the trip point for V_{CCA}.

The V_{CC5} input trip point is disabled if its voltage is equal to the voltage on $V_{CC3} \pm 25$mV and the voltage on V_{CC5} is less than 4.15V. In this manner the part will behave as a 3.3V monitor and the V_{CC5} reset will be disabled.

The V_{CC5} trip point is reenabled when the voltage on V_{CC5} is equal to the voltage on $V_{CC3} \pm 25$mV and the two inputs are greater than approximately 4.15V. In this manner the LTC1326 can function as a 5V monitor with the 3.3V monitor disabled.

When monitoring either 3.3V or 5V with V_{CC3} strapped to V_{CC5}, (see Figure 1) the LTC1326 determines which is the appropriate range. The LTC1326 handles this situation as shown in Figure 2. Above 1V and below V_{RT3}, $\overline{RST}$ is held low. From V_{RT3} to approximately 4.15V the LTC1326 assumes 3.3V supply monitoring and $\overline{RST}$ is deasserted. Above approximately 4.15V the LTC1326 operates as a 5V monitor. Table 1 summarizes the state of $\overline{RST}$ and RST at various operating voltages with $V_{CC3} = V_{CC5}$.

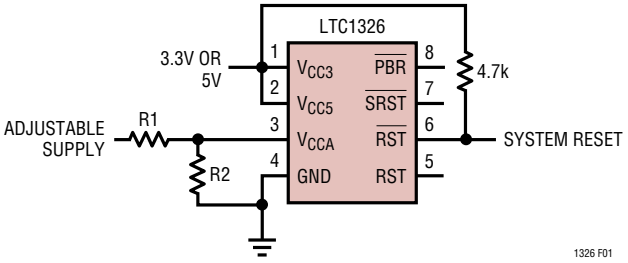


Figure 1

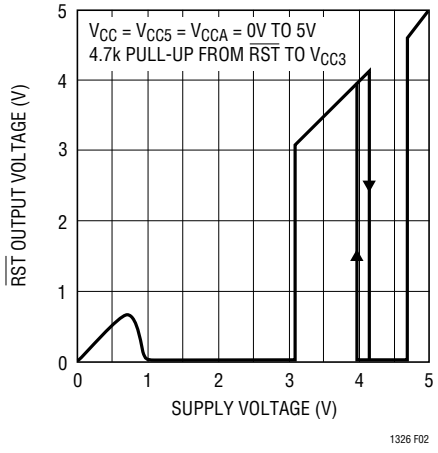


Figure 2. $\overline{RST}$ Voltage vs Supply Voltage

Table 1. Override Truth Table ($V_{CC3} = V_{CC5}$)

INPUTS ($V_{CC3} = V_{CC5} = V_{CC}$)	$\overline{RST}$	RST
$0V \le V_{CC} \le 1V$	—	—
$1V \le V_{CC} \le V_{RT3}$	0	1
$V_{RT3} \le V_{CC} \le 4.15V$	1	0
$4.15V \le V_{CC} \le V_{RT5}$	0	1
$V_{RT5} \le V_{CC}$	1	0

Interfacing to 5V Logic

The LTC1326 is powered internally from the V_{CC3} pin. In applications where the $\overline{RESET}$ signal is going to a 5V microprocessor, it is possible to have a case where the 5V supply is up and the 3.3V supply is at 0V. In this situation the LTC1326 doesn't have the drive capability to ensure a valid low on the $\overline{RST}$ pin. This is especially true if there is a pull-up resistor to V_{CC5}. The circuit, Figure 3, will ensure proper assertion of system $\overline{RESET}$ to the 5V logic as long as either the 5V or 3.3V supply has at least 1V applied.

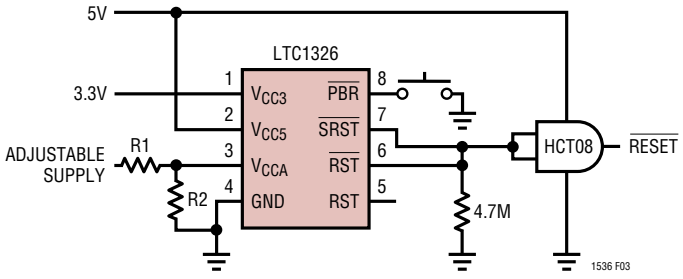
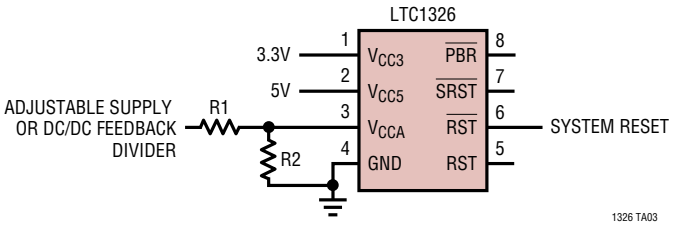


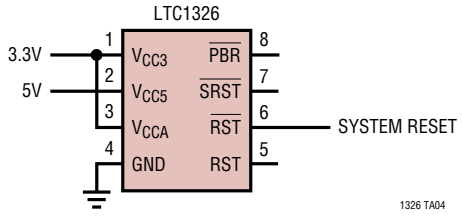
Figure 3. Triple Supply Monitor Interfacing to a 5V Microprocessor

TYPICAL APPLICATIONS

Triple Supply Monitor (3.3V, 5V and Adjustable)

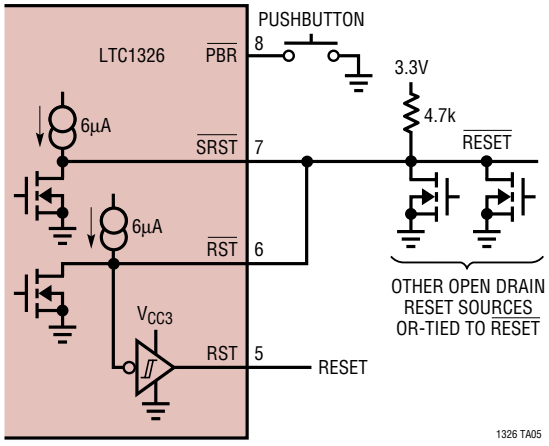


Dual Supply Monitor (3.3V and 5V, Defeat V_{CCA} Input)

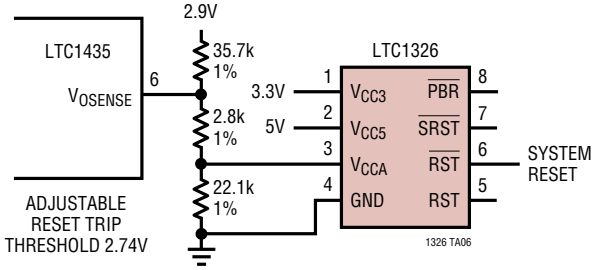


TYPICAL APPLICATIONS

$\overline{SRST}$ Tied to $\overline{RST}$ and OR-Tying Other Sources to $\overline{RST}$ to Generate $\overline{Reset}$ and Reset

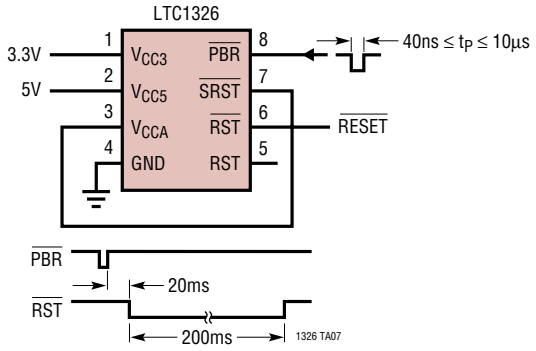


Using V_{CCA} Tied to DC/DC Feedback Divider

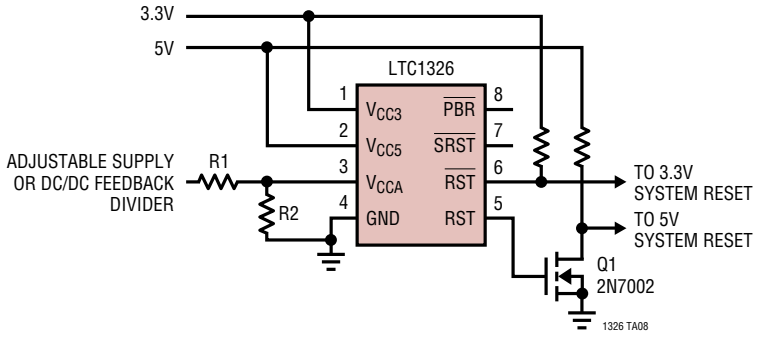


TYPICAL APPLICATIONS

Using the Short Pulse Width, Pushbutton Soft Reset Feature to Initiate Hard Reset



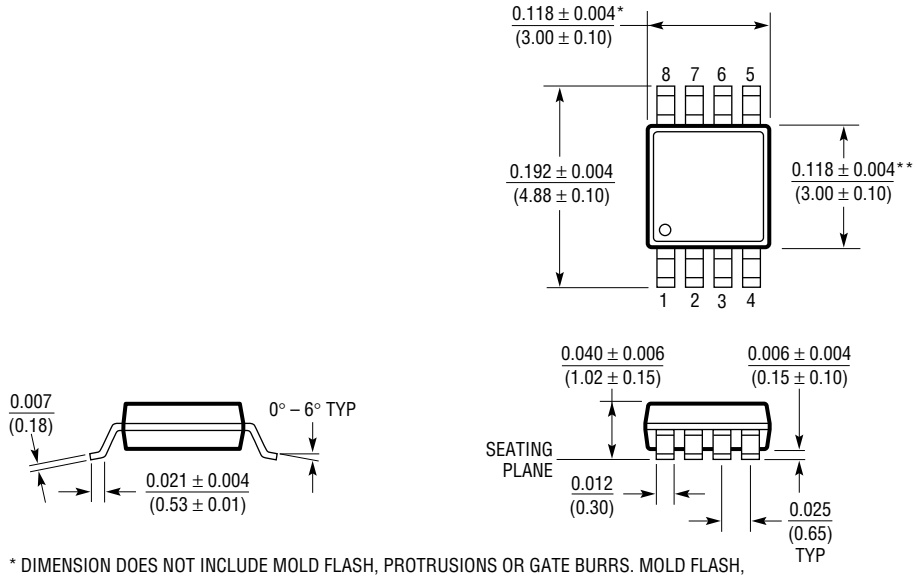
Triple Supply Monitor with 3.3V and 5V System Resets



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)

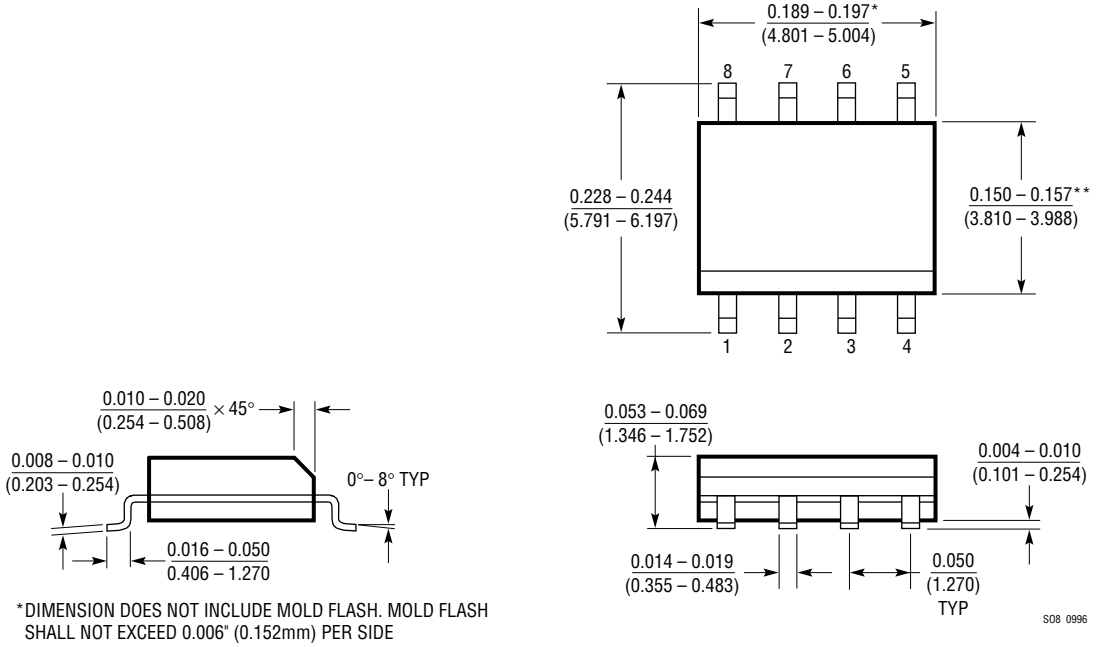


* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

MSOP08 0596

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Pushbutton Reset	4.37V/4.62V Threshold
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications