INITIAL RELEASE

Final Electrical Specifications

LT1394

7ns, Low Power, Single Supply, Ground-Sensing Comparator

May 1998

FEATURES

- **Ultrafast: 7ns**
- **Low Power: 6mA**
- **Low Offset Voltage: 0.8mV**
- Operates Off Single 5V or Dual ±5V Supplies
- Input Common Mode Extends to Negative Supply
- No Minimum Slew Rate Requirement
- Complementary TTL Outputs
- Inputs Can Exceed Supplies without Phase Reversal
- Pin Compatible with LT1016 and LT1116
- Output Latch Capability
- Available in SO-8 Package

APPLICATIONS

- High Speed A/D Converters
- Zero-Crossing Detectors
- Current Sense for Switching Regulators
- Extended Range V/F Coverters
- Fast Pulse Height/Width Discriminators
- High Speed Triggers
- Line Receivers
- High Speed Sampling Circuits

DESCRIPTION

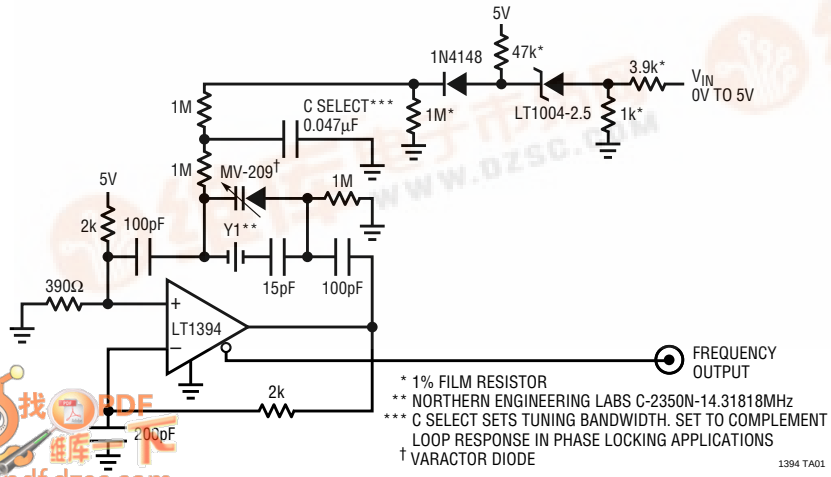
The LT®1394 is an UltraFast™ (7ns) comparator with complementary outputs and latch. The input common mode range extends from 1.5V below the positive supply down to the negative supply rail. Like the LT1016 and LT1116, this comparator has complementary outputs designed to interface directly to TTL or CMOS logic. The LT1394 may operate from either a single 5V supply or dual ±5V supplies. Low offset voltage specifications and high gain allow the LT1394 to be used in precision applications.

The LT1394 is designed for improved speed and stability for a wide range of operating conditions. The output stage provides active drive in both directions for maximum speed into TTL, CMOS or passive loads with minimal cross-conduction current. Unlike other fast comparators, the LT1394 remains stable even for slow transitions through the active region, which eliminates the need to specify a minimum input slew rate.

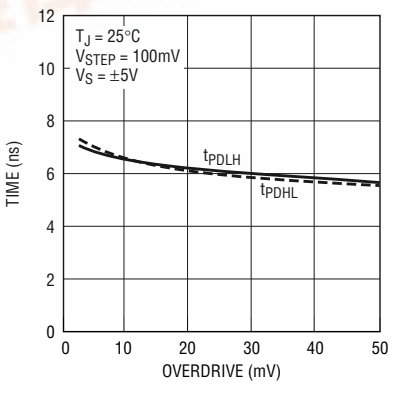
The LT1394 has an internal, TTL/CMOS compatible latch for retaining data at the outputs. The latch holds data as long as the LATCH pin is held high. Device parameters such as gain, offset and negative power supply current are not significantly affected by variations in negative supply voltage.

TYPICAL APPLICATION

14.31818MHz (4X NTSC) Voltage Tunable Crystal Oscillator



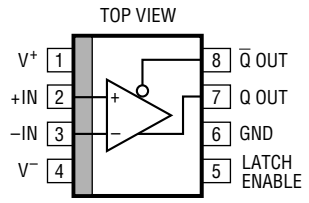
Propagation Delay vs Input Overdrive



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage 7V
Negative Supply Voltage ..... –7V
Total Supply Voltage (V^+ to V^-) 12V
Differential Input Voltage ..... ±12V
Input and Latch Current ..... ±10mA
Output Current (Continuous) ..... ±20mA
Operating Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1394CS8
S8 PART MARKING
1394

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = –5V, $V_{OUT}(Q)$ = 1.4V, V_{LATCH} = V_{CM} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 1)			0.8	2.5	mV
			●			4.0	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		4		µV/°C
I_{OS}	Input Offset Current				0.1	0.5	µA
			●			0.8	µA
I_B	Input Bias Current	(Note 2)			2	4.5	µA
			●			7.0	µA
IVR	Input Voltage Range		●	–5		3.5	V
		Single 5V Supply	●	0		3.5	V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 3.5V$			100		dB
			●	55			dB
		Single 5V Supply $0V \le V_{CM} \le 3.5V$			100		dB
			●	55			dB
PSRR	Power Supply Rejection Ratio	$4.6V \le V^+ \le 5.4V$			65		dB
			●	50			dB
		$-7V \le V^- \le -2V$			100		dB
			●	65			dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		750	1600		V/V
V_{OH}	Output Voltage Swing High	$V^+ \ge 4.6V$, I_{OUT} = 1mA	●	2.7	3.1		V
		$V^+ \ge 4.6V$, I_{OUT} = 4mA	●	2.4	3.0		V
V_{OL}	Output Voltage Swing Low	I_{OUT} = –4mA	●		0.3	0.5	V
		I_{OUT} = –10mA			0.4		V
I^+	Positive Supply Current				6	8.5	mA
			●			10.0	mA
I^-	Negative Supply Current				1.2	2.2	mA
			●			2.5	mA

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = –5V, $V_{OUT}(Q)$ = 1.4V, V_{LATCH} = V_{CM} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	LATCH Pin High Input Voltage		●	2			V
V_{IL}	LATCH Pin Low Input Voltage		●			0.8	V
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V	●		–4	–10	µA
t_{PD}	Propagation Delay (Note 3)	ΔV_{IN} = 100mV, V_{OD} = 5mV	 ●		7	9 14	ns ns
Δt_{PD}	Differential Propagation Delay (Note 3)	ΔV_{IN} = 100mV, V_{OD} = 5mV			0.5	2.2	ns
t_{LPD}	Latch Propagation Delay (Note 4)				6		ns
t_{SU}	Latch Setup Time (Note 4)				–0.4		ns
t_H	Latch Hold Time (Note 4)				2		ns
$t_{PW}(D)$	Minimum Disable Pulse Width				3		ns

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

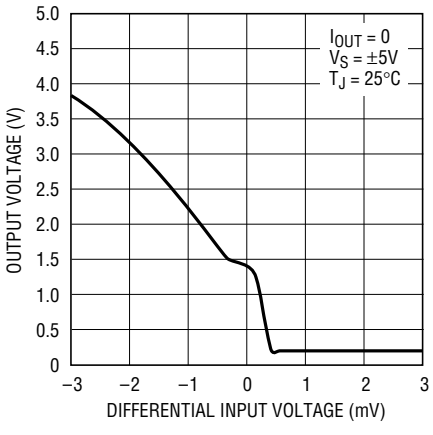
Note 3: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1394 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. Propagation delay (t_{PD}) is measured with the overdrive added to the actual V_{OS}. Differential propagation delay is defined as:

$$\Delta t_{PD} = t_{PD}^+ - t_{PD}^-$$

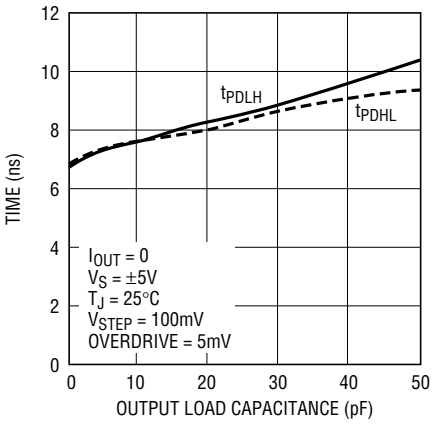
Note 4: Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the LATCH pin is deasserted. Latch setup time (t_{SU}) is the interval in which the input signal must remain stable prior to asserting the latch signal. Latch hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable.

TYPICAL PERFORMANCE CHARACTERISTICS

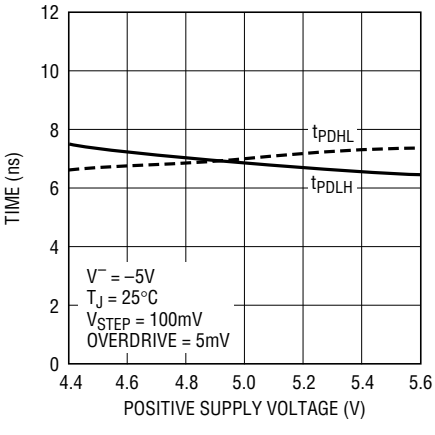
Gain Characteristics



Propagation Delay vs Load Capacitance



Propagation Delay vs Positive Supply Voltage



APPLICATIONS INFORMATION

Common Mode Considerations

The LT1394 is specified for a common mode range of –5V to 3.5V on a ±5V supply or a common mode range of 0V to 3.5V on a single 5V supply. A more general consideration is that the common mode range is 0V below the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criterion for common mode limit is that the output still responds correctly to a small differential input signal.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

Either input may go above the positive common mode limit without damaging the comparator as long as it does not go far enough above the positive supply to conduct more than 10mA. Functionality will continue if the remaining input stays within the allowed common mode range. There will, however, be an increase in propagation delay as the input signal switches back into the common mode range.

Input Bias Current

Input bias current is measured with the output held at 1.4V. As with any PNP differential input stage, the LT1394 bias current flows out of the device. It will go to zero on an input which is high and double on an input which is low.

LATCH Pin Dynamics

The LATCH pin is intended to retain input data (output latched) when the LATCH pin goes high. The pin will float to a high state when disconnected, so a flow-through condition requires that the LATCH pin be grounded. The LATCH pin is designed to be driven with either a TTL or CMOS output. It has no built-in hysteresis.

High Speed Design Techniques

A substantial amount of design effort has made the LT1394 relatively easy to use. It is much less prone to oscillation than some slower comparators, even with slow input signals. However, as with any high speed comparator, there are a number of problems which may arise because of PC board layout and design. The most common problem involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move with changing internal current levels of the connected devices. This will almost always result in improper operation. In addition, adjacent devices connected through an unbypassed supply can interact with each other through the finite supply impedances. Bypass capacitors furnish a simple solution to this problem by providing a local reservoir of energy at the device, keeping supply impedances low.

Bypass capacitors should be as close as possible to the LT1394. A good high frequency capacitor such as a 0.1µF ceramic is recommended, in parallel with a larger capacitor such as a 4.7µF tantalum.

Poor trace routes and high source impedances are also common sources of problems. Be sure to keep trace lengths as short as possible, and avoid running any output trace adjacent to an input trace to prevent unnecessary coupling. If output traces are longer than a few inches, be sure to terminate them with a resistor to eliminate any reflections that may occur. Resistor values are typically 250Ω to 400Ω. Also, be sure to keep source impedances as low as possible, preferably 1kΩ or less.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	Ultrafast Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of LT1016