INITIAL RELEASE
Final Electrical Specifications

LTC1536

Precision Triple Supply Monitor for PCI Applications

FEATURES

- **Simultaneously Monitors 5V, 3.3V and Adjustable Inputs**
- **Guaranteed Threshold Accuracy: ±0.75%**
- Low Supply Current: 100µA
- Internal Reset Time Delay: 200ms
- Manual Pushbutton Reset Input
- Active Low and Active High Reset Outputs
- Active Low "Soft" Reset Output
- Power Supply Glitch Immunity
- Guaranteed $\overline{\text{Reset}}$ for Either $V_{CC3} \geq 1V$ or $V_{CC5} \geq 1V$
- Meets PCI t_{FAIL} Timing Specifications Rev 2.1
- 8-Pin SO and MSOP Packages

APPLICATIONS

- PCI-Based Systems
- Desktop Computers
- Notebook Computers
- Intelligent Instruments
- Portable Battery-Powered Equipment
- Network Servers

DESCRIPTION

The LTC®1536 is designed for PCI local bus applications with multiple supply voltages that require low power, small size, high speed and high accuracy supply monitoring.

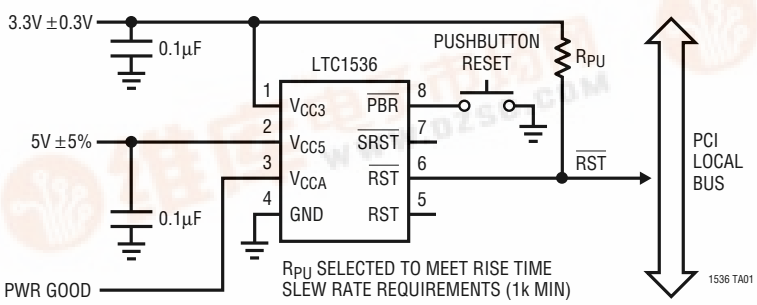
For 3.3V and 5V supplies that are >500mV below spec or for the condition when the 5V supply falls below the 3.3V supply, the LTC1536 has a very fast response time capable of meeting the PCI t_{FAIL} timing specification. Tight 0.75% threshold accuracy and glitch immunity ensure reliable reset operation without false triggering.

The $\overline{\text{RST}}$ output is guaranteed to be in the correct state for V_{CC5} or V_{CC3} down to 1V. The 100µA typical supply current makes the LTC1536 ideal for power-conscious systems.

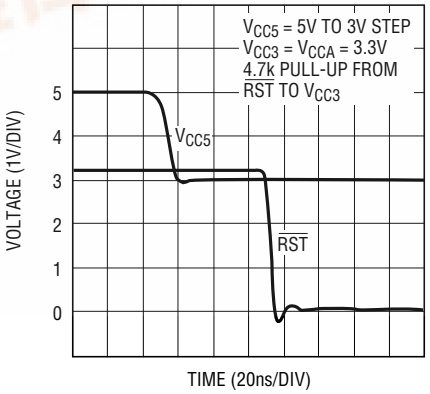
A manual pushbutton reset input provides the ability to generate a very narrow "soft" reset pulse (100µs typ) or a 200ms reset pulse equivalent to a power-on reset. Both $\overline{\text{SRST}}$ and $\overline{\text{RST}}$ outputs are open-drain and can be OR-tied with other reset sources.

TYPICAL APPLICATION

PCI $\overline{\text{RST}}$ Generation



Power Fail Waveform
5V Dropping Below 3.3V by 300mV



ABSOLUTE MAXIMUM RATINGS

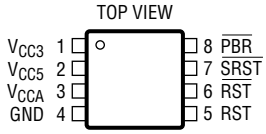
(Notes 1, 2)

Terminal Voltage

V_{CC3}, V_{CC5}, V_{CCA} ..... –0.3V to 7V
$\overline{RST}$, $\overline{SRST}$ ..... –0.3V to 7V
RST ..... –0.3V to V_{CC3} + 0.3V
$\overline{PBR}$ ..... –7V to 7V

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

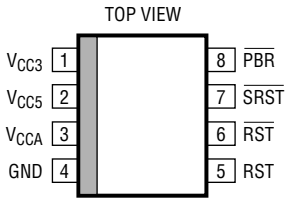
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LTC1536CMS8
MS8 PART NUMBER
LTBV



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1536CS8
S8 PART NUMBER
1536

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC3} = 3.3V, V_{CC5} = 5V, V_{CCA} = V_{CC3}, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT3}	Reset Threshold V_{CC3}		●	2.959	2.985	3.008	V
V_{RT5}	Reset Threshold V_{CC5}		●	4.687	4.725	4.762	V
V_{RTA}	Reset Threshold V_{CCA}		●	0.992	1.000	1.007	V
V_{CC}	V_{CC3} or V_{CC5} Operating Voltage	$\overline{RST}$ in Correct Logic State	●	1		7	V
I_{VCC3}	V_{CC3} Supply Current	$\overline{PBR}$ = V_{CC3}	●		100	200	µA
I_{VCC5}	V_{CC5} Input Current	V_{CC5} = 5V	●		10	20	µA
I_{VCCA}	V_{CCA} Input Current	V_{CCA} = 1V	●	–5	0	5	nA
t_{RST}	Reset Pulse Width	$\overline{RST}$ Low with 10kΩ Pull-Up to V_{CC3}	●	140	200	280	ms
t_{SRST}	Soft Reset Pulse Width	$\overline{SRST}$ Low with 10kΩ Pull-Up to V_{CC3}	●	50	100	200	µs
t_{UV}	V_{CC} Undervoltage Detect to $\overline{RST}$	V_{CC5}, V_{CC3} or V_{CCA} Less than Reset Threshold V_{RT} by 1%			13		µs

ELECTRICAL CHARACTERISTICS

V_{CC3} = 3.3V, V_{CC5} = 5V, V_{CCA} = V_{CC3}, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PBR}	$\overline{PBR}$ Pull-Up Current	$\overline{PBR}$ = 0V	●	3	7	10	µA
V_{IL}	$\overline{PBR}$, $\overline{RST}$ Input Low Voltage		●			0.8	V
V_{IH}	$\overline{PBR}$, $\overline{RST}$ Input High Voltage		●	2			V
t_{PW}	$\overline{PBR}$ Min Pulse Width		●	40			ns
t_{DB}	$\overline{PBR}$ Debounce	Deassertion of $\overline{PBR}$ Input to $\overline{SRST}$ Output ($\overline{PBR}$ Pulse Width = 1µs)	●		20	35	ms
t_{PB}	$\overline{PBR}$ Assertion Time to Reset	$\overline{PBR}$ Held Less Than V_{IL}	●	1.4	2.0	2.8	s
V_{OL}	$\overline{RST}$ Output Voltage Low	I_{SINK} = 5mA	●		0.15	0.4	V
		I_{SINK} = 100µA, V_{CC3} = 1V, V_{CC5} = 0V	●		0.05	0.4	V
		I_{SINK} = 100µA, V_{CC3} = 0V, V_{CC5} = 1V	●		0.05	0.4	V
		I_{SINK} = 100µA, V_{CC3} = 1V, V_{CC5} = 1V	●		0.05	0.4	V
	$\overline{SRST}$ Output Voltage Low	I_{SINK} = 2.5mA	●		0.15	0.4	V
	RST Output Voltage Low	I_{SINK} = 2.5mA	●		0.15	0.4	V
V_{OH}	$\overline{RST}$ Output Voltage High (Note 3)	I_{SOURCE} = 1µA	●	V_{CC3} – 1			V
	$\overline{SRST}$ Output Voltage High (Note 3)	I_{SOURCE} = 1µA	●	V_{CC3} – 1			V
	RST Output Voltage High	I_{SOURCE} = 600µA	●	V_{CC3} – 1			V
t_{PHL}	Propagation Delay $\overline{RST}$ to RST High Input to Low Output	C_{RST} = 20pF			25		ns
t_{PLH}	Propagation Delay $\overline{RST}$ to RST Low Input to High Output	C_{RST} = 20pF			45		ns
t_{FAIL1}	V_{CC5} or V_{CC3} 0.5V Undervoltage to $\overline{RST}$ (Note 4)	V_{CC5} Drops Below 4.25V or V_{CC3} Drops Below 2.5V (Note 5)	●		150	450	ns
t_{FAIL2}	V_{CC5} < (V_{CC3} – 300mV) to $\overline{RST}$ (Note 4)	V_{CC5} Drops Below V_{CC3} By 300mV (Note 6)	●		50	90	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: The output pins $\overline{SRST}$ and $\overline{RST}$ have weak internal pull-ups to V_{CC3} of 6µA. However, external pull-up resistors may be used when faster rise times are required.

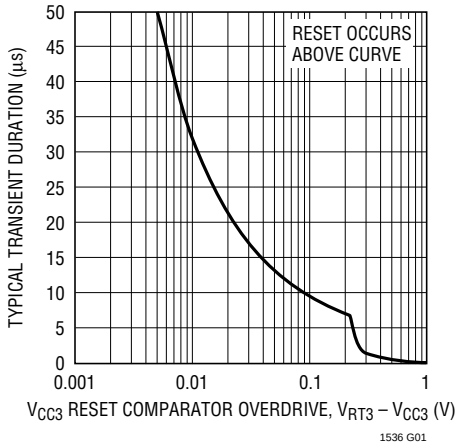
Note 4: Conforms to PCI Local Bus Specification Rev 2.1, Sect. 4.3.2 for t_{FAIL}.

Note 5: V_{CC3} or V_{CC5} falling at 0.1V/µs, time measured from V_{RTX} – 500mV to $\overline{RST}$ at 1.5V.

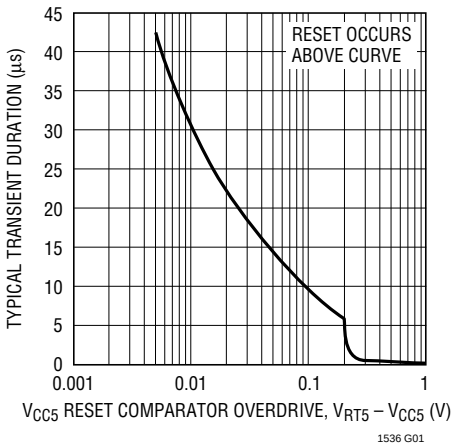
Note 6: V_{CC5} falling from 5V to 3V in ≤ 10ns, time measured from V_{CC5} = (V_{CC3} – 300mV) to $\overline{RST}$ at 1.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

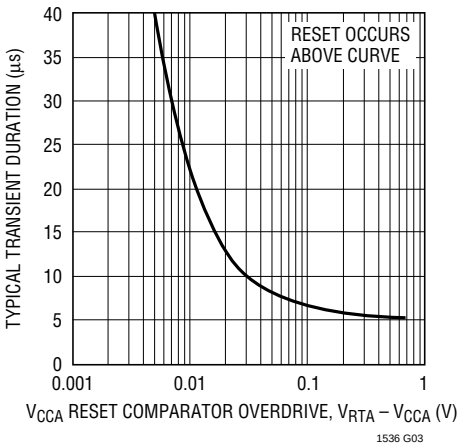
V_{CC3} Typical Transient Duration vs Reset Comparator Overdrive



V_{CC5} Typical Transient Duration vs Reset Comparator Overdrive



V_{CCA} Typical Transient Duration vs Reset Comparator Overdrive



PIN FUNCTIONS

V_{CC3} (Pin 1): 3.3V Sense Input and Power Supply Pin for the IC. Bypass to ground with ≥ 0.1µF ceramic capacitor.

V_{CC5} (Pin 2): 5V Sense Input.

V_{CCA} (Pin 3): 1V Sense, High Impedance Input. If unused it can be tied to either V_{CC3} or V_{CC5}.

GND (Pin 4): Ground.

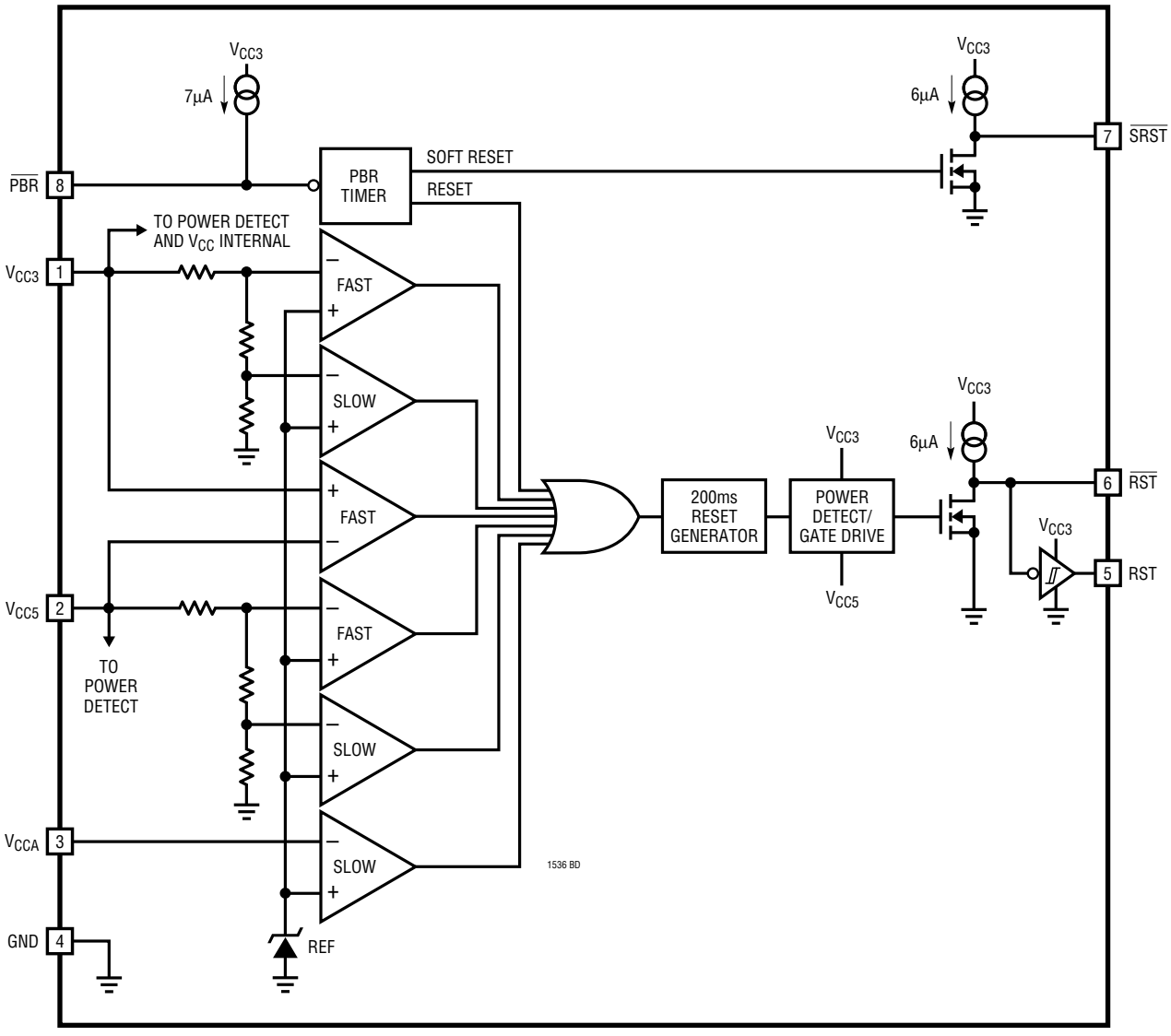
RST (Pin 5): Reset Logic Output. Active high CMOS logic output, drives high to V_{CC3}, buffered compliment of $\overline{RST}$. An external pull-down on the $\overline{RST}$ pin will drive this pin high.

$\overline{RST}$ (Pin 6): Reset Logic Output. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted when one or more of the supplies are below trip thresholds and held for 200ms after all supplies become valid. Also asserted after $\overline{PBR}$ is held low for more than two seconds and for an additional 200ms after $\overline{PBR}$ is released.

$\overline{SRST}$ (Pin 7): "Soft" Reset. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted for 100µs after $\overline{PBR}$ is held low for less than two seconds and released.

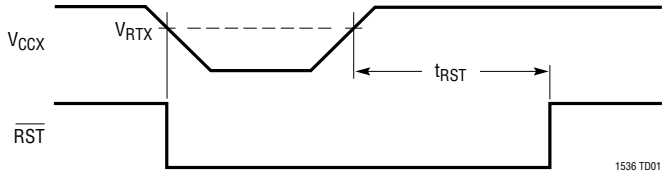
$\overline{PBR}$ (Pin 8): Push-Button Reset. Active low logic input with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. When asserted for less than two seconds, outputs a soft reset 100µs pulse on the $\overline{SRST}$ pin. When $\overline{PBR}$ is asserted for greater than two seconds, the $\overline{RST}$ output is forced low and remains low until 200ms after $\overline{PBR}$ is released.

BLOCK DIAGRAM

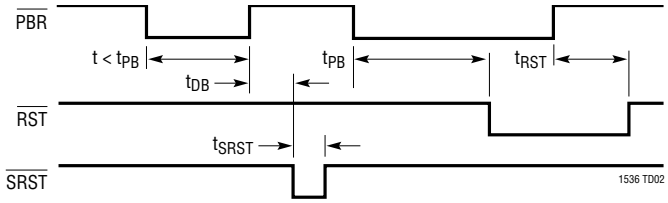


TIMING DIAGRAMS

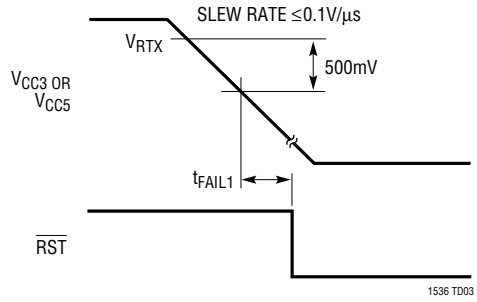
V_{CC} Monitor Timing



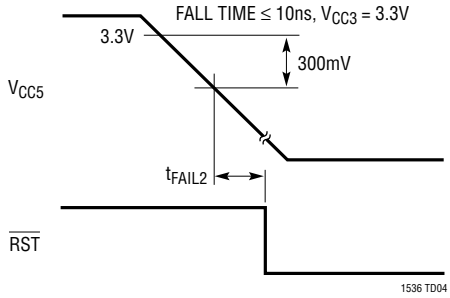
Push-Button Reset Function Timing



t_{FAIL1} Fast Undervoltage Detect



t_{FAIL2} Fast Undervoltage Detect



APPLICATIONS INFORMATION

Operation

The LTC1536 is a low power, high accuracy triple supply monitoring circuit. This reset generator has two basic functions: generation of a reset when power supplies are out of range, and generation of a reset or "soft" reset when the reset button is pushed. The LTC1536 has the added feature that when the reset supplies are grossly undervoltage there is a very short delay from undervoltage detect to assertion of $\overline{RST}$.

Supply Monitoring

All three V_{CC} inputs must be above predetermined thresholds for 200ms before the reset output is released. The LTC1536 will assert reset during power-up, power-down and brownout conditions on any one or more of the V_{CC} inputs.

On power-up, either the V_{CC5} or V_{CC3} pin can power the drive circuits for the $\overline{RST}$ pin. This ensures that $\overline{RST}$ will be low when either V_{CC5} or V_{CC3} reaches 1V. As long as any one of the V_{CC} inputs is below its predetermined threshold, $\overline{RST}$ will stay a logic low. Once all of the V_{CC} inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after 200ms. RST outputs the inverted state of what is seen on $\overline{RST}$.

$\overline{RST}$ is reasserted whenever any one of the V_{CC} inputs drops below its predetermined threshold and remains asserted until 200ms after all of the V_{CC} inputs are above their thresholds.

On power-down, once any of the V_{CC} inputs drops below its threshold, $\overline{RST}$ is held at a logic low. A logic low of 0.4V is guaranteed until both V_{CC3} and V_{CC5} drop below 1V.

Push-Button Reset

The LTC1536 provides a push-button reset input pin. The $\overline{PBR}$ input has an internal pull-up current source to V_{CC3}. If the $\overline{PBR}$ pin is not used it can be left floating.

When the $\overline{PBR}$ is pulled low for less than t_{PB} (≈2 sec), a narrow (100µs typ) soft reset pulse is generated on the $\overline{SRST}$ output pin after the button is released. The push-button circuitry contains an internal debounce counter

APPLICATIONS INFORMATION

which delays the output of the soft reset pulse by typically 20ms. This pin can be OR-tied to the $\overline{RST}$ pin and issue what is called a "soft" reset. The $\overline{SRST}$ thereby resets the microprocessor without interrupting the DRAM refresh cycle. In this manner DRAM information remains undisturbed. Alternatively, $\overline{SRST}$ may be monitored by the processor to initiate a software-controlled reset.

When the $\overline{PBR}$ pin is held low for longer than t_{PB} (≈2 sec), a standard reset is generated. Once the 2-second period has elapsed, a reset signal is produced by the push-button logic, thereby clearing the reset counter. Once the $\overline{PBR}$ pin is released, the reset counter begins counting the reset period (200ms nominal). Consequently, the reset outputs remain asserted for approximately 200ms after the button is released.

Fast Undervoltage for PCI Applications

The LTC1536 is designed for PCI Local Bus applications that require reset to be asserted quickly in response to one or both of the power supply rails (5V and 3.3V) going out of spec. The spec for t_{FAIL} is met with enough margin to give the designer the ability to add follow-on logic as needed by system requirements. The V_{CCA} pin can be used to monitor the "power good" signal and keep reset applied until both supplies are in spec and the power good signal is high.

Glitch Immunity and Fast Undervoltage Detection

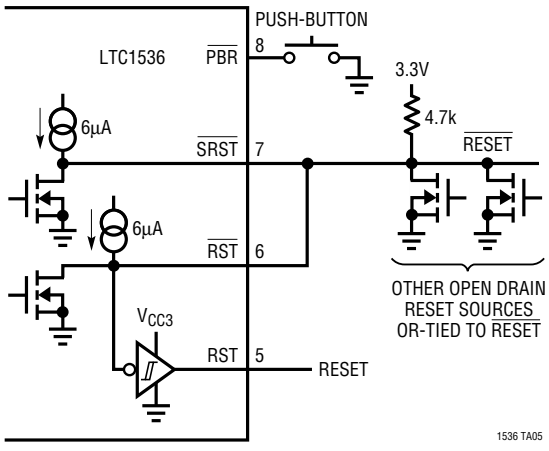
The LTC1536 achieves its high speed characteristics while maintaining glitch immunity by using two sets of comparators. Both the V_{CC5} and V_{CC3} sense inputs each have two comparators set at different thresholds. A slow, very accurate comparator monitors the supply for precision undervoltage detection. In parallel, with a lower threshold, is a very fast comparator that detects when the supply is grossly out of specification.

3V or 5V Power Detect/Gate Drive

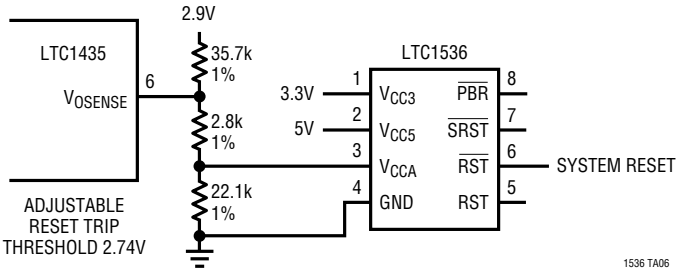
The LTC1536 for the most part is powered internally from the V_{CC3} pin. The exception is at the gate drive of the output FET on the $\overline{RST}$ pin. On the input to this FET is power detect circuitry used to detect and drive the gate from either the 3.3V pin or the 5V pin, whichever pin has the highest potential. This ensures the part pulls the $\overline{RST}$ pin low as soon as either input pin is ≥1V.

TYPICAL APPLICATIONS

$\overline{SRST}$ Tied to $\overline{RST}$ and OR-Tying Other Sources to $\overline{RST}$ to Generate $\overline{Reset}$ and Reset

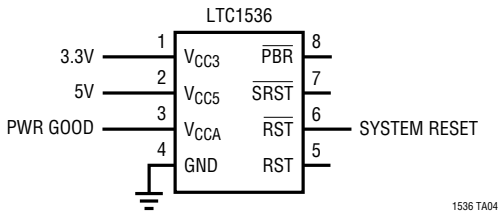


Using V_{CCA} Tied to DC/DC Feedback Divider

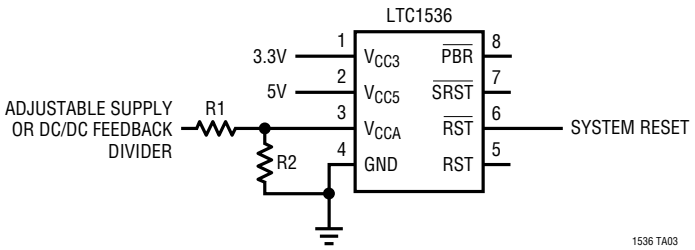


TYPICAL APPLICATIONS

Dual Supply Monitor (3.3V and 5V, V_{CCA} Input Monitoring "Power Good")



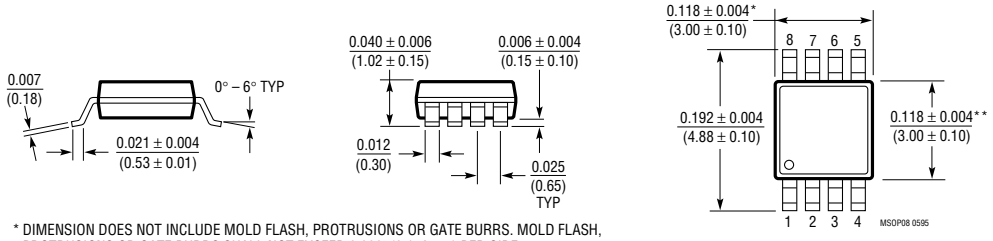
Triple Supply Monitor (3.3V, 5V and Adjustable)



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

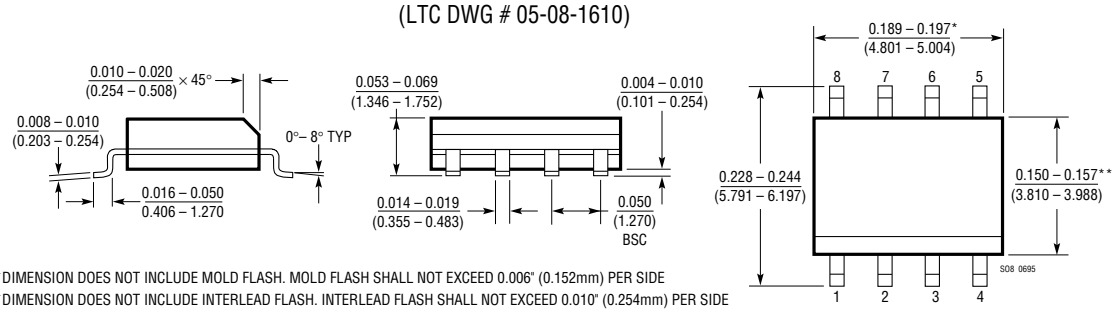
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Push-Button Reset	4.37V/4.62V Threshold
LTC1326	Micropower Precision Triple Supply Monitor	4.725V, 3.118V, 1V Thresholds (±0.75%)