



Very Low Noise, Low Distortion Active RC Quad Universal Filter

December 1998

FEATURES

- Continuous Time—No Clock
- Four 2nd Order Filter Sections, 20kHz to 300kHz Center Frequency
- Butterworth, Chebyshev, Elliptic or Equiripple Delay Response
- Lowpass, Bandpass, Highpass Responses
- 99dB Typical S/N, $\pm 5V$ Supply ($Q = 1$)
- 93dB Typical S/N, Single 5V Supply ($Q = 1$)
- Rail-to-Rail Input and Output Voltages
- DC Accurate to 3mV (Typ)
- $\pm 0.5\%$ Typical Center Frequency Accuracy
- “Zero-Power” Shutdown Mode
- Single or Dual Supply, 5V to 10V Total
- Resistor-Programmable f_0 , Q , Gain

APPLICATIONS

- High Resolution Systems (14 Bits to 18 Bits)
- Antialiasing/Reconstruction Filters
- Data Communications, Equalizers
- Dual or I-and-Q Channels (Two Matched 4th Order Filters in One Package)
- Linear Phase Filtering
- Replacing LC Filter Modules

DESCRIPTION

The LTC[®]1562-2 is a low noise, low distortion continuous time filter with rail-to-rail inputs and outputs, optimized for a center frequency (f_0) of 20kHz to 300kHz. It contains four independent 2nd order filter blocks, which can be cascaded in any combination, such as one 8th order or two 4th order filters. Each block's response is programmed with three external resistors for center frequency, Q and gain, using simple design formulas. Each 2nd order block provides lowpass and bandpass outputs. Highpass response is available if an external capacitor replaces one of the resistors. Allpass and elliptic responses can also be realized.

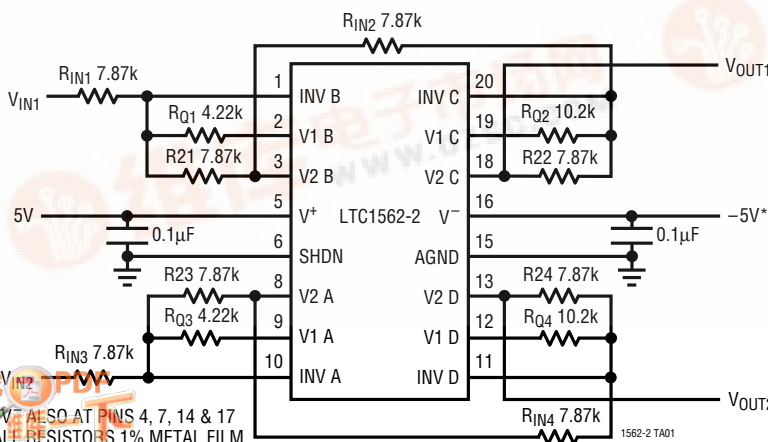
The LTC1562-2 is designed for applications where dynamic range is important. For example, by cascading 2nd order sections in pairs, the user can configure the IC as a dual 4th order Butterworth lowpass filter with over 90dB signal-to-noise ratio from a single 5V power supply. Low level signals can exploit the built-in gain capability of the LTC1562-2. Varying the gain of a section can achieve a dynamic range as high as 114dB with a $\pm 5V$ supply.

Other cutoff frequency ranges can be provided upon request. Please contact LTC Marketing.

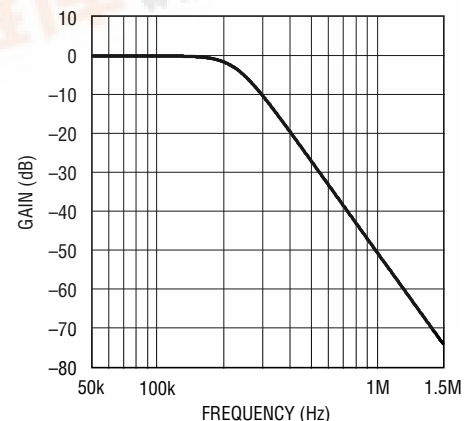
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TYPICAL APPLICATION

Dual 4th Order 200kHz Butterworth Lowpass Filter



Amplitude Response



1562-2 TA02

LTC1562-2

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 11V

Maximum Input Voltage

at Any Pin ($V^- - 0.3V$) $\leq V \leq$ ($V^+ + 0.3V$)

Storage Temperature Range -65°C to 150°C

Operating Temperature Range

LTC1562C-2 0°C to 70°C

LTC1562I-2 -40°C to 85°C

Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW INV B 1, V1 B 2, V2 B 3, V- 4, V+ 5, SHDN 6, V- 7, V2 A 8, V1 A 9, INV A 10, INV D 11, V1 D 12, V2 D 13, V- 14, AGND 15, V- 16, V- 17, V2 C 18, V1 C 19, INV C 20 G PACKAGE 20-LEAD PLASTIC SSOP *G PACKAGE PINS 4, 7, 14, 17 ARE SUBSTRATE/SHIELD CONNECTIONS AND MUST BE TIED TO V- T_{JMAX} = 150°C, θ_{JA} = 136°C/W	ORDER PART NUMBER
	LTC1562CG-2 LTC1562IG-2

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, outputs unloaded, $T_A = 25^\circ\text{C}$, SHDN pin to logic "low", unless otherwise noted. AC specs are for a single 2nd order section, $R_{IN} = R_2 = 10.4k \pm 0.1\%$, $R_Q = 9.09k \pm 0.1\%$, $f_0 = 175kHz$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _S	Total Supply Voltage			4.75		10.5	V
I _S	Supply Current	V _S = ±2.375V, R _L = 5k, C _L = 30pF, Outputs at 0V			21	23.5	mA
		V _S = ±5V, R _L = 5k, C _L = 30pF, Outputs at 0V			22.5	25	mA
		V _S = ±2.375V, R _L = 5k, C _L = 30pF, Outputs at 0V	●			28	mA
		V _S = ±5V, R _L = 5k, C _L = 30pF, Outputs at 0V	●			30	mA
	Output Voltage Swing, V2 Outputs	V _S = ±2.375V, R _L = 5k, C _L = 30pF	●	4.2	4.6		V _{P-P}
		V _S = ±5V, R _L = 5k, C _L = 30pF	●	9.3	9.8		V _{P-P}
	Output Voltage Swing, V1 Outputs	V _S = ±2.375V, R _L = 5k, C _L = 30pF, f = 250kHz			4.5		V _{P-P}
		V _S = ±5V, R _L = 5k, C _L = 30pF, f = 250kHz		8.4	9.7		V _{P-P}
V _{OS}	DC Offset Magnitude, V2 Outputs	V _S = ±2.375V, Input at AGND Voltage			3	17	mV
		V _S = ±5V, Input at AGND Voltage			3	17	mV
	DC AGND Reference Point	V _S = Single 5V Supply			2.5		V
	Center Frequency (f ₀) Error (Notes 2, 3)	V _S = ±5V, V2 Output Has R _L = 5k, C _L = 30pF			0.5	1.7	%
H _L	Lowpass Passband Gain at V2 Output	V _S = ±2.375V, f _{IN} = 10kHz, V2 Output Has R _L = 5k, C _L = 30pF	●	0	+0.05	+0.1	dB
	Q Accuracy	V _S = ±2.375V, V2 Output Has R _L = 5k, C _L = 30pF			+2		%
	Wideband Output Noise	V _S = ±2.375V, BW = 400kHz, Input AC GND			39		μV _{RMS}
		V _S = ±5V, BW = 400kHz, Input AC GND			39		μV _{RMS}
	Input-Referred Noise, Gain = 100	BW = 400kHz, f ₀ = 200kHz, Q = 1, Input AC GND			7.3		μV _{RMS}

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, outputs unloaded, $T_A = 25^\circ C$, SHDN pin to logic “low”, unless otherwise noted. AC specs are for a single 2nd order section, $R_{IN} = R_2 = 10.4k \pm 0.1\%$, $R_Q = 9.09k \pm 0.1\%$, $f_0 = 175kHz$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
THD	Total Harmonic Distortion, V2 Output	$f_{IN} = 20kHz$, $2.8V_{P-P}$, V1 and V2 Outputs Have $R_L = 5k$, $C_L = 30pF$		-100		dB
		$f_{IN} = 20kHz$, $9V_{P-P}$, V1 and V2 Outputs Have $R_L = 5k$, $C_L = 30pF$		-82		dB
	Shutdown Supply Current	SHDN Pin to V^+ SHDN Pin to V^+ , $V_S = \pm 2.375V$		1.5 1.0	15	μA μA
	Shutdown-Input Logic Threshold			2.5		V
	Shutdown-Input Bias Current	SHDN Pin to 0V		-10	-20	μA
	Shutdown Delay	SHDN Pin Steps from 0V to V^+		20		μs
	Shutdown Recovery Delay	SHDN Pin Steps from V^+ to 0V		100		μs
	Inverting Input Bias Current, Each Biquad			5		pA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: f_0 change from $\pm 5V$ to ± 2.375 supplies is -0.2% typical, f_0 temperature coefficient, $-40^\circ C$ to $85^\circ C$, is $25ppm/^\circ C$ typical.

Note 3: This data sheet reflects initial production limits that will be tightened in the final data sheet.

PIN FUNCTIONS

Power Supply Pins: The V^+ and V^- pins should be bypassed with $0.1\mu F$ capacitors to an adequate analog ground or ground plane. These capacitors should be connected as closely as possible to the supply pins. Pins 4, 7, 14 and 17 are internally connected to V^- (Pin 16) and should also be tied to the same point as Pin 16 for best shielding. Low noise linear supplies are recommended. Switching supplies are not recommended as they will lower the filter dynamic range.

Analog Ground (AGND): The AGND pin is the midpoint of a resistive voltage divider, developing a potential halfway between the V^+ and V^- pins, with an equivalent series resistance nominally $7k$. This serves as an internal ground reference. Filter performance will reflect the quality of the analog signal ground and an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, the AGND pin should be connected to the ground plane. For single supply operation, the AGND pin should be bypassed to the

ground plane with at least a $0.1\mu F$ capacitor (at least $1\mu F$ for best AC performance).

Shutdown (SHDN): When the SHDN input goes high or is open-circuited, the LTC1562-2 enters a “zero-power” shutdown state and only junction leakage currents flow. The AGND pin and the amplifier outputs (see Figure 1) assume a high impedance state and the amplifiers effectively disappear from the circuit. (If an input signal is applied to a complete filter circuit while the LTC1562-2 is in shutdown, some signal will normally flow to the output through passive components around the inactive op amps.)

A small pull-up current source at the SHDN input *defaults the LTC1562-2 to the shutdown state if the SHDN pin is left floating*. Therefore, the user *must* connect the SHDN pin to a logic “low” (0V for $\pm 5V$ supplies, V^- for 5V total supply) for normal operation of the LTC1562-2. (This convention permits true “zero-power” shutdown since not even the driving logic must deliver current while the part is in shutdown.)

PIN FUNCTIONS

INVA, INVB, INVC, INV D: Each of the INV pins is a virtual-ground summing point for the corresponding 2nd order section. For each section, all three external components Z_{IN} , R_2 , R_Q connect to the INV pin as shown in Figure 1 and described further in the Applications Information. Note that the INV pins are sensitive internal nodes of the filter and will readily receive any unintended signals that are capacitively coupled into them. Capacitance to the INV nodes will also affect the frequency response of the filter sections. For these reasons, printed circuit connections to the INV pins must be kept as short as possible, less than one inch (2.5cm) total and surrounded by a ground plane.

V1 A, V1 B, V1 C, V1 D: Output Pins. Provide a bandpass, highpass or other response depending on external circuitry (see Applications Information section). Each V1 pin

also connects to the R_Q resistor of the corresponding 2nd order filter section (see Figure 1 and Applications Information). Each output is designed to drive a nominal net load of 4k Ω and 30pF, which includes the loading due to the external R_Q . Distortion performance improves when the outputs are loaded as lightly as possible.

V2 A, V2 B, V2 C, V2 D: Output Pins. Provide a lowpass, bandpass or other response depending on external circuitry (see Applications Information section). Each V2 pin also connects to the R_2 resistor of the corresponding 2nd order filter section (see Figure 1 and Applications Information). Each output is designed to drive a nominal net load of 4k Ω and 30pF, which includes the loading due to the external R_2 . Distortion performance improves when the outputs are loaded as lightly as possible.

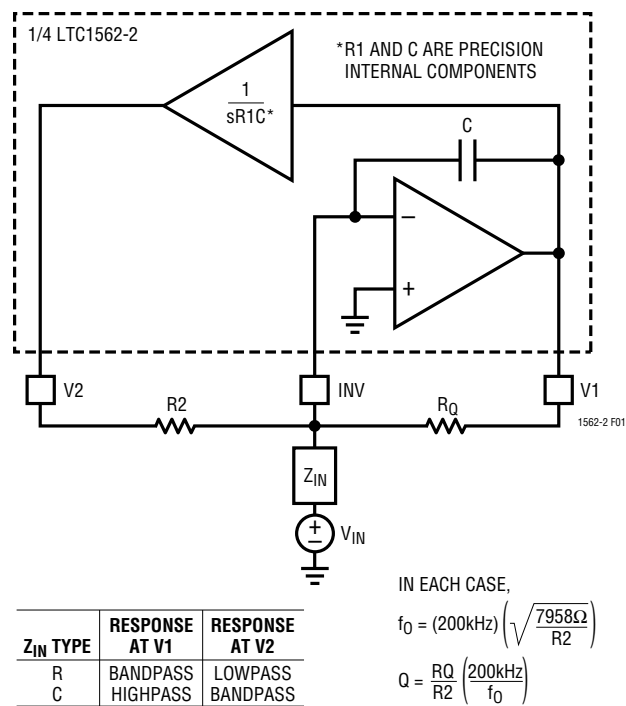


Figure 1. Equivalent Circuit of a Single 2nd Order Section (Inside Dashed Line) Shown in Typical Connection. Form of Z_{IN} Determines Response Types at the Two Outputs (See Table)

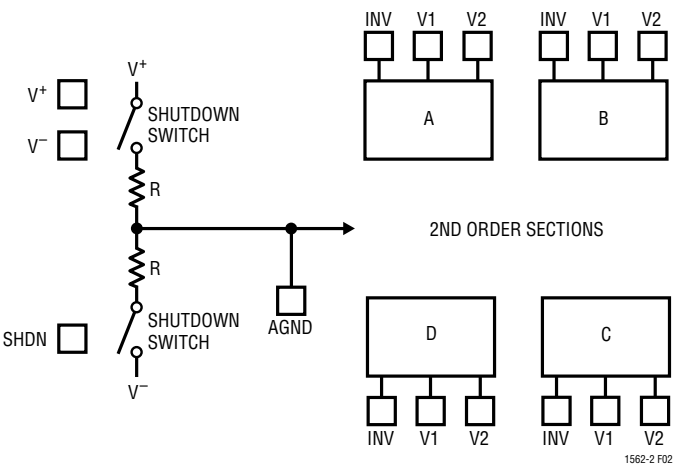


Figure 2. Overall Block Diagram Showing Four 3-Terminal 2nd Order Sections

APPLICATIONS INFORMATION

Functional Description

The LTC1562-2 contains four matched, 2nd order, 3-terminal universal continuous-time filter blocks, each with a virtual-ground input node (INV) and two rail-to-rail outputs (V1, V2). In the most basic application, one such block and three external resistors provide 2nd order lowpass and bandpass responses simultaneously (Figure 1, with a resistor for Z_{IN}). The three external resistors program f_0 , Q and gain. A combination of internal precision components and external resistor R2 sets the center frequency f_0 of each 2nd order block. The LTC1562-2 is trimmed at manufacture so that f_0 will be $200\text{kHz} \pm 0.5\%$ if the external resistor R2 is exactly 7958Ω . The LTC1562-2 is a higher frequency, pin compatible variant of the LTC1562, with different internal R and C values and higher speed amplifiers.

However, lowpass/bandpass filtering is only one specific application for the 2nd order building blocks in the LTC1562-2. Highpass response results if the external impedance Z_{IN} in Figure 1 becomes a capacitor C_{IN} (whose value sets only gain, not critical frequencies) as described below. Responses with zeroes (e.g., elliptic or notch responses) are available by feedforward connections with multiple 2nd order blocks (see Typical Applications). Moreover, the virtual-ground input gives each 2nd order section the built-in capability for analog operations such as gain (preamplification), summing and weighting of multiple inputs, or accepting current or charge signals directly. **These Operational Filter™ frequency-selective building blocks are nearly as versatile as operational amplifiers.**

Setting f_0 , Q and Gain

Standard all-pole transfer functions characterize the response of each 2nd order filter section. The responses from V_{IN} in Figure 1 to the V2 and V1 outputs, with a resistor R_{IN} for Z_{IN} , are, respectively:

$$H_{LP}(s) = \frac{-H_L \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

$$H_{BP}(s) = \frac{-H_B (\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

The external resistors R_2 , R_{IN} and R_Q set the filter parameters $\omega_0 = 2\pi f_0$, Q, H_L and H_B as follows:

$$f_0 = \frac{1}{2\pi(C)\sqrt{(R_1)(R_2)}} = \left(\sqrt{\frac{7958\Omega}{R_2}} \right) (200\text{kHz})$$

$$\text{or, } R_2 = \left(\frac{200\text{kHz}}{f_0} \right)^2 (7958\Omega)$$

$$Q = \frac{R_Q}{\sqrt{(R_1)(R_2)}} \quad H_L = \frac{R_2}{R_{IN}} \quad H_B = \frac{R_Q}{R_{IN}}$$

Note that $R_1 (= 7958\Omega)$ and $C (= 100\text{pF})$ are internal to the LTC1562-2 while R_2 , R_{IN} and R_Q are external. The usual design procedure is to first determine R_2 from the required f_0 , then determine R_Q to set Q once R_2 is known, and finally determine R_{IN} to set gain.

The f_0 range is approximately 20kHz to 300kHz, limited mainly by the magnitudes of the external resistors required. As shown above, R_2 varies with the inverse square of f_0 . This relationship desensitizes f_0 to R_2 's tolerance (by a factor of 2 incrementally), but it also implies that R_2 has a wider range than f_0 . (R_Q and R_{IN} also tend to scale with R_2 .) At high f_0 these resistors fall below 4k, heavily loading the outputs of the LTC1562-2 and leading to increased THD and other effects. At the other extreme, a lower f_0 limit of 20kHz reflects an arbitrary upper resistor limit of 1M. The LTC1562-2's MOS input circuitry can accommodate higher resistor values than this, but junction leakage current from the input protection circuitry may cause DC errors.

The 2nd order transfer functions $H_{LP}(s)$, $H_{BP}(s)$ and $H_{HP}(s)$ (below) are all inverting so that, for example, at DC the lowpass gain is $-H_L$. If two such sections are cascaded, these phase inversions cancel. Thus, the filter in the application schematic on the first page of this data sheet

APPLICATIONS INFORMATION

is a dual DC preserving, noninverting, rail-to-rail lowpass filter, approximating two “straight wires with frequency selectivity.”

Highpass Option

If Z_{IN} in Figure 1 becomes a capacitor of value C_{IN} , then a standard all-pole highpass response becomes available between V_{IN} and the V1 output.

$$H_{HP}(s) = \frac{-H_H s^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

Here, the passband gain is $H_H = C_{IN}/C$ where C is the internal capacitance, 100pF. The expressions for f_0 and Q remain as above.

Two Bandpass Options

There are two distinct ways to obtain a bandpass response $H_{BP}(s)$ from the LTC1562-2. When Z_{IN} in Figure 1 is a resistor of value R_{IN} , the V1 output has a bandpass response from V_{IN} . Alternatively, with an input capacitor C_{IN} for Z_{IN} , the V1 output has a highpass response as described above, but simultaneously the V2 output now has a bandpass response, with the same $H_{BP}(s)$ form as above. The bandpass gain parameter becomes $H_B = (R_Q/R_1)(C_{IN}/100\text{pF})$ where again $R_1 = 7958\Omega$. f_0 and Q are controlled by R_2 and R_Q as always.

Relative Signal Swings

The signal swings in each 2nd order section must be scaled so that neither output overloads (saturates), even if it is not used as a signal output. (Filter literature often calls this the “dynamics” issue.) For an LTC1562-2 section as in Figure 1, magnitudes of the two outputs V2 and V1, at a frequency $\omega = 2\pi f$, have the ratio:

$$\frac{|V_2(j\omega)|}{|V_1(j\omega)|} = \frac{(200\text{kHz})}{f}$$

Thus an input frequency above or below 200kHz produces larger output amplitude at V1 or V2, respectively. When an unused output has a larger signal swing than the output of interest, the section’s gain or input amplitude must be scaled to avoid overdriving the unused output. The LTC1562-2 can still be used with high performance in such situations as long as this constraint is followed.

The following cases are the most convenient because the relative-signal-swing issue does not arise: the unused output’s swing is naturally the lower of the two.

Lowpass response (resistor input, V2 output) with $f_0 < 200\text{kHz}$

Bandpass response (capacitor input, V2 output) with $f_0 < 200\text{kHz}$

Bandpass response (resistor input, V1 output) with $f_0 > 200\text{kHz}$

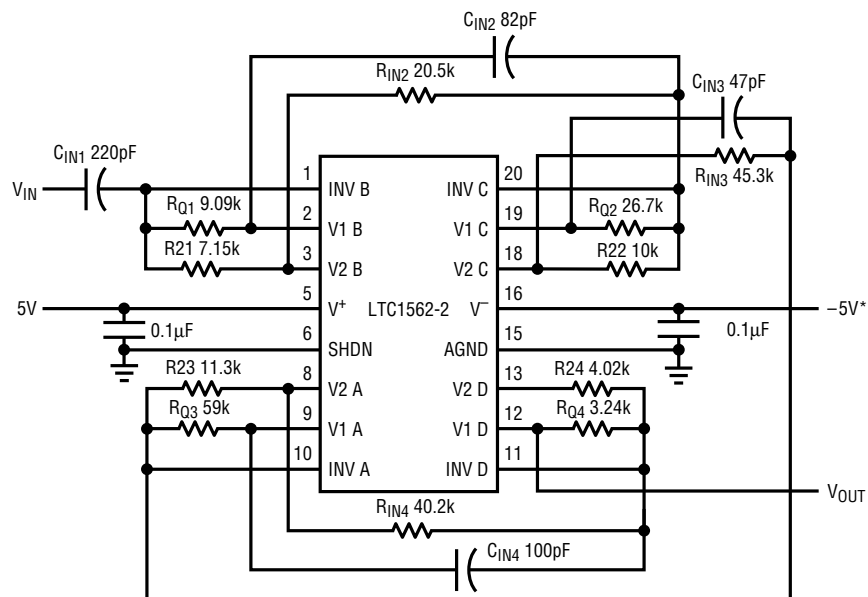
Highpass response (capacitor input, V1 output) with $f_0 > 200\text{kHz}$

Low Level or Wide Range Input Signals

The LTC1562-2 contains a built-in capability for low noise amplification of low level signals. The Z_{IN} impedance in each 2nd order section controls the block’s gain. When set for unity passband gain, a 2nd order section can deliver an output signal 99dB above the noise level. If low level inputs require further dynamic range, reducing the value of Z_{IN} boosts the signal gain while reducing the input-referred noise. This feature can increase the SNR for low level signals. Varying or switching Z_{IN} is also an efficient way to effect automatic gain control (AGC). From a system viewpoint, this technique boosts the ratio of maximum signal to minimum noise, for a typical 2nd order lowpass response ($Q = 1$, $f_0 = 200\text{kHz}$), to 114dB.

TYPICAL APPLICATIONS

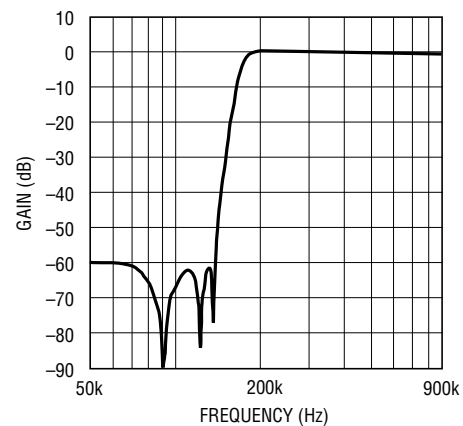
175kHz 8th Order Elliptic Highpass Filter



*V⁻ ALSO AT PINS 4, 7, 14 & 17
ALL RESISTORS 1% METAL FILM
ALL CAPACITORS 5% STANDARD VALUES

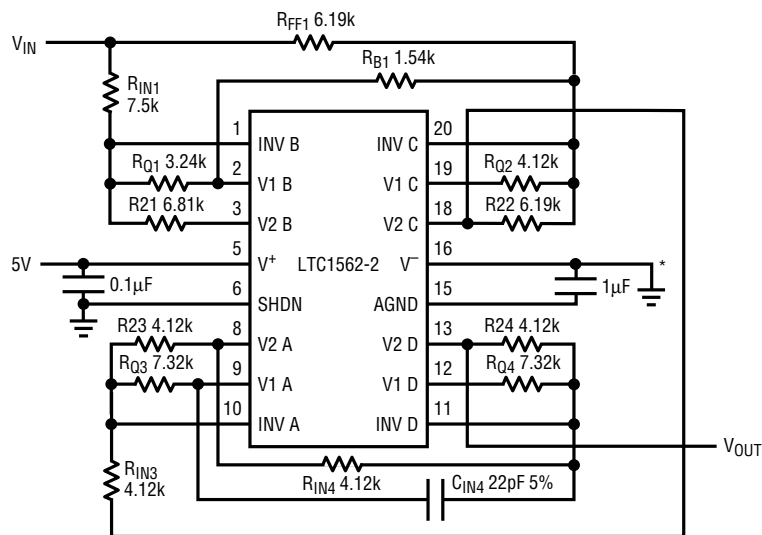
1562-2 TA03a

Amplitude Response



1562-2 TA03b

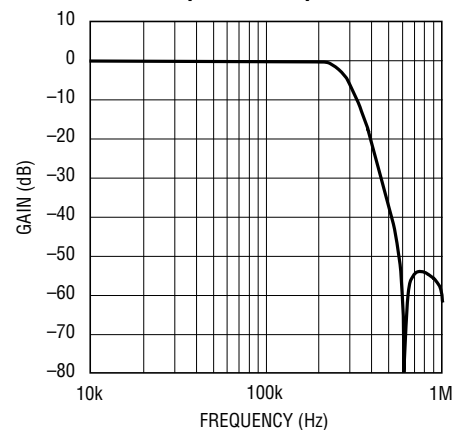
256kHz Linear Phase 6th Order Lowpass Filter, Single Supply



*GROUND ALSO AT PINS 4, 7, 14 & 17
ALL RESISTORS 1% METAL FILM

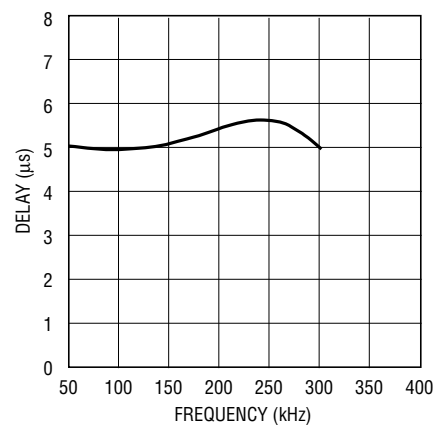
1562-2 TA04a

Amplitude Response



1562-2 TA04b

Group Delay Response

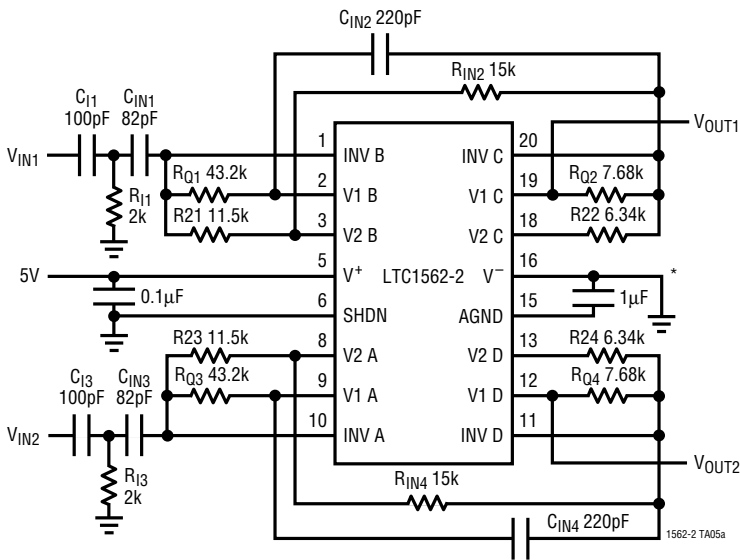


1562-2 TA04c

LTC1562-2

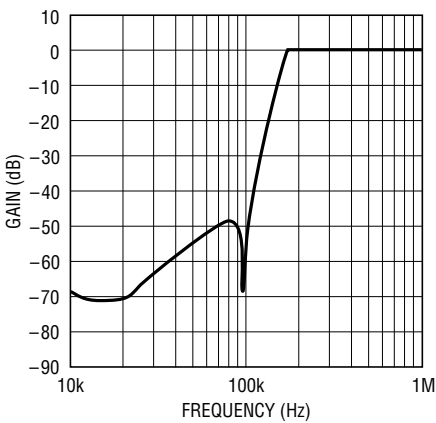
TYPICAL APPLICATIONS

Dual 5th Order 170kHz Elliptic Highpass Filter, Single 5V Supply



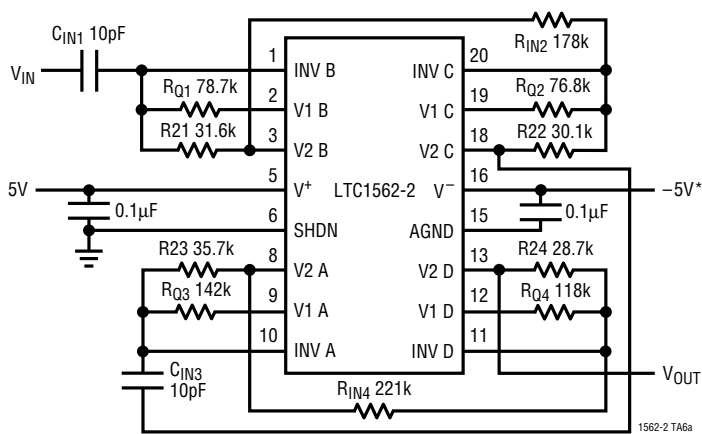
*GROUND ALSO AT PINS 4, 7, 14 & 17

Amplitude Response



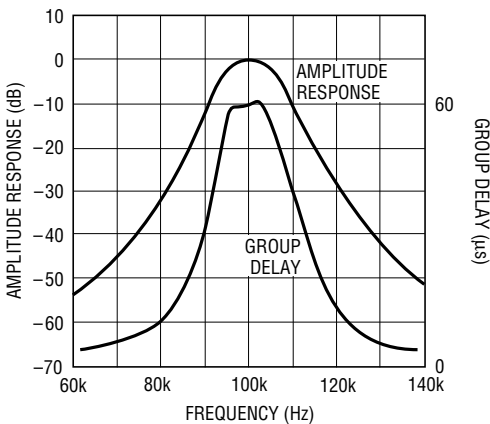
1562-2 TA05b

100kHz 8th Order Bandpass Linear Phase, -3dB BW = f_{CENTER}/10



*V- ALSO AT PINS 4, 7, 14 & 17

Frequency Response



1562-2 TA06b

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1068	Quad 2-Pole Switched Capacitor Building Block	Clock Tuned
LTC1560-1	5-Pole Elliptic Lowpass, f _C = 1MHz/0.5MHz	No External Components, S08
LTC1562	Quad 2-Pole Active RC, 10kHz to 150kHz	Same Pinout as LTC1562-2