LINEAR TECHNOLOGY

LT1630/LT1631

30MHz, 10V/μs, Dual/Quad Rail-to-Rail Input and Output Precision Op Amps

February 1998

FEATURES

- **Gain-Bandwidth Product: 30MHz**
- **Slew Rate: 10V/μs**
- **Low Supply Current per Amplifier: 3.5mA**
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Input Offset Voltage, Rail-to-Rail: 525μV Max
- Input Offset Current: 150nA Max
- Input Bias Current: 1000nA Max
- Open-Loop Gain: 1000V/mV Min
- Low Input Noise Voltage: 6nV/√Hz Typ
- Wide Supply Range: 2.7V to ±15V
- Large Output Drive Current: 70mA
- Dual in 8-Pin PDIP and SO Packages
- Quad in Narrow 14-Pin SO Package

APPLICATIONS

- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Driving A/D Converters
- Low Voltage Signal Processing
- Battery-Powered Systems

DESCRIPTION

The LT®1630/LT1631 are dual/quad, rail-to-rail input and output op amps with a 30MHz gain-bandwidth product and a 10V/μs slew rate.

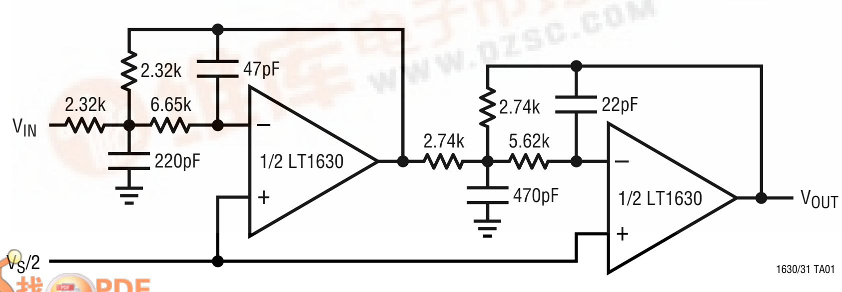
The LT1630/LT1631 have excellent DC precision over the full range of operation. Input offset voltage is typically less than 150μV and the minimum open-loop gain of one million into a 10k load virtually eliminates all gain error. To maximize common mode rejection, the LT1630/LT1631 employ a patented trim technique for both input stages, one at the negative supply and the other at the positive supply, that gives a typical CMRR of 106dB over the full input range.

The LT1630/LT1631 maintain their performance for supplies from 2.7V to 36V and are specified at 3V, 5V and ±15V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output. The output delivers load currents in excess of 50mA.

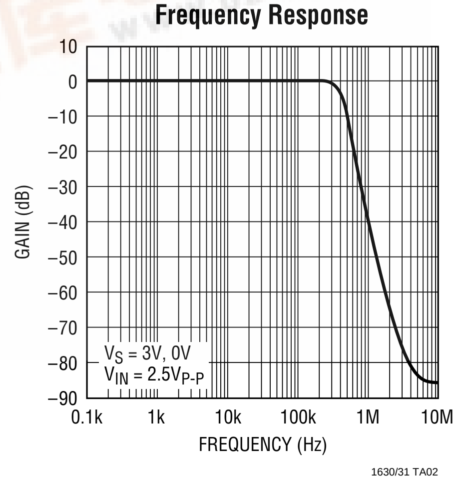
The LT1630 is available in 8-pin PDIP and SO packages with the standard dual op amp pinout. The LT1631 features the standard quad op amp configuration and is available in a 14-pin plastic SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and performance.

TYPICAL APPLICATION

Single Supply, 400kHz, 4th Order Butterworth Filter



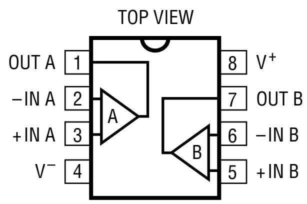
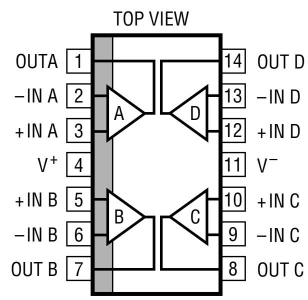
Frequency Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current .... ±10mA
Output Short-Circuit Duration (Note 1) .... Continuous
Operating Temperature Range (Note 3) . −40°C to 85°C
Specified Temperature Range .... 0°C to 70°C
Junction Temperature .... 150°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8) T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)	LT1630CN8 LT1630CS8 **S8 PART MARKING** 1630	 S PACKAGE 14-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 150°C/W	LT1631CS

Consult factory for Military and Industrial grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		150 150	525 525	µV µV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V^-$ to V^+		150	525	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Note 4)		200	950	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	0 −1000	540 −540	1000 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		1080	2000	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4) $V_{CM} = V^-$ (Note 4)		25 25	300 300	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		20 20	150 150	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		40	300	nA
	Input Noise Voltage	0.1Hz to 10Hz		300		nV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz		6		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz		0.9		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			5		pF
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 300mV to 4.7V, R_L = 10k V_S = 3V, V_O = 300mV to 2.7V, R_L = 10k	500 400	3500 2000		V/mV V/mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+		79 75	90 86		dB dB
	CMRR Match (Channel-to-Channel) (Note 4)	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+		72 67	96 88		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 12V, V_{CM} = V_O = 0.5V		87	105		dB
	PSRR Match (Channel-to-Channel) (Note 4)	V_S = 2.7V to 12V, V_{CM} = V_O = 0.5V		80	107		dB
	Minimum Supply Voltage (Note 8)	V_{CM} = V_O = 0.5V			2.6	2.7	V
V_{OL}	Output Voltage Swing Low (Note 5)	No Load I_{SINK} = 0.5mA I_{SINK} = 25mA, V_S = 5V I_{SINK} = 20mA, V_S = 3V			14 31 600 500	30 60 1200 1000	mV mV mV mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 20mA, V_S = 5V I_{SOURCE} = 15mA, V_S = 3V			15 42 900 680	40 80 1800 1400	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V		±20 ±15	±41 ±30		mA mA
I_S	Supply Current per Amplifier				3.5	4.4	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz		15	30		MHz
SR	Slew Rate (Note 7)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V V_S = 3V, A_V = –1, R_L = Open		4.6 4.2	9.2 8.5		V/μs V/μs

0°C < T_A < 70°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ – 0.1V V_{CM} = V^- + 0.2V	● ●		175 175	700 700	μV μV
V_{OS} TC	Input Offset Voltage Drift (Note 2)	 V_{CM} = V^+ – 0.1V	● ●		2.5 2.5		μV/°C μV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		175	750	μV
	Input Offset Voltage Match (Channel-to-Channel)	V_{CM} = V^- + 0.2V, V^+ – 0.1V (Note 4)	●		200	1200	μV
I_B	Input Bias Current	V_{CM} = V^+ – 0.1V V_{CM} = V^- + 0.2V	● ●	0 –1100	585 –585	1100 0	nA nA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		1170	2200	nA
	Input Bias Current Match (Channel-to-Channel)	V_{CM} = V^+ – 0.1V (Note 4) V_{CM} = V^- + 0.2V (Note 4)	● ●		25 25	340 340	nA nA
I_{OS}	Input Offset Current	V_{CM} = V^+ – 0.1V V_{CM} = V^- + 0.2V	● ●		20 20	170 170	nA nA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		40	340	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 300mV to 4.7V, R_L = 10k V_S = 3V, V_O = 300mV to 2.7V, R_L = 10k	● ●	450 350	3500 2000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- + 0.2V to V^+ – 0.1V V_S = 3V, V_{CM} = V^- + 0.2V to V^+ – 0.1V	● ●	75 71	89 83		dB dB
	CMRR Match (Channel-to-Channel) (Note 4)	V_S = 5V, V_{CM} = V^- + 0.2V to V^+ – 0.1V V_S = 3V, V_{CM} = V^- + 0.2V to V^+ – 0.1V	● ●	70 65	90 85		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 12V, V_{CM} = V_O = 0.5V	●	82	101		dB
	PSRR Match (Channel-to-Channel) (Note 4)	V_S = 3V to 12V, V_{CM} = V_O = 0.5V	●	78	102		dB

ELECTRICAL CHARACTERISTICS

0°C < T_A < 70°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Minimum Supply Voltage (Note 8)	V_{CM} = V_O = 0.5V	●		2.6	2.7	V
V_{OL}	Output Voltage Swing Low (Note 5)	No Load	●		17	40	mV
		I_{SINK} = 0.5mA	●		36	80	mV
		I_{SINK} = 25mA, V_S = 5V	●		700	1400	mV
		I_{SINK} = 20mA, V_S = 3V	●		560	1200	mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load	●		16	40	mV
		I_{SOURCE} = 0.5mA	●		50	100	mV
		I_{SOURCE} = 15mA, V_S = 5V	●		820	1600	mV
		I_{SOURCE} = 10mA, V_S = 3V	●		550	1100	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	±18	±36		mA
		V_S = 3V	●	±13	±25		mA
I_S	Supply Current per Amplifier		●		4.0	5.1	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	●	14	28		MHz
SR	Slew Rate (Note 7)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V	●	4.2	8.3		V/µs
		V_S = 3V, A_V = –1, R_L = Open	●	3.9	7.7		V/µs

–40°C < T_A < 85°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ – 0.1V	●		250	775	µV
		V_{CM} = V^- + 0.2V	●		250	775	µV
V_{OS} TC	Input Offset Voltage Drift (Note 2)		●		2.5		µV/°C
		V_{CM} = V^+ – 0.1V	●		2.5		µV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		200	750	µV
	Input Offset Voltage Match (Channel-to-Channel)	V_{CM} = V^- + 0.2V, V^+ (Note 4)	●		210	1500	µV
I_B	Input Bias Current	V_{CM} = V^+ – 0.1V	●	0	650	1300	nA
		V_{CM} = V^- + 0.2V	●	–1300	–650	0	nA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		1300	2600	nA
	Input Bias Current Match (Channel-to-Channel)	V_{CM} = V^+ – 0.1V (Note 4)	●		25	390	nA
		V_{CM} = V^- + 0.2V (Note 4)	●		25	390	nA
I_{OS}	Input Offset Current	V_{CM} = V^+ – 0.1V	●		25	195	nA
		V_{CM} = V^- + 0.2V	●		25	195	nA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		50	390	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 300mV to 4.7V, R_L = 10k	●	400	3500		V/mV
		V_S = 3V, V_O = 300mV to 2.7V, R_L = 10k	●	300	1800		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- + 0.2V to V^+ – 0.1V	●	75	87		dB
		V_S = 3V, V_{CM} = V^- + 0.2V to V^+ – 0.1V	●	71	83		dB
	CMRR Match (Channel-to-Channel) (Note 4)	V_S = 5V, V_{CM} = V^- + 0.2V to V^+ – 0.1V	●	69	89		dB
		V_S = 3V, V_{CM} = V^- + 0.2V to V^+ – 0.1V	●	65	85		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 12V, V_{CM} = V_O = 0.5V	●	82	98		dB
	PSRR Match (Channel-to-Channel) (Note 4)	V_S = 3V to 12V, V_{CM} = V_O = 0.5V	●	78	102		dB
	Minimum Supply Voltage (Note 8)	V_{CM} = V_O = 0.5V	●		2.6	2.7	V
V_{OL}	Output Voltage Swing Low (Note 5)	No Load	●		18	40	mV
		I_{SINK} = 0.5mA	●		38	80	mV
		I_{SINK} = 25mA, V_S = 5V	●		730	1500	mV
		I_{SINK} = 20mA, V_S = 3V	●		580	1200	mV

ELECTRICAL CHARACTERISTICS

$-40°C < T_A < 85°C$, V_S = 5V, 0V; V_S = 3V, 0V; $V_{CM} = V_{OUT}$ = half supply, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output Voltage Swing High (Note 5)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 15mA, V_S = 5V I_{SOURCE} = 10mA, V_S = 3V	● ● ● ●		15 55 860 580	40 110 1700 1200	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±17 ±12	±34 ±24		mA mA
I_S	Supply Current per Amplifier		●		4.1	5.2	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	●	14	28		MHz
SR	Slew Rate (Note 7)	V_S = 5V, A_V = –1, R_L = Open, V_O = 4V V_S = 3V, A_V = –1, R_L = Open	● ●	3.5 3.3	7 6.5		V/μs V/μs

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$			220 220	1000 1000	μV μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+			150	1000	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Note 4)			200	1500	μV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$		0 –1100	550 –550	1100 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+			1100	2200	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4) $V_{CM} = V^-$ (Note 4)			20 20	300 300	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$			20 20	150 150	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+			40	300	nA
	Input Noise Voltage	0.1Hz to 10Hz			300		nV_{P-P}
e_n	Input Noise Voltage Density	f = 1kHz			6		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			0.9		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 100kHz			5		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R_L = 10k V_O = –10V to 10V, R_L = 2k		1000 650	5000 3500		V/mV V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k		112	134		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+		89	106		dB
	CMRR Match (Channel-to-Channel) (Note 4)	$V_{CM} = V^-$ to V^+		86	110		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V		87	105		dB
	PSRR Match (Channel-to-Channel) (Note 4)	V_S = ±5V to ±15V		82	107		dB
V_{OL}	Output Voltage Swing Low (Note 5)	No Load I_{SINK} = 5mA I_{SINK} = 25mA			16 150 600	35 300 1200	mV mV mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA			15 250 1200	40 500 2400	mV mV mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current			±35	±70		mA
I_S	Supply Current per Amplifier				4.1	5.0	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz		15	30		MHz
SR	Slew Rate	A_V = –1, R_L = Open, V_O = ±10V, Measure at V_O = ±5V		5	10		V/µs

0°C < T_A < 70°C, V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ – 0.1V V_{CM} = V^- + 0.2V	● ●		300 300	1250 1250	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 2)	 V_{CM} = V^+ – 0.1V	● ●		2.5 2.5		µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		180	1100	µV
	Input Offset Voltage Match (Channel-to-Channel)	V_{CM} = V^- + 0.2V, V^+ – 0.1V (Note 4)	●		300	2000	µV
I_B	Input Bias Current	V_{CM} = V^+ – 0.1V V_{CM} = V^- + 0.2V	● ●	0 –1200	600 –600	1200 0	nA nA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		1200	2400	nA
	Input Bias Current Match (Channel-to-Channel)	V_{CM} = V^+ – 0.1V (Note 4) V_{CM} = V^- + 0.2V (Note 4)	● ●		30 30	350 350	nA nA
I_{OS}	Input Offset Current	V_{CM} = V^+ – 0.1V V_{CM} = V^- + 0.2V	● ●		25 25	175 175	nA nA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●		50	350	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R_L = 10k V_O = –10V to 10V, R_L = 2k	● ●	900 600	6000 4000		V/mV V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k	●	112	132		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●	88	104		dB
	CMRR Match (Channel-to-Channel) (Note 4)	V_{CM} = V^- + 0.2V to V^+ – 0.1V	●	84	104		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	●	86	100		dB
	PSRR Match (Channel-to-Channel) (Note 4)	V_S = ±5V to ±15V	●	80	104		dB
V_{OL}	Output Voltage Swing Low (Note 5)	No Load I_{SINK} = 5mA I_{SINK} = 25mA	● ● ●		19 175 670	45 350 1400	mV mV mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA	● ● ●		15 300 1400	40 600 2800	mV mV mV
I_{SC}	Short-Circuit Current		●	±28	±57		mA
I_S	Supply Current per Amplifier		●		4.6	5.6	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	●	14	28		MHz
SR	Slew Rate	A_V = –1, R_L = Open, V_O = ±10V, Measured at V_O = ±5V	●	4.5	9		V/µs

ELECTRICAL CHARACTERISTICS

$-40°C < T_A < 85°C$, $V_S = ±15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.1V$ $V_{CM} = V^- + 0.2V$	● ●		350 350	1400 1400	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 2)	 $V_{CM} = V^+ - 0.1V$	● ●		2.5 2.5		µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^- + 0.2V$ to $V^+ - 0.1V$	●		180	1200	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^- + 0.2V$, $V^+ - 0.1V$ (Note 4)	●		350	2200	µV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.1V$ $V_{CM} = V^- + 0.2V$	● ●	0 –1400	690 –690	1400 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.2V$ to $V^+ - 0.1V$	●		1380	2800	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+ - 0.1V$ (Note 4) $V_{CM} = V^- + 0.2V$ (Note 4)	● ●		30 30	420 420	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.1V$ $V_{CM} = V^- + 0.2V$	● ●		30 30	210 210	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.2V$ to $V^+ - 0.1V$	●		60	420	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -14.5V$ to $14.5V$, $R_L = 10k$ $V_O = -10V$ to $10V$, $R_L = 2k$	● ●	700 400	6000 4000		V/mV V/mV
	Channel Separation	$V_O = -10V$ to $10V$, $R_L = 2k$	●	112	132		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^- + 0.2V$ to $V^+ - 0.1V$	●	87	104		dB
	CMRR Match (Channel-to-Channel) (Note 4)	$V_{CM} = V^- + 0.2V$ to $V^+ - 0.1V$	●	84	104		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±5V$ to $±15V$	●	84	100		dB
	PSRR Match (Channel-to-Channel) (Note 4)	$V_S = ±5V$ to $±15V$	●	80	100		dB
V_{OL}	Output Voltage Swing Low (Note 5)	No Load $I_{SINK} = 5mA$ $I_{SINK} = 25mA$	● ● ●		22 180 700	50 350 1400	mV mV mV
V_{OH}	Output Voltage Swing High (Note 5)	No Load $I_{SOURCE} = 5mA$ $I_{SOURCE} = 25mA$	● ● ●		15 300 1500	40 600 3000	mV mV mV
I_{SC}	Short-Circuit Current		●	±27	±54		mA
I_S	Supply Current per Amplifier		●		4.8	5.9	mA
GBW	Gain-Bandwidth Product (Note 6)	f = 100kHz	●	14	27		MHz
SR	Slew Rate	$A_V = -1$, R_L = Open, $V_O = ±10V$, Measure at $V_O = ±5V$	●	4.2	8.5		V/µs

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 2: This parameter is not 100% tested.

Note 3: The LT1630/LT1631 are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. Guaranteed I grade parts are available, consult factory.

Note 4: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1631; between the two amplifiers on the LT1630.

Note 5: Output voltage swings are measured between the output and power supply rails.

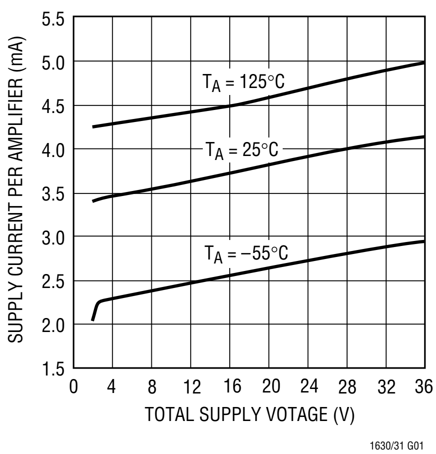
Note 6: $V_S = 3V$, $V_S = ±15V$ GBW limit guaranteed by correlation to 5V tests.

Note 7: $V_S = 3V$, $V_S = 5V$ slew rate limit guaranteed by correlation to ±15V tests.

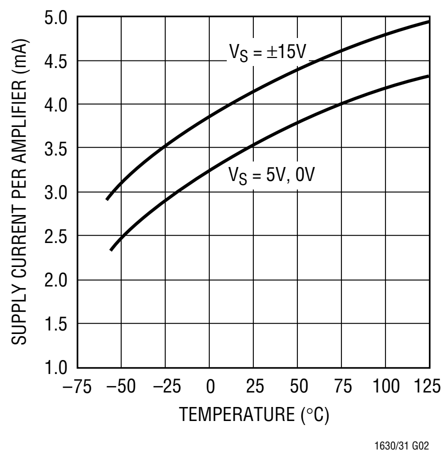
Note 8: Minimum supply voltage is guaranteed by testing the change of V_{OS} to be less than 250µV when the supply voltage is varied from 3V to 2.7V.

TYPICAL PERFORMANCE CHARACTERISTICS

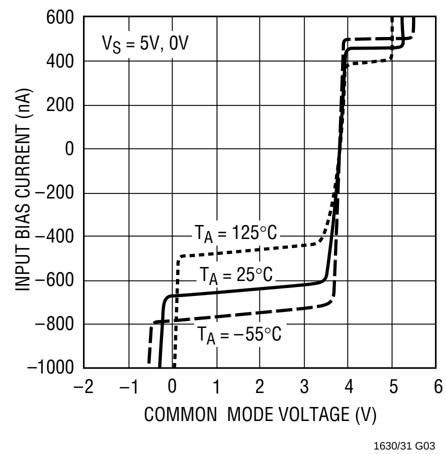
Supply Current vs Supply Voltage



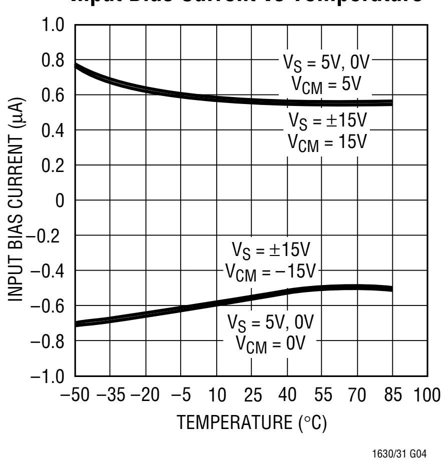
Supply Current vs Temperature



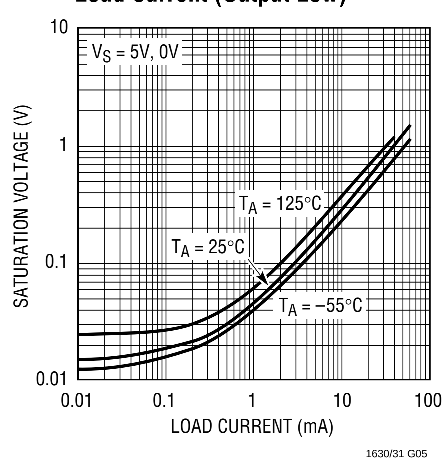
Input Bias Current vs Common Mode Voltage



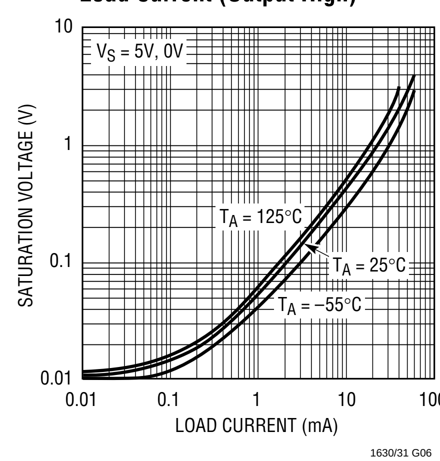
Input Bias Current vs Temperature



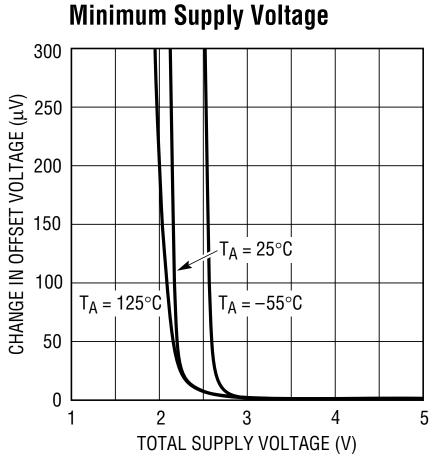
Output Saturation Voltage vs Load Current (Output Low)



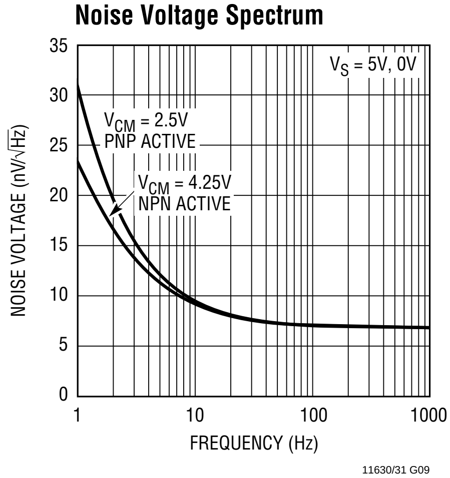
Output Saturation Voltage vs Load Current (Output High)



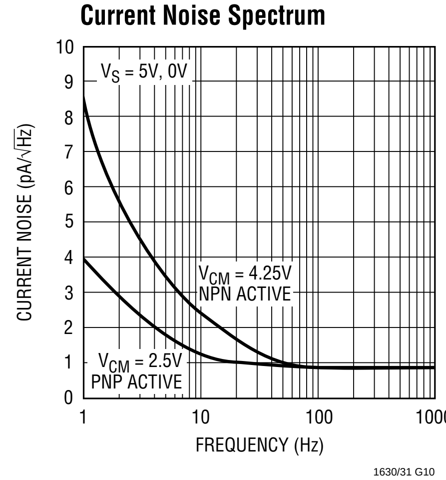
Minimum Supply Voltage



Noise Voltage Spectrum

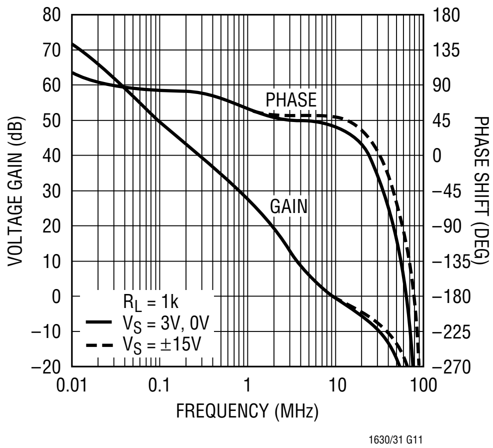


Current Noise Spectrum

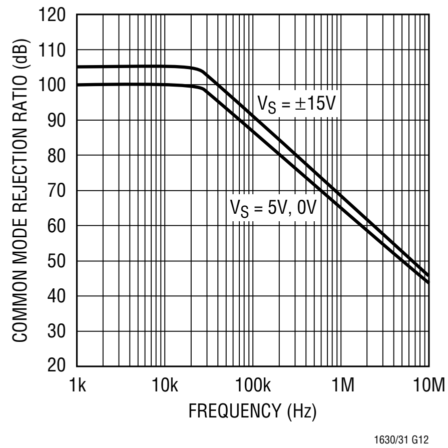


TYPICAL PERFORMANCE CHARACTERISTICS

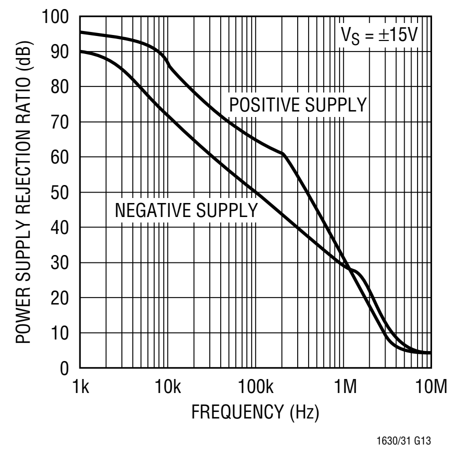
Gain and Phase vs Frequency



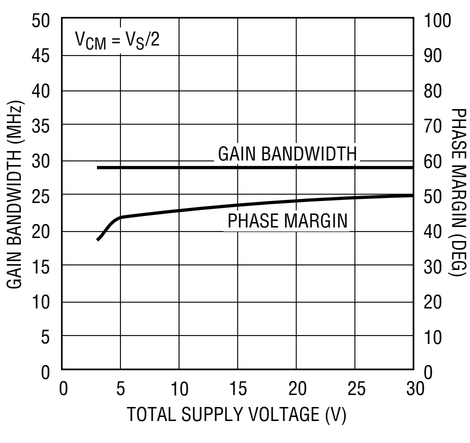
CMRR vs Frequency



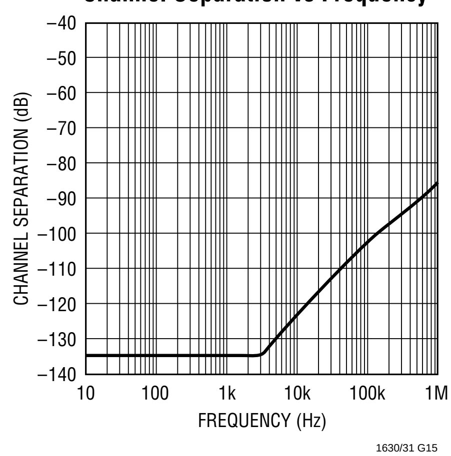
PSRR vs Frequency



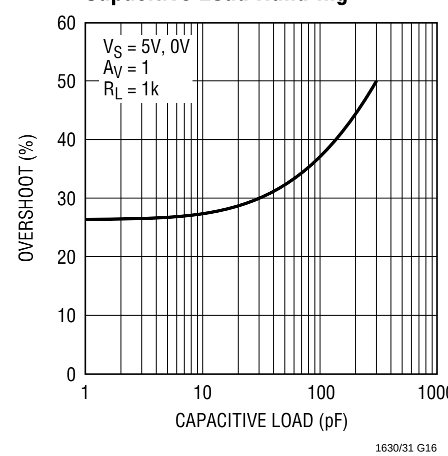
Gain Bandwidth and Phase Margin vs Supply Voltage



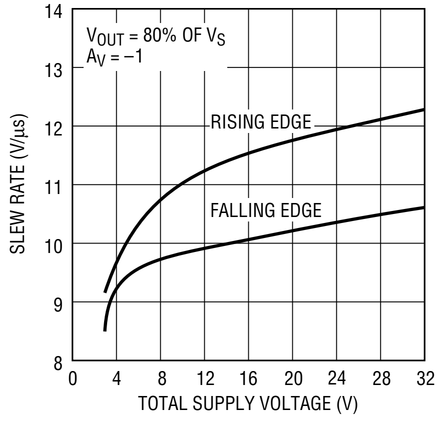
Channel Separation vs Frequency



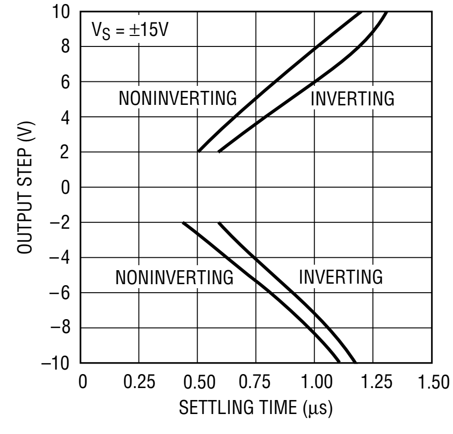
Capacitive Load Handling



Slew Rate vs Supply Voltage

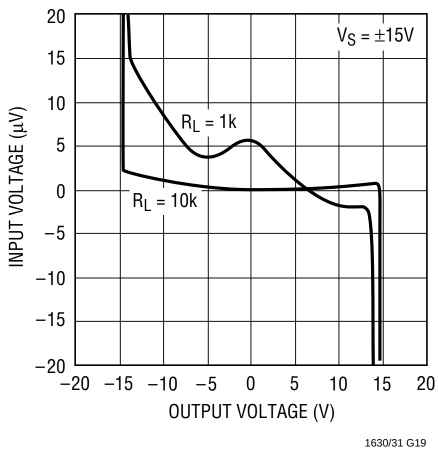


Output Step vs Settling Time to 0.01%

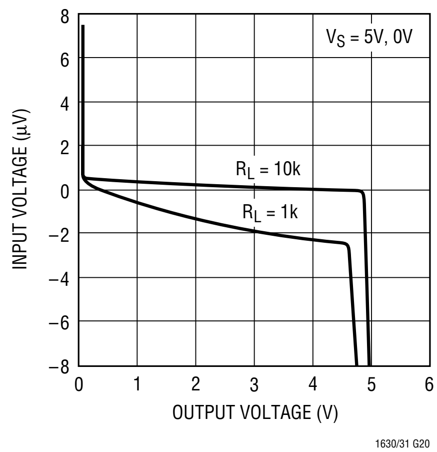


TYPICAL PERFORMANCE CHARACTERISTICS

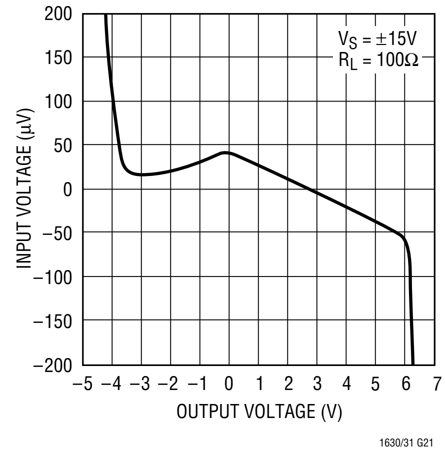
Open-Loop Gain



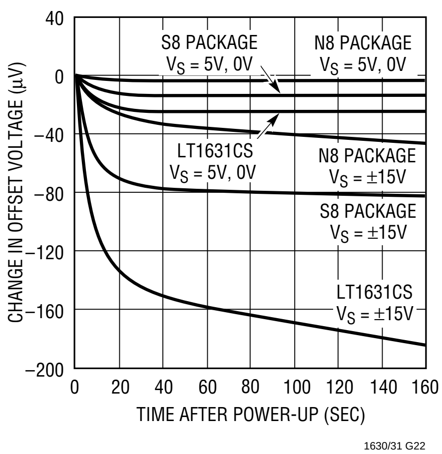
Open-Loop Gain



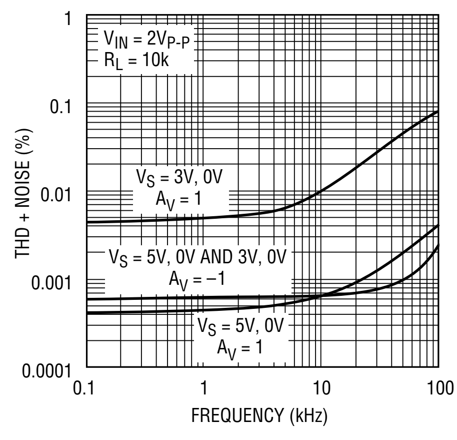
Open-Loop Gain



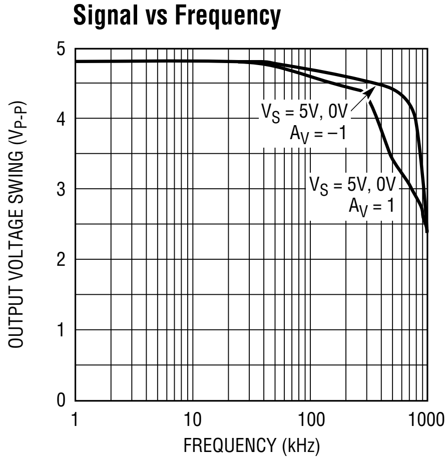
Warm-Up Drift vs Time



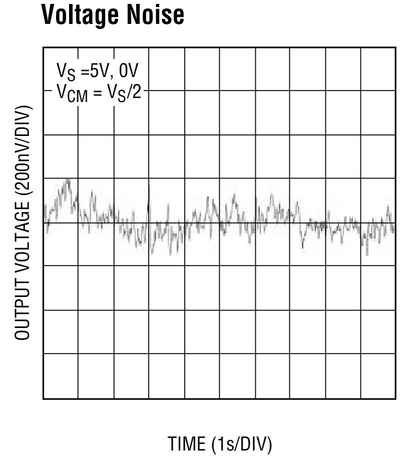
Total Harmonic Distortion + Noise vs Frequency



Maximum Undistorted Output Signal vs Frequency

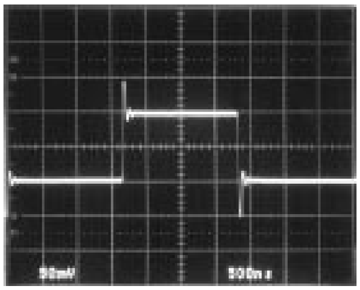


0.1Hz to 10Hz Output Voltage Noise



TYPICAL PERFORMANCE CHARACTERISTICS

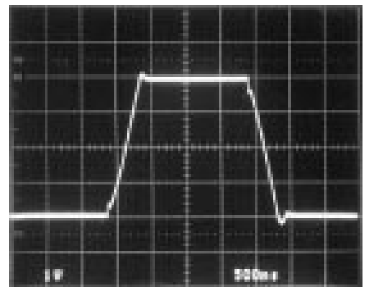
5V Small-Signal Response



V_S = 5V, 0V
A_V = 1
R_L = 1k

1630/31 G26

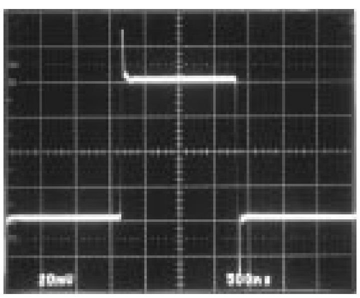
5V Large-Signal Response



V_S = 5V, 0V
A_V = 1
R_L = 1k

1630/31 G27

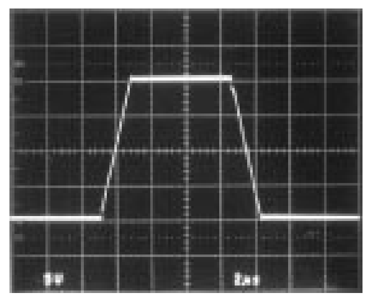
±15V Small-Signal Response



V_S = ±15V
A_V = 1
R_L = 1k

1630/31 G28

±15V Large-Signal Response



V_S = ±15V
A_V = 1
R_L = 1k

1630/31 G29

APPLICATIONS INFORMATION

Rail-to-Rail Input and Output

The LT1630/LT1631 are fully functional for an input and output signal range from the negative supply to the positive supply. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4 that are active over different ranges of input common mode voltage. The PNP differential input pair is active for input common mode voltages V_{CM} between the negative supply to approximately 1.4V below the positive supply. As V_{CM} moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply.

The output is configured with a pair of complementary common emitter stages Q14/Q15 that enables the output to swing from rail to rail. These devices are fabricated on Linear Technology's proprietary complementary bipolar process to ensure similar DC and AC characteristics. Capacitors C1 and C2 form local feedback loops that lower the output impedance at high frequencies.

Power Dissipation

The LT1630/LT1631 amplifiers combine high speed and large output current drive in a small package. Because the amplifiers operate over a very wide supply range, it is possible to exceed the maximum junction temperature of 150°C in plastic packages under certain conditions. Junc-

APPLICATIONS INFORMATION

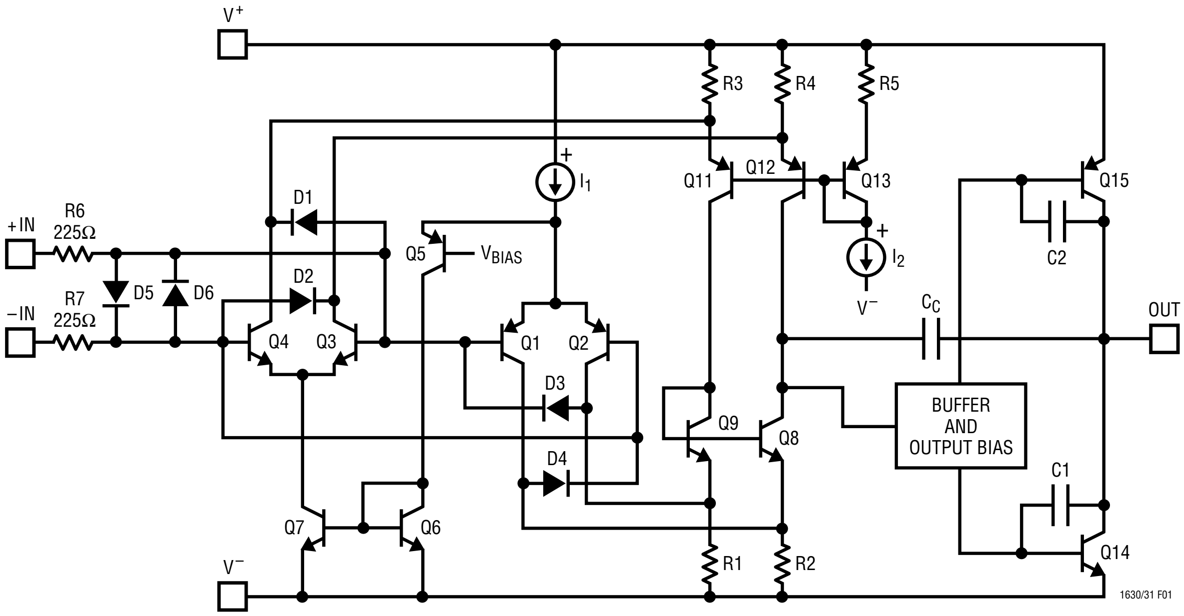


Figure 1. LT1630 Simplified Schematic Diagram

tion temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LT1630CN8: $T_J = T_A + (P_D \bullet 130°C/W)$
LT1630CS8: $T_J = T_A + (P_D \bullet 190°C/W)$
LT1631CS: $T_J = T_A + (P_D \bullet 150°C/W)$

The power dissipation in the IC is the function of the supply voltage, output voltage and load resistance. For a given supply voltage, the worst-case power dissipation P_{DMAX} occurs at the maximum supply current and when the output voltage is at half of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is given by:

$$P_{DMAX} = (V_S \bullet I_{SMAX}) + (V_S/2)^2/R_L$$

To ensure that the LT1630/LT1631 are used properly, calculate the worst-case power dissipation, get the thermal resistance for a chosen package and its maximum junction temperature to derive the maximum ambient temperature.

Example: An LT1630CS8 operating on ±15V supplies and driving a 500Ω, the worse-case power dissipation per amplifier is given by:

$$P_{DMAX} = (30V \bullet 4.75mA) + (15V – 7.5V)(7.5/500)$$
$$= 0.143 + 0.113 = 0.256W$$

If both amplifiers are loaded simultaneously, then the total power dissipation is 0.512W. The SO-8 package has a junction-to-ambient thermal resistance of 190°C/W in still air. Therefore, the maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J – (P_{DMAX} \bullet 190°C/W)$$
$$T_A = 150°C – (0.512W \bullet 190°C/W) = 53°C$$

For a higher operating temperature, lower the supply voltage or use the DIP package part.

APPLICATIONS INFORMATION

Input Offset Voltage

The offset voltage changes depending upon which input stage is active, and the maximum offset voltages are trimmed to less than 525μV. To maintain the precision characteristics of the amplifier, the change of V_{OS} over the entire input common mode range (CMRR) is guaranteed to be less than 525μV on a single 5V supply.

Input Bias Current

The input bias current polarity depends on the input common mode voltage. When the PNP differential pair is active, the input bias currents flow out of the input pins. They flow in the opposite direction when the NPN input stage is active. The offset voltage error due to input bias currents can be minimized by equalizing the noninverting and inverting input source impedance.

Output

The outputs of the LT1630/LT1631 can deliver large load currents; the short-circuit current limit is 70mA. Take care to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section). The output of these amplifiers have reverse-biased diodes to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred mA, no damage to the part will occur.

Overdrive Protection

To prevent the output from reversing polarity when the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 are employed. When the input voltage exceeds either power supply by approximately 700mV, D1/D2 or D3/D4 will turn on, forcing the output to the proper polarity. For this phase reversal protection to work properly, the input current must be limited to less than 5mA. If the amplifier is to be severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1630/LT1631's input stages are protected against large differential input voltages by a pair of back-to-back diodes D5/D6. When a differential voltage of more than 0.7V is applied to the inputs, these diodes will turn on, preventing the emitter-base breakdown of the input transistors. The current in D5/D6 should be limited to less than 10mA. Internal 225Ω resistors R6 and R7 will limit the input current for differential input signals of 4.5V or less. For larger input levels, a resistor in series with either or both inputs should be used to limit the current. Worst-case differential input voltage usually occurs when the output is shorted to ground. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins.

Capacitive Load

The LT1630/LT1631 are wideband amplifiers that can drive capacitive loads up to 200pF on ±15V supplies in a unity-gain configuration. On a 3V supply, the capacitive load should be kept to less than 100pF. When there is a need to drive larger capacitive loads, a resistor of a couple hundred ohms should be connected between the output and the capacitive load. The feedback should still be taken from the output so that the resistor isolates the capacitive load to ensure stability.

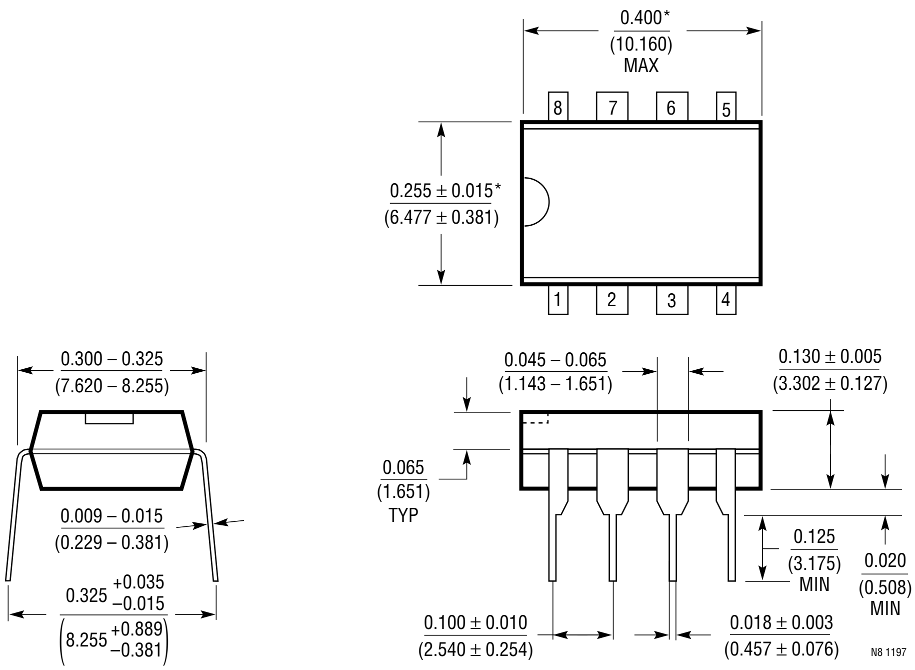
Feedback Components

The low input bias currents of the LT1630/LT1631 make it possible to use the high value feedback resistors to set the gain. However, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1630/LT1631 in a noninverting gain of 2, set with two 20k resistors, will probably oscillate with 10pF total input capacitance (5pF input capacitance and 5pF board capacitance). The amplifier has a 5MHz crossing frequency and a 52° phase margin at 6dB of gain. The feedback resistors and the total input capacitance form a pole at 1.6MHz that induces a phase shift of 72° at 5MHz! The solution is simple: either lower the value of the resistors or add a feedback capacitor of 10pF or more.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

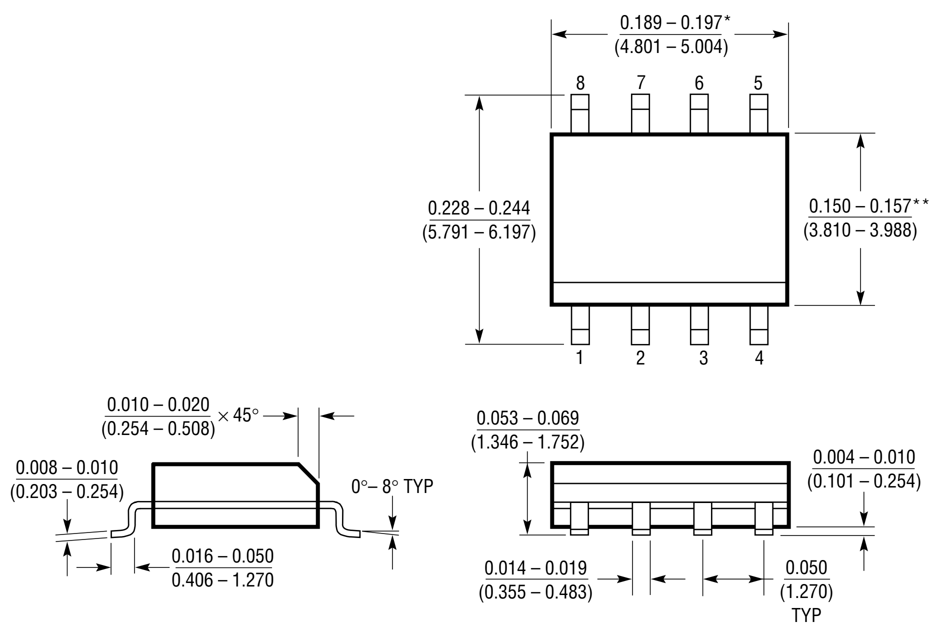


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

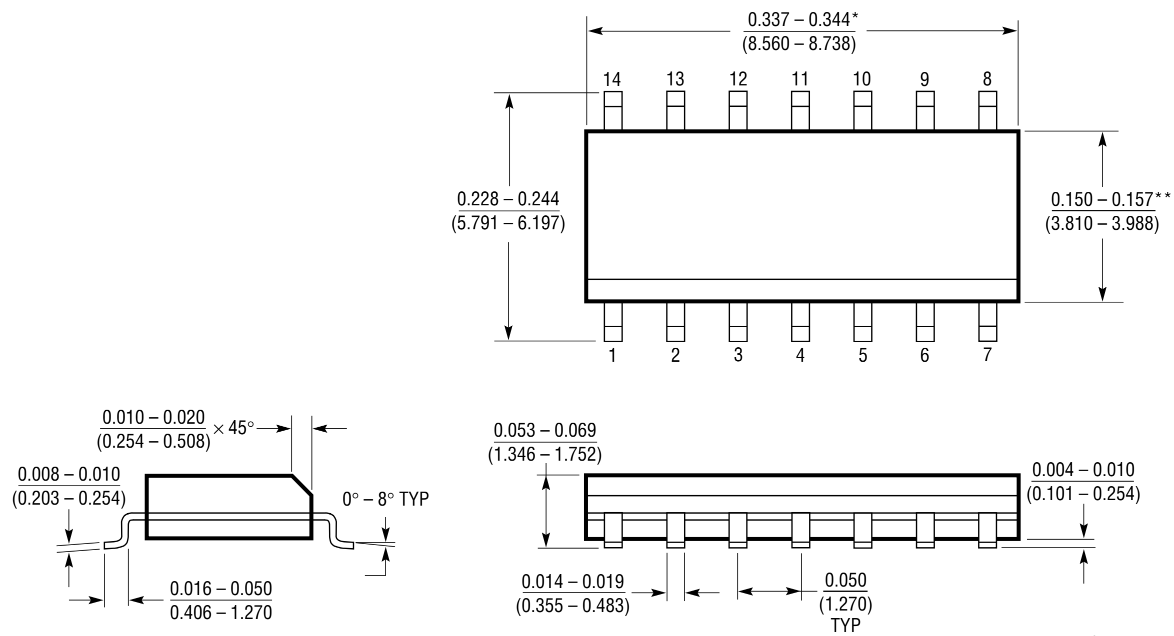
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTON	COMMENTS
LT1211/LT1212	Dual/Quad 14MHz, 7V/µs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 275µV $V_{OS(MAX)}$, 6µV/°C Max Drift, Max Supply Current 1.8mA per Op Amp
LT1213/LT1214	Dual/Quad 28MHz, 12V/µs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 275µV $V_{OS(MAX)}$, 6µV/°C Max Drift, Max Supply Current 3.5mA per Op Amp
LT1215/LT1216	Dual/Quad 23MHz, 50V/µs, Single Supply Precision Op Amps	Input Common Mode Includes Ground, 450µV $V_{OS(MAX)}$, 6µV/°C Max Drift, Max Supply Current 6.6mA per Op Amp
LT1498/LT1499	Dual/Quad 10MHz, 6V/µs Rail-to-Rail Input and Output C-Load™ Op Amps	High DC Accuracy, 475µV $V_{OS(MAX)}$, 4µV/°C Max Drift, Max Supply Current 2.2mA per Amp
LT1632/LT1633	Dual/Quad 45MHz, 45V/µs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 1.35mV $V_{OS(MAX)}$, 70mA Output Current, Max Supply Current 5.2mA per Amp

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