LINEAR TECHNOLOGY

LT1251/LT1256

40MHz Video Fader and DC Gain Controlled Amplifier

FEATURES

- **Accurate Linear Gain Control: ±1% Typ, ±3% Max**
- **Constant Gain with Temperature**
- Wide Bandwidth: 40MHz
- High Slew Rate: 300V/µs
- Fast Control Path: 10MHz
- Low Control Feedthrough: 2.5mV
- High Output Current: 40mA
- Low Output Noise
  - 45nV/√Hz at A_V = 1
  - 270nV/√Hz at A_V = 100
- Low Distortion: 0.01%
- Wide Supply Range: ±2.5V to ±15V
- Low Supply Current: 13mA
- Low Differential Gain and Phase: 0.02%, 0.02°

APPLICATIONS

- Composite Video Gain Control
- RGB, YUV Video Gain Control
- Video Faders, Keyers
- Gamma Correction Amplifiers
- Audio Gain Control, Faders
- Multipliers, Modulators
- Electronically Tunable Filters

DESCRIPTION

The LT1251/LT1256 are two-input, one-output, 40MHz current feedback amplifiers with a linear control circuit that sets the amount each input contributes to the output. These parts make excellent electronically controlled variable gain amplifiers, filters, mixers and faders. The only external components required are the power supply bypass capacitors and the feedback resistors. Both parts operate on supplies from ±2.5V (or single 5V) to ±15V (or single 30V).

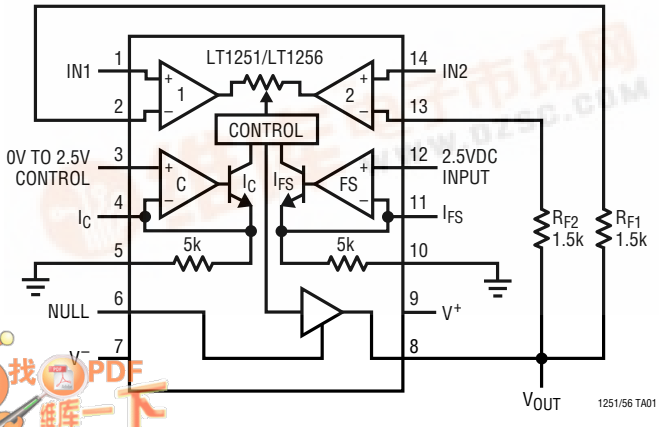
Absolute gain accuracy is trimmed at wafer sort to minimize part-to-part variations. The circuit is completely temperature compensated.

The LT1251 includes circuitry that eliminates the need for accurate control signals around zero and full scale. For control signals of less than 2% or greater than 98%, the LT1251 sets one input completely off and the other completely on. This is ideal for fader applications because it eliminates off-channel feedthrough due to offset or gain errors in the control signals.

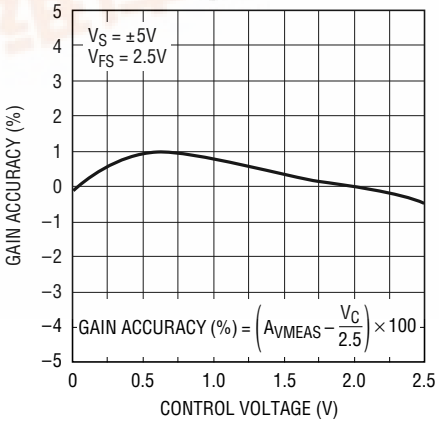
The LT1256 does not have this on/off feature and operates linearly over the complete control range. The LT1256 is recommended for applications requiring more than 20dB of linear control range.

TYPICAL APPLICATION

Two-Input Video Fader



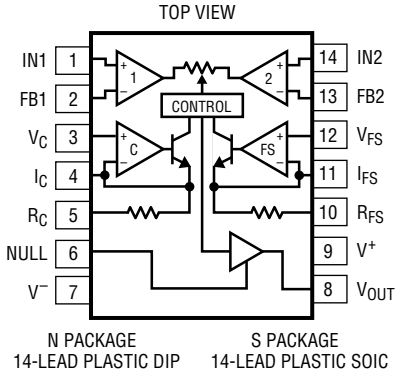
LT1256
Gain Accuracy vs Control Voltage



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Input Voltage on Pins 3,4,5,10,11,12 ..... V^- to V^+
Output Short Circuit Duration (Note 1) ..... Continuous
Specified Temperature Range (Note 2) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
14-LEAD PLASTIC DIP

S PACKAGE
14-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER

LT1251CN
LT1251CS
LT1256CN
LT1256CS

(Note 2)

Consult factory for Industrial and Military grade parts.

SIGNAL AMPLIFIER AC CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±5V, V_{IN} = 1V_{RMS}, f = 1kHz, A_{VMAX} = 1, R_{F1} = R_{F2} = 1.5k, V_{FS} = 2.5V, I_C = I_{FS} = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
2%IN1	2% Input 1 Gain	V_C (Pin 3) = 0.05V	LT1251	●	0		0.1	%
			LT1256	●	0.1		5.0	%
10%IN1	10% Input 1 Gain	V_C (Pin 3) = 0.25V		●	7		13	%
20%IN1	20% Input 1 Gain	V_C (Pin 3) = 0.50V		●	17		23	%
30%IN1	30% Input 1 Gain	V_C (Pin 3) = 0.75V		●	27		33	%
40%IN1	40% Input 1 Gain	V_C (Pin 3) = 1.00V		●	37		43	%
50%IN1	50% Input 1 Gain	V_C (Pin 3) = 1.25V		●	47		53	%
60%IN1	60% Input 1 Gain	V_C (Pin 3) = 1.50V		●	57		63	%
70%IN1	70% Input 1 Gain	V_C (Pin 3) = 1.75V		●	67		73	%
80%IN1	80% Input 1 Gain	V_C (Pin 3) = 2.00V		●	77		83	%
90%IN1	90% Input 1 Gain	V_C (Pin 3) = 2.25V		●	87		93	%
98%IN1	98% Input 1 Gain	V_C (Pin 3) = 2.45V	LT1251	●	99.9		100.0	%
			LT1256	●	95.0		99.9	%
2%IN2	2% Input 2 Gain	V_C (Pin 3) = 2.45V	LT1251	●	0		0.1	%
			LT1256	●	0.1		5.0	%
10%IN2	10% Input 2 Gain	V_C (Pin 3) = 2.25V		●	7		13	%
20%IN2	20% Input 2 Gain	V_C (Pin 3) = 2.00V		●	17		23	%
30%IN2	30% Input 2 Gain	V_C (Pin 3) = 1.75V		●	27		33	%
40%IN2	40% Input 2 Gain	V_C (Pin 3) = 1.50V		●	37		43	%
50%IN2	50% Input 2 Gain	V_C (Pin 3) = 1.25V		●	47		53	%
60%IN2	60% Input 2 Gain	V_C (Pin 3) = 1.00V		●	57		63	%
70%IN2	70% Input 2 Gain	V_C (Pin 3) = 0.75V		●	67		73	%
80%IN2	80% Input 2 Gain	V_C (Pin 3) = 0.50V		●	77		83	%
90%IN2	90% Input 2 Gain	V_C (Pin 3) = 0.25V		●	87		93	%
98%IN2	98% Input 2 Gain	V_C (Pin 3) = 0.05V	LT1251	●	99.9		100.0	%
			LT1256	●	95.0		99.9	%

SIGNAL AMPLIFIER AC CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{IN} = 1V_{RMS}$, f = 1kHz, $A_{VMAX} = 1$, $R_{F1} = R_{F2} = 1.5k$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Supply Rejection	$V_C = 1.25V$, $V_S = \pm 5V$ to $\pm 15V$	●		0.03	0.10	%/V
	External Resistor Gain 50% Input 1	Pins 5,10 = Open, External 5k Resistors from Pins 4,11 to Ground, $V_C = 1.25V$	●	45		55	%
SR	Slew Rate	$V_{IN} = \pm 2.5V$, V_O at $\pm 2V$, $R_L = 150\Omega$	●	150	300		V/µs
	Control Feedthrough	$V_C = 1.25VDC + 2.5V_{P-P}$ at 1kHz			2.5		mV_{P-P}
	Full Power Bandwidth	$V_O = 1V_{RMS}$			20		MHz
BW	Small-Signal Bandwidth	$V_S = \pm 5V$ $V_S = \pm 15V$			30 40		MHz MHz
	Differential Gain (Notes 4,5)	Control = 0% or 100% Control = 25% or 75%			0.02 0.90		% %
	Differential Phase (Notes 4,5)	Control = 0% or 100% Control = 25% or 75%			0.02 0.55		DEG DEG
THD	Total Harmonic Distortion	Gain = 100% Gain = 50% Gain = 10%			0.002 0.015 0.4		% % %
t_r, t_f	Rise Time, Fall Time	10% to 90%, $V_O = 100mV$			11		ns
OS	Overshoot	$V_O = 100mV$			3		%
t_{PD}	Propagation Delay	$V_O = 100mV$			10		ns
t_S	Settling Time	0.1%, $\Delta V_O = 2V$			65		ns

SIGNAL AMPLIFIER DC CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{CM} = 0V$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input Difference Between Inputs	● ●	 −3	2 1	5 3	mV mV
	Input Offset Voltage Drift				10		µV/°C
I_{IN}^+	Noninverting Input Bias Current	Either Input	●	−2.5	0.5	2.5	µA
I_{IN}^-	Inverting Input Bias Current	Either Input Difference Between Inputs	● ●	−30 −1	10 0.5	30 1	µA µA
	Inverting Input Bias Current Null Change	Null (Pin 6) Open to V^-	●	−280	−170	−60	µA
e_n	Input Noise Voltage Density	f = 1kHz			2.7		$nV/\sqrt{Hz}$
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.5		$pA/\sqrt{Hz}$
$-i_n$	Inverting Input Noise Current Density	f = 1kHz			29		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Either Noninverting Input	●	5	17		MΩ
C_{IN}	Input Capacitance	Either Noninverting Input	●		1.5		pF
	Input Voltage Range	$V_S = \pm 5V$ $V_S = 5V$	● ●	±3 2	±3.2	 3	V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -3V$ to 3V $V_S = 5V$, $V_{CM} = 2V$ to 3V, $V_O = 2.5V$	● ●	55 50	61 57		dB dB
	Inverting Input Current Common-Mode Rejection	$V_{CM} = -3V$ to 3V $V_S = 5V$, $V_{CM} = 2V$ to 3V, $V_O = 2.5V$	● ●		0.07 0.17	0.25 0.70	µA/V µA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	●	70	76		dB
	Noninverting Input Current Power Supply Rejection	$V_S = \pm 5V$ to $\pm 15V$	●		30	100	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm 5V$ to $\pm 15V$	●		30	200	nA/V

SIGNAL AMPLIFIER DC CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{CM} = 0V$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_O = -3V$ to 3V, $R_L = 150\Omega$	●	83	93		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}^-$	$V_O = -3V$ to 3V, $R_L = 150\Omega$	●	1.0	1.8		MΩ
V_{OUT}	Maximum Output Voltage Swing	No Load	●	±4.0	±4.2		V
		$R_L = 150\Omega$	●	±3.0	±3.5		V
		$V_S = \pm 15V$, No Load	●	±14.0	±14.2		V
		$V_S = 5V$, $V_{CM} = 2.5V$, (Note 6)	●	1.2		3.8	V
I_O	Maximum Output Current	$V_S = \pm 5V$	●	±30	±40		mA
		$V_S = 5V$, $V_{CM} = V_O = 2.5V$	●	±20	±30		mA
I_S	Supply Current	$V_C = V_{FS} = 2.5V$	●	10.0	13.5	17.0	mA
		$V_C = V_{FS} = 1.25V$	●	5.0	7.5	9.5	mA
		$V_C = V_{FS} = 0V$	●	0.8	1.3	1.8	mA
		$V_C = V_{FS} = 2.5V$, $V_S = \pm 15V$	●	10.0	14.5	18.5	mA
		$V_C = V_{FS} = 0V$, $V_S = \pm 15V$	●	0.8	1.4	2.0	mA

CONTROL AND FULL SCALE AMPLIFIER CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_S = \pm 5V$, $V_{FS} = 2.5V$, $I_C = I_{FS}$ = NULL = Open, Pins 5,10 = GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Control Amplifier Input Offset Voltage	Pin 4 to Pin 3	●		5	15	mV
	Full Scale Amplifier Input Offset Voltage	Pin 11 to Pin 12	●		5	15	mV
	Control Amplifier Input Resistance		●	25	100		MΩ
	Full Scale Amplifier Input Resistance		●	25	100		MΩ
	Control Amplifier Input Bias Current		●	–750	–300		nA
	Full Scale Amplifier Input Bias Current		●	–750	–300		nA
R_C	Internal Control Resistor	$T_A = 25°C$		3.75	5	6.25	kΩ
R_{FS}	Internal Full Scale Resistor	$T_A = 25°C$		4	5	6	kΩ
	Resistor Temperature Coefficient				0.2		%/°C
	Control Path Bandwidth	Small Signal, V_C = 100mV, (Note 7)			10		MHz
	Control Path Rise and Fall Time	Small Signal, V_C = 100mV, (Note 7)			35		ns
	Control Path Transition Time	0% to 100%			150		ns
	Control Path Propagation Delay	Small Signal, ΔV_C = 100mV			50		ns
		V_C from 0% or 100%			90		ns

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: A heat sink may be required depending on the power supply voltage.

Note 2: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

Note 3: T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the following formulas:

LT1251CN/LT1256CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1251CS/LT1256CS: $T_J = T_A + (P_D \times 100°C/W)$

Note 4: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Five identical amplifier stages were cascaded giving an effective resolution of 0.02% and 0.02°.

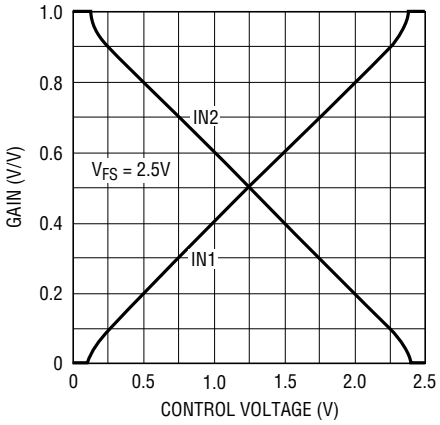
Note 5: Differential gain and phase are best when the control is set at 0% or 100%. See the Typical Performance Characteristics curves.

Note 6: Tested with $R_L = 150\Omega$ to 2.5V to simulate an AC coupled load.

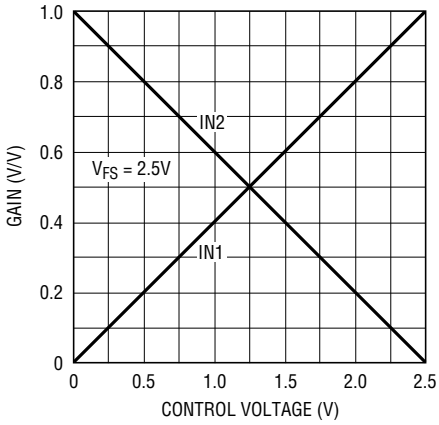
Note 7: Small-signal control path response is measured driving R_C (pin 5) to eliminate peaking caused by stray capacitance on pin 4.

TYPICAL PERFORMANCE CHARACTERISTICS

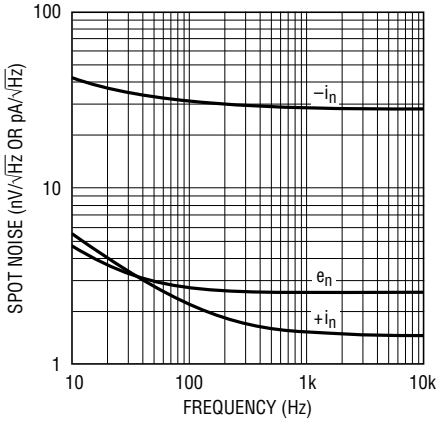
LT1251
Gain vs Control Voltage



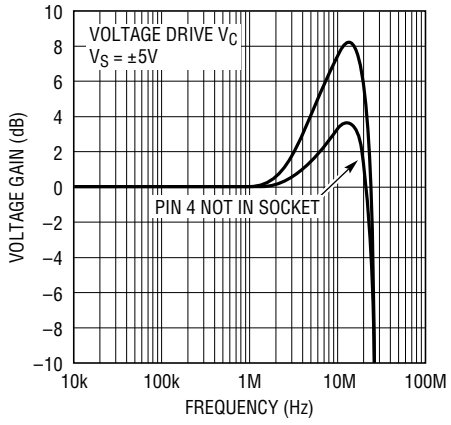
LT1256
Gain vs Control Voltage



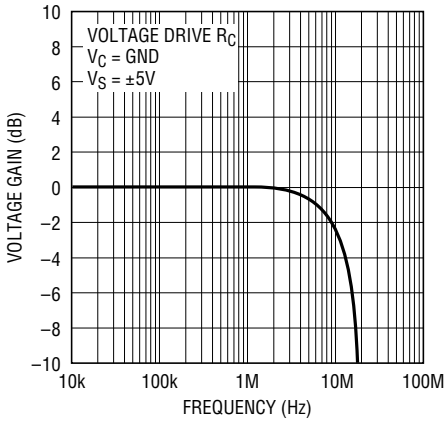
Spot Input Noise Voltage and Current vs Frequency



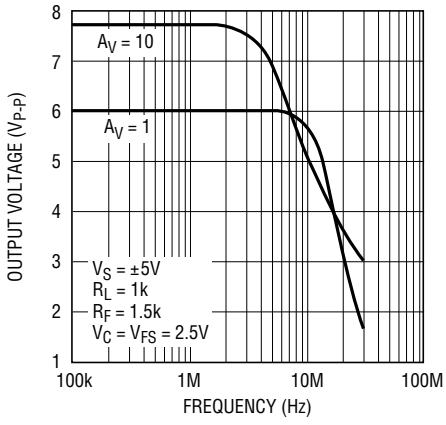
LT1251/LT1256
Control Path Bandwidth



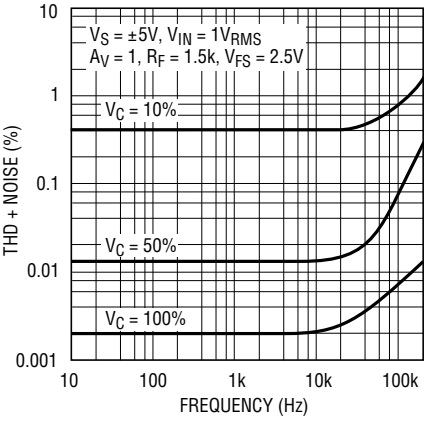
LT1251/LT1256
Control Path Bandwidth



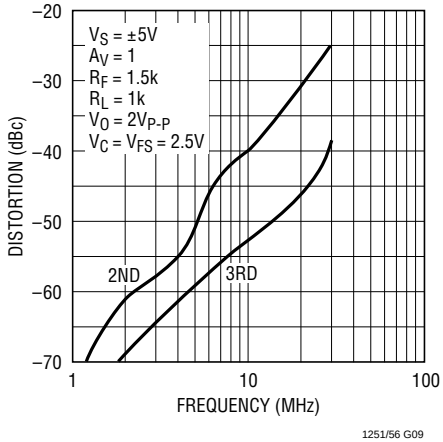
Undistorted Output Voltage vs Frequency



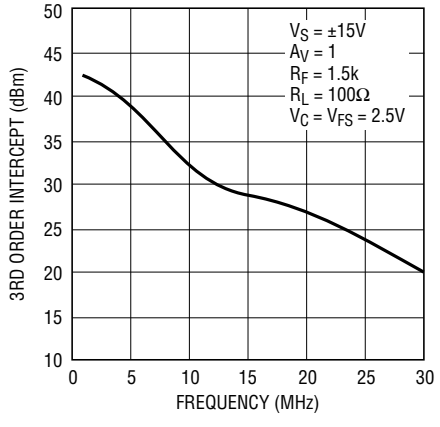
THD Plus Noise vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency

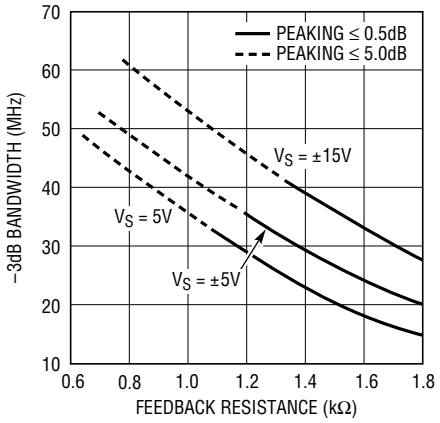


3rd Order Intercept vs Frequency



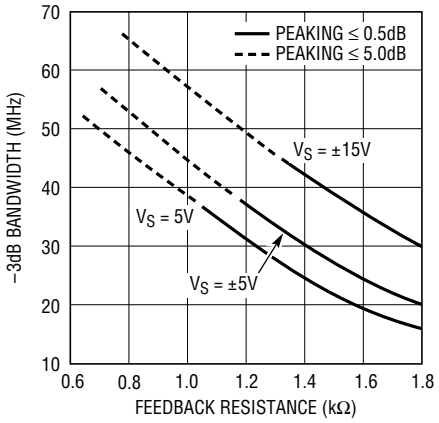
TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Feedback Resistance, A_V = 1, R_L = 100Ω



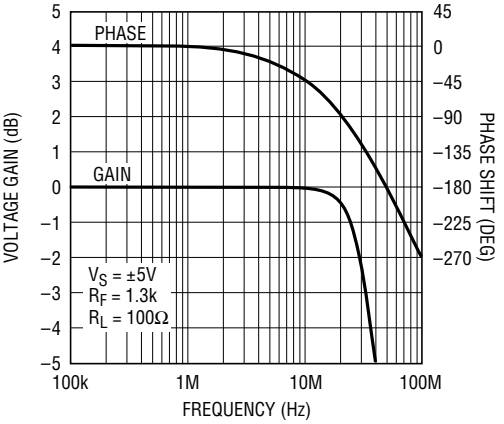
1251/56 G11

Bandwidth vs Feedback Resistance, A_V = 1, R_L = 1k



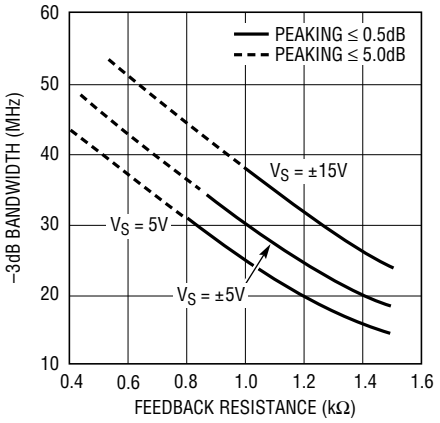
1251/56 G12

Voltage Gain and Phase vs Frequency



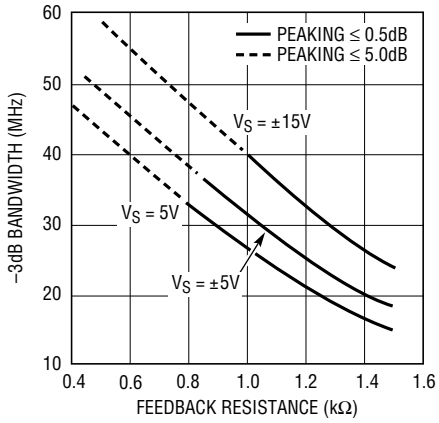
1251/56 G13

Bandwidth vs Feedback Resistance, A_V = 10, R_L = 100Ω



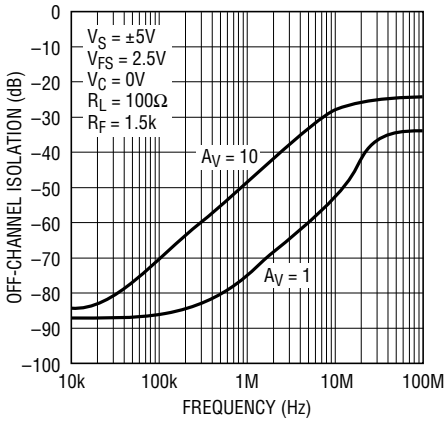
1251/56 G14

Bandwidth vs Feedback Resistance, A_V = 10, R_L = 1k



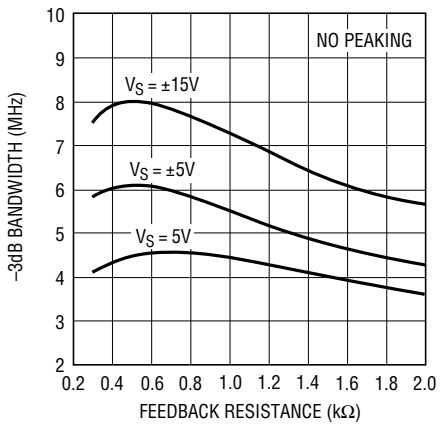
1251/56 G15

Off-Channel Isolation vs Frequency



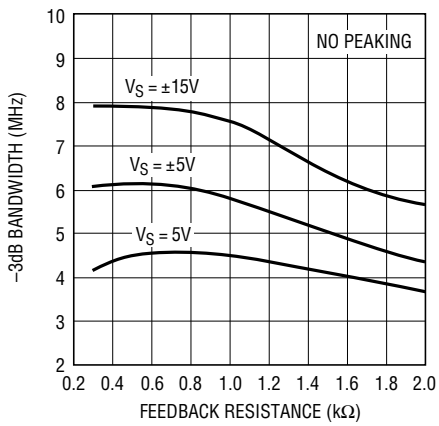
1251/56 G16

Bandwidth vs Feedback Resistance, A_V = 100, R_L = 100Ω



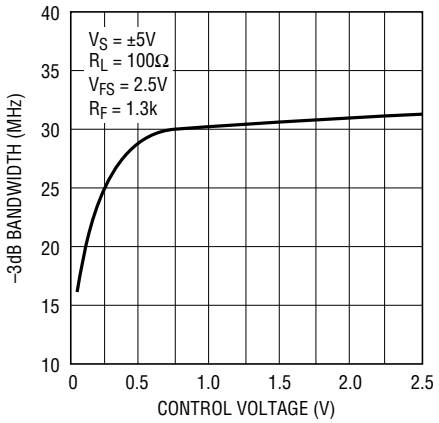
1251/56 G17

Bandwidth vs Feedback Resistance, A_V = 100, R_L = 1k



1251/56 G18

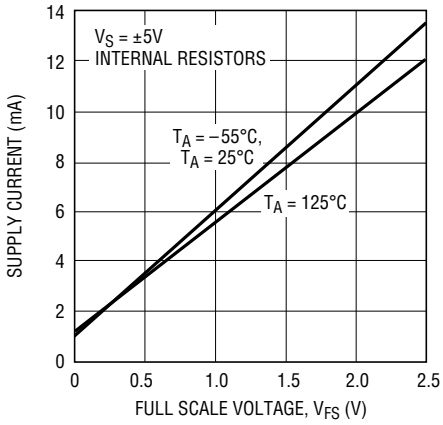
–3dB Bandwidth vs Control Voltage



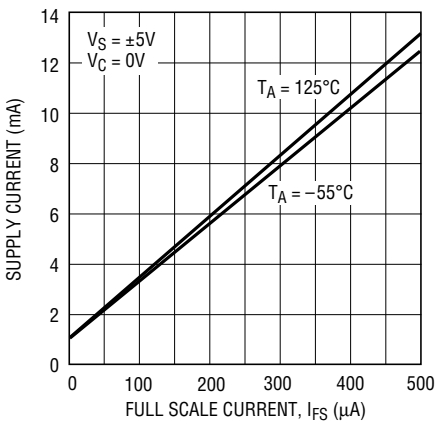
1251/56 G19

TYPICAL PERFORMANCE CHARACTERISTICS

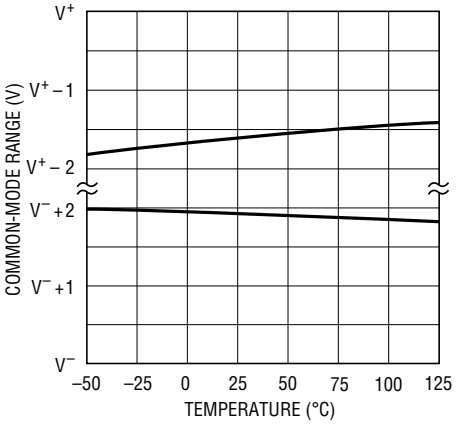
Supply Current vs Full Scale Voltage



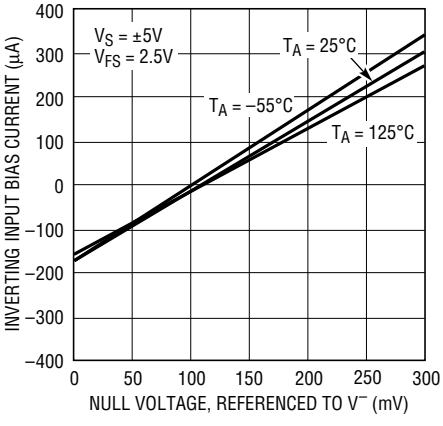
Supply Current vs Full Scale Current



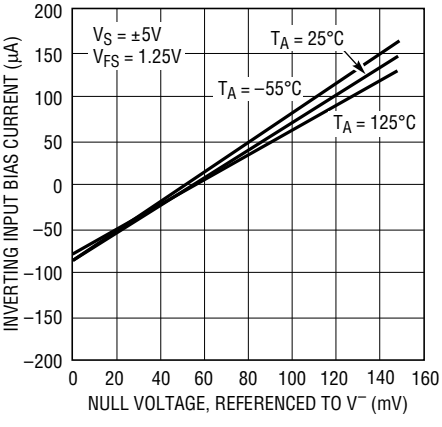
Input Common-Mode Range vs Temperature



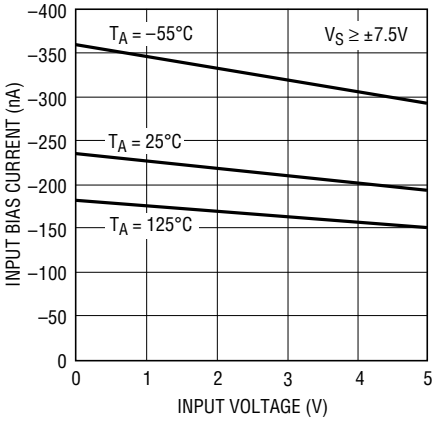
Inverting Input Bias Current vs Null Voltage



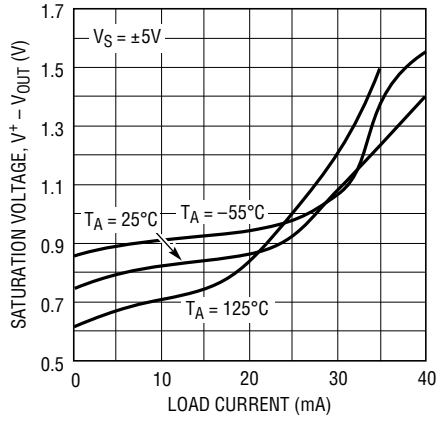
Inverting Input Bias Current vs Null Voltage



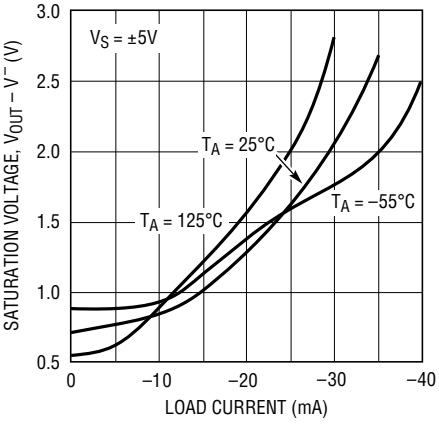
Control and Full Scale Amp Input Bias Current vs Input Voltage



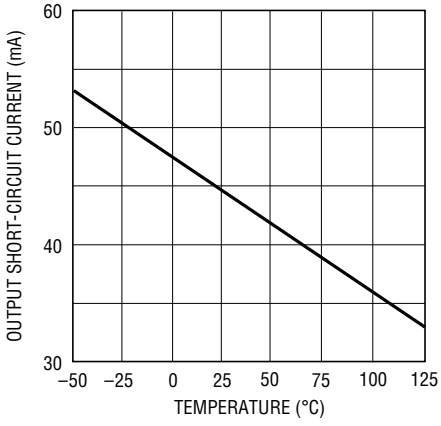
Positive Output Saturation Voltage vs Load Current



Negative Output Saturation Voltage vs Load Current

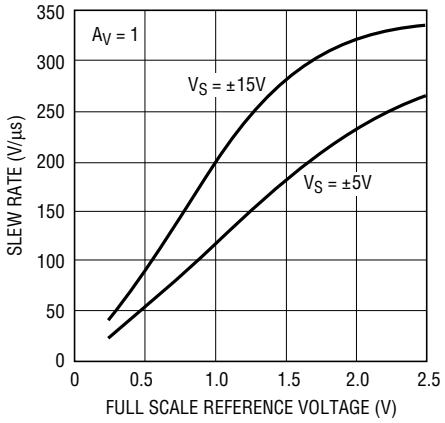


Output Short-Circuit Current vs Temperature



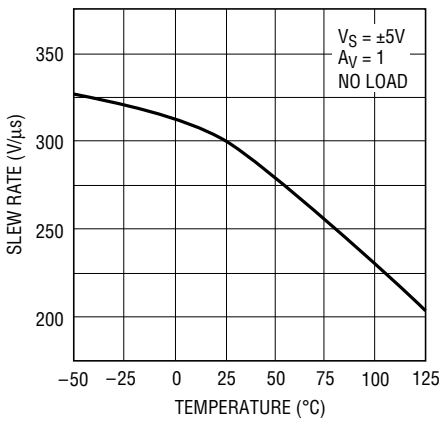
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Full Scale Reference Voltage



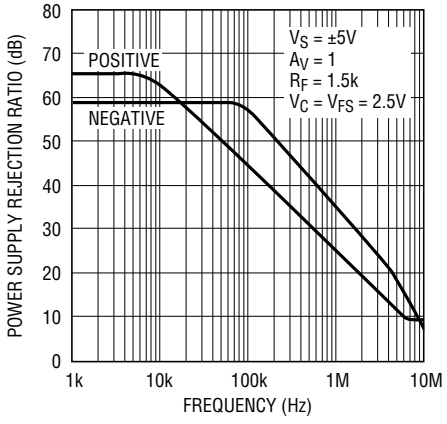
1251/56 G29

Slew Rate vs Temperature



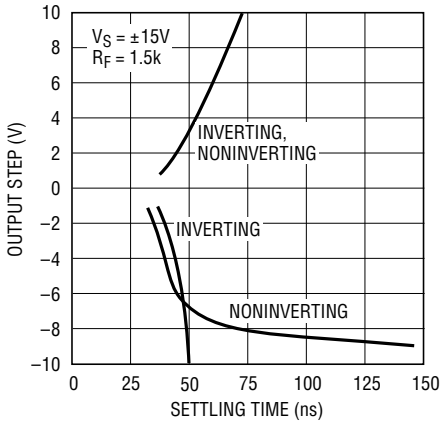
1251/56 G30

Power Supply Rejection Ratio vs Frequency



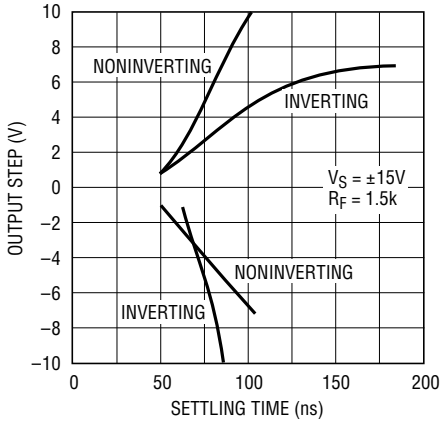
1251/56 G31

Settling Time to 10mV vs Output Step



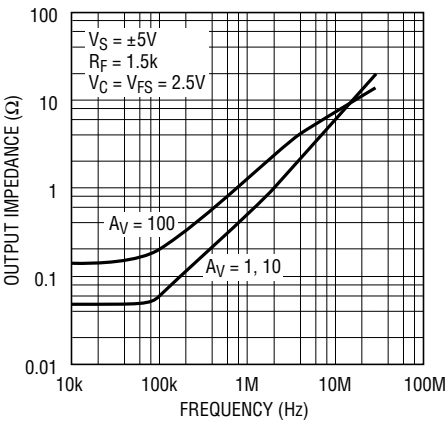
1251/56 G32

Settling Time to 1mV vs Output Step



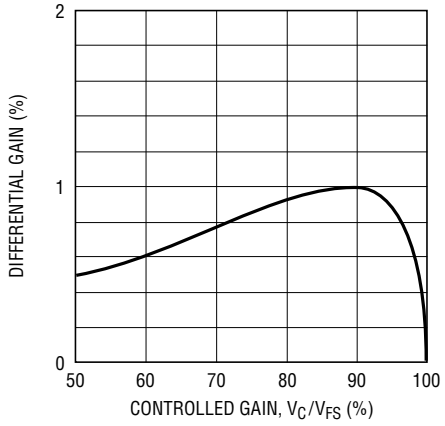
1251/56 G33

Output Impedance vs Frequency



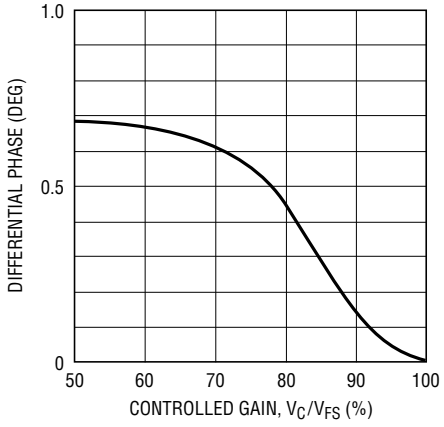
1251/56 G34

Differential Gain vs Controlled Gain



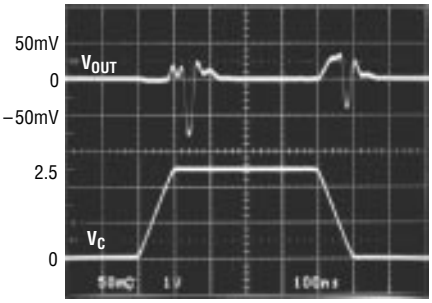
1251/56 G35

Differential Phase vs Controlled Gain



1251/56 G36

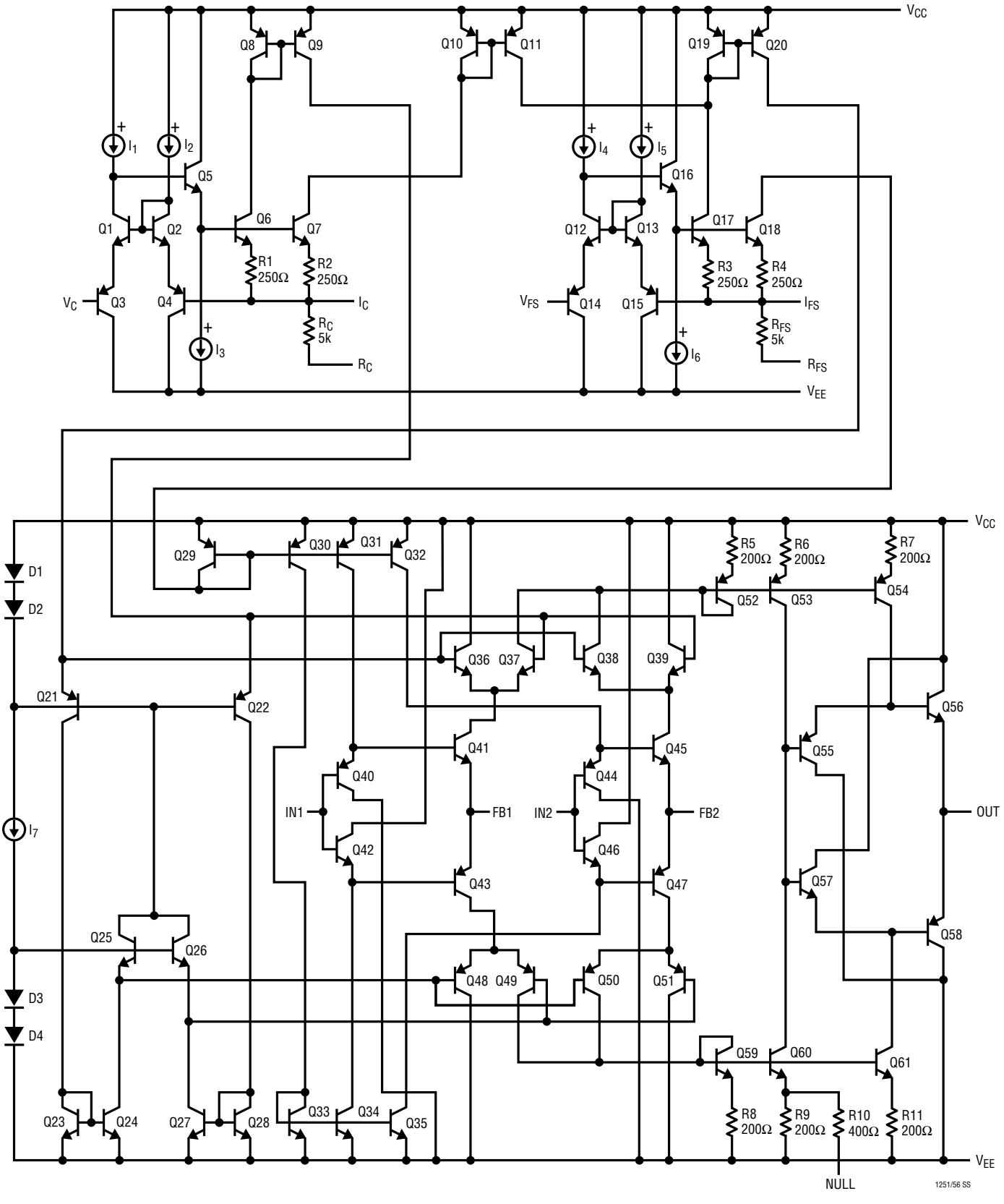
LT1251 Switching Transient (Glitch)



V_{FS} = 2.5V
R_{F1} = R_{F2} = 1.5k
V_S = ±5V

1251/56 G37

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

Supply Voltage

The LT1251/LT1256 are high speed amplifiers. To prevent problems, use a ground plane with point-to-point wiring and small bypass capacitors (0.01μF to 0.1μF) at each supply pin. For good settling characteristics, especially driving heavy loads, a 4.7μF tantalum within an inch or two of each supply pin is recommended.

The LT1251/LT1256 can be operated on single or split supplies. The minimum total supply is 4V (pins 7 to 9). However, the input common-mode range is only guaranteed to within 2V of each supply. On a 4V supply the parts must be operated in the inverting mode with the noninverting input biased half way between pin 7 and pin 9. See the Typical Applications section for the proper biasing for single supply operation.

The op amps in the control section operate from V^- (pin 7) to within 2V of V^+ (pin 9). For this reason the positive supply should be 4.5V or greater in order to use 2.5V control and full scale voltages.

Inputs

The noninverting inputs (pins 1 and 14) are easy to drive since they look like a 17M resistor in parallel with a 1.5pF capacitor at most frequencies. However, the input stage can oscillate at very high frequencies (100MHz to 200MHz) if the source impedance is inductive (like an unterminated cable). Several inches of wire look inductive at these high frequencies and can cause oscillations. Check for oscillations at the inverting inputs (pins 2 and 13) with a 10× probe and a 200MHz oscilloscope. A small capacitor (10pF to 50pF) from the input to ground or a small resistor (100Ω to 300Ω) in series with the input will stop these parasitic oscillations, even when the source is inductive. These components must be within an inch of the IC in order to be effective.

All of the inputs to the LT1251/LT1256 have ESD protection circuits. During normal operation these circuits have no effect. If the voltage between the noninverting and inverting inputs exceeds 6V, the protection circuits will trigger and attempt to short the inputs together. This condition will continue until the voltage drops to less than 500mV or the current to less than 10mA. If a very fast edge is used to measure settling time with an input step of more than 6V, the protection circuits will cause the 1mV settling time to become hundreds of microseconds.

Feedback Resistor Selection

The feedback resistor value determines the bandwidth of the LT1251/LT1256 as in other current feedback amplifiers. The curves in the Typical Performance Characteristics show the effect of the feedback resistor on small-signal bandwidth for various loads, gains and supply voltages. The bandwidth is limited at high gains by the 500MHz to 800MHz gain-bandwidth product as shown in the curves. Capacitance on the inverting input will cause peaking and increase the bandwidth. Take care to minimize the stray capacitance on pins 2 and 13 during printed circuit board layout for flat response.

If the two input stages are not operating with equal gain, the gain versus control voltage characteristic will be nonlinear. This is true even if R_{F1} equals R_{F2}. This is because the open-loop characteristic of a current feedback amplifier is dependent on the Thevenin impedance at the inverting input. For linear control of the gain, the loop gain of the two stages must be equal. For an extreme example, let's take a gain of 101 on input 1, R_{F1} = 1.5k and R_{G1} = 15Ω, and unity-gain on input 2, R_{F2} = 1.5k. The curve in Figure 1 shows about 25% error at mid-scale. To eliminate this nonlinearity we must change the value of R_{F2}. The correct value is the Thevenin impedance at inverting input 1 (including the internal resistance of 27Ω) times the gain set at input 1. For a linear gain versus control voltage characteristic when input 2 is operating at unity-gain, the formula is:

$$R_{F2} = A_{V1} \times (R_{F1} \,||\, R_{G1} + 27)$$

$$R_{F2} = 101 \times (14.85 + 27) = 4227$$

Because the feedback resistor of the unity-gain input is increased, the bandwidth will be lower and the output noise will be higher. We can improve this situation by reducing the values of R_{F1} and R_{G1}, but at high gains the internal 27Ω dominates.

APPLICATIONS INFORMATION

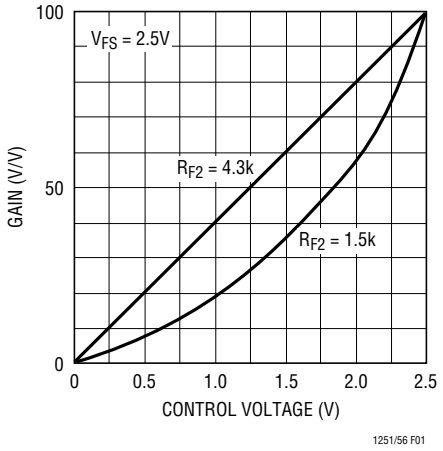


Figure 1. Linear Gain Control from 0 to 101

Capacitive Loads

Increasing the value of the feedback resistor reduces the bandwidth and open-loop gain of the LT1251/LT1256; therefore, the pole introduced by a capacitive load can be overcome. If there is little or no resistive load in parallel with the load capacitance, the output stage will resonate, peak and possibly oscillate. With a resistive load of 150Ω, any capacitive load can be accommodated by increasing the feedback resistor. If the capacitive load cannot be paralleled with a DC load of 150Ω, a network of 200pF in series with 100Ω should be placed from the output to ground. Then the feedback resistor should be selected for best response.

The Null Pin

Pin 6 can be used to adjust the gain of an internal current mirror to change the output offset. The open circuit voltage at pin 6 is set by the full scale current I_{FS} flowing through 200Ω to the negative supply. Therefore, the null pin sits 100mV above the negative supply with V_{FS} equal to 2.5V. Any op amp whose output swings within a few millivolts of the negative supply can drive the null pin. The AM modulator application shows an LT1077 driving the null pin to eliminate the output DC offset voltage.

Crosstalk

The amount of signal from the off input that appears at the output is a function of frequency and the circuit topology. The nature of a current feedback input stage is to force the voltage at the inverting input to be equal to the voltage at the noninverting input. This is independent of feedback and forced by a buffer amplifier between the inputs. When the LT1251/LT1256 are operating noninverting, the off input signal is present at the inverting input. Since one end of the feedback resistor is connected to this input, the off signal is only a feedback resistor away from the output. The amount of unwanted signal at the output is determined by the size of the feedback resistor and the output impedance of the LT1251/LT1256. The output impedance rises with increasing frequency resulting in more crosstalk at higher frequencies. Additionally, the current that flows in the inverting input is diverted to the supplies within the chip and some of this signal will also show up at the output. With a 1.5k feedback resistor, the crosstalk is down about 86dB at low frequencies and rises to –78dB at 1MHz and on to –60dB at 6MHz. The curves show the details.

Distortion

When only one input is contributing to the output (V_C = 0% or 100%) the LT1251/LT1256 have very low distortion. As the control reduces the output, the distortion will increase. The amount of increase is a function of the current that flows in the inverting input. Larger input signals generate more distortion. Using a larger feedback resistor will reduce the distortion at the expense of higher output noise.

APPLICATIONS INFORMATION

Signal Path Description

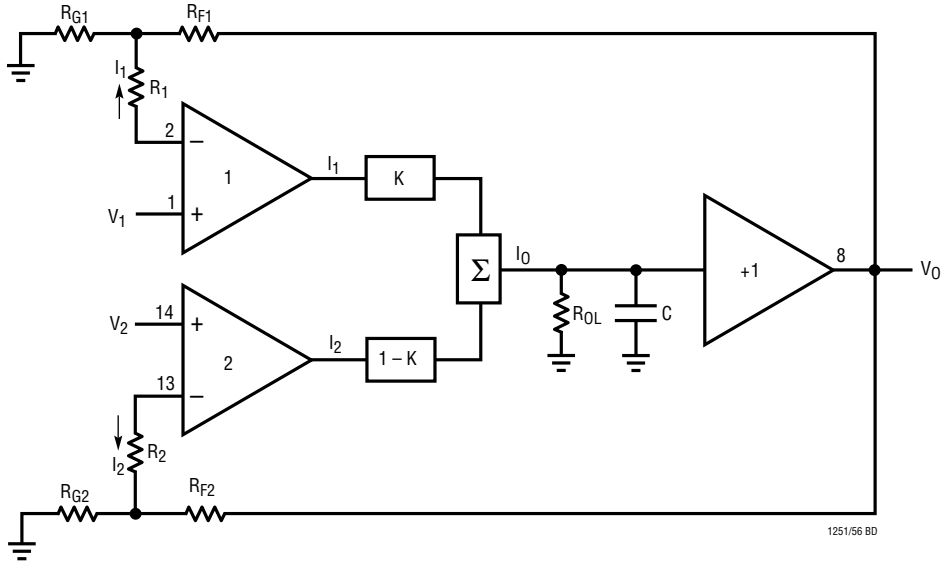


Figure 2. Signal Path Block Diagram

Figure 2 is the basic block diagram of the LT1251/LT1256 signal path with external resistors R_{G1}, R_{F1}, R_{G2} and R_{F2}. Both input stages are operating as noninverting amplifiers with two input signals V_1 and V_2.

Each input stage has a unity-gain buffer from the noninverting input to the inverting input. Therefore, the inverting input is at the same voltage as the noninverting input. R_1 and R_2 represent the internal output resistances of these buffers, approximately 27Ω.

K is a constant determined by the control circuit, and can be any value between 0 and 1. The control circuit is described in a later section.

By inspection of the diagram:

$$I_1 = \frac{V_1}{R_1 + \frac{(R_{G1})(R_{F1})}{R_{G1} + R_{F1}}} - \frac{V_0}{R_{F1} + R_1\left(\frac{R_{F1}}{R_{G1}} + 1\right)}$$

$$I_2 = \frac{V_2}{R_2 + \frac{(R_{G2})(R_{F2})}{R_{G2} + R_{F2}}} - \frac{V_0}{R_{F2} + R_2\left(\frac{R_{F2}}{R_{G2}} + 1\right)}$$

$$I_0 = KI_1 + (1-K)I_2$$

$$V_0 = I_0\left(\frac{R_{OL}}{(1 + sR_{OL}C)}\right)$$

Substituting and rearranging gives:

$$V_0 = \frac{\frac{KV_1}{R_1 + \frac{(R_{G1})(R_{F1})}{R_{G1} + R_{F1}}} + \frac{(1-K)V_2}{R_2 + \frac{(R_{G2})(R_{F2})}{R_{G2} + R_{F2}}}}{\frac{1 + sR_{OL}C}{R_{OL}} + \frac{K}{R_{F1} + R_1\left(\frac{R_{F1}}{R_{G1}} + 1\right)} + \frac{(1-K)}{R_{F2} + R_2\left(\frac{R_{F2}}{R_{G2}} + 1\right)}}$$

General Equation for the Noninverting Amplifier Case

APPLICATIONS INFORMATION

In low gain applications, R_1 and R_2 are small compared to the feedback resistors and therefore we can simplify the equation to:

$$V_O = \frac{\dfrac{KV_1}{(R_{G1})(R_{F1})} + \dfrac{(1-K)V_2}{(R_{G2})(R_{F2})}}{\dfrac{R_{G1}+R_{F1}}{R_{G2}+R_{F2}}} \Bigg/ \left(\frac{1+sR_{OL}C}{R_{OL}} + \frac{K}{R_{F1}} + \frac{(1-K)}{R_{F2}}\right)$$

Note that the denominator causes a gain error due to the open-loop gain (typically 0.1% for frequencies below 20kHz) and for mismatches in R_{F1} and R_{F2}. A 1% mismatch in the feedback resistors results in a 0.25% error at K = 0.5.

If we set $R_{F1} = R_{F2}$ and assume $R_{OL} >> R_{F1}$ (a 0.1% error at low frequencies) the above equation simplifies to:

$$V_O = KV_1A_{V1} + (1-K)V_2A_{V2}$$

$$\text{where} \quad A_{V1} = 1 + \frac{R_{F1}}{R_{G1}} \quad \text{and} \quad A_{V2} = 1 + \frac{R_{F2}}{R_{G2}}$$

This shows that the output fades linearly from input 2, times its gain, to input 1, times its gain, as K goes from 0 to 1.

If only one input is used (for example, V_1) and pin 14 is grounded, then the gain is proportional to K.

$$\frac{V_O}{V_1} = KA_{V1}$$

Similarly for the inverting case where the noninverting inputs are grounded and the input voltages V_1 and V_2 drive the normally grounded ends of R_{G1} and R_{G2}, we get:

$$V_O = -\frac{\dfrac{KV_1}{R_{G1}+R_1\left(\dfrac{R_{G1}}{R_{F1}}+1\right)} + \dfrac{(1-K)V_2}{R_{G2}+R_2\left(\dfrac{R_{G2}}{R_{F2}}+1\right)}}{\dfrac{1+sR_{OL}C}{R_{OL}} + \dfrac{K}{R_{F1}+R_1\left(\dfrac{R_{F1}}{R_{G1}}+1\right)} + \dfrac{(1-K)}{R_{F2}+R_2\left(\dfrac{R_{F2}}{R_{G2}}+1\right)}}$$

General Equation for the Inverting Amplifier Case

Note that the denominator is the same as the noninverting case. In low gain applications, R_1 and R_2 are small compared to the feedback resistors and therefore we can simplify the equation to:

$$V_O = -\frac{\dfrac{KV_1}{R_{G1}} + \dfrac{(1-K)V_2}{R_{G2}}}{\dfrac{1+sR_{OL}C}{R_{OL}} + \dfrac{K}{R_{F1}} + \dfrac{(1-K)}{R_{F2}}}$$

Again if we set $R_{F1} = R_{F2}$ and assume $R_{OL} >> R_{F1}$ (a 0.1% error at low frequencies) the above equation simplifies to:

$$V_O = -\left[KV_1A_{V1} + (1-K)V_2A_{V2}\right]$$

$$\text{where} \quad A_{V1} = \frac{R_{F1}}{R_{G1}} \quad \text{and} \quad A_{V2} = \frac{R_{F2}}{R_{G2}}$$

The four-resistor difference amplifier yields the same result as the inverting amplifier case, and the common-mode rejection is independent of K.

APPLICATIONS INFORMATION

Control Circuit Description

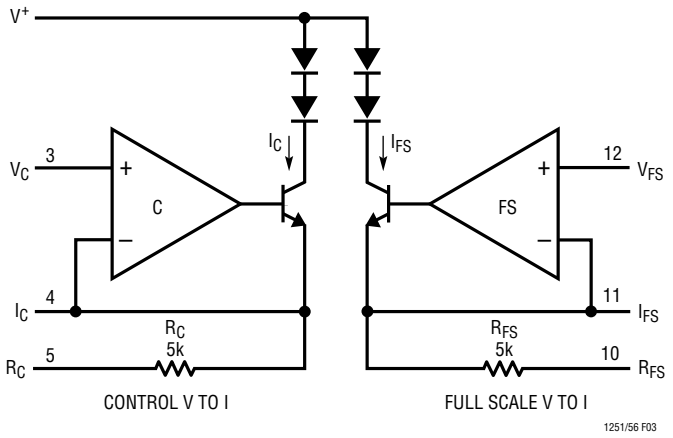


Figure 3. Control Circuit Block Diagram

The control section of the LT1251/LT1256 consists of two identical voltage-to-current converters (V-to-I); each V-to-I contains an op amp, an NPN transistor and a resistor. The converter on the right generates a *full scale* current I_{FS} and the one on the left generates a *control* current I_C. The ratio I_C/I_{FS} is called K. K goes from a minimum of zero (when I_C is zero) to a maximum of one (when I_C is equal to, or greater than, I_{FS}). K determines the gain from each signal input to the output.

The op amp in each V-to-I drives the transistor until the voltage at the inverting input is the same as the voltage at the noninverting input. If the open end of the resistor (pin 5 or 10) is grounded, the voltage across the resistor is the same as the voltage at the noninverting input. The emitter current is therefore equal to the input voltage V_C divided by the resistor value R_C. The collector current is essentially the same as the emitter current and it is the ratio of the two collector currents that sets the gain.

The LT1251/LT1256 are tested with pins 5 and 10 grounded and a full scale voltage of 2.5V applied to V_{FS} (pin 12). This sets I_{FS} at approximately 500μA; the control voltage V_C is applied to pin 3. When the control voltage is negative or zero, I_C is zero and K is zero. When V_C is 2.5V or greater, I_C is equal to or greater than I_{FS} and K is one. The gain of channel one goes from 0% to 100% as V_C goes from zero to 2.5V. The gain of channel two goes the opposite way, from 100% down to 0%. The worst case error in K (the gain) is ±3% as detailed in the electrical tables. By using a 2.5V full scale voltage and the internal resistors, no additional errors need be accounted for.

In the LT1256, K changes linearly with I_C. To insure that K is zero, V_C must be negative 15mV or more to overcome the worst case control op amp offset. Similarly to insure that K is 100%, V_C must be 3% larger than V_{FS} based on the guaranteed gain accuracy.

To eliminate the overdrive requirement, the LT1251 has internal circuitry that senses when the control current is at about 5% and sets K to 0%. Similarly, at about 95% it sets K to 100%. The LT1251 guarantees that a 2% (50mV) input gives zero and 98% (2.45V) gives 100%.

The operating currents of the LT1251/LT1256 are derived from I_{FS} and therefore the quiescent current is a function of V_{FS} and R_{FS}. The electrical tables show the supply current for three values of V_{FS} including zero. An approximate formula for the supply current is:

$$I_S = 1mA + (24 \times I_{FS}) + (V_S/20k)$$

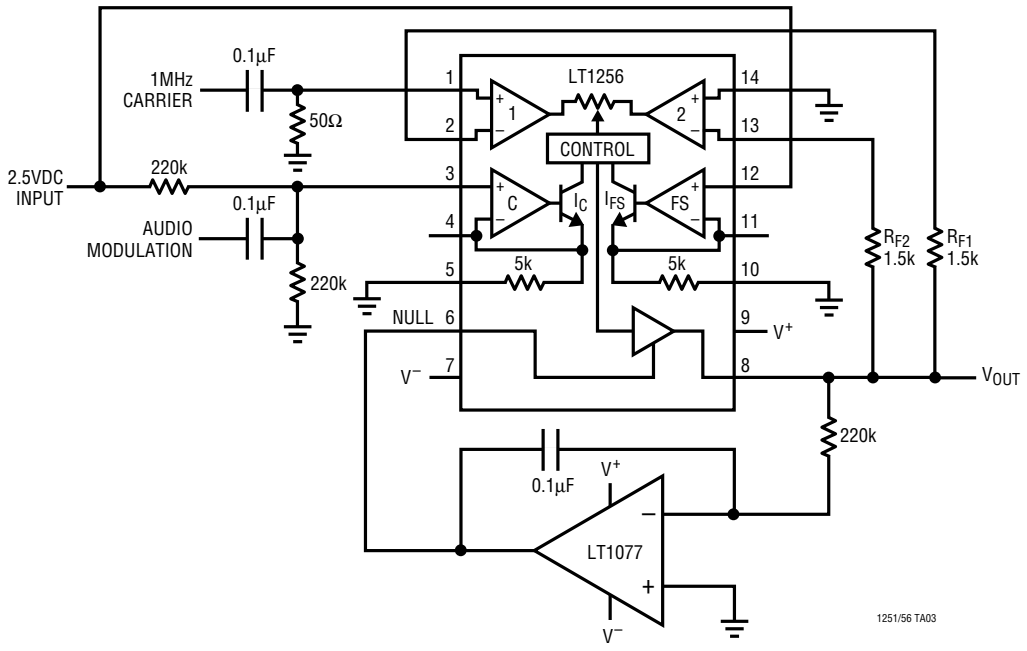
where V_S is the total supply voltage between pins 9 and 7. By reducing I_{FS} the supply current can be reduced, however the slew rate and bandwidth will also be reduced as indicated in the characteristic curves. Using the internal resistors (5k) with V_{FS} equal to 2.5V results in I_{FS} equal to 500μA; there is no reason to use a larger value of I_{FS}.

The inverting inputs of the V-to-I converters are available so that external resistors can be used instead of the internal ones. For example, if a 10V full scale voltage is desired, an external pair of 20k resistors should be used to set I_{FS} to 500μA. The positive supply voltage must be 2.5V greater than the maximum V_C and/or V_{FS} to keep the transistors from saturating. Do not use the internal resistors with external resistors because the internal resistors have a large positive temperature coefficient (0.2%/°C) that will cause gain errors.

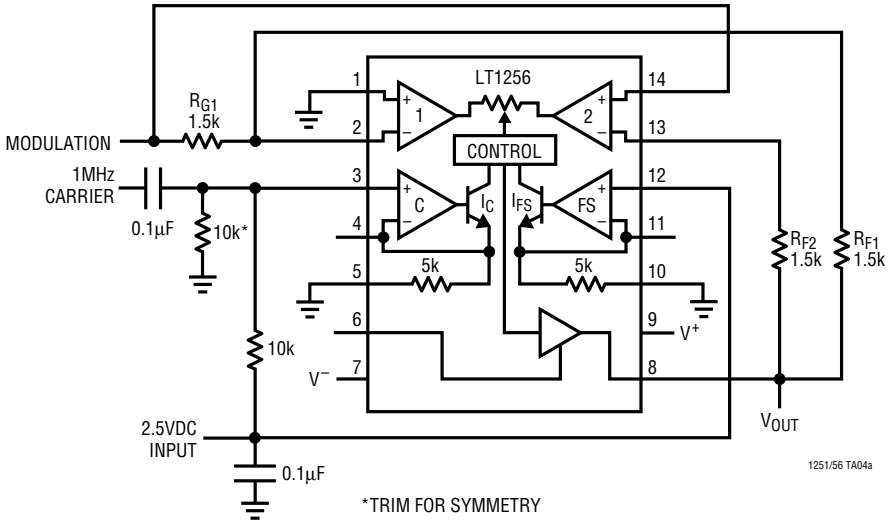
If the control voltage is applied to the free end of resistor R_C (pin 5) and the V_C input (pin 3) is grounded, the polarity of the control voltage must be inverted. Therefore, K will be 0% for zero input and 100% for –2.5V input, assuming V_{FS} equals 2.5V. With pin 3 grounded, pin 4 is a virtual ground; this is convenient for summing several negative going control signals.

TYPICAL APPLICATIONS

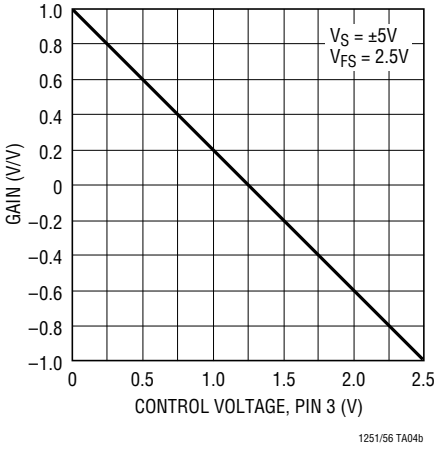
AM Modulator with DC Output Nulling Circuit



Four-Quadrant Multiplier as a Double-Sideband Suppressed-Carrier Modulator

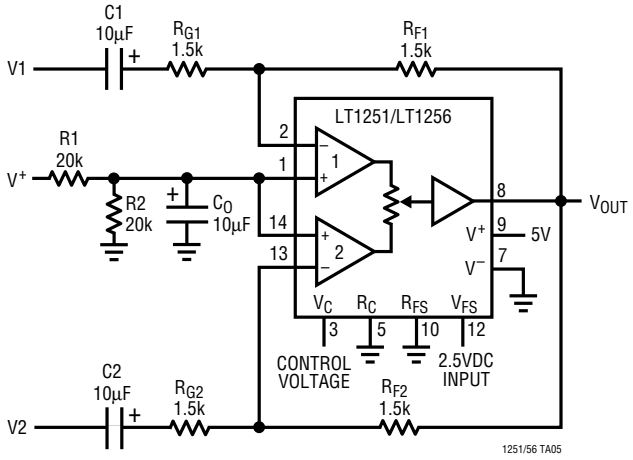


Modulation Gain vs Control Voltage

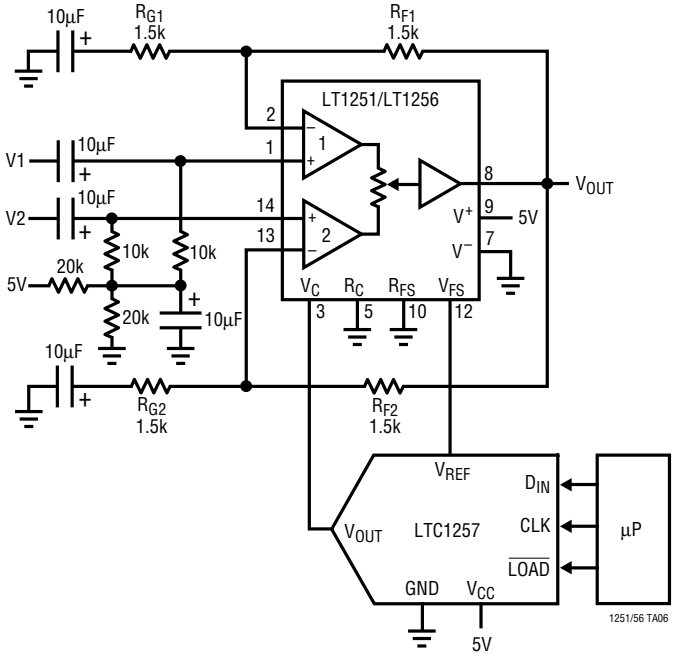


TYPICAL APPLICATIONS

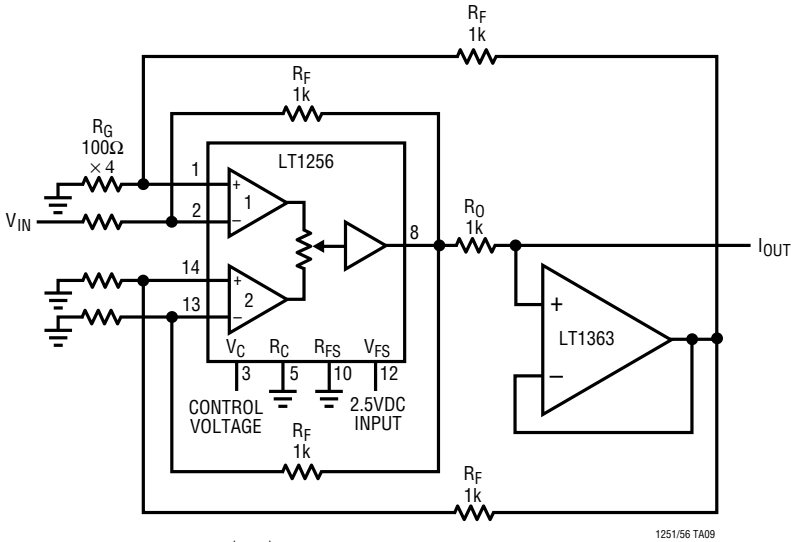
Single Supply Inverting AC Amplifier



Single Supply Noninverting AC Amplifier with Digital Gain Control



Controlled Gain, Voltage-to-Current Converter (Current Source)

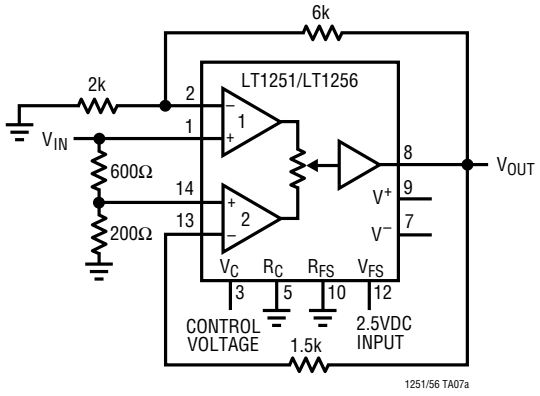


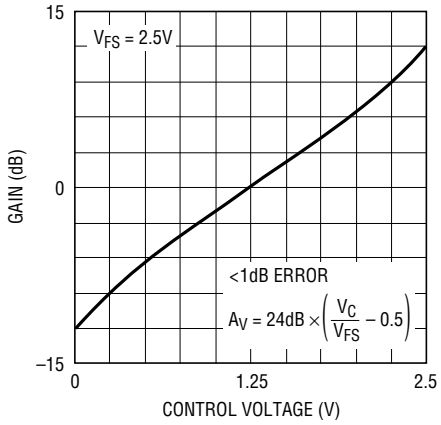
$$I_{OUT} = \frac{V_{IN}}{R_O}\left(\frac{R_F}{R_G}\right)\frac{V_C}{V_{FS}}$$

OUTPUT RESISTANCE DEPENDS ON MATCHING OF RESISTORS

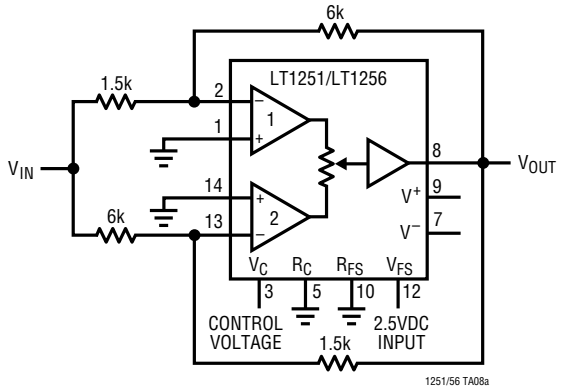
TYPICAL APPLICATIONS

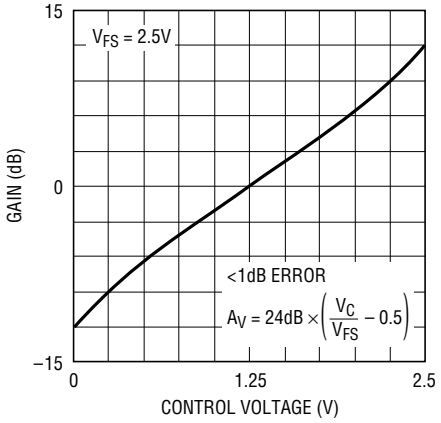
Logarithmic Gain Control (Noninverting)



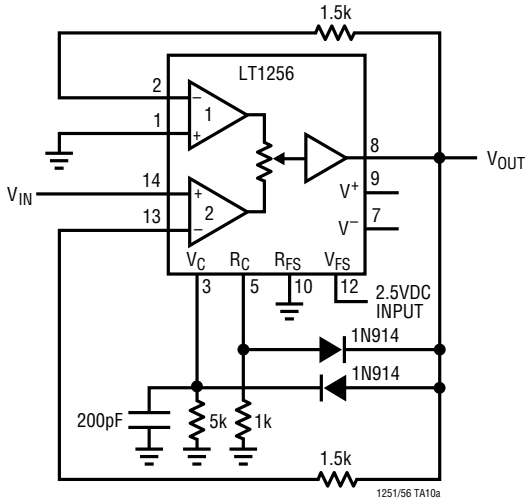


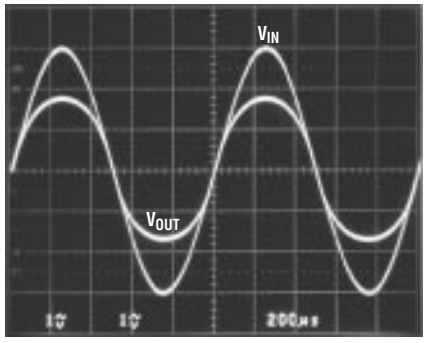
Logarithmic Gain Control (Inverting)





Soft Clipper



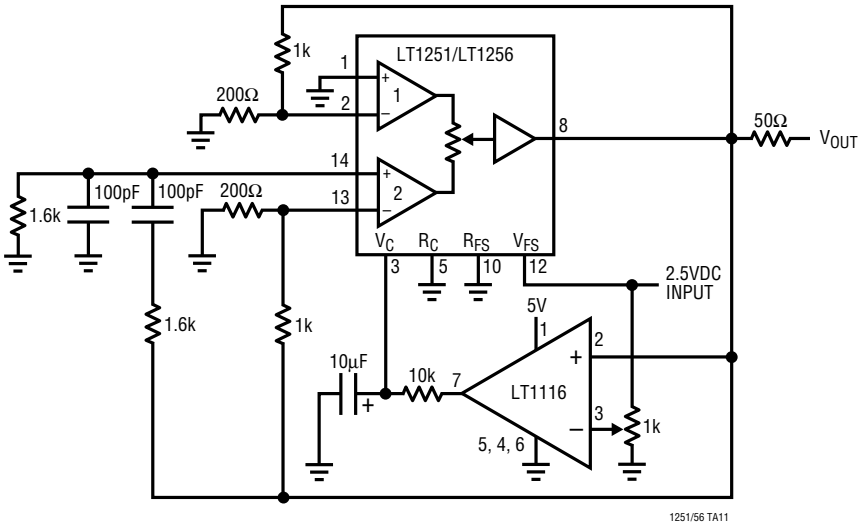


VFS = 2.5V
VS = ±5V
f = 1kHz

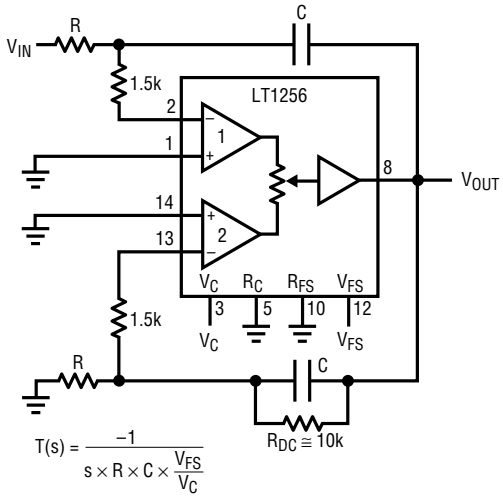
1251/56 TA10b

TYPICAL APPLICATIONS

1MHz Wien Bridge Oscillator



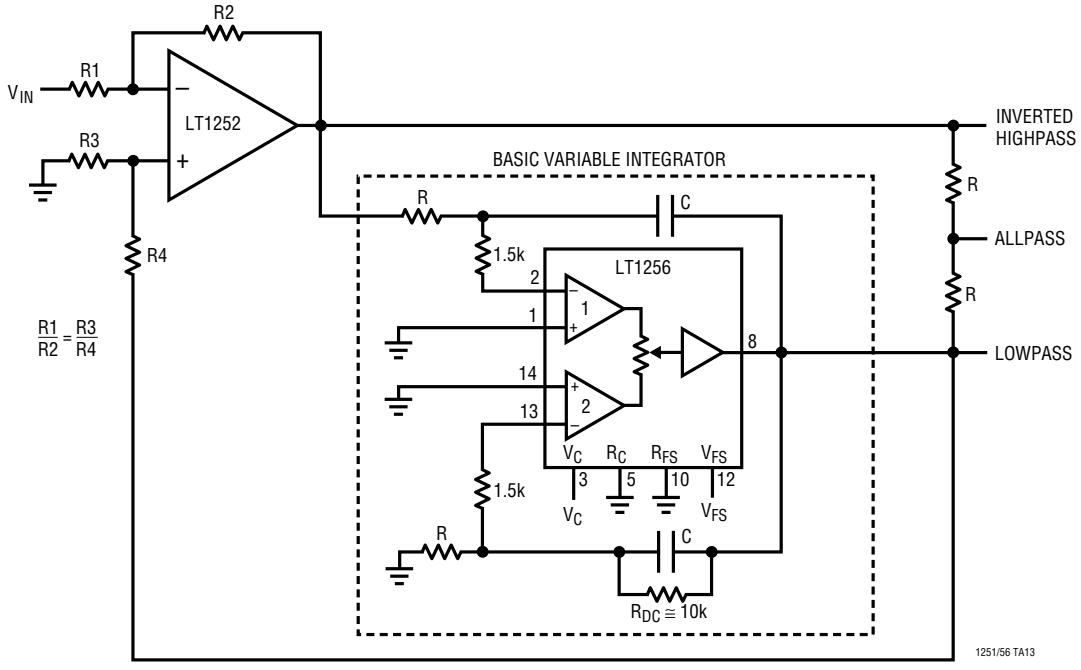
Basic Variable Integrator



THE TIME CONSTANT IS INVERSELY PROPORTIONAL TO V_C. R_{DC} IS REQUIRED TO DEFINE THE DC OUTPUT WHEN THE CONTROL IS AT ZERO.

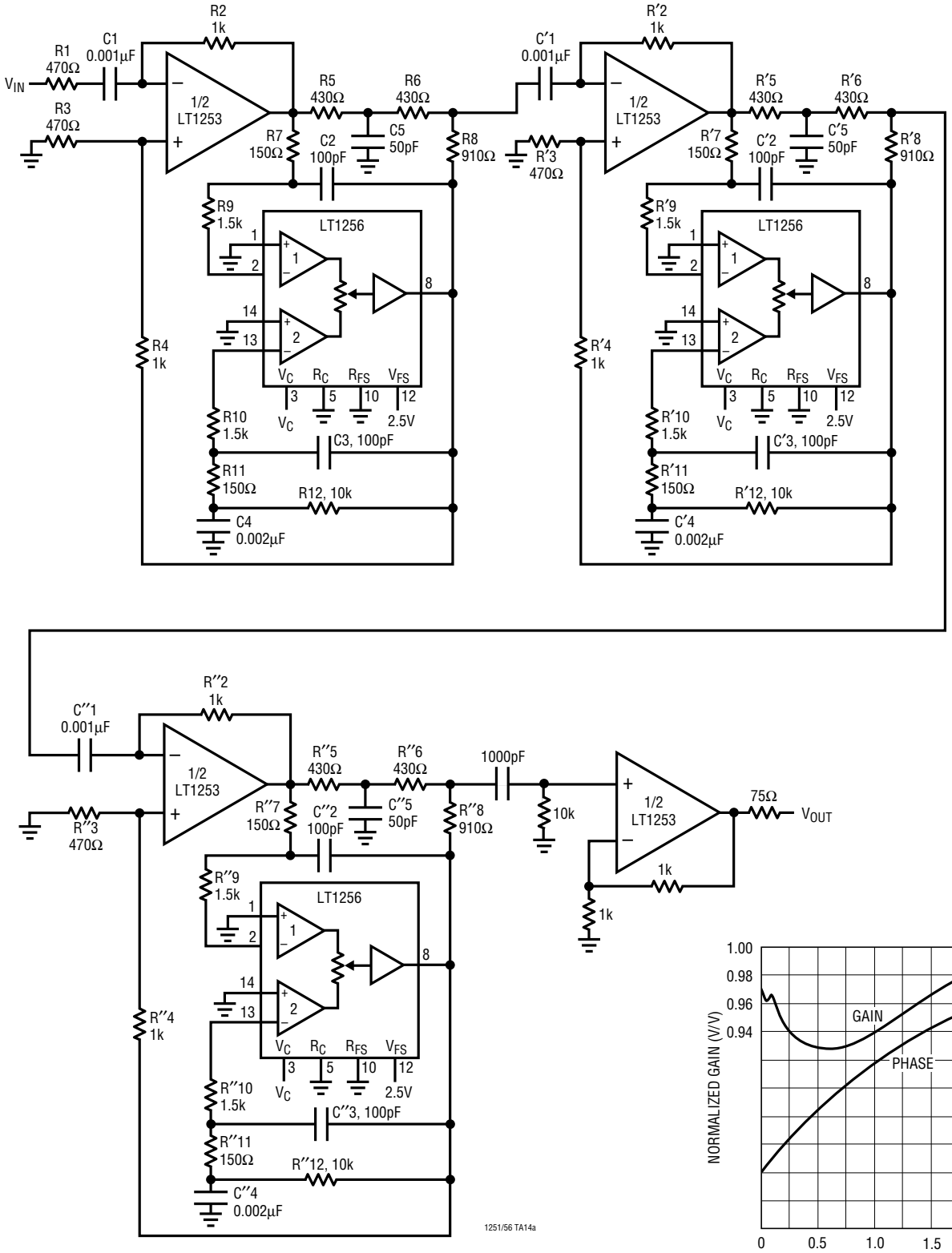
1251/56 TA12

Variable Lowpass, Highpass and Allpass Filter



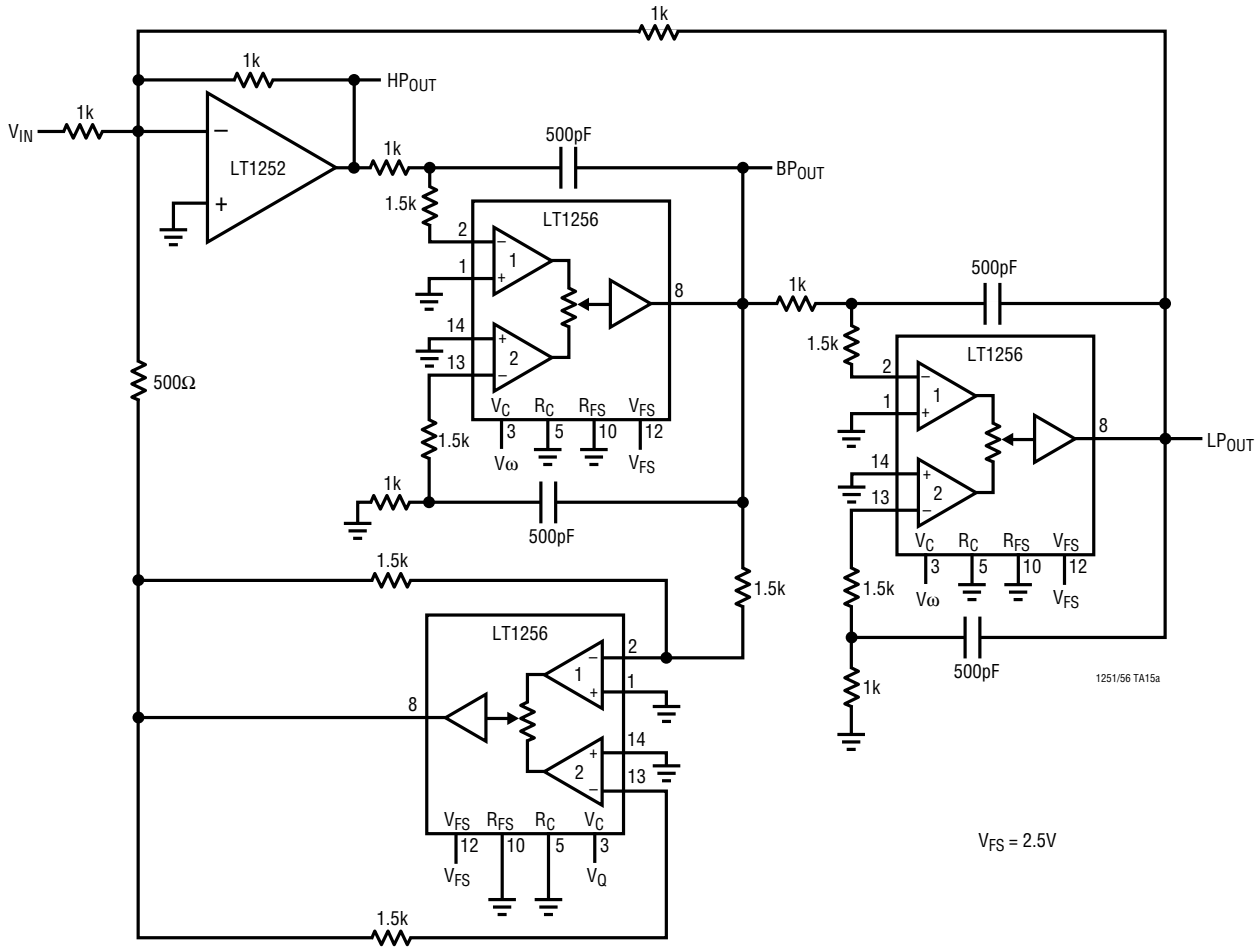
TYPICAL APPLICATIONS

3.58MHz Phase Shifter

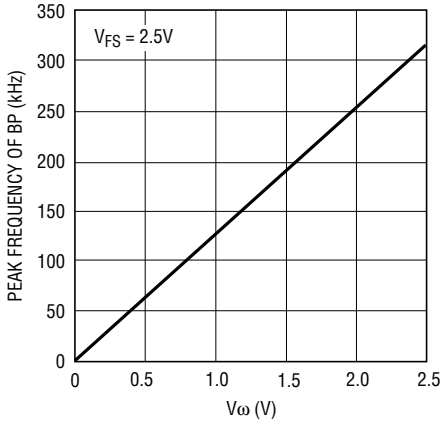


TYPICAL APPLICATIONS

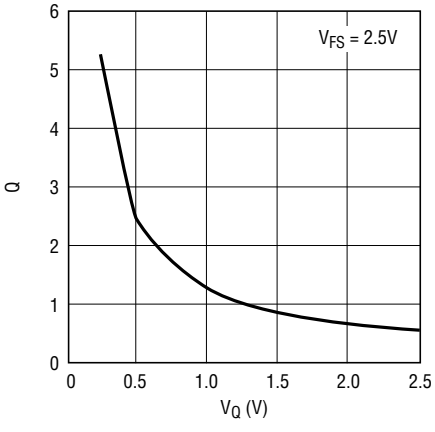
State Variable Filter with Adjustable Frequency and Q



Center Frequency vs Control Voltage Vω



Q vs Control Voltage V_Q



MACROMODEL

For PSpice™

```
*
* Linear Technology LT1251/LT1256 VIDEO FADER MACROMODEL
* Written: 3-11-1994 BY WILLIAM H. GROSS.
*
* Connections: as per datasheet pinout
*1=first noninverting input
*2=first inverting input
*3=control voltage input
*4=control current input
*5=control resistor, RC
*6=null input
*7=positive supply
*8=output
*9=negative supply
*10=full scale resistor, RFS
*11=full scale current input
*12=full scale voltage input
*13=second inverting input
*14=second noninverting input
*
.SUBCKT LT1251 1 2 3 4 5 6 7 8 9 10 11 12 13 14
*
*first input stage
IB1       1     0     500NA
RI1       1     0     17MEG
C1        1     0     1.5PF
E1       2A     0     VALUE={LIMIT (V(1), V(8N)+0.4, V(8P)-0.4)+V(EN)/30}
VOS1     2A    2B     2.5MV
R1       2B     2     27
C2        2     0     1PF
*
*second input stage
IB2      14     0     450NA
RI2      14     0     17MEG
C14      14     0     1.5PF
E2      13A     0     VALUE={LIMIT (V(14), V(8N)+0.4, V(8P)-0.4)+V(EN)/30}
VOS2    13A    13B    1.5MV
R2      13B    13     27
C13      13     0     1PF
*
*control amp
IBC       3     0     -300NA
RIC       3     0     100MEG
C3        3     0     1PF
R3        3    3A     1600
CBWC     3A     0     10PF
EC       3B     0     3A     0    1.0
VOSC     3B     4     5MV
C4        4     0     1PF
RC        4     5     5K
C5        5     0     1PF
*
```

PSpice is a trademark of MicroSim Corporation

MACROMODEL

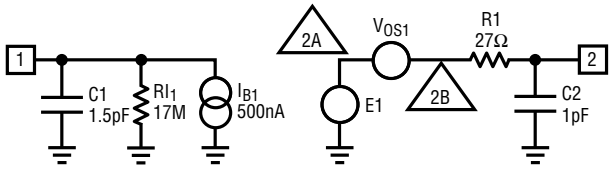
```
*full scale amp
IBFS     12      0      -300NA
RIFS     12      0      100MEG
C12      12      0      1PF
R12      12    12A      1600
CBWFS   12A      0      10PF
EFS     12B      0      12A    0     1.0
VOSFS   12B     11      -5MV
C11      11      0      1PF
RFS      11     10      5K
C10      10      0      1PF
*
*generating K
*** the next two lines are for the LT1251
EK K 0 TABLE {I(VOSC)/I(VOSFS)}=  (-100,0)    (0.04,0)    (0.1,0.11)
+                                 (0.9,0.907) (0.95,1.0)  (100,1.0)
*** the next two lines are for the LT1256
*EK K 0 TABLE {I(VOSC)/I(VOSFS)}= (-100,0)    (0,0)       (0.2,0.21)
*+                                (0.9,0.9)   (1.0,1.0)   (100,1.0)
RDUMMY    K      0      1MEG
RNOISE1  EN      0      200K
RNOISE2  EN      0      200K
*generates 40.7nV/rtHz
*
*null circuit
GNULL     9     6A      VALUE={I(VOSFS)}
RN1      6A      9      200
VNULL    6A     6B      0.0V
RN2      6B      6      400
C6        6      9      1PF
*
*output stage
E6       8A      0
+VALUE={1.8MEG*(I(VOS1)*V(K)+I(VOS2)*(1-V(K))-I(VNULL)+0.10UA+0.0007*V(EN))}
RG       8A     8B      1.8MEG
CG       8B      0      3.4PF
E8       8C      0      8B      0     1.0
V8       8C     8D      0.0V
R8       8D      8      11
*
*output swing and current limit
DP       8B     8P      D1
VDP      8P      7      -1.4V
DN       8N     8B      D1
VDN      8N      9      1.4V
.MODEL   D1      D
GCL      8B      0      TABLE {I(V8)}=(-1,-1)(-0.04,0)(0.04,0)(1,1)
*
*supply current
GQ        7      9      VALUE={1MA+24*I(VOSFS)+(V(7)-V(9))/20K}
GCC       7      0      TABLE {I(V8)}=(-1,0)(0,0)(1,1)
GEE       9      0      TABLE {I(V8)}=(-1,-1)(0,0)(1,0)
*
.ENDS LT1251
```

MACROMODEL

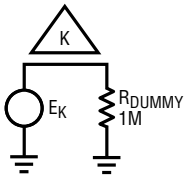
LT1251/LT1256 Macro Model for PSpice

PIN # IN □ NODE # IN △

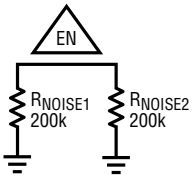
FIRST INPUT STAGE



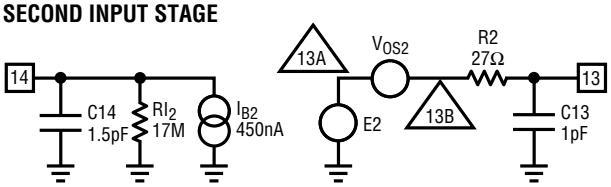
K GENERATOR



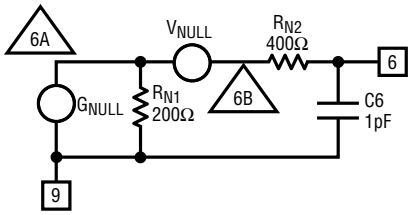
NOISE GENERATOR



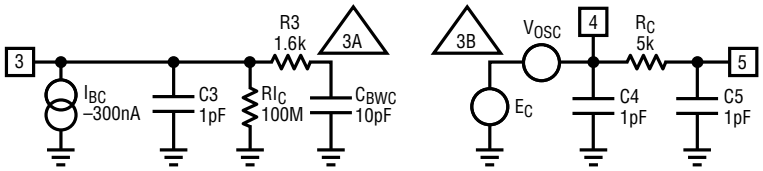
SECOND INPUT STAGE



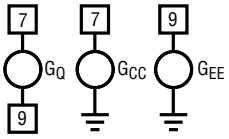
NULL CIRCUIT



CONTROL AMP

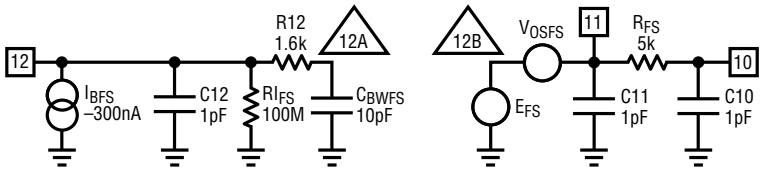


SUPPLY CURRENTS

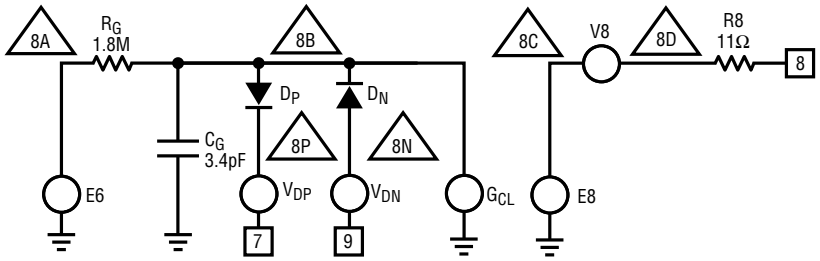


1251/56 MM

FULL SCALE AMP



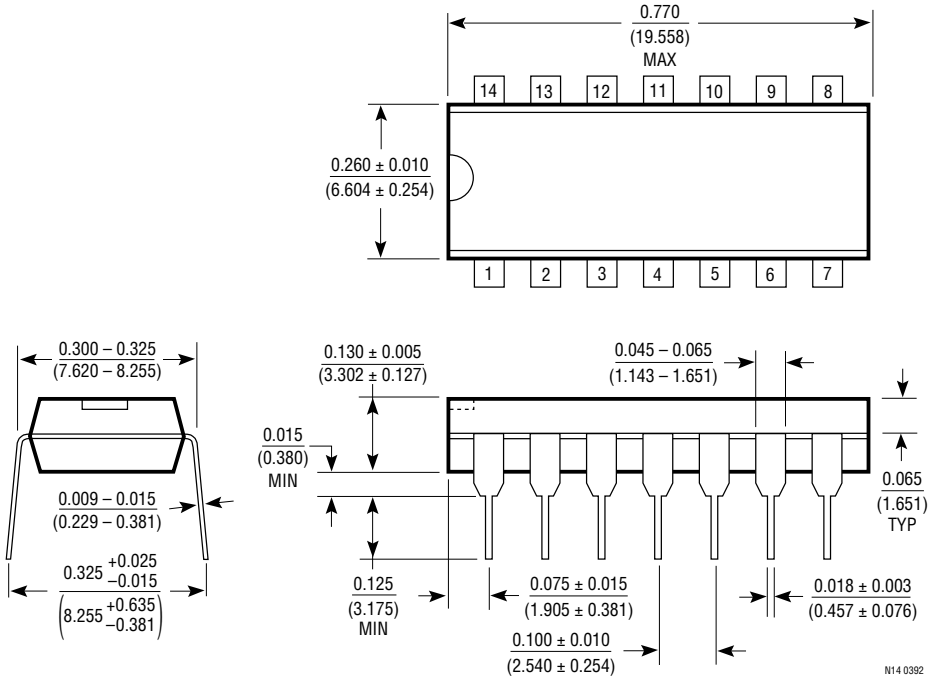
OUTPUT STAGE AND VOLTAGE SWING/CURRENT LIMIT



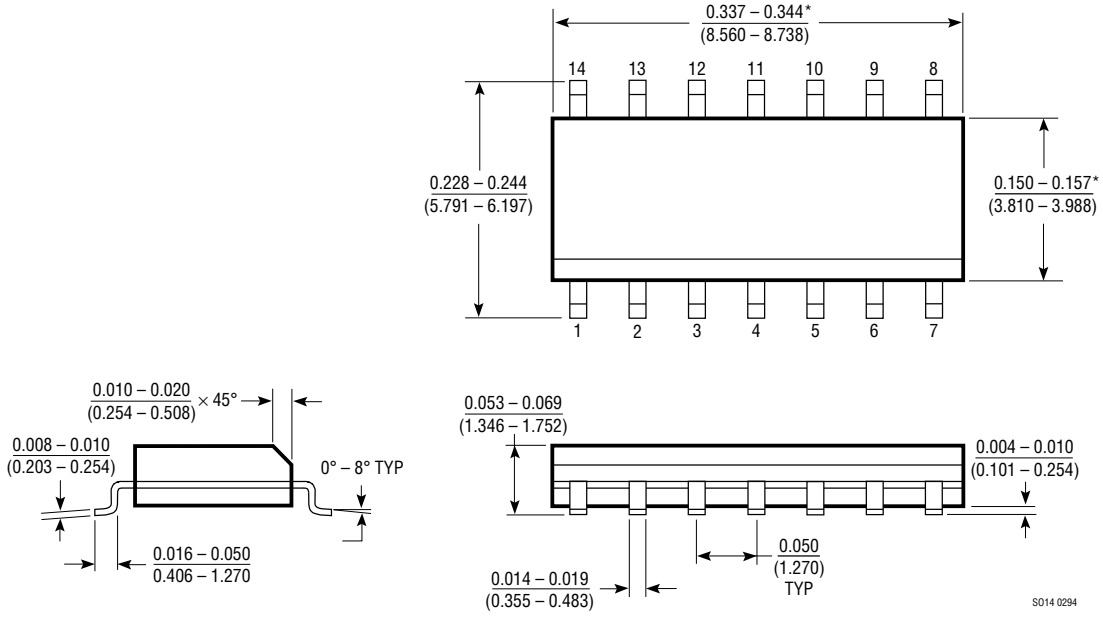
PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

N Package
14-Lead Plastic DIP



S Package
14-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).