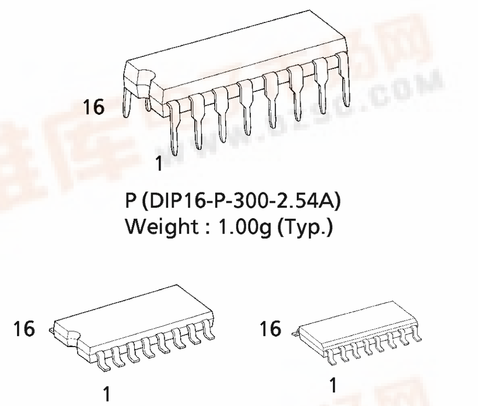
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC283AP, TC74HC283AF, TC74HC283AFN

4 – BIT BINARY FULL ADDER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74HC283A is a high speed CMOS 4 - BIT BINARY FULL ADDER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit.
This adder features full internal look - ahead across all four bits.
A4 × n bit binary adder is easily built up by cascading the HC283A without any additional logic.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

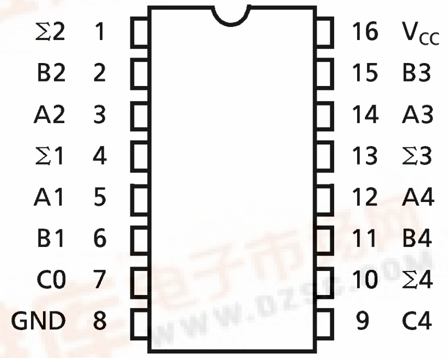
F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

FEATURES :

- High Speed ···························· t_{pd} = 17ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ··············· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ··················· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ············ 10 LSTTL Loads
- Symmetrical Output Impedance··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS283

PIN ASSIGNMENT

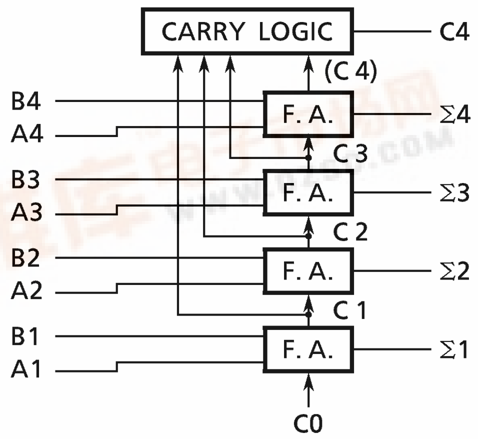


(TOP VIEW)

TRUTH TABLE (1bit)

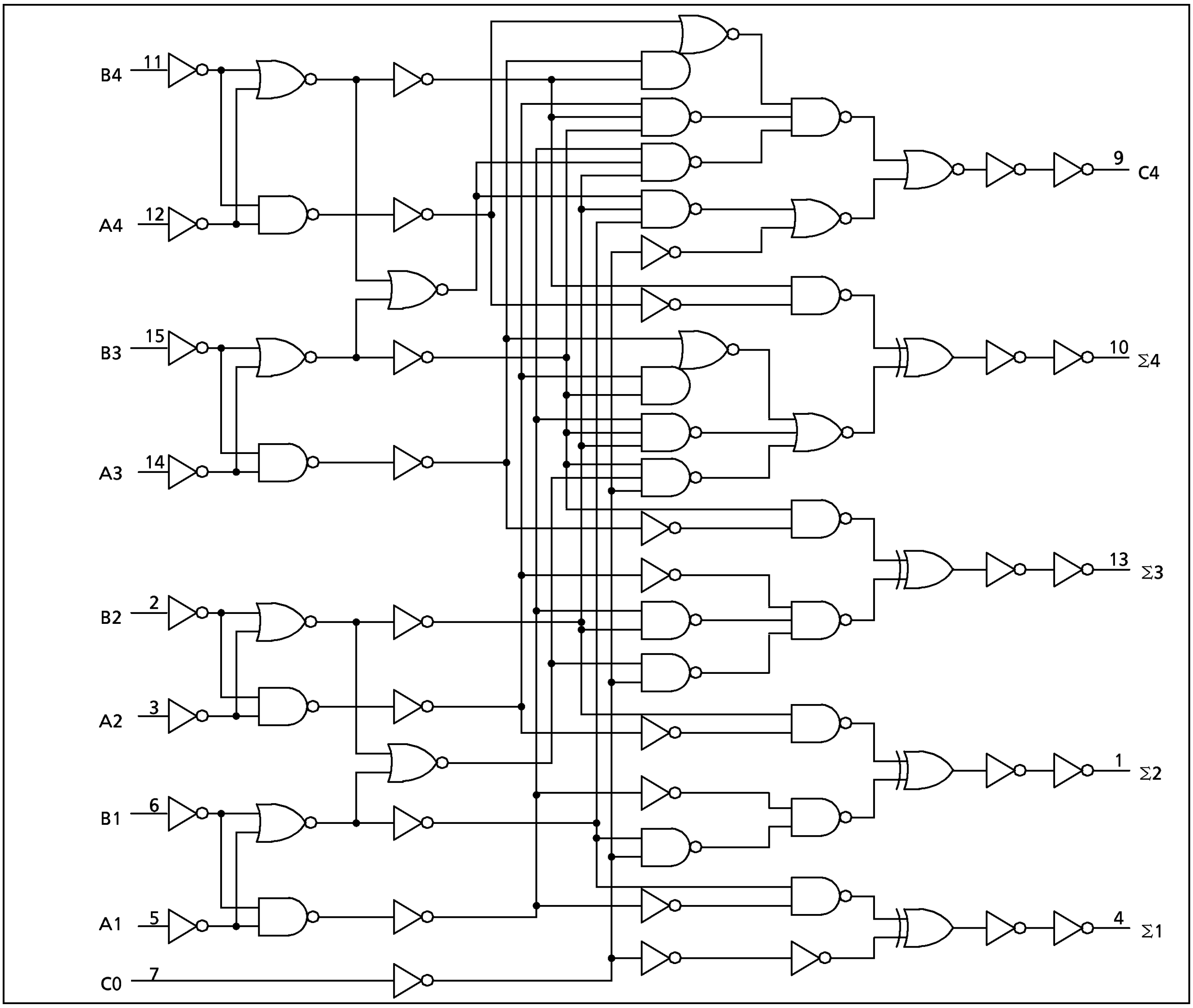
INPUTS			OUTPUTS	
Bn	An	Cn − 1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

BLOCK DIAGRAM

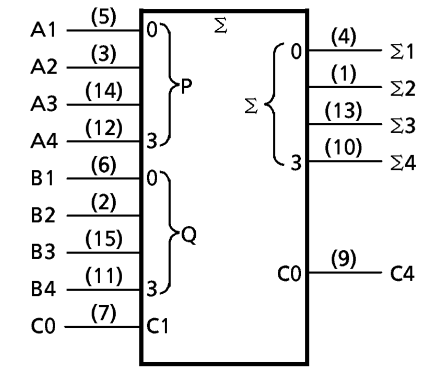


980910EBA2

SYSTEM DIAGRAM



IEC LOGIC SYMBOL



980910EBA2'

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5\sim7$	V
DC Input Voltage	V_{IN}	$-0.5\sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5\sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65\sim150$	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2\sim6$	V
Input Voltage	V_{IN}	$0\sim V_{CC}$	V
Output Voltage	V_{OUT}	$0\sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40\sim85$	°C
Input Rise and Fall Time	t_r, t_f	$0\sim1000$ ($V_{CC}=2.0$V) $0\sim500$ ($V_{CC}=4.5$V) $0\sim400$ ($V_{CC}=6.0$V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$I_{OH}=-20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			$I_{OH}=-4$ mA $I_{OH}=-5.2$ mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	$I_{OL}=20\mu A$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$I_{OL}=4$ mA $I_{OL}=5.2$ mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (C0 − Σn)	t_{pLH} t_{pHL}		—	17	26	
Propagation Delay Time (C0 − C4)	t_{pLH} t_{pHL}		—	17	26	
Propagation Delay Time (An, Bn − Σn)	t_{pLH} t_{pHL}		—	23	37	
Propagation Delay Time (An, Bn − C4)	t_{pLH} t_{pHL}		—	21	34	

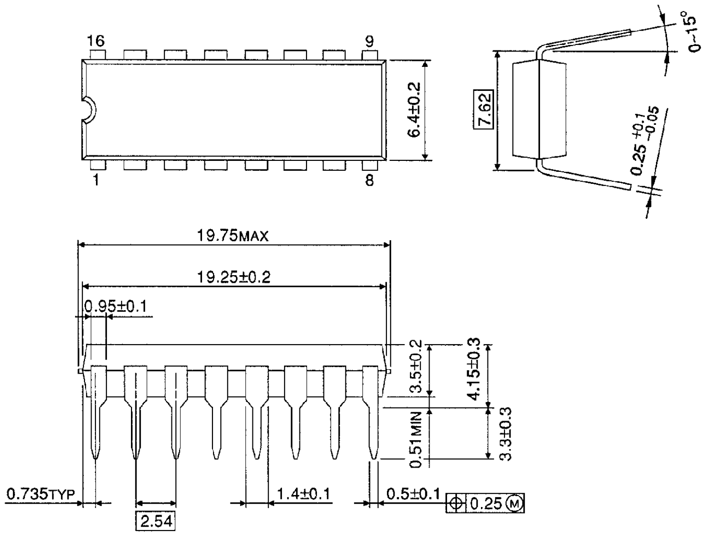
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (C0 − Σn)	t_{pLH} t_{pHL}		2.0	—	60	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	32	
Propagation Delay Time (C0 − C4)	t_{pLH} t_{pHL}		2.0	—	60	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	32	
Propagation Delay Time (An, Bn − Σn)	t_{pLH} t_{pHL}		2.0	—	95	210	—	265	
			4.5	—	27	42	—	53	
			6.0	—	22	36	—	45	
Propagation Delay Time (An, Bn − C4)	t_{pLH} t_{pHL}		2.0	—	80	195	—	245	
			4.5	—	25	39	—	49	
			6.0	—	20	33	—	42	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	126	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

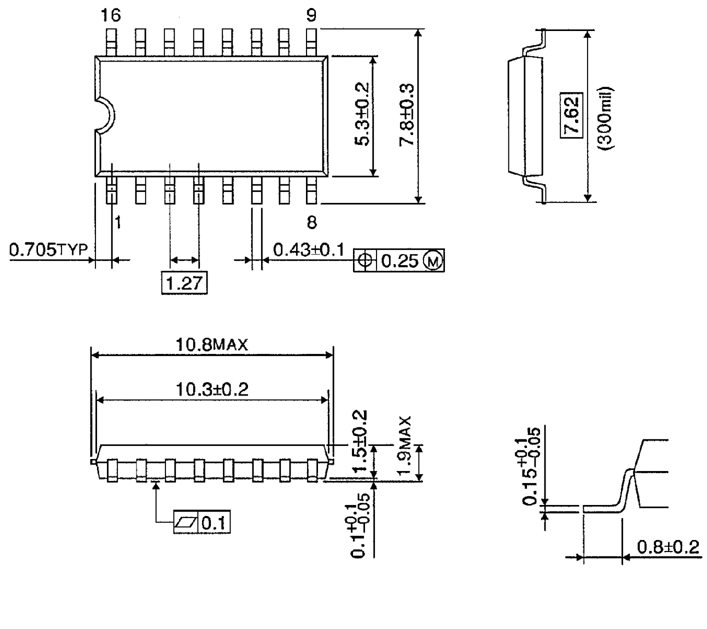
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm

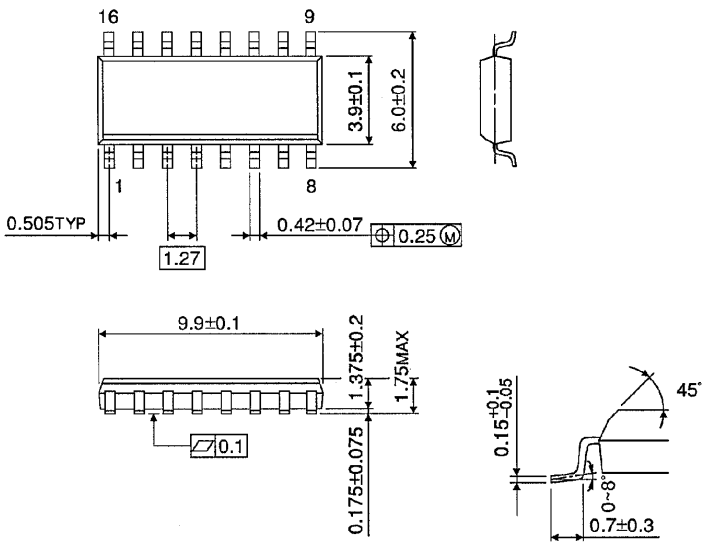


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)