

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MH273FK

Octal D-Type Flip Flop with Clear

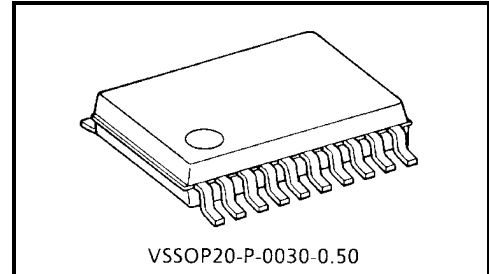
The TC7MH273FK is an advanced high speed CMOS octal D-type flip-flop fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the CLR input is held "L", the Q outputs are at a low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



Weight: 0.03 g (typ.)

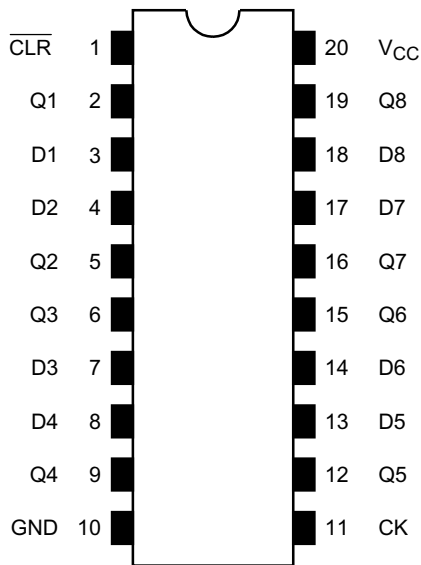
Features

- High speed: $f_{max} = 165 \text{ MHz (typ.) (VCC = 5 V)}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A (max) (Ta = 25^\circ\text{C})}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC (opr)} = 2\sim 5.5 \text{ V}$
- Low noise: $V_{OLP} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74ALS273

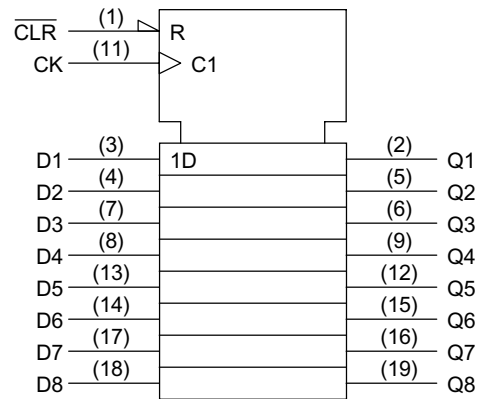
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Pin Assignment (top view)



IEC Logic Symbol

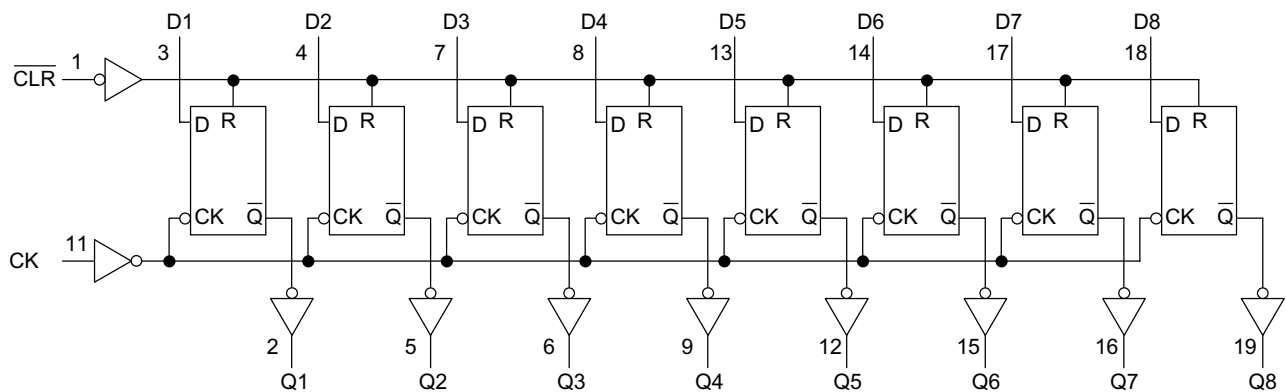


Truth Table

| Inputs | | | Outputs | Function |
|-------------------------|---|----|---------|-----------|
| $\overline{\text{CLR}}$ | D | CK | Q | |
| L | X | X | L | Clear |
| H | L | | L | — |
| H | H | | H | — |
| H | X | | Q_n | No change |

X: Don't care

System Diagram



Maximum Ratings

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|----------------------|------|
| Supply voltage range | V_{CC} | -0.5~7.0 | V |
| DC input voltage | V_{IN} | -0.5~7.0 | V |
| DC output voltage | V_{OUT} | -0.5~ $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | -20 | mA |
| Output diode current | I_{OK} | ±20 | mA |
| DC output current | I_{OUT} | ±25 | mA |
| DC V_{CC} /ground current | I_{CC} | ±75 | mA |
| Power dissipation | P_D | 180 | mW |
| Storage temperature | T_{stg} | -65~150 | °C |

Recommended Operating Conditions

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|---|------|
| Supply voltage | V_{CC} | 2.0~5.5 | V |
| Input voltage | V_{IN} | 0~5.5 | V |
| Output voltage | V_{OUT} | 0~ V_{CC} | V |
| Operating temperature | T_{opr} | -40~85 | °C |
| Input rise and fall time | dt/dv | 0~100 ($V_{CC} = 3.3 \pm 0.3$ V) 0~20 ($V_{CC} = 5 \pm 0.5$ V) | ns/V |

Electrical Characteristics

DC Characteristics

| Characteristics | Symbol | Test Condition | $T_a = 25^\circ\text{C}$ | | | $T_a = -40\sim 85^\circ\text{C}$ | | Unit | | | |
|--------------------------|-----------|--------------------------|----------------------------------|----------------------------|------|----------------------------------|---------------------|---------------------|------|------|---|
| | | | V_{CC} (V) | Min | Typ. | Max | Min | | Max | | |
| Input voltage | "H" level | V_{IH} | 2.0 | 1.50 | — | — | 1.50 | — | V | | |
| | | | 3.0~5.5 | $V_{CC} \times 0.7$ | — | — | $V_{CC} \times 0.7$ | — | | | |
| | "L" level | V_{IL} | 2.0 | — | — | 0.50 | — | 0.50 | V | | |
| | | | 3.0~5.5 | — | — | $V_{CC} \times 0.3$ | — | $V_{CC} \times 0.3$ | | | |
| Output voltage | "H" level | V_{OH} | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu\text{A}$ | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | | | 4.5 | 3.94 | — | — | 3.80 | — | |
| | "L" level | V_{OL} | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 50 \mu\text{A}$ | 2.0 | — | 0 | 0.1 | — | 0.1 | |
| | | | | | 3.0 | — | 0 | 0.1 | — | 0.1 | |
| | | | | | 4.5 | — | 0 | 0.1 | — | 0.1 | |
| | | | | | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | | 4.5 | — | — | 0.36 | — | 0.44 | | |
| Input leakage current | I_{IN} | $V_{IN} = 5.5$ V or GND | 0~5.5 | — | — | ±0.1 | — | ±1.0 | μA | | |
| Quiescent supply current | I_{CC} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | — | 4.0 | — | 40.0 | μA | | |

Timing Requirements (Input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | Ta = -40~85°C | | Unit |
|---|----------------------|----------------|------------------------|--------|---------------|------------|------|
| | | | V _{CC} (V) | Typ. | Limit | Limit | |
| Minimum pulse width (CK) | $t_w(L)$ $t_w(H)$ | — | 3.3 ± 0.3 | — | 5.5 | 6.5 | ns |
| | | | 5.0 ± 0.5 | — | 5.0 | 5.0 | |
| Minimum pulse width ($\overline{\text{CLR}}$) | $t_w(L)$ | — | 3.3 ± 0.3 5.0 ± 0.5 | — — | 5.0 5.0 | 6.0 5.0 | ns |
| Minimum set-up time | t_s | — | 3.3 ± 0.3 5.0 ± 0.5 | — — | 5.5 4.5 | 6.5 4.5 | ns |
| Minimum hold time | t_h | — | 3.3 ± 0.3 5.0 ± 0.5 | — — | 1.0 1.0 | 1.0 1.0 | ns |
| Minimum removal time ($\overline{\text{CLR}}$) | t_{rem} | — | 3.3 ± 0.3 5.0 ± 0.5 | — — | 2.5 2.0 | 2.5 2.0 | ns |

AC Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40~85°C | | Unit | | | |
|---|--------------------------|----------------|---------------------|---------------------|-----|---------------|------|------|------|-----|-----|
| | | | V _{CC} (V) | C _L (pF) | Min | Typ. | Max | | Min | Max | |
| Propagation delay time (CK-Q) | t_{pLH} t_{pHL} | — | 3.3 ± 0.3 | 15 | — | 8.7 | 13.6 | 1.0 | 16.0 | ns | |
| | | | | 50 | — | 11.2 | 17.1 | 1.0 | 19.5 | | |
| | | | 5.0 ± 0.5 | 15 | — | 5.8 | 9.0 | 1.0 | 10.5 | | ns |
| | | | | 50 | — | 7.3 | 11.0 | 1.0 | 12.5 | | |
| Propagation delay time ($\overline{\text{CLR}}$ -Q) | t_{pHL} | — | 3.3 ± 0.3 | 15 | — | 8.9 | 13.6 | 1.0 | 16.0 | ns | |
| | | | | 50 | — | 11.4 | 17.1 | 1.0 | 19.5 | | |
| | | | 5.0 ± 0.5 | 15 | — | 5.2 | 8.5 | 1.0 | 10.0 | | ns |
| | | | | 50 | — | 6.7 | 10.5 | 1.0 | 12.0 | | |
| Maximum clock frequency | f_{max} | — | 3.3 ± 0.3 | 15 | 75 | 120 | — | 65 | — | MHz | |
| | | | | 50 | 50 | 75 | — | 45 | — | | |
| | | | 5.0 ± 0.5 | 15 | 120 | 165 | — | 100 | — | | MHz |
| | | | | 50 | 80 | 110 | — | 70 | — | | |
| Output to output skew | t_{osLH} t_{osHL} | (Note1) | 3.3 ± 0.3 | 50 | — | — | 1.5 | — | 1.5 | ns | |
| | | | 5.0 ± 0.5 | 50 | — | — | 1.0 | — | 1.0 | | |
| Input capacitance | C _{IN} | — | — | — | 4 | 10 | — | 10 | pF | | |
| Power dissipation capacitance | C _{PD} | (Note2) | — | — | 31 | — | — | — | pF | | |

Note1: This parameter is guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

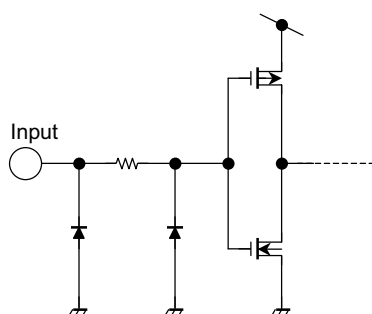
And the total C_{PD} when n pcs of flip-flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 22 + 9 \cdot n$$

Noise Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Unit |
|--|------------------|------------------------|---------------------|------|-------|------|
| | | | V _{CC} (V) | Typ. | Limit | |
| Quiet output maximum dynamic V _{OL} | V _{OLP} | C _L = 50 pF | 5.0 | 0.5 | 0.8 | V |
| Quiet output minimum dynamic V _{OL} | V _{OLV} | C _L = 50 pF | 5.0 | -0.5 | -0.8 | V |
| Minimum high level dynamic input voltage V _{IH} | V _{IHD} | C _L = 50 pF | 5.0 | — | 3.5 | V |
| Maximum low level dynamic input voltage V _{IL} | V _{ILD} | C _L = 50 pF | 5.0 | — | 1.5 | V |

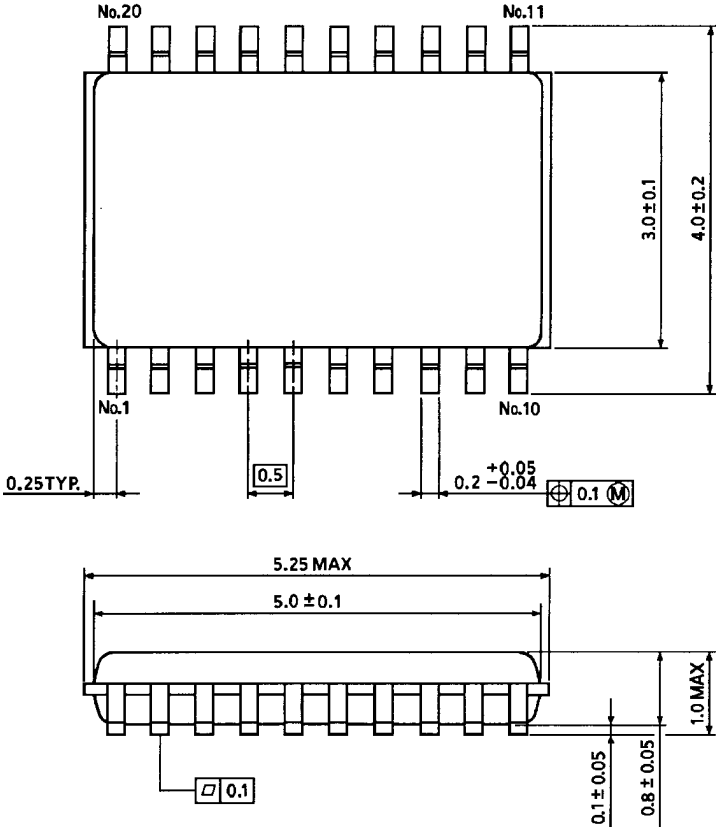
Input Equivalent Circuit



Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)