TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

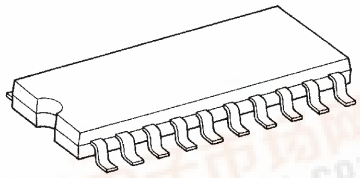
TC74LCX273F, TC74LCX273FW, TC74LCX273FT

LOW VOLTAGE OCTAL D-TYPE FLIP-FLOP WITH 5 V TOLERANT INPUTS AND OUTPUTS

The TC74LCX273 is a high parformance CMOS OCTAL D-TYPE FLIP FLOP. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.
This 8bit D-type flip-flop is controlled by a clock input (CK) and a clear input ($\overline{CLR}$). When the $\overline{CLR}$ input is low, the eight outputs are at a low logic level.
All inputs are equipped with protection circuits against static discharge.

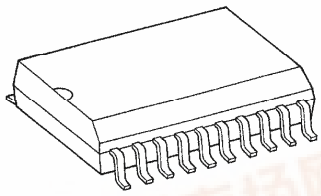
(Note) : The JEDEC SOP (FW) is not available in Japan.

TC74LCX273F



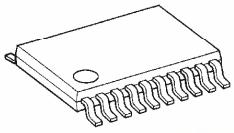
SOP20-P-300-1.27

TC74LCX273FW



SOL20-P-300-1.27

TC74LCX273FT



TSSOP20-P-0044-0.65

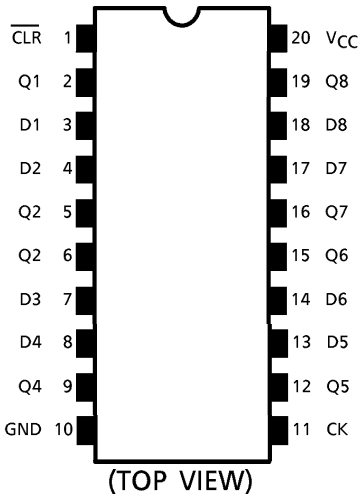
FEATURES

- Low voltage operation : V_{CC} = 2.0~3.6 V
- High speed operation : t_{pd} = 8.5 ns (max) (V_{CC} = 3.0~3.6 V)
- Output current : $|I_{OH}| / I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance : ± 500 mA
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC / VHC / HC / F / ALS / LS etc.) 273 type.

Weight
SOP20-P-300-1.27 : 0.22 g (Typ.)
SOL20-P-300-1.27 : 0.46 g (Typ.)
TSSOP20-P-0044-0.65 : 0.08 g (Typ.)

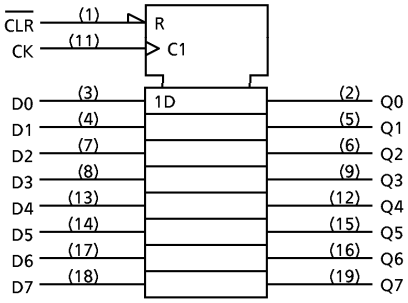
980910EBA1

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

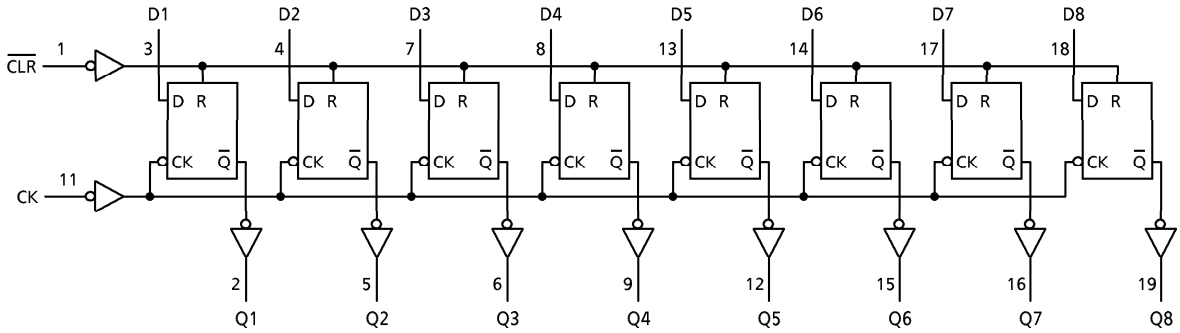


TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Qn	No change

X : Don't Care

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Note 1)	V
		−0.5~V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	180	mW
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) : V_{CC} = 0 V
(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) : V_{OUT} < GND, V_{OUT} > V_{CC}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~10 (Note 9)	ns / V

(Note 4) : Data Retention Only
(Note 5) : V_{CC} = 0 V
(Note 6) : High or Low State
(Note 7) : V_{CC} = 3.0~3.6 V
(Note 8) : V_{CC} = 2.7~3.0 V
(Note 9) : V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = −40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V_{IH}			2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7~3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0~5.5 V		2.7~3.6	—	±5.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN} / V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
			V_{IN} = 3.6~5.5 V		2.7~3.6	—	±10.0	
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7~3.6	—	500	μA

AC characteristics (Ta = −40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	(Fig.1, 2)	2.7	—	—	MHz
			3.3 ± 0.3	150	—	
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}	(Fig.1, 2)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Propagation Delay Time ($\overline{CLR}$-Q)	t_{pHL}	(Fig.1, 3)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Minimum Pulse Width (CK)	t_w (H) t_w (L)	(Fig.1, 2)	2.7	3.3	—	ns
			3.3 ± 0.3	3.3	—	
Minimum Pulse Width ($\overline{CLR}$)	t_w (L)	(Fig.1, 3)	2.7	3.3	—	ns
			3.3 ± 0.3	3.3	—	
Minimum Set-Up Time	t_s	(Fig.1, 2)	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum Hold Time	t_h	(Fig.1, 2)	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Minimum Removal Time	t_{rem}	(Fig.1, 4)	2.7	2.5	—	ns
			3.3 ± 0.3	2.0	—	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10) : Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Ta = 25°C, Input $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V

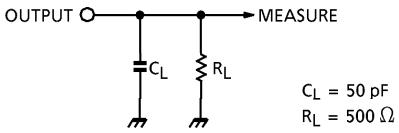
CAPACITIVE CHARACTERISTICS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Input Capacitance	C_{IN}	—	3.3	7	pF
Output Capacitance	C_{OUT}		0	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10 MHz (Note 11)	3.3	25	pF

(Note 11) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

TEST CIRCUIT

Fig.1



AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}, t_w, t_s, t_h

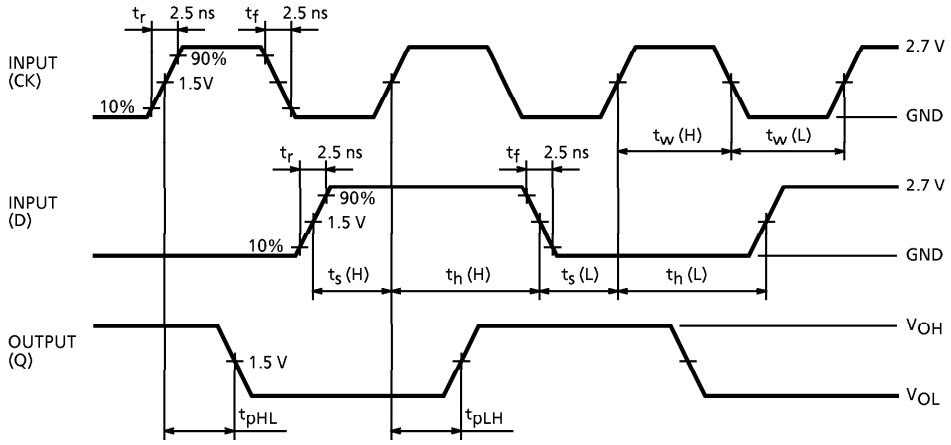


Fig.3 t_{pLH}, t_{pHL}

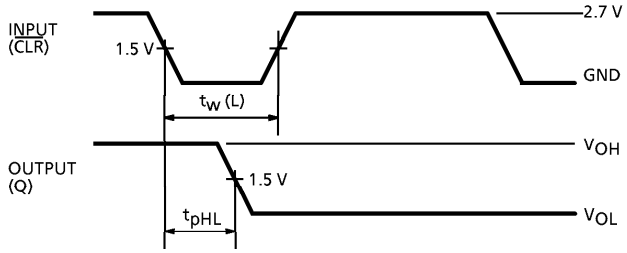
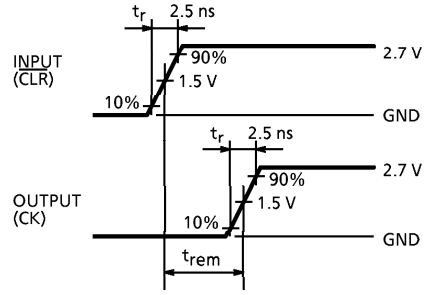
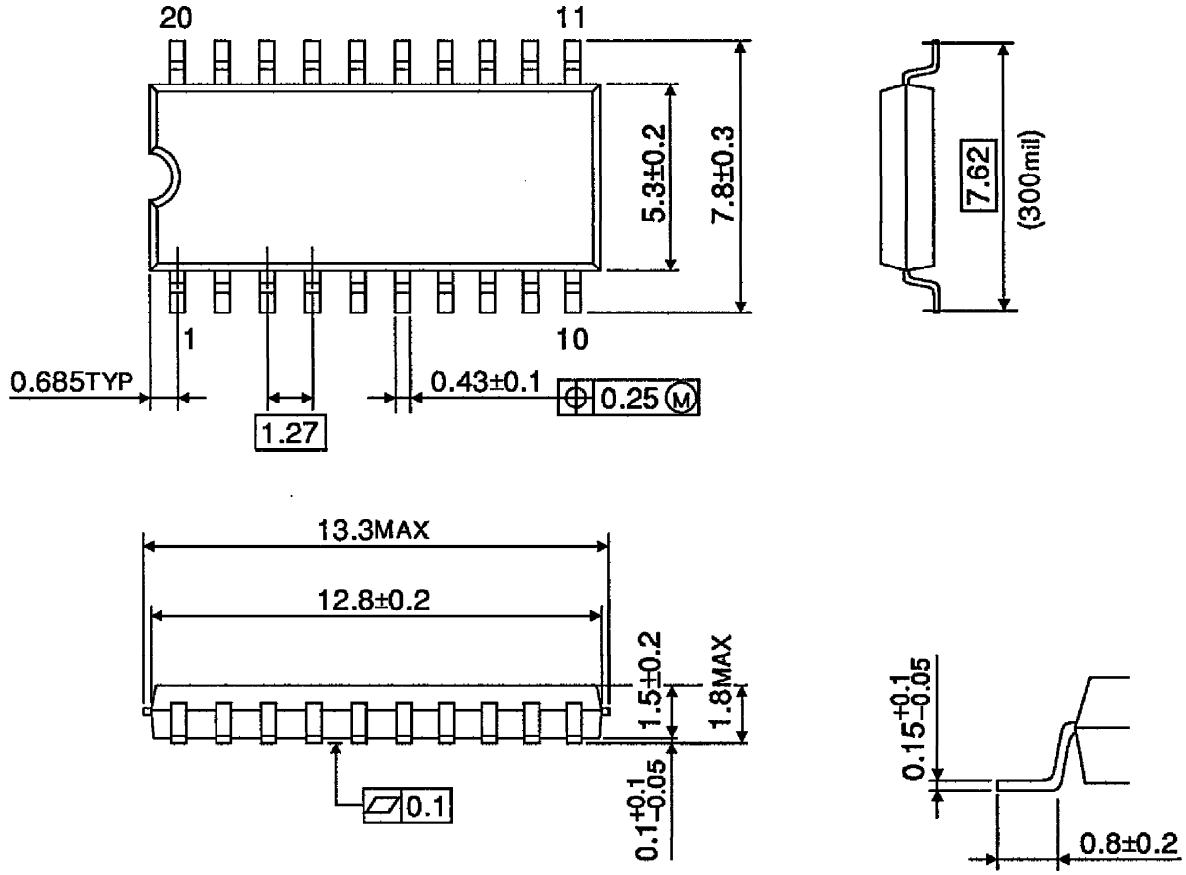


Fig.4 t_{rem}



PACKAGE DIMENSIONS

SOP20-P-300-1.27 Unit : mm



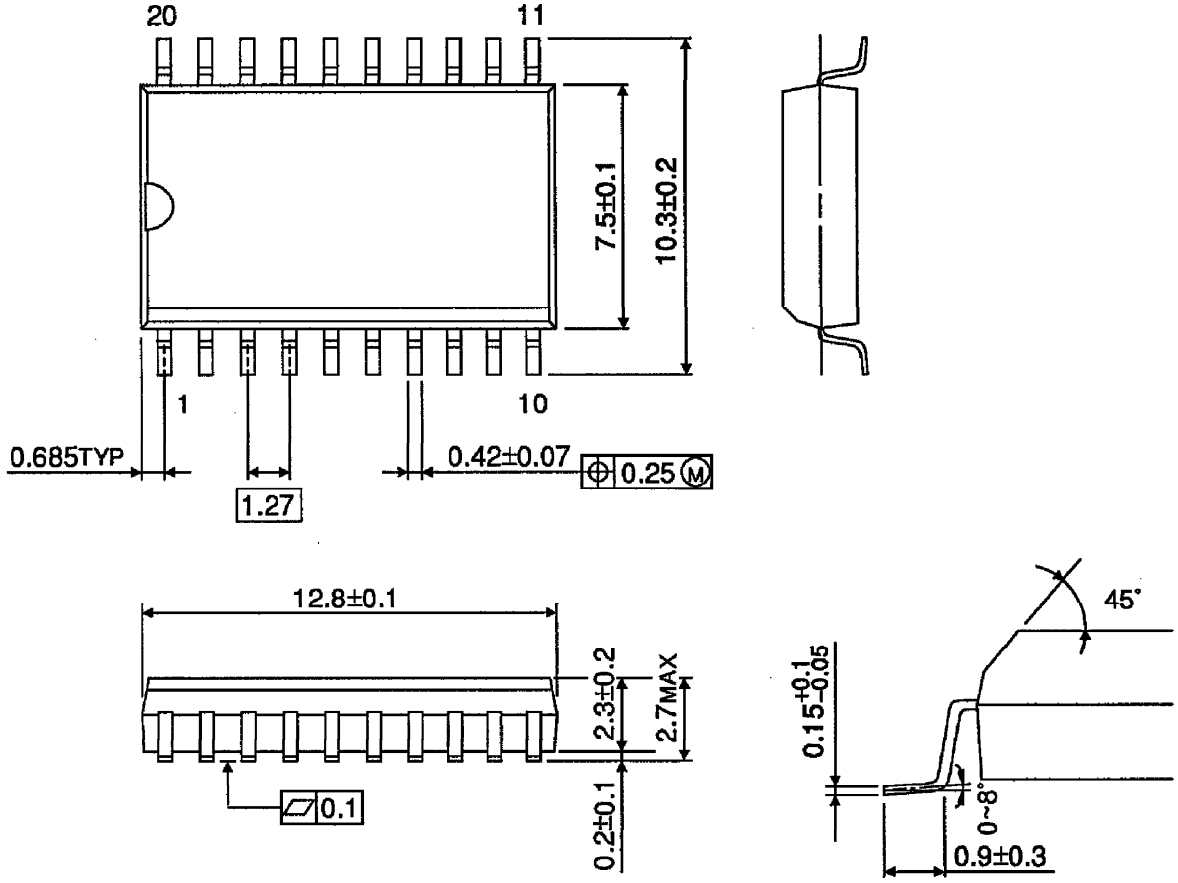
Weight : 0.22 g (Typ.)

PACKAGE DIMENSIONS

SOL20-P-300-1.27

Unit : mm

(Note) This package is not available in Japan.

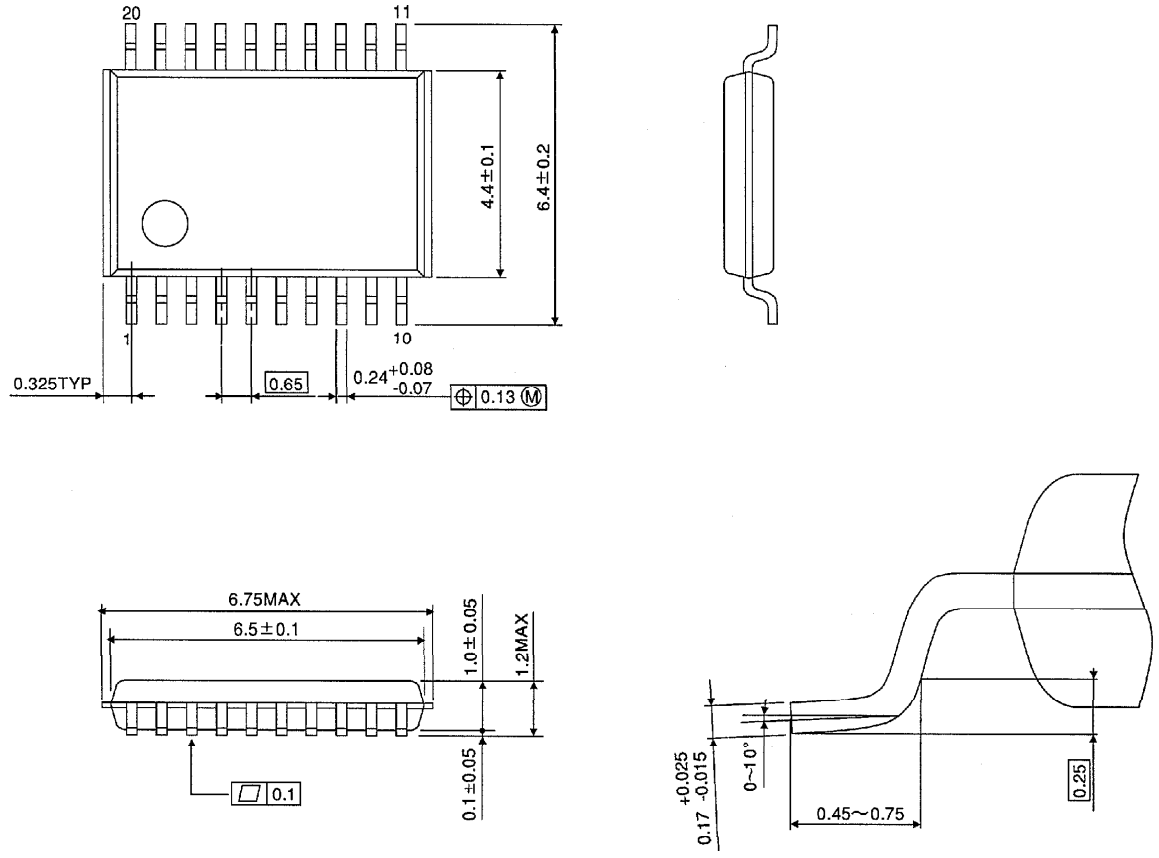


Weight : 0.46 g (Typ.)

PACKAGE DIMENSIONS

TSSOP20-P-0044-0.65

Unit : mm



Weight : 0.08 g (Typ.)