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Measurement on the C166 Family

I/O - „Scope Probes Connected to an Output Pin“

Andreas Hettmann / Siemens Cupertino

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I/O - “Scope Probes Connected to an Output Pin”

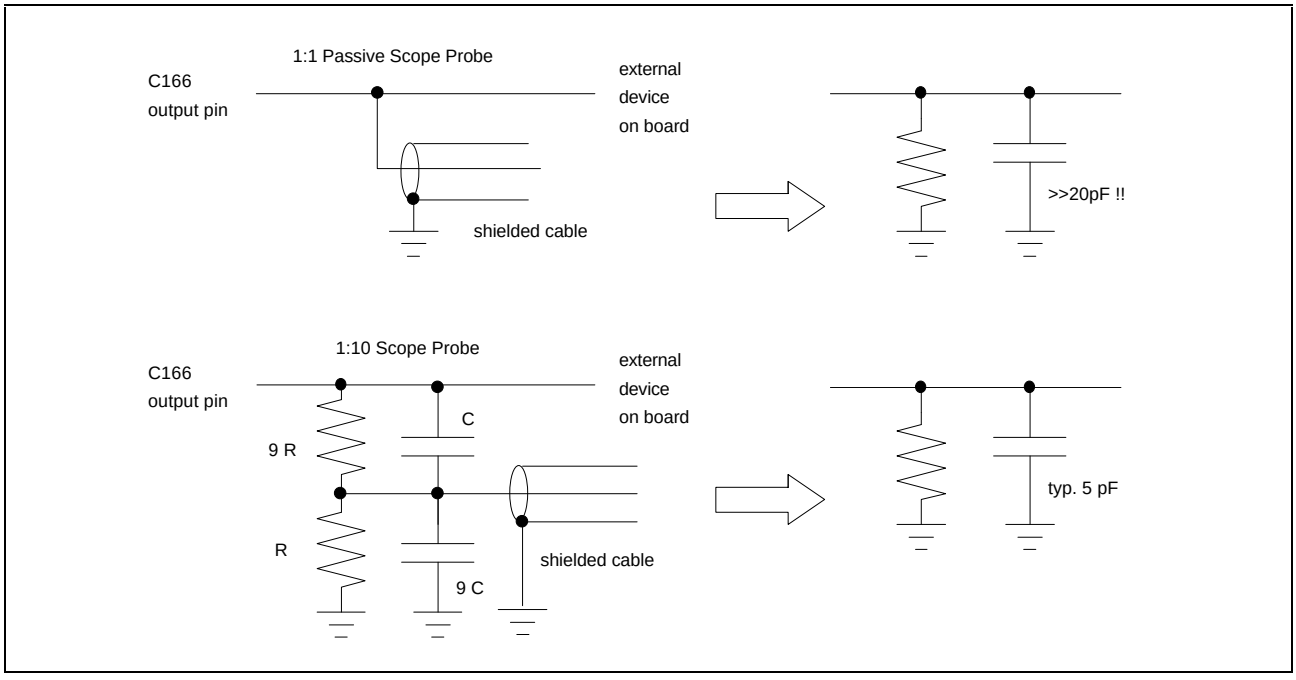
Siemens’ C166-Family is manufactured in advanced CMOS technology to achieve high performance at low power consumption. There are no open drain outputs at standard data and address busses and control signals like RD# or WR#. Output drivers have been designed for full TTL compatibility (output LOW voltage max. 0.4V @ 2.4mA / 1.6mA and HIGH voltage min. 2.4V @ -2.4mA / -1.6mA; refer to User’s Manual for respective specification).

Problems may occur if under test conditions long wires or not suitable scope probes are connected to an output pin. These devices will bring several capacitances and inductances into the system which results in static and/or dynamic overload and flatten signal edges. Signals will appear delayed at their destination e.g. WR# pin of on-board memory causing serious timing problems or system failures.

Additional delay times can be easily calculated by

$$t_{add} = C_{add} \frac{V_{HIGH} - V_{LOW}}{I_{out}}$$

Assuming a 2.4mA output driver (I_{out}) and a LOW to HIGH voltage difference of 2V (V_{HIGH} - V_{LOW}) a cable or probe capacitance of 20pF will show an additional signal delay time of approximately 17nsec which will be too much in almost all cases.



Different scope probes connected to signal lines influences the dynamic load of line drivers.