GCDR3300A

The GCDR3300A is a macro to be used within the SH100G Gate Array-environment. This macro is designed for 2.5 - 3.3 GHz applications. It contains a 1:2 demultiplexer and a phase detector (PD) [1] with bit error detection and VCO (fig. 1).
The block named 'UP' and 'DOWN' represents a mixer circuit for the UP and DOWN signals of the PD and the FD. The VCO has its own GND (I9) and negative supply N2V5 (I10), and is controlled by pin I7 (VF0). With a frequency window detector (FD), an operational amplifier and a voltage reference diode, a complete PLL can be built. The external configuration is shown in figure 3.

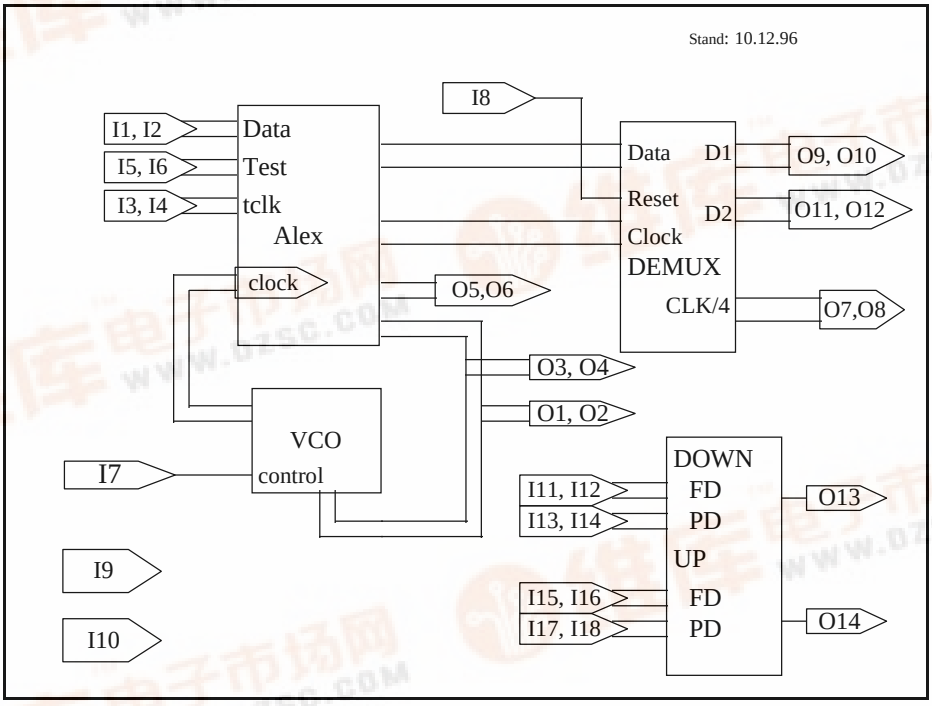


fig. 1: Block diagram GCDR3300A

Table 1 shows the signal class and the function of the input and the output pins. The correct pin pad combination is given in table2.

Table 1: Pin list

Pinname	Signal class	Notes
I1,I2 data	Analog	Differential data, 10 mV- 500 mV_{pp}. 50 Ohm on chip resistors
I3,I4 tclk	CML2	Differential clock used for testing.
I5,I6 test	ECL2	Select test mode. High = Test mode on
I7 control	Analog	Input integral path from PD, FD
I8	CML	Reset toggle ff's demux
I9, I19	Analog	GND for internal VCO
I10	Analog	N2V5 for internal VCO nom. -2.5V
I11, I12	CML2	Down signal frequency detector
I13, I14	CML2	Down signal phase detector
I15, I16	CML2	Up signal frequency detector
I17, I18	CML2	Up signal phase detector
O1,O2 down	CML2	Down signal phase detector
O3,O4 up	CML2	Up signal phase detector
O5,O6 ber	CML2	Bit error detection
O7,O8 c/4	ECL2	Clock/4
O9,O10 d1	CML2	Data 1
O11,O12 d2	CML2	Data 2
O13 DON	Analog	DON signal phase detector + 1/10 frequency detector
O14 UPN	Analog	UPN signal phase detector + 1/10 frequency detector

Table 2: Pad macros

Pin name	Pad macro
I1, I2	PA50I
I7	PIWIRE2A
I9	PASUP1
I10	PASUP1
O13	PAWIRE
O14	PAWIRE

Description Block Diagram

In figure 1, the internal structure of the macro is shown. The block ALEX represents the combined phase detector and decision circuit [1]. In this block, the data signal is recovered and the UP and DOWN signals are generated. Also a Bit error detection signal (BER) is available. This BER signal can be used to build a 'Loss Of Signal' detection (LOS). The VCO is a ring oscillator structure with a K_{VCO} of about 2 GHz/V (fig. 3). The 1:2 demultiplexer circuit gets the data and clock signal from the ALEX.

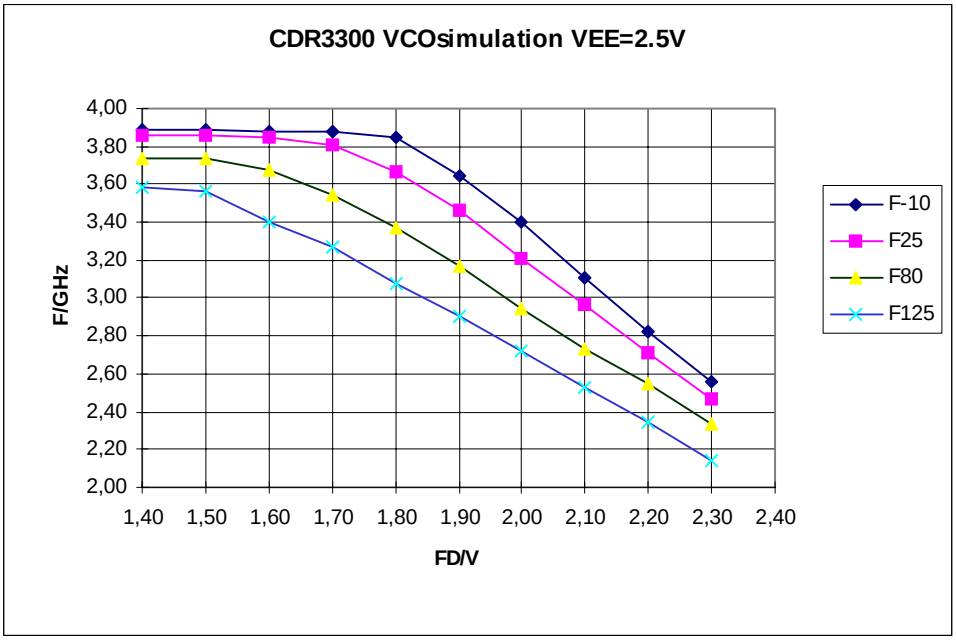


fig. 2: VCO frequency as function of the voltage at I7.

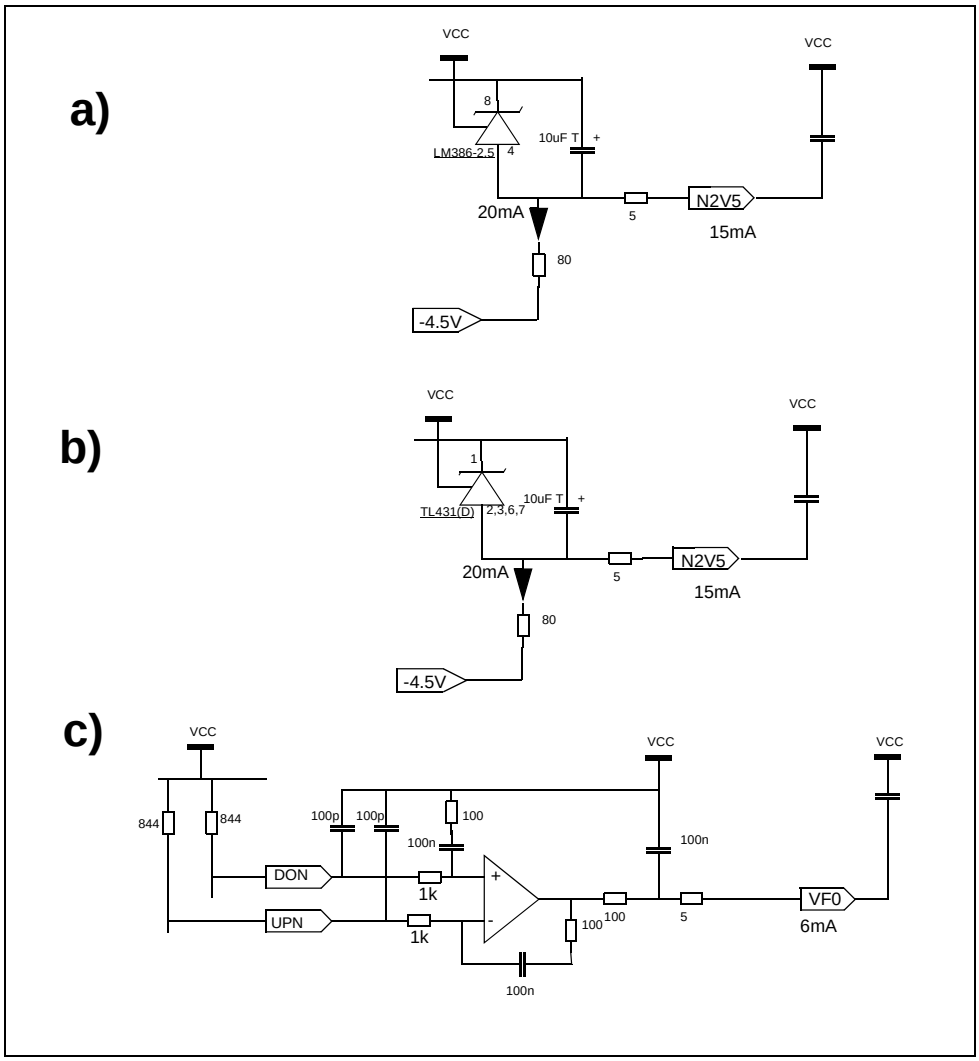


fig. 3: External Parts of the PLL circuit

a) negative VCO Supply from external reference (LM385-2.5).

b) negative VCO Supply from external reference(TL431(SO8)).

c) Integrator (part of Loop filter) e.g. TS3V912.

Remark:

The values given in this application note result in a supply range from 4 to 5.5V and a lower frequency limit of 2.4GHz.

OPAMP requirements

$I_{(-1V)}$: 0 mA
$I_{(-2.8V)}$: 4.8 mA
U_{os}: < 5 mV

Pinout

Table 3 shows the pad numbers for the G1 and G2 master with the two possible placements of the macro. Table 4 shows the placement of the connections from the core side.

Table 3: Pad list of pad numbers

Pin	G1 Top	G1 Bottom	G2 Top	G2 Bottom
I1	PP317	PP124	PP309	PP118
I2	PP318	PP123	PP311	PP116
I7	PP321	PP119	PP315	PP112
I9	PP316	PP125	PP310	PP117
I10	PP315	PP126	PP306	PP121
I19	PP319	PP122	PP312	PP115
O13	PP321	PP117	PP317	PP110
O14	PP320	PP118	PP316	PP111

Table 4: Core ports

Pin	G1 Top	G1 Bottom	G2 Top	G2 Bottom
I3, I4	C1625	C0152	C1007	C0137
I5, I6	C1627	C0150	C1009	C0135
I8	C1643	C0132	C1028	C0116
I11, I12	C1651	C0126	C1038	C0107
I13, I14	C1642	C0134	C1027	C0117
I15, I16	C1649	C0128	C1036	C0109
I17, I18	C1641	C0135	C1026	C0118
O1, O2	C1628	C0149	C1010	C0134
O3, O4	C1629	C0148	C1011	C0133
O5,O6	C1626	C0151	C1008	C0136
O7, O8	C1647	C0130	C1033	C0111
O9, O10	C1650	C0127	C1037	C0108
O11, O12	C1648	C0129	C1034	C0110

Test Description

A static test can be done by switching into the test mode (I5 = High, I6 = Low). Then the macro can be tested with an external clock (pin I3, I4) and data (pin I1, I2). At the beginning of a test sequence a reset (pin8) is done. The internal VCO can be stopped by leaving the pins N2V5 and VF0 open.

Hints for Simulation

In the simulation model, the VCO is inoperable. For simulations, the testmode is switched on. When the test mode is off, all outputs of the macro show the X-state. To simulate the demultiplexer part of the macro, a reset (pin8) has to be done.

Data recovery Circuit in the SH100G Environment

To build a complete PLL with LOS and demultiplexer, some additional circuits in the periphery and in the core area are needed.

PLL

The PLL consists of a phase detector(PD), a frequency detector (FD), and a loopfilter. The PD is realized in the macro GCDR3300A.The outputs O1-O4 of this macro are the UP and DOWN signals of the PD. These UP and DOWN signals are mixed with the UP and DOWN signals of the FD. This can be done with the inputs I11-I18 of the GCDR3300A. The signals of the PD are weighted 9 times stronger than the signals of the FD. So it is important to use the right input for each signal (see figure 1 and table 1)! Pin O13 and O14 of the GCDR3300A are fed to the loop filter. The external circuits can be implemented as shown in figure 3. The FD compares the divided VCO signal with a reference clock. The value of a counter, after a certain time, gives the information wether the VCO is too fast or too slow. When the FD gives the value ’too slow’ or ’too fast’ the PD signals have to be turned off at pin I13, I14 and I17, I18. This can be done by a multiplexer
(fig. 4).

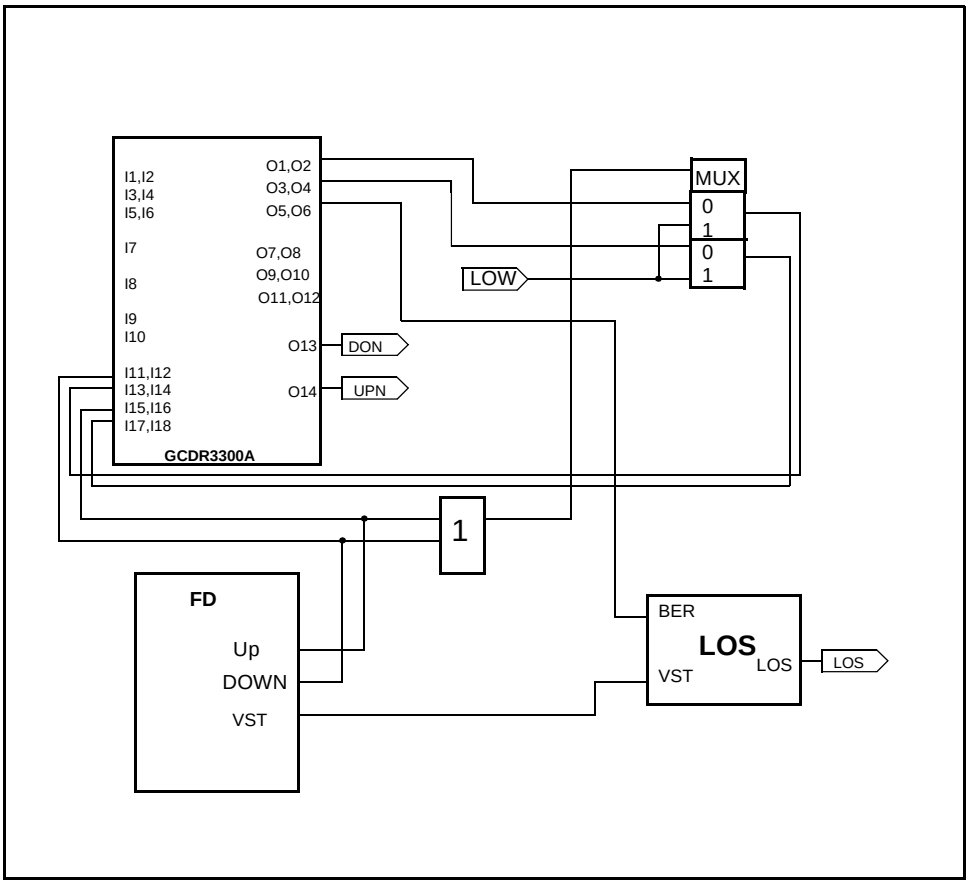


fig. 4: Internal PLL circuit

Frequency Detector

For the frequency window detector (FWD) a reference clock (REF) is needed. This reference clock is divided by n, and this divided clock is the main parameter for designing the other parts of the FWD. A certain frequency window (FW) is given when the FWD is turned off.
The counter is clocked by the VCO signal divided by x. After a certain time, given by REF, the value of the counter is compared with a reference value window. This comparison gives an UP or DOWN or OK (UP=DOWN= LOW) signal that is passed on a pulse former and then to the loop filter. For the design of the PLL, there are two constrains that have to be considered: the size of the loop filter and the size of the counter. A large counter range will determine the accuracy of the frequency but the FD will give less information in a certain time. Therefore a large loop filter is needed.This invokes a long transient time for the PLL.

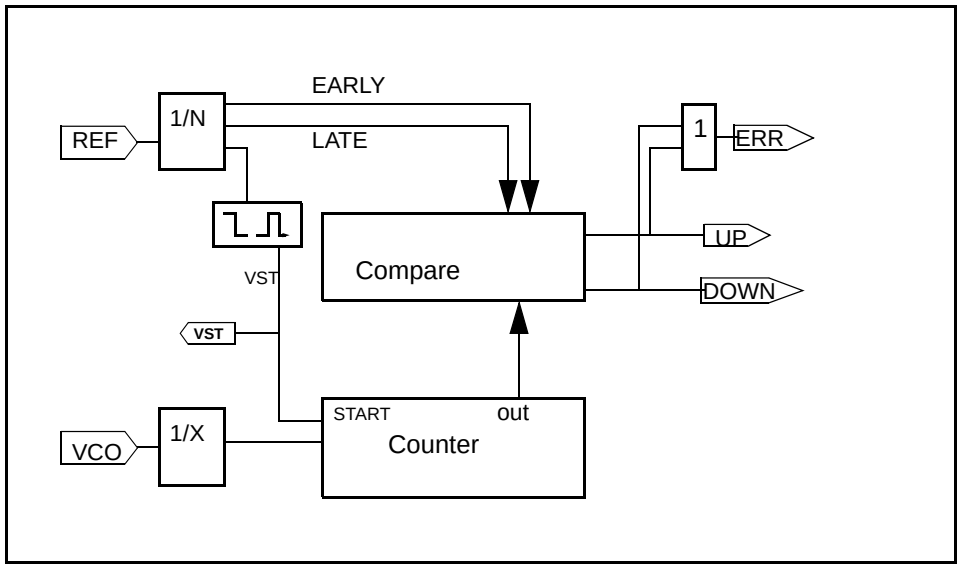


fig. 5: Frequency window detector block diagram

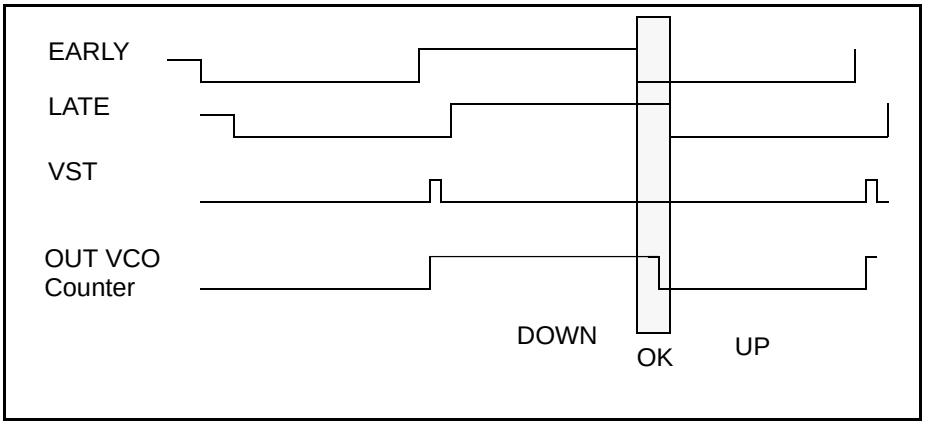


fig. 6: Waveform frequency detector

LOS

A LOS can be generated with the help of the BER signal, pin O5 O6 of the GCDR3300A. This can be done with a counter that is reset after a certain time generated by the reference clock. When this counter reaches a specified value a LOS will be set immediately. The LOS will be reset when the value of the counter drops below another specified value that is below the first value.
This time is specified by VST and SHIFT (fig. 8).

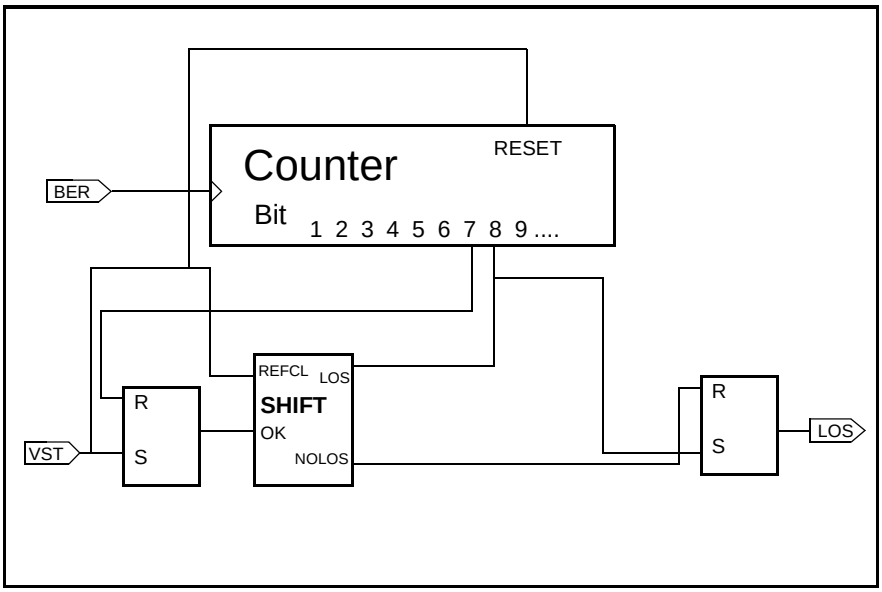


fig. 7: LOS detection

Example:

The LOS has to be HIGH when the pulse rate of BER is higher then 10E-3.
f $VST = (Fbit)/2^{16}$
$(2)^{16} = 65536\text{Bit}.\quad 10\text{E-}3 = 65\text{Bit}$
LOS is LOW if less then 128 BER pulses are generated in a certain time.

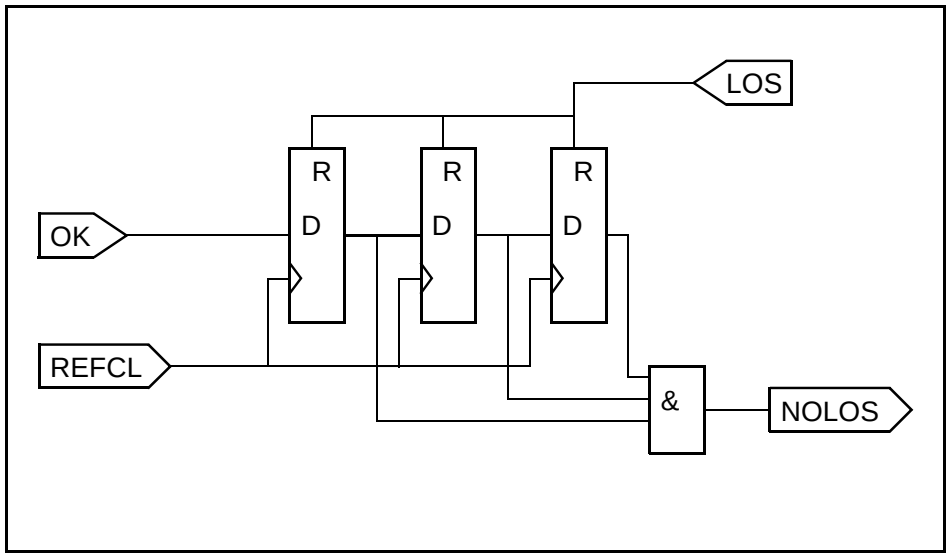
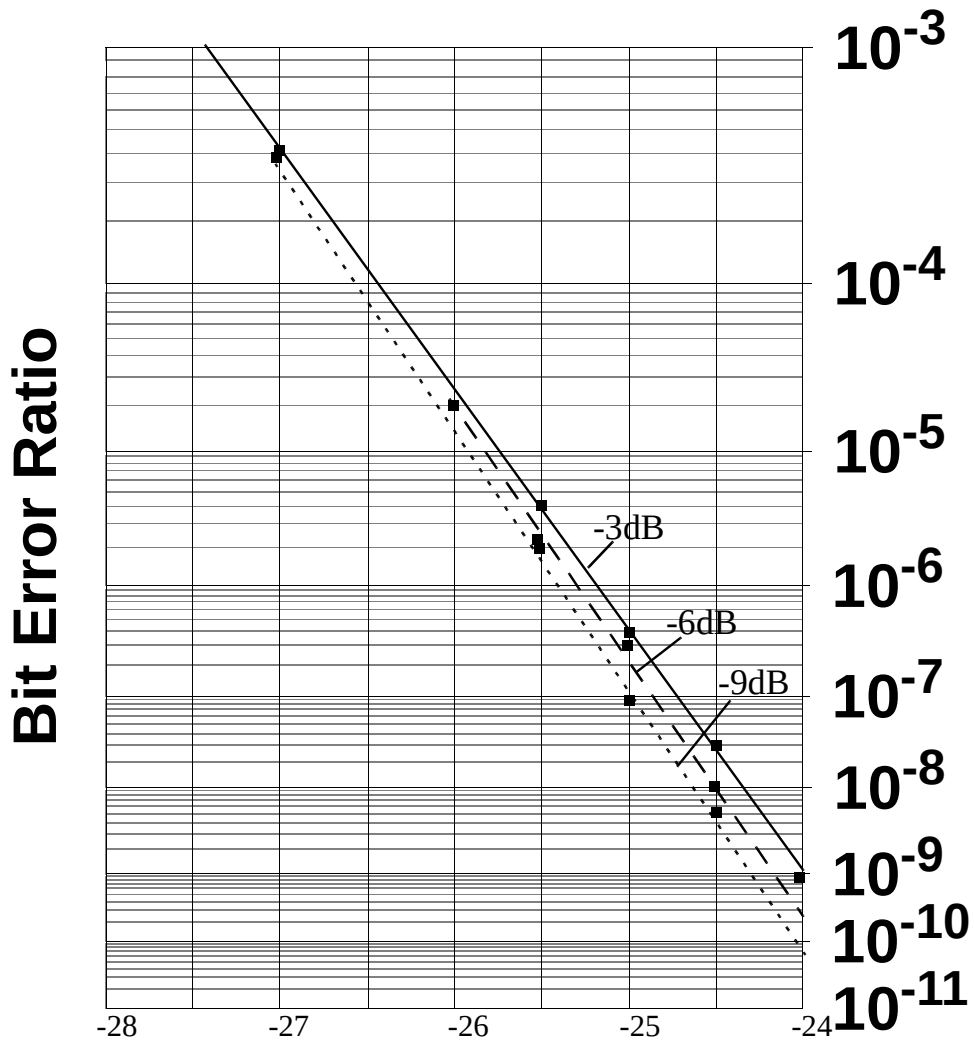
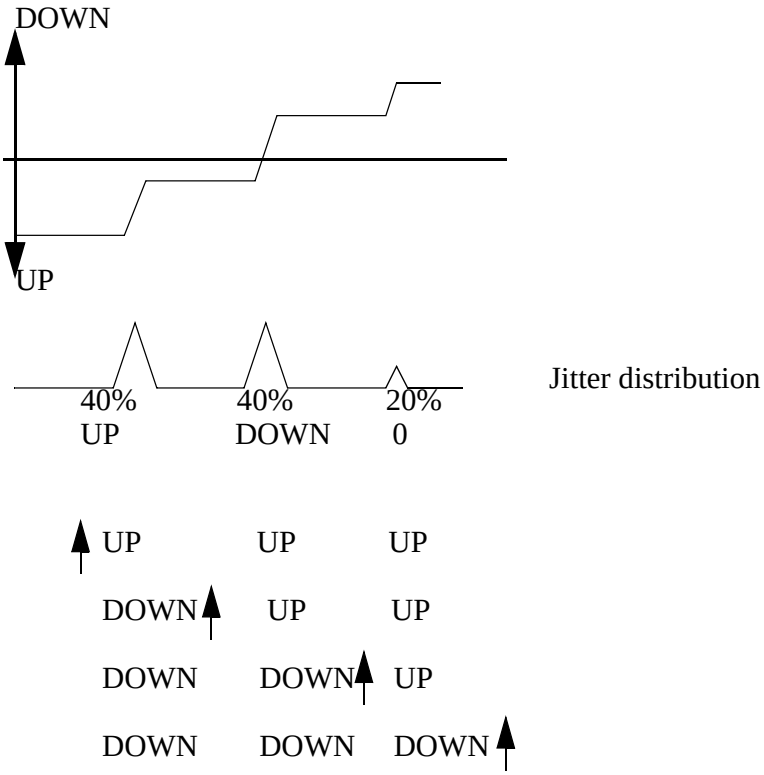


fig. 8: SHIFT

The Flip-flops in SHIFT are positive edge triggered


Bit Error Ratio
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
-3dB
-6dB
-9dB
-28
-27
-26
-25
-24
Optical Power /dBm



References

[1] J. J. D. H. Alexander: "Clock Recovery from Random Binary Signals", Electronics Letters 11, pp. 541-542, Oct. 1975.