

# SIEMENS

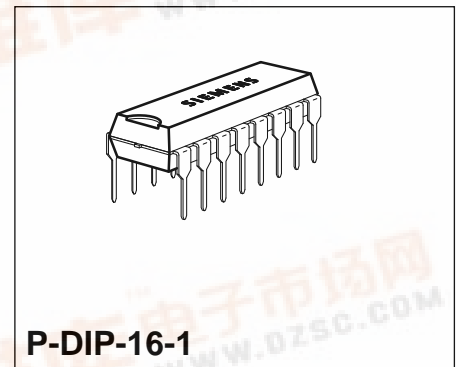
## 256 x 8-Bit Static CMOS RAM NMOS-Compatible

SAE 81C52

### Preliminary Data CMOS IC

#### Features

- 256 x 8-bit organization
- Standby mode
- Compatible with the NMOS and CMOS versions of the microprocessor/microcontroller families SAB 8086, SAB 8051
- Very low power dissipation
- Data retention up to  $V_{DD} \geq 1\text{ V}$
- Three different chip select inputs for two chip select modes
- No increasing power consumption in standby mode if the control inputs are on undefined potential
- Temperature range – 40 to 110 °C



Type	Ordering Code	Package
SAE 81C52 P	Q67100-H9017	P-DIP-16-1
SAE 81C52 G	Q67100-H9015	P-DSO-20-1 (SMD)

The SAE 81C52 is a CMOS-silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus interfaces directly to 8-bit microprocessors/microcontrollers without any timing or level problems, e.g. the families SAB 8086, SAB 8051.

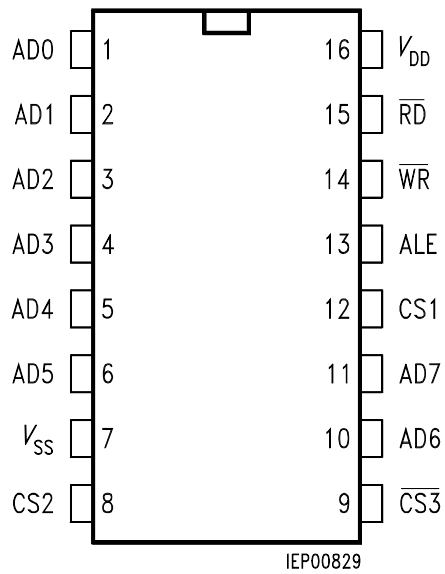
All inputs and outputs are fully compatible with NMOS circuits, except CS1. Data retention is ensured up to  $V_{DD} \geq 1.0\text{ V}$ . The SAE 81C52 has three different inputs for two chip select modes which allow to inhibit either the address/data lines ( $\overline{AD} 0 \dots \overline{AD} 7$ ) and the control lines ( $\overline{WR}$ ,  $\overline{RD}$ , ALE, CS2, CS3), or only the control lines  $\overline{RD}$ ,  $\overline{WR}$ .

The power consumption is max. 5.5  $\mu\text{W}$  in standby mode and max. 16.5 mW in operation. In standby mode, the power consumption will not increase if the control inputs are on undefined potential.

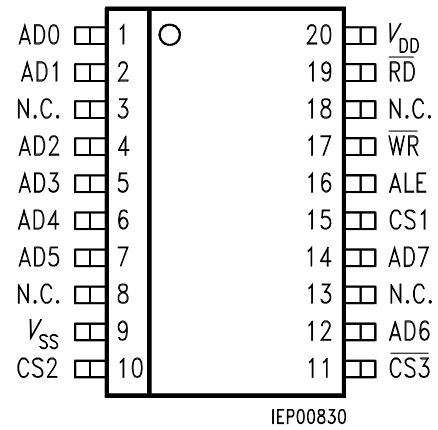


## Pin Configurations (top view)

### SAE 81C52 P

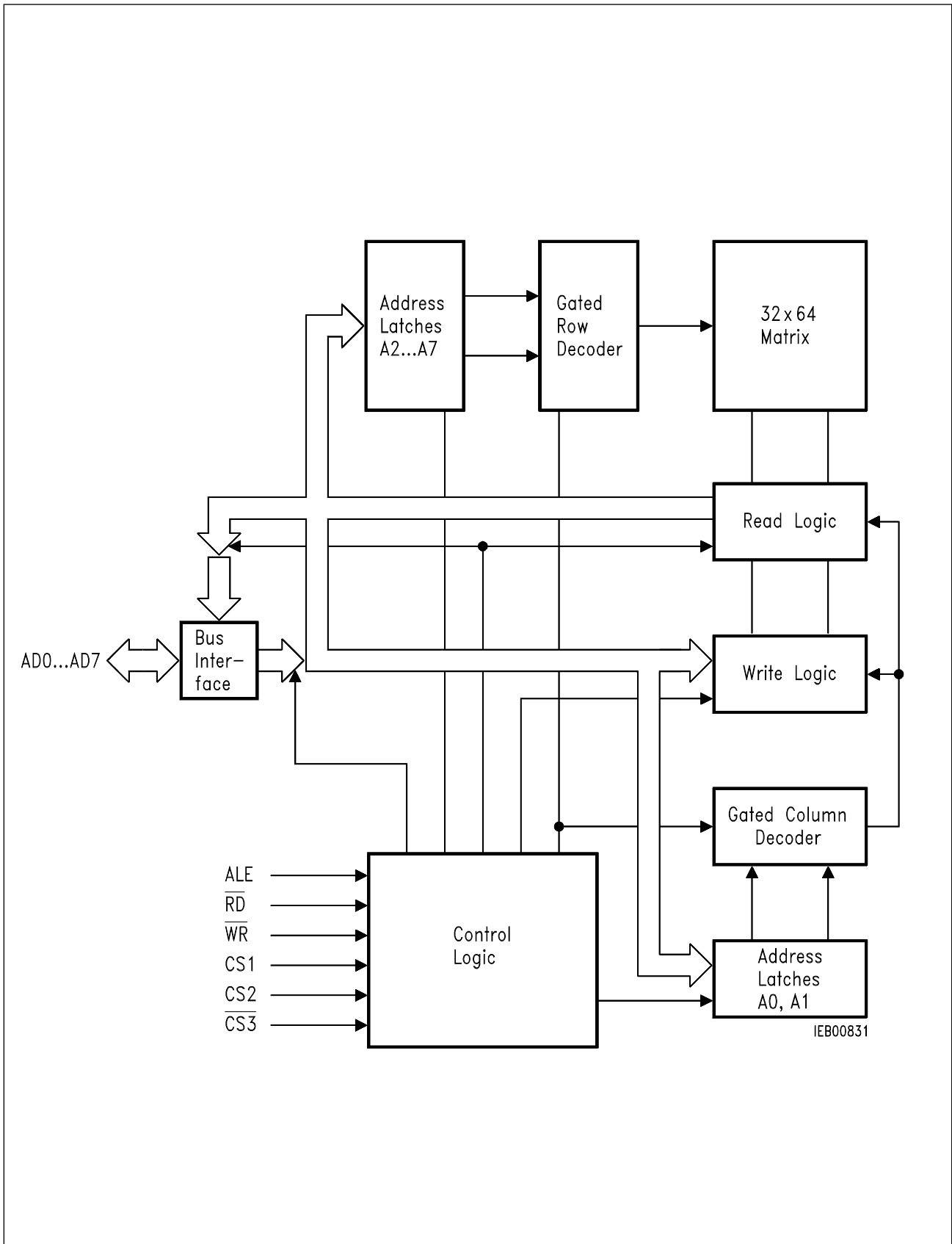


### SAE 81C52 G

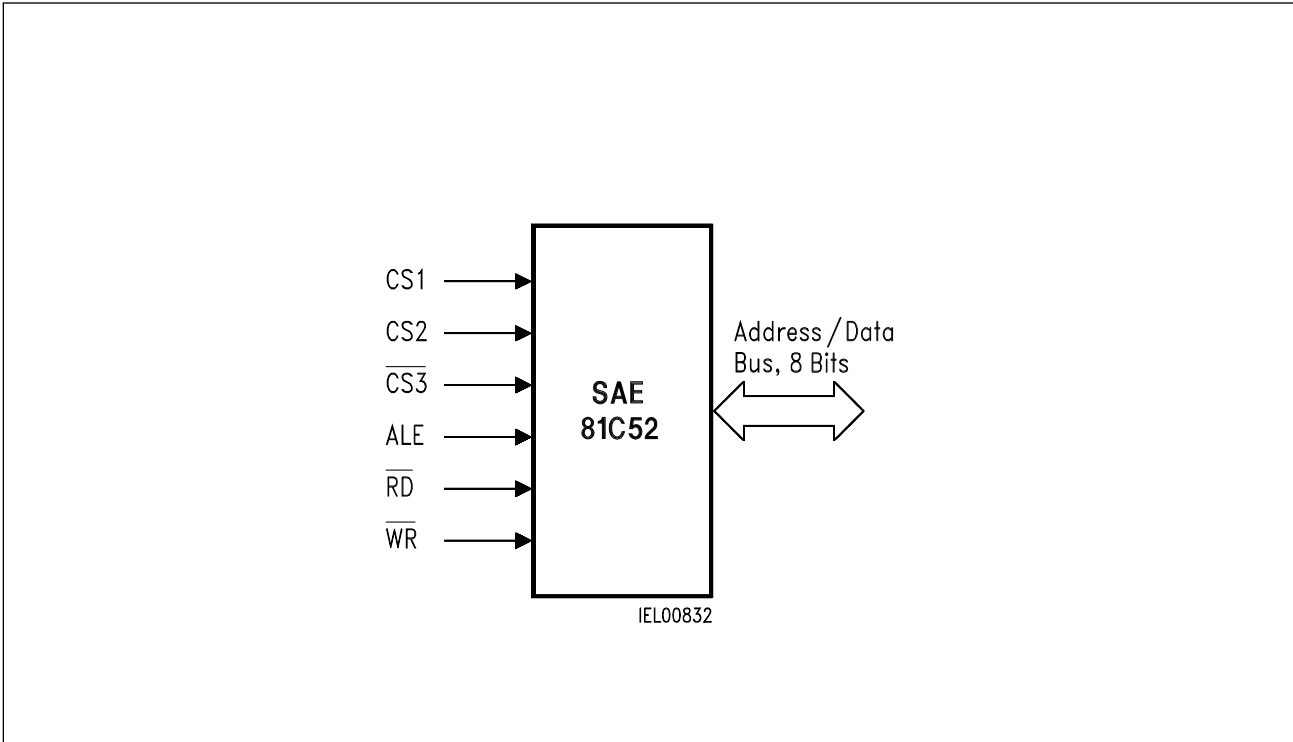


## Pin Definitions and Functions

SAE 81C52 G	SAE 81C52 P	Symbol	Function
Pin No.	Pin No.		
1, 2, 4, 5, 6 7, 12, 14	1 ... 6 10, 11	AD0 ... 7	Address/data lines
15	12	CS1	Chip select 1 (standby) active low; inhibits all lines including control lines
16	13	ALE	Address latch enable
17 19	14 15	$\overline{WR}$ $\overline{RD}$	Write enable Read enable
20	16	$V_{DD}$	Power supply
9	7	$V_{SS}$	GND (0 V)
10 11	8 9	CS2 $\overline{CS3}$	Chip select 2; inhibits control inputs $\overline{RD}$ , $\overline{WR}$ Counterpart to CS2



Block Diagram



### Logic Symbol

### Truth Table

CS1	CS2	$\overline{\text{CS3}}$	ALE	$\overline{\text{RD}}$	$\overline{\text{WR}}$	AD0 ... AD7	Function
L	*	*	*	*	*	Floating (tristate)	Standby
H	X	X	H	H	H	Addresses to memory	Store addresses
H	H	L	L	L	H	Data from memory	Read
H	H	L	L	H	L	Data to memory	Write
H	L	X	L	X	X	Floating (tristate)	None
H	X	H	L	X	X	Floating (tristate)	None

\*: Level =  $V_{SS} \dots V_{DD}$   
 X: Level = low or high

## Absolute Maximum Ratings

$T_A = -40$  to  $110$  °C

Parameter	Symbol	Limit Values	Unit
Supply voltage referred to GND ( $V_{SS}$ ) All input and output voltages	$V_{DD}$ $V_{IM}$	0 to 6 $V_{SS} - 0.3$ $V_{DD} + 0.3$	V V V
Total power dissipation Power dissipation for each output	$P_{tot}$ $P_Q$	250 50	mW mW
Junction temperature Storage temperature	$T_j$ $T_{stg}$	125 - 55 to 125	°C °C
Thermal resistance system - air P-DIP-16-1 P-DSO-20-1	$R_{th SA}$ $R_{th SA}$	70 95	K/W K/W

## Operating Range

Supply voltage	$V_{DD}$	4.5 to 5.5	V
Ambient temperature	$T_A$	- 40 to 110	°C

### DC Characteristics

$T_A = -40$  to  $110$  °C;  $V_{DD} = 4.25$  V to  $5.5$  V;  $V_{SS} = 0$  V

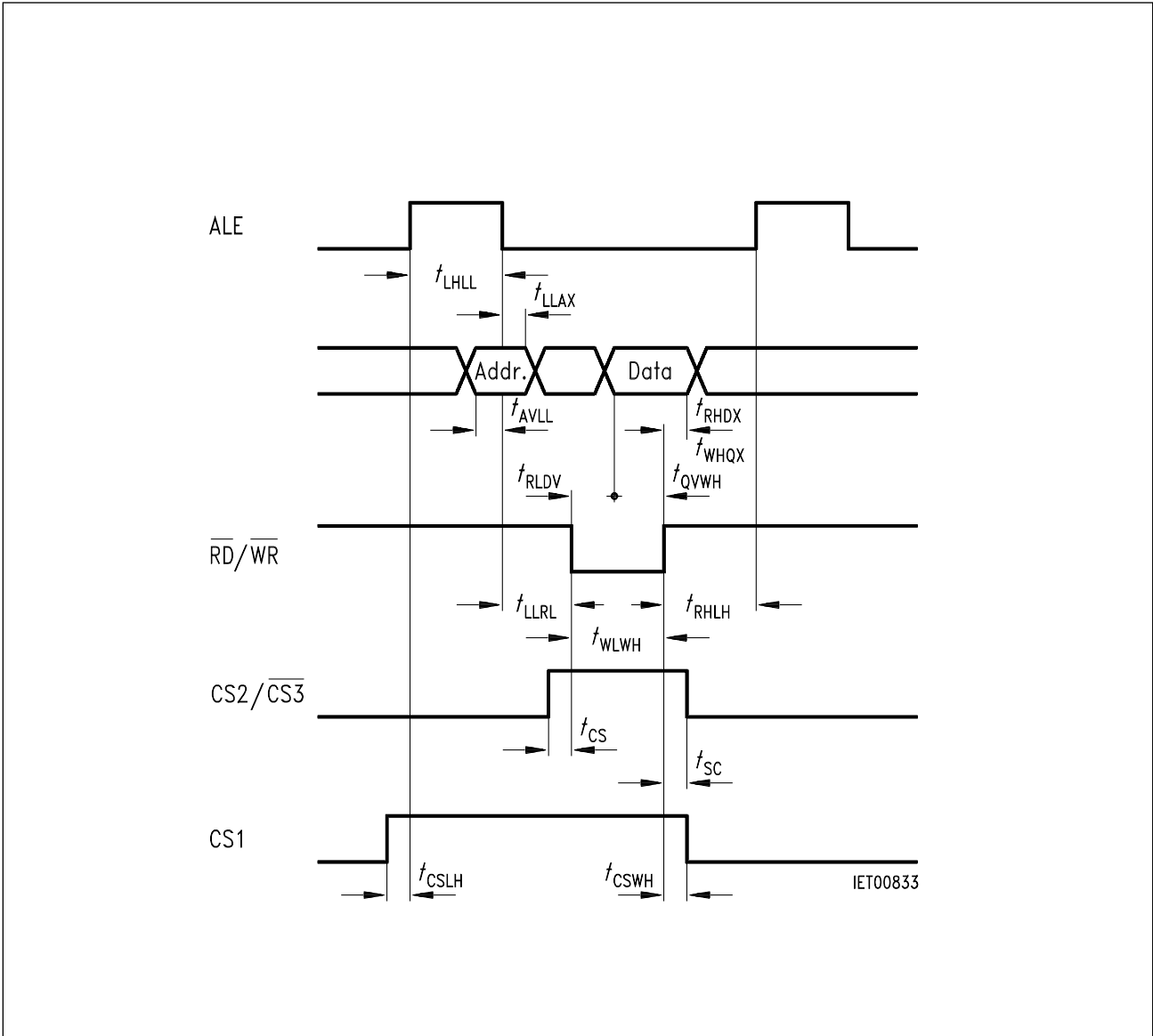
Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby supply current	$I_{DD}$		1	$\mu$ A	$V_{DD} = 5.5$ V; $T_A = 25$ °C; $V_{CS1} = 0$ V $\Delta t_{cyc} = 1$ $\mu$ s; $V_{DD} = 5.5$ V; $C_L = 100$ pF
Supply current	$I_{DD}$		3	mA	
Standby voltage for data retention	$V_{DD}$	1.0		V	
L-input current (for each input)	$I_{IL}$		1	$\mu$ A	$V_I = 0$ to $V_{DD}$
Output leakage current	$I_{QLK}$		1	$\mu$ A	$V_Q = 0$ to $V_{DD}$ tristate
L-input voltage	$V_{IL}$	$V_{SS}$	0.8	V	
H-input voltage	$V_{IH}$	2.2	$V_{DD}$	V	
L-output voltage	$V_{QL}$		0.4	V	$I_{QL} = 1$ mA
H-output voltage	$V_{QH}$	2.6		V	$I_{QL} = 1$ mA
L-input voltage CS1	$V_{IL}$	$V_{SS}$	1	V	
H-input voltage CS1	$V_{IH}$	$V_{DD} - 1$	$V_{DD}$	V	

## AC Characteristics

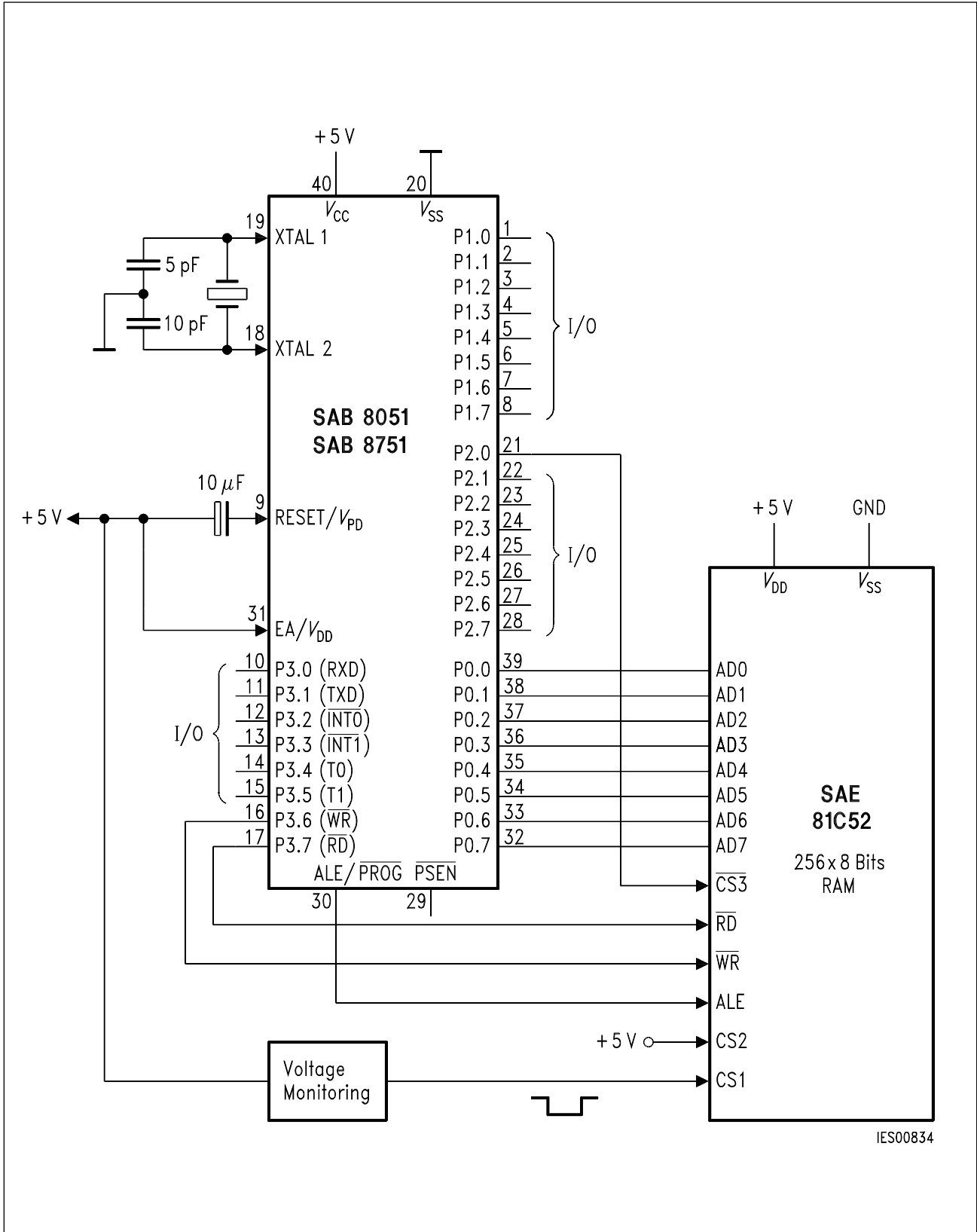
$T_A = -40$  to  $110$  °C;  $V_{DD} = 4.5$  to  $5.5$  V;  $V_{SS} = 0$  V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	$t_{LHLL}$	100		ns
ALE low before $\overline{RD}$ low	$t_{LLRL}$	50		ns
$\overline{RD}$ high before ALE high	$t_{RHLH}$	18		ns
ALE low before $\overline{WR}$ low	$t_{LLWL}$	50		ns
$\overline{WR}$ high before ALE high	$t_{WHLH}$	18		ns
Address setup before ALE	$t_{AVLL}$	18		ns
Address hold after ALE	$t_{LLAX}$	30		ns
$\overline{WR}$ or $\overline{RD}$ pulse width	$t_{WLWH}$	250		ns
Data setup before $\overline{WR}$	$t_{QVWH}$	50		ns
Data hold after $\overline{WR}$	$t_{WHQX}$	18		ns
Data hold after $\overline{RD}$	$t_{RHDX}$		90	ns
Chip select (2, 3) before $\overline{RD}$ , $\overline{WR}$	$t_{CS}$	50		ns
Chip select (2, 3) after $\overline{RD}$ , $\overline{WR}$	$t_{SC}$	18		ns
Chip select 1 before ALE	$t_{CSLH}$	20		ns
Chip select 1 after $\overline{RD}$ , $\overline{WR}$	$t_{CSWH}$	50		ns
Output delay time	$t_{RLDV}$		200	ns
Input capacitance to $V_{SS}$ (for each input)	$C_I$		10	pF





Timing Diagram



## Application Circuit

SAE 81C52 with the  $\mu$ C SAB 8051