SIEMENS

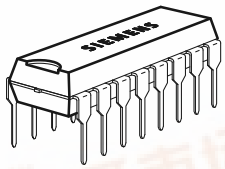
CMOS RAM

SAE 81C54

Preliminary DataACMOS IC

Features

- 512 x 8 bit-organization
- Multiplexed address and data bus
- Tristate address and data lines
- On-chip address register
- Very low current consumption: 1 µA at 5.5 V during standby
- Dual chip selection
- Wide supply voltage range from 2.5 V to 5.5 V
- Fully compatible 5 V ± 10 %
- Data retention up to 1.0 V
- Temperature range – 40 to 110 °C

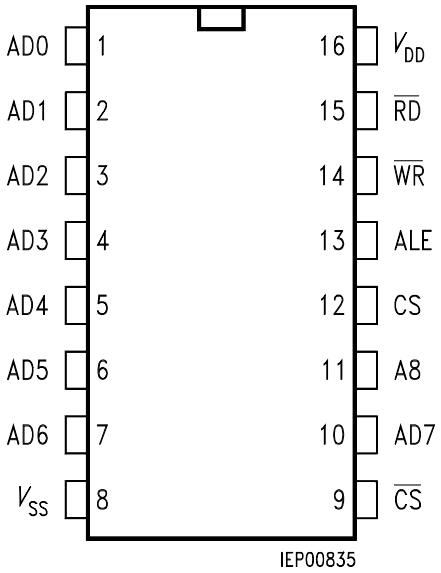


P-DIP-16-1

Type	Ordering Code	Package
SAE 81C54 P	Q67100-H8486	P-DIP-16-1

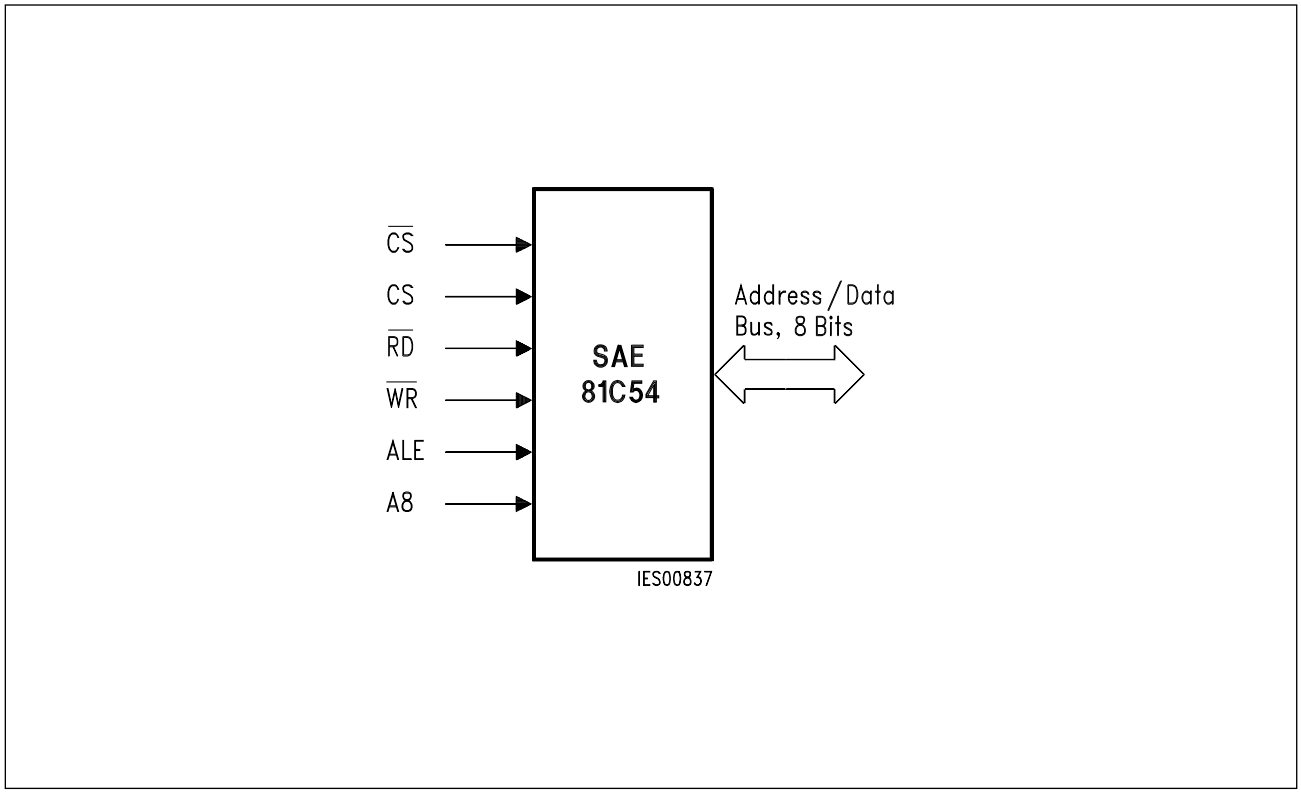
The SAE 81C54 P is a static 4096-bit RAM (512 words by 8 bits) in Advanced CMOS technology. The address and data bus in the multiplex operation allows directly interfaces to 8-bit microprocessors/microcontroller families, e.g. SAB 8086, SAB 8088, SAB 8051. Due to its low power dissipation of less than 1 µA in standby mode this component requires only minimum supply current.

Pin Configurations
(top view)



Pin Definitions and Functions

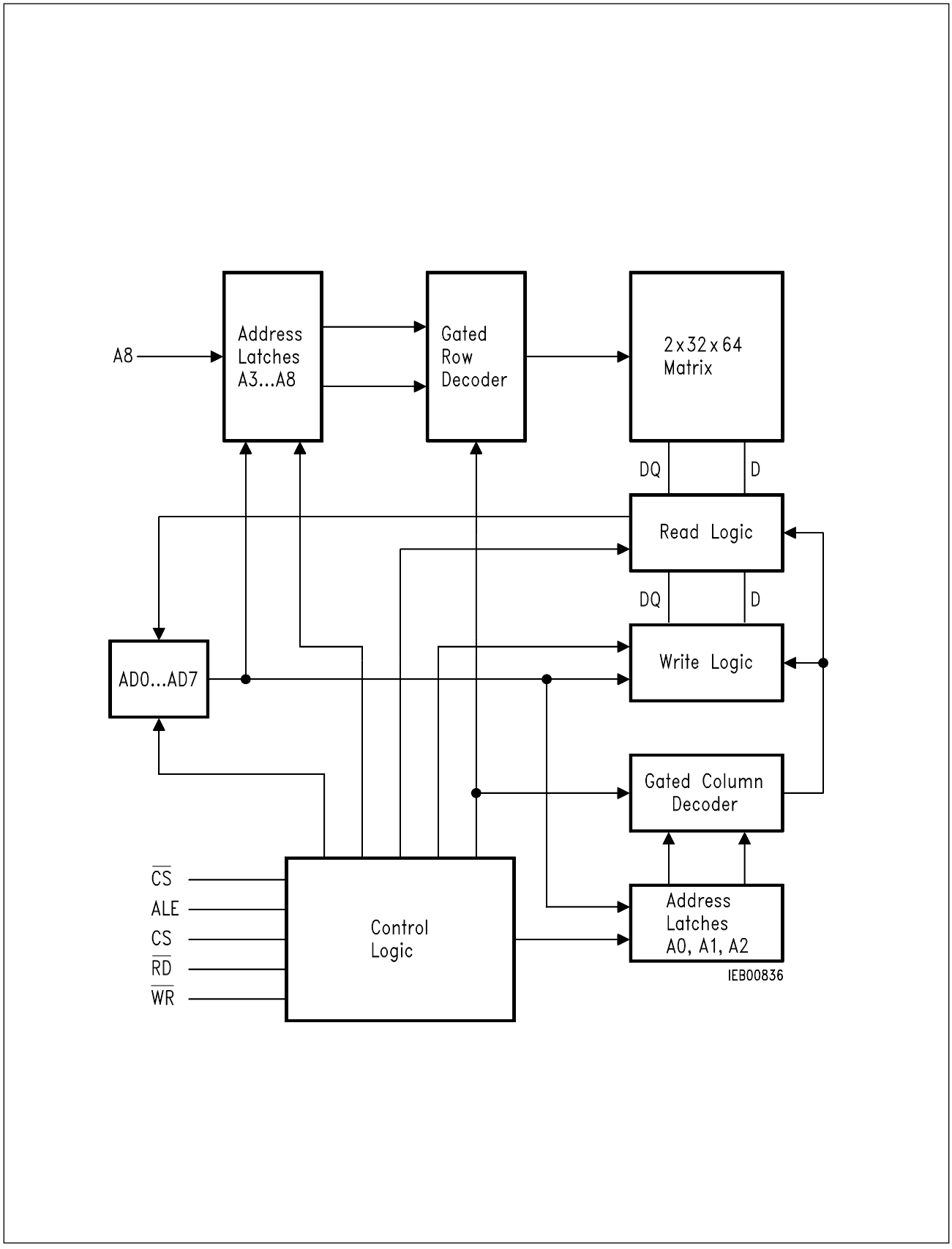
Pin No.	Symbol	Function
1-7, 10	AD0-7	Address/data lines
8	V_{SS}	Ground
9	$\overline{CS}$	Chip select
11	A8	Address line
12	CS	Chip select
13 14 15	ALE $\overline{WR}$ $\overline{RD}$	Address signal latch enable Write enable Read enable
16	V_{DD}	Supply voltage



Logic Symbol

Truth Table for Control and Data Bus Pin Status

$\overline{CS}$	CS	$\overline{RD}$	$\overline{WR}$	AD0-7 During Data Phase	Function
H	X	X	X	Floating	None
X	L	X	X	Floating	None
L	H	L	H	Data from memory	Read
L	H	H	L	Data to memory	Write



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature	T_A	– 40 to 110	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance system - air	$R_{th\ SA}$	70	K/W

DC Characteristics

T_A = – 40 to 110 °C; V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Standby supply current	I_{DD}			1	µA	T_A = 25 °C
Operating supply current	I_{DD}		500		µA	100-kHz ALE
Operating supply voltage	V_{DD}	2.5		5.5	V	
Standby supply voltage	V_{DD}	1.0		5.5	V	Data retention
Input current	I_{IL}			1	µA	V_I = 0 – 5.5 V
Output leakage current	I_{QL}			1	µA	V_Q = 0 – 5.5 V floating
L-input voltage (V_{DD} < 4.5 V)	V_I	– 0.8		0.6	V	
L-input voltage (V_{DD} > 4.5 V)	V_{IL}	– 0.8		0.8	V	
H-input voltage	V_{IH}	0.6 x V_{DD}		V_{DD} + 0.8	V	
H-input voltage	V_{IH}			V_{DD} + 0.8	V	V_{DD} = 5 V

DC Characteristics (cont'd)

T_A = – 40 to 110 °C; V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-output voltage (V_{DD} < 4.5 V)	V_{QL}			0.4	V	I_{QL} = 1 mA
L-output voltage (V_{DD} > 4.5 V)	V_{QL}			0.4	V	I_{QL} = 2 mA
H-output voltage (V_{DD} < 4.5 V)	V_{QH}	0.75 x V_{DD}			V	I_{QH} = 1 mA
H-output voltage (V_{DD} > 4.5 V)	V_{QH}	0.75 x V_{DD}			V	I_{QH} = 2 mA

AC Characteristics

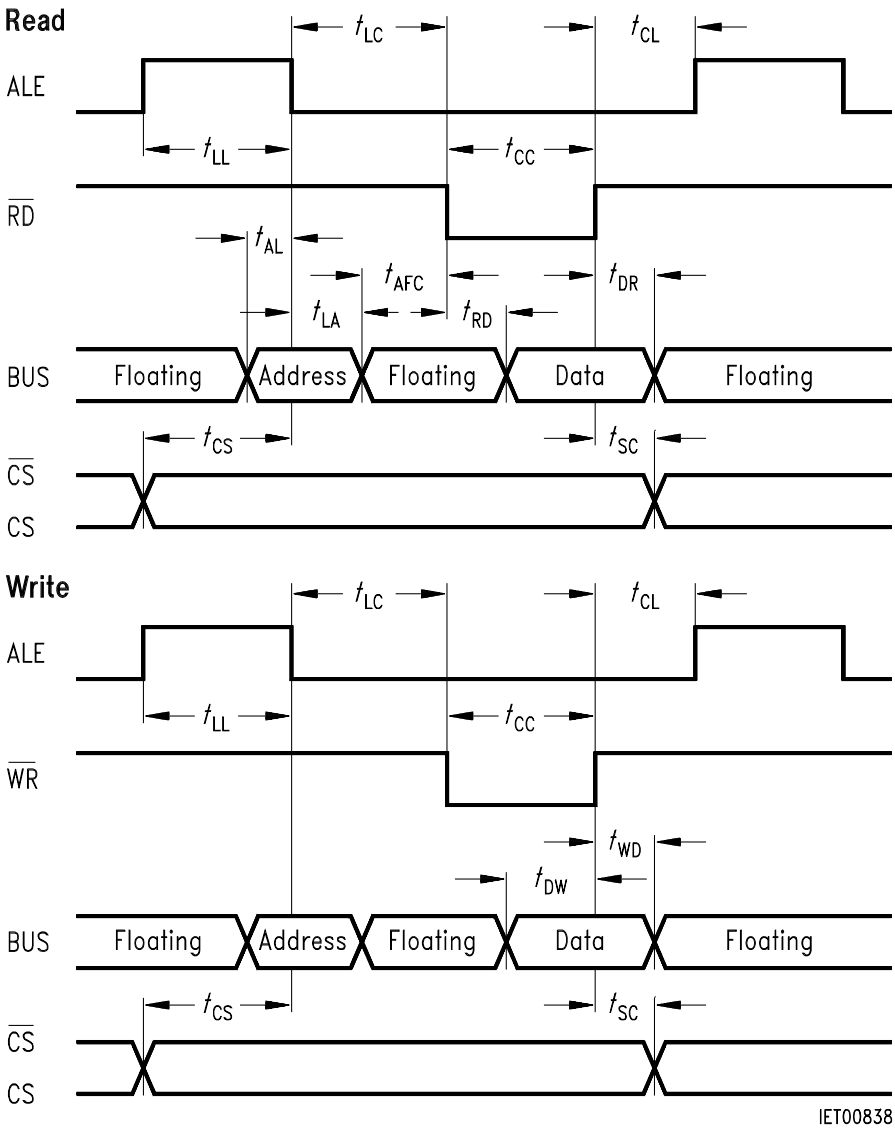
T_A = – 40 to 110 °C; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LL}	40		ns
Address setup before ALE	t_{AL}	25		ns
Address hold after ALE	t_{LA}	25		ns
$\overline{WR}$ pulse width	t_{CC}	60		ns
$\overline{RD}$ pulse width	t_{CW}	130		ns
Data setup before $\overline{WR}$	t_{DW}	70		ns
Data hold after $\overline{WR}$	t_{WD}	20		ns
Data hold after $\overline{RD}$	t_{DR}		30	ns
Access time $\overline{RD}$ to data output	t_{RD}		130	ns
Address floating to $\overline{RD}$	t_{AFC}	0		ns
CS before ALE	t_{CS}	30		ns
CS after $\overline{WR}$ or RD	t_{SC}	10		ns
ALE to $\overline{RD}$ or $\overline{WR}$	t_{LC}	35		ns
RD or $\overline{WR}$ to ALE = high	t_{CL}	25		ns

AC Characteristics

T_A = – 40 to 110 °C; V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LL}	60		ns
Address setup before ALE	t_{AL}	40		ns
Address hold after ALE	t_{LA}	60		ns
$\overline{WR}$ pulse width	t_{CC}	200		ns
$\overline{RD}$ pulse width	t_{CW}	350		ns
Data setup before $\overline{WR}$	t_{DW}	200		ns
Data hold after $\overline{WR}$	t_{WD}	60		ns
Data hold after $\overline{RD}$	t_{DR}		95	ns
Access time $\overline{RD}$ to data output	t_{RD}		350	ns
Address floating to $\overline{RD}$	t_{AFC}	0		ns
CS before ALE	t_{CS}	80		ns
CS after $\overline{WR}$ or $\overline{RD}$	t_{SC}	30		ns
ALE to $\overline{RD}$ or $\overline{WR}$	t_{LC}	60		ns
RD or $\overline{WR}$ to $\overline{ALE}$ = high	t_{CL}	30		ns


Read
ALE
RD
BUS
CS
CS
Write
ALE
WR
BUS
CS
CS
t_{LC}
t_{CL}
t_{LL}
t_{CC}
t_{AL}
t_{AFC}
t_{DR}
t_{LA}
t_{RD}
t_{CS}
t_{SC}
t_{WD}
t_{DW}
Floating
Address
Floating
Data
Floating
IET00838

Diagrams