SIEMENS

DSR QPSK-Demodulator

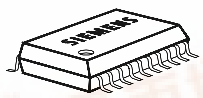
SDA 6310X

Preliminary Data

Bipolar IC

Features

- Internal reference voltage source.
- Automatic gain control (AGC) with integrated AGC amplifier.
- Output for adjustable delayed tuner AGC.
- Oscillator circuitry for VCO with external varicaps.
- Symmetrical demodulator output for inphase arm.
- Open collector counter output for measurement of oscillator frequency.
- Phase detector circuitry with offset adjust and turn off facility, including arm filters to suppress high frequency terms.
- Data separator for inphase and quadrature arm, output voltage levels TTL input compatible.



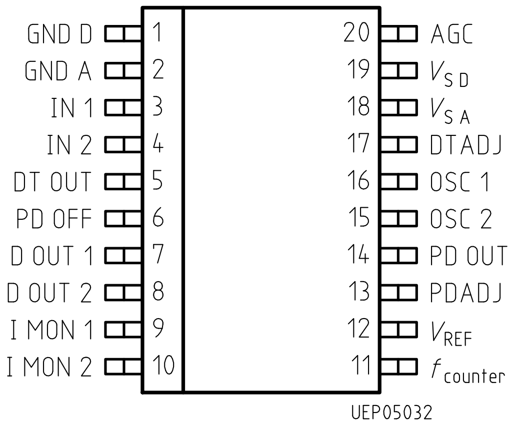
P-DSO-20-1

Type	Ordering Code	Package
SDA 6310X	Q67000-A5089	P-DSO-20-1 (SMD)

The SDA 6310 is an integrated circuit for amplification and demodulation of QPSK-modulated signals.

Pin Configuration
(top view)

P-DSO-20-1

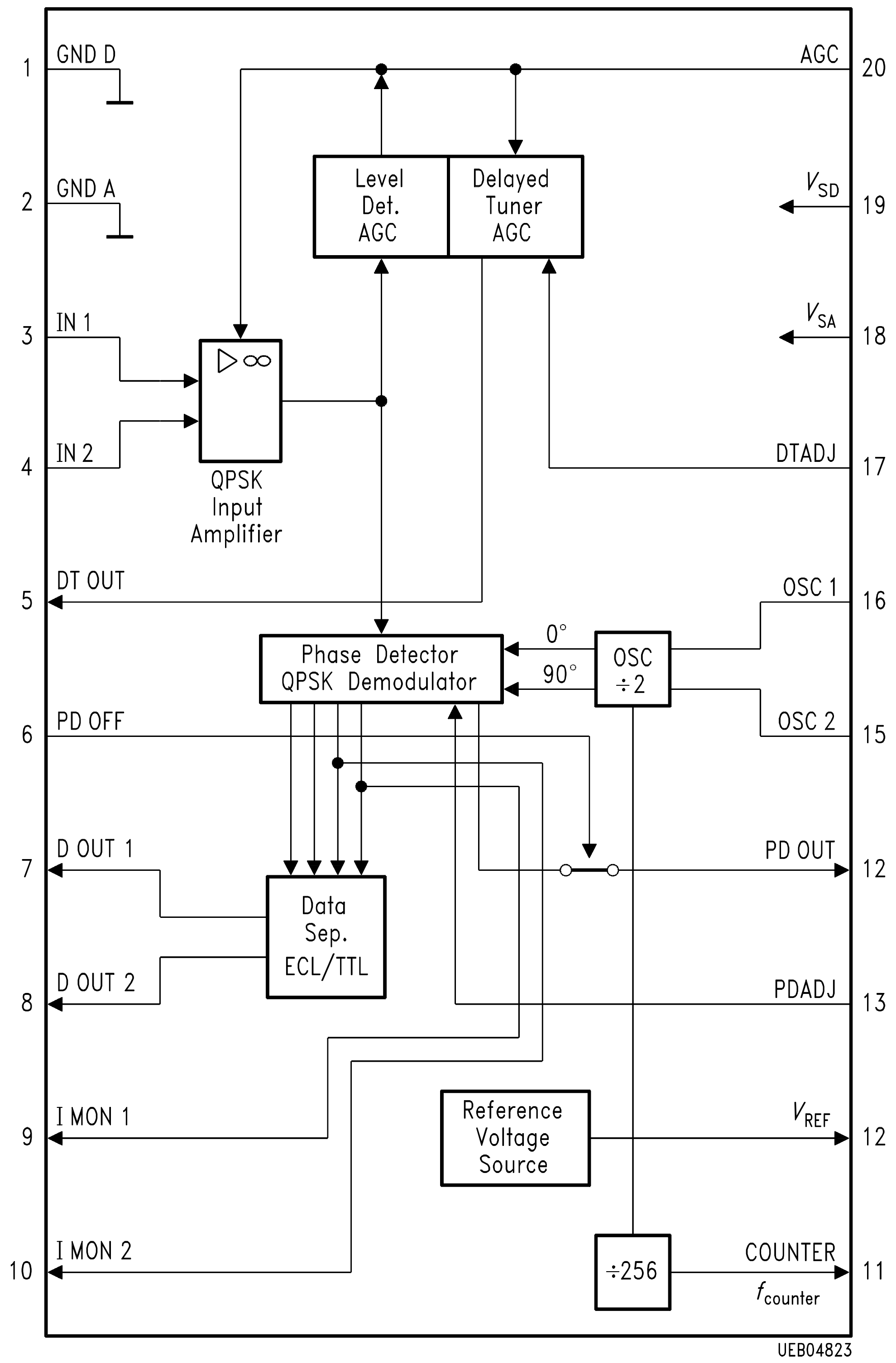


Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND D	Digital GND
2	GND A	Analog GND
3	IN 1	QPSK input 1
4	IN 2	QPSK input 2, inverse polarity
5	DT OUT	Delayed Tuner AGC output
6	PD OFF	Phase Detector off input
7	D OUT 1	Data output 1
8	D OUT 2	Data output 2
9	I MON 1	Inphase monitor output 1
10	I MON 2	Inphase monitor output 2
11	$f_{counter}$	Counter frequency output
12	V_{REF}	Reference Voltage Source
13	PDADJ	Phase Detector offset adjust input
14	PD OUT	Phase Detector output
15	OSC 2	Oscillator pin 2
16	OSC 1	Oscillator pin 1
17	DTADJ	Delayed Tuner AGC adjust input
18	$V_{S\,A}$	Analog supply voltage
19	$V_{S\,D}$	Digital supply voltage
20	AGC	Automatic Gain Control

Pin Description

Pin No.	Description
1	Digital GND (counter, data separator, automatic gain control unit).
2	Analog GND (AGC amplifier, oscillator, phase detector, reference voltage source). Reference point for input signal, input filter, PLL loop filter and offset adjust, oscillator, and AGC voltage. Short connection to digital GND required.
3	QPSK input 1.
4	QPSK input 2, inverse polarity.
5	Delayed tuner AGC output, open collector.
6	Phase detector off input, high level switches the phase detector output to high impedance state.
7	Data output 1, inphase arm.
8	Data output 2, quadrature arm.
9	Inphase monitor output 1, inverse polarity.
10	Inphase monitor output 2.
11	Counter frequency output, open collector output ($f_{counter} = f_{carr}/256$).
12	Reference voltage source output, DC reference point for phase detector output, phase detector offset adjust, and delayed tuner AGC adjust.
13	Phase detector offset adjust input.
14	Phase detector output, PLL loop filter.
15	Oscillator pin 2, inverse polarity.
16	Oscillator pin 1 (Oscillator pins 1 and 2 may be used as inputs to force the oscillator).
17	Delayed tuner AGC adjust input. If no delayed tuner AGC is used, connect to digital supply voltage.
18	Analog supply voltage (AGC amplifier, oscillator, phase detector, reference voltage source).
19	Digital supply voltage (counter, data separator, automatic gain control unit).
20	Automatic gain control filter pin, low voltage corresponds to maximum gain of the QPSK input amplifier.



Block Diagram

Circuit Description

Power Supply, Reference Voltage Source

The SDA 6310 has separated power supplies for digital and analog parts. A temperature stable reference voltage source is used for the operating points.

QPSK Input Amplifier, AGC

The input amplifier is a variable gain amplifier with symmetrical input. The gain control voltage is derived from a level detector at the amplifier output. If the input level exceeds an adjustable value, a sink current is generated which may be used to reduce the tuner output level.

Oscillator

The symmetrical oscillator contains a divider by 2 to generate the 0° and 90° signals used for the demodulation of the inphase and the quadrature component. For frequency measurement there is a counter output with carrier frequency divided by 256.

Phase Detector

There is an inphase and a quadrature arm consisting of AM demodulator and armfilter to suppress high frequency terms. The demodulated and filtered inphase and quadrature components are passed to the data separator and the multiplier/adder circuitry. The muliplier/adder circuitry is used to produce a phase detector characteristic with 4 stable points. The phase detector offset current is adjustable, the output can be turned off to high impedance state. The demodulated and filtered inphase component can be monitored at a symmetrical output.

Data Separator

2 data streams are separated from the analog inphase and quadrature component signals and converted to TTL input compatible voltage levels.

Absolute Maximum Ratings

T_A = – 40 °C to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Analog GND	V_2	– 0.1	0.1	V	
QPSK input 1	V_3	0	6	V	
QPSK input 2	V_4	0	6	V	
Delayed tuner AGC output	V_5	0	13.2	V	
Phase detector off input	V_6	0	13.2	V	
Data output 1	I_7	– 5	5	mA	
Data output 2	I_8	– 5	5	mA	
Inphase monitor output 1	I_9	– 5	0.5	mA	
Inphase monitor output 2	I_{10}	– 5	0.5	mA	
Counter frequency output	I_{11}	0	5	mA	
Counter frequency output	V_{11}	0	13.2	V	
Reference voltage source	I_{12}	– 5	1	mA	except capacitive load current at power on
Phase detector offset adjust input	V_{13}	0	V_{12}	V	
Phase detector output	V_{14}	0	V_{18} – 1.5	V	
Oscillator pin 2	V_{15}	0	5	V	
Oscillator pin 1	V_{16}	0	5	V	
Delayed tuner AGC adjust input	V_{17}	0	V_{12}	V	
Analog supply voltage	V_{18}	0	13.2	V	
Digital supply voltage	V_{19}	0	13.2	V	
Automatic gain control	V_{20}	0	V_{19}	V	
Junction temperature	T_J	– 40	150	°C	
Storage temperature	T_S	– 40	125	°C	
Thermal resistance	$R_{th\ SA}$		90	K/W	
ESD-Voltage, HBM	V_{ESD}	– 4	4	kV	100 pF, 1500 Ω

Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Operating Range					
Analog supply voltage	V_{18}	10.8	13.2	V	
Digital supply voltage	V_{19}	10.8	13.2	V	
Oscillator frequency	$f_{15,\ 16}$	70	240	MHz	
QPSK carrier frequency	$f_{3,\ 4}$	35	120	MHz	
Data rate	$DR_{7,\ 8}$	0	15	Mbit/s	
Data output load	$C_{7,\ 8}$	0	10	pF	
Reference source DC current	$I_{12,\ \mathrm{DC}}$	– 2.5	0.5	mA	
Reference source peak current	I_{12}	– 5	1	mA	
Ambient temperature	T_{A}	0	70	°C	

AC/DC-Characteristics

T_A = – 25 °C; V_S = 12 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Total supply current	I_S		50	65	mA	$I_{18} + I_{19}$

Power Supply

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Digital supply current	I_{19}		18	25	mA	
Analog supply current	I_{18}		32	45	mA	

Reference Voltage Source

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Reference voltage	V_{12}	5.5	6	6.5	V	
Line regulation	ΔV_{12}	0	30	60	mV	$V_{18, 19}$ = 10.8 → 13.2 V
Load regulation	ΔV_{12}	0	20	60	mV	I_R = – 5 to 1 mA
Temperature reg.	ΔV_{12}	– 60	0	60	mV	T_A = 0 °C to 70 °C

AGC Unit
Input Amplifier
$f_{3, 4}$ = 40.15 MHz

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
inp. imp. resistive inp. imp. capacitive	R_3, R_4 C_3, C_4	0.7	1 1	1.3	kΩ pF	
AGC low voltage	$V_{20\ L}$	0.2	0.7	1.2	V	$V_{3, 4}$ = 52 dB/µV[1)]
AGC high voltage	$V_{20\ H}$	2.7	3.2	3.7	V	$V_{3, 4}$ = 98 dB/µV
Minimum input level	$V_{3,\ 4\ min}$		49	52	dB/µV	V_{20} = 0.2 V
Maximum input level	$V_{3,\ 4\ max}$	98	102	106	dB/µV	V_{20} = 5 V

AGC Load Characteristic
$f_{3, 4}$ = 40.15 MHz, reference level $V_{3, 4}$ = 86 dB/µV

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
AGC load current	$I_{20\ load}$	– 30	– 20	– 15	µA	$V_{3, 4}$ = 96 dB/µV[1)]
AGC sink current	$I_{20\ load}$	10	20	25	µA	$V_{3, 4}$ = 76 dB/µV
AGC load character.	ΔI_{20}	– 11	– 8	– 5	µA/dB	$V_{3, 4}$ = 85 → 87 dB/µV

1) Note 1
(see page 72)

AC/DC-Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delayed Tuner AGC (DTAGC) V_{17} = 2 V, V_5 = 5 V						
DTAGC ON current	$I_{5\ ON}$	3	6		mA	$V_{20} = V_{17}$ + 0.1 V[2)]
DTAGC OFF current	$I_{5\ OFF}$		0.05	0.5	mA	$V_{20} = V_{17}$ – 0.2 V
DTAGC characteristic	$\Delta I_5/\Delta V_{20}$	20	30	45	mA/V	$V_{20} = V_{17}$ – 10 mV...V_{17} + 10 mV
DTAGC DC volt. range	V_{17}	0		V_{12}	V	
Frequency Response reference frequency 40.15 MHz						
high level upper limit	$f_{max\ H}$	130	150		MHz	$V_{3,\ 4}$ = 98 dB/µV, – 3 dB I MON 1,2
high level lower limit	$f_{min\ H}$		20	25	MHz	$V_{3,\ 4}$ = 98 dB/µV, – 3 dB I MON 1,2
low level upper limit	$f_{max\ L}$	130	180		MHz	$V_{3,\ 4}$ = 52 dB/µV, – 3 dB I MON 1,2
low level lower limit	$f_{min\ L}$		25	30	MHz	$V_{3,\ 4}$ = 52 dB/µV, – 3 dB I MON 1,2
Input Amplifier $f_{3,\ 4}$ = 118 MHz						
AGC low voltage	$V_{20\ L}$	0.5	1	1.5	V	$V_{3,\ 4}$ = 52 dB/µV
AGC high voltage	$V_{20\ H}$	2.7	3.2	3.7	V	$V_{3,\ 4}$ = 98 dB/µV
Minimum input level	$V_{3,\ 4\ min}$		46	52	dB/µV	V_{20} = 0.2 V
Maximum input level	$V_{3,\ 4\ max}$	98	105	109	dB/µV	V_{20} = 5 V

2) Note 2
(see page 73)

AC/DC-Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Phase Detector (PD)						
PD Gain	PDG	700	950	1200	µA/ rad	[3]
PD DC range	V_{14}	2.5	V_{12}	V_{18} – 1.5	V	
PD large signal offset current	$I_{14/12}$	– 30	0	30	µA	
PD DC-offset current	$I_{14/12}$	– 30	0	30	µA	$V_{3,\,4} = 0$
PD offset adjust current range	$I_{14/12}$ $I_{14/12}$	– 90 5	– 30 30	– 5 90	µA µA	V_{13} = 1.5 V V_{13} = 4.5 V
PD offset adjust characteristic	$\Delta I_{14}/\Delta V_{13}$	30	40	50	µA/V	V_{13} = 2.5 → 3.5 V
PD offset adjust input impedance		3.5	5	6.5	kΩ	
Leakage current PD OFF	$I_{14/12}$	– 0.2	0	0.2	µA	$V_{14} = V_{12}$, $V_6 = V_{12}$
PD source resistor	R_{14}	300	400		kΩ	
Input voltage PD OFF	$V_{6\ OFF}$	2.0			V	[4]
Input voltage PD ON	$V_{6\ ON}$			0.8	V	
PD OFF threshold	$V_{6\ thr}$	0.8	1.4	2.0	V	
Low input current	$I_{6\ L}$	– 10	– 0.6	0	µA	$V_6 = 0$
High input current	$I_{6\ H}$	0	0.05	1	µA	$V_6 = V_{18}$
Monitor Output						
Monitor DC voltage	V_9 = , V_{10} =	V_{18} – 4	V_{18} – 3.5	V_{18} – 3	V	
Monitor AC voltage	$V_{10\sim} - V_{9\sim}$	350	500	650	mV_{pp}	

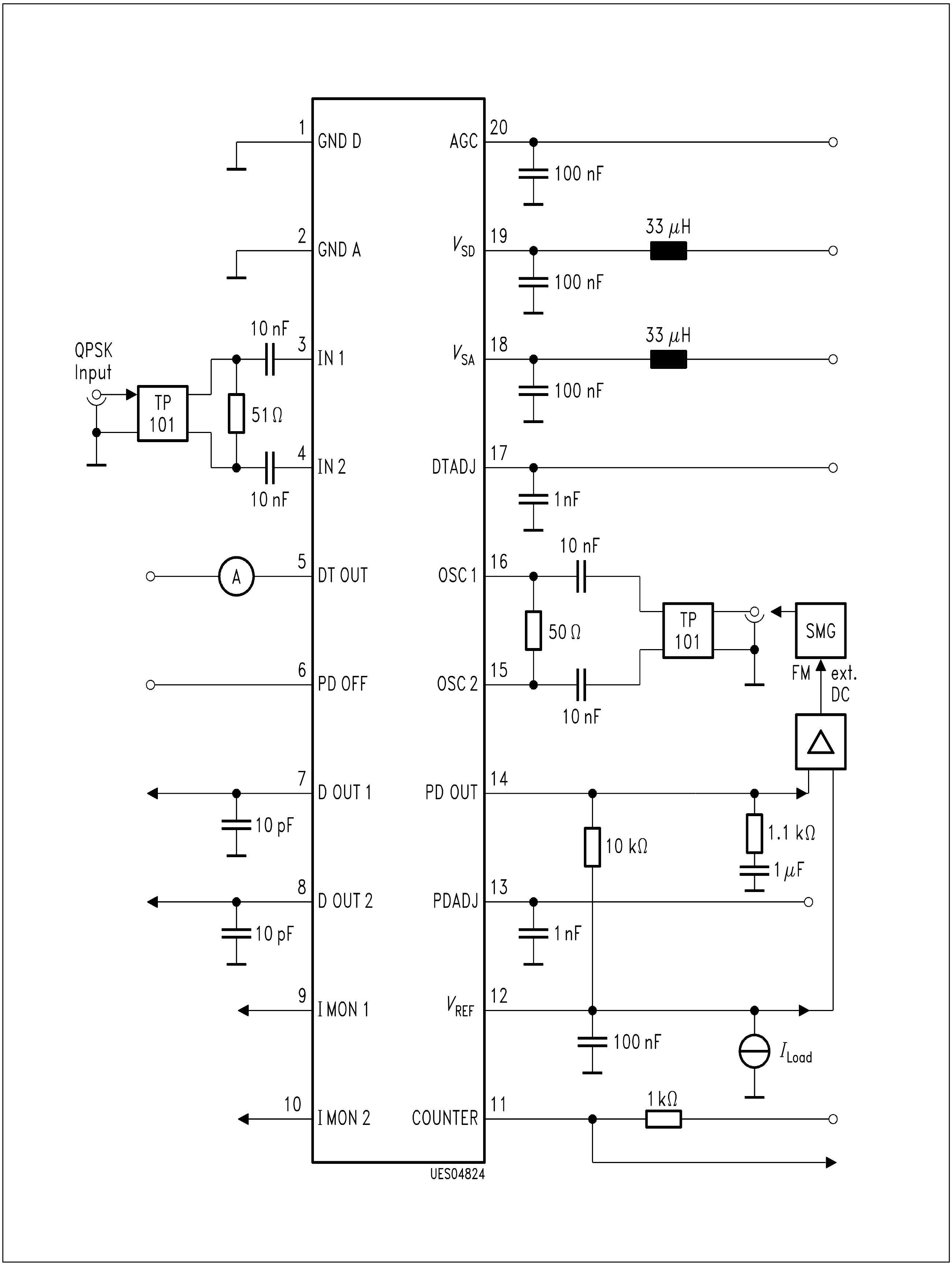
3) Note 3
(see page 74)

4) Note 4
(see page 75)

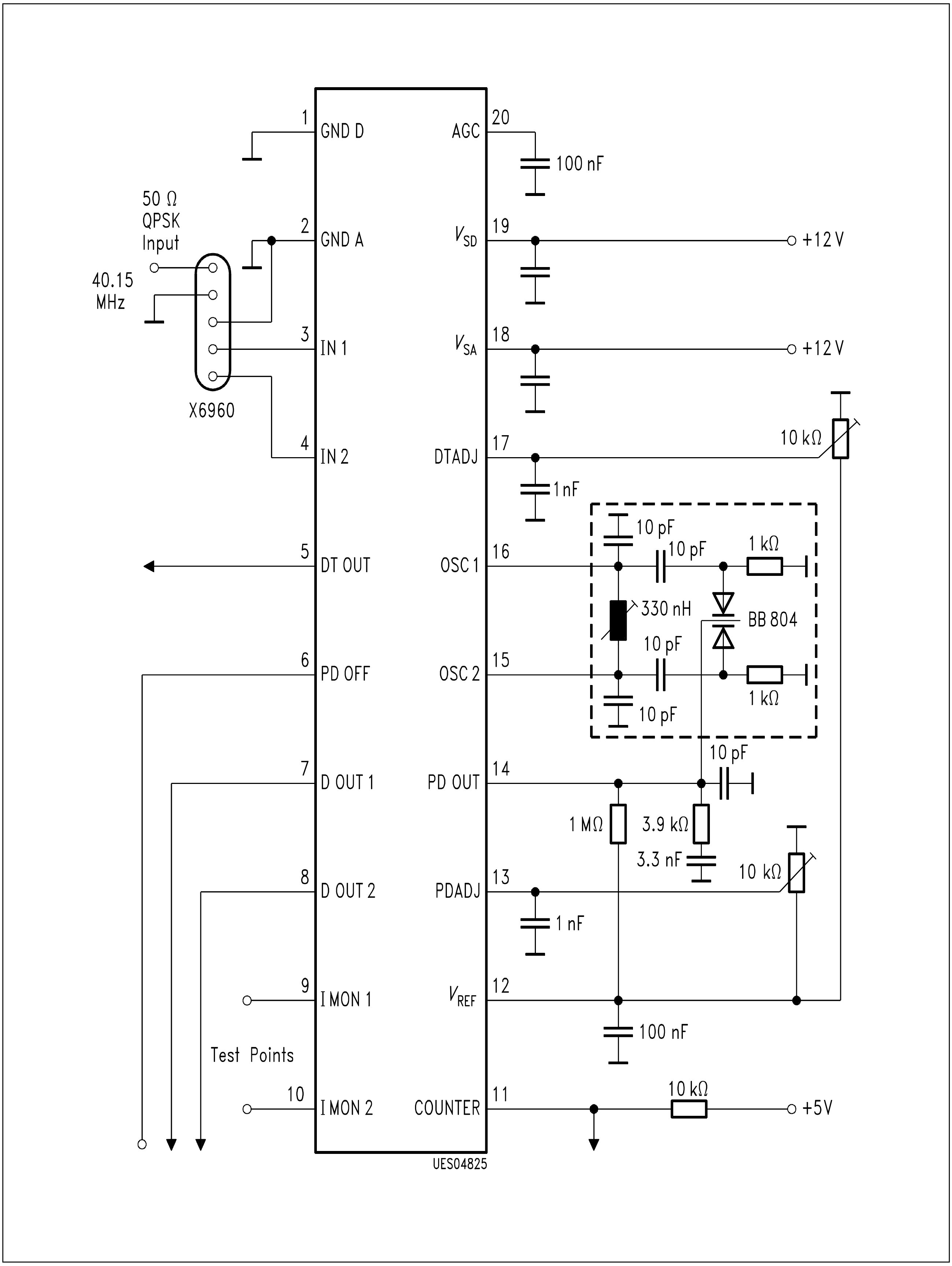
AC/DC-Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Data Separator						
Separator offset		– 5	0	5	%	
Output low level	$V_{7,\,8\,L}$		0.3	0.6	V	
Output high level	$V_{7,\,8\,H}$	2.4	3.0		V	
Rise time 0.8 V → 2.0 V	$t_{7,\,8\,rise}$		18	30	ns	$C_{7,\,8}$ = 10 pF
Fall time 2.0 V → 0.8 V	$t_{7,\,8\,fall}$		18	30	ns	$C_{7,\,8}$ = 10 pF
Oscillator[5)]						
Oscillator input threshold	$V_{15,\,16}$		97	102	dB/µV	PDG = – 3 dB
PD-Gain linearity	ΔPDG	– 1	0	1	dB	$V_{15,\,16}$ = 107 → 113 dB/µV
Oscillator input admittance	Y = G + jB, SIE = 1/Ω					
Real part	$G_{15,\,16}$		– 5	– 3	mS	f = 80.3 MHz
Imag. part	$B_{15,\,16}$		– 3		mS	f = 80.3 MHz
Real part	$G_{15,\,16}$		– 5	– 1	mS	f = 236 MHz
Imag. part	$B_{15,\,16}$		5		mS	f = 236 MHz
Oscillation level	V_{OSC} V_{OSC}	107 107	110 110	113 113	dB/µV dB/µV	f = 80.3 MHz f = 236 MHz
Counter Frequency Output $f_{counter} = f_{carr}/256 = f_{osc}/512$						
Low level voltage	$V_{11\,L}$			0.4	V	I_{11} = 3 mA
High level leakage curr.	$I_{11\,H}$			0.1	µA	V_{11} = 5 V
Rise time 10 → 90 %	$t_{11\,rise}$		500	800	ns	R_{11} = 10 kΩ (5 V), C_{load} = 10 pF
Fall time 90 → 10 %	$t_{11\,fall}$		10	200	ns	R_{11} = 10 kΩ (5 V), C_{load} = 10 pF

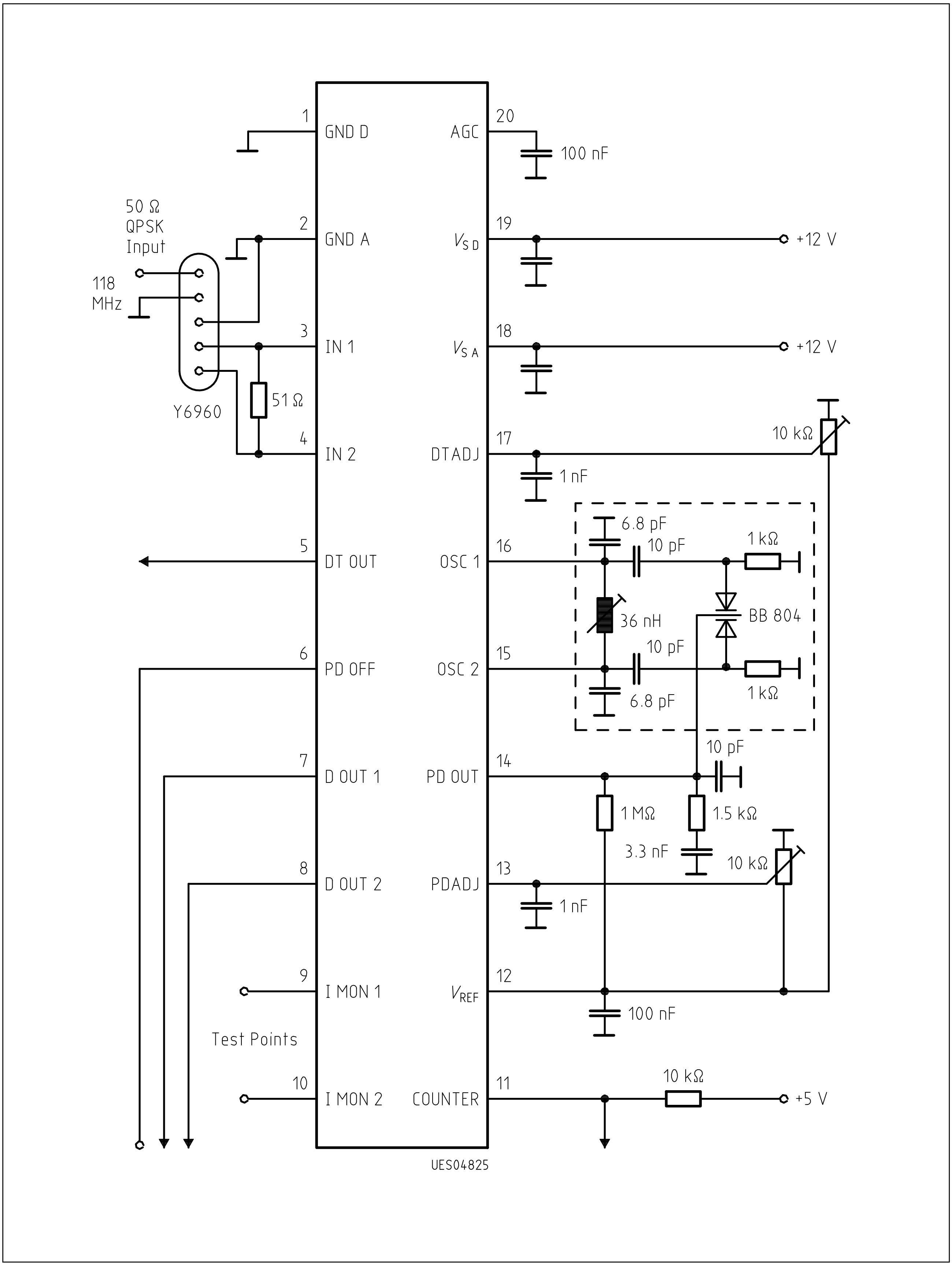
5) Note 5
(see page 75)



Test Circuit



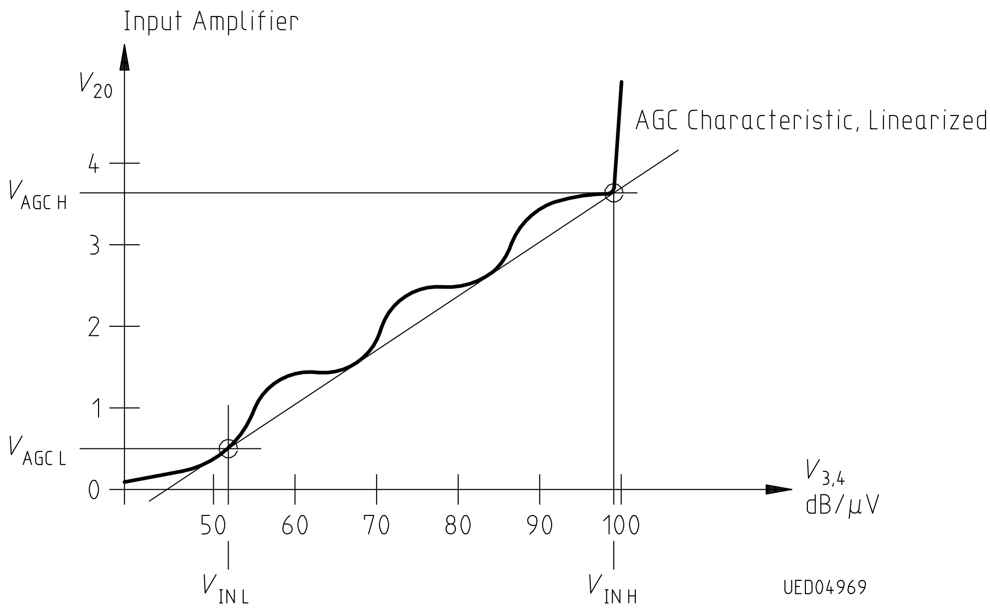
Application Circuit 40.15 MHz



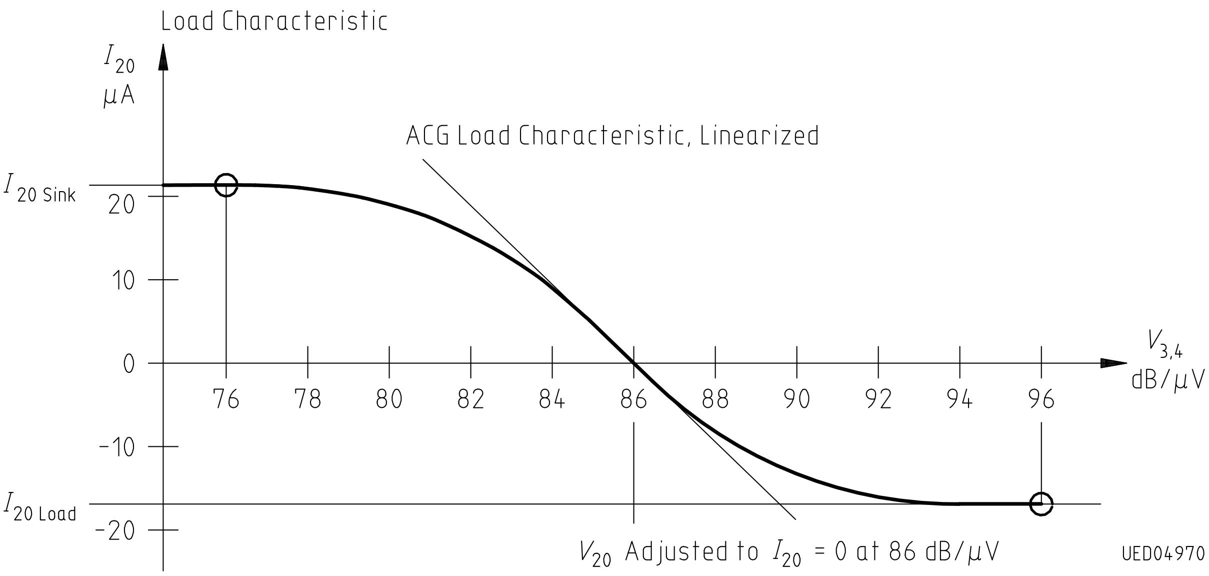
Application Circuit 118 MHz

Note 1
AGC Characteristics

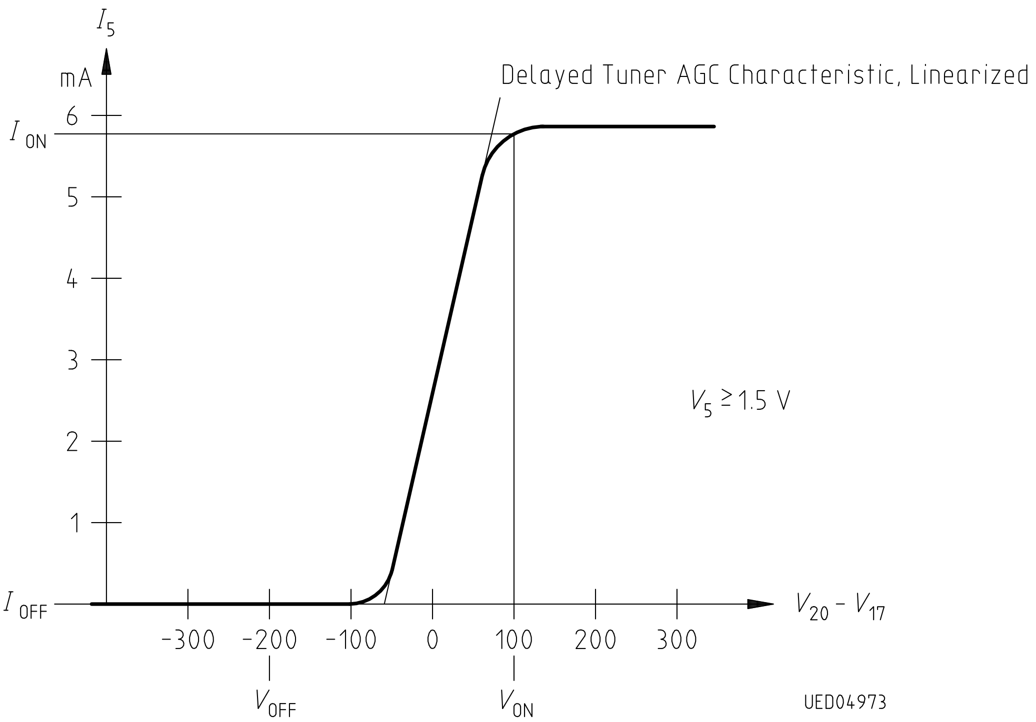
Input Amplifier



Load Characteristic

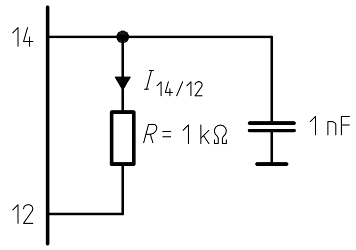


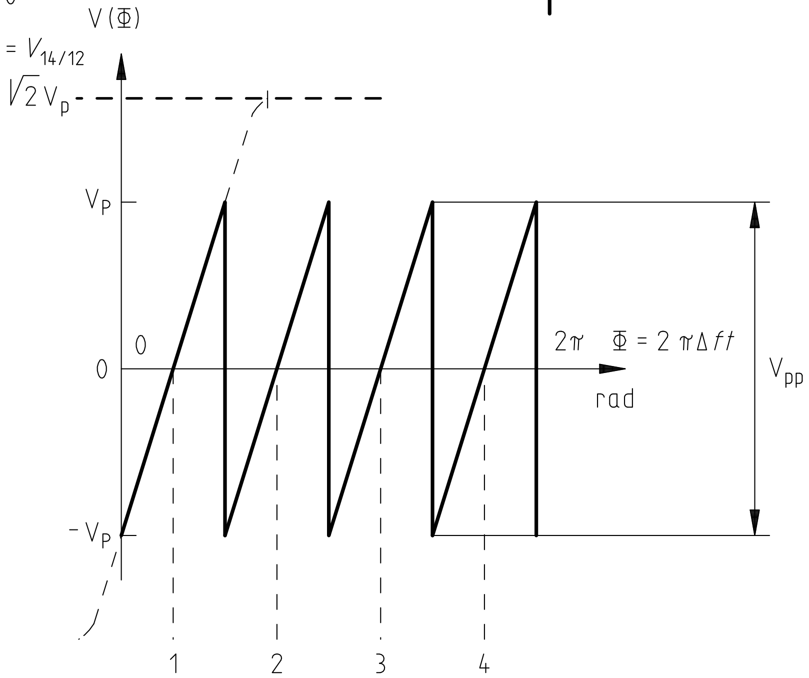
Note 2
Delayed Tuner AGC Characteristic



Note 3
Definition of Phase Detector Gain (*PDG*)

$V_{3,4} = 50\ mV_{rms}$
$f_{3,4} = 40.15\ MHz + 1\ kHz = 40.15\ MHz + \Delta f$
$V_{15,16} = 300\ mV_{rms}$
$f_{15,16} = 80.3\ MHz$
$V_6 = 0$
$I_{13} = 0$





$$\text{PD - Gain } PDG = \frac{1}{R} \cdot \frac{d(V_{14} - V_{12})}{dt} \cdot \frac{1}{2\pi\Delta f}\bigg|_{V_{14} - V_{12} = 0}$$

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Theorie:
$V(\Phi) = V_p \sin\Phi \text{ sign}(\cos\Phi) - V_p \cos\Phi \text{ sign}(\sin\Phi)$

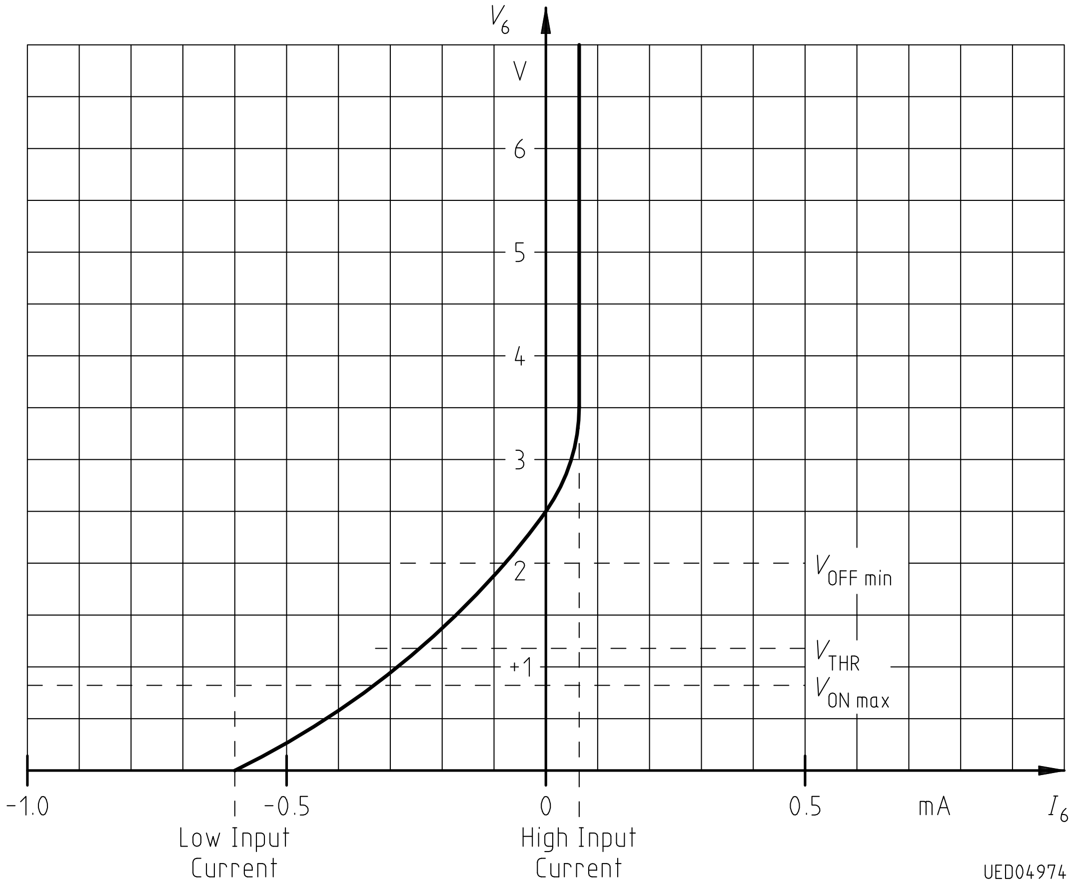
$$\text{PD-Gain} PDG = \sqrt{0.5} V_{pp}/R \frac{1}{\text{rad}} \text{(not exact because of non ideal waveform)}$$

Approximations: $PDG = 1.15\sqrt{0.5} V_{pp}/R \frac{1}{\text{rad}} = \frac{0.816 V_{pp}}{R\ \text{rad}}$

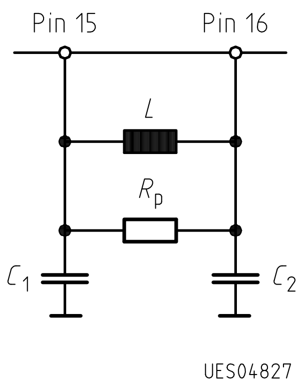
$$PDG = 1.09\sqrt{\frac{2\pi}{\pi - 2}} V_{rms}/R \frac{1}{\text{rad}} = \frac{2.56 V_{rms}}{R\ \text{rad}}$$

Application hint: PD-Gain is lower with data modulation on, typ. – 8 dB.

Note 4
PD OFF Input Characteristic



Note 5
Application Circuit for use of Internal Oscillator
(not subject to production testing)



Center Freq.	**80.3 MHz**	**236 MHz**	**Remarks**
L	330 nH	36 nH	Coil
C_1	12 pF	8.2 pF	Ceramic Capacitor
C_2	12 pF	8.2 pF	Ceramic Capacitor
R_p	2 kΩ	1 kΩ	Resistor