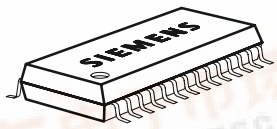
SIEMENS

Smart Sixfold Low-Side Switch TLE 5212 G

Features

- Overload protection
- Short circuit protection
- Cascadeable serial diagnostic interface
- Overvoltage protection
- Overtemperature monitoring
- µC compatible input
- **E**lectro**s**tatic **d**ischarge (ESD) protection
- Open drain outputs



P-DSO-28-6

Type	Ordering Code	Package
TLE 5216 G	Q67000-A9137	P-DSO-28-6

Application

- All kinds of resistive and inductive loads (relays, electromagnetic valves)
- µC compatible power switch for 12 V applications
- Solenoid control switch in automotive and industrial control systems

General Description

Sixfold Low-Side Switch in Smart Power Technology (SPT) with six independant inputs and six open drain DMOS output stages. The error feedback is done via a serial diagnostic interface.

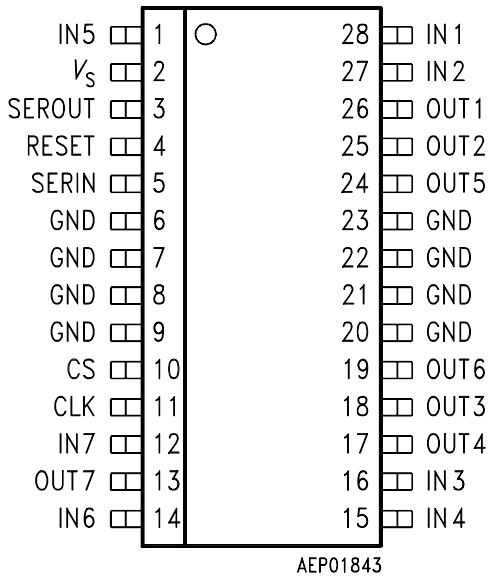
The TLE 5212 G is protected by embedded protection functions (Z-diodes from output to ground) and is particularly suitable for automotive and industrial applications.

Product Summary

Parameter	Symbol	Values	Unit
Supply voltage	V_S	5.5 … 24	V
Drain source clamping voltage (OUT1 - OUT6)	$V_{DS(AZ)max}$	34	V
ON resistance	$R_{ON(typ)\ 1\text{-}4}$	8	Ω
	$R_{ON(typ)\ 5,\ 6}$	0.8	Ω
Output current	$I_{D\ 1\text{-}4}$	4×50	mA
	$I_{D\ 5,\ 6}$	2×500	mA

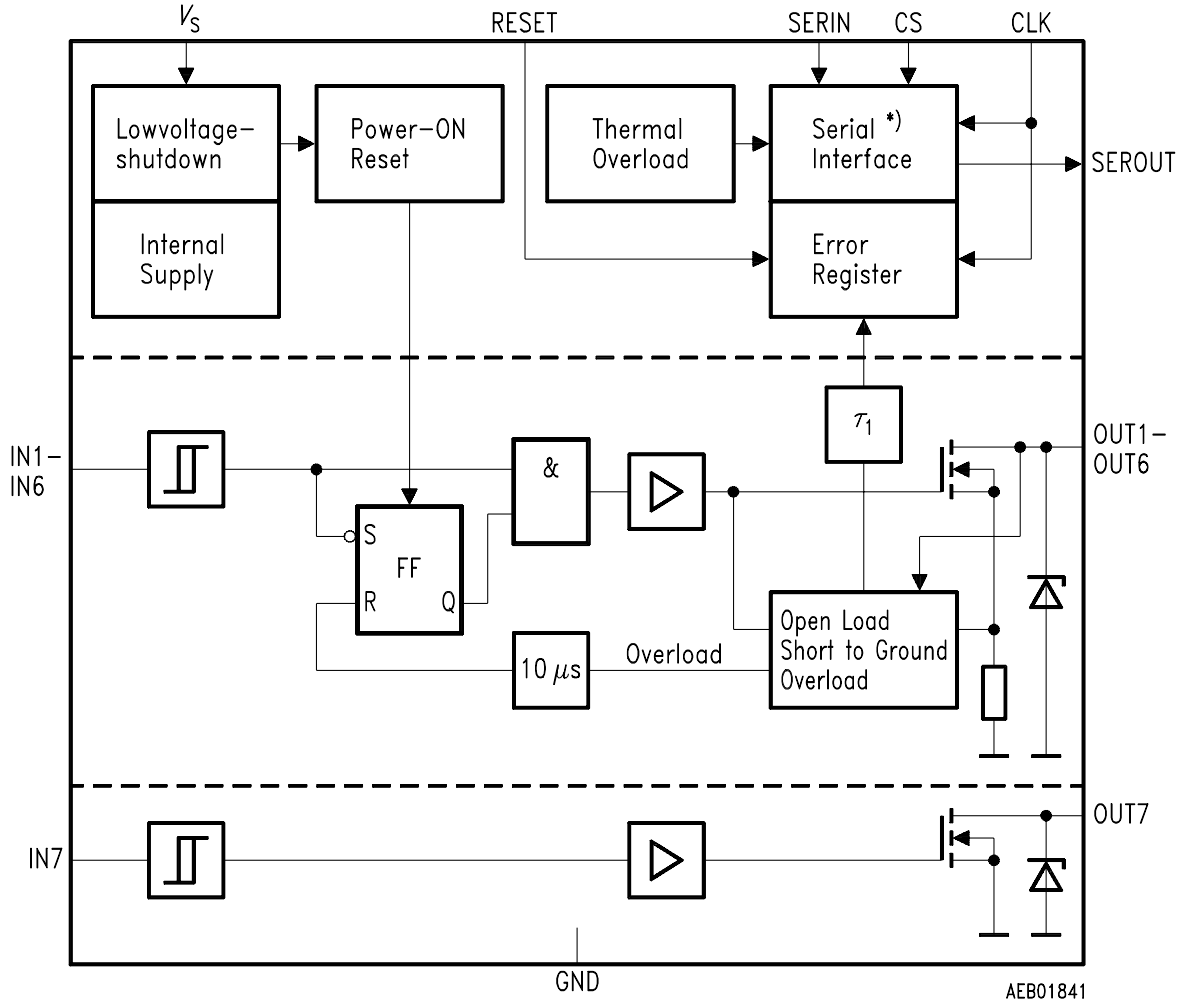
Pin Configuration
(top view)

TLE 5212 G



Pin Definitions and Functions

Pin No.	Symbol	Function
1	IN5	Input switch 5, active HIGH (500 mA) TTL level with hysteresis
2	V_S	Supply voltage, must be blocked to ground by capacitor
3	SEROUT	Diagnostic interface data OUT, connects to SERIN of mother IC or µC
4	RESET	Diagnostic interface reset, resets error flag register
5	SERIN	Diagnostic interface data IN, can be connected to SEROUT of mother IC
6, 7, 8, 9	GND	Ground, cooling, with copper area on PCB
10	CS	Diagnostic interface chip select, signal from µC activates data transfer
11	CLK	Diagnostic interface clock, signal from µC drives data transfer
12	IN7	Input switch 7, active HIGH (5 mA), TTL level with hysteresis
13	OUT7	Output switch 7, not protected, not monitored (5 mA)
14	IN6	Input switch 6, active HIGH (500 mA), TTL level with hysteresis
15	IN4	Input switch 4, active HIGH (50 mA), TTL level with hysteresis
16	IN3	Input switch 3, active HIGH (50 mA), TTL level with hysteresis
17	OUT4	Output switch 4 (50 mA), self protecting
18	OUT3	Output switch 3 (50 mA), self protecting
19	OUT6	Output switch 6 (500 mA), self protecting
20, 21, 22, 23	GND	Ground, cooling, with copper area on PCB
24	OUT5	Output switch 5 (500 mA), self protecting
25	OUT2	Output switch 2 (50 mA), self protecting
26	OUT1	Output switch 1 (50 mA), self protecting
27	IN2	Input switch 2, active HIGH (50 mA) TTL-level with hysteresis
28	IN1	Input switch 1, active HIGH (50 mA) TTL-level with hysteresis



*) For further informations see page 12.

Block Diagram

Application Description

Applications in automotive electronics call for intelligent power switches that can be activated by logical signals, which have to be shorted load protected and which provide error feedback.

This IC contains six power switches connected to ground (low-side switches). On inductive loads the integrated Z-diodes clamp the discharging voltage. In addition there is a 5 mA low-side-switch, which is not protected against overload and which is not included in the error monitoring.

The IC can be connected directly to the battery voltage (5.5 V … 24 V).

By means of TTL signals on the control inputs (active HIGH) all six switches can be activated independently of one another. The inputs are highly resistive and therefore must not be left unconnected but should always be on fixed potential (noise immunity).

The serial error feedback interface is cascadeable (see diagram).

Circuit Description

Input Circuits

The control inputs consist of TTL-compatible Schmitt-triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the DMOS power transistors.

Switching Stages

The output stages consist of DMOS power transistors with open drain. Each stage has its own protective circuit for limiting power dissipation and shorted load current, which makes the outputs shorted load protected to the supply voltage throughout the operating range. Integrated clamp-diodes limit positive voltage spikes that occur when inductive loads are discharged.

Monitoring and Protective Functions

Each power output is monitored for overload in its activated status. In deactivated mode open load or short to ground can be detected and differentiated.

In case of shorted load the outputs will be shutdown after a delay time of typically 10 µs. Shutdown is stored in a flip-flop. A reactivation of the switch is only possible if the concerned input is switched off and on again. The information of every single malfunction is registered and stored in the serial diagnostic interface.

If the junction temperature raises beyond 170 °C the bit for thermal overload in the serial diagnostic interface is set. The outputs are not shutdown!

The sequence of the bits is as follows:

Bit	Sequence
1	Thermal overload
2	Overload switch 6
3	Open load switch 6
4	Short to ground switch 6
5-7	Overload, open load, short to ground switch 5
8-10	Overload, open load, short to ground switch 4
11-13	Overload, open load, short to ground switch 3
14-16	Overload, open load, short to ground switch 2
17-19	Overload, open load, short to ground switch 1

All errors are stored until the information is read out via the serial interface.

The first puls on the clock line resets the error register. This error register can also be reset by a low signal at the RESET pin (pin 12), so it can be set to a defined status while the IC is switched on.

Via the SERIN-pin the serial diagnostic interface of a following IC can be connected through to the µC.

At a supply voltage of V_S = 5.5 V to 24 V full function is guaranteed.

Absolute Maximum Ratings

T_j = – 40 °C to 150 °C

Parameter		Symbol	Values	Unit
Supply voltage		V_S	0 … 45	V
Continuous drain source voltage		V_{DS}	– 0.7 … 25	V
Input voltage		V_{IN}	0 … 7	V
Operating temperature range		T_j	– 40 … 150	°C
Storage temperature range		T_{stg}	– 55 … 125	
Output current		$I_{D(lim)}$	Self limited	A
Output current at reverse poling		$I_{D\ 5,\ 6}$	– 500	mA
		$I_{D\ 1\text{-}4}$	– 50	
Output current during clamping		$I_{D(AZ)\ 5,\ 6}$	700	mA
(see diagram)		$I_{D(AZ)\ 1\text{-}4}$	70	
Thermal resistance	junction-case[1)]	R_{thJC}	19	K/W
	junction-ambient	R_{thJA}	60	

[1)] Pins 6 to 9 and 20 to 23 have to be connected to the ground-plane used as thermal heatsink to achieve the optimum thermal resistance.

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter		Symbol	Values	Unit
Supply voltage		V_S	5.5 … 24	V
Output voltage		$V_{DS(OUT)}$	– 0.3 … 24	V
Junction temperature		T_j	– 40 … 125	°C
Clock frequency	design value	f_{CLK}	2	MHz

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

V_S = 6 V to 16 V; T_j = – 40 °C to 140 °C (unless otherwise specified)

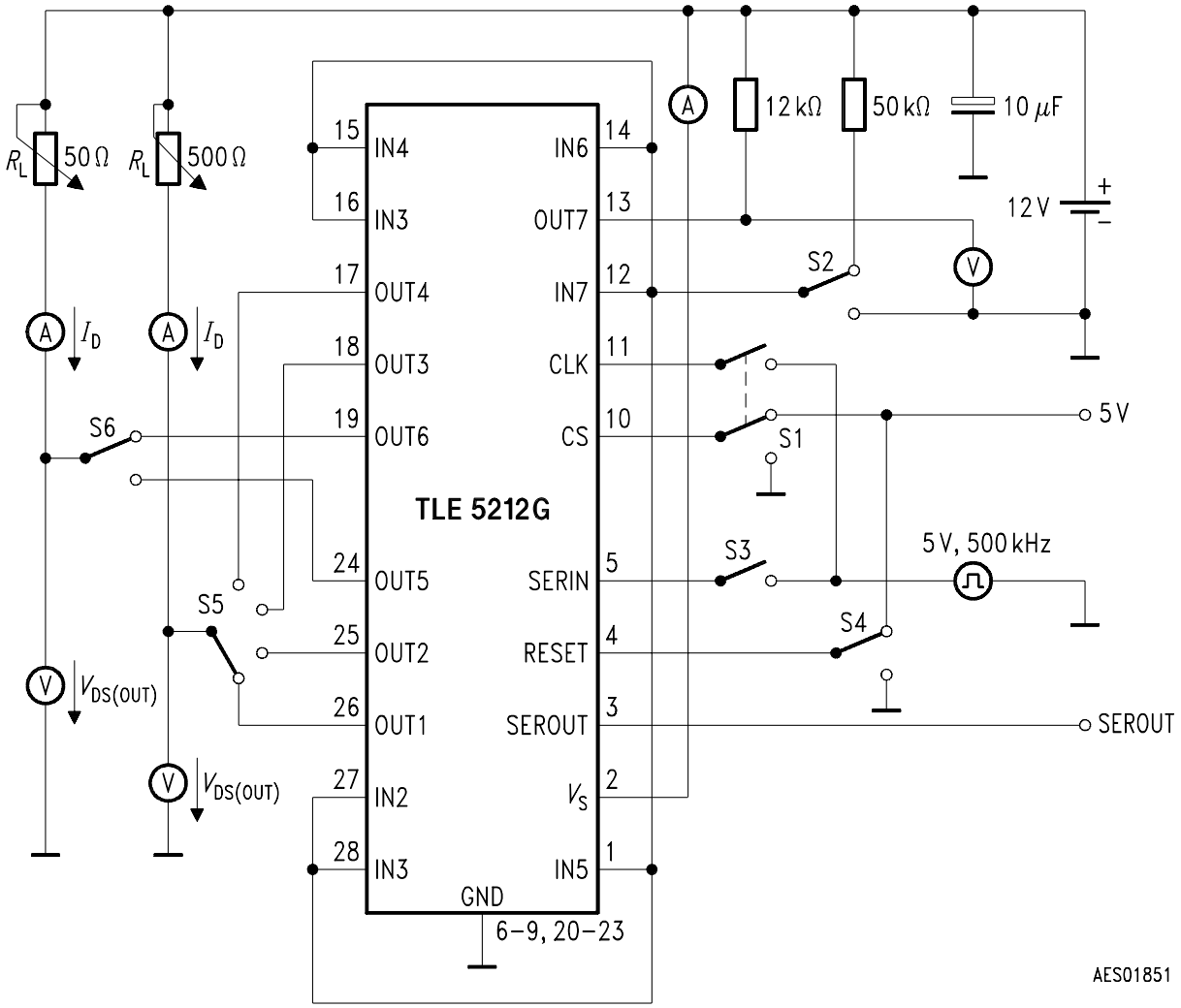
Parameter		Symbol	Limit Values			Unit
			min.	typ.	max.	
Power Supply (V_S)						
Supply current	Outputs ON	I_S			20	mA
	Outputs OFF				15	
Power Outputs						
ON state resistance;	T_j = 25 °C	$R_{DS(ON)\ 1\text{-}4}$		8		Ω
Channel 1-4	T_j = 140 °C				16	
ON state resistance;	T_j = 25 °C	$R_{DS(ON)\ 5,\ 6}$		0.8		Ω
Channel 5, 6	T_j = 140 °C				1.6	
Clamping voltage	I_D = 50 mA	$V_{DS(AZ)\ 1\text{-}4}$	24.2		32	V
(OUT1-OUT6)	I_D = 500 mA	$V_{DS(AZ)\ 5,\ 6}$	24.2		34	
Shorted load current	V_D < 16 V	$I_{D\ 1\text{-}4\ max}$	50			mA
		$I_{D\ 5,\ 6}$	500			
Leakage current	switches OFF; V_D = 12 V	$I_{D\ 1\text{-}6}$			300	µA
Turn ON delay time	see diagrams	$t_{DON\ 1\text{-}4}$	0.1	1.5	2.5	µs
		$t_{DON\ 5,\ 6}$		6	20	
Turn OFF delay time	see diagrams	$t_{DOFF\ 1\text{-}4}$		1.5	2.5	µs
		$t_{DOFF\ 5,\ 6}$		3	5	
Digital Inputs (IN1-IN6)						
Input HIGH voltage		V_{INH}	1.3	1.8	2.1	V
Input LOW voltage		V_{INL}	0.9	1.2	1.5	V
Hysteresis		V_{INHys}	0.3	0.6	1.0	V
Input current		I_{IN}	– 5		5	µA
Digital Input (IN7)						
Input HIGH voltage		V_{INH}	1.0	1.8	2.1	V
Input LOW voltage		V_{INL}	0.6	1.2	1.5	V
Hysteresis		V_{INHys}	0.3	0.6	1.0	V

Electrical Characteristics (cont'd)

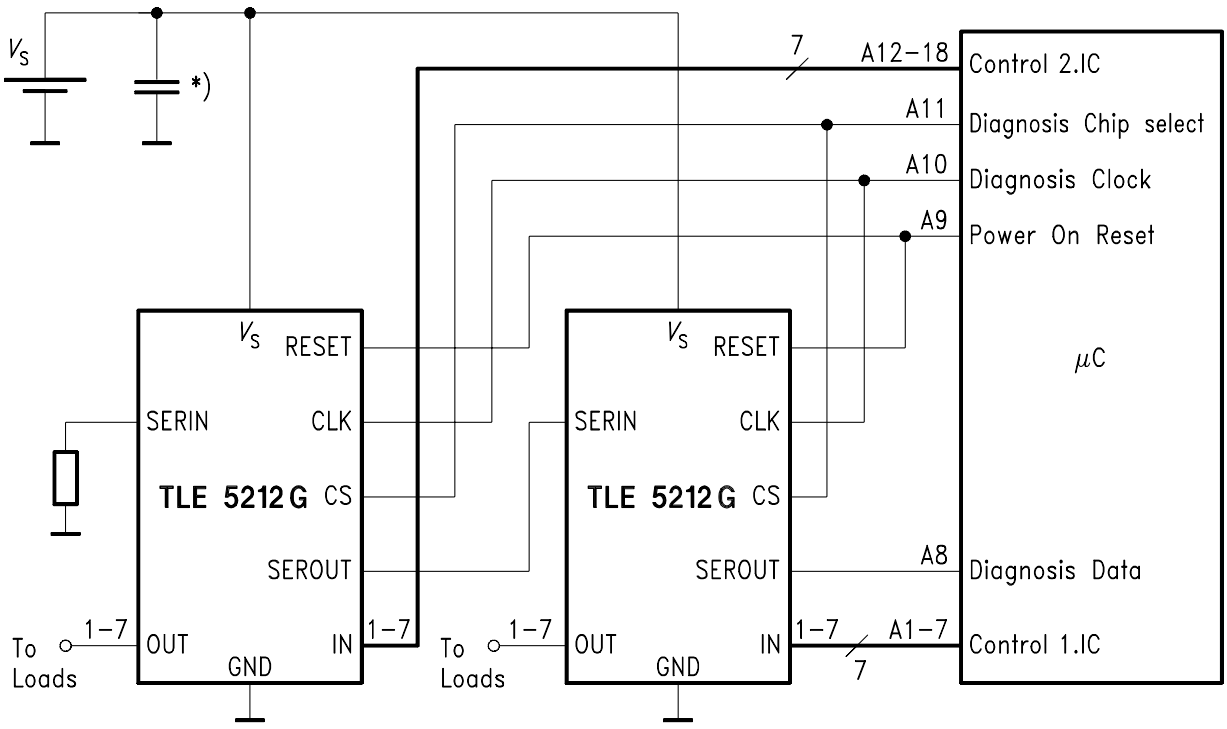
V_S = 6 V to 16 V; T_j = – 40 °C to 140 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Diagnostic Interface Inputs (SERIN, CS, CLK)					
Input HIGH voltage	V_{INH}	3.15			V
Input LOW voltage	V_{INL}			0.9	V
Diagnostic Interface Outputs (SEROUT)					
Output HIGH voltage I_{SERIN} = 0	$V_{SEROUTH}$	3.5		5.4	V
Output LOW voltage I_{SERIN} = 1 mA	$V_{SEROUTL}$			1	V
I_{SERIN} = 0.1 mA	$V_{SEROUTL}$			0.2	
Open load voltage monitoring threshold V_S = 12 V	$V_{DS(OUT)}$	3		9	V
Overload delay time	$t_{d(OV)\ 1\text{-}6}$		10	40	µs
Overtemperature Protection					
Monitoring threshold (no shutdown!); only a design value	T_{thST}		170		°C

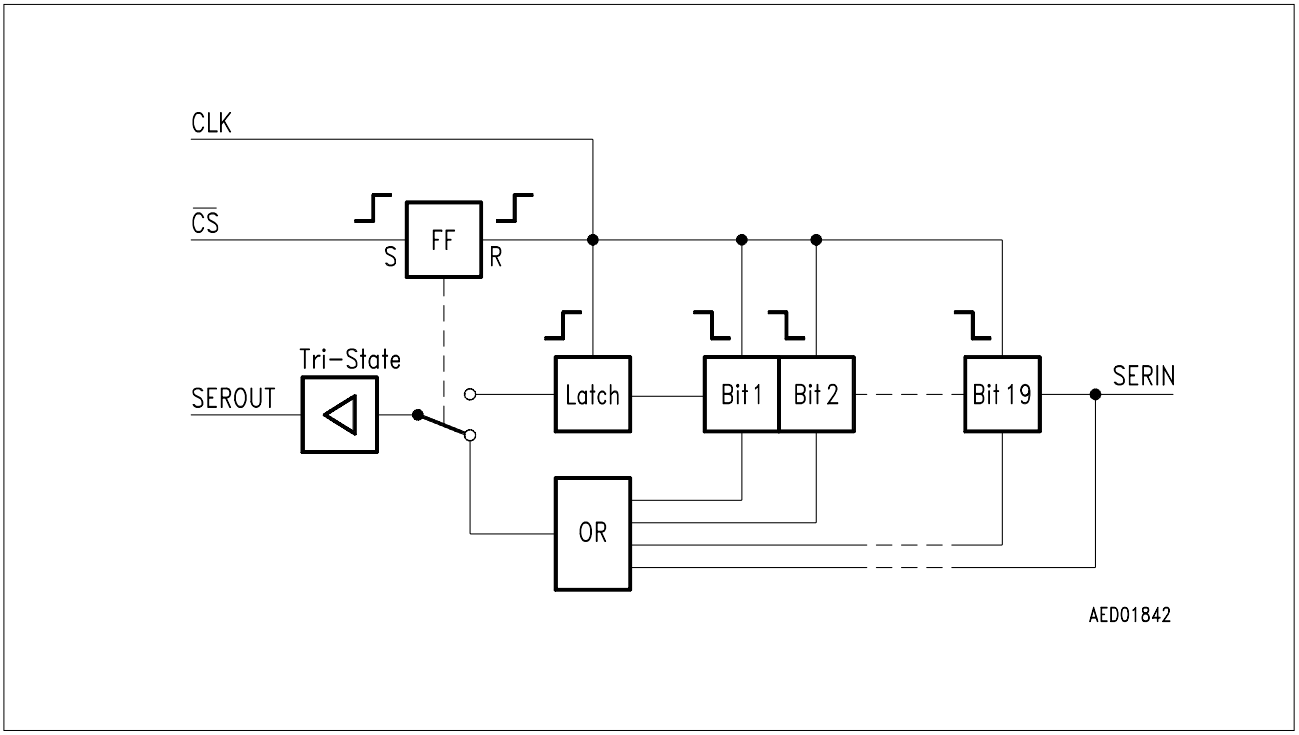
Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.



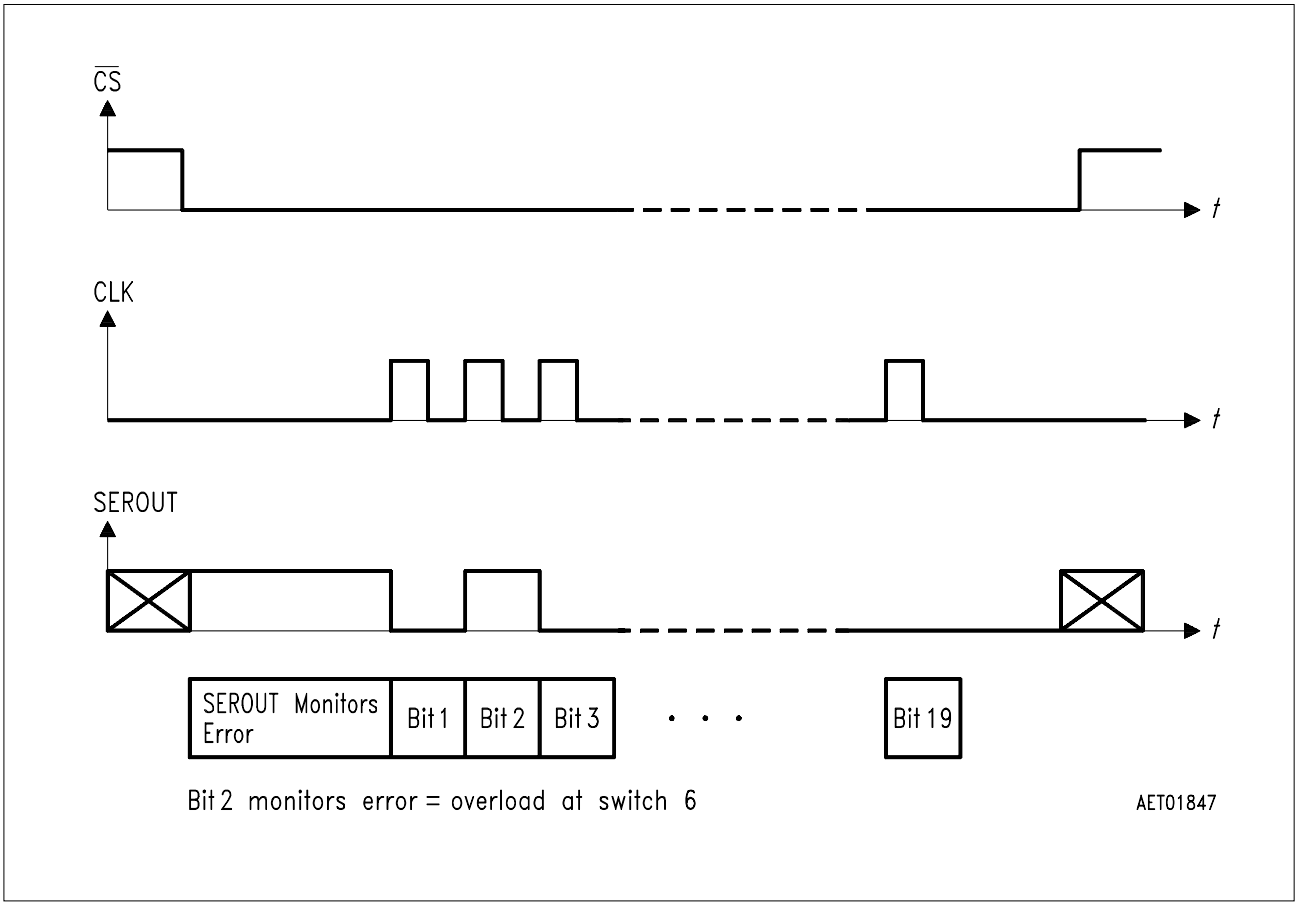
Test Circuit



Application Circuit

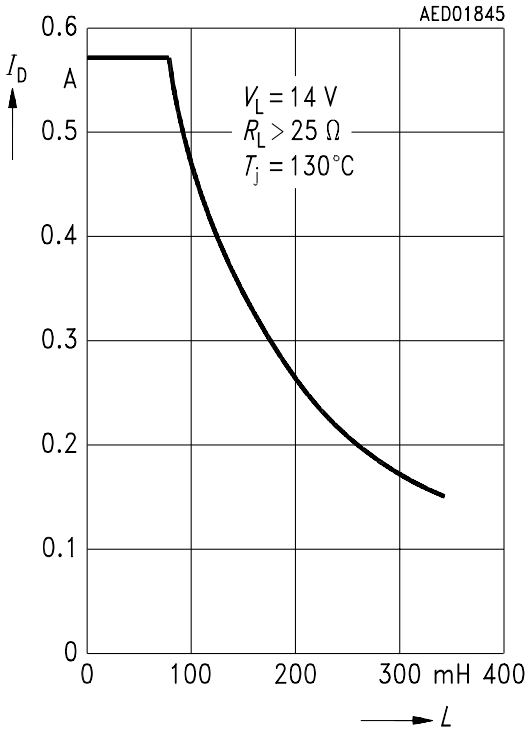


Block Diagram of Serial Diagnostic

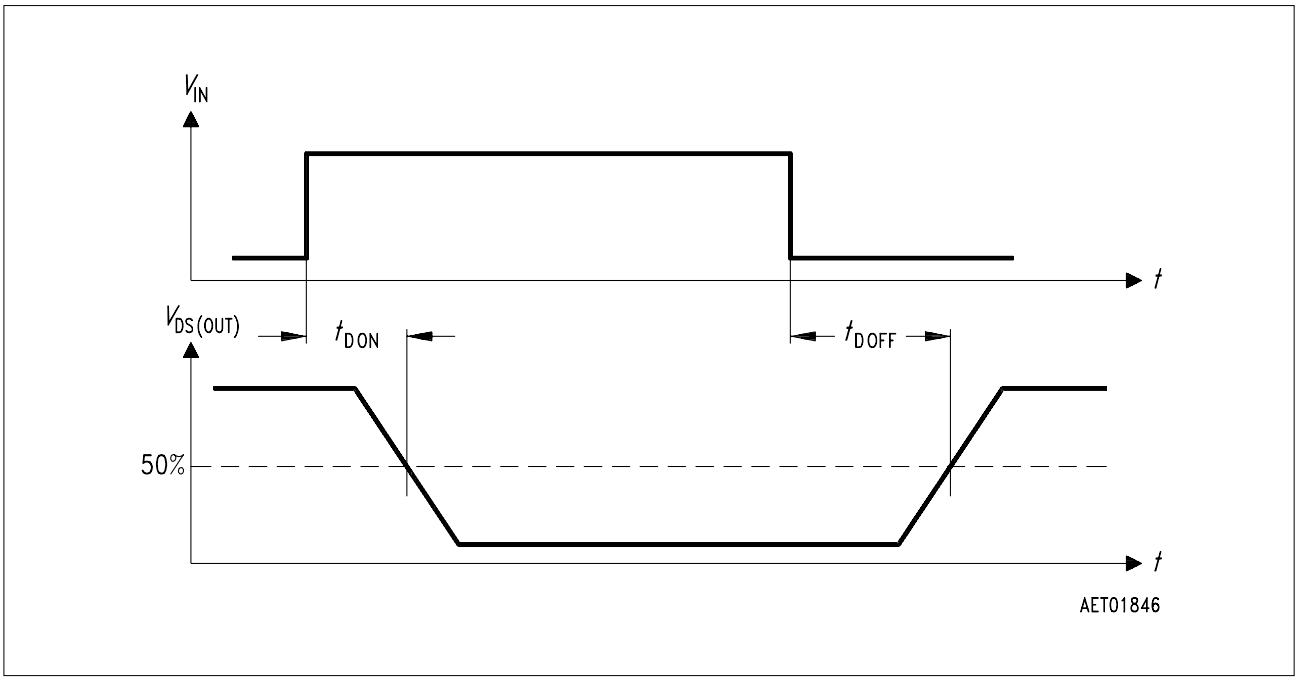


Timing Diagram of Serial Diagnostic Interface

Permissible Load Inductance versus Load Current



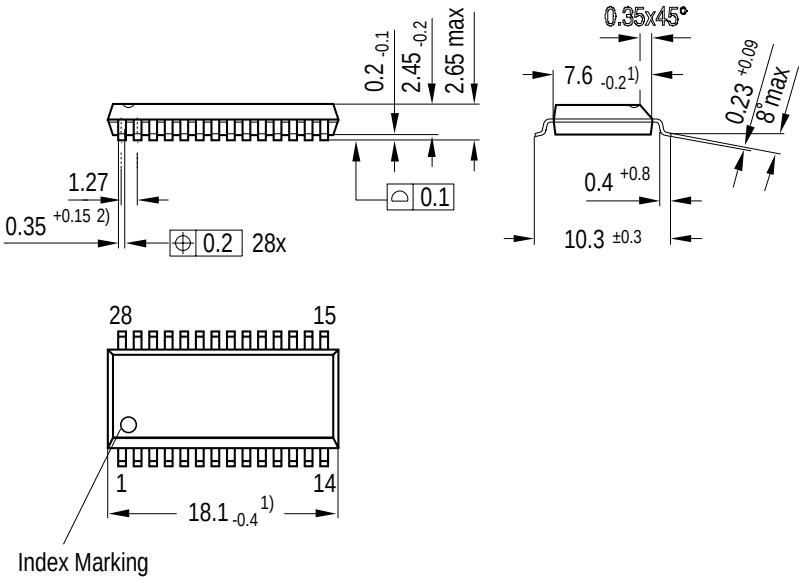
While switching the maximum inductive loads, the maximum temperature T_j of 150 °C may be briefly exceeded. The IC will not be destroyed by this, but the restrictions concerning useful life should be observed.



Timing Diagram

Package Outlines

P-DSO-28-6
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max per side

2) Does not include dambar protrusion of 0.05 max per side

GPD05123

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm