SIEMENS

SAT Mixer-Oscillator-PLL for 3.3 GHz TUA 6110XS

Features

P-SSOP-28-1

- Smallest possible lock-in time; no asynchronous divider stage
- 1-chip system for MPU control (I^2C Bus)
- Fast I^2C Bus mode possible
- 4 programmable chip addresses
- Short pull-in time for quick channel switch-over and optimized loop stability
- 3 high-current switch outputs
- 2 TTL inputs
- 5-level A/D converter
- Lock-in flag
- Power-down flag
- Few external components
- Frequency and amplitude-stable balanced oscillator for the Band A and Band B frequency range
- Optimum decoupling of input frequency from oscillator
- Double balanced mixer with wide dynamic range and low-impedance inputs for the Band A and Band B frequency range
- Internal band switch
- Low-noise reference voltage
- Package P-SSOP-28-1

Type	Ordering Code	Package
▼ TUA 6110XS	Q67000-A5211	P-SSOP-28-1

▼ New type

Application

The IC is suitable for all SAT-Tuners in TV-VCR-Sets and TOPSET-Converters.

Pin Configuration
(top view)

P-SSOP-28-1

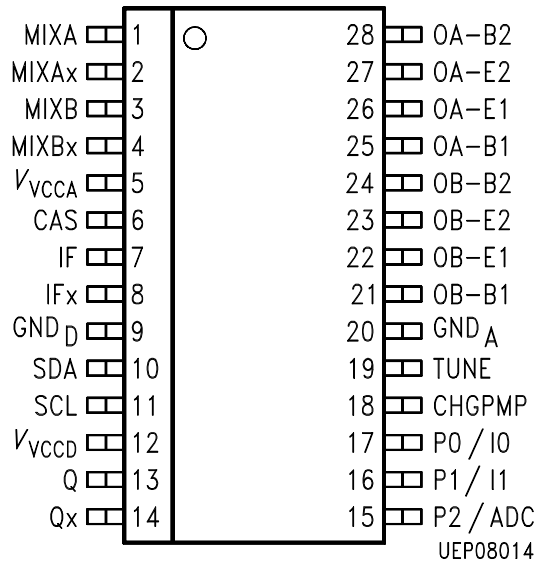


Figure 10

Pin Definitions and Functions

PLL Section

Pin No.	Symbol	Function
6	CAS	Chip address select
9	GND_D	Ground for digital block (PLL)
10	SDA	Data input/output for the I^2C Bus
11	SCL	Clock input for the I^2C Bus
12	V_{VCCD}	Positive supply voltage for digital block (PLL)
13	Q	4 MHz low-impedance crystal oscillator input
14	Qx	4 MHz low-impedance crystal oscillator input
15	P2/ADC	Port output/ADC input
16	P1/I1	Port output/TTL input
17	P0/I0	Port output/TTL input
18	CHGPMP	Charge pump output/loop filter
19	TUNE	Open collector output for pull up resistor/loop filter

Mixer-Oscillator Section

Pin No.	Symbol	Function
1	MIXA	Band A mixer input, low-impedance, symmetrical to MlXAx
2	MlXAx	Band A mixer input, low-impedance, symmetrical to MIXA
3	MIXB	Band B mixer input, low-impedance, symmetrical to MlXBx
4	MlXBx	Band B mixer input, low-impedance, symmetrical to MlXB
5	V_{VCCA}	Positive supply voltage for analog block
7	IF	Open collector mixer output, high-impedance, symmetrical to IF_x
8	IFx	Open collector mixer output, high-impedance, symmetrical to IF
20	GND_A	Ground for analog block
21	OB-B1	Band B oscillator amplifier, high-impedance base input, symmetrical to OB-B2
22	OB-E1	Band B oscillator amplifier, low-impedance emitter output, symmetrical to OB-E2
23	OB-E2	Band B oscillator amplifier, low-impedance emitter output, symmetrical to OB-E1
24	OB-B2	Band B oscillator amplifier, high-impedance base input, symmetrical to OB-B1
25	OA-B1	Band A oscillator amplifier, high-impedance base input, symmetrical to OA-B2
26	OA-E1	Band A oscillator amplifier, low-impedance emitter output, symmetrical to OA-E2
27	OA-E2	Band A oscillator amplifier, low-impedance emitter output, symmetrical to OA-E1
28	OA-B2	Band A oscillator amplifier, high-impedance base input, symmetrical to OA-B1

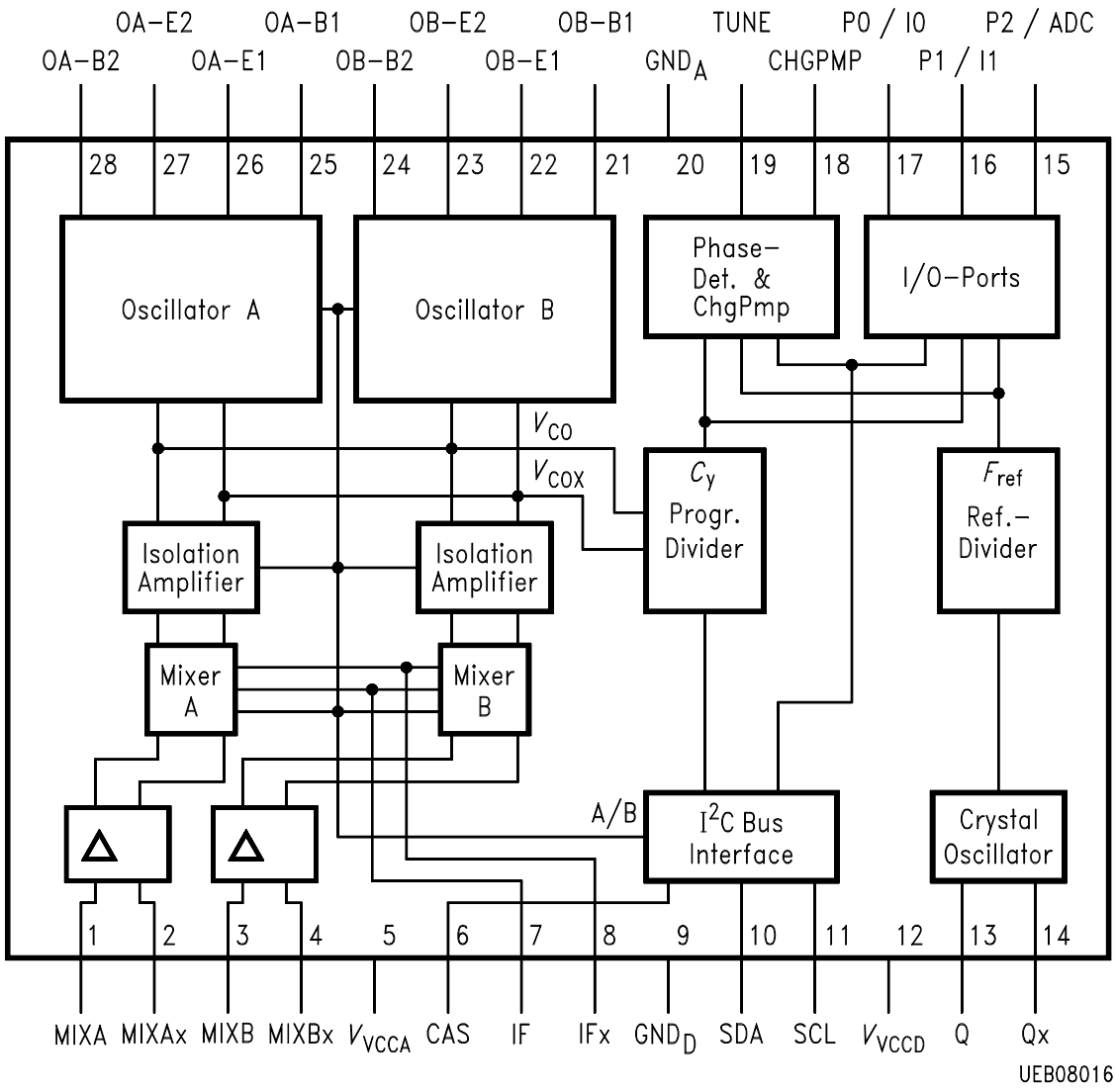


Figure 11
Block Diagram

Functional Description

The **TUA 6110X** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in SAT tuners. The PLL block with four hard-switched chip addresses, forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the sattuner oscillator up to 3.3 GHz in increments of 125 kHz. The tuning process is controlled by a microprocessor via an I^2C Bus. The device has three output ports, which all can also be used as input ports (two TTL inputs and one A/D converter input). A flag is set when the loop is locked. The input ports and lock flag can be read by the processor via the I^2C Bus. The mixer-oscillator block includes two balanced mixers (double balanced mixer with low-impedance input), two frequency and amplitude-stable balanced oscillators for Band A and Band B, a low-noise reference voltage source and a band switch.

Circuit Description

General Description

Mixer-Oscillator Block

The mixer-oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for Band A and Band B, a reference voltage source and a band switch.

The band switch ensures that only one mixer-oscillator block at a time is activated. In the activated band the signal passes a frontend stage with MESFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has a low-impedance input.

The input signal is mixed there with the on chip oscillator signal from the activated oscillator section.

PLL Block

The mixer-oscillator signal VCO/VCOx is internally DC-coupled as a differential signal at the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/phase detector to a reference frequency f_{REF} = 125 kHz. This frequency is derived from a balanced, low-impedance 4 MHz crystal oscillator (pin Q, Qx) divided by Q = 32.

The phase detector has two outputs UP and DOWN that drive two current sources I+ and I– of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the I+ current source pulses for the duration of the phase difference. In the reverse case the I– current source pulses. If the two signals are in phase, the charge pump output (CHGPMP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pullup resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state when the control bit T0 = 1. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuity. TUNE may be switched off by the control bit OS to allow external adjustments.

By means of a control bit 5I the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports P0, P1, and P2 are general-purpose open-collector outputs. The test bit T1 = 1, switches the test signals f_{REF} (4 MHz/32) and Cy (divided input signal) to P0 and P1 respectively. P0, P1, and P2 are bidirectional: P0 and P1 are TTL inputs; P2 is an A/D converter input.

Data are exchanged between the processor and the PLL via the I²C Bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I²C Bus.

The data from the processor pass through an I²C Bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The **table 3** ‘Bit Allocation’ should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The eighth bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the first bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type or a stop condition has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of two bits from the TTL input ports, three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate connection of pin CAU (see **table 4** ‘Address Selection’).

When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when V_{VCCD} goes below 3.2 V. It will be reset at the end of a READ operation.

The lock detector resets the lock flag FL when the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, when FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P(K_{vco} / f_Q) (C_1 + C_2) / (C_1 C_2)$$

where I_p is the charge pump current, K_{VCO} the VCO gain, f_Q the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see **Application Circuit**). As the charge pump pulses at 125 kHz (= f_{REF}), it takes a maximum of 8 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore, it takes between 64 and 72 µs for FL to be set after the loop regains lock.

Table 3
Bit Allocation Read/Write Data

	MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB	Ack
Write Data									
Address Byte	1	1	0	0	0	MA1	MA0	0	Ack
Prog. Divider Byte1	0	n14	n13	n12	n11	n10	n9	n8	Ack
Prog. Divider Byte 2	n7	n6	n5	n4	n3	n2	n1	n0	Ack
Control Byte1	1	5I	T1	T0	1	1	1	OS	Ack
Control Byte 2	A/B	x	x	x	x	P2	P1	P0	Ack
Read Data									
Address Byte	1	1	0	0	0	MA1	MA0	1	Ack
Status Byte	POR	FL	x	I1	I0	A2	A1	A0	Ack

Note: MSB is shifted first.

Divider Ratio

N = 16384 × n14 + 8192 × n13 + 4096 × n12 + 2048 × n11 + 1024 × n10 + 512 × n9 + 256 × n8 + 128 × n7 + 64 × n6 + 32 × n5 + 16 × n4 + 8 × n3 + 4 × n2 + 2 × n1 + n0

Ports P0, P1, P2

1 Open-collector output is active
0 Open-collector output is inactive, TTL-inputs I1, I0 and ADC available

Bandswitch A/B

High switch to OSC/MIX B

Pump Current 5I

High switch to high current

Disabling Tuning Voltage OS

High disables TUNE

Power On Reset flag POR:flag is set at power-on and reset at the end of a READ operation
PLL lock flag FL: flag is set when loop is locked
TTL-inputs I1, I0: input data from pins P1/I1, P0/I0

Table 4
Address Selection

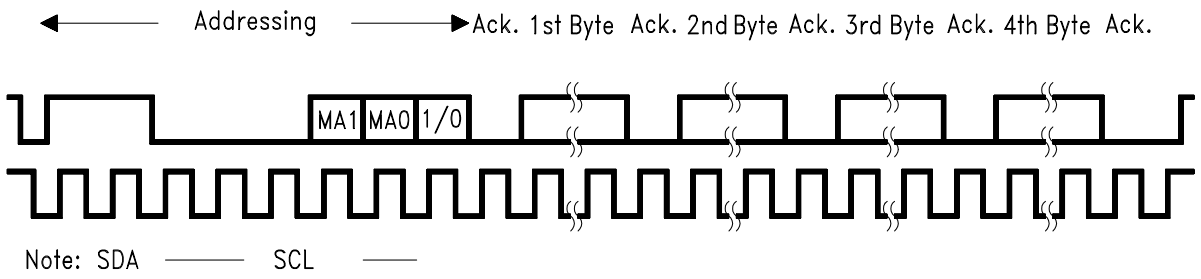
Voltage at CAS	M1	M0
(0 … 0.1) × V_{VCCD}	0	0
Open circuit	0	1
(0.4 … 0.6) × V_{VCCD}	1	0
(0.9 … 1) × V_{VCCD}	1	1

Table 5
Test Modes

Test Mode	T1	T0
Normal operation	0	0
P1 = Cy output, P0 = f_{REF} output	1	0
Charge pump output CHGPMP is in high-impedance state	0	1
TTL-inputs I1/I0 are Cy/f_{REF} inputs of phase detector	1	1

Table 6
A/D Converter Levels

Voltage at P2/ADC	A2	A1	A0
(0 … 0.15) × V_{VCCD}	0	0	0
(0.15 … 0.3) × V_{VCCD}	0	0	1
(0.3 … 0.45) × V_{VCCD}	0	1	0
(0.45 … 0.6) × V_{VCCD}	0	1	1
(0.6 … 1) × V_{VCCD}	1	0	0



Telegram examples:

Start–Addr–DR1–DR2–CW1–CW2–Stop
Start–Addr–CW1–CW2–DR1–DR2–Stop
Start–Addr–DR1–DR2–CW1–Stop
Start–Addr–CW1–CW2–DR1–Stop
Start–Addr–DR1–DR2–Stop
Start–Addr–CW1–CW2–Stop
Start–Addr–DR1–Stop
Start–Addr–CW1–Stop

Start = Start Condition
Addr = Address
DR1 = Divider Ratio 1st Byte
DR2 = Divider Ratio 2nd Byte
CW1 = Control Word 1st Byte
CW2 = Control Word 2nd Byte
Stop = Stop Condition

UED08015

Figure 12
Circuit Description

Absolute Maximum Ratings

T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
PLL					
Supply voltage	V_{VCCD}	– 0.3	+ 6	V	
Current	I_{VCCD}		40	mA	
Output CHGPMP	V_{CHGPMP}	– 0.3	+ 3.5	V	
Crystal oscillator pins Q, Qx	V_Q	– 0.3	V_{VCCD}	V	
Bus input/output SDA	V_{SDA}	– 0.3	+ 6	V	
Bus input SCL	V_{SCL}	– 0.3	+ 6	V	
Port outputs P0, P1, P2	V_P	– 0.3	+ 13	V	
Chip address switch CAU	V_{CAU}	– 0.3	V_{VCCD}	V	
Output active filter TUNE	V_{TUNE}	– 0.3	+ 33	V	
Bus output SDA	I_{SDAL}	– 1	5	mA	open collector
Port outputs P0, P1, P2	I_{PL}	– 1	15	mA	open collector
Total port output current	ΣI_{PL}		20	mA	
Junction temperature	T_j		+ 125	°C	
Storage temperature	T_S	– 40	+ 125	°C	
Thermal resistance (junction to ambient)	R_{thA}		75	K/W	
Mixer-Oscillator					
Supply voltage	V_{VCCA}	– 0.3	+ 6	V	
Current	I_{VCCA}		40	mA	
Output IF, IFX	I_{IF}, I_{IFX}		9	mA	open collector

Operating Range

Parameter	Symbol	Limit Values		Units	Remarks
		min.	max.		
Supply voltage	V_{VCCD}	+ 4.5	+ 5.5	V	
Supply voltage	V_{VCCA}	+ 4.5	+ 5.5	V	

Operating Range

Parameter	Symbol	Limit Values		Units	Remarks
		min.	max.		
Supply current	I_{VCCD}	18	35	mA	
Supply current	I_{VCCA}	18	35	mA	
Mixer output voltage	V_{IF}, I_{FX}	+ 4.5	+ 5.5	V	open collector
Mixer output current	I_{IF}, I_{FX}	4.0	8.0	mA	open collector
Programmable divider factor	N	256	32767		
Band A Mixer input frequency range	f_{MA}	900	2050	MHz	
Band B Mixer input frequency range	f_{MB}	1700	2550	MHz	
Band A Oscillator frequency range	f_{OA}	1350	2300	MHz	
Band B Oscillator frequency range	f_{OB}	2250	3000	MHz	
Ambient temperature	T_A	– 20	+ 80	°C	

AC/DC Characteristics

V_{VCCD} = 4.5 V to 5.5 V; T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
PLL						
Supply current	I_{VCCD}	21	26	31	mA	V_{VCCD} = 5 V

Crystal Oscillator Connections Q, QX

Crystal frequency	f_Q	3.2	4.0	4.8	MHz	series resonance
Crystal resistance[1)]	R_Q	10		100	Ω	series resonance
Oscillation frequency	f_Q	3.99975	4.000	4.00025	MHz	f_Q = 4 MHz
Drive current[1)]	I_Q	tbd	tbd	tbd	µArms	f_Q = 4 MHz
Input impedance	Z_Q	– 600	– 750	– 900	Ω	f_Q = 4 MHz
Margin from 1st (fundamental) to 2nd and 3rd harmonics[1)]	a_H			20	dB	f_Q = 4 MHz

Notes see **page 141**.

AC/DC Characteristics (cont'd)
V_{VCCD} = 4.5 V to 5.5 V; T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Charge Pump Output CHGPMP (V_{VCCD} = 5 V)						
HIGH output current	I_{CPH}	± 90	± 220	± 300	µA	5I = 1, V_{CP} = 2 V
LOW output current	I_{CPL}	± 22	± 50	± 75	µA	5I = 0, V_{CP} = 2 V
Tristate current	I_{CPZ}		+ 1		nA	T0 = 1, V_{CP} = 2 V
Output voltage	V_{CP}	1.0		2.5	V	locked
Drive Output TUNE (open collector)						
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V, T0 = 1
LOW output voltage	V_{TL}			0.5	V	I_{TL} = 1.5 mA
Port Outputs P0, P1, P2 (open collector)						
HIGH output current	I_{POH}			10	µA	V_{POH} = 13.5 V
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 15 mA
TTL Port Inputs P0, P1						
HIGH input voltage	V_{PIH}	2.7			V	
LOW input voltage	V_{PIL}			0.8	V	
HIGH input current	I_{PIH}			10	µA	V_{PIH} = 13.5 V
LOW input current	I_{PIL}		– 10		µA	V_{PIL} = 0 V
ADC Port Input P2						
HIGH input current	I_{ADCH}			10	µA	
LOW input current	I_{ADCL}	– 10			µA	

AC/DC Characteristics (cont'd)
V_{VCCD} = 4.5 V to 5.5 V; T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Address Selection Input CAS						
HIGH input current	I_{CASH}			50	µA	V_{CASH} = 5 V
LOW input current	I_{CASL}	– 50			µA	V_{CASL} = 0 V
I²C Bus						
Bus inputs SCL, SDA						
HIGH input voltage	V_{IH}	3		5.5	V	
LOW input voltage	V_{IL}			1.5	V	
HIGH input current	I_{IH}			10	µA	$V_{IH} = V_S$
LOW input current	I_{IL}	– 20			µA	V_{IL} = 0 V
Bus Output SDA (open collector)						
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA
Edge Speed SCL, SDA						
Rise time	t_r			300	ns	
Fall time	t_f			300	ns	
Clock Timing SCL						
Frequency	f_{SCL}	0		400	kHz	
HIGH pulse width	t_H	0.6			µs	
LOW pulse width	t_L	1.3			µs	

AC/DC Characteristics (cont'd)
V_{VCCD} = 4.5 V to 5.5 V; T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Start Condition						
Set-up time	t_{susta}	0.6			µs	
Hold time	t_{hsta}	0.6			µs	
Stop Condition						
Set-up time	t_{susto}	0.6			µs	
Bus free	t_{buf}	1.3			µs	
Data Transfer						
Set-up time	t_{sudat}	0.1			µs	
Hold time	t_{hdat}	0			µs	
Input hysteresis SCL, SDA[1)]	V_{hys}		200		mV	
Noise immunity SCL, SDA[1), 2)]	V_N		5		Vpp	f_N = 1 MHz … 14 MHz
Capacitive load for each bus line	C_L			400	pF	
Mixer-Oscillator						
Current consumption	I_{VCCA}	21	26	32	mA	Bit A/B = L
	I_{VCCB}	21	26	32	mA	Bit A/B = H
Mixer output impedance	$R_{IF, IFX}$		11		kΩ	Parallel equivalent circuit
	$C_{IF, IFx}$		0.5		pF	Parallel equivalent circuit

1) Design note: no 100 % final inspection.
2) Sinusoidal noise signal applied via 33 pF coupling capacitor.

AC/DC Characteristics (cont'd)
V_{VCCD} = 4.5 V to 5.5 V; T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Band A Circuit Section						
Oscillator frequency range	f_{OscA}	1350		2550	MHz	V_d = 0 … 28 V
Oscillator drift	Δf_{OscA}			2	MHz	V_S = 5 V ± 10 %
	Δf_{OscA}			2	MHz	ΔT = 25 °C
	Δf_{OscA}			5	MHz	t = 5 s up to 15 min. after switching on
Oscillator pulling	V_{MIXA}				dBµV	Δf = tbd
	V_{MIXA}				dBµV	Δf = tbd
	V_{MIXA}				dBµV	Δf_{int} = tbd
	V_{MIXA}				dBµV	Δf_{int} = tbd
Mixer gain	G_{MixA}	3	6	9	dB	
Mixer noise figure	F_{MixA}		9		dB	f_e = 950 MHz (DSB)
	F_{MixA}		15		dB	f_e = 2.1 GHz (DSB)
Mixer input impedance	R_{MixA}		25		Ω	serial equivalent circuit
	L_{MixA}		10		nH	serial equivalent circuit
IF suppression	a_{IF}		20		dB	V_{MixB} = 80 dBµV

AC/DC Characteristics (cont'd)
V_{VCCD} = 4.5 V to 5.5 V; T_A = – 20 °C to 80 °C

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Band B Circuit Section						
Oscillator frequency range	Δf_{OscB}	2.25		3.0	GHz	V_t = 0 … 28 V
Oscillator drift	Δf_{OscB}			1	MHz	V_S = 5 V ± 10 %
	Δf_{OscB}			1	MHz	ΔT = 25 °C
	Δf_{OscB}			2	MHz	t = 5 s up to 15 min. after switching on
Oscillator pulling	V_{MIXB}				BµV	Δf = tbd
	V_{MIXB}				BµV	Δf = tbd
	V_{MIXB}				dBµV	Δf_{int} = tbd
	V_{MIXB}				dBµV	Δf_{int} = tbd
Mixer gain	G_{MixB}		3		dB	
Mixer noise figure	F_{MixB}		15		dB	f_e = 2.0 GHz (DSB)
			18		dB	f_e = 2.5 GHz (DSB)
Mixer input impedance	R_{MixB}		35		Ω	serial equivalent circuit
	L_{MixB}		10		nH	serial equivalent circuit
IF suppression	a_{IF}		20		dB	V_{MixB} = 80 dBµV

Test Circuit 1

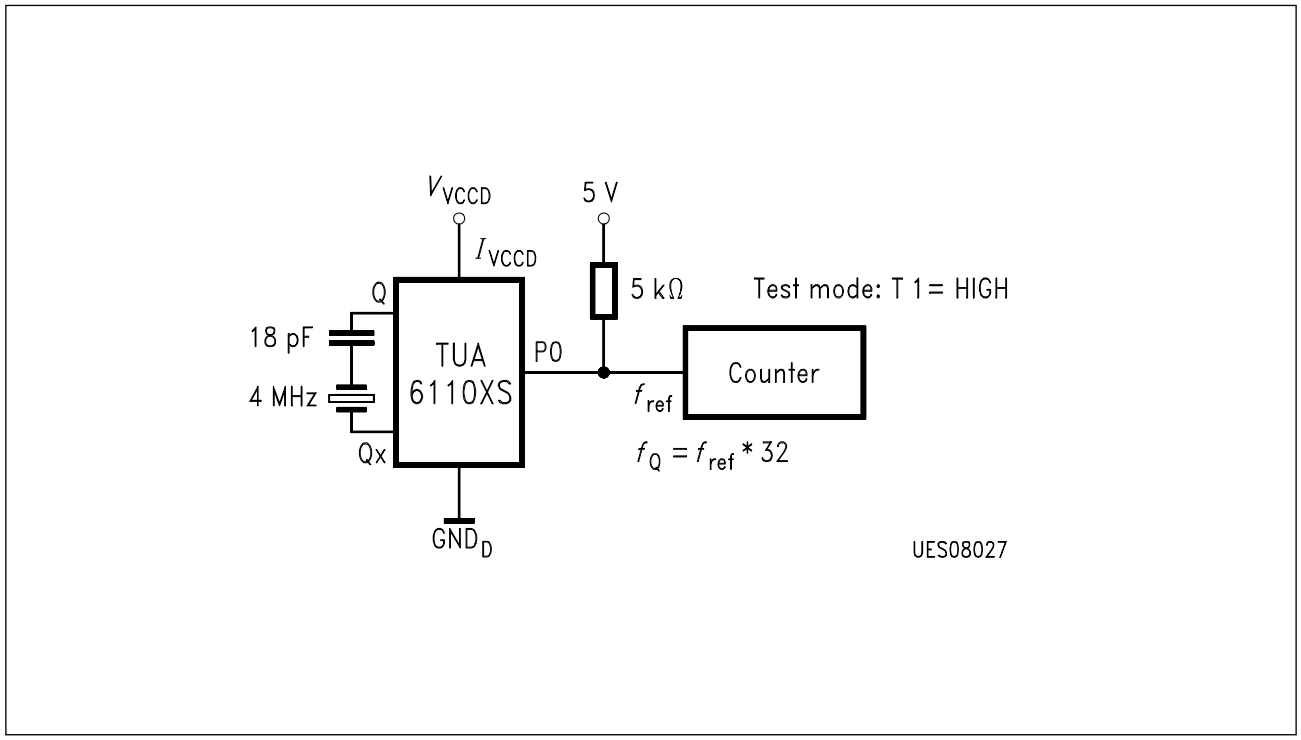


Figure 13
Measurement of Crystal Oscillator Frequency

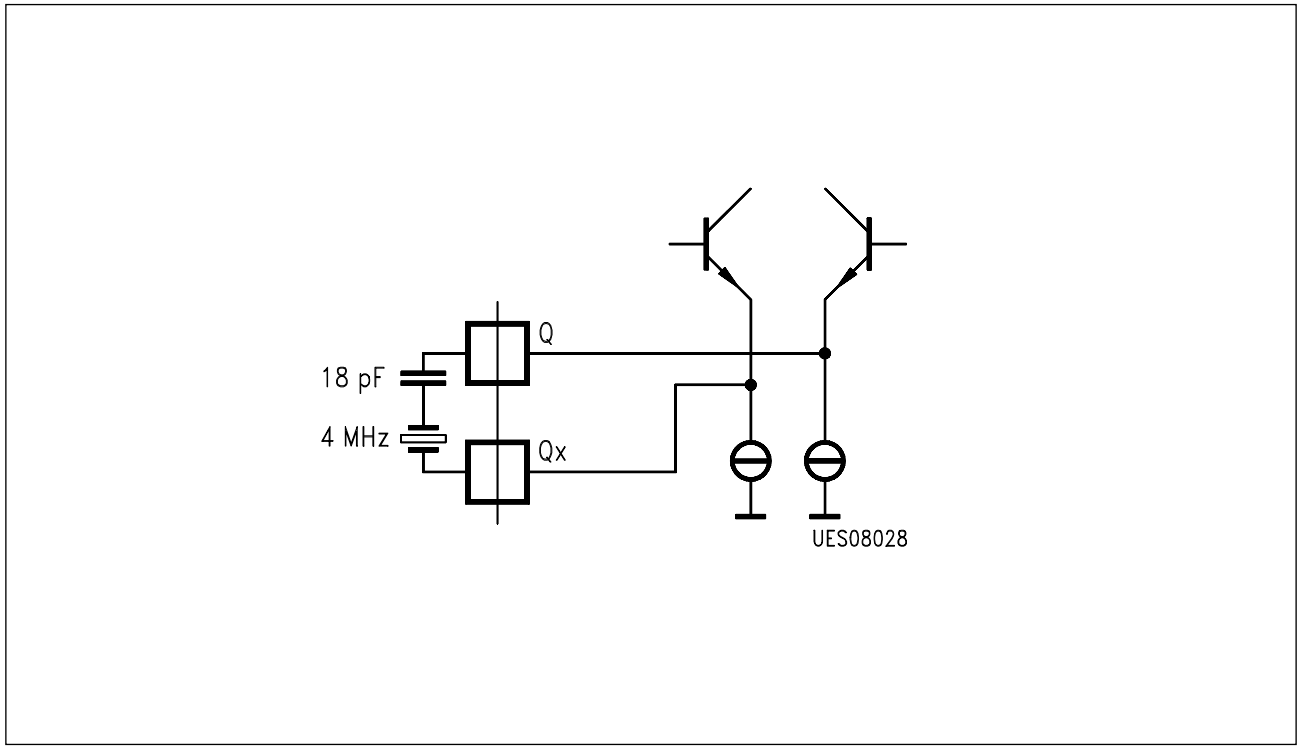


Figure 14
Equivalent I/O-Schematic

Test Circuit 2

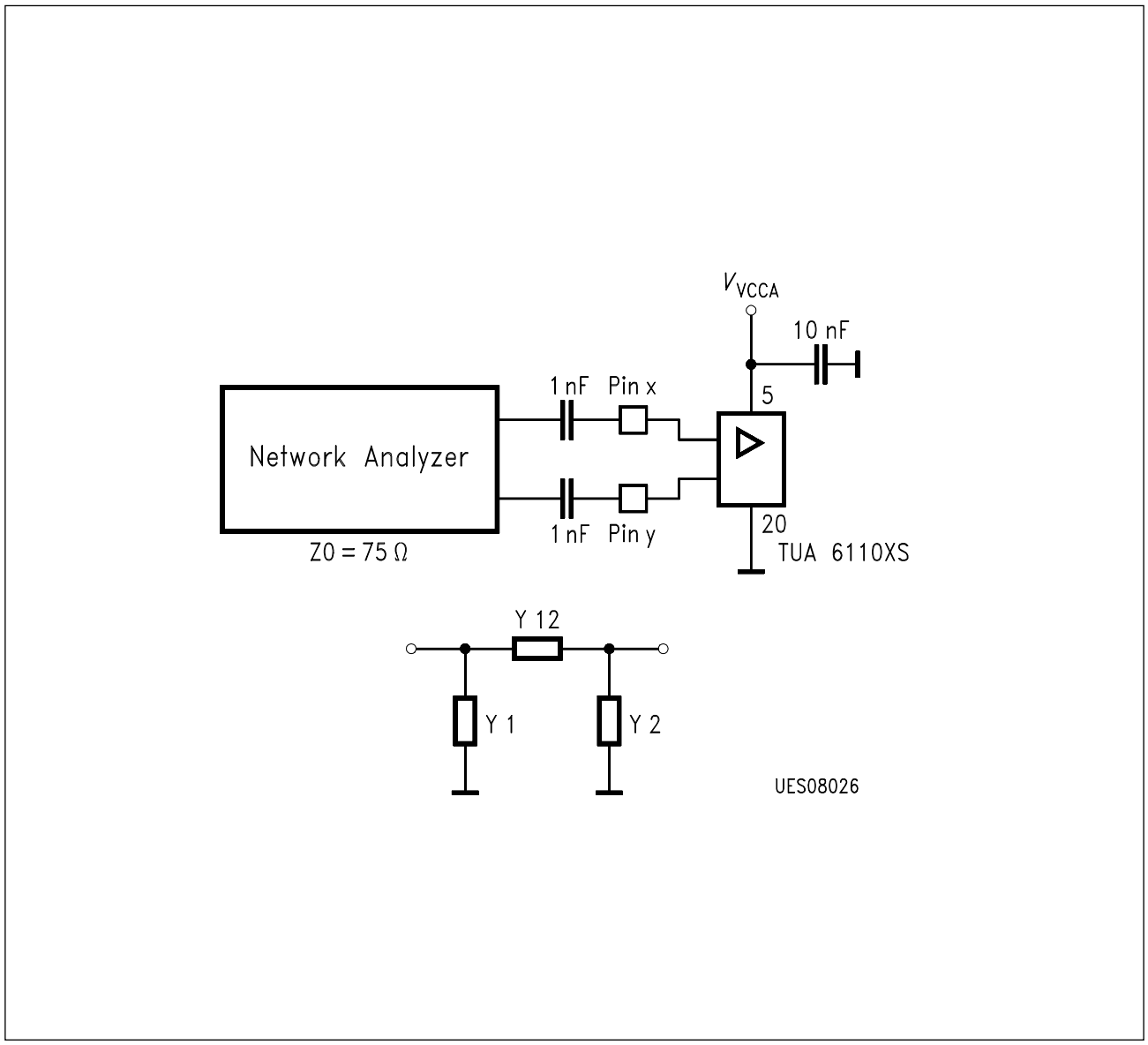


Figure 15
Measurement of S-Parameter S11, S12, S21, S22 and Calculation of π-Equivalent Circuit

Table 7
Test Frequency

Test Point	Test Frequency in MHz	Pin x	Pin y
Mixer input impedance A	950	1	2
Mixer input impedance B	2000	3	4

Test Circuit 3

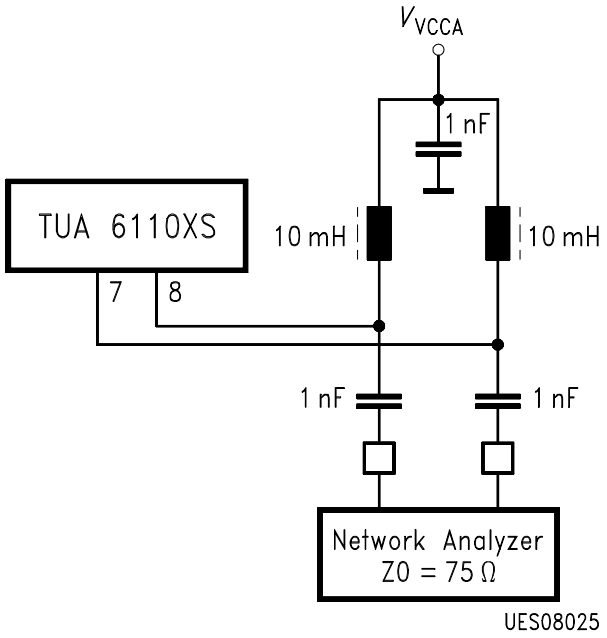


Figure 16
Measurement of Output Capacitance by Measurement of S-Parameters S11, S12, S21, S22 at 480 MHz

Test Circuit 4

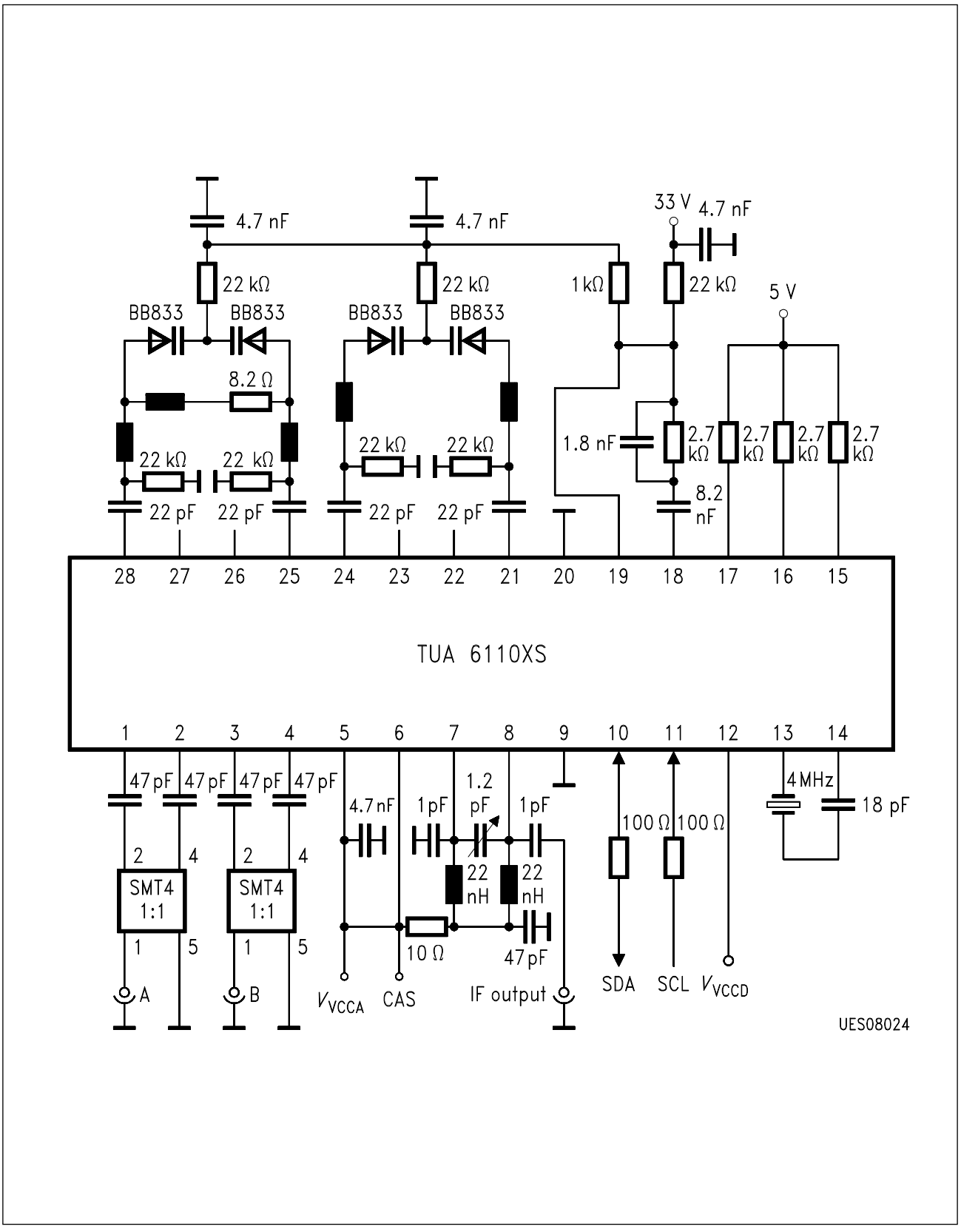


Figure 17

Equivalent I/O-Schematic

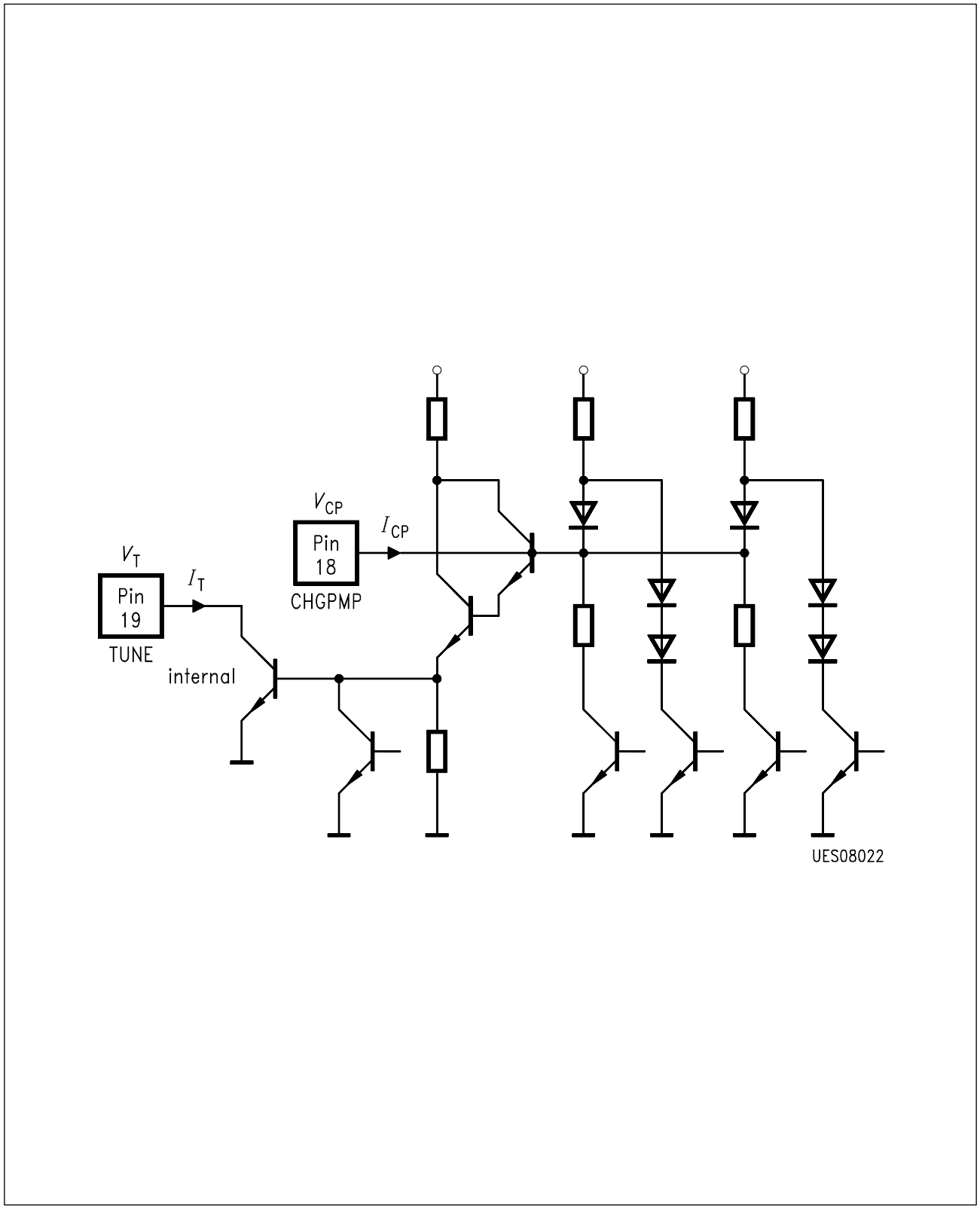


Figure 18
Equivalent I/O-Schematic of Charge Pump

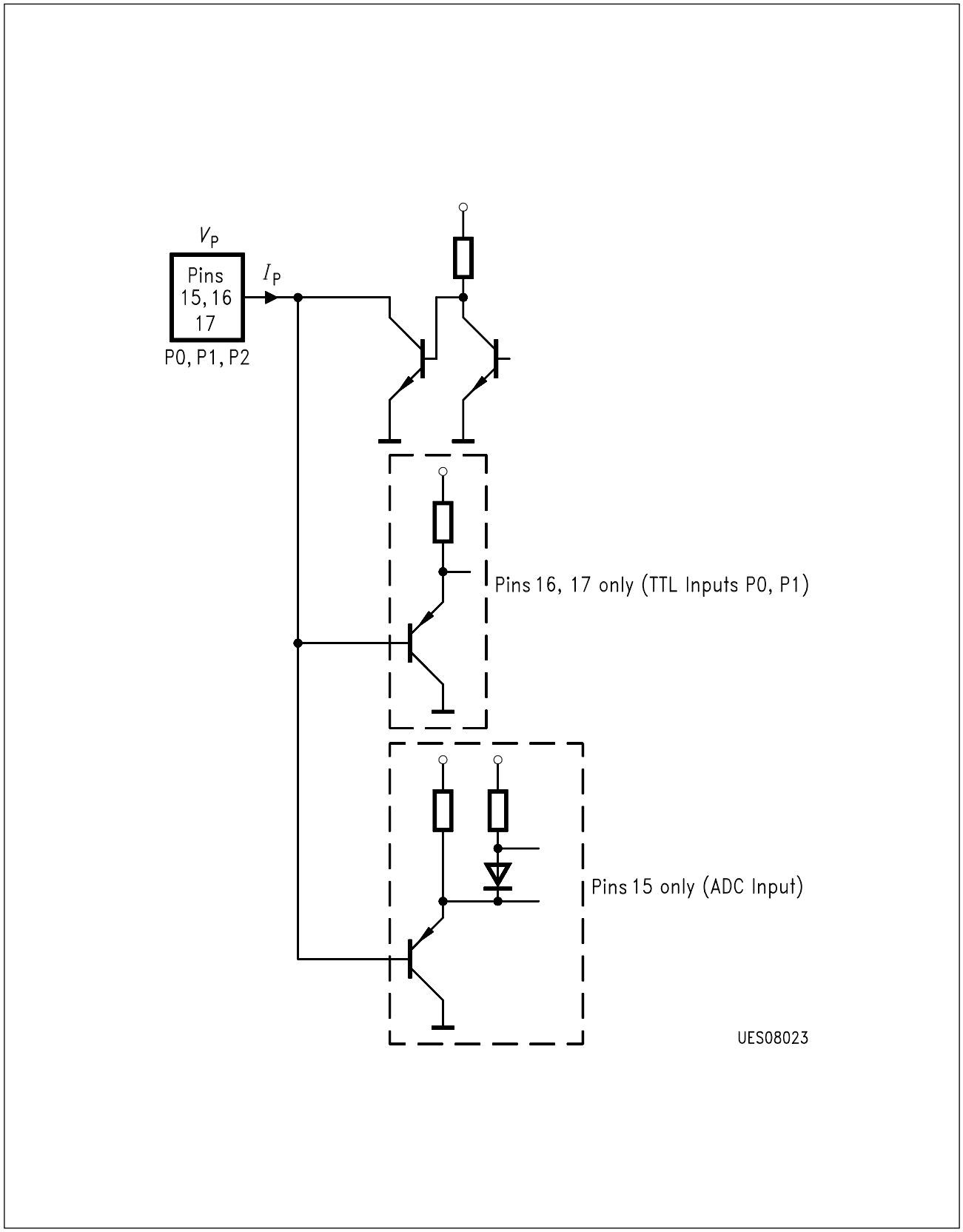


Figure 19
Equivalent I/O-Schematic of Port Pins

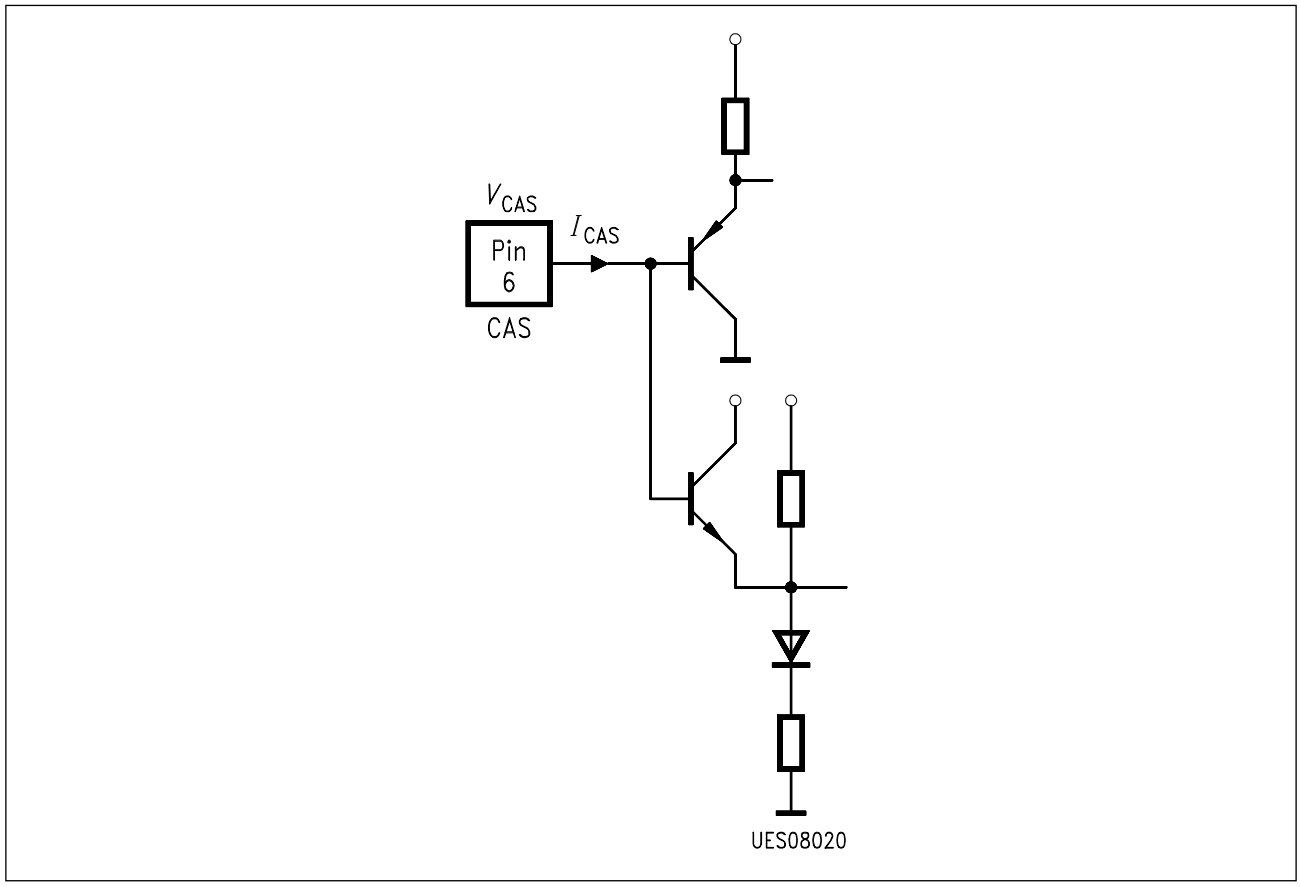


Figure 20
Equivalent I/O-Schematic of CAS Pin

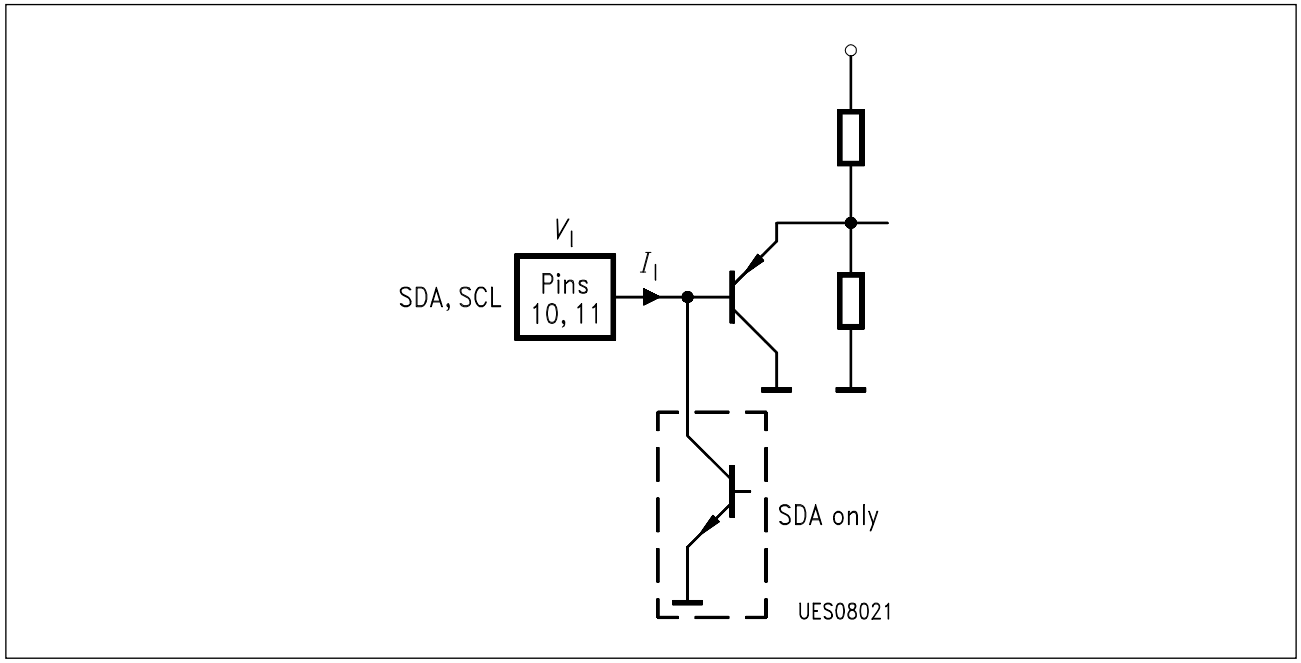


Figure 21
Equivalent I/O-Schematic of SDA/SCL Pins

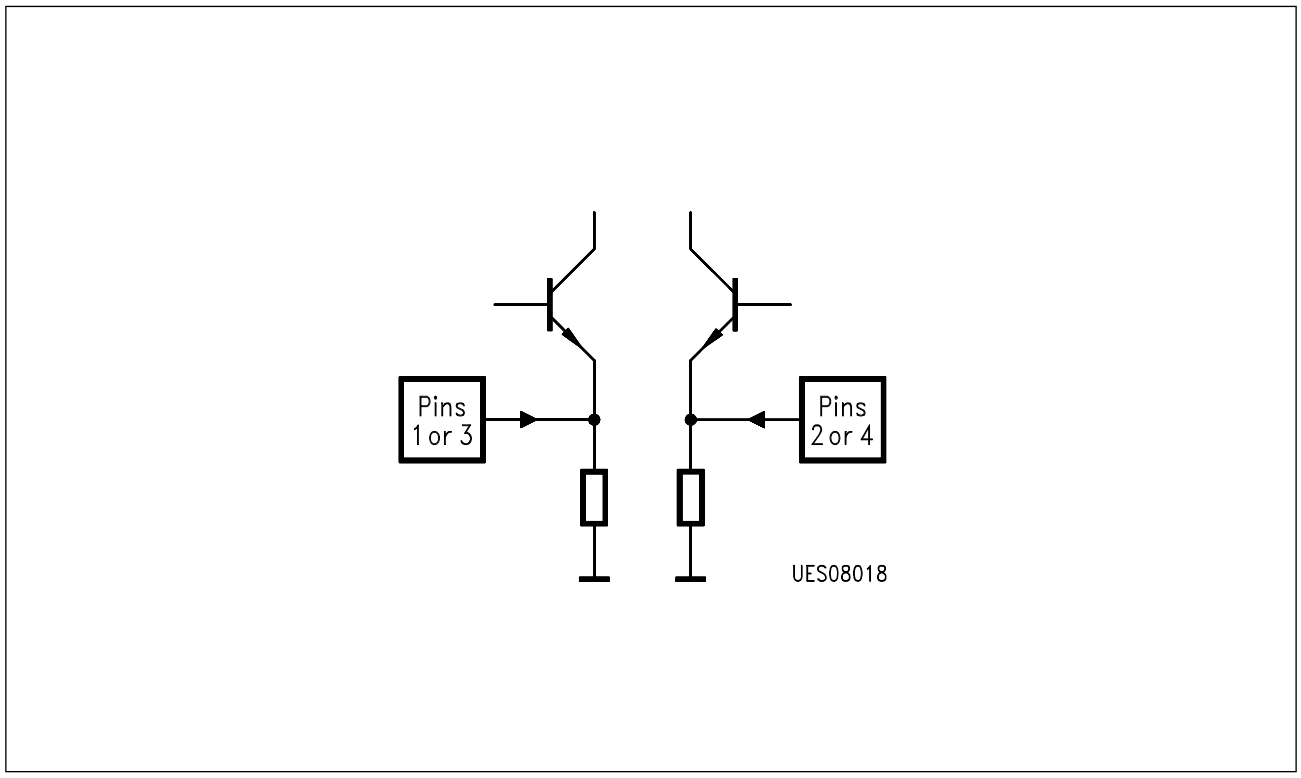


Figure 22
Equivalent I/O-Schematic of MIXA / MIXAX / MIXB / MIXBX Pins

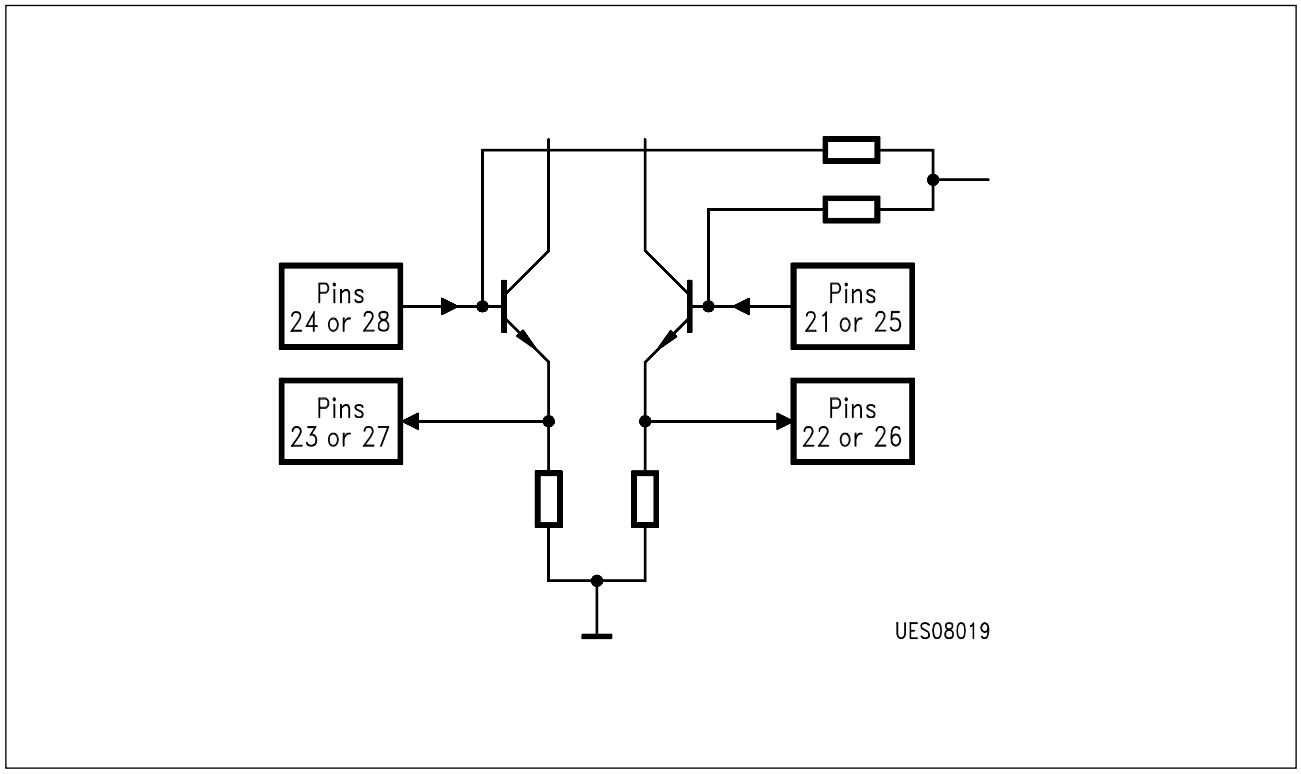
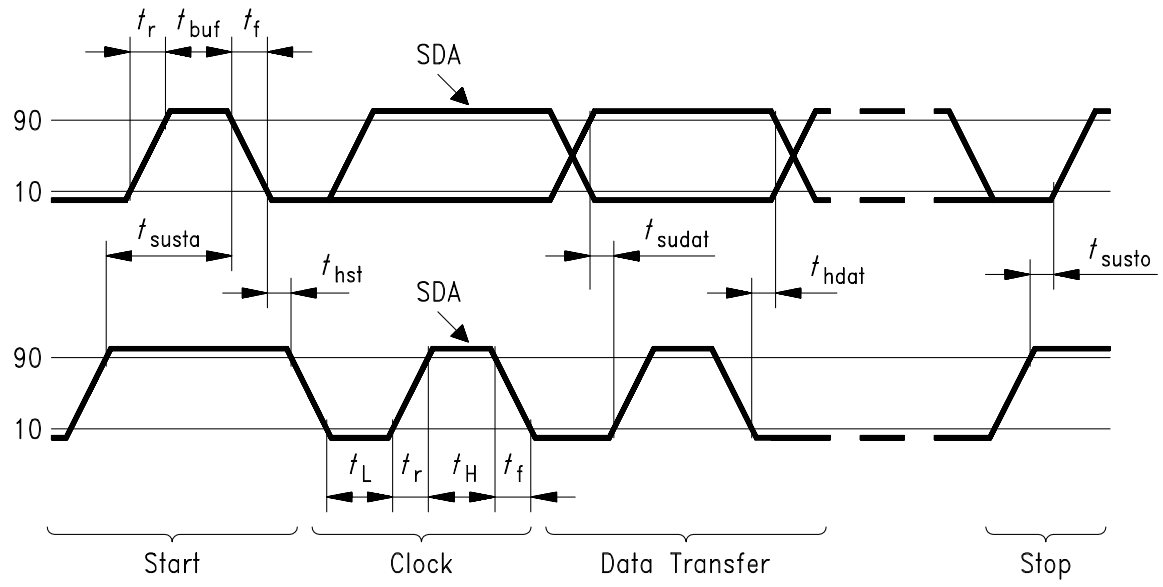


Figure 23
Equivalent I/O-Schematic of Oscillator Pins



t_{buf}	bus free time
t_r	data/clock rise time
t_f	data/clock fall time
t_{susta}	start set–up time
t_{hsta}	start hold time
t_L	LOW clock pulse width
t_H	HIGH clock pulse width
t_{sudat}	data transfer set–up time
t_{hdat}	data transfer hold time
t_{susto}	stop set–up time

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Figure 24
I²C Bus Timing