

**DG5143****Vishay Siliconix**

Low-Power, High-Speed CMOS Analog Switch

FEATURES

- $\pm 15\text{-V}$ Input Range
- On-Resistance: $50\ \Omega$
- Fast Switching Action— t_{ON} : $100\ \text{ns}$
- Low Power— P_D : $<350\ \mu\text{W}$
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Low Signal Errors
- Break-Before-Make Switching Action
- Reduced Power Consumption
- Simple Interfacing

APPLICATIONS

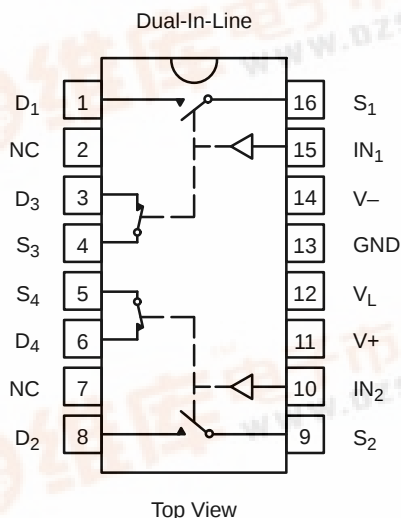
- Audio Switching
- Precision Switching
- High-Speed Switching
- Battery Powered Systems

DESCRIPTION

The DG5143 solid state analog switch is built on the Vishay Siliconix proprietary high-voltage silicon gate process to achieve high voltage rating and superior switch time on/off performance. Break-before-make switching action guarantees that an on-channel will be turned off before the off-channel can turn on. The DG5143 features ultra-low power supply requirements and TTL and CMOS compatibility.

Each switch conducts equally well in both directions when on and blocks input voltages to the supply values when off. This switch is ideal for battery powered industrial applications with a maximum power supply current of $1\ \mu\text{A}$. An epitaxial layer prevents latchup.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	SW ₁ , SW ₂	SW ₃ , SW ₄
0	OFF	ON
1	ON	OFF

Logic "0" $\leq 0.8\ \text{V}$
 Logic "1" $\geq 2.4\ \text{V}$

ORDERING INFORMATION

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5143CJ

DG5143

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ABSOLUTE MAXIMUM RATINGS

(V+) – (V–)	< 36 V
(V+) – (V _D) ^a	< 30 V
(V _D) – (V–) ^a	< 30 V
(V _D) – (V _S) ^a	< ± 22 V
(V _L) – (V–)	< 33 V
(V _L) – (V _{IN})	< 30 V
V _L	< 20 V
V _{IN} ^a	< 20 V

Continuous Current, Any Terminal	30 mA
Peak Current, S or D (pulsed a 1 ms, 10% duty cycle max)	100 mA
Storage Temperature	–65 to 125°
Power Dissipation (Package) ^b	
16-Pin Plastic DIP	450 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V, VL = 5 V VIN = 2.4 V, 0.8 V ^e	Temp ^a	C Suffix 0 to 70°C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	-15		15	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = ± 10 V, I _S = - 10 mA	Room Full			75 100	Ω
Switch Off Leakage Current	I _{S(off)}	V _D = ∓ 10 V, V _S = ± 10 V	Room Full	-5 -20		5 20	nA
	I _{D(off)}		Room Full	-5 -20		5 20	
Channel On Leakage Current	I _{D(on)}	V _S = V _D = -10 to 10 V	Room Full	-2 -40		2 40	
Digital Control							
Input Current with V _{IN} Low	I _{IL}		Full	-1		1	μA
Input Current with V _{IN} High	I _{IH}		Full	-1		1	
Dynamic Characteristics							
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF See Figure 1	Room			175	ns
Turn-Off Time	t _{OFF}		Room			150	
Break-Before-Make	t _{ON} - t _{OFF}		Room			5	
Charge Injection ^d	Q	C _L = 10,000 pF, V _{gen} = 0 V, R _{gen} = 0 Ω	Room			150	pC
Off Isolation ^d	OIRR	R _L = 100 Ω, C _L ≤ 5 pF, f = 1 MHz	Room	-50			dB
Channel-to-Channel Crosstalk ^d	X _{TALK}	Any Other Channel Switches R _L = 100 Ω, C _L ≤ 5 pF, f = 1 MHz	Room			-50	
Power Supplies							
Positive Supply Current	I+	V _{IN} = 0 V or 5 V Switch Duty Cycle <10%	Room			10	μA
Negative Supply Current	I-		Room	-10			
Logic Supply Current	I _L		Room			10	
Ground Current	I _{GND}		Room	-10			

Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

The diagram shows a 2-to-1 multiplexer with inputs V_{S1} and V_{S2} , and select input IN . The output V_{O1} is connected to a feedback network consisting of a resistor R_{L1} (300 Ω) and a capacitor C_{L1} (35 pF) in parallel, which is then connected to the V_{S2} input. The multiplexer's control pins are V_L and V_+ (both at +5 V), and its power pins are V_+ (+15 V) and V_- (-15 V). The internal nodes of the multiplexer are labeled D_1 and D_2 . A square wave source is connected to the IN pin. The output V_{O2} is taken from the node between R_{L1} and C_{L1} . A second feedback network with resistor R_{L2} (300 Ω) and capacitor C_{L2} (35 pF) is connected from V_{O2} to the V_{S1} input. The text specifies $V_S = 10$ V for t_{ON} and $V_S = -10$ V for t_{OFF} .

The diagram shows four signals over time:

- Logic Input:** A square wave switching between 3 V and 0 V. The 50% transition point is marked.
- Switch Input:** A step function switching between V_S and 0 V.
- Switch Output:** A signal that transitions from 0 V to V_O (90% level) during t_{ON} and from V_O to 0 V during t_{OFF} .
- Switch Input:** A signal that transitions from 0 V to V_O (90% level) during t_{ON} and from V_O to 0 V during t_{OFF} .

Key parameters labeled:

- $t_r < 20 \text{ ns}$ (rise time)
- $t_f < 20 \text{ ns}$ (fall time)
- t_{ON} (turn-on delay)
- t_{OFF} (turn-off delay)
- V_S (supply voltage)
- V_O (output voltage)
- 90% (output voltage level)
- $90\% V_O$ (output voltage level)

FIGURE 1. Switching Time