

2N/SST5484 Series

N-Channel JFETs

2N5484 SST5484
 2N5485 SST5485
 2N5486 SST5486

Product Summary

Part Number	V _{GS(off)} (V)	V _{(BR)GSS} Min (V)	g _{fs} Min (mS)	I _{DSS} Min (mA)
2N/SST5484	-0.3 to -3	-25	3	1
2N/SST5485	-0.5 to -4	-25	3.5	4
2N/SST5486	-2 to -6	-25	4	8

Features

- Excellent High-Frequency Gain:
Gps 13 dB (typ) @ 400 MHz – 5485/6
- Very Low Noise: 2.5 dB (typ) @
400 MHz – 5485/6
- Very Low Distortion
- High AC/DC Switch Off-Isolation

Benefits

- Wideband High Gain
- Very High System Sensitivity
- High Quality of Amplification
- High-Speed Switching Capability
- High Low-Level Signal Amplification

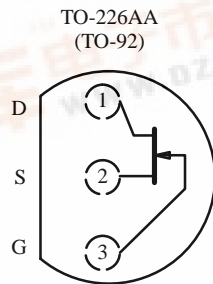
Applications

- High-Frequency Amplifier/Mixer
- Oscillator
- Sample-and-Hold
- Very Low Capacitance Switches

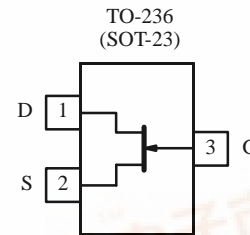
Description

The 2N/SST5484 series consists of n-channel JFETs designed to provide high-performance amplification, especially at high frequencies up to and beyond 400 MHz.

The 2N series, TO-226AA (TO-92), and SST series, TO-236 (SOT-23), packages provide low-cost options and are available with tape-and-reel to support automated assembly (see Packaging Information).



Top View
 2N5484
 2N5485
 2N5486



Top View
 SST5484 (H4)*
 SST5485 (H5)*
 SST5486 (H6)*

*Marking Code for TO-236

Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage	-25 V	Operating Junction Temperature	-55 to 150°C
Gate Current	10 mA	Power Dissipation ^a	350 mW
Lead Temperature	300°C	Notes	
Storage Temperature	-65 to 150°C	a. Derate 2.8 mW/°C above 25°C	

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70246.

Applications information may also be obtained via FaxBack, request document #70595 and #70598.

2N/SST5484 Series

Specifications^a for 2N Series

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit	
				2N5484		2N5485		2N5486			
				Min	Max	Min	Max	Min	Max		
Static											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-35	-25		-25		-25		V	
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 15 V, I_D = 10 nA$		-0.3	-3	-0.5	-4	-2	-6		
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 15 V, V_{GS} = 0 V$		1	5	4	10	8	20	mA	
Gate Reverse Current	I_{GSS}	$V_{GS} = -20 V, V_{DS} = 0 V$	-0.002		-1		-1		-1	nA	
		$T_A = 100^\circ C$	-0.2		-200		-200		-200		
Gate Operating Current ^d	I_G	$V_{DG} = 10 V, I_D = 1 mA$	-20							pA	
Gate-Source Forward Voltage ^d	$V_{GS(F)}$	$I_G = 10 mA, V_{DS} = 0 V$	0.8							V	
Dynamic											
Common-Source Forward Transconductance ^c	g_{fs}	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 kHz$		3	6	3.5	7	4	8	mS	
Common-Source Output Conductance ^c	g_{os}				50		60		75	μS	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 MHz$	2.2		5		5		5	pF	
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1		1		1		
Common-Source Output Capacitance	C_{oss}		1		2		2		2		
Equivalent Input Noise Voltage ^d	\bar{e}_n	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 100 Hz$	10							nV/\sqrt{Hz}	
High-Frequency											
Common-Source Transconductance	$Y_{fs(RE)}$	$V_{DS} = 15 V$ $V_{GS} = 0 V$	$f = 100 MHz$	5.5	2.5					mS	
			$f = 400 MHz$	5.5		3		3.5			
Common-Source Output Conductance	$Y_{os(RE)}$		$f = 100 MHz$	45		75				μS	
			$f = 400 MHz$	65			100		100		
Common-Source Input Conductance	$Y_{is(RE)}$		$f = 100 MHz$	0.05		0.1				mS	
			$f = 400 MHz$	0.8			1		1		
Common-Source Power Gain	G_{ps}	$V_{DS} = 15 V, I_D = 1 mA$ $f = 100 MHz$	20	16	25					dB	
		$V_{DS} = 15 V$ $I_D = 4 mA$	$f = 100 MHz$	21		18	30	18	30		
			$f = 400 MHz$	13		10	20	10	20		
Noise Figure	NF	$V_{DS} = 15 V, V_{GS} = 0 V$ $R_G = 1 M\Omega, f = 1 kHz$	0.3		2.5		2.5		2.5	dB	
		$V_{DS} = 15 V, I_D = 1 mA$ $R_G = 1 k\Omega, f = 100 MHz$	2		3						
		$V_{DS} = 15 V$ $I_D = 4 mA$ $R_G = 1 k\Omega$	$f = 100 MHz$	1				2			2
			$f = 400 MHz$	2.5				4			4

2N/SST5484 Series

Specifications^a for SST Series

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit
				SST5484		SST5485		SST5486		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 15 V, I_D = 10 nA$		-0.3	-3	-0.5	-4	-2	-6	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 15 V, V_{GS} = 0 V$		1	5	4	10	8	20	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -20 V, V_{DS} = 0 V$	-0.002		-1		-1		-1	nA
		$T_A = 100^\circ C$	-0.2		-200		-200		-200	nA
Gate Operating Current ^d	I_G	$V_{DG} = 10 V, I_D = 1 mA$	-20							pA
Gate-Source Forward Voltage ^d	$V_{GS(F)}$	$I_G = 10 mA, V_{DS} = 0 V$	0.8							V
Dynamic										
Common-Source Forward Transconductance ^c	g_{fs}	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 kHz$		3	6	3.5	7	4	8	mS
Common-Source Output Conductance ^c	g_{os}				50		60		75	μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 MHz$	2.2							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7							
Common-Source Output Capacitance	C_{oss}		1							
Equivalent Input Noise Voltage ^d	\bar{e}_n	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 100 Hz$	10							nV/ \sqrt{Hz}
High-Frequency										
Common-Source Transconductance	Y_{fs}	$V_{DS} = 15 V$ $V_{GS} = 0 V$	$f = 100 MHz$	5.5						mS
			$f = 400 MHz$	5.5						
Common-Source Output Conductance	Y_{os}		$f = 100 MHz$	45						μS
			$f = 400 MHz$	65						
Common-Source Input Conductance	Y_{is}		$f = 100 MHz$	0.05						mS
			$f = 400 MHz$	0.8						
Common-Source Power Gain	G_{ps}	$V_{DS} = 15 V, I_D = 1 mA$ $f = 100 MHz$	20						dB	
		$V_{DS} = 15 V$ $I_D = 4 mA$	$f = 100 MHz$	21						
			$f = 400 MHz$	13						
Noise Figure	NF	$V_{DS} = 15 V, V_{GS} = 0 V$ $R_G = 1 M\Omega, f = 1 kHz$	0.3						dB	
		$V_{DS} = 15 V, I_D = 1 mA$ $R_G = 1 k\Omega, f = 100 MHz$	2							
		$V_{DS} = 15 V$ $I_D = 4 mA$ $R_G = 1 k\Omega$	$f = 100 MHz$	1						
			$f = 400 MHz$	2.5						

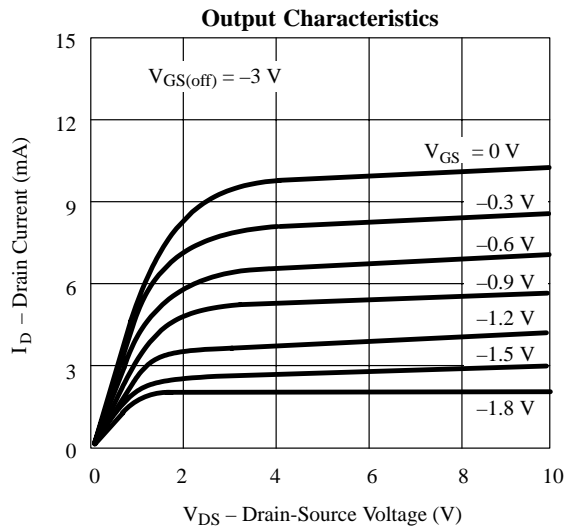
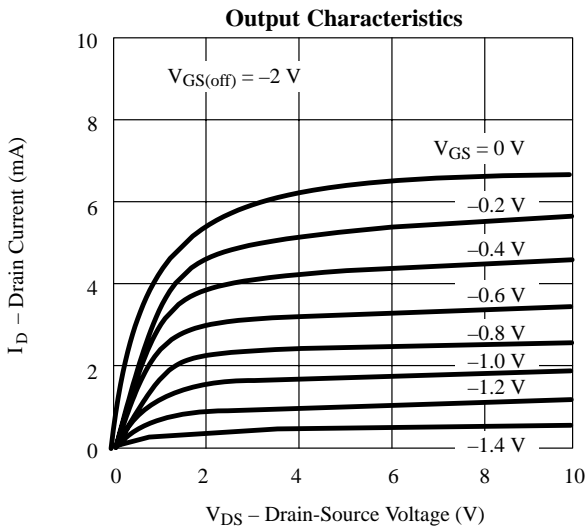
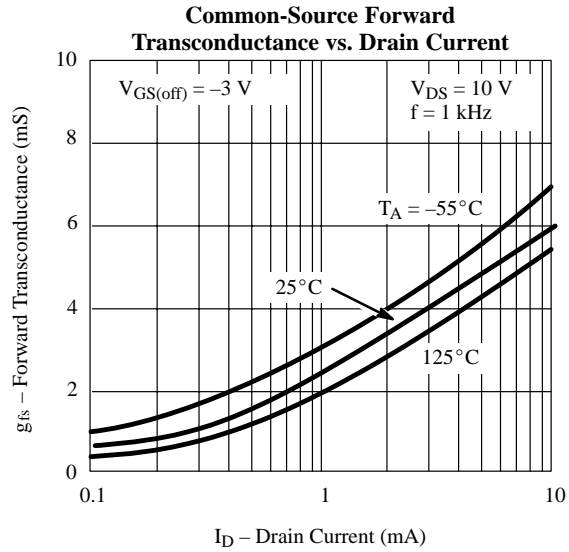
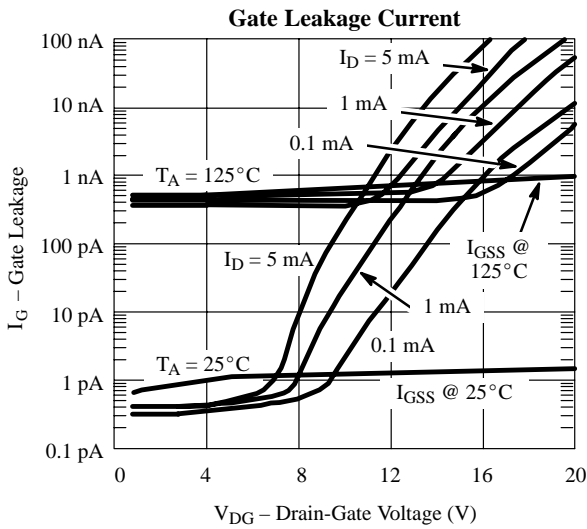
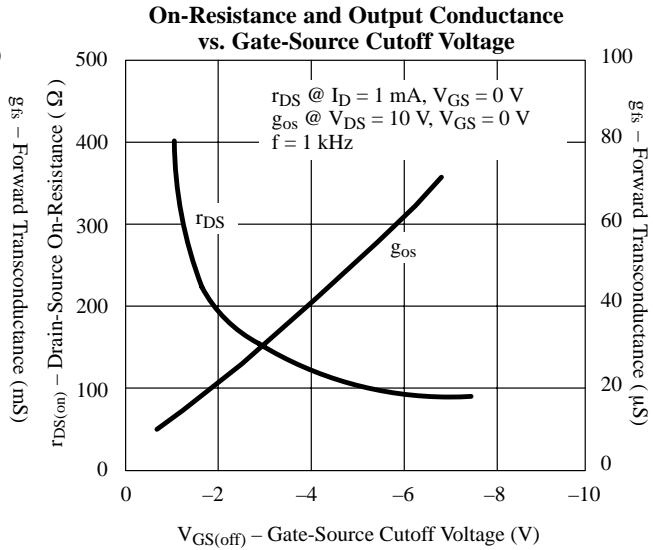
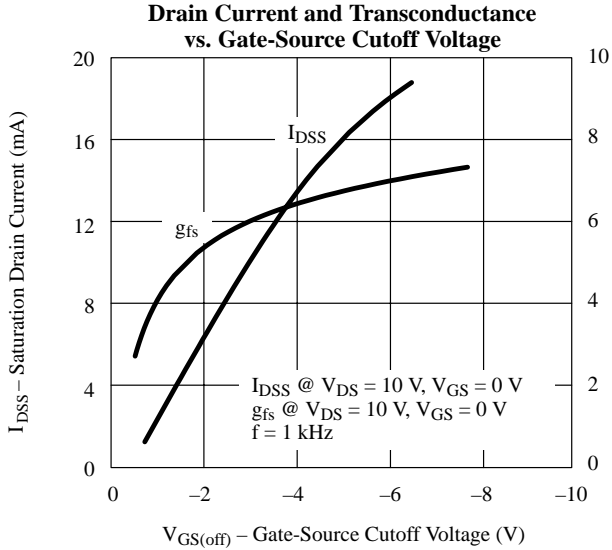
Notes

- $T_A = 25^\circ C$ unless otherwise noted.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.
- This parameter not registered with JEDEC.

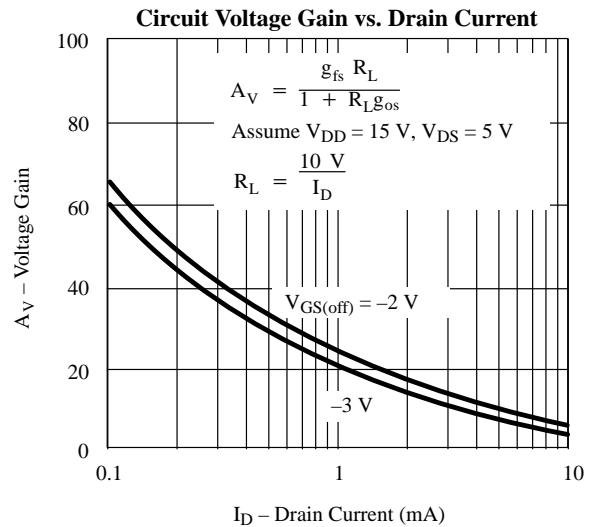
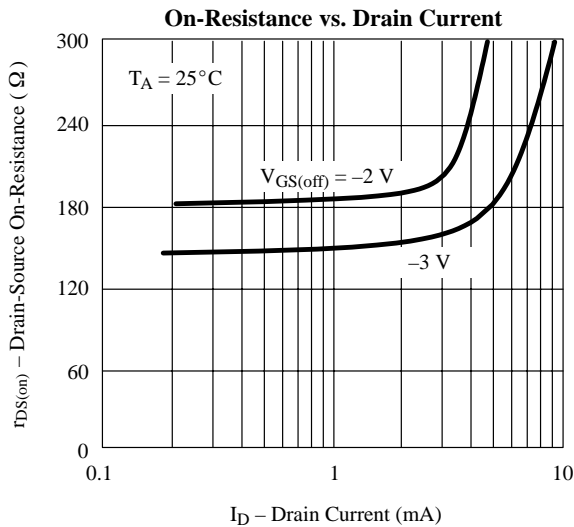
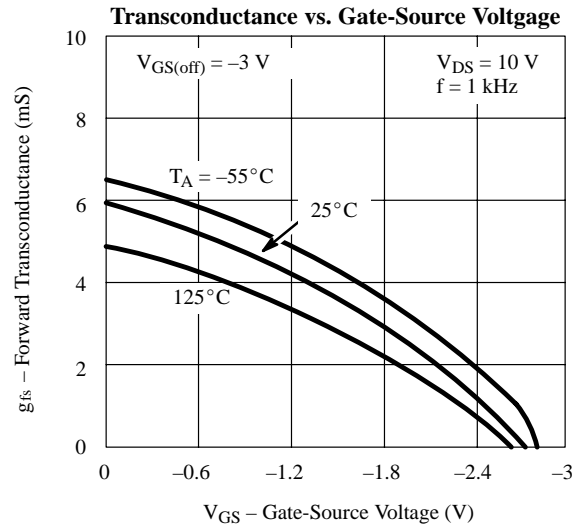
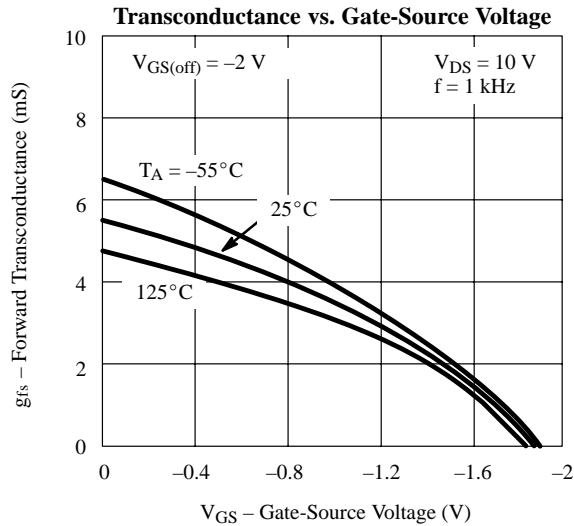
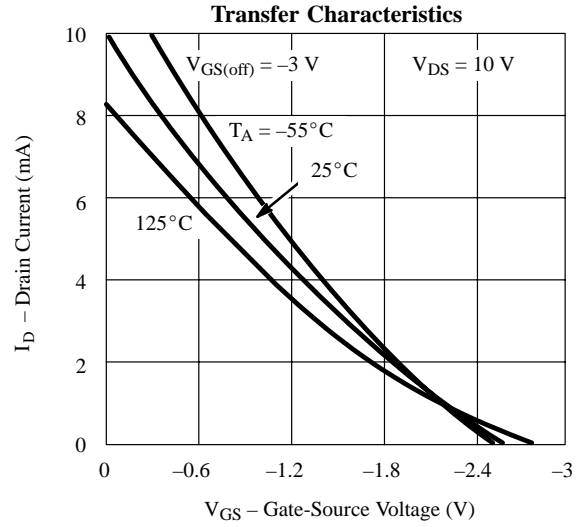
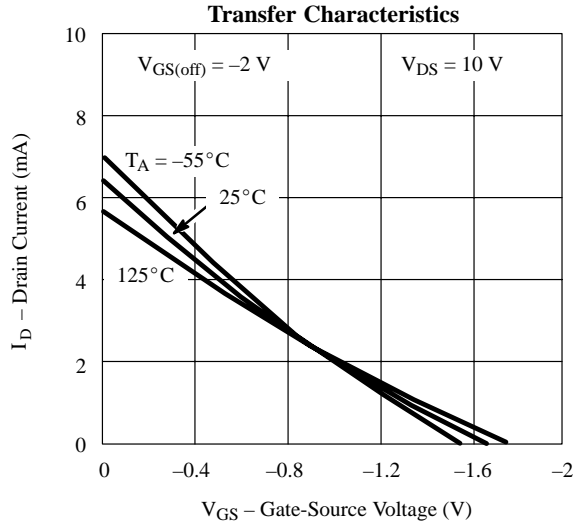
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2N/SST5484 Series

Typical Characteristics



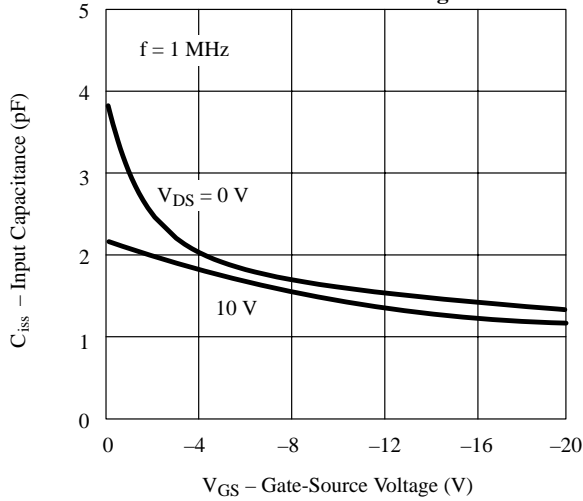
Typical Characteristics (Cont'd)



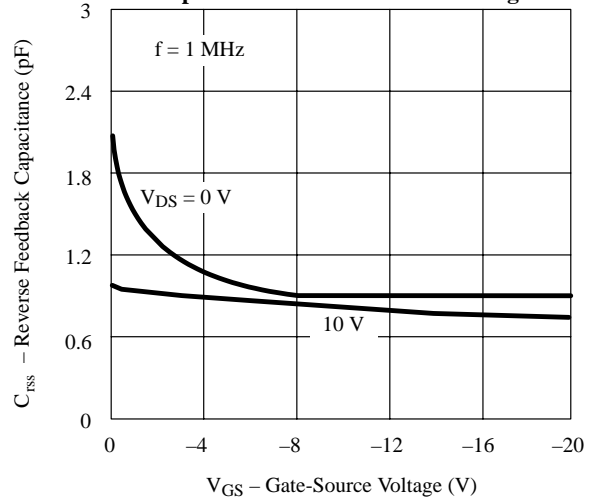
2N/SST5484 Series

Typical Characteristics (Cont'd)

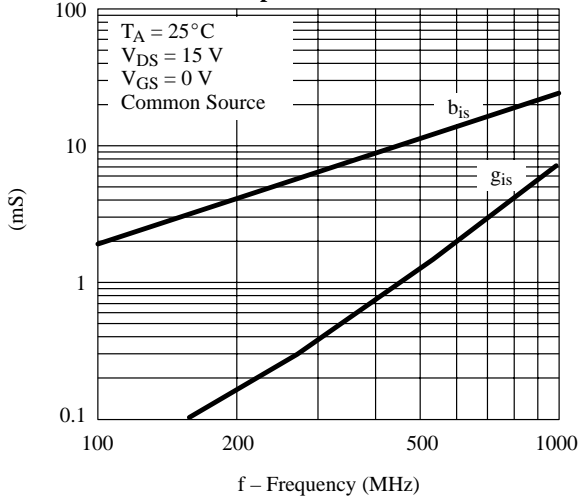
Common-Source Input Capacitance vs. Gate-Source Voltage



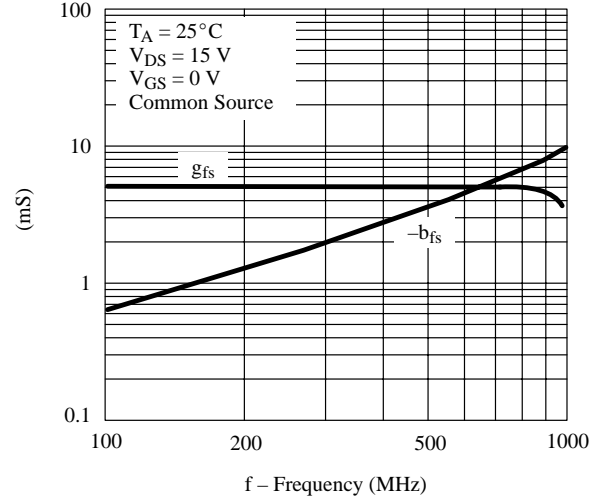
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



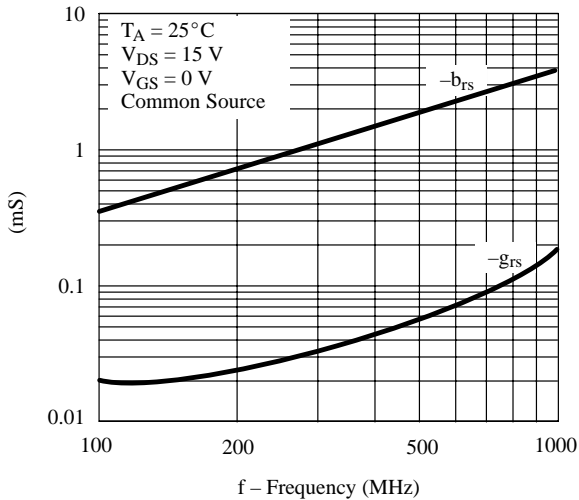
Input Admittance



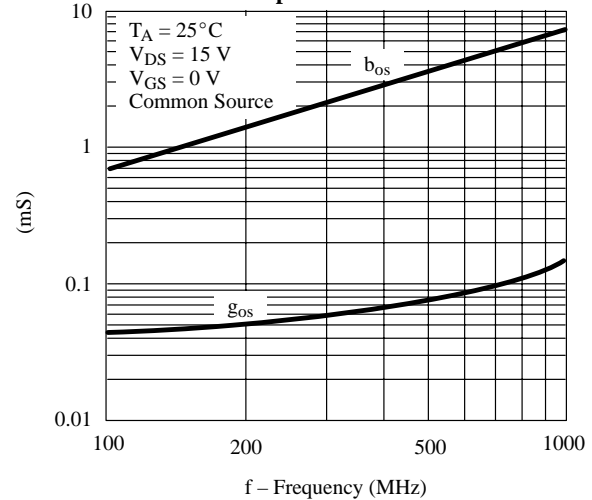
Forward Admittance



Reverse Admittance



Output Admittance



2N/SST5484 Series

Typical Characteristics (Cont'd)

