

SST/U401 Series

Monolithic N-Channel JFET Duals

SST404 U401 U406
SST406 U404

Product Summary

Part Number	V _{GS(off)} (V)	V _{(BR)GSS} Min (V)	g _{fs} Min (mS)	I _G Typ (pA)	V _{GS1} - V _{GS2} Max (mV)
U401	-0.5 to -2.5	-40	1	-2	5
SST/U404	-0.5 to -2.5	-40	1	-2	15
SST/U406	-0.5 to -2.5	-40	1	-2	40

Features

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 2 pA
- Low Noise
- High CMRR: 102 dB

Benefits

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

Applications

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

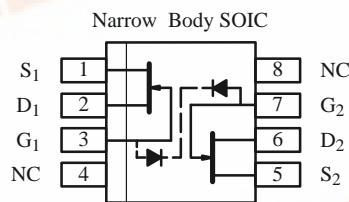
Description

The SST/U401 series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. This series has a wide selection of offset and drift specifications with the U401 featuring a 5-mV offset and 10-μV/°C drift.

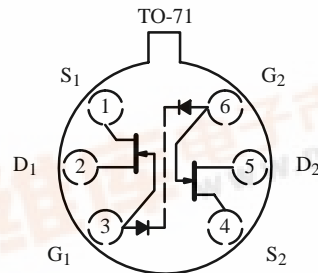
available with full military processing (see Military Information). The SST series SO-8 package provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods (see Packaging Information).

The U series' hermetically sealed TO-71 package is

For similar high-gain products in TO-78 packaging, see the 2N5911/5912 data sheet.



Top View
SST404, SST406



Top View
U401, U404, U406

Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage	-40 V
Gate Current	10 mA
Lead Temperature (1/16" from case for 10 sec.)	300°C
Storage Temperature:	
U Prefix	-65 to 200°C
SST Prefix	-55 to 150°C

Operating Junction Temperature	-55 to 150°C
Power Dissipation:	
Per Side ^a	300 mW
Total ^b	500 mW

Notes

- Derate 2.4 mW/°C above 25°C
- Derate 4 mW/°C above 25°C

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70247. Applications information may also be obtained via FaxBack, request document #70599.

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Specifications^a

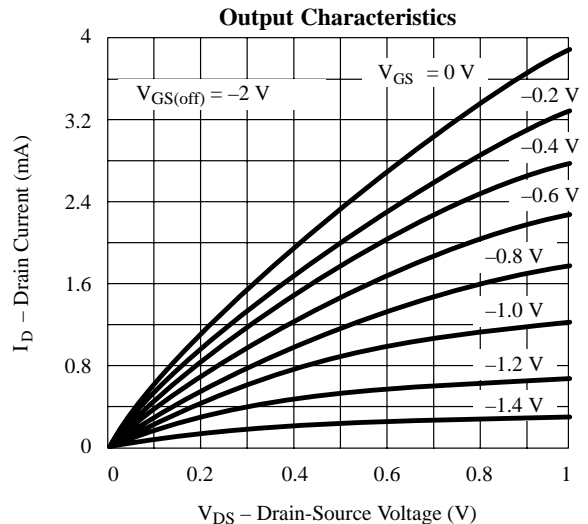
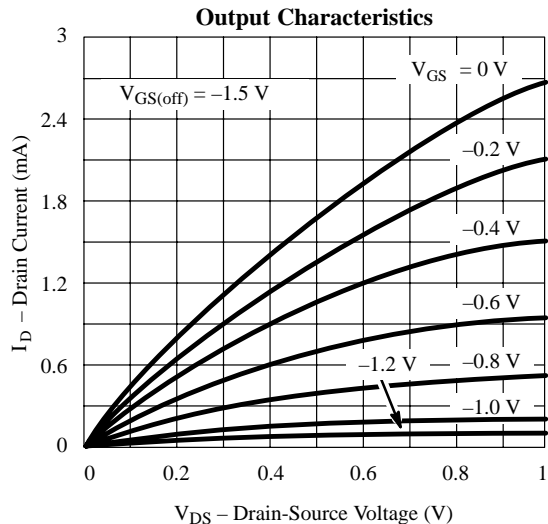
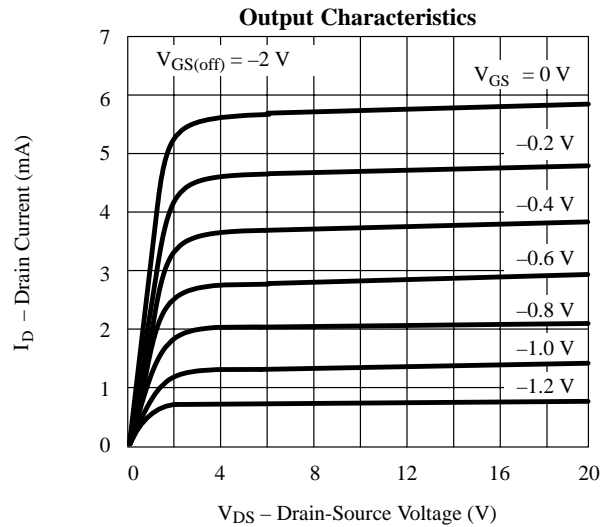
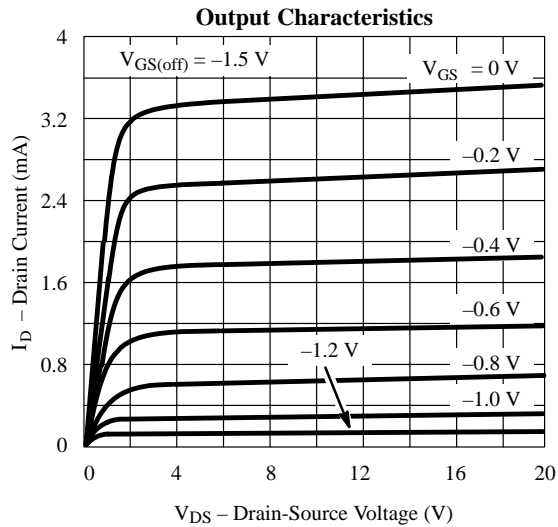
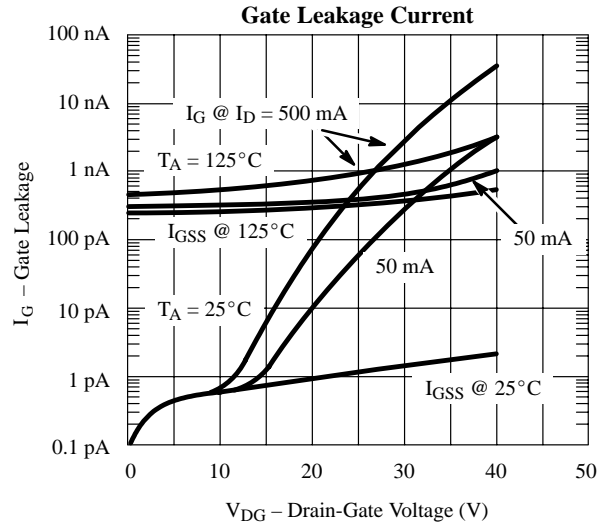
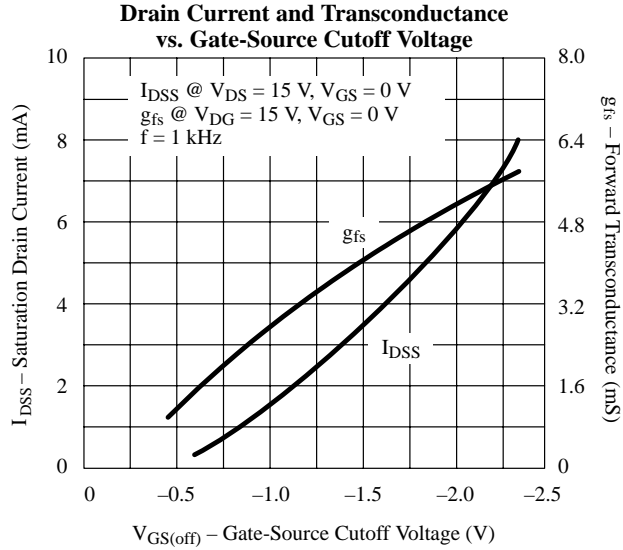
Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit
				U401		SST/U404		SST/U406		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-58	-40		-40		-40		V
	$V_{(BR)G1-G2}$	$I_G = \pm 1 \mu A, V_{DS} = 0 V, V_{GS} = 0 V$	± 45	± 30		± 30		± 30		
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 15 V, I_D = 1 nA$	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 10 V, V_{GS} = 0 V$	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -30 V, V_{DS} = 0 V$	-2		-25		-25		-25	pA
		$T_A = 125^\circ C$	-1							nA
Gate Operating Current	I_G	$V_{DG} = 15 V, I_D = 200 \mu A$	-2		-15		-15		-15	pA
		$T_A = 125^\circ C$	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0 V, I_D = 0.1 mA$	250							Ω
Gate-Source Voltage	V_{GS}	$V_{DG} = 15 V, I_D = 200 \mu A$	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7							
Dynamic										
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 15 V, I_D = 200 \mu A, f = 1 kHz$	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	μS
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz$	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		5		30		30		30	μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 15 V, I_D = 200 \mu A, f = 1 MHz$	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 15 V, I_D = 200 \mu A, f = 10 Hz$	10		20		20		20	nV/ \sqrt{Hz}
Matching										
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10 V, I_D = 200 \mu A$			5		15		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10 V, I_D = 200 \mu A, T_A = -55 \text{ to } 125^\circ C$	SST404	20						$\mu V/^\circ C$
			SST406	40						
			All U		10		25		80	
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10 \text{ to } 20 V, I_D = 200 \mu A$	102	95		95				dB

Notes

- $T_A = 25^\circ C$ unless otherwise noted.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.

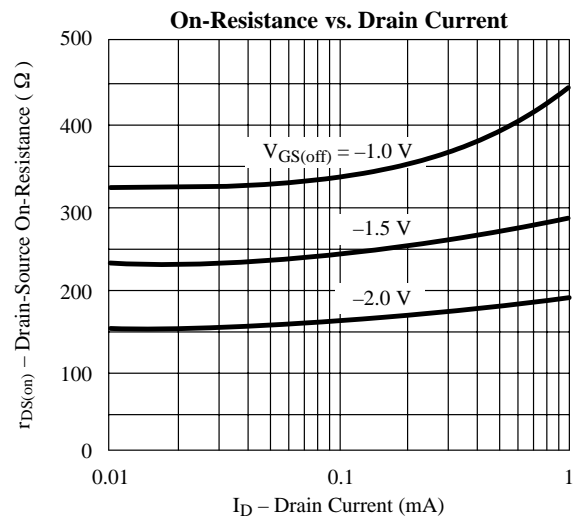
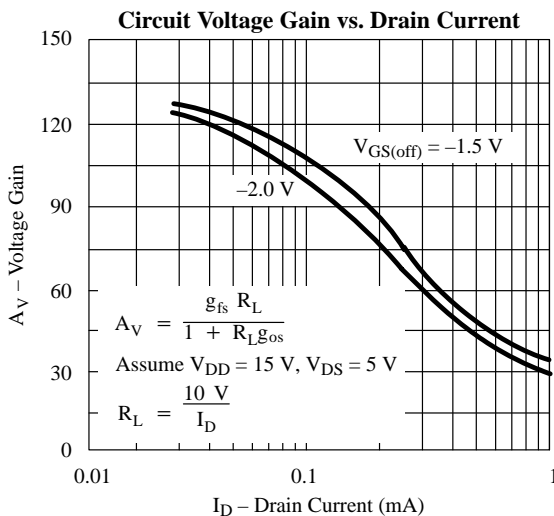
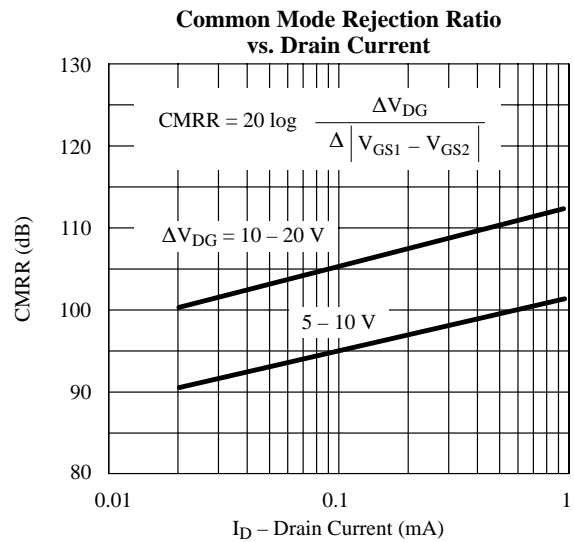
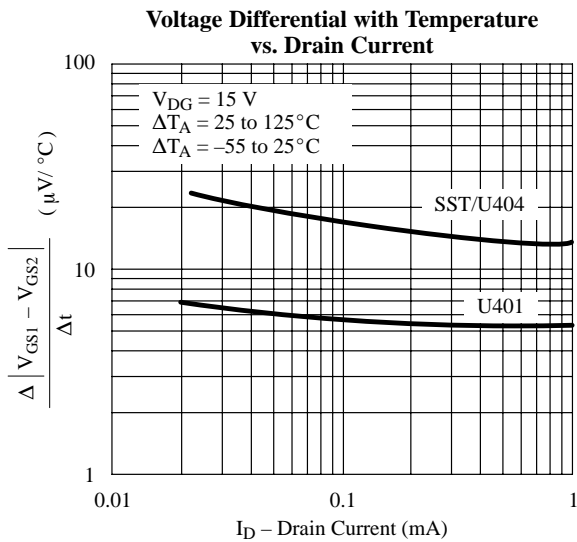
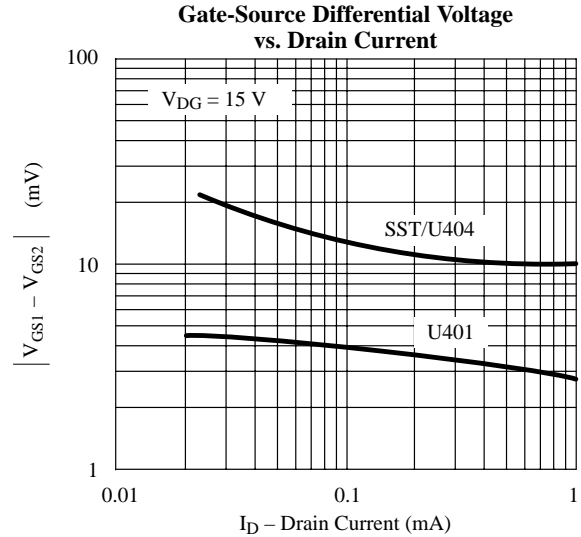
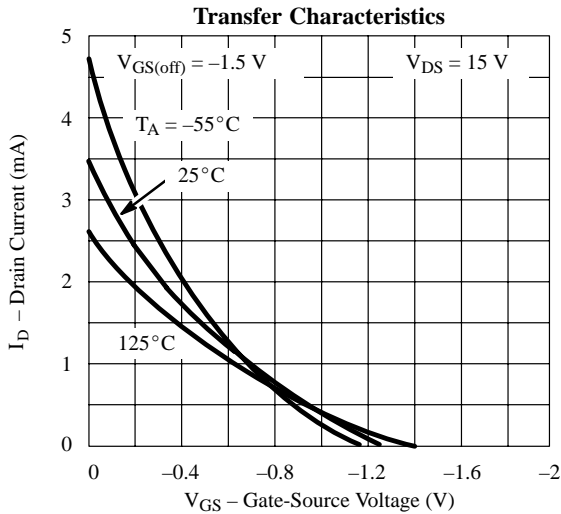
NRR

Typical Characteristics



SST/U401 Series

Typical Characteristics (Cont'd)



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Typical Characteristics (Cont'd)

