



**Si9990ACS**

**Vishay Siliconix**

## 5-V VCM Driver/Spindle Motor Driver For 1.8- and 2.5-Hard Disk Drives

### FEATURES

- On-Board Half-Bridge Drivers
  - Spindle = 2.3  $\Omega$  Total at 1 A
  - VCM = 3.3  $\Omega$  Total at 0.3 A
- Spindle Driver Features:
  - Back EMF Commutation
  - Linear Current Control
  - Internal Current Sense Resistor
  - Start-Up Current Limit (10% Accurate)

### BENEFITS

- Single 5-V Supply
- Rail-to-Rail Output Voltage Swing
- VCM Driver Features:
  - Class AB Linear Operation
  - Externally Programmable Gain and Bandwidth
  - Programmable Retract Current and Fixed Voltage Clamp

### APPLICATIONS

- Over-Temperature Protection
- System Voltage Monitor
- Undervoltage Head Retract
- Sleep Mode and Idle Mode
- Reference Generator
- Two Uncommitted Amplifiers

### DESCRIPTION

The Si9990ACS has a 3-phase brushless dc (spindle) motor driver and a linear transconductance amplifier suitable for driving a voice coil motor (head actuator).

#### Spindle Motor Driver

The spindle driver features three 1-A, 2.3- $\Omega$  (total) all n-channel MOSFET half-bridge output stages. The spindle driver uses internal back EMF sensing circuitry that eliminates the need for hall sensors. An internal charge pump allows rail-to-rail output voltage swing with a nominal 5-V supply. A unique output structure eliminates the need for an external Schottky diode to isolate the system 5-V supply if it fails during operation. This makes the output half-bridge drive capability equivalent to drivers with 1-A, 1.9- $\Omega$  specifications in series with the required Schottky diode.

#### VCM Driver

The VCM driver provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier

and a 300-mA power amplifier featuring four MOSFETs in an H-bridge configuration. The output crossover protection ensures no cross-conducting current and Class AB operation during linear tracking. Externally programmable gain switching at the input summing junction increases the resolution and dynamic range for a given DAC. The head retract circuitry can be activated by either an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract. The retract voltage clamp is set at 0.44 V.

A reference generator and two uncommitted amplifiers are also provided for analog interface.

In sleep mode, internal logic initiates a head retract operation followed by spindle brake and shutdown of all analog circuitry except the supply monitor. The standby power dissipation is less than 6 mW. The VCM may also be disabled without disabling spindle operation (idle mode). All controls from the microprocessor are communicated via the serial interface. Additional housekeeping functions of the driver include thermal shutdown and undervoltage lockout.

The Si9990ACS is manufactured using a self-isolated BiC/DMOS process and is available in a 64-pin SQFP package for operation over the commercial (0 to 70°C) temperature range.

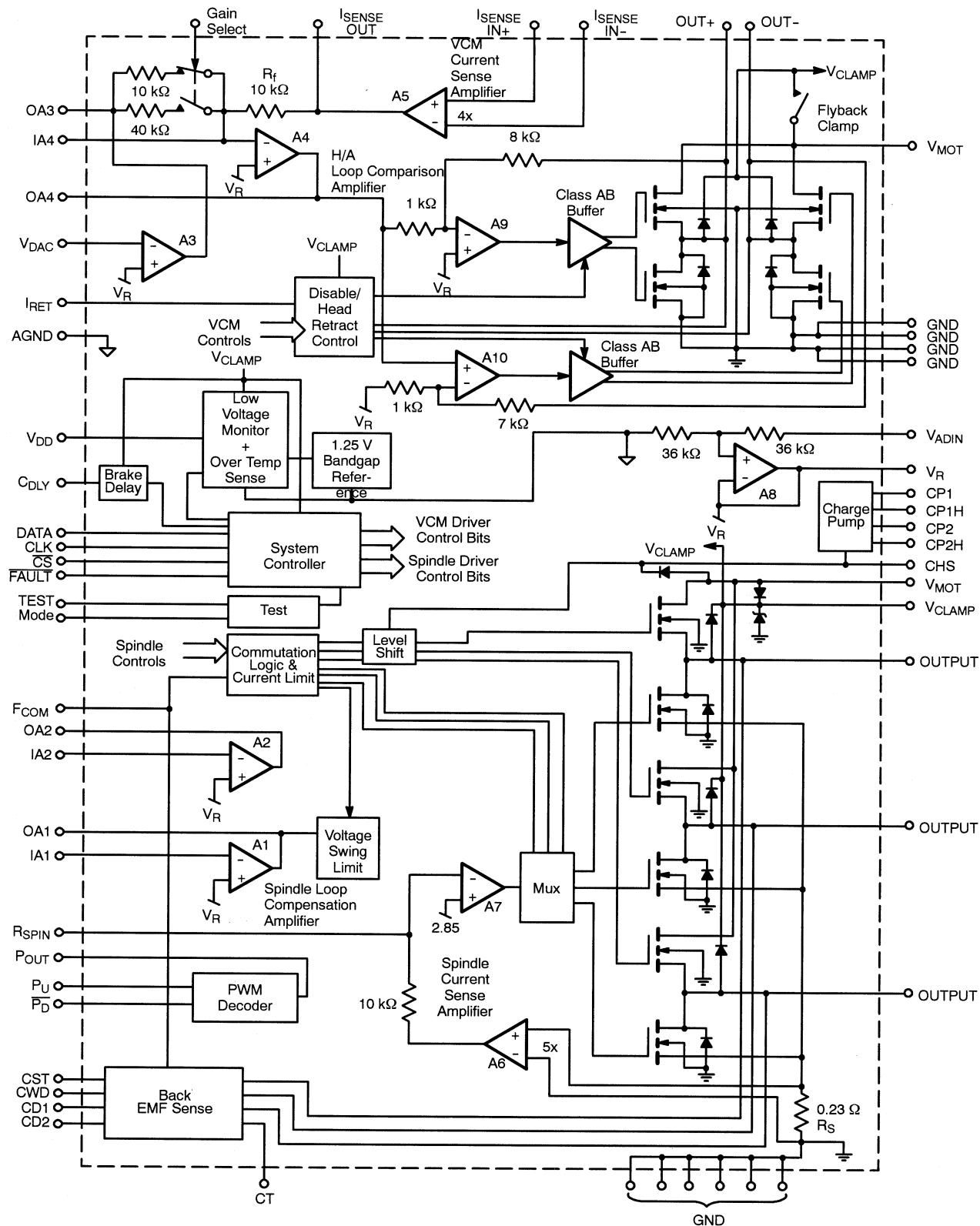


# Si9990ACS

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## FUNCTIONAL BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to Common Pin

$V_{DD}$ Supply Range	-0.3 V to 7 V
Pin (Output A, B and C)	-0.3 V to $V_{CLAMP} + 0.3$ V
Pin (Output + and -)	-0.3 to $V_{MOT} + 0.3$ V
Pin (CHS, CP1H, CP2H)	-0.3 V to 16 V

Maximum Output Current<sup>a</sup>

Output A, B and C (Peak)	1.2 A
Output A, B, and C (Continuous)	0.4 A
Output + and - (Peak)	0.5 A
Output + and - (Continuous)	0.3 A

Pin (All Others) -0.3 V to  $V_{DD} + 0.3$  V

Maximum Clamp Current<sup>b</sup>

Output A, B and C	$\pm 1.2$ A
Output + and -	$\pm 0.5$ A
(Pulsed 10 ms at 10% duty cycle)	
All Other Pins	$\pm 20$ mA

$V_{MOT}$ to $V_{CLAMP}$ Diode (Peak)	100 mA
$V_{MOT}$ to $V_{CLAMP}$ Diode (Continuous)	50 mA
$V_{MOT}$ to CHS Diode (Peak)	50 mA
$V_{MOT}$ to CHS Diode (Continuous)	25 mA

Storage Temperature -65 to 150°C

Operating Temperature 0 to 70°C

Junction Temperature ( $T_J$ ) 150°C

Power Dissipation<sup>c</sup> — 64-Pin SQFP 2.0 W

Thermal Impedance ( $\theta_{JA}$ )<sup>c</sup> — 64-Pin SQFP 62.5°C/W

Notes

a. Output current rating is dependent on the system duty cycle, start-up timing and heat dissipation capability.

b. Diode currents depend on power supply start-up transient and bypass capacitor values.

c. Device mounted with all leads soldered or welded to PC board.

## SPECIFICATIONS

Parameters	Symbol	Test Conditions Unless Specified  $V_{ADIN} = V_{DD} = V_{MOT} = 5\text{ V} \pm 10\%$ $R_S(VCM) = 1.67\ \Omega$ $R_{SPIN} = 17\text{ k}\Omega$ , $T_A = 0\text{ to }70^\circ\text{C}$	Limits			Unit
			Min	Typ	Max	
Supply						
Supply Current	$I_{DD} + I_{MOT}$	Static, No Load, Sleep Mode		0.9	1.2	mA
		Static, No Load, Normal Operation		20	41	
		Static, No Load, Idle Mode		14	19	
$V_{DD}$ , $V_{MOT}$ Operating Range	$V_{DD}$ , $V_{MOT}$		4.5	5	5.5	V
Control Logic						
Low Input Voltage (G/S, DATA, CLK, $\overline{CS}$ , $P_U$ , $\overline{P_D}$ )	$V_{IL}$		-0.3		1.5	V
High Input Voltage	$V_{IH}$		3.5		5.3	
Low Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$	-1			$\mu\text{A}$
High Input Current	$I_{IH}$	$V_{IH} = 5\text{ V}$			1	
Mode Pin Pull Down Current	$I_{PD}$	$V_{IN} = 5\text{ V}$			100	
Low Output Voltage ( $F_{COM}$ , $FAULT$ , $P_{OUT}$ )	$V_{OL}$	$I_{OUT} = 500\ \mu\text{A}$			0.5	V
High Output Voltage	$V_{OH}$	$I_{OUT} = -500\ \mu\text{A}$	4			
$P_{OUT}$ Off-State Leakage Current		$V_{OUT} = 2.5\text{ V}$	-1		1	$\mu\text{A}$
EMF Comparator Offset	$V_{OS}$		20	40	70	mV
Maximum EMF Comparator Input Common Mode Voltage				4.3		V
CST Current	$I_{CST}$	Charging or Discharging		5		$\mu\text{A}$
CD Current (CD1 or CD2)	$I_{CST1}$ or $I_{CST2}$	Charging		10		
		Discharging		-20		
$I_{CD}$ (Discharging)/ $I_{CD}$ (Charging)		$C_{D1}$ or $C_{D2}$		2.0		
CWD Current	$I_{CWD}$	Charging		5		$\mu\text{A}$
		Discharging		-25		
CWD Threshold Voltage	$V_{TL}$			0.5		V
	$V_{TH}$			2.50		



SPECIFICATIONS							
Parameters		Symbol	Test Conditions Unless Specified $V_{ADIN} = V_{DD} = V_{MOT} = 5\text{ V} \pm 10\%$ $R_S(V_{CM}) = 1.67\ \Omega$ $R_{SPIN} = 17\text{ k}\Omega$ , $T_A = 0\text{ to }70^\circ\text{C}$	Limits			Unit
				Min	Typ	Max	
Spindle Transconductance Amplifier ( $A_1$ )							
Voltage Gain		$A_V$	$R_{LOAD} = 50\text{ k}\Omega$ to $V_R$ (See Note a) Measured at 1.2 to 2.9 V		60		dB
Gain-Bandwidth		$F_o$	$R_{LOAD} = 50\text{ k}\Omega$ , $C_{LOAD} = 100\text{ pF}$ to $V_R$		1		MHz
Slew Rate		SR		0.5			V/ $\mu$ s
Output Voltage Swing		$V_{OUT}$	$R_{LOAD} = 50\text{ k}\Omega$ to $V_R$ Bits $D_2\ D_3 = 00$ to $11$	0.8		3.1	V
Input Bias Current		$I_b$				50	nA
Offset Voltage		$V_{OS}$				10	mV
Power Supply		PSRR	$f = 10\text{ kHz}$		50		dB
Spindle Transconductance Amplifier ( $A_6$ and $A_7$ )							
Transconductance		$G_{ms}$	$R_{LOAD} = 4\ \Omega$ to $V_{MOT}$	0.4	0.5	0.6	A/V
Output Current Limit Accuracy				-20		20	%
-3 dB Bandwidth		$F_o$	$R_{LOAD} = 4\ \Omega$ to $V_{MOT}$ , $C_{LOAD} = 100\text{ pF}$		70		kHz
Slew Rate		SR			1		V/ $\mu$ s
Output Current Cutoff Voltage			Measured at OA1 with respect to GND	2.70	2.85	3.0	V
Spindle Half-Bridge							
On-Resistance (Sink or Source)		$r_{DS(on)}$	$I_{OUT} = 1\text{ A}$		0.6		$\Omega$
			$I_{OUT} = 1\text{ A}$ including $0.23\ \Omega\ R_S$		0.7		
			(Sink + Source), $I_{OUT} = 1\text{ A}$			2.3	
Output Leakage Current		$I_{DS(off)}$	$V_{OUT} = V_{MOT}$			100	$\mu$ A
			$V_{OUT} = 0\text{ V}$	-100			
Clamp Diode		$V_{f(on)}$	$I_{OUT} = 1\text{ A}$	-1.5			V
VCM Transconductance Amplifier ( $A_3$ , $A_4$ , $A_5$ , $A_9$ , $A_{10}$ and DMOS FETs)							
Transconductance		$G_{MVH}$	Gain Select = High, $I_{OUT} = \pm 300\text{ mA}$	142	150	158	mA/V
		$G_{MVL}$	Gain Select = Low, $I_{OUT} = \pm 75\text{ mA}$	35.6	37.5	39.4	
Output Offset Current, High Gain		$I_{OS}$ , HG	Gain Select = High	-5	0	+5	mA
Output Offset Current, Low Gain		$I_{OS}$ , LG	$I_{OS}$ (G/Sel = High)- $I_{OS}$ (G/Sel = Low)	-5	0	+5	
Output Compliance		$V_{OH}$	$I_{OH} = 0.3\text{ A}$ , $V_{MOT} = 4.5\text{ V}$ , $\pm$ Output	3.9	4.2		V
		$V_{OL}$	$I_{OL} = 0.3\text{ A}$ , $V_{MOT} = 4.5\text{ V}$ , $\pm$ Output		0.2	0.4	
Clamp Diode Voltage		$V_{CL}$	$I_F = 0.3\text{ A}$			1.5	
Feedback Resistance		$R_F$	From $I_{SENSE(OUT)}$ to IA4		10		k $\Omega$
3 dB Bandwidth	$A_4$ , $A_5$				1		MHz
	$A_9$ , $A_{10}$				0.4		
PSRR			@ 10 kHz		50		dB
Output Swing	$A_3$ , $A_5$		$R_{LOAD} = 50\text{ k}\Omega$ to $V_R$	0.2		$V_{DD} - 0.2$	V
	$A_4$			1.2		$V_{DD} - 1.2$	
Reference Generator ( $A_8$ )							
Input Resistance			Measured at $V_{ADIN}$ Pin		72		k $\Omega$
Output Voltage		$V_R$	$I_{OUT} = \pm 2\text{ mA}$	2.37	2.5	2.63	V



SPECIFICATIONS						
Parameters	Symbol	Test Conditions Unless Specified $V_{ADIN} = V_{DD} = V_{MOT} = 5\text{ V} \pm 10\%$ $R_S(VCM) = 1.67\ \Omega$ $R_{SPIN} = 17\text{ k}\Omega$ , $T_A = 0\text{ to }70^\circ\text{C}$	Limits			Unit
			Min	Typ	Max	
Power Supply Monitor						
$V_{DD}$ Undervoltage Threshold			3.7	3.9	4.1	V
Hysteresis				70		mV
Overtemperature Protection						
Trip Point				165		$^\circ\text{C}$
Hystersis				20		
Head Retract Function (Undervoltage Or Sleep Mode; $C_{DLY}$ tied to $V_{CLAMP}$ )						
$I_{RET}$ Bias Voltage	$V_{RET}$	$I_{RET} = \frac{V_{RET}}{R_{RET}}$ , $I_{OUT} = -(200 \times I_{RET})$		0.25		V
Retract Output Current Limit	$I_{OUT+}$	$R_{RET} = 2.5\text{ k}\Omega$ , $V_{OUT+} = 0.2\text{ V}$	14	20	26	mA
Retract Output Voltage Limit	$V_{OUT-}$	$I_{OUT-} = -20\text{ mA}$	0.31	0.44	0.5	V
Emergency Retract Supply Current	$I_{CLAMP}$	$V_{CLAMP} = 3\text{ V}$ , $R_{RET} = 2.5\text{ k}\Omega$ $V_{DD} = 0\text{ V}$ , Static, No Load		2	4	mA
Retract Supply Voltage Range	$V_{CLAMP}$		1.41	5	5.5	V
CHS Leakage	$I_{CHS}$	$V_{DD} = 0\text{ V}$ , $V_{CLAMP} = 3\text{ V}$ , $V_{CHS} = 10\text{ V}$			2	$\mu\text{A}$
dc to dc Converter (Charge Pump)						
Output Voltage	CHS	$I_{CHS} = -5\text{ mA}$ , $V_{DD} = V_{MOT} = 4.5\text{ V}$	11			V
Flyback Clamp						
Flyback Clamp Switch Resistance		Normal Mode, $I_{CLAMP} = 0.1\text{ A}$		4		$\Omega$
Clamp Zener Voltage	$V_Z$	$I_{CLAMP} = 0.1\text{ A}$		9.1		V
Uncommitted Amplifier ( $A_2$ )						
Input Offset Voltage	$V_{OS}$		-15	0	+15	mV
Input Bias Current	$I_B$				50	nA
Unity Gain Bandwidth		$R_{LOAD} = 50\text{ k}\Omega$ , $C_{LOAD} = 100\text{ pF}$ to $V_R$		1		MHz
Slew Rate	SR		1			V/ $\mu\text{s}$
Power Supply Rejection Ratio	PSRR	@ 10 kHz		50		dB
Open Loop Voltage Gain	$A_{VOL}$	$R_{LOAD} = 50\text{ k}\Omega$ to $V_R$ , Measured at $V_R \pm 1.8\text{ V}$		60		
Output Voltage Swing	$V_O$	$R_{LOAD} = 50\text{ k}\Omega$ to $V_R$	0.2		$V_{DD} - 0.2$	V
Timing						
Chip Select to Clock Setup Time	$t_{CS}$	See Timing Diagram, Figure 1.	160			ns
Data Setup Time	$t_{DS}$		160			
Data Hold Time	$t_{DH}$		160			
Head Retract Time-Out (Brake Delay)	$t_{DLY}$	$t_{DLY} = 514\text{ k}\Omega \times C_{DLY}$ , $C_{DLY} = 0.18\ \mu\text{F}$ , $V_{DD} = 0\text{ V}$ , $V_{CLAMP} = 1.41\text{ to }5.5\text{ V}$	55	100	240	ms

**Notes**

a. 50-k $\Omega$  load is in addition to the  $R_{SPIN}$  load.



### DETAILED DESCRIPTION

#### Serial Port

A 6-bit word at the serial port DATA pin is used to program basic operating conditions. The function of each bit is shown in Tables 1 and 2. To write data to the serial port,  $\overline{CS}$  is pulled low during CLOCK low. This holds the existing word while new data is written into the shift registers on a positive CLOCK edge. The new data becomes valid on the rising edge of  $\overline{CS}$ . When  $\overline{CS}$  is high, CLOCK is disabled and data cannot be shifted.

D0 is the last bit written to the serial port. It enters sleep mode ( $D0 = 0$ ) upon power up. When D0 is written "0", a head retract is automatically initiated and  $t_{DL}$  applies following the next  $\overline{CS}$  rising edge.

The Mode pin is used for production testing only. It should be tied low during normal operation.

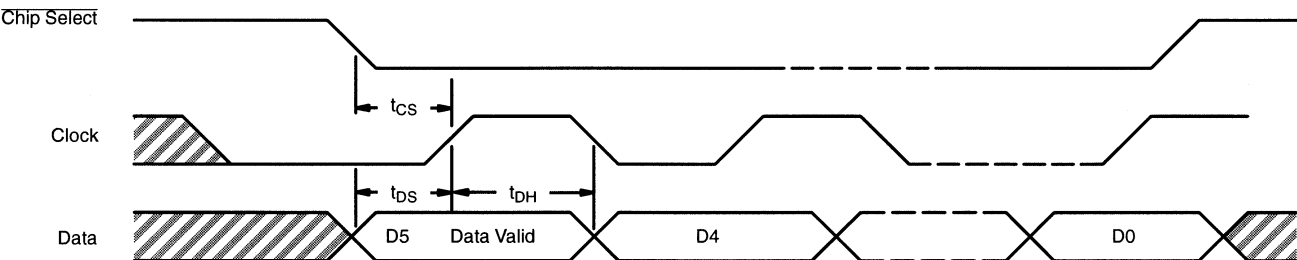
**TABLE 1.** Serial Port Definitions

Bit	Name	Function	
		0	1
D0	Sleep Mode/System Enable	Sleep Mode: VCM retracted, spindle and VCM brake applied after period $t_{DL}$	Normal Operation
D1	Spindle Brake	Normal Operation	Spindle Disabled and Brake Applied, VCM Enabled
D2	Spindle Current Limit	See Table 2.	
D3	Spindle Current Limit	See Table 2.	
D4	Idle Mode/VCM Enable	Idle: VCM Disabled and Brake Applied, Spindle Running	Normal Operation
D5	Spindle Step Mode	Normal Operation	Test Pin Becomes Single Step Commutation Clock

**TABLE 2.** Spindle Current Limit

D2	D3	Current Limit	Current Limit ( $R_{SPIN} = 17 \text{ k}\Omega$ )	Current Limit ( $R_{SPIN} = 15.7 \text{ k}\Omega$ )
0	0	$1.85 \text{ V} \cdot G_{ms}$	925 mA	1 A
0	1	$1.45 \text{ V} \cdot G_{ms}$	725 mA	780 mA
1	0	$1.05 \text{ V} \cdot G_{ms}$	525 mA	570 mA
1	1	$0.65 \text{ V} \cdot G_{ms}$	325 mA	350 mA

$G_{ms}$  = Transconductance (Refer to VCM Design Equations)

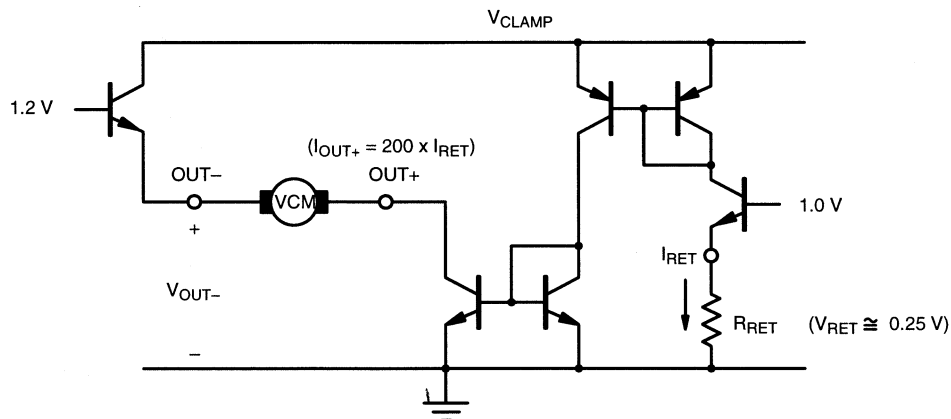


**FIGURE 1.** Write Cycle Timing Diagram

## Motor Shutdown Sequence

The Si9990ACS executes a motor shutdown sequence whenever  $V_{DD}$  drops below 3.9 V (emergency retract), or serial bit D0 is set low (sleep mode). The shutdown sequence is terminated by a programmable one-shot (brake delay). During the time-out ( $t_{DLY}$ ), both the spindle and VCM outputs are turned off. Simultaneously, a separate VCM retract circuit is activated. As shown in Figure 2, the all-bipolar design enables retract function all the way down to a supply of 1.41 V

at V<sub>CLAMP</sub> pin. The retract current typically is 20 mA, adjustable with an external resistor, R<sub>RET</sub>. To limit retract velocity, a fixed clamp limits the voltage across VCM to no more than 440 mV. After the time-out, the retract circuitry is shut off while the spindle motor and VCM brake is activated by turning on all low-side DMOS drivers. To brake faster (i.e., with lower impedance short across the motor windings) the low-side drivers are powered by the residual charges on the CHS bypass capacitor.



**FIGURE 2.** Simplified Retract Circuit

## Spindle Driver

**TABLE 3.** Spindle PWM Speed Control (Double Integrator)

System State	P <sub>U</sub>	P <sub>D</sub>	P <sub>OUT</sub>	State
Run	0	0	1	Decel
Run	0	1	Z	Hold
Run	1	0	Z	Hold
Run	1	1	0	Accel
Spindle Brake/ Sleep	X	X	0	Accel

**TABLE 4.** Spindle Commutation Sequence

Sequencer State	OUT <sub>A</sub>	OUT <sub>B</sub>	OUT <sub>C</sub>
Reset *	Z	Z	Z
1	High	Low	Z
2	High	Z	Low
3	Z	High	Low
4	Low	High	Z
5	Low	Z	High
6	Z	Low	High

\*Reset is the state after exiting sleep or spindle brake mode.

Note: X = Don't Care, Z = High Impedance

## PIN DESCRIPTION

POWER SUPPLIES		
Function	Pin Number	Description
$V_{DD}$	61	+5-V supply for VCM and spindle controller logic.
$V_{MOT}$	7, 8, 57, 58	+5-V supply for VCM and spindle drivers.
$V_{CLAMP}$	53	Inductive flyback clamp and emergency head retract power supply. This pin is shorted to $V_{MOT}$ by an on-chip switch during normal operation. The switch eliminates the need for an external Schottky diode.
AGND	24	Low noise ground return for critical analog functions
GND	3, 4, 11, 12, 36, 37, 38, 39, 42, 43	Ground return for the entire chip. All ground pins are connected to each other through the die substrate and lead frame. The large number of direct connections to the lead frame lowers thermal impedance and improves power dissipation.
CHS	56	Output of the dc-to-dc converter, used to power VCM and spindle drive MOSFETs. The converter is a 3X charge pump capable of sourcing 5 mA. An external $>0.1 \mu\text{F}$ capacitor between Pin 56 and ground is necessary.
CP2H	59	Positive side of the external 3X charge pump capacitor.
CP1H	60	Positive side of the external 2X charge pump capacitor.
CP2	54	500-kHz oscillator output, used to drive the 3X charge pump.
CP1	55	Inverted output of the on-chip 500-kHz oscillator, used to drive the external 2X charge pump capacitor.
$V_{ADIN}$	23	Low noise +5-V supply pin for the on-chip reference generator.
$V_R$	22	Output of the on-chip reference generator: $V_R = V_{ADIN}/2$ . This is used as the dc reference level for all analog signals.

VOICE COIL MOTOR DRIVER		
Function	Pin Number	Description
GAIN SELECT	2	Input pin used to select VCM transconductance. A high input sets the gain to the maximum and a low input sets the gain to be $1/4$ of the maximum.
$V_{DAC}$	16	Inverting input of servo PWM filter amplifier.
OA3	15	Output of servo PWM filter amplifier. Connect $R_C$ network from this pin to $V_{DAC}$ to set filter bandwidth. A positive OA3 relative to $V_R$ will set $V_{CM}$ output current positive.
IA4	14	Inverting input of $V_{CM}$ loop compensation amplifier.
OA4	13	Output of $V_{CM}$ loop compensation amplifier. Connect lead-lag network from this pin to IA4 to set desired loop bandwidth.
$I_{SENSE IN+}$	62	Positive input terminal for $V_{CM}$ current sense amplifier. This pin connects to external sense resistor and $V_{CM}$ .
$I_{SENSE IN-}$	63	Negative input terminal for $V_{CM}$ current sense amplifier. This pin connects to the other side of sense resistor and OUT+ pin.
$I_{SENSE OUT}$	64	Output terminal of $V_{CM}$ current sense amplifier.
OUT+	5, 6	$V_{CM}$ power amplifier positive output terminal. Current from OUT+ is positive.
OUT-	9, 10	$V_{CM}$ power amplifier negative output terminal. During head retract, $V_{CM}$ output current will be negative, or flowing from this pin into the $V_{CM}$ load.
$I_{RET}$	1	Control pin for head retract current (nominally 0.25 V). An external resistor is connected to this pin. The current is amplified 200 times at the $V_{CM}$ driver.
$C_{DLY}$	21	An external capacitor is connected to this pin to set the maximum head retract time, $t_{DLY} = 514 \text{ k}\Omega \times C_{DLY}$ . At the end of the delay, the spindle motor is set to brake. A head retract may also be forced, by asserting this pin low.





MICROCONTROLLER INTERFACE		
Function	Pin Number	Description
DATA	18	Data input for the serial port.
CLK	19	Clock input for serial port data.
CS	20	Strobe input for data word. System commands are executed at the rising edge of $\overline{CS}$ .
FAULT	17	Undervoltage flag output. Forced low if 5-V supply drops below 3.9 V, or the internal power-on reset timer (approximately 0.5 ms) is timing out.

DIAGNOSTIC FUNCTIONS		
Function	Pin Number	Description
MODE	51	Control input used for manufacture testing only. Grounded or left open during normal operation.
TEST	52	Used as temperature test or step mode clock input. Controlled by serial port.

SPINDLE MOTOR DRIVER		
Function	Pin Number	Description
F <sub>COM</sub>	27	Spindle commutation clock output. A positive going pulse is generated whenever a valid back EMF zero crossing is detected. The external speed control, working in either phase or frequency domain, compares this signal against a reference clock and feedbacks a PWM servo signal to the spindle driver via the PWM decoder and low-pass filter (A <sub>2</sub> ).
P <sub>U</sub>	49	Pulse width modulation pull-up command from speed control.
P <sub>D</sub>	50	Pulse width modulation pull-down command from speed control.
P <sub>OUT</sub>	48	Pulse width modulation output from speed control. This pin is connected to the external integrating resistor of A <sub>2</sub> . P <sub>OUT</sub> is low, or accelerating, if P <sub>U</sub> = high and P <sub>D</sub> = high. P <sub>OUT</sub> is high, or decelerating, if P <sub>U</sub> = low and P <sub>D</sub> = low. P <sub>OUT</sub> is tri-state, or holding, otherwise.
IA2	25	Inverting input of spindle PWM low-pass filter amplifier.
OA2	26	Output of spindle PWM low-pass filter amplifier. Connect RC network from this pin to IA2 to set desired cutoff frequency.
IA1	35	Inverting input of spindle loop compensation amplifier.
OA1	34	Output of spindle loop compensation amplifier. Connect RC lead-lag network from this pin to IA1 to set compensation.
R <sub>SPIN</sub>	33	Connect an accurate external resistor from this pin to OA1 to set spindle transconductance and current limit. The recommended resistance is 17 k $\Omega$ .
OUT <sub>A</sub>	46, 47	Spindle phase A output terminal.
OUT <sub>B</sub>	44, 45	Spindle phase B output terminal.
OUT <sub>C</sub>	40, 41	Spindle phase C output terminal.
CST	31	An external capacitor connected to this pin will generate commutation pulses to start up the spindle motor.
CWD	30	An external capacitor connected to this pin will disable the back EMF comparators during diode recirculation, detect incorrect motor rotation or stall.
CD1	29	Connect at this pin one of the two external capacitors used to generate the ideal commutation point from the back EMF zero crossing points.
CD2	28	Connect a second capacitor identical to CD1 at this pin to generate the optimum commutation delay.
CT	32	Spindle motor center tap input for back EMF sensing.

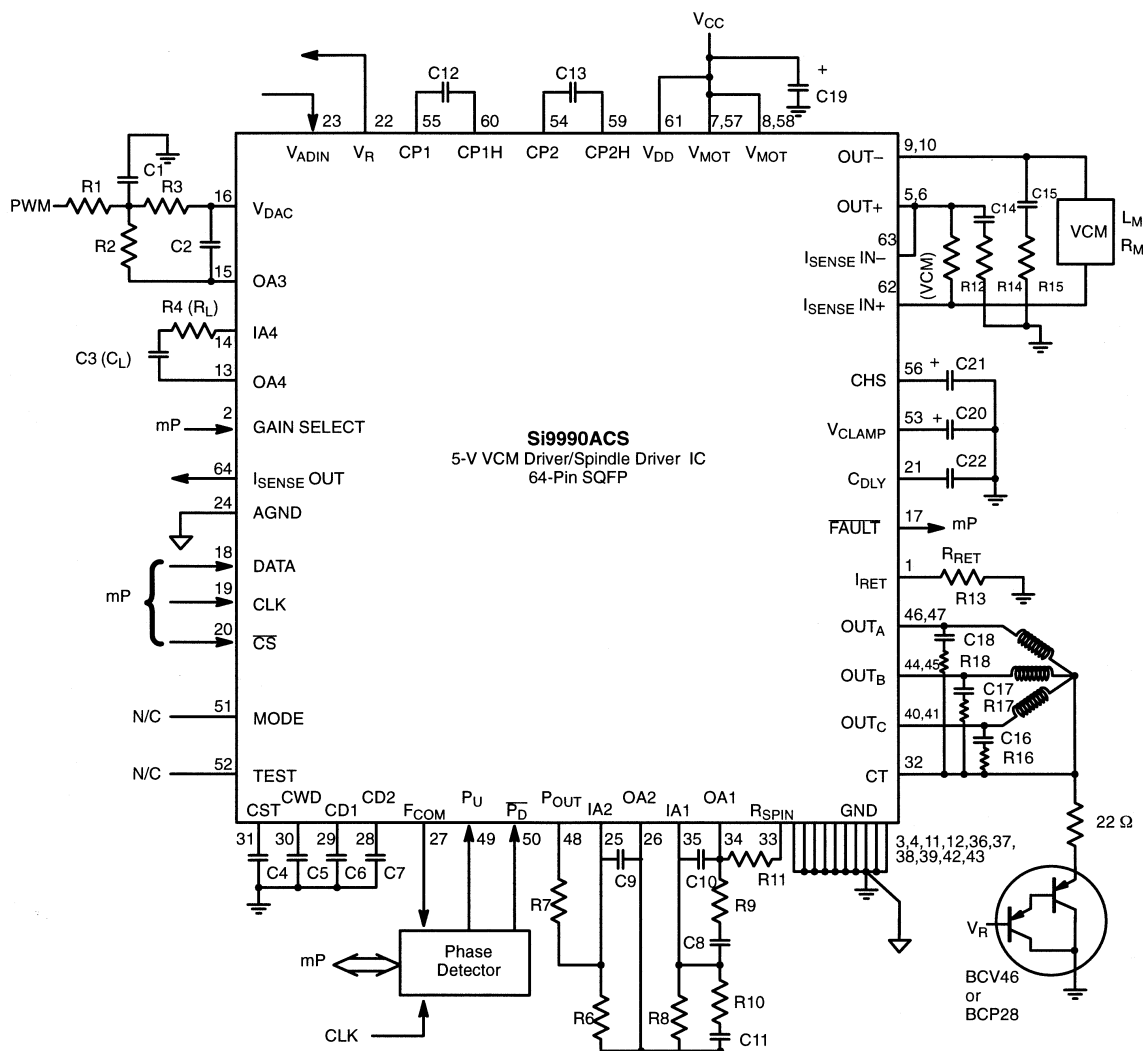
# Si9990ACS

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## APPLICATION

64-Pin SQFP test board for typical 2½" or smaller HDD (shown with external phase detector for spindle speed control and external PWM for VCM DAC)



### VCM Design Equations:

#### (1) Transconductance ( $G_{mv}$ )

$$\text{High Gain} = \frac{1}{4 R_S}; G/SEL = \text{High}$$

$$\text{Low Gain} = \frac{1}{16 R_S}; G/SEL = \text{Low}$$

#### (2) Output Retract Current

$$I_{OUT} = 200 \times I_{RET} = 200 \times \frac{0.25 V}{R_{RET}}$$

### Spindle Design Equation:

$$\text{Transconductance } (G_{ms}) = \frac{8700}{R_{SPIN}}$$

#### (3) Transconductance Loop Compensation

$$\text{Closed-Loop BW} = \frac{4(16)}{2 \pi (10 K) C_L} \left( \frac{R_S}{R_M + R_S} \right)$$

$$C_L = \frac{64}{2 \pi (10 K) BW} \left( \frac{R_S}{R_M + R_S} \right)$$

or

$$R_L = \frac{L_M}{C_L (R_M + R_S)}$$

$R_M$  = Motor Resistance

$L_M$  = Motor Inductance

(4) Refer to AN93-1 for all servo equations.



## APPLICATION

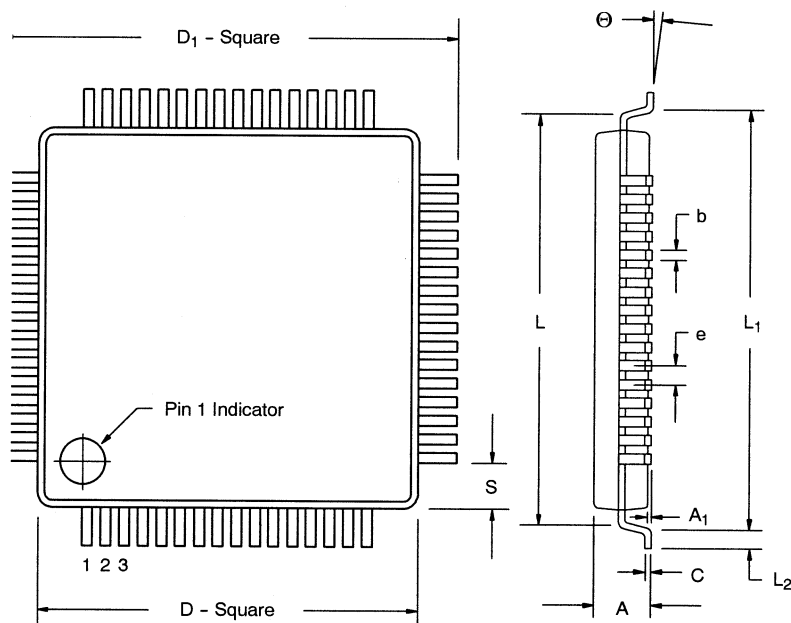
TABLE 5. Components for Test Board

Name	Value	Comments
R1	100 k	VCM PWM Low Pass Filter
R2	100 k	VCM PWM Low Pass Filter
R3	100 k	VCM PWM Low Pass Filter
R4	2.61 k	VCM Transconductance Amplifier Compensator
R6	39 k	Spindle PWM Low Pass Filter
R7	110 k	Spindle PWM Low Pass Filter
R8	5.6 M	Spindle Speed Control Lead-Lag Compensator
R9	910 k	Spindle Speed Control Lead-Lag Compensator
R10	470 k	Spindle Speed Control Lead-Lag Compensator
R11	17 k	R <sub>SPIN</sub> Resistor
R12	1.67	VCM Sense Resistor
R13	2.5 k	VCM Retract Bias Resistor (R <sub>RET</sub> )
R14	30	VCM Snubber Resistor
R15	30	VCM Snubber Resistor
R16	62	Spindle Snubber Resistor
R17	62	Spindle Snubber Resistor
R18	62	Spindle Snubber Resistor
C1	1.2 nF	VCM PWM Low Pass Filter
C2	100 pF	VCM PWM Low Pass Filter
C3	18 nF	VCM Transconductance Amplifier Compensator

Name	Value	Comments
C4	27 nF	Spindle Start-Up Capacitor
C5	680 pF	Spindle Watch-Dog Capacitor
C6	1.8 nF	Spindle Commutation Delay Capacitor #1
C7	1.8 nF	Spindle Commutation Delay Capacitor #2
C8	0.22 nF	Spindle Loop 'Zero' Capacitor
C9	2.7 nF	Spindle PWM Low Pass Filter
C10	2.2 nF	Spindle Speed Control Lead-Lag Compensator
C11	10 nF	Spindle Speed Control Lead-Lag Compensator
C12	82 nF	Charge Pump Capacitor #1
C13	82 nF	Charge Pump Capacitor #2
C14	100 nF	VCM Snubber Capacitor
C15	100 nF	VCM Snubber Capacitor
C16	180 nF	Spindle Snubber Capacitor
C17	180 nF	Spindle Snubber Capacitor
C18	180 nF	Spindle Snubber Capacitor
C19	≥ 0.1 μF	Bypass Capacitor
C20	≥ 0.1 μF	Bypass Capacitor
C21	≥ 0.1 μF	Bypass Capacitor
C22	180 nF	Brake Delay Capacitor (C <sub>DLY</sub> )

Note: These values are entirely dependent on motor characteristics.

## PACKAGE OUTLINE: SQFP 64-PIN



Dim	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.60	0.053	0.063
A <sub>1</sub>	0.04	0.16	0.002	0.006
b	0.14	0.26	0.006	0.010
C	0.117	0.177	0.005	0.007
D	9.90	10.10	0.390	0.398
D <sub>1</sub>	11.7	12.3	0.461	0.484
e	0.40	0.60	0.016	0.024
L	-	10.80	-	0.425
L <sub>1</sub>	10.80	11.20	0.425	0.441
L <sub>2</sub>	0.30	0.70	0.012	0.028
S	-	1.20	-	0.047
θ	0°	4°	0°	4°

\*For Reference Only