INITIAL RELEASE
Final Electrical Specifications

LT1714

7ns, Low Power, 3V/5V Dual Rail-to-Rail Comparator

June 2000

FEATURES

- **Ultrafast: 7ns at 20mV Overdrive**
  8.5ns at 5mV Overdrive
- **Input Common Mode Extends Beyond Supplies**
- **Specified at Single 2.7V or 5V Supply or ±5V**
- TTL/CMOS Compatible Rail-to-Rail Outputs
- Low Power (Per Comparator): 5mA
- Dual Output Latch Capability
- Inputs Can Exceed Supplies Without Phase Reversal
- Available in 16-Lead Narrow SSOP

APPLICATIONS

- High Speed Automatic Test Equipment
- Current Sense for Switching Regulators
- Crystal Oscillator Circuits
- High Speed Sampling Circuits
- High Speed A/D Converters
- Pulse Width Modulators
- Window Comparators
- Extended Range V/F Converters
- Fast Pulse Height/Width Discriminators
- Line Receivers
- High Speed Triggers

DESCRIPTION

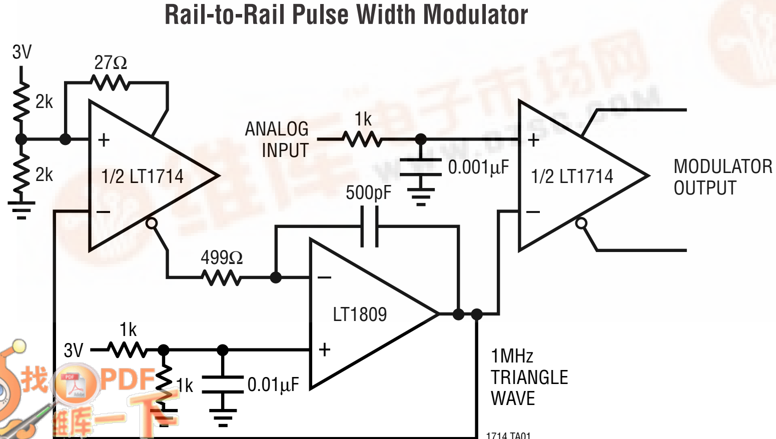
The LT®1714 is an UltraFast™ 7ns dual comparator featuring rail-to-rail inputs, complementary rail-to-rail outputs and dual internal output latches. Optimized for 3V and 5V power supplies, it operates over a single supply voltage range from 2.4V to 12V or from ±2.4V to ±6V dual supplies.

The LT1714 is designed for ease of use in a variety of systems. In addition to the wide supply voltage flexibility, the rail-to-rail input common mode range extends 100mV beyond both supply rails, and the outputs are protected against phase reversal for inputs extending further beyond the rails. Also, the rail-to-rail inputs may be taken to opposite rails with no significant increase in input current. The rail-to-rail matched complementary outputs interface directly to TTL or CMOS logic and can sink 10mA to within 0.5V of GND or source 10mA to within 0.7V of V^+.

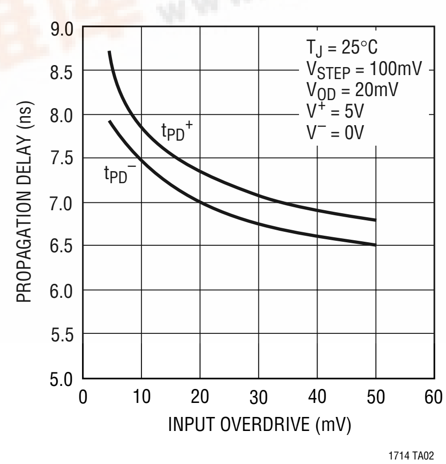
The LT1714 has dual internal TTL/CMOS compatible latches for retaining data at the outputs. The latch holds data as long as the latch pin is held high. Latch pin hysteresis provides protection against slow moving or noisy latch signals. The LT1714 is available in the 16-pin narrow SSOP.

TYPICAL APPLICATION

Rail-to-Rail Pulse Width Modulator



Propagation Delay vs Input Overdrive



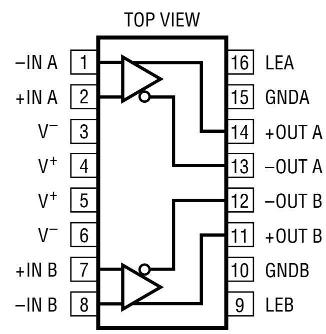
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V^+ to V^- 12.6V
- V^+ to GND 12.6V
- V^- to GND ....−10V to 0.3V

Differential Input Voltage .... ±12.6V
Latch Pin Voltage 7V
Input and Latch Current .... ±10mA
Output Current (Continuous) .... ±20mA
Operating Temperature Range .... −40°C to 85°C
Specified Temperature Range (Note 2) ... −40°C to 85°C
Junction Temperature .... 150°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

$T_{JMAX} = 150°C, \theta_{JA} = 150°C/W$

ORDER PART NUMBER
LT1714CGN LT1714IGN
GN PART MARKING
1714 1714I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25°C$. $V^+ = 5V$, $V^- = -5V$, $V_{CM} = 0V$, $V_{LATCH} = 0.8V$, $V_{OVERDRIVE} = 20mV$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Positive Supply Voltage Range		●	2.4		7	V
V^-	Negative Supply Voltage Range (Note 3)		●	−7		0	V
V_{OS}	Input Offset Voltage (Note 4)	$R_S = 50\Omega$, $V_{CM} = 0V$			1.0	3.0	mV
		$R_S = 50\Omega$, $V_{CM} = 0V$	●			4.0	mV
		$R_S = 50\Omega$, $V_{CM} = -5V$			1.0	3.5	mV
		$R_S = 50\Omega$, $V_{CM} = 5V$			2.0	5.0	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		5		µV/°C
I_{OS}	Input Offset Current				0.1	1	µA
			●			2	µA
I_B	Input Bias Current (Note 5)			−7	−1.5	2	µA
			●	−15		5	µA
V_{CM}	Input Voltage Range		●	−5.1		5.1	V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 5V$		62	70		dB
			●	60			dB
$PSRR^+$	Positive Power Supply Rejection Ratio	$2.4V \le V^+ \le 7V$, $V_{CM} = -5V$		68	80		dB
			●	65			dB
$PSRR^-$	Negative Power Supply Rejection Ratio	$-7V \le V^- \le 0V$, $V_{CM} = 5V$		65	80		dB
			●	60			dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 4V$, $R_L = \infty$		5	25		V/mV
V_{OH}	Output Voltage Swing HIGH (Note 8)	$I_{OUT} = 1mA$	●	4.5	4.8		V
		$I_{OUT} = 10mA$	●	4.3	4.6		V
V_{OL}	Output Voltage Swing LOW (Note 8)	$I_{OUT} = -1mA$	●		0.20	0.4	V
		$I_{OUT} = -10mA$	●		0.35	0.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 5V, V^- = –5V, V_{CM} = 0V, V_{LATCH} = 0.8V, C_{OUT} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I^+	Positive Supply Current (Per Comparator)				5.5	7.5	mA
			●			9.0	mA
I^-	Negative Supply Current (Per Comparator)				3.5	4.5	mA
			●			5.0	mA
V_{IH}	Latch Pin High Input Voltage		●	2			V
V_{IL}	Latch Pin Low Input Voltage		●			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = 5V	●			10	µA
t_{PD}	Propagation Delay (Note 6)	ΔV_{IN} = 100mV, V_{OD} = 20mV			7	10	ns
		ΔV_{IN} = 100mV, V_{OD} = 20mV	●			12	ns
		ΔV_{IN} = 100mV, V_{OD} = 5mV			8.5		ns
Δt_{PD}	Differential Propagation Delay (Note 6)	ΔV_{IN} = 100mV, V_{OD} = 20mV			0.5	3	ns
t_r	Output Rise Time	10% to 90%			4		ns
t_f	Output Fall Time	90% to 10%			4		ns
t_{LPD}	Latch Propagation Delay (Note 7)				8		ns
t_{SU}	Latch Setup Time (Note 7)				1.5		ns
t_H	Latch Hold Time (Note 7)				0		ns
t_{DPW}	Minimum Latch Disable Pulse Width (Note 7)				8		ns
f_{MAX}	Maximum Toggle Frequency	V_{IN} = 100mV_{P-P} Sine Wave			65		MHz
t_{JITTER}	Output Timing Jitter	V_{IN} = 630mV_{P-P} (0dBm) Sine Wave, f = 30MHz			15		ps

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 2.7V or V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_{LATCH} = 0.8V, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Positive Supply Voltage Range		●	2.4		7	V
V_{OS}	Input Offset Voltage (Note 4)	R_S = 50Ω, V_{CM} = 2.5V, V^+ = 5V			1.0	3.0	mV
		R_S = 50Ω, V_{CM} = 0V, V^+ = 5V			1.0	3.5	mV
		R_S = 50Ω, V_{CM} = 5V, V^+ = 5V			1.5	5.0	mV
		R_S = 50Ω, V_{CM} = 1.35V, V^+ = 2.7V			1.0	4.0	mV
		R_S = 50Ω, V_{CM} = 0V, V^+ = 2.7V			1.0	3.5	mV
		R_S = 50Ω, V_{CM} = 2.7V, V^+ = 2.7V			1.5	5.0	mV
		R_S = 50Ω, V_{CM} = 2.5V, V^+ = 5V	●			4.0	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		5		µV/°C
I_{OS}	Input Offset Current				0.1	1	µA
			●			2	µA
I_B	Input Bias Current (Note 5)			–6	–1.5	2	µA
			●	–12		3	µA
V_{CM}	Input Voltage Range (Note 9)		●	–0.1		V^+ + 0.1	V
CMRR	Common Mode Rejection Ratio	V^+ = 5V, 0V ≤ V_{CM} ≤ 5V		60	70		dB
		V^+ = 5V, 0V ≤ V_{CM} ≤ 5V	●	58			dB
		V^+ = 2.7V, 0V ≤ V_{CM} ≤ 2.7V		57	70		dB
		V^+ = 2.7V, 0V ≤ V_{CM} ≤ 2.7V	●	55			dB
$PSRR^+$	Positive Power Supply Rejection Ratio	2.4V ≤ V^+ ≤ 7V, V_{CM} = 0V		65	80		dB
			●	60			dB
$PSRR^-$	Negative Power Supply Rejection Ratio	–7V ≤ V^- ≤ 0V, V^+ = 5V, V_{CM} = 5V		65	80		dB
			●	60			dB
A_V	Small-Signal Voltage Gain	1V ≤ V_{OUT} ≤ 4V, R_L = ∞		5	25		V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V^+ = 2.7V or V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_{LATCH} = 0.8V, C_{OUT} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output Voltage Swing HIGH	I_{OUT} = 1mA, V^+ = 5V I_{OUT} = 10mA, V^+ = 5V I_{OUT} = 1mA, V^+ = 2.7V I_{OUT} = 10mA, V^+ = 2.7V	● ● ● ●	4.5 4.3 2.2 2.0	4.80 4.60 2.45 2.30		V V V V
V_{OL}	Output Voltage Swing LOW	I_{OUT} = –1mA I_{OUT} = –10mA	● ●		0.20 0.35	0.4 0.5	V V
I^+	Positive Supply Current (Per Comparator)	V^+ = 5V	 ●		5	6.5 8.0	mA mA
I^-	Negative Supply Current (Per Comparator)	V^+ = 5V	 ●		3	4.0 4.5	mA mA
V_{IH}	Latch Pin High Input Voltage		●	2			V
V_{IL}	Latch Pin Low Input Voltage		●			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = V^+	●			10	µA
t_{PD}	Propagation Delay (Note 6)	ΔV_{IN} = 100mV, V_{OD} = 20mV, V^+ = 5V ΔV_{IN} = 100mV, V_{OD} = 20mV, V^+ = 5V ΔV_{IN} = 100mV, V_{OD} = 5mV, V^+ = 5V ΔV_{IN} = 100mV, V_{OD} = 20mV, V^+ = 2.7V ΔV_{IN} = 100mV, V_{OD} = 20mV, V^+ = 2.7V ΔV_{IN} = 100mV, V_{OD} = 5mV, V^+ = 2.7V	 ● ● 		8.0 9.0 8.0 9.0	10.5 12.0 11.0 12.5 	ns ns ns ns ns ns
Δt_{PD}	Differential Propagation Delay (Note 6)	ΔV_{IN} = 100mV, V_{OD} = 20mV			0.5	3	ns
t_r	Output Rise Time	10% to 90%			4		ns
t_f	Output Fall Time	90% to 10%			4		ns
t_{LPD}	Latch Propagation Delay (Note 7)				8		ns
t_{SU}	Latch Setup Time (Note 7)				1.5		ns
t_H	Latch Hold Time (Note 7)				0		ns
t_{DPW}	Minimum Latch Disable Pulse Width (Note 7)				8		ns
f_{MAX}	Maximum Toggle Frequency	V_{IN} = 100mV_{P-P} Sine Wave			65		MHz
t_{JITTER}	Output Timing Jitter	V_{IN} = 630mV_{P-P} (0dBm) Sine Wave, f = 30MHz			15		ps

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1714C and LT1714I are guaranteed to meet specified performance from 0°C to 70°C. The LT1714C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1714I is guaranteed to meet specified performance from –40°C to 85°C.

Note 3: The negative supply should not be greater than the ground pin voltages and the maximum voltage across the positive and negative supplies should not be greater than 12V.

Note 4: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to V^+/2.

Note 5: Input bias current (I_B) is defined as the average of the two input currents.

Note 6: Propagation delay (t_{PD}) is measured with the overdrive added to the actual V_{OS}. Differential propagation delay is defined as: $\Delta t_{PD} = t_{PD}^+ - t_{PD}^-$. Load capacitance is 10pF. Due to test system requirements, the LT1714 propagation delay is specified with a 1kΩ load to ground for ±5V supplies, or to mid-supply for 2.7V or 5V single supplies.

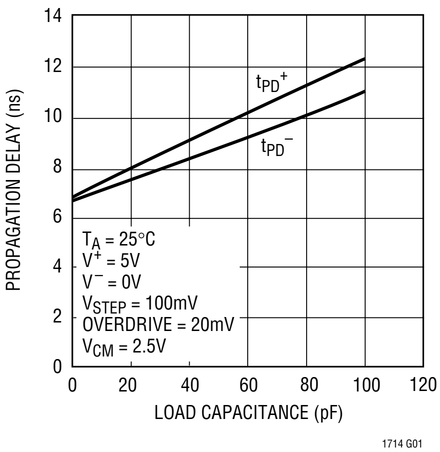
Note 7: Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the latch pin is deasserted. Latch setup time (t_{SU}) is the interval in which the input signal must remain stable prior to asserting the latch signal. Latch hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable. Latch disable pulse width (t_{DPW}) is the width of the negative pulse on the latch enable pin that latches in new data on the data inputs.

Note 8: Output voltage swings are characterized and tested at V^+ = 5V and V^- = 0V. They are designed and expected to meet these same specifications at V^- = –5V.

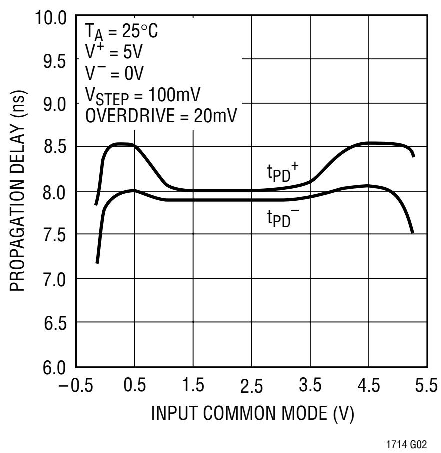
Note 9: The input voltage range is tested under the more demanding conditions of V^+ = 5V and V^- = –5V. The LT1714 is designed and expected to meet these specifications at V^- = 0V.

TYPICAL PERFORMANCE CHARACTERISTICS

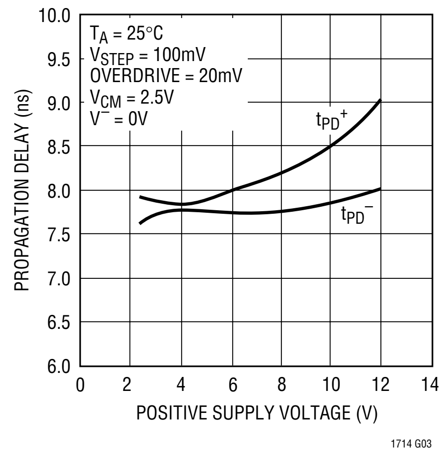
Propagation Delay vs Load Capacitance



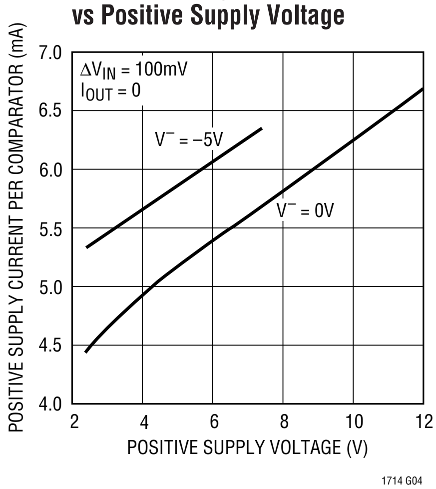
Propagation Delay vs Input Common Mode Voltage



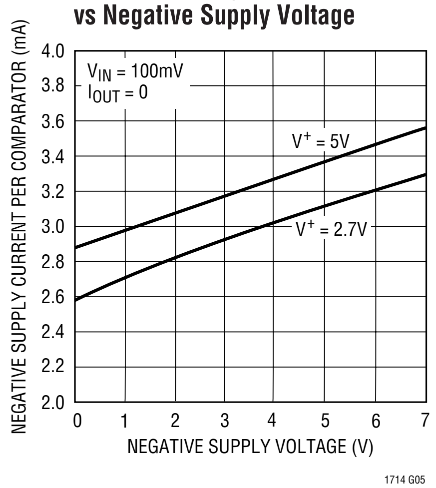
Propagation Delay vs Positive Supply Voltage



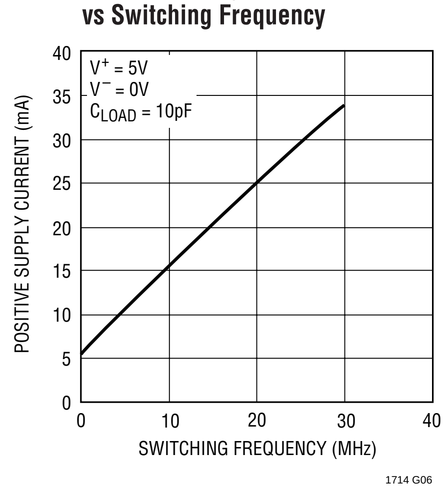
Positive Supply Current vs Positive Supply Voltage



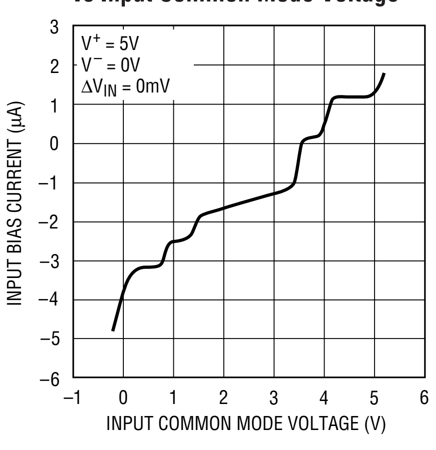
Negative Supply Current vs Negative Supply Voltage



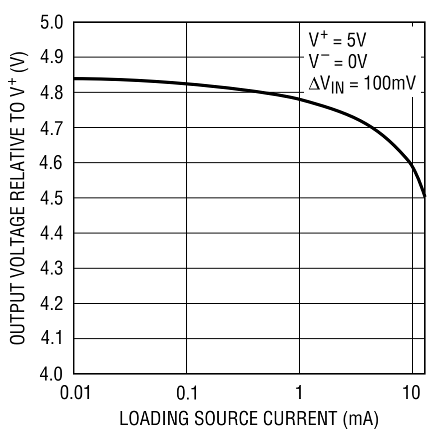
Positive Supply Current vs Switching Frequency



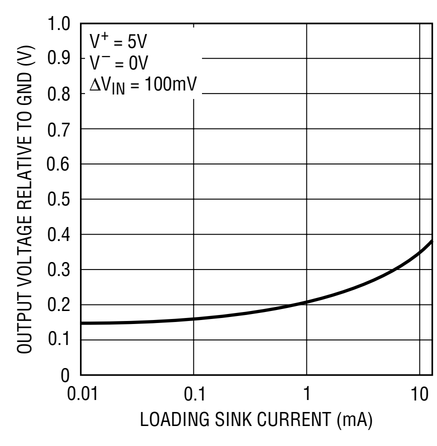
Input Bias Current vs Input Common Mode Voltage



Output High Voltage vs Source Current

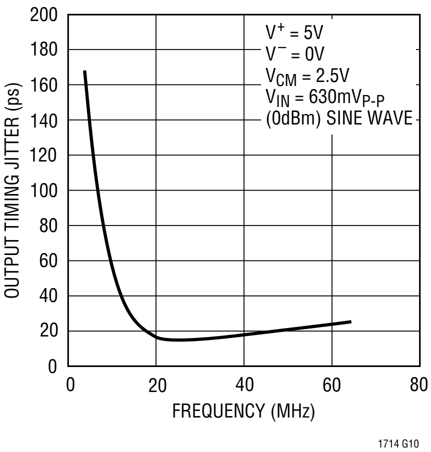


Output Low Voltage vs Sink Current

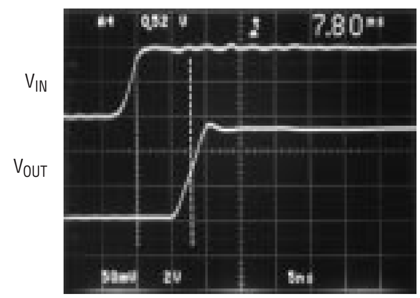


TYPICAL PERFORMANCE CHARACTERISTICS

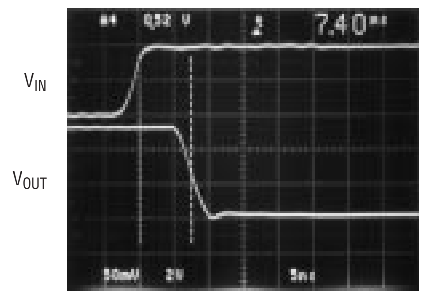
Output Timing Jitter vs Switching Frequency



Output Rising Edge



Output Falling Edge



PIN FUNCTIONS

–IN A (Pin 1): Inverting Input of A Channel Comparator.

+IN A (Pin 2): Noninverting Input of A Channel Comparator.

V^- (Pins 3, 6): Negative Supply Voltage, Usually –5V. Pins 3 and 6 should be connected together externally.

V^+ (Pins 4, 5): Positive Supply Voltage, Usually 5V. Pins 4 and 5 should be connected together externally.

+IN B (Pin 7): Noninverting Input of B Channel Comparator.

–IN B (Pin 8): Inverting Input of B Channel Comparator.

LEB (Pin 9): Latch Enable Input of B Channel Comparator.

GNDB (Pin 10): Ground Supply Voltage of B Channel Comparator, Usually 0V.

+OUT B (Pin 11): Noninverting Output of B Channel Comparator.

–OUT B (Pin 12): Inverting Output of B Channel Comparator.

–OUT A (Pin 13): Inverting Output of A Channel Comparator.

+OUT A (Pin 14): Noninverting Output of A Channel Comparator.

GNDA (Pin 15): Ground Supply Voltage of A Channel Comparator, Usually 0V

LEA (Pin 16): Latch Enable Input of A Channel Comparator.

APPLICATIONS INFORMATION

Common Mode Considerations

The LT1714 is specified for a common mode range of –5.1V to 5.1V on a ±5V supply, or a common mode range of –0.1V to 5.1V on a single 5V supply. A more general consideration is that the common mode range is from 100mV below the negative supply to 100mV above the positive supply, independent of the actual supply voltage. The criteria for common mode limit is that the output still responds correctly to a small differential input signal.

When either input signal falls outside the common mode limit, the internal PN diode formed with the substrate can turn on resulting in significant current flow through the die. Schottky clamp diodes between the inputs and the supply rails speed up recovery from excessive overdrive conditions by preventing these substrate diodes from turning on.

Input Bias Current

Input bias current is measured with the outputs held at 2.5V with a 5V supply voltage. As with any rail-to-rail differential input stage, the LT1714 bias current flows into or out of the device depending upon the common mode level. The input circuit consists of an NPN pair and a PNP pair. For inputs near the negative rail, the NPN pair is inactive, and the input bias current flows out of the device; for inputs near the positive rail, the PNP pair is inactive, and these currents flow into the device. For inputs far enough away from the supply rails, the input bias current will be some combination of the NPN and PNP bias currents. As the differential input voltage increases, the input current of each pair will increase for one of the inputs and decrease for the other input. Large differential input voltages result in different input currents as the input stage enters various regions of operation. To reduce the influence of these changing input currents on system operation, use a low source resistance.

Latch Pin Dynamics

The internal latches of both LT1714 comparators retain the input data (output latched) when their respective latch pin goes high. Each latch pin will float to a low state when disconnected, but it is better to ground the latch when a flow-through condition is desired. The latch pin is designed to be driven with either a TTL or CMOS output. It has built-in hysteresis of approximately 100mV, so that slow moving or noisy input signals do not impact latch performance. If only one of the comparators is being used at a given time, it is best to latch the second comparator to avoid any possibility of interactions between the comparators in the same package.

High Speed Design Techniques

A substantial amount of design effort has made the LT1714 relatively easy to use. As with most high speed comparators, careful attention to PC board layout and design is important in order to prevent oscillations. The most common problem involves power supply bypassing which is necessary to maintain low supply impedance. Resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels, thereby allowing the supply voltages to move as the supply current changes. This movement of the supply voltages will often result in improper operation. In addition, adjacent devices connected through an unbypassed supply can interact with each other through the finite supply impedances.

Bypass capacitors furnish a simple solution to this problem by providing a local reservoir of energy at the device, thus keeping supply impedance low. Bypass capacitors should be as close as possible to the LT1714 supply pins. A good high frequency capacitor, such as a 0.1μF ceramic, is recommended in parallel with a larger capacitor, such as a 4.7μF tantalum.

Poor trace routes and high source impedances are also common sources of problems. Keep trace lengths as short as possible and avoid running any output trace adjacent to an input trace to prevent unnecessary coupling. If output traces are longer than a few inches, provide proper termination impedances (typically 100Ω to 400Ω) to eliminate any reflections that may occur. Also keep source impedances as low as possible, preferably less than 1kΩ.

The input and output traces should also be isolated from one another. Power supply traces can be used to achieve this isolation as shown in Figure 1, a typical topside layout of the LT1714 on a multilayer PC board. Shown is the topside metal etch including traces, pin escape vias and

APPLICATIONS INFORMATION

the land pads for a GN16 LT1714 and its adjacent X7R 0805 10nF bypass capacitors. The V^+, V^- and GND traces all shield the inputs from the outputs. Although the two V^- pins are connected internally, they should be shorted together externally as well in order for both to function as shields. The same is true for the two V^+ pins. The two GND pins are not connected internally, but in most applications they are both connected directly to the ground plane.

Another useful technique to avoid oscillations is to provide positive feedback, also known as hysteresis, from the output to the input. Increased levels of hysteresis, however, reduce the sensitivity of the device to input voltage levels, so the amount of positive feedback should be tailored to particular system requirements. The LT1714 is completely flexible regarding the application of hysteresis, due to rail-to-rail inputs and the complementary outputs. Specifically, feedback resistors can be connected from one or both outputs to their corresponding inputs without regard to common mode considerations. Figure 2 shows several configurations.

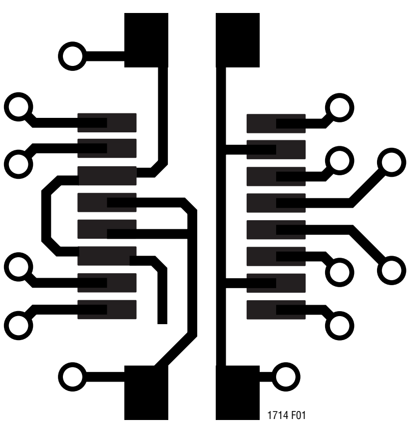


Figure 1. Typical Topside Metal for Multilayer PCB Layout

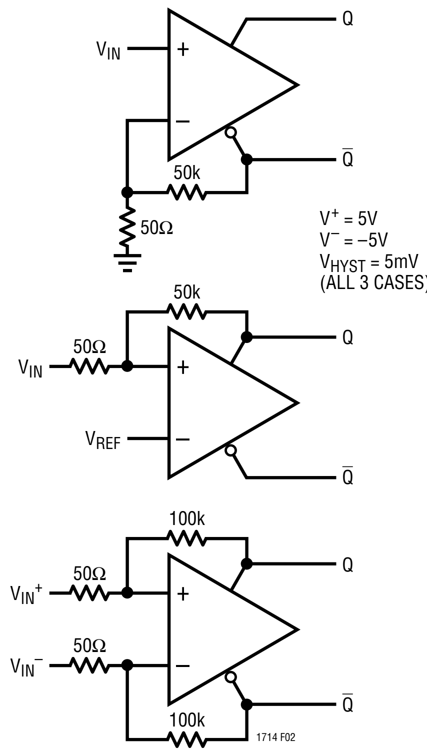


Figure 2. Various Configurations for Introducing Hysteresis

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	UltraFast Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground Sensing Comparator	Single Supply Version of the LT1016
LT1394	7ns, UltraFast Single Supply Comparator	6mA Single Supply Comparator
LT1671	60ns, Low Power, Single Supply Comparator	450μA Single Supply Comparator
LT1719	4.5ns, Single Supply 3V/5V Comparator	4mA Comparator with Rail-to-Rail Outputs
LT1720/LT1721	Dual/Quad, 4.5ns, Single Supply Comparator	Dual/Quad Version of the LT1719