



MX23C8111

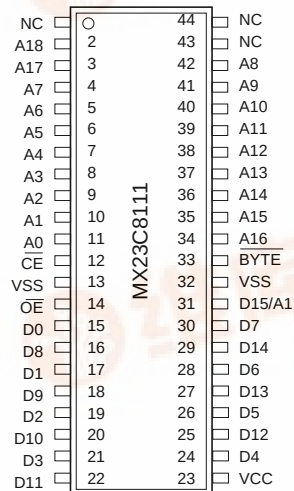
8M-BIT MASK ROM (8/16 BIT OUTPUT)

FEATURES

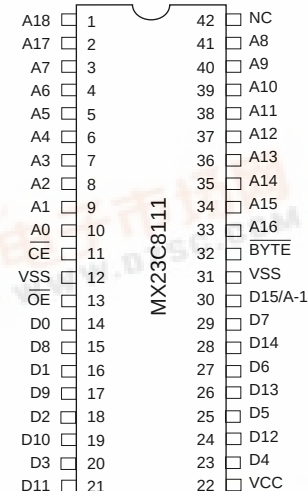
- Bit organization
 - 1M x 8 (byte mode)
 - 512K x 16 (word mode)
- Fast access time
 - Random access: 95ns (max.)
 - Page access: 50ns (max.)
- Current
 - Operating: 60mA
 - Standby: 100uA
- Supply voltage
 - 5V±10%
- Package
 - 44 pin SOP (500mil)
 - 42 pin PDIP (600mil)

PIN CONFIGURATION

44 SOP



42 PDIP



ORDER INFORMATION

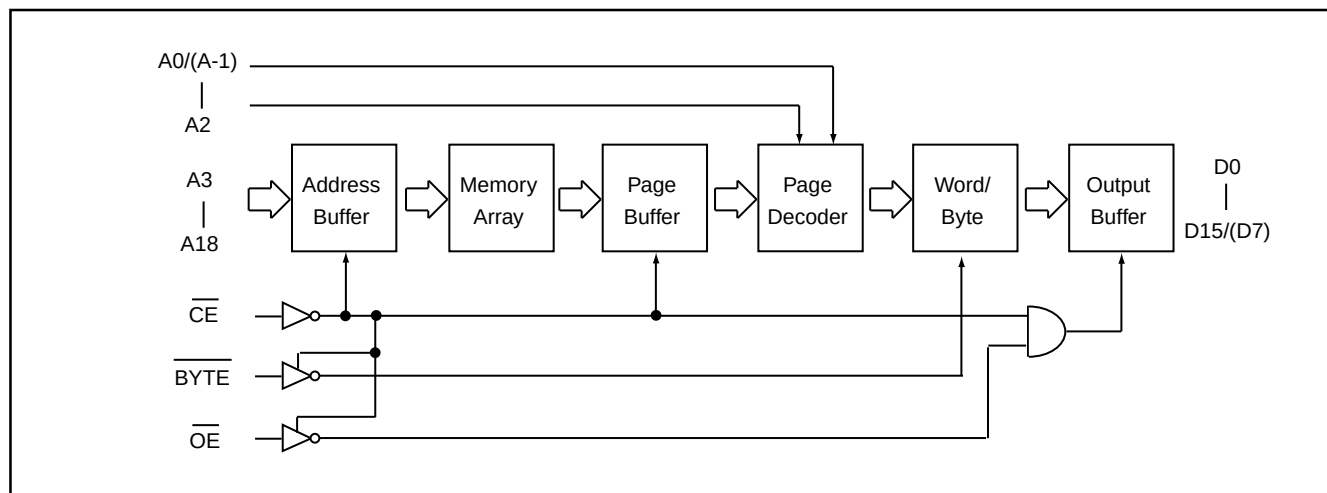
Part No.	Access Time	Page Access Time	Package
MX23C8111MC-95	95ns	50ns	44 pin SOP
MX23C8111MC-10	100ns	50ns	44 pin SOP
MX23C8111MC-12	120ns	60ns	44 pin SOP
MX23C8111PC-95	95ns	50ns	42 pin PDIP
MX23C8111PC-10	100ns	50ns	42 pin PDIP
MX23C8111PC-12	120ns	60ns	42 pin PDIP

PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D7	Data Outputs
CE	Chip Enable Input
OE	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

MODE SELECTION

CE	OE	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VCC	-0.3V to 7.0V
Input Voltage	VI	-0.3V to VCC + 0.5V
Output Voltage	VO	-0.3V to VCC + 0.5V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC1	-	60mA	f=10MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{\text{CE}}$ =VIH
Standby Current (CMOS)	ISTB2	-	100uA	$\overline{\text{CE}}$ > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ



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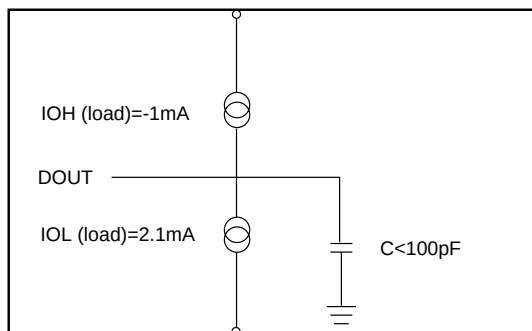
AC CHARACTERISTICS (Ta = 0 °C ~ 70 °C, VCC = 5V±10%)

Item	Symbol	23C8111-95		23C8111-10		23C8111-12	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	95ns	-	100ns	-	120ns	-
Address Access Time	tAA	-	90ns	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	95ns	-	100ns	-	120ns
Page Mode Access Time	tPA	-	50ns	-	50ns	-	60ns
Output Enable Time	tOE	-	50ns	-	50ns	-	60ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from $\overline{\text{OE}}$ or $\overline{\text{CE}}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0.4V~2.7V for 95ns and 100ns speed grade 0.4V~2.4V for 120ns speed grade
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



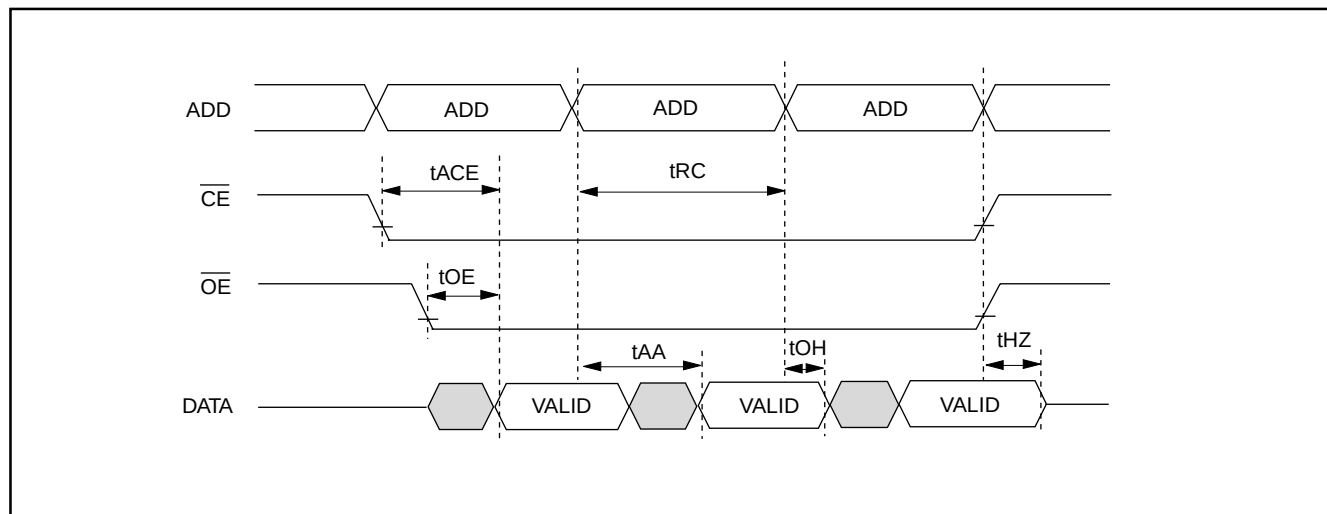
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

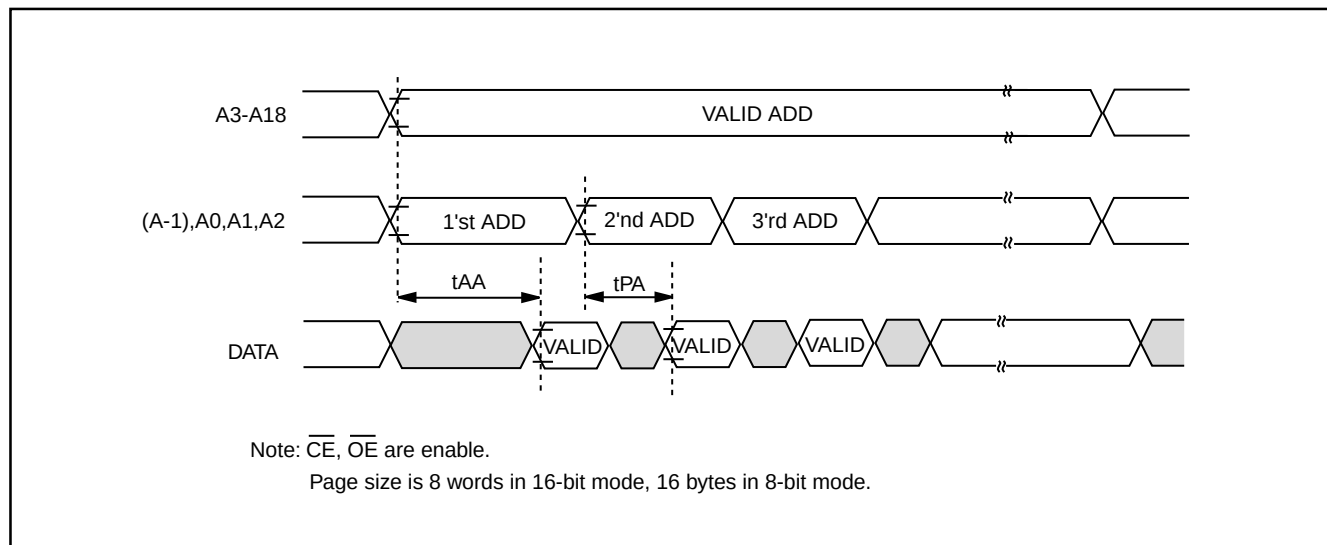
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

Access Timing (Normal Access)



Page Read





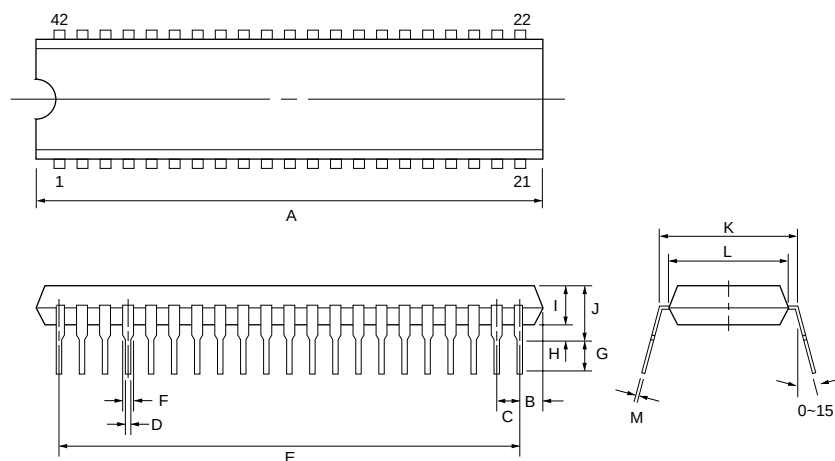
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PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	0.76 [REF]	.030 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	50.76	2.000
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

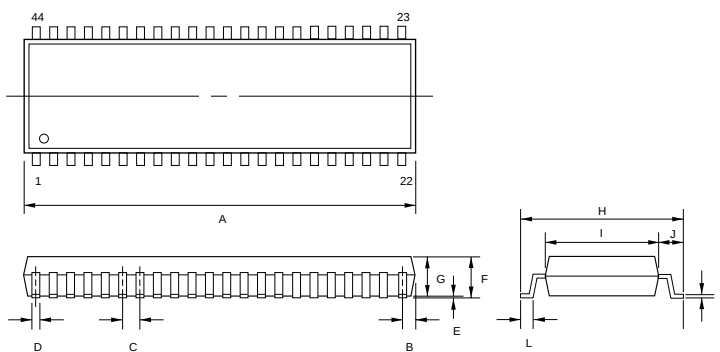
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



44-PIN PLASTIC SOP

ITEM	MILLIMETERS	INCHES
A	28.70 max.	1.130 max.
B	1.10 [REF]	.043 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 ± .10 [Typ.]	.016 ± .004 [Typ.]
E	.010 min.	.004 min.
F	3.00 max.	.118 max.
G	2.80 ± .13	.110 ± .005
H	16.04 ± .30	.631 ± .012
I	12.60	.496
J	1.72	.068
K	.15 ± .10 [Typ.]	.006 ± .004 [Typ.]
L	.80 ± .20	.031 ± .008

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.





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REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
2.1	AC Characteristics: tOH 10ns --> 0ns	P3	JAN/29/1999



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MACRONIX INTERNATIONAL Co., LTD.

HEADQUARTERS:

TEL: +886-3-578-8888

FAX: +886-3-578-8887

EUROPE OFFICE:

TEL: +32-2-456-8020

FAX: +32-2-456-8021

JAPAN OFFICE:

TEL: +81-44-246-9100

FAX: +81-44-246-9105

SINGAPORE OFFICE:

TEL: +65-747-2309

FAX: +65-748-4090

TAIPEI OFFICE:

TEL: +886-3-509-3300

FAX: +886-3-509-2200

MACRONIX AMERICA, INC.

TEL: +1-408-453-8088

FAX: +1-408-453-8488

CHICAGO OFFICE:

TEL: +1-847-963-1900

FAX: +1-847-963-1909

[http : //www.macronix.com](http://www.macronix.com)
