MX25L4004

4M-BIT [4M x 1] CMOS SERIAL FLASH EEPROM

FEATURES

- Low voltage operation: 2.7V ~ 3.6V
- SPI Bus compatible
- Sector erase architecture:
  - 1024 equal sectors of 536 bytes each
  - Sector erase time: 8ms typical
- Page program operation:
  - Internal data latches for 134 bytes per page
  - Page programming time: 3ms typical
- Auto Erase and Auto Program algorithms:
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page
- Four independently protected sectors on the top for boot code storage

- Status register feature for detection of
  - Program or erase cycle completion
  - Array to Buffer transfer
  - Sleep
  - Auto Program/Erase error report
- Six extra bytes on each page for user page management
- Dual buffers for buffer write when chip is busy
- Input data format:
  - 1-byte OP code, 2-byte sector address, 1-byte page number, 1-byte byte address
- 32-pin TSOP TYPE(I)

GENERAL DESCRIPTION

The MX25L4004 is a CMOS 4,390,912 bit serial Flash EEPROM, which is configured as 548,864 x 8 internally. The MX25L4004 features a serial peripheral interface and software protocal allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by $\overline{CS}$ input.

The MX25L4004 features sector protected and unprotected modes, which disable/enable both program and erase operation in the top four sectors.

After program/erase command is issued, auto program/ erase algorithms which program/erase and verify the specified sector/page locations will be executed. Program command is executed on a page (134 bytes) basis, and erase command is executed on a sector (536 bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

When the device is not in operation and $\overline{CS}$ is high, it is put in standby mode and draws less than 30uA DC current. To save power further, the device may be put into sleep mode. During sleep mode, the device only draws 1uA DC current. Recovery time from sleep mode is less than 25us.

The MX25L4004 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 10,000 program and erase cycles.

PIN CONFIGURATIONS

32 TSOP(I)

SCLK — 2
SO — 3
VCC — 4

CS — 13
SI — 14
VSS — 15

32 TEST
31 PROT
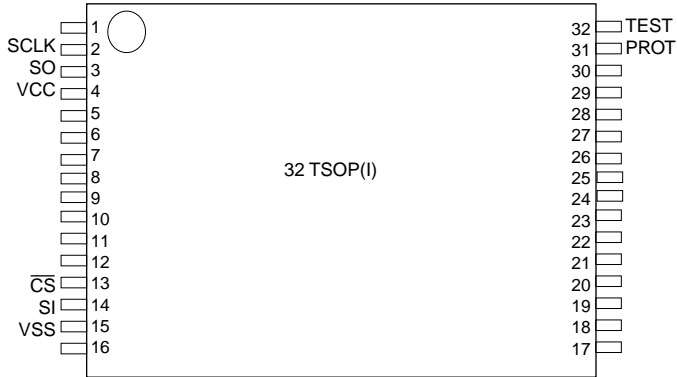
PIN DESCRIPTION

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select
TEST	Test Mode Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
PROT	Protection Enable
VCC	+ 3.0V Power Supply
VSS	Ground
All other pins	Not Connected

Note:
1.TEST input is used for in-house tesing and must be tied to ground during normal user operation.

BLOCK DIAGRAM
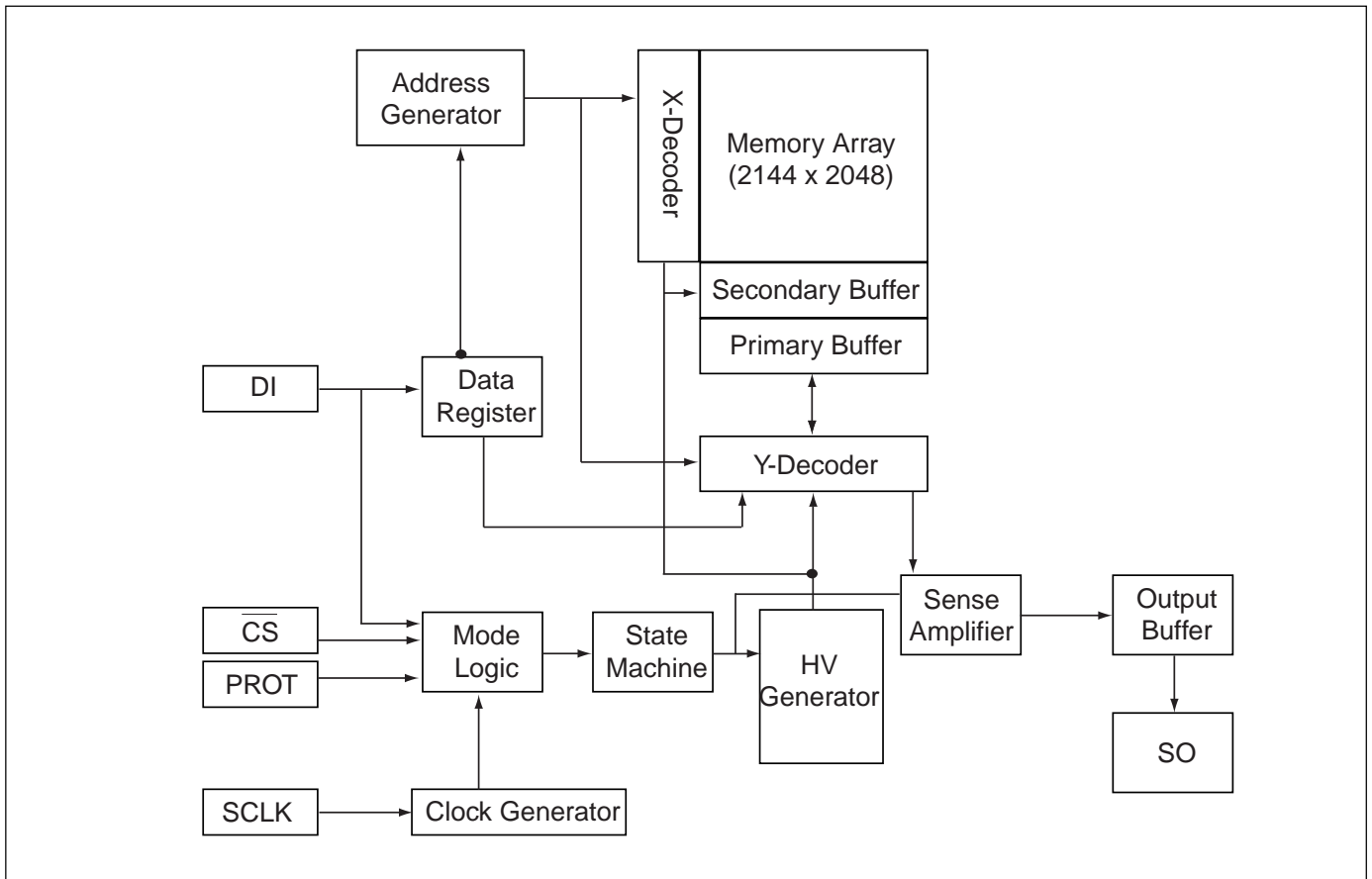
COMMAND DEFINITION

Com- mand	Read Array	Array to Buffer	Read Buffer	Write Buffer	Status Read	Clear Status	Read ID	Read Error Buffer
1st byte	52H	53H	81H	82H	83H	89H	85H	86H
2nd byte	SA2	SA2	BA	BA			X	X
3rd byte	SA1	SA1	X					
4th byte	PN	PN						
5th byte	BA							
6th byte	X							
7th byte	X							
8th byte	X							
9th byte	X							
Action	n bytes read out until $\overline{CS}$ $\mathcal{f}$	start to transfer at CS $\mathcal{f}$	n bytes read out until CS $\mathcal{f}$	n bytes write until CS $\mathcal{f}$	Output status byte until $\overline{CS}$ $\mathcal{f}$	Clear status byte	Output vendor code until $\overline{CS}$ $\mathcal{f}$	n bytes read out until $\overline{CS}$ $\mathcal{f}$

Com- mand	Sector Erase	Page Program	Extra Byte Program	Sleep	Wake Up
1st byte	F1H	F2H	F3H	88H	87H
2nd byte	SA2	SA2	SA2		
3rd byte	SA1	SA1	SA1		
4th byte		PN	PN		
5th byte		BA	BA		
6th byte					
7th byte					
8th byte					
9th byte					
Action	Start to erase at $\overline{CS}$ $\mathcal{f}$	Load n bytes data to buffer until $\overline{CS}$ $\mathcal{f}$ & start to program	Load n bytes data to extra byte buffer until $\overline{CS}$ $\mathcal{f}$ & start to program	Enter sleep mode Sleep bit set	Enter standby mode Sleep bit reset

1-byte op code
       Bit7(MSB), Bit6, Bit5, Bit4, Bit3, Bit2, Bit1, Bit0

2-byte sector address(0 to 03FFH)
     SA1: A17   A16   A15   A14   A13   A12   A11   A10
     SA2: X   X   X   X   X   X   A19 A18

1-byte page number(0 to 3)
      PN: X   X   X   X   X   X   A9   A8

1-byte page address(0 to 85H)
      BA: A7   A6   A5   A4   A3   A2   A1   A0
            A7 = 0 -------> 128 normal bytes
            A7 = 1 -------> 6 extra bytes

DEVICE OPERATION(please refer to serial data input/output timing on page 10 for basic bus timing)

Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

COMMAND DESCRIPTION

(1) Read Array

This command is sent with the sector address, the page number, and the byte address, followed by four dummy bytes sent to give the device time to stabilize. The device will then send out data starting at the byte address until $\overline{CS}$ goes high. The clock to clock out the data is supplied by the master SPI. If the end of the page is reached then the device will wrap around to the beginning of the page.

(2) Array to Buffer

This command is sent with the sector address and the page number. The device will then transfer the entire page into the page buffer without any further input. This should be completed in under 40 µs.

(3) Read Buffer

This command is sent with the byte address, followed by a dummy byte. The device will then send out the data starting at the byte address until $\overline{CS}$ goes high. The clock to clock out the data is supplied by the master SPI. If the end of the page is reached then the device will wrap around to the beginning of the page.

(4) Write Buffer

This command is sent with the byte address. The device will then receive the data starting at the byte address until $\overline{CS}$ goes high. The clock to clock in the data is supplied by the master SPI. If the end of the page is reached then the device will wrap around to the beginning of the page.

The write buffer command could be issued after 40µs from the rising edge of $\overline{CS}$ of program/erase operation.

(5) Read Status Register

When this command is sent, the device will continuously send out the status register contents starting at bit7. The clock to clock out the data is supplied by the master SPI.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ready busy	array to buf	sleep	erase error	program error			
1=busy	1=transfering	1=sleep	1=error	1=error	0	0	0

Bit 7 = "1" -----> Device is busy doing program /erase operation.
      = "0" -----> Device is not doing program/erase operation.
Bit 6 = "1" -----> Device is busy doing array to buffer transfer.
      = "0" -----> Device is not doing array to buffer transfer.

Bit 5 = "1" -----> Device is in sleep mode.
      = "0" -----> Device is not in sleep mode.
Bit 4 = "1" -----> There is an error occurred in last erase operation.
      = "0" -----> There is no error occurred in last erase operation.
Bit 3 = "1" -----> There is an error occurred in last program operation. Error location could be extracted in read error
                 buffer mode.
      = "0" -----> There is no error occurred in last program operation.

(6) Clear Status Register

This command only resets erase error bit (bit 4) and program error bit (bit 3) . These two bits are set by on-chip state machine during program/erase operation, and can only be reset by issuing a clear status register command or by powering down VCC . For other bits of the status register, R/B bit (bit 7) wil be automatically reset when device completes program/rease operation, array to buffer bit (bit 6) is reset when array to buffer transfer is completed, and sleep bit (bit 5) is automatically reset when device gets out of sleep mode.

 If status register indicates that error occured in the last program/erase operation, any further program/erase operation will be prohibited until status register is cleared.

(7) Read ID

This command is sent with an extra dummy byte(a 2-byte command). The device will clock out manfacturer code (C2H) and device code (42H) when this command is issued.   The clock to clock out the data is supplied by the master SPI.

(8) Read Error Buffer

This command is sent with a dummy byte. If the error flag is set after programming, read error buffer command can be issued to find the failed location(s). This command will cycle through the whole page and clock out the data of error buffer sequentially from byte 0 until $\overline{CS}$ goes high, so the error(s) can be determined and appropriate action taken. This will be accomplished without disturbing the contents of the primary buffer. Any "0" in the output string means error at the corresponding location. Status register will be cleared automatically when this command is issued.

(9) Sector Erase

This command is sent with the sector address. The device will start the erase sequence after $\overline{CS}$ goes high without any further input. A sector should be erased in a typical of 8ms. The write buffer command can be issued in preparation for the next programming sequence after 40us from the rising edge of CS of the current erase operation. The average current is less than 25mA.

(10) Page Program

This command is sent with the sector address, page number, and byte address, followed by programming data. One to 134 bytes(including extra bytes) of data can be loaded into the device and then simultaneously written during the programming period. Until CS goes high the device will program the specified page with buffered data. The typical page program time is 3ms. The write buffer command can be issued in preparation for the next programming sequence after 40μs from the rising edge of $\overline{CS}$ of the current program operation. The average current is less than 25mA.

(11) Extra Byte Program

This command is sent with sector address, page number, and byte address, followed by programming data. Only extra bytes will be simultaneously written during the programming period. Until $\overline{CS}$ goes high the device will program the specified page address with buffered data. The typical extra byte page program time is 3ms. The Write Buffer command can be issued in preparation for the next programming sequence after 40us from the rising edge of $\overline{CS}$ of the on-going program operation. The average current is less than 25mA. Please note that only extra bytes (from page address 80H to 85H) will be programmed by issuing this command.

Extra byte program provides users with the convenience of programming extra bytes without having to load data for regular bytes. The error buffer would be cleared if this command is issued.

(12) Sleep

The Sleep command can be issued during Array to Buffer, Sector Erase, or Page Program operation before completion, or in standby mode. Once current operation is completed, either Ready/Busy bit (bit7) or Array to Buffer bit (bit 6)is reset, and Sleep bit is set. Since status register is not reset during sleep mode, error bit (bit4 or bit 3) may have been set in the last erase or program operation. Issuing a wake up command will bring the device out of the sleep mode. The read status register command could be issued to detect the status bit. Typical sleep current is less than 1uA.

(13) Wake up

This command will bring the device out of the sleep mode and prepare it for the next operation. The next command should be issued at less 25us later.

OTHER OPERATION MODES

(1)Standby Mode

When $\overline{CS}$ is high and there is no operation in progress, the device is put in standby mode. Typical standby current is less than 30uA.

(2)Write Protect Mode

If PROT pin is sampled high on falling edge of $\overline{CS}$ input, the top 4 sectors will be protected from Program or Erase operation; please refer to the PROT signal timing on page 10. Other sectors are not subject to this protection mechanism.

POWER-ON STATE

After power-up, the device is placed in the following state :

• The status register is reset.

Bit 7 = "0" -----> Device is not in program/erase operation.
Bit 6 = "0" -----> Device is not in array to buffer mode.
Bit 5 = "0" -----> Device is not in sleep state.
Bit 4 = "0" -----> Erase error flag is reset.
Bit 3 = "0" -----> Program error flag is reset.

DATA SEQUENCE

Output data is serially sent out through SO pin, synchronized with the falling edge of SCLK, whereas input data is serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data is bit 7 (MSB) first, then bit 6, bit 5, ..., and bit 0.

ADDRESS SEQUENCE

The address assignment is described as follows :
BA : byte address, used to specify byte location within a page.
     Bit sequence: A7 A6 A5 A4 A3 A2 A1 A0
               A7 = 0 to select regular byte
               A7 = 1 to select extra byte
PN : page number, used to select a page within a sector
     Bit sequence: X X X X X X A9 A8
SA1, SA2 : sector address, used to select a sector.
   SA1 Bit sequence: A17 A16 A15 A14 A13 A12 A11 A10
     SA2 Bit sequence: X X X X X X A19 A18

APPLICATION EXAMPLE

PAGE PROGRAM FLOW CHART

This example demonstrates how errors detected in the current page can be corrected immediately after page program operation. Only 6 bytes of host memory is needed temporarily save data for 6 extra bytes. Extra bytes provides users with a method to record the errors occured in the normal 128 bytes.

DEFECT MANAGMENT FOR PAGE PROGRAM
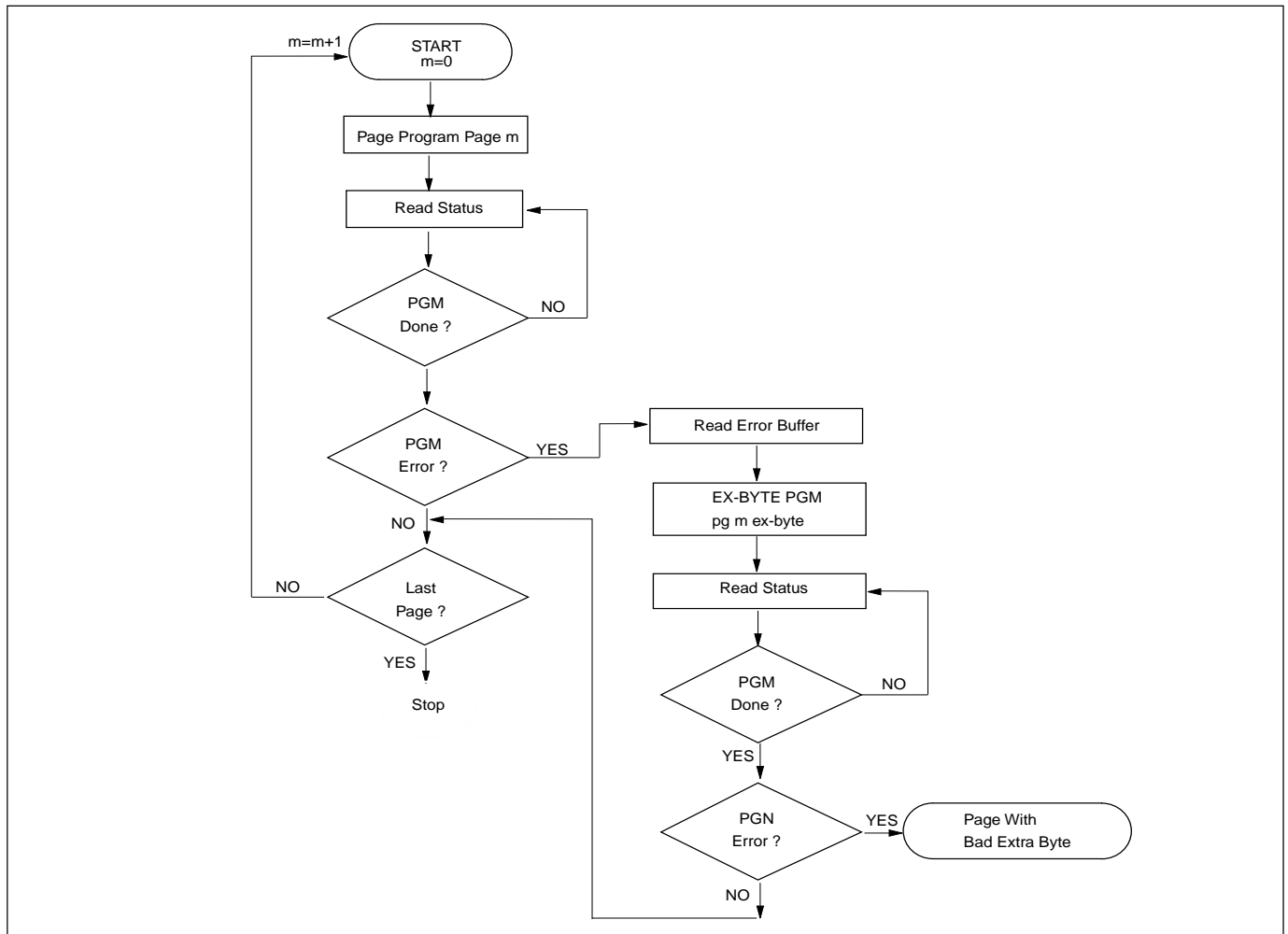
ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

| RATING	VALUE
Ambient Operating Temperature	-10°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 3.8V
Applied Output Voltage	-0.5V to 3.8V
VCC to Ground Potential	-0.5V to 3.8V

NOTICE:

1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

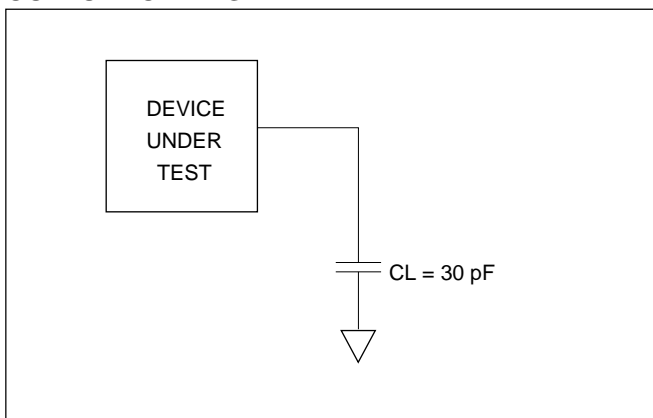2.Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			16	pF	VOUT = 0V

INPUT TEST WAVEFORMS AND MEASURESMENT LEVEL

3.0V

0V

1.5V

AC
Measurement
Level

OUTPUT LOADING

DEVICE
UNDER
TEST

CL = 30 pF
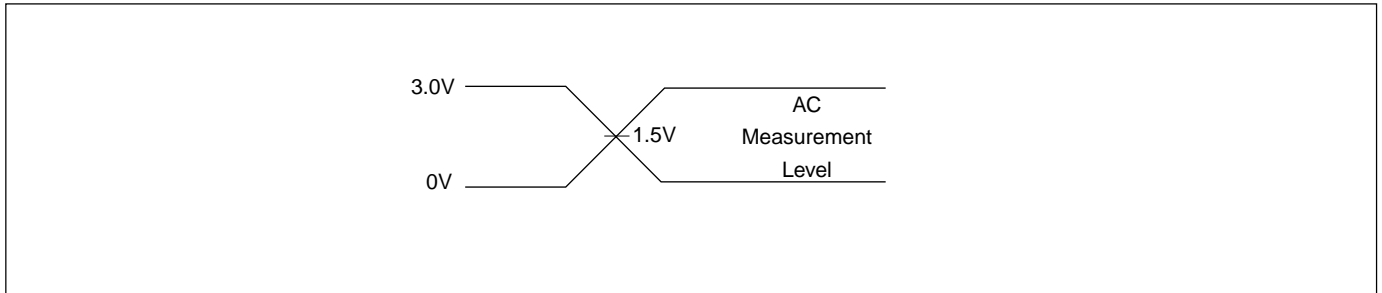
DC CHARACTERISTICS = -10°C to 85°C, VCC = 2.7V ~ 3.6V

| SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current(CMOS)	1		30	60	uA	$\overline{VCC}$ = VCC Max $\overline{CS}$ = VCC ± 0.2V
ISB2	VCC Standby Current(TTL)			1	2	mA	$\overline{VCC}$ = VCC Max $\overline{CS}$ = VIH
IDP	VCC Sleep Current	1		1	10	uA	$\overline{CS}$ = VCC ± 0.2V
ICC1	VCC Read	1		10	30	mA	
ICC3	VCC Program Current	1		10	30	mA	Program in Progress
ICC4	VCC Erase Current	1		10	30	mA	Erase in Progress
VIL	Input Low Voltage	2	-0.5		0.4	V	
VIH	Input High Voltage	3	2.4		VCC+0.5	V	
VOL	Output Low Voltage				0.45	V	IOL = 500uA
VOH	Output High Voltage		2.4			V	IOH = -100uA

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at VCC = 3.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. VIL min. = -1.0V for pulse width ≤ 50ns.
   VIL min. = -2.0V for pulse width ≤ 20ns.
3. VIH max. = VCC + 1.5V for pulse width ≤ 20ns. If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS

SYMBOL	PARAMETER	Min.	Typ.	Max.	Units	Conditions
fSCLK	Clock Frequency	0		11	MHz	
tCYC	Clock Cycle Time	100			ns	
tSKH	Clock High Time	50			ns	
tSKL	Clock Low Time	50			ns	
tR	Clock Rise Time			10	ns	
tF	Clock Fall Time			10	ns	
tCSA	$\overline{CS}$ Lead Clock Time	50			ns	
tCSB	$\overline{CS}$ Lag Clock Time	50			ns	
tCSH	$\overline{CS}$ High Time	100			ns	
tDSU	SI Setup Time	5			ns	
tDH	SI Hold Time	25			ns	
tAA	Acess Time	5		55	ns	
tDOH	SO Hold Time			5	ns	
tPSH	PROT Setup Time	25			ns	
tPHO	PROT Hold Time	25			ns	
tECY	Erase Cycle Time		8		ms	
tPCY	Program Cycle Time		3		ms	
tSR	Status Read After $\overline{CS}$	1			us	
tWUT	Wake Up Time	25			us	

SERIAL DATA INPUT/OUTPUT TIMING
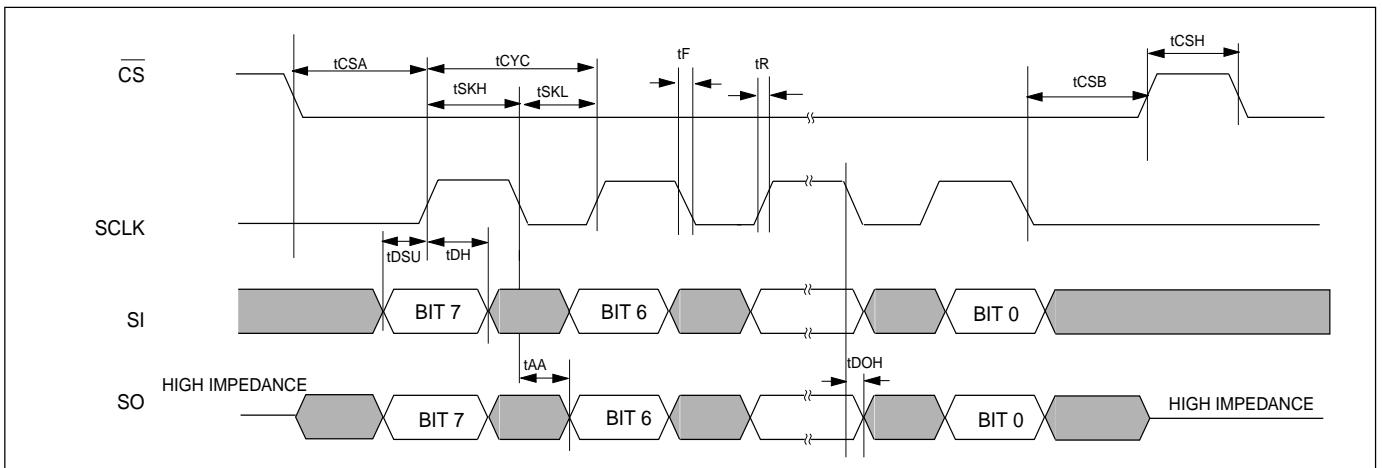
PROT SIGNAL TIMING
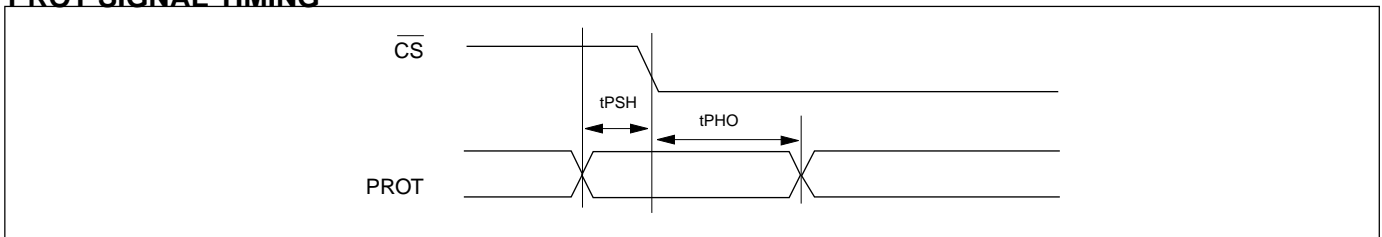
Revision History

Revision No.	Description	Page	Date
2.4	Standby mode current changed to 30uA. Flow chart typing error.		Nov/20/96
2.5	Add one error byte.		Dec/26/96
2.6	Operation conditon changed to 2.7V~3.6V/11MHz and no defect byte is alowed. tDH value is also changed.		Mar/31/98
2.7	Change operation temperature from 0~60°C to -10~85°C	P8;P9	Sep/25/98
	tAA change from 45ns to 55ns @ -10~85°C operation	P10	

32-PIN PLASTIC TSOP(I)

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.078 ± .006
B	18.40 ± .10	.724 ± .004
C	8.20 max.	.323 max.
D	.15[Typ.]	.006[Typ.]
E	.80[Typ.]	.031[Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50[Typ.]	.020[Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~ 5°	.500
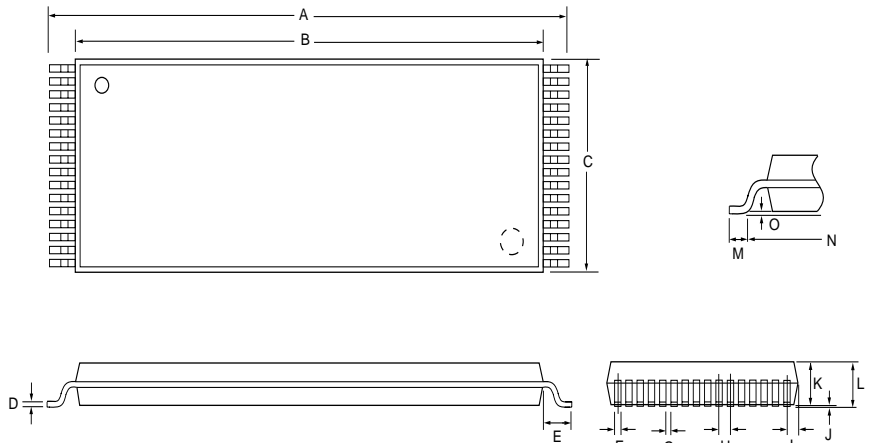
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.