## Features

- Fast Read Access Time - 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64-Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1 to 64-Byte Page Write Operation
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- Single 3.3V ± 5% Supply
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

# 256K (32K x 8) Low Voltage CMOS $E^2$PROM

## Description

The AT28LV256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

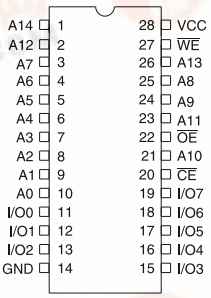
The AT28LV256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to

*(continued)*

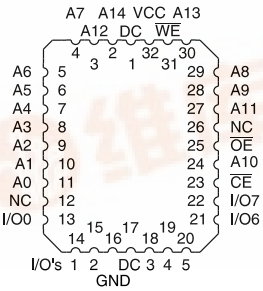
## Pin Configurations

| Pin Name | Function |
|---|---|
| A0 - A14 | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| I/O0 - I/O7 | Data Inputs/Outputs |
| NC | No Connect |
| DC | Don't Connect |

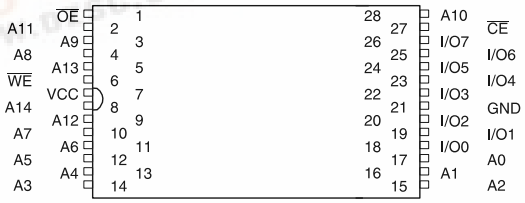
PDIP, SOIC
Top View




PLCC
Top View




TSOP
Top View




Note: PLCC package pins 1 and 17 are DON'T CONNECT.

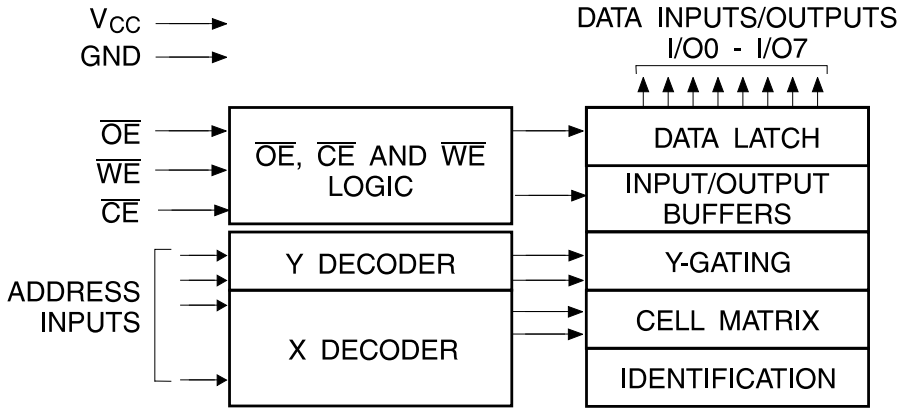
0273E

## Description (Continued)

64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28LV256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of $E^2$PROM for device identification or tracking.

## Block Diagram




## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to $V_{CC}$ + 0.6V |
| Voltage on $\overline{OE}$ and A9 with Respect to Ground | -0.6V to +13.5V |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Device Operation

**READ:** The AT28LV256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

**BYTE WRITE:** A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of $t_{WC}$, a read operation will effectively be a polling operation.

**PAGE WRITE:** The page write operation of the AT28LV256 allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs ($t_{BLC}$) of the previous byte. If the $t_{BLC}$ limit is exceeded the AT28LV256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

**$\overline{DATA}$ POLLING:** The AT28LV256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

**TOGGLE BIT:** In addition to $\overline{DATA}$ Polling the AT28LV256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

**DATA PROTECTION:** If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

**HARDWARE PROTECTION:** Hardware features protect against inadvertent writes to the AT28LV256 in the following ways: (a) $V_{CC}$ power-on delay - once $V_{CC}$ has reached 1.8V (typical) the device will automatically time out 10 ms (typical) before allowing a write: (b) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (c) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

**SOFTWARE DATA PROTECTION:** A software-controlled data protection feature has been implemented on the AT28LV256. Software data protection (SDP) helps prevent inadvertent writes from corrupting the data in the device. SDP can prevent inadvertent writes during power-up and power-down as well as any other potential periods of system instability.

The AT28LV256 can only be written using the software data protection feature. A series of three write commands to specific addresses with specific data must be presented to the device before writing in the byte or page mode. The same three write commands must begin each write operation. All software write commands must obey the page mode write timing specifications. The data in the 3-byte command sequence is not written to the device; the address in the command sequence can be utilized just like any other location in the device.

Any attempt to write to the device without the 3-byte sequence will start the internal write timers. No data will be written to the device; however, for the duration of $t_{WC}$, read operations will effectively be polling operations.

**DEVICE IDENTIFICATION**: An extra 64-bytes of $E^2$PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

## DC and AC Operating Range

| | | AT28LV256-20 | AT28LV256-25 |
|---|---|---|---|
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C |
| $V_{CC}$ Power Supply | | 3.3V ± 5% | 3.3V ± 5% |

## Operating Modes

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O |
|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ |
| Write (2) | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ |
| Standby/Write Inhibit | $V_{IH}$ | X (1) | X | High Z |
| Write Inhibit | X | X | $V_{IH}$ | |
| Write Inhibit | X | $V_{IL}$ | X | |
| Output Disable | X | $V_{IH}$ | X | High Z |
| Chip Erase | $V_{IL}$ | $V_H$ (3) | $V_{IL}$ | High Z |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to AC Programming Waveforms.
3. $V_H$ = 12.0V ± 0.5V.

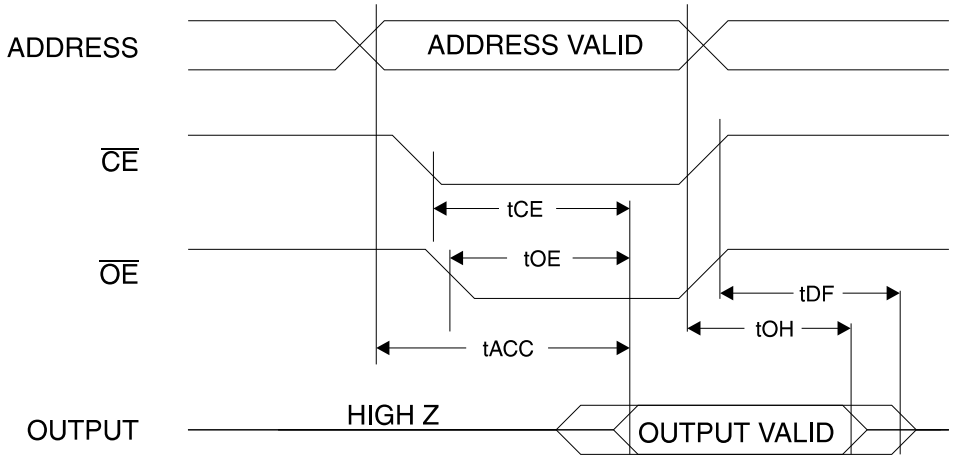
## DC Characteristics

| Symbol | Parameter | Condition | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ + 1V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{I/O}$ = 0V to $V_{CC}$ | | | 10 | µA |
| $I_{SB}$ | $V_{CC}$ Standby Current CMOS | $\overline{CE}$ = $V_{CC}$ - 0.3V to $V_{CC}$ + 1V | Com. | | 20 | µA |
| | | | Ind. | | 50 | µA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz; $I_{OUT}$ = 0 mA | | | 15 | mA |
| $V_{IL}$ | Input Low Voltage | | | | 0.6 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1.6 mA | | | 0.3 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100 µA | | 2.0 | | V |

## AC Read Characteristics

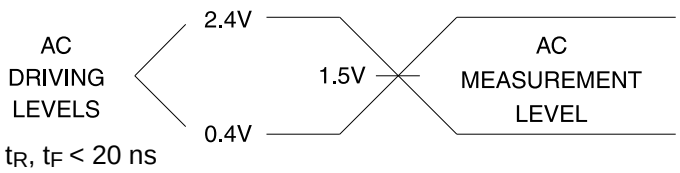
| Symbol | Parameter | AT28LV256-20 | | AT28LV256-25 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | | 200 | | 250 | ns |
| $t_{CE}$ (1) | $\overline{CE}$ to Output Delay | | 200 | | 250 | ns |
| $t_{OE}$ (2) | $\overline{OE}$ to Output Delay | 0 | 80 | 0 | 100 | ns |
| $t_{DF}$ (3, 4) | $\overline{CE}$ or $\overline{OE}$ to Output Float | 0 | 55 | 0 | 60 | ns |
| $t_{OH}$ | Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first | 0 | | 0 | | ns |

## AC Read Waveforms (1, 2, 3, 4)



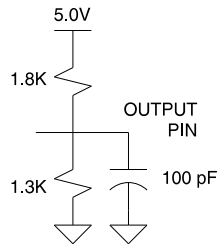

Notes: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on $t_{ACC}$.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$ or by $t_{ACC} - t_{OE}$ after an address change without impact on $t_{ACC}$.
3. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L$ = 5 pF).
4. This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level




$t_R$, $t_F$ < 20 ns

## Output Test Load




## Pin Capacitance (f = 1 MHz, T = 25°C) (1)

| | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 6 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: 1. This parameter is characterized and is not 100% tested.

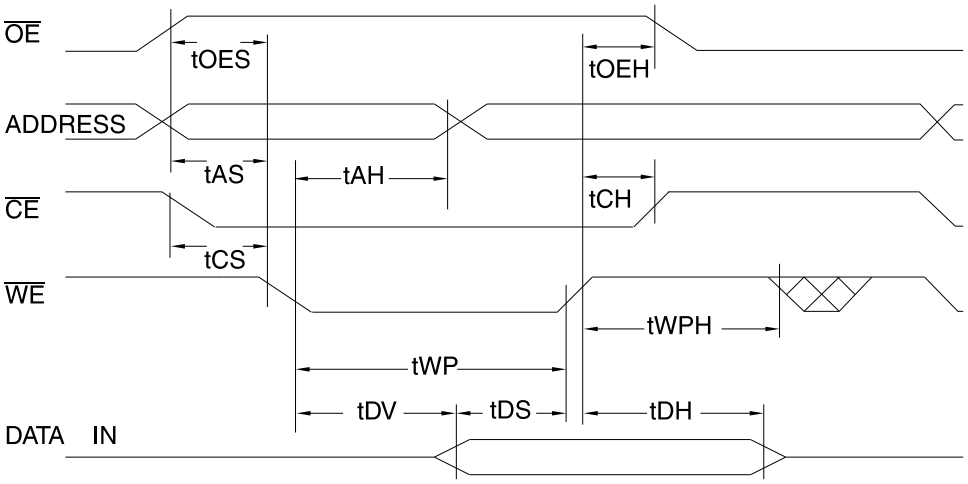
## AC Write Characteristics

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AS}$, $t_{OES}$ | Address, $\overline{OE}$ Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{CS}$ | Chip Select Set-up Time | 0 | | ns |
| $t_{CH}$ | Chip Select Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width ($\overline{WE}$ or $\overline{CE}$) | 200 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | ns |
| $t_{DH}$, $t_{OEH}$ | Data, $\overline{OE}$ Hold Time | 0 | | ns |
| $t_{DV}$ | Time to Data Valid | NR (1) | | |

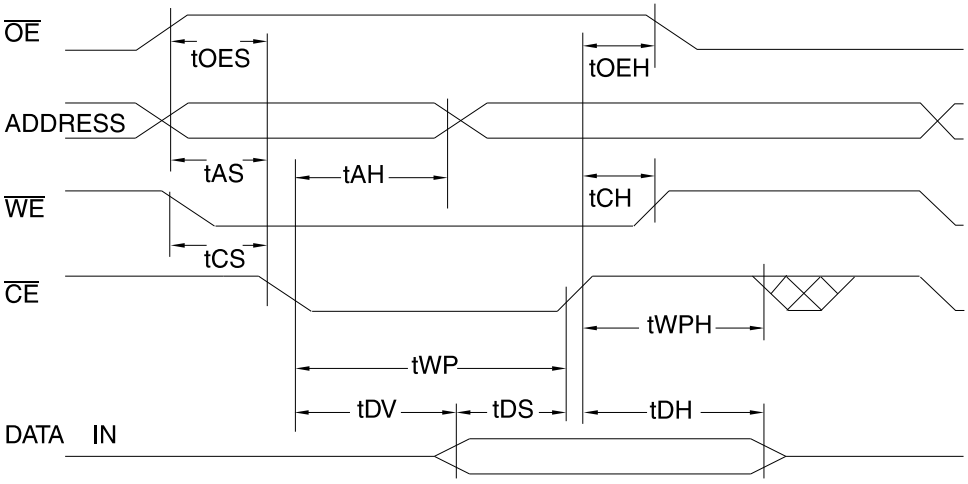
Note: 1. NR = No Restriction

## AC Write Waveforms

### $\overline{WE}$ Controlled



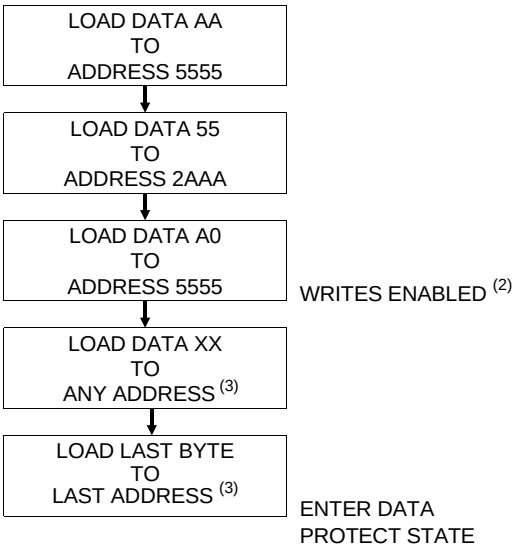

### $\overline{CE}$ Controlled



## Page Mode Characteristics

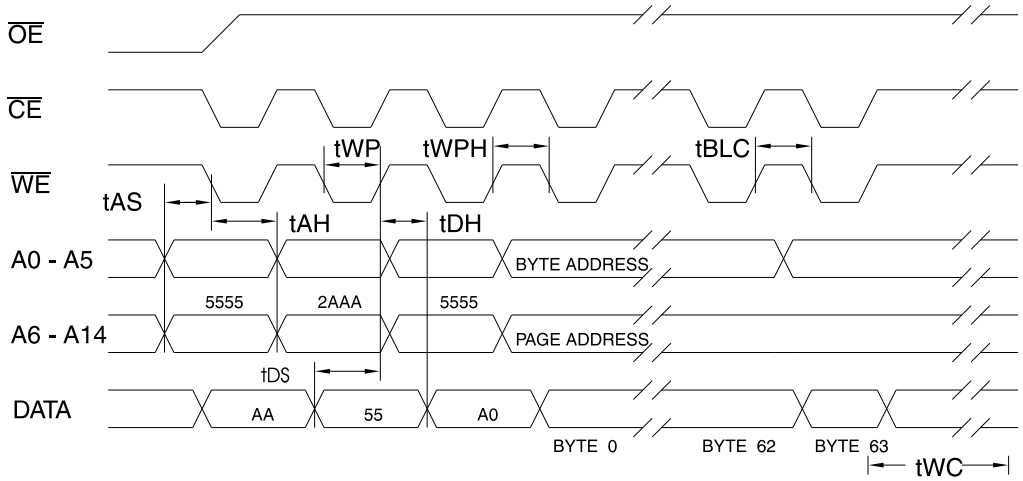
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | | 10 | ms |
| $t_{AS}$ | Address Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 200 | | ns |
| $t_{BLC}$ | Byte Load Cycle Time | | 150 | µs |
| $t_{WPH}$ | Write Pulse Width High | 100 | | ns |

## Programming Algorithm




Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 64-bytes of data are loaded.

## Software Protected Write Cycle Waveforms (1, 2, 3)



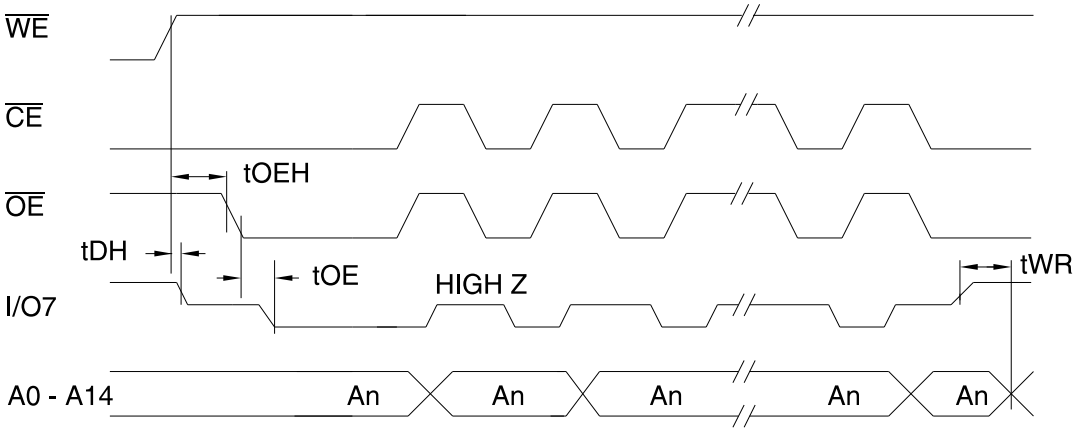

Notes: 1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.
2. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

## $\overline{\text{Data}}$ Polling Characteristics (1)

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{DH}$ | Data Hold Time | 0 | | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time | 0 | | | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay (2) | | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

## $\overline{\text{Data}}$ Polling Waveforms

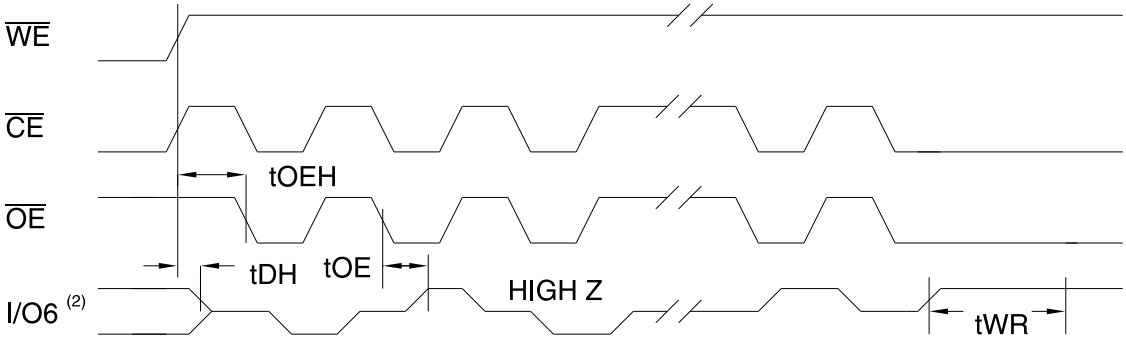



## Toggle Bit Characteristics (1)

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay (2) | | | | ns |
| $t_{OEHP}$ | $\overline{OE}$ High Pulse | 150 | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

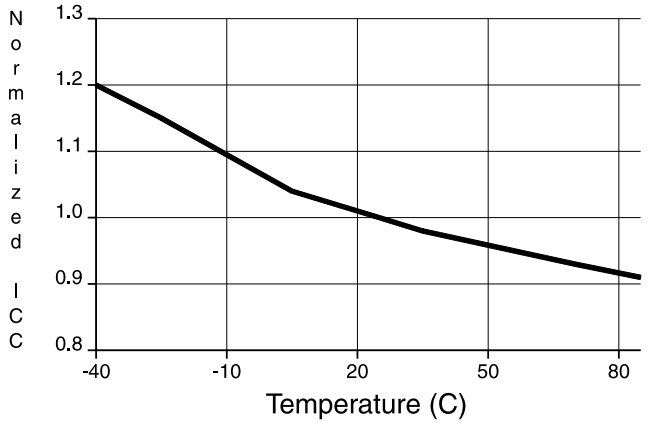
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

## Toggle Bit Waveforms

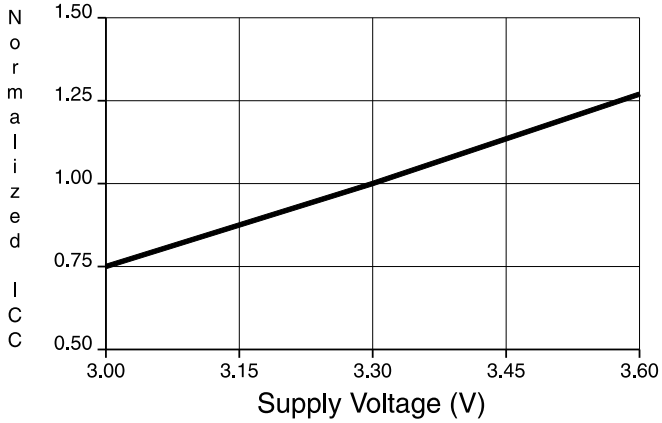



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

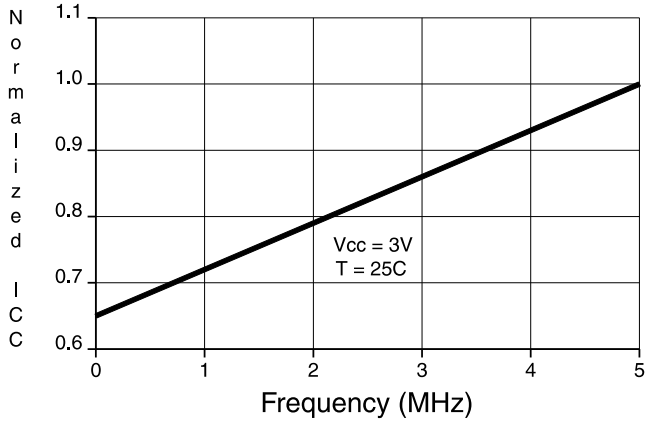
## NORMALIZED SUPPLY CURRENT vs. TEMPERATURE




## NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE




## NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



## Ordering Information [1]

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 200 | 80 | 0.2 | AT28LV256-20JC<br>AT28LV256-20PC<br>AT28LV256-20SC<br>AT28LV256-20TC | 32J<br>28P6<br>28S<br>28T | Commercial<br>(0°C to 70°C) |
| | 80 | 0.2 | AT28LV256-20JI<br>AT28LV256-20PI<br>AT28LV256-20SI<br>AT28LV256-20TI | 32J<br>28P6<br>28S<br>28T | Industrial<br>(-40°C to 85°C) |
| 250 | 80 | 0.2 | AT28LV256-25JC<br>AT28LV256-25PC<br>AT28LV256-25SC<br>AT28LV256-25TC | 32J<br>28P6<br>28S<br>28T | Commercial<br>(0°C to 70°C) |
| | 80 | 0.2 | AT28LV256-25JI<br>AT28LV256-25PI<br>AT28LV256-25SI<br>AT28LV256-25TI | 32J<br>28P6<br>28S<br>28T | Industrial<br>(-40°C to 85°C) |

Note: 1. See Valid Part Number table below.

## Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

| Device Numbers | Speed | Package and Temperature Combinations |
|---|---|---|
| **AT28LV256** | 20 | JC, JI, PC, PI, SC, SI, TC, TI |
| **AT28LV256** | 25 | JC, JI, PC, PI, SC, SI, TC, TI |

| Package Type | |
|---|---|
| **32J** | 32 Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| **28P6** | 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **28S** | 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| **28T** | 28 Lead, Plastic Thin Small Outline Package (TSOP) |