DS3170DK
DS3/E3 Single-Chip Transceiver Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS3170DK is a fully integrated design kit for the DS3170 DS3/E3 single-chip transceiver (SCT). This design kit contains all the necessary circuitry to evaluate the DS3170 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

DS3170DK Board
Download:
- ChipView Software
- DS3170DK.DEF Definition File
- DS3170DK Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS3170DK	Design Kit for the DS3170 DS3/E3 Single-Chip Transceiver

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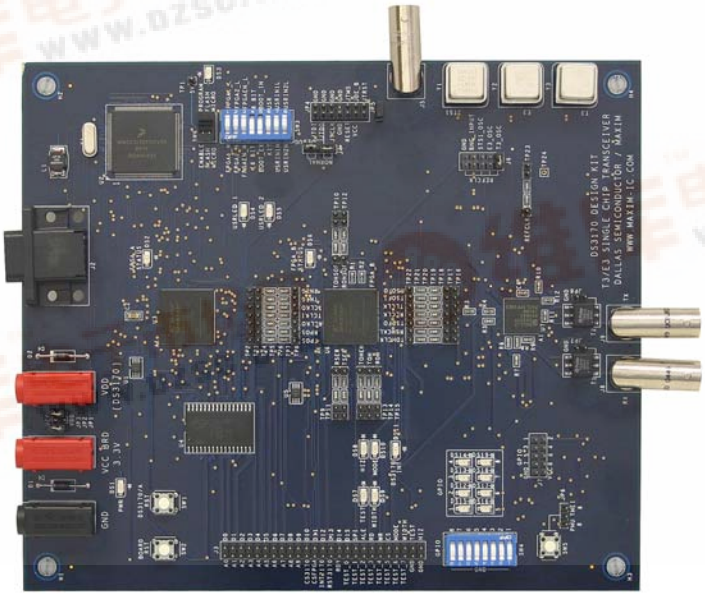
FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Demonstrates Key Functions of the DS3170 DS3/E3 Single-Chip Transceiver (SCT)
- Includes DS3170 Single-Chip Transceiver (SCT), Transformers, 75Ω BNC, and Termination Passives
- Interfaces with Any PC with an RS-232 Serial Interface
- High Level Windows®-Based Software Provides Visual Access to All Registers
- Software Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing
- Precision Test Points for All Clocks and Signals
- On-Board DS3 and E3 Crystal Oscillators for Stable Clock Generation
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDS



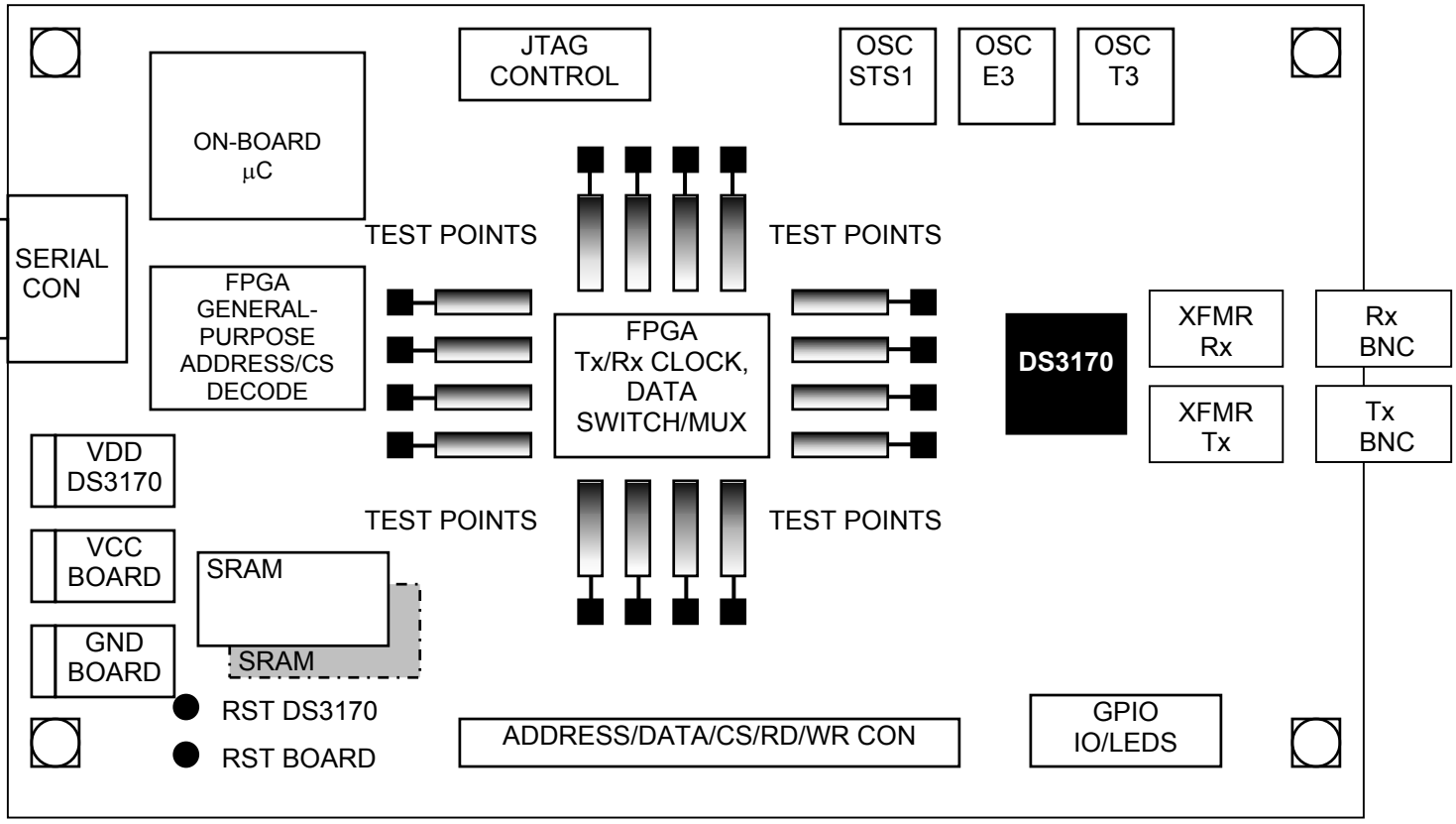
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
C1, C4, C5, C10, C14, C15, C18, C19, C21, C24, C25–C32, C36-C38, C39–C44, C47–C49, C50, C52–C56, C59–C61, C66, C68, C70, C73, C74	44	0.1µF 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C2, C3, C16, C17, C20, C22, C23, C33, C34, C51, C57, C69, C75	13	1µF 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C6, C62, C65	3	0.001µF 10%, 50V ceramic capacitors (0603)	Panasonic	ECJ-1VB1H102K
C7, C8, C9, C11, C35, C58, C76	7	68µF 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
C12, C13	2	10pF 5%, 50V ceramic capacitors (tall case)	Phycomp	1206CG100J9B200
C45, C46	2	10,000pF 10%, 16V ceramic capacitors (0603)	Panasonic	ECJ-1VB1C103K
C63, C64, C67	3	0.01µF 10%, 50V X7R ceramic capacitors (0603)	AVX	06035C103KAT
C71, C72	2	56,000pF 10%, 16V ceramic capacitors (0603)	Panasonic	ECJ-1VB1C563K
D1, D2	2	1A 50V general-purpose silicon diodes	General Semiconductor	1N4001
DS1, DS2, DS6–DS10	7	LED, green, SMD	Panasonic	LN1351C
DS3, DS4, DS5, DS11–DS19	12	LED, red, SMD	Panasonic	LN1251C
J1, PWR_CONNBAN1	2	Banana plug sockets (horizontal, black)	Mouser Electronics	164-6218
J2	1	DB9 right-angle connector (long case)	AMP	747459-1
J3	1	50-pin, dual-row, vertical terminal strip	Samtec	TSW-125-07-T-D
J4	1	100-mils 4-position jumper	Samtec	NA
J5	1	50Ω BNC connector (5-pin right-angle header)	Trompeter	CBJR220
J6, J7	2	Terminal strip, 10-pin, dual row, vertical	Samtec	NA
J8, J9	2	75Ω BNC connectors (5-pin right-angle)	Trompeter	UCBJR220
JP1, JP2, JP3, JP5, JP7, JP8	6	2-pin headers, 0.100” centerline (vertical)	Samtec	TSW-102-07-T-S
JP4	1	14-pin connector (dual row, vertical)	Samtec	NA
JP6	1	100-mils 3-position jumper	Samtec	NA
L1	1	1.0µH 20% 2-pin surface-mount inductor	Coiltronics	UP1B-1R0
PWR_CONNBAN2	1	Banana plug socket (horizontal, red)	Mouser Electronics	164-6219

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
R1–R4, R12, R42, R43, R54–R56, R59, R63, R68, R69, R70, R73, R74, R83, R93, R107	20	150Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF1500V
R5–R8, R10, R15, R51, R57, R62, R71, R81, R85, R92, R94, R95, R100, R101, R103–R106, R109	22	33Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ330V
R9, R11, R16, R22, R30, R32, R38, R46, R60, R61, R64, R65, R72, R77–R80, R89, R90, R91, R96	22	330Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R13	1	1.0MΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
R14, R17–R21, R23–R29, R31, R33–R37, R39, R40, R41, R44, R45, R47, R48, R49, R52, R53, R58, R67, R75, R76, R82, R86, R87, R98, R99, R102, R108, R110	41	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R50	1	1.0kΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ102V
R66, R88, R97	3	0Ω 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R84	1	51.1Ω 1%, 1/16W resistor (0603)	Panasonic	ERJ-3EKF51R1V
SW1, SW2, SW5	3	4-pin single-pole switch MOM	Panasonic	EVQPAE04M
SW3, SW4	2	8-position switch, 16-pin DIP, low profile	AMP	435668-7
SW6	1	Slide switch (DPDT) 6-pin through-hole	Tyco	SSA22
T1, T2	2	1:2 XFMR T3/E3/STS-1 (industrial)	Pulse	T3012
TP1–TP24	24	Test points, compensated, 3pF, 953Ω, 3 plated holes	NA	KIT1
U1, U5	2	8-pin power-μMAX (1.8V or Adj)	Maxim	MAX1792EUA18
U2	1	M-CORE 32-bit microcontroller	Motorola	MMC2107
U3, U6	2	Spartan-IIE 200K gate, 1.8V FPGA, 256 PIN BGA	Xilinx	XC2S200E-6FT256C
U4, U11	2	128K x 8 SRAM	Cypress	CY62128V
U7	1	DS3/E3 SCT 100-pin CSBGA (11mm x 11mm)	Dallas Semiconductor	DS3170
U8	1	3.3V RS-232 20-pin SO	Maxim	MAX3233EEWP
U9, U14, U16–U20, U23	8	High-speed buffer	Fairchild	NC7SZ86

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
U10, U12	2	2Mb flash-based configuration memory	Xilinx	XCF02SV020C
U13	1	Quad 2-input NAND gate 14-pin SO	Toshiba	TC74HC00AFN
U15, U21, U24	3	Hex inverter, SO	Toshiba	TC74HC04AFN
U22	1	SOT switch debouncer	Maxim	MAX6816
X1	1	8.0MHz low-profile crystal	Dove Electronic	EC1-8.000M
Y1	1	3.3V 51.840MHz oscillator, crystal clock	SaRonix	NTH089AA3-51.840
Y2	1	3.3V 34.368MHz oscillator, crystal clock	SaRonix	NTH089AA3-34.368
Y3	1	3.3V 44.736MHz oscillator, crystal clock	SaRonix	NTH089AA3-44.736

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS3170DK QuickView page for files.

The support files are used with an evaluation program called ChipView with is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings)

- For single power-supply operation, short jumpers JP1-JP3. This connects VDD of the DS3170 to the board VCC.
- Ensure that *PROGRAM FLASH MICRO* is selected (SW6). DS3 should not be on.
- Connect reference clock. See Table 1.
- DIP switches (SW3) can be in either the ON or OFF position depending on the desired configuration. See Table 6..
- Connect serial cable from DS3170DK (J2) to PC.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.

Reference Clock Configuration

The reference clock for the DS3170 (SCT) can be configured a number of ways depending on the application's need. This is done by shorting the REFCLK signal on J6 to the signal inputs, which are also connected to J6.

Table 1: Reference Clock Configuration

REFERENCE CLOCK	DESCRIPTION
GND	Short pins J6.1 and J6.2 together. Open all other pins on J6.
BNC Input	Short pins J6.3 and J6.4 together. Open all other pins on J6.
STS1 OSC	Short pins J6.5 and J6.6 together. Open all other pins on J6.
E3 OSC	Short pins J6.7 and J6.8 together. Open all other pins on J6.
T3 OSC	Short pins J6.9 and J6.10 together. Open all other pins on J6.

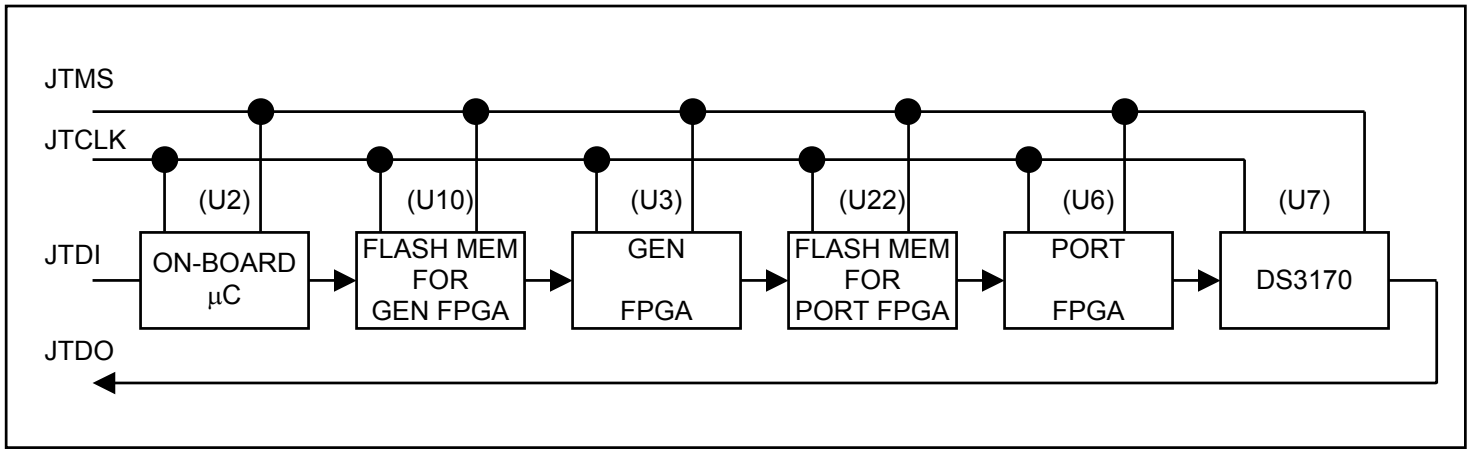
JTAG Configuration

The JTAG chain is controlled by the following connectors: J4, JP4, and JP5. Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the three connectors can be configured to accomplish the desired task. For information on programming the internal flash of the microcontroller, refer to the microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. Figure 1 shows the complete chain as well as what order the devices will appear during boundary scan. To set up this configuration, perform the following:

- Connect JTDI to JP4.1
- Connect JTDO to JP4.3
- Connect JTMS to JP4.10
- Connect JCLK to JP4.5
- Connect J4.1 to J4.2
- Connect J4.3 to J4.4
- Connect JP5.1 to JP5.2

Figure 1. JTAG Chain



Address/Data BUS Connector

The DS3170DK has a connector (J3) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If FPGA_ENABLE (SW3.3) is logic 0, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS3170 into another system without making any modifications to the hardware. See Table 2 for specific pin information for connector J3.

Table 2. Address/Data Connector

PIN NUM	PIN NAME	DESCRIPTION		PIN NUM	PIN NAME	DESCRIPTION
1	A0	Local Address Bit 0		2	D0	Local Data Bit 0
3	A1	Local Address Bit 1		4	D1	Local Data Bit 1
5	A2	Local Address Bit 2		6	D2	Local Data Bit 2
7	A3	Local Address Bit 3		8	D3	Local Data Bit 3
9	A4	Local Address Bit 4		10	D4	Local Data Bit 4
11	A5	Local Address Bit 5		12	D5	Local Data Bit 5
13	A6	Local Address Bit 6		14	D6	Local Data Bit 6
15	A7	Local Address Bit 7		16	D7	Local Data Bit 7
17	A8	Local Address Bit 8		18	D8	Local Data Bit 8
19	A9	Local Address Bit 9		20	D9	Local Data Bit 9
21	CS3170	Chip Select DS3170		22	D10	Local Data Bit 10
23	CSFPGA	Chip Select Port FPGA		24	D11	Local Data Bit 11
25	INT3170	INT PIN DS3170		26	D12	Local Data Bit 12
27	RST3170	RST PIN DS3170		28	D13	Local Data Bit 13
29	RDY	Ready Handshake DS3170		30	D14	Local Data Bit 14
31	TEST0	Generic I/O Bit 0		32	D15	Local Data Bit 15
33	TEST1	Generic I/O Bit 1		34	SPI	DS3170 Serial/Parallel Bus Mode
35	TEST2	Generic I/O Bit 2		36	ALE	Address Latch Enable
37	TEST3	Generic I/O Bit 3		38	RD_DS	Read (Intel)/Data Strobe (MOT)
39	TEST4	Generic I/O Bit 4		40	WR_W/R	Write (Intel)/Write_READ (MOT)
41	TEST5	Generic I/O Bit 5		42	CS_OUT	Programmable CS_OUT Pin
43	TEST6	Generic I/O Bit 6		44	MODE	Mot/Intel Mode
45	TEST7	Generic I/O Bit 7		46	WIDTH	Data Bus Width
47	GND	GND		48	TEST	Test Enable (Active Low)
49	GND	GND		50	HIZ	High Impedance (Active Low)

High Impedance and Compensated Test Points

The test points for all the clock and data lines are unique for this board such that each test point listed in Table 3 have a relative high-impedance pin and a compensated pin. The compensated pin is part of a (20:1) voltage divider that when used with the standard 50Ω load of an oscilloscope provides a very clean signal. If you are making critical timing and or slew rate measurements, the compensated test points are very useful. Figure 2 shows the relationship between the high-impedance and compensated test point pins.

Figure 2. Test Point Logical and Physical View

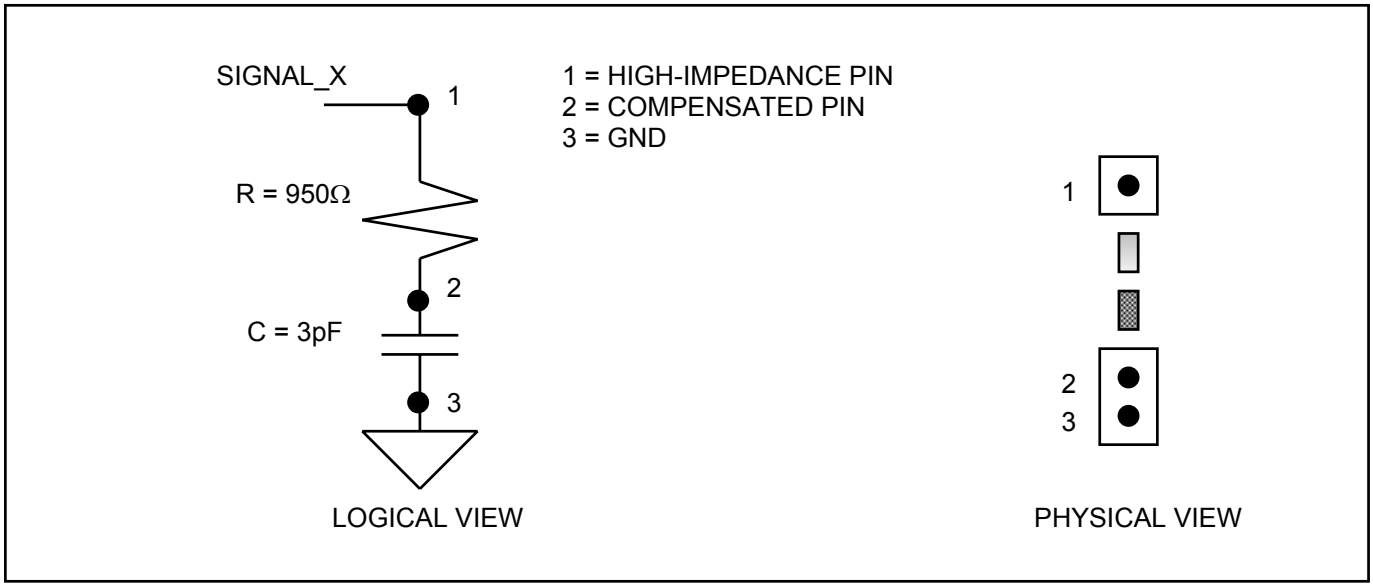


Table 3. Test Points

REF DES	SIGNAL NAME		REF DES	SIGNAL NAME
TP5	TCLKI		TP7	TNEG
TP6	TCLKO		TP8	RNEG
TP4	RCLKO		TP2	TPOS
TP20	TLCLK		TP3	RPOS
TP19	RLCLK		TP11	TSER
TP10	TOHSOF		TP9	RSER
TP12	ROHSOF		TP13	TOHEN
TP16	TOHCLK		TP14	TOH
TP17	ROHCLK		TP15	ROH
TP19	TSOFO		TP23	REFCLK
TP22	RSOFO		TP21	TSOFI

General Purpose Input/Output for DS3170

The DS3170 SCT has an 8-bit port that can be bit configured as either general-purpose I/O or specific alarms, a TEMI input, or PMU input. Refer to the DS3170 data sheet for specific questions about the operation of the DS3170 GPIO port.

Each GPIO pin has two types of inputs and an LED for easy identification of the pin's state. The first input type for the GPIO port is an 8-bit switch (SW4). Each pin on SW4 corresponds to the bit in the GPIO. When the switch is in the "On" position, the pin for the switch is grounded and provides logic 0 to the port. When the switch is in the "Off" position, the pin for the switch floats to VDD and provides logic 1 to the port.

The second input type for the GPIO port is a straight 10-pin header (J7). This can be simply a monitoring pin for the GPIO port or used as input stimulus. **Note:** If you plan to drive a bit to a value other than GND, the GPIO bit in SW4 must be in the "Off" position. See the DS3170DK schematic for questions on the connection of the GPIO port.

Table 4 provides a description of pin out of SW4 and J7.

Table 4. GPIO Header and Switch Pinout

PIN NUMBER		PIN NAME
SW4.1	J7.1	GPIO Bit 1
SW4.2	J7.2	GPIO Bit 2
SW4.3	J7.3	GPIO Bit 3
SW4.4	J7.4	GPIO Bit 4
SW4.5	J7.5	GPIO Bit 5
SW4.6	J7.6	GPIO Bit 6
SW4.7	J7.7	GPIO Bit 7
SW4.8	J7.8	GPIO Bit 8

TEMI and PMU Inputs

GPIO Bit 6 and GPIO Bit 8 can be configured to be the TEMI and PMU inputs respectively. A pushbutton (SW5) and 3-position jumper (JP6) are available to provide a glitch-free input to either of these inputs. **Note:** When using the pushbutton (SW5) and 3-position jumper (JP6) as an input to the GPIO pins, you must have the appropriate switch in SW4 in the "Off" position.

Table 5. TEMI and PMU Configuration

SIGNAL NAME	SETUP PROCEDURE
TEMI	Set SW4.6 to the "Off" position
	Short (Jumper) JP6.3 and JP2
PMU	Set SW4.8 to the "Off" position
	Short (Jumper) JP6.1 and JP2

User Input Switch (SW3)

SW3 is an 8-pin DIP switch that controls the function of the on-board microcontroller and the two on-board FPGAs, and offers a number of generic inputs for user programs.

Table 6. User Input Switch Pinout

PIN	NAME	FUNCTION
1	FPGA INPUT 1	Generic Input-Only Pin to the General-Purpose FPGA. Value of pin is copied to general-purpose register XXXXXXXX. Can be used for user programs. This pin has no effect if FPGA ENABLE is logic 0.
2	FPGA INPUT 2	Generic Input-Only Pin to the General-Purpose FPGA. Value of pin is copied to general-purpose register XXXXXXXX. Can be used for user programs. This pin has no effect if FPGA ENABLE is logic 0.
3	FPGA ENABLE	Input-Only Pin to the General-Purpose FPGA (U3). When this pin is logic 1 (SW3.3 is OFF), the FPGA is enabled and will transfer data from the DS3170 and FPGA as directed from the on-board microcontroller. When this pin is logic 0 (SW3.3 is ON), the FPGA is disabled. All inputs and outputs to the DS3170 and port FPGA are tri-stated. **Note:** This pin does not cause a hardware enable for the PORT FGPA.
4	DATA BUS SELECT	Input-Only Pin to the General-Purpose FPGA (U3). When this pin is logic 1 (SW3.4 is OFF), the DS3170 and the port FPGA are set up such that they use the 16-bit bus from the on-board microcontroller. When this pin is logic 0 (SW3.4 is ON), the DS3170 and the port FPGA are set up such that they use the 8-bit bus from the on-board microcontroller. This pin has no effect if FPGA ENABLE is logic 0.
5	BOOT SEL	Input-Only Pin to the On-Board Microcontroller. When this pin is logic 1 (SW3.5 is OFF), the on-board microcontroller loads the firmware from an external source rather than the internal flash bank. When this pin is logic 0 (SW3.5 is ON), the microcontroller loads the firmware from the internal flash bank. If you choose to load code from an external source, refer to the user manual for the on-board microcontroller (U2) to ensure that all the timing and data are correct to run this program. This option should only be used by the advanced user.
6	KIT	Input-Only Pin to the On-Board Microcontroller. Not implemented with the firmware shipped from Dallas Semiconductor. This pin can be used by a user program.
7	USER INPUT 1	Input/Output Pin to the General-Purpose FPGA (U3). This pin has an LED (DS4) to track the value of this signal. This pin has no effect if FPGA ENABLE is logic 0. **Note:** If you choose to use this as an output, USER INPUT 1 (SW3.7) must be in the off position.
8	USER INPUT 2	Input/Output Pin to the General-Purpose FPGA (U3). This pin has an LED (DS5) to track the value of this signal. This pin has no effect if FPGA ENABLE is logic 0. **Note:** If you choose to use this as an output, USER INPUT 1 (SW3.8) must be in the off position.

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Settings).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.EXE. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.
- Load the DS3170DK.DEF file.
- Make sure that all the register settings are correct for the proper function desired for the DS3170DK.
- Refer to the DS3170 data sheet for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given in Table 7 are relative to the beginning of the user address space. All device registers can be easily modified using ChipView.EXE host-based user-interface software.

Table 7. Relative Address Map

REF DES	DEVICE	OFFSET
U3	General-purpose FPGA	0x0000
U6	FPGA Tx/Rx clock, data switch/mux	0x1000
U7	DS3170 DS3/E3 single-chip transceiver	0x2000

Table 8. General-Purpose Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read Only	Board ID
0x02	DSIDH	Read Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read Only	Board Rev
0x06	ASMREV	Read Only	Assembly Rev
0x07	FPGAREV	Read Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Reg #1

ID REGISTERS

BID: BOARD ID (Offset=0X0000)

BID is read only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset=0X0002)

XBIDH is read only with a value of 0x00.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset=0X0003)

XBIDM is read only with a value of 0x07.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset=0X0004)

XBIDL is read only with a value of 0x00.

BREV: BOARD FAB REVISION (Offset=0X0005)

BREV is read only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset=0X0006)

AREV is read only and displays the current assembly revision.

PREV: PLD REVISION (Offset=0X0007)

PREV is read only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: **CTRL1**
Register Description: **Control Register 1**
Register Offset: **0x0008**

Bit #	7	6	5	4	3	2	1	0
Name	SPI_CPOL	SPI_CPHA	SPI_SWAP	SPI	HIZ	WIDTH	MOT	MUX
Default	0	0	0	0	1	0	0	0

Bit 7: SPI_CPOL: This bit controls the SPI Interface Clock Polarity pin, which is muxed with the D7 pin on the DS3170. Bit 7 is only active when bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 6: SPI_CPHA: This bit controls the SPI Interface Clock Phase pin, which is muxed with the D6 pin on the DS3170. Bit 6 is only active when Bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 5: SPI_SWAP: This bit controls the SPI Interface Bit Order Swap pin, which is muxed with the D5 pin on the DS3170. Bit 5 is only active when Bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 4: SPI: This bit controls the SPI Bus Mode bit.
0 = parallel bus mode
1 = SPI bus mode

Bit 3: HIZ: This bit controls the high-impedance test-enable bit (active low). This signal puts all the digial outputs and bidirectional outputs to a high-impedance state when pulled low and also when the JTRST is pulled low. For nomal operation, keep it as a logic 1.

Bit 2: WIDTH: This bit controls the databus width pin for parallel bus mode.
0 = 8-bit parallel mode
1 = 16-bit parallel mode

Bit 1: MOT: This bit controls the MODE pin for the DS3170.
0 = RD/WR strobe mode (Intel)
1 = DS strobe mode (Motorola)

Bit 0: MUX: This bit determines if the ALE pin on the DS3170 is in mux mode or nonmux mode (constantly high).
0 = nonmux mode
1 = mux mode

Register Name: **CTRL2**
Register Description: **Control Register 2–Line IO**
Register Offset: **0x0009**

Bit #	7	6	5	4	3	2	1	0
Name	RNEG3	RNEG2	RNEG1	RNEG0	RPOS3	RPOS2	RPOS1	RPOS0
Default	0	0	0	0	1	0	0	0

Bits 7 to 4: RNEGx: These bits control the source of the RNEG signal.

Bits 3 to 0: RPOSx: These bits control the source of the RPOS signal.

RPOSx	DESCRIPTION
0x00	HI-Z
0x01	TPOS
0x02	T3 OSC
0x03	E3 OSC
0x04	STS1 OSC
0x05	BNC_INPUT
0x06	Logic 0
0x07	Logic 1
0x08–0xFF	HI-Z

RNEGx	DESCRIPTION
0X00	HI-Z
0X01	TNEG
0X02	T3 OSC
0X03	E3 OSC
0X04	STS1 OSC
0X05	BNC_INPUT
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL3**
Register Description: **Control Register 3–Line RCLK**
Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RLCLK3	RLCLK2	RLCLK1	RLCLK0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: These bits are unused.

Bits 3 to 0: RLCLKx: These bits control the source of the RLCLK signal.

RLCLKx	DESCRIPTION
0X00	HI-Z
0X01	TLCLK
0X02	T3 OSC
0X03	E3 OSC
0X04	STS1 OSC
0X05	BNC_INPUT
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL4**
Register Description: **Control Register 4 Overhead Interface**
Register Offset: **0x000B**

Bit #	7	6	5	4	3	2	1	0
Name	TOHEN3	TOHEN2	TOHEN1	TOHEN0	TOH3	TOH2	TOH1	TOH0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: TOHENx: These bits control the source of the TOHEN signal.

Bits 3 to 0: TOHx: These bits control the source of the TOH signal.

TOHENx	DESCRIPTION
0X00	HI-Z
0X01	TOHSOF
0X02	ROHSOF
0X03	Not used
0X04	Not used
0X05	Not used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

TOHx	DESCRIPTION
0X00	HI-Z
0X01	ROH
0X02	Not used
0X03	Not used
0X04	Not used
0X05	Not used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL5**
Register Description: **Control Register 5 Serial Data Overhead Interface**
Register Offset: **0x000C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TSER3	TSER2	TSER1	TSER0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: These bits are unused.

Bits 3 to 0: TSERx: These bits control the source of the TSER signal.

TSERx	DESCRIPTION
0X00	HI-Z
0X01	RSER
0X02	Not Used
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL6**
Register Description: **Control Register 6 Serial Data Overhead Interface**
Register Offset: **0x000D**

Bit #	7	6	5	4	3	2	1	0
Name	TSOFI3	TSOFI2	TSOFI1	TSOFI0	TCLKI3	TCLKI2	TCLKI1	TCLKI0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: TSOFIx: These bits control the source of the TSOFI signal.

Bits 3 to 0: TCLKIx: These bits control the source of the TCLKI signal.

TSOFIx	DESCRIPTION
0X00	HI-Z
0X01	TSOFO
0X02	RSOFO
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

TCLKIx	DESCRIPTION
0X00	HI-Z
0X01	TCLKO
0X02	RCLKO
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

DS3170 INFORMATION

For more information about the DS3170, refer to the DS3170 data sheet available on our website at www.maxim-ic.com/DS3170. Software downloads are also available for this design kit.

DS3170DK INFORMATION

For more information about the DS3170DK including software downloads, consult the DS3170DK data sheet available on our website at www.maxim-ic.com/DS3170DK.

TECHNICAL SUPPORT

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

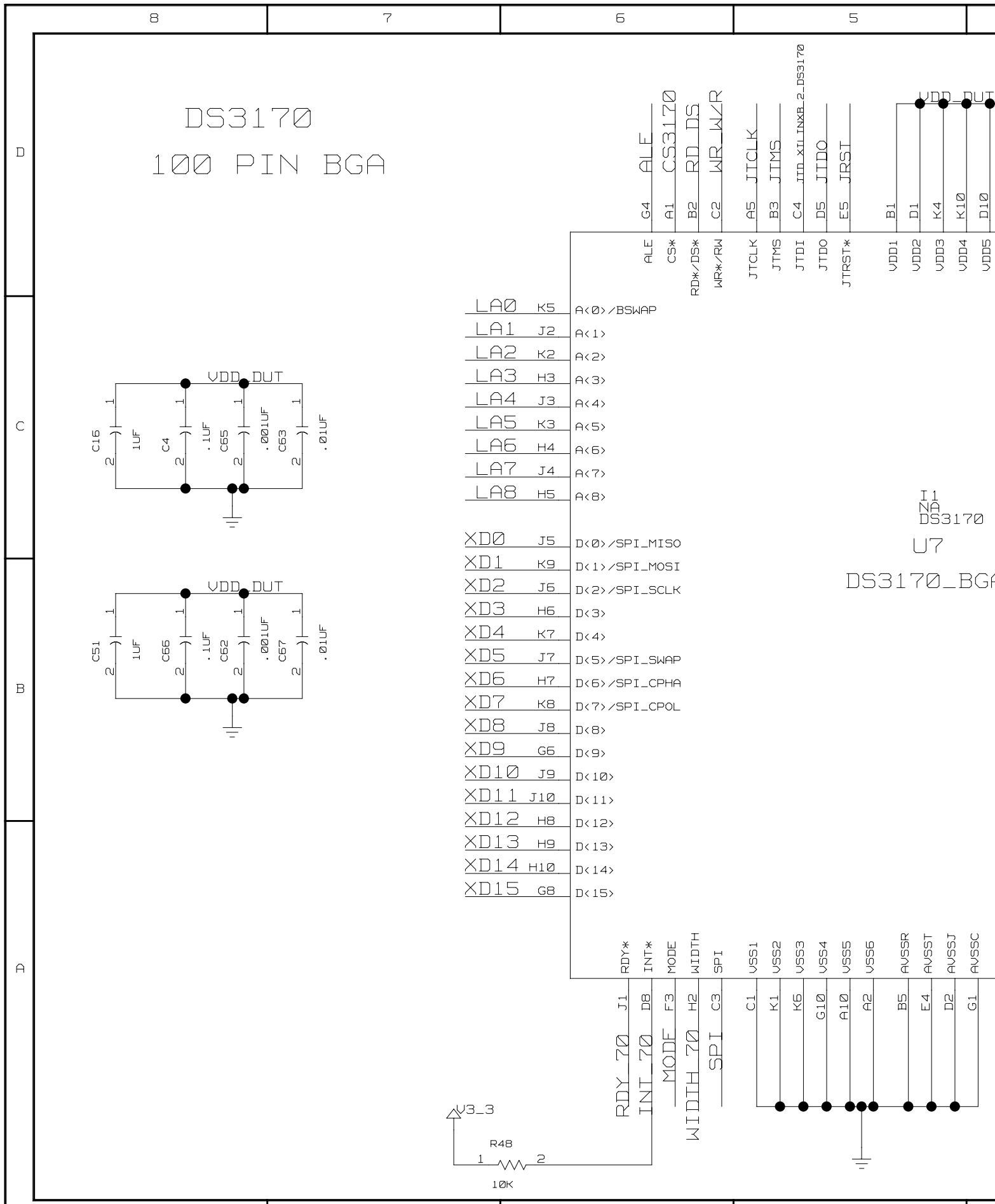
SCHEMATICS

The DS3170DK schematics are featured in the following 23 pages.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

DS3170 DES

CREATED
DALLAS SEMICO
JUNE 26, 2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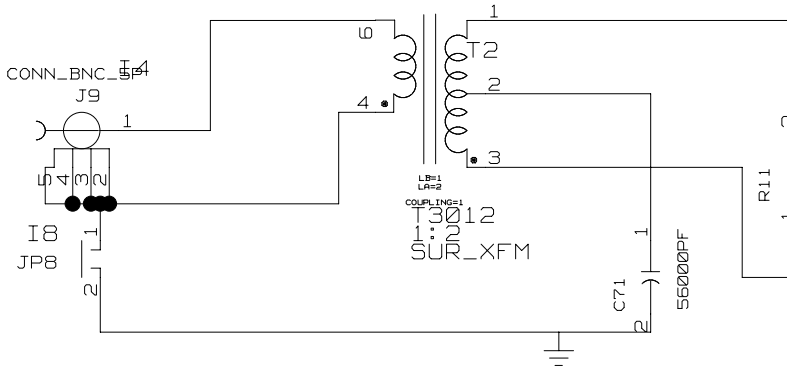
100 PIN BGA
VDD_DUT
C16
1UF
C4
.1UF
C65
.001UF
C63
.01UF
C51
1UF
C66
.1UF
C62
.001UF
C67
.01UF
ALE G4
CS* A1
RD*/DS* B2
WR*/RW C2
JTCLK A5
JTMS B3
JTDI C4
JTDO D5
JTRST* E5
VDD1 B1
VDD2 D1
VDD3 K4
VDD4 K10
VDD5 D10
LA0 K5 A<0>/BSWAP
LA1 J2 A<1>
LA2 K2 A<2>
LA3 H3 A<3>
LA4 J3 A<4>
LA5 K3 A<5>
LA6 H4 A<6>
LA7 J4 A<7>
LA8 H5 A<8>
XD0 J5 D<0>/SPI_MISO
XD1 K9 D<1>/SPI_MOSI
XD2 J6 D<2>/SPI_SCLK
XD3 H6 D<3>
XD4 K7 D<4>
XD5 J7 D<5>/SPI_SWAP
XD6 H7 D<6>/SPI_CPHA
XD7 K8 D<7>/SPI_CPOL
XD8 J8 D<8>
XD9 G6 D<9>
XD10 J9 D<10>
XD11 J10 D<11>
XD12 H8 D<12>
XD13 H9 D<13>
XD14 H10 D<14>
XD15 G8 D<15>
U7
DS3170_BGA
RDY* J1
INT* D8
MODE F3
WIDTH H2
SPI C3
VSS1 C1
VSS2 K1
VSS3 K6
VSS4 G10
VSS5 A10
VSS6 A2
AVSSR B5
AVSST E4
AVSSJ D2
AVSSC G1
RDY_70
INT_70
MODE
WIDTH_70
SPI
3V3_3
R48
10K

DS3170

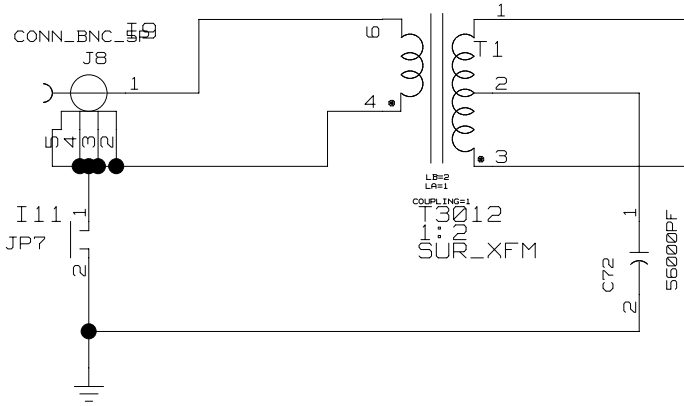
100 PIN BGA

LIU INTERFACE

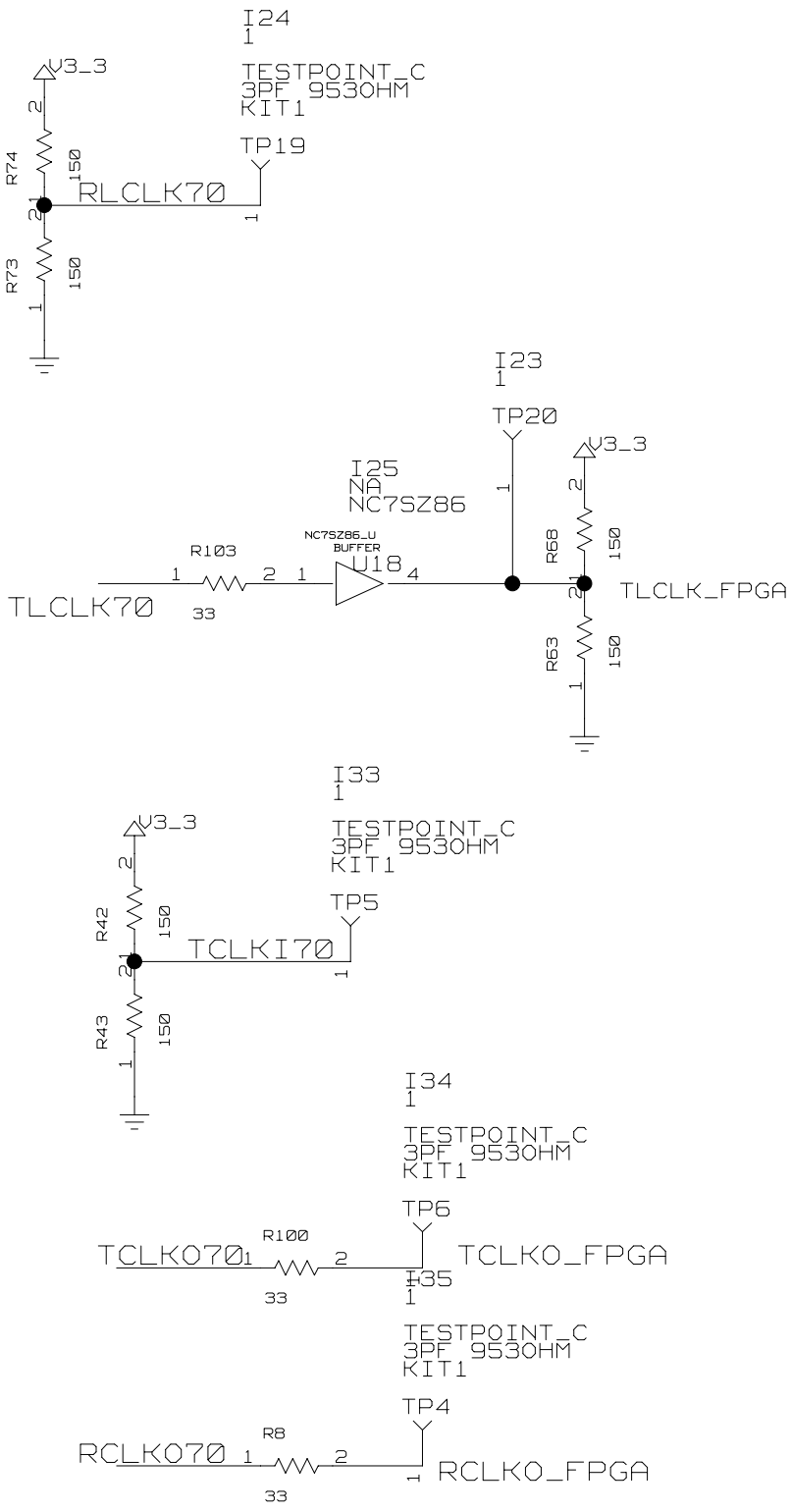
TRANSMIT

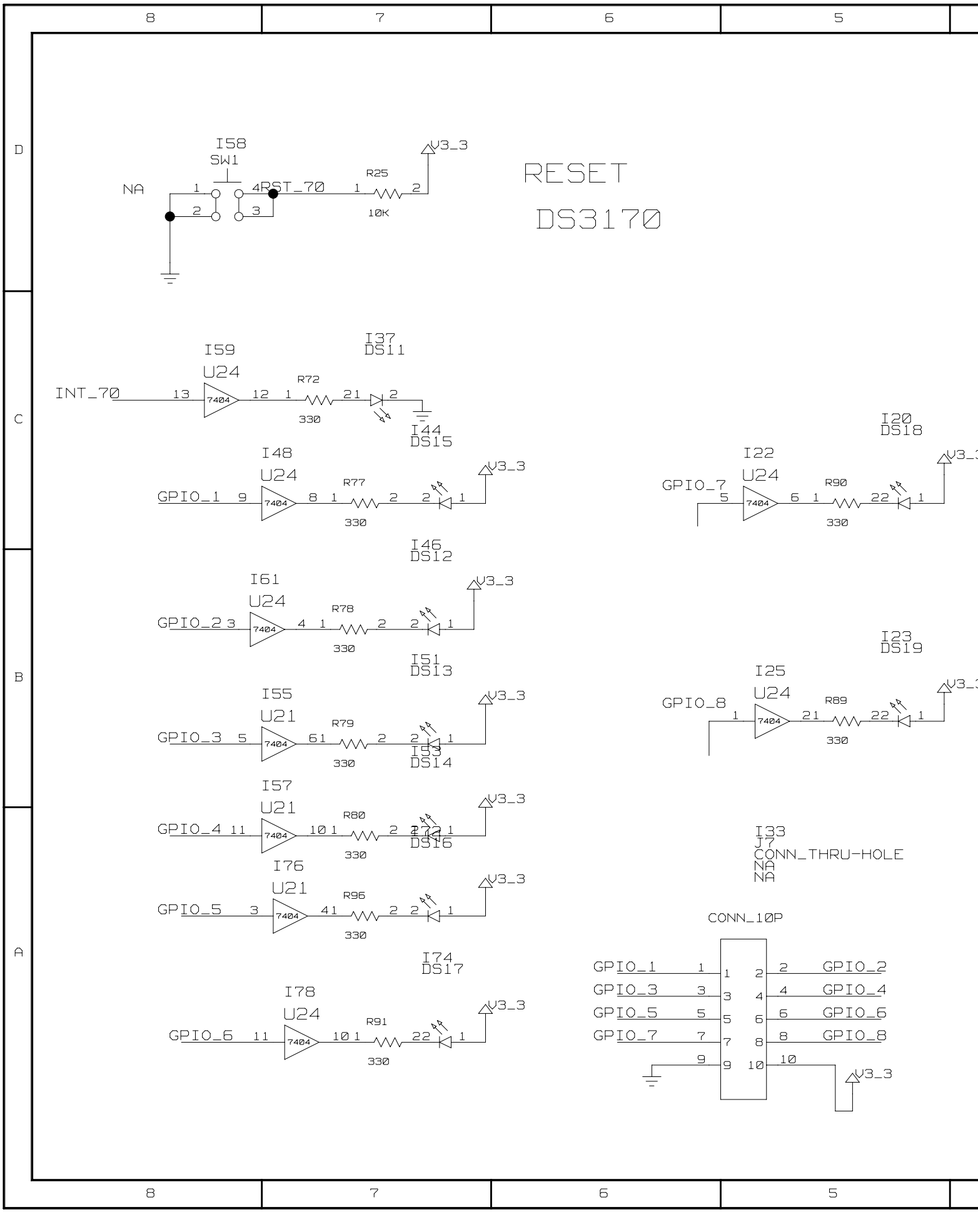


RECEIVE



TCLK/RCLK TERMINATION

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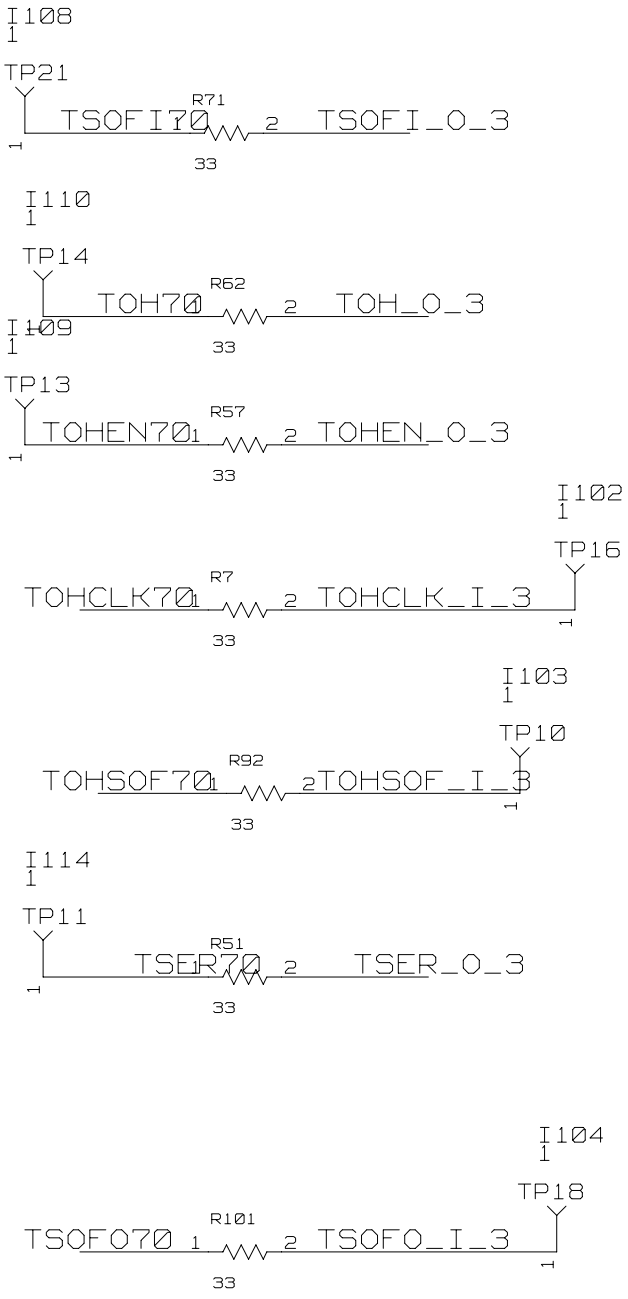
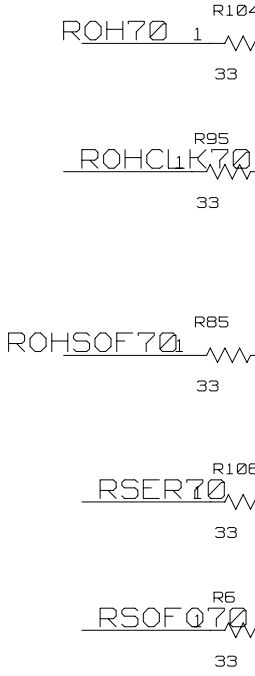
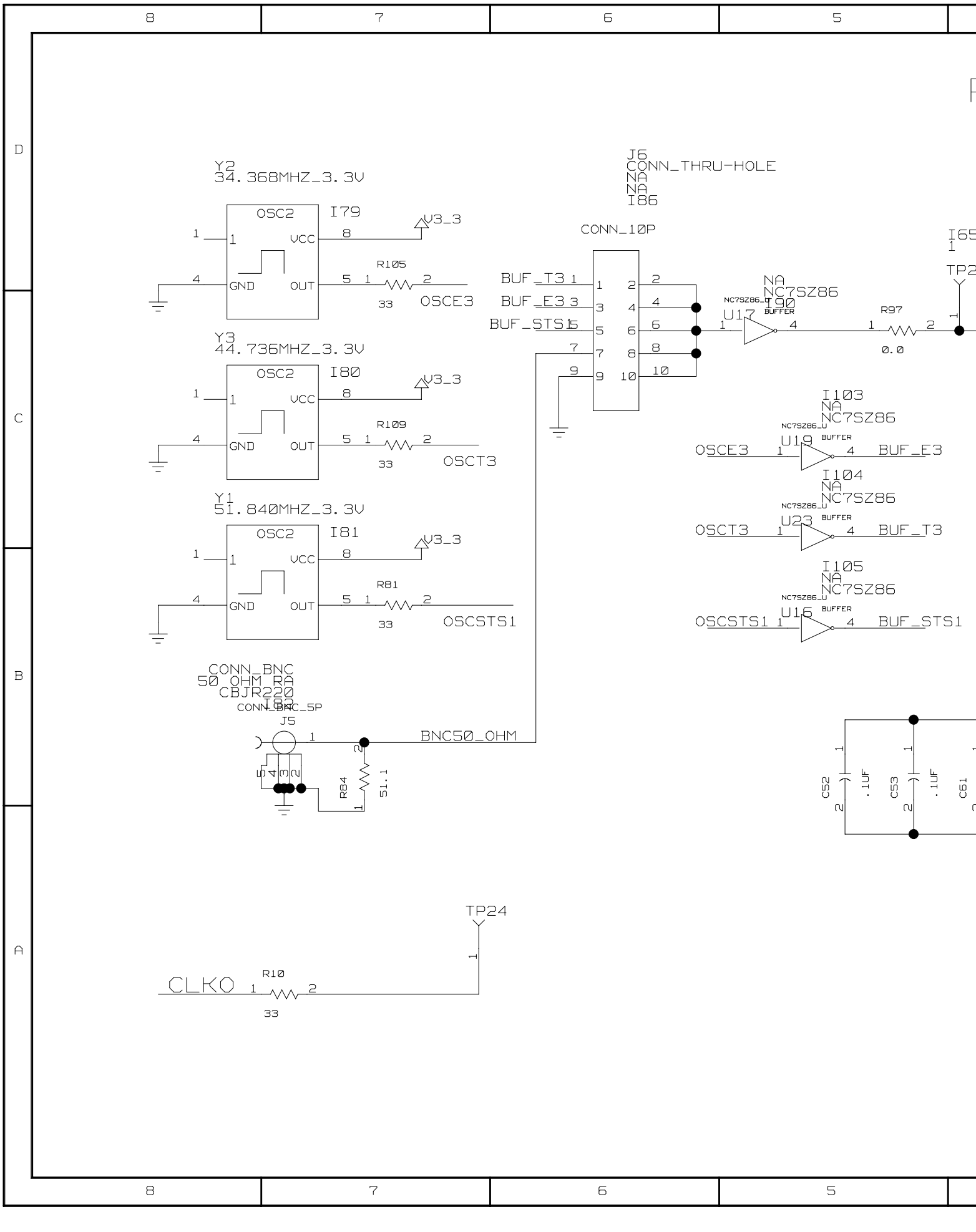
7
6
5
D
C
B
A
I58
SW1
NA
RST_70
R25
10K
V3_3
RESET
DS3170
I59
U24
INT_70
7404
R72
330
I37
DS11
I44
DS15
I48
U24
GPIO_1
R77
330
I46
DS12
I61
U24
GPIO_2
R78
330
I51
DS13
I55
U21
GPIO_3
R79
330
I53
DS14
I57
U21
GPIO_4
R80
330
I76
U21
GPIO_5
R96
330
I74
DS17
I78
U24
GPIO_6
R91
330
I20
DS18
I22
U24
GPIO_7
R90
330
I23
DS19
I25
U24
GPIO_8
R89
330
I33
J7
CONN_THRU-HOLE
NA
NA
CONN_10P
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8

DS3170

MISC TELECOM TER



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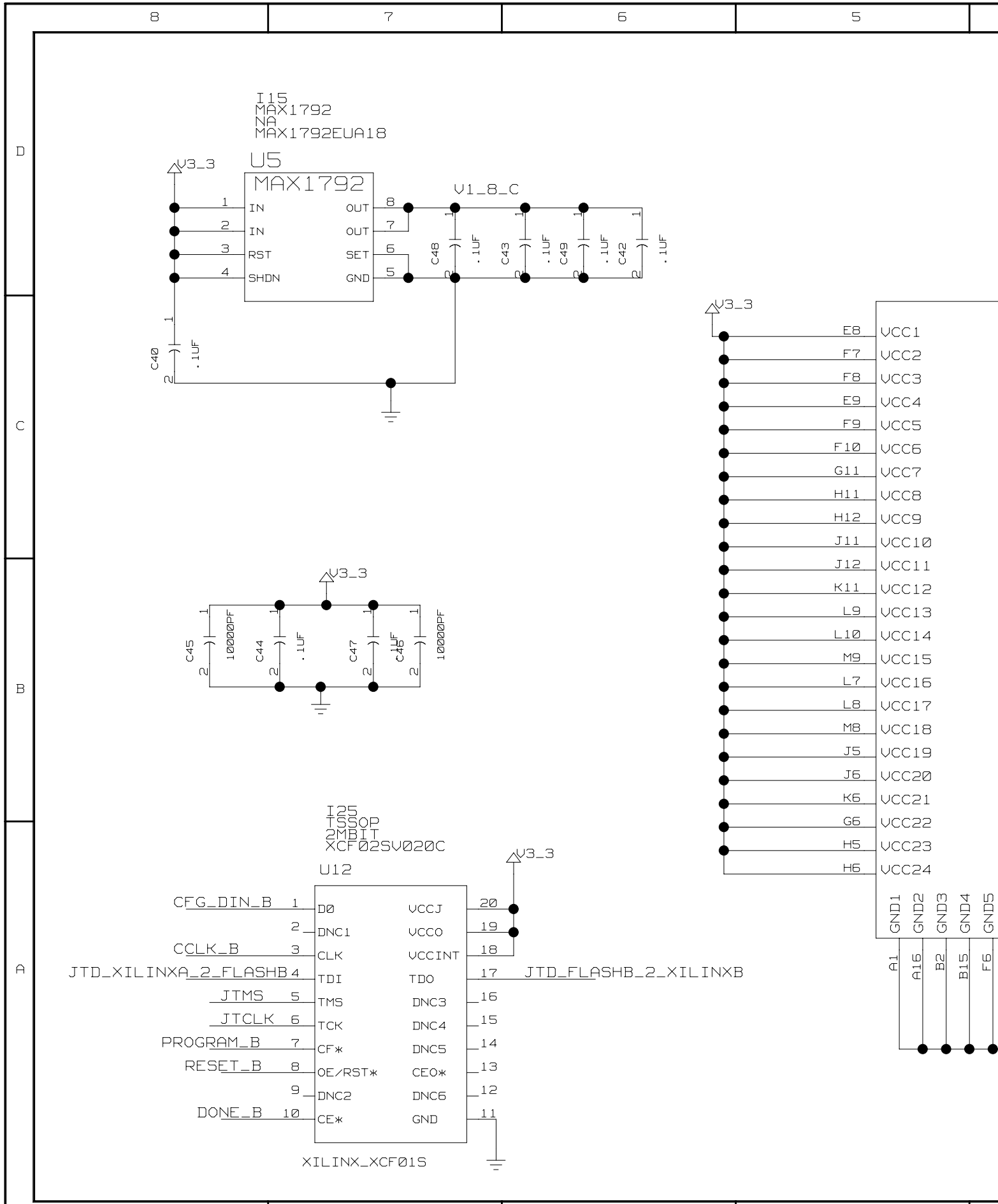
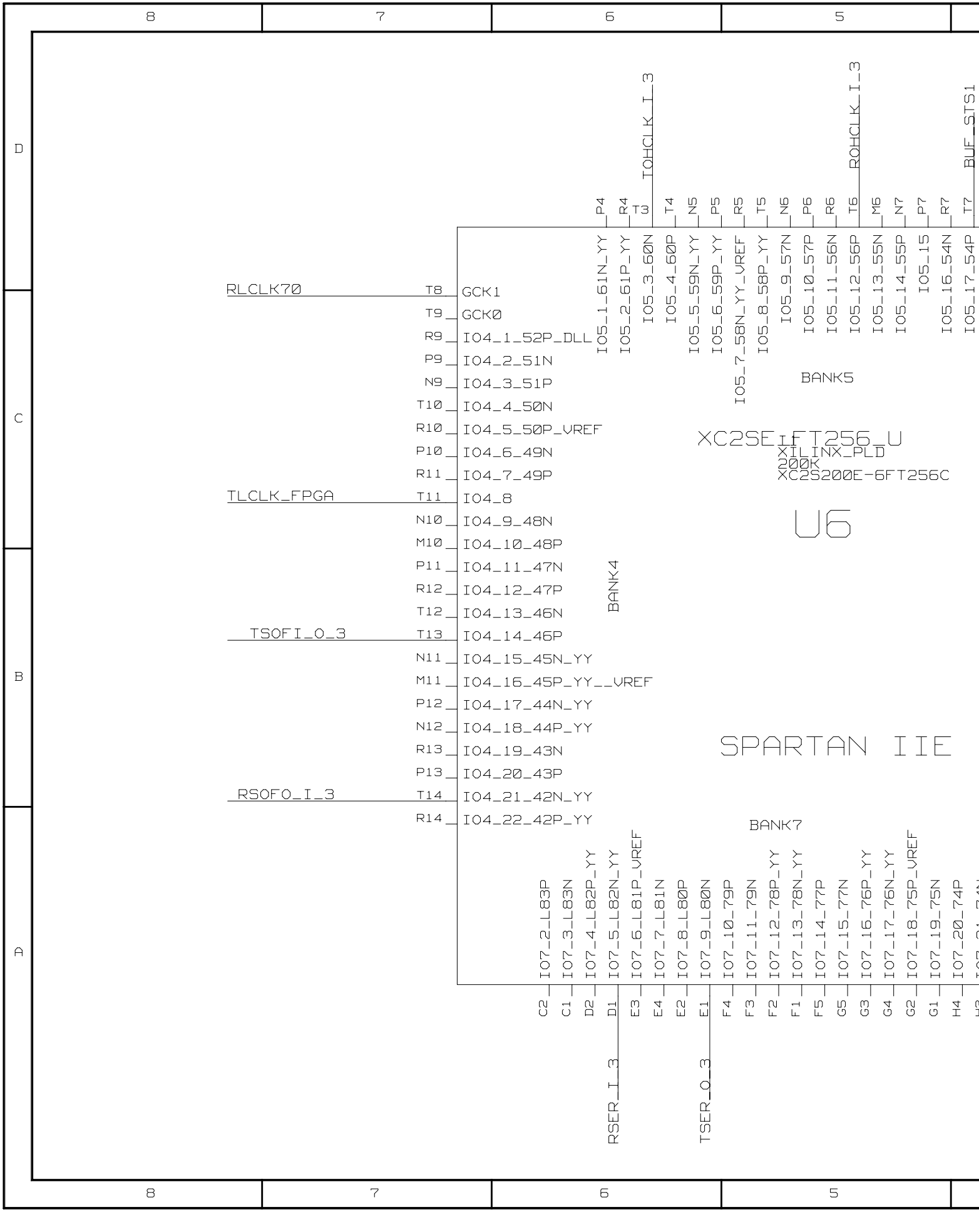
34.368MHZ_3.3V
OSC2
I79
VCC
GND
OUT
V3_3
R105
33
OSCE3
Y3
44.736MHZ_3.3V
I80
R109
OSCT3
Y1
51.840MHZ_3.3V
I81
R81
OSCSTS1
CONN_BNC
50_OHM_RA
CBJR220
I82
CONN_BNC_5P
J5
BNC50_OHM
R84
51.1
J6
CONN_THRU-HOLE
I86
CONN_10P
BUF_T3
BUF_E3
BUF_STS1
NC7SZ86
BUFFER
U17
I90
R97
0.0
I65
TP2
I103
U19
OSCE3
BUF_E3
I104
U23
OSCT3
BUF_T3
I105
U15
OSCSTS1
BUF_STS1
C52
C53
C61
.1UF
TP24
CLKO
R10
33


I15
MAX1792
ZD
MAX1792EUA18
U5
MAX1792
V3_3
V1_8_C
IN
IN
RST
SHDN
OUT
OUT
SET
GND
C40
C48
C43
C49
C42
.1UF
10000PF
C45
C44
C47
C46
I25
TSSOP
2MBIT
XCF02SV020C
U12
CFG_DIN_B
CCLK_B
JTD_XILINXA_2_FLASHB
JTMS
JTCLK
PROGRAM_B
RESET_B
DONE_B
D0
DNC1
CLK
TDI
TMS
TCK
CF*
OE/RST*
DNC2
CE*
VCCJ
VCCO
VCCINT
TDO
DNC3
DNC4
DNC5
CEO*
DNC6
GND
JTD_FLASHB_2_XILINXB
XILINX_XCF01S
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
GND1
GND2
GND3
GND4
GND5
A1
A16
B2
B15
F6

8
7
6
5
D
C
B
A
TCLKO_FPGA
LA0
LA1
LA2
LA3
LA5
LA6
LA8
LA9
LA7
LA4
RPOS_70
TPOS_I_3
INT_BRD
C8 GCK3
D8 IO0_1_8N_DLL
A7 IO0_2
E7 IO0_3_7P
D7 IO0_4_7N_VREF
C7 IO0_5_6P
B7 IO0_6_6N
A6 IO0_7
B6 IO0_8_5P
C6 IO0_9_5N
A5 IO0_10_4P
B5 IO0_11_4N
D6 IO0_12_3P
E6 IO0_13_3N
D5 IO0_14_2P_YY
C5 IO0_15_2N_YY_VREF
B4 IO0_16_1P_YY
C4 IO0_17_1N_YY
A4 IO0_18_0P_YY
A3 IO0_19_0N_YY
B3 IO0_20
BANK0
P15 IO3_1_41N_YY_INIT
P16 IO3_2_41P_YYD7
N15 IO3_3_40N
N16 IO3_4_40P
N14 IO3_5_39N
M14 IO3_6_39P
M15 IO3_7_38N_VREF
M16 IO3_8_38P
BUF_E3
M13 IO3_9
L14 IO3_10
L15 IO3_11_36N
L16 IO3_12_36PD6
L13 IO3_13_35N_YYD5
K14 IO3_14_35P_YY
K15 IO3_15_34N
K16 IO3_16_34P
L12 IO3_17_33N
K12 IO3_18_33P
BANK3
B8 RCLKO_FPGA
A14
A13 RNFG_70
B13
C12
B12
A12 TNFG_I_3
D12
E11
D11 XD7
C11 XD6
B11 XD5
A11 XD4
E10 XD3
D10 XD2
C10 XD1
B10 XD0
A10
GCK2
IO1_1_18P_YY_CS
IO1_2_18N_YY_WR
IO1_3_17P
IO1_4_17N
IO1_5_16P_YY
IO1_6_16N_YY
IO1_7_15P_YY_VREF
IO1_8_15N_YY
IO1_9_14P
IO1_10_14N
IO1_11_13P
IO1_12_13N
IO1_13_12P
IO1_14_12N
IO1_15
IO1_16_11P
IO1_17_11N
BANK1
I1
XILINX_PLD
200K
XC2S200E-6FT256C
XC2S
U6
SPARTAN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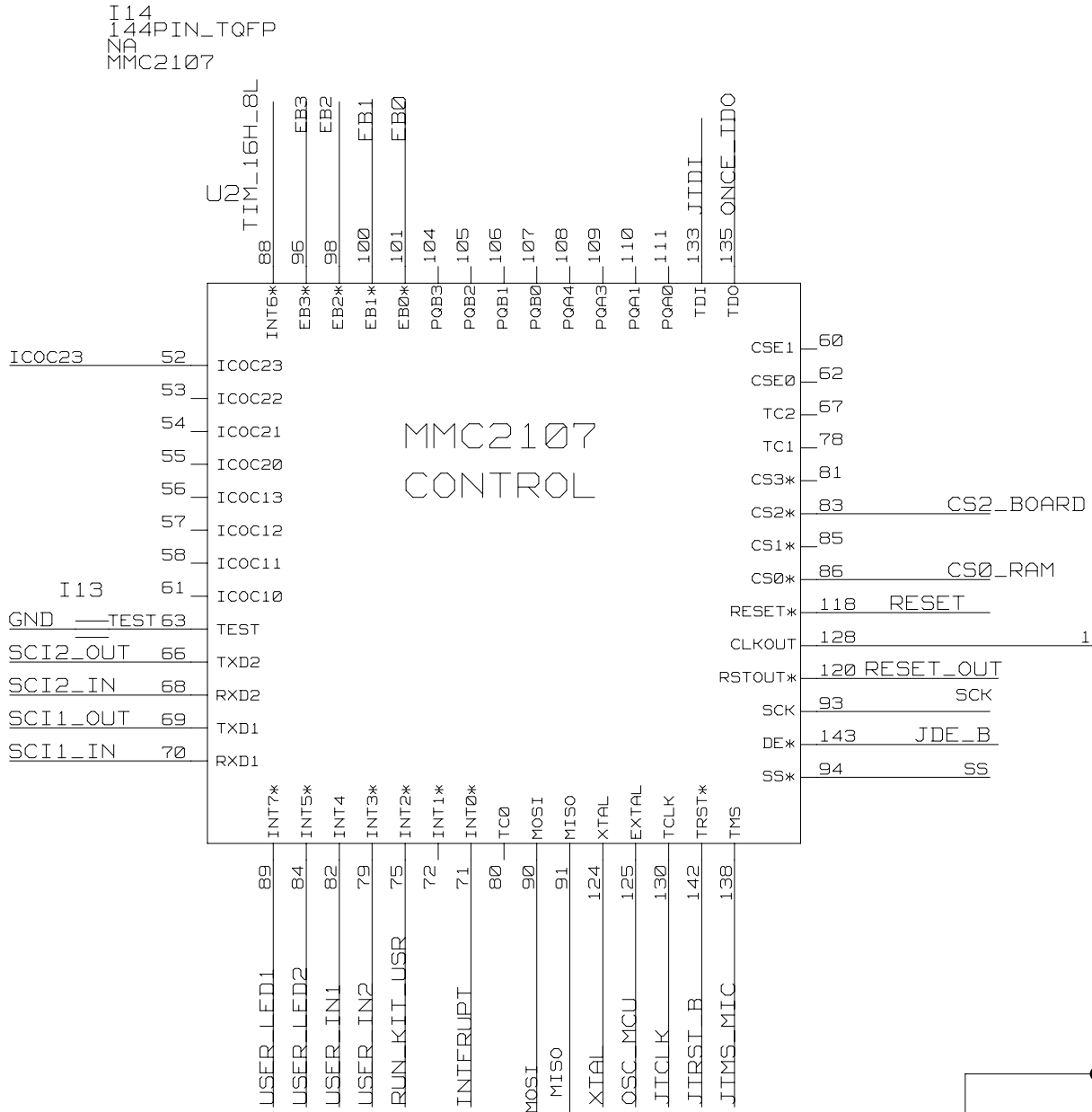
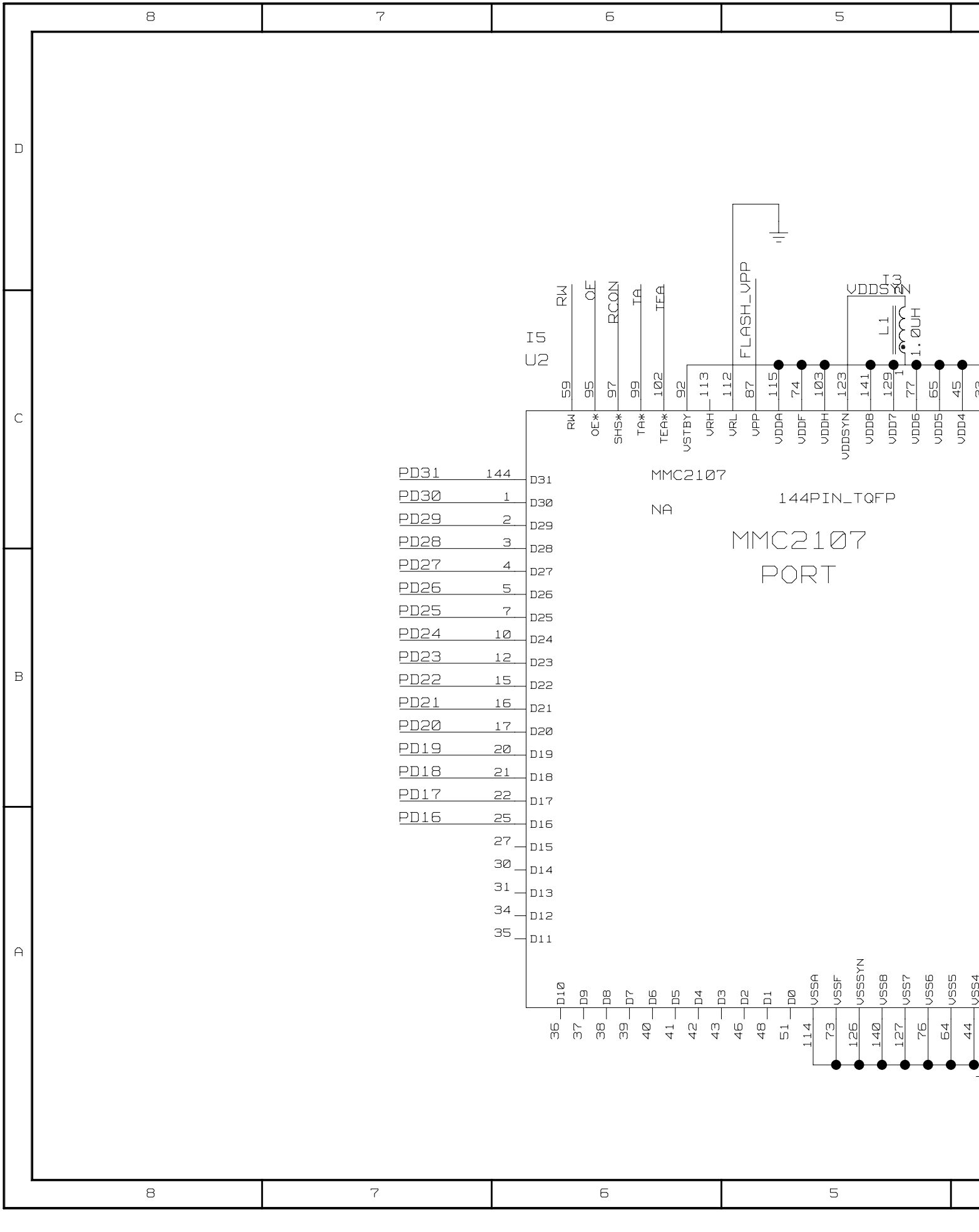
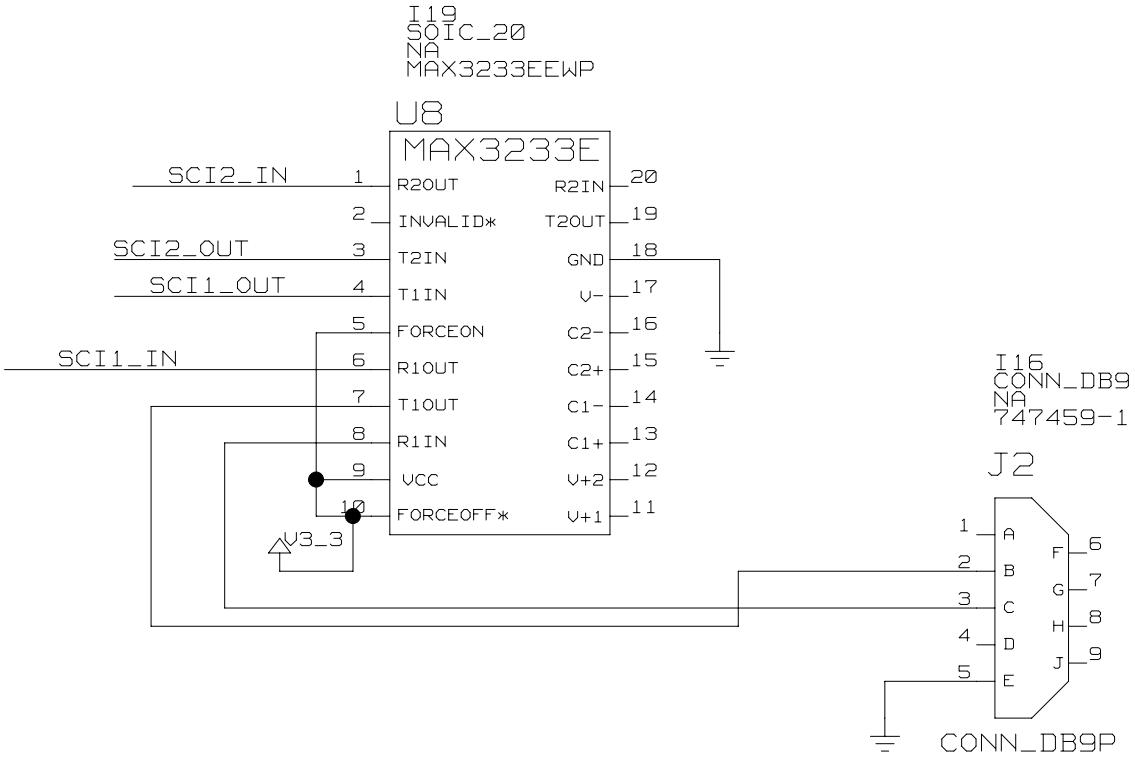
7
6
5
D
C
B
A
RLCLK70
TLCLK_FPGA
TSOFI_O_3
RSOFO_I_3
T8 GCK1
T9 GCK0
R9 IO4_1_52P_DLL
P9 IO4_2_51N
N9 IO4_3_51P
T10 IO4_4_50N
R10 IO4_5_50P_VREF
P10 IO4_6_49N
R11 IO4_7_49P
T11 IO4_8
N10 IO4_9_48N
M10 IO4_10_48P
P11 IO4_11_47N
R12 IO4_12_47P
T12 IO4_13_46N
T13 IO4_14_46P
N11 IO4_15_45N_YY
M11 IO4_16_45P_YY__VREF
P12 IO4_17_44N_YY
N12 IO4_18_44P_YY
R13 IO4_19_43N
P13 IO4_20_43P
T14 IO4_21_42N_YY
R14 IO4_22_42P_YY
BANK4
P4 IO5_1_61N_YY
R4 IO5_2_61P_YY
T3 IO5_3_60N TOHCLK_I_3
T4 IO5_4_60P
N5 IO5_5_59N_YY
P5 IO5_6_59P_YY
R5 IO5_7_58N_YY_VREF
T5 IO5_8_58P_YY
N6 IO5_9_57N
P6 IO5_10_57P
R6 IO5_11_56N
T6 IO5_12_56P ROHCLK_I_3
M6 IO5_13_55N
N7 IO5_14_55P
P7 IO5_15
R7 IO5_16_54N
T7 IO5_17_54P BUF_STS1
BANK5
XC2SE IT FT256_U
XILINX_PLD
200K
XC2S200E-6FT256C
U6
SPARTAN IIE
BANK7
C2 IO7_2_L83P
C1 IO7_3_L83N
D2 IO7_4_L82P_YY
D1 IO7_5_L82N_YY
E3 IO7_6_L81P_VREF
E4 IO7_7_L81N
E2 IO7_8_L80P
E1 IO7_9_L80N
F4 IO7_10_79P
F3 IO7_11_79N
F2 IO7_12_78P_YY
F1 IO7_13_78N_YY
F5 IO7_14_77P
G5 IO7_15_77N
G3 IO7_16_76P_YY
G4 IO7_17_76N_YY
G2 IO7_18_75P_VREF
G1 IO7_19_75N
H4 IO7_20_74P
RSER_I_3
TSER_O_3

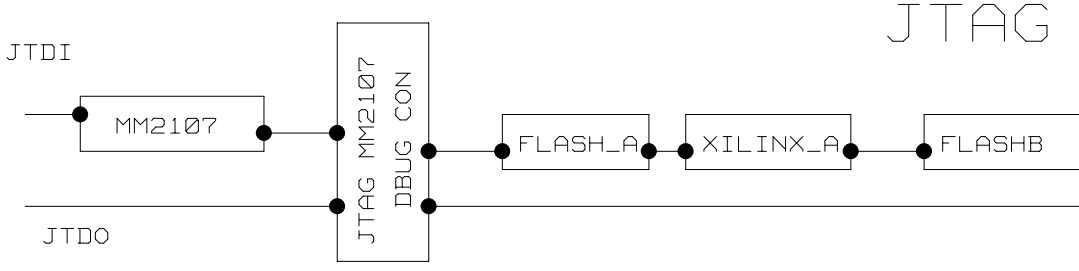

I14
144PIN_TQFP
ZMD
MMC2107
U2
TIM_16H_8L
MMC2107
CONTROL
INT6*
EB3*
EB2*
EB1*
EB0*
PQB3
PQB2
PQB1
PQB0
PQA4
PQA3
PQA1
PQA0
TDI
TDO
EB3
EB2
EB1
EB0
JTDI
ONCE_TDO
ICOC23
ICOC22
ICOC21
ICOC20
ICOC13
ICOC12
ICOC11
ICOC10
TEST
TXD2
RXD2
TXD1
RXD1
I13
GND
TEST
SCI2_OUT
SCI2_IN
SCI1_OUT
SCI1_IN
CSE1
CSE0
TC2
TC1
CS3*
CS2*
CS1*
CS0*
RESET*
CLKOUT
RSTOUT*
SCK
DE*
SS*
CS2_BOARD
CS0_RAM
RESET
RESET_OUT
SCK
JDE_B
SS
R15
33
INT7*
INT5*
INT4
INT3*
INT2*
INT1*
INT0*
TC0
MOSI
MISO
XTAL
EXTAL
TCLK
TRST*
TMS
USER_LED1
USER_LED2
USER_IN1
USER_IN2
RUN_KIT_USR
INTERRUPT
MOSI
MISO
XTAL
OSC_MCU
JTCLK
JTRST_B
JTMS_MIC
C24
0.1UF
C15
0.1UF


U2
I5
RW
OE
RCON
TA
TEA
FLASH_VPP
VDDSYN
L1
1.0UH
MMC2107
144PIN_TQFP
NA
MMC2107
PORT
PD31 144 D31
PD30 1 D30
PD29 2 D29
PD28 3 D28
PD27 4 D27
PD26 5 D26
PD25 7 D25
PD24 10 D24
PD23 12 D23
PD22 15 D22
PD21 16 D21
PD20 17 D20
PD19 20 D19
PD18 21 D18
PD17 22 D17
PD16 25 D16
27 D15
30 D14
31 D13
34 D12
35 D11
RW 59
OE* 95
SHS* 97
TA* 99
TEA* 102
VSTBY 92
VRH 113
VRL 112
VPP 87
VDDA 115
VDDF 74
VDDH 103
VDDSYN 123
VDD8 141
VDD7 129
VDD6 77
VDD5 65
VDD4 45
D10 36
D9 37
D8 38
D7 39
D6 40
D5 41
D4 42
D3 43
D2 46
D1 48
D0 51
VSSA 114
VSSF 73
VSSSYN 126
VSS8 140
VSS7 127
VSS6 76
VSS5 64
VSS4 44

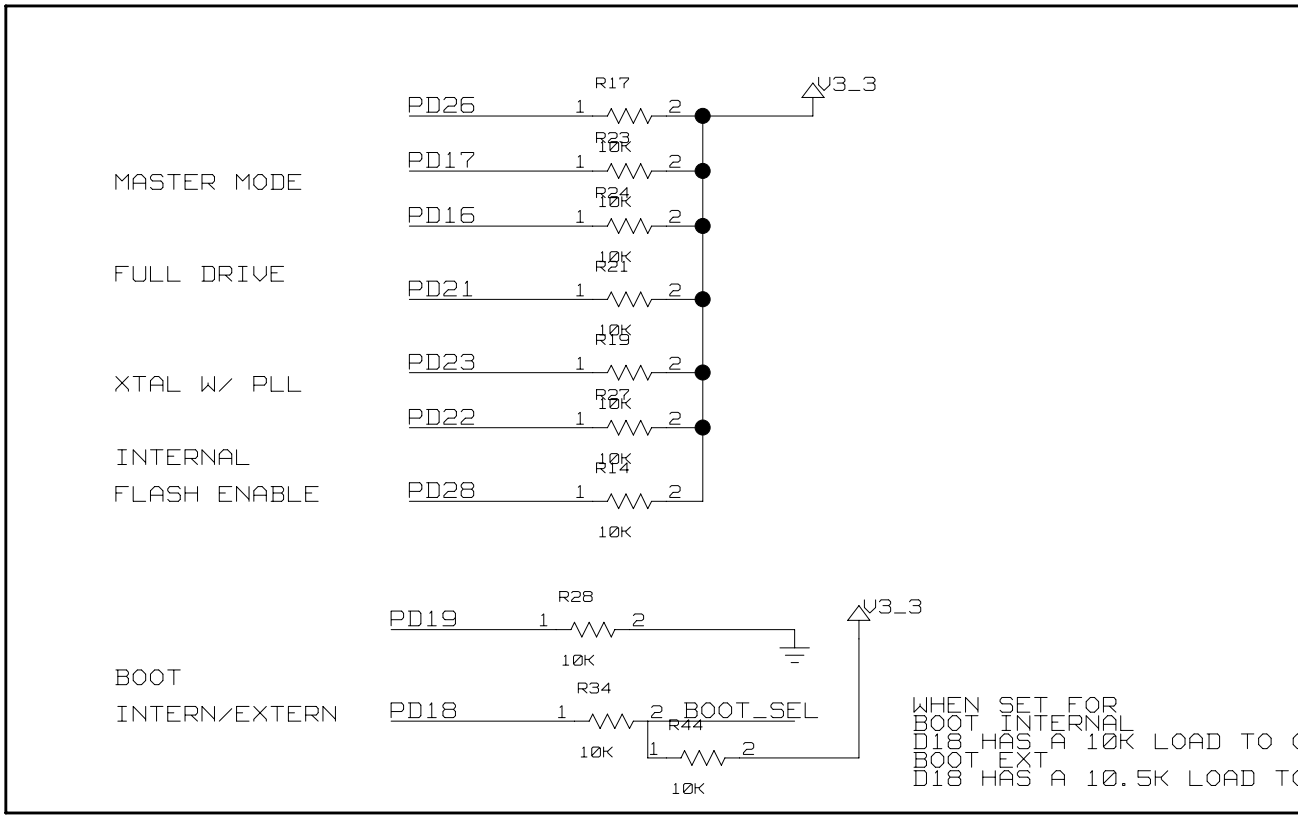
SERIAL INTERFACE

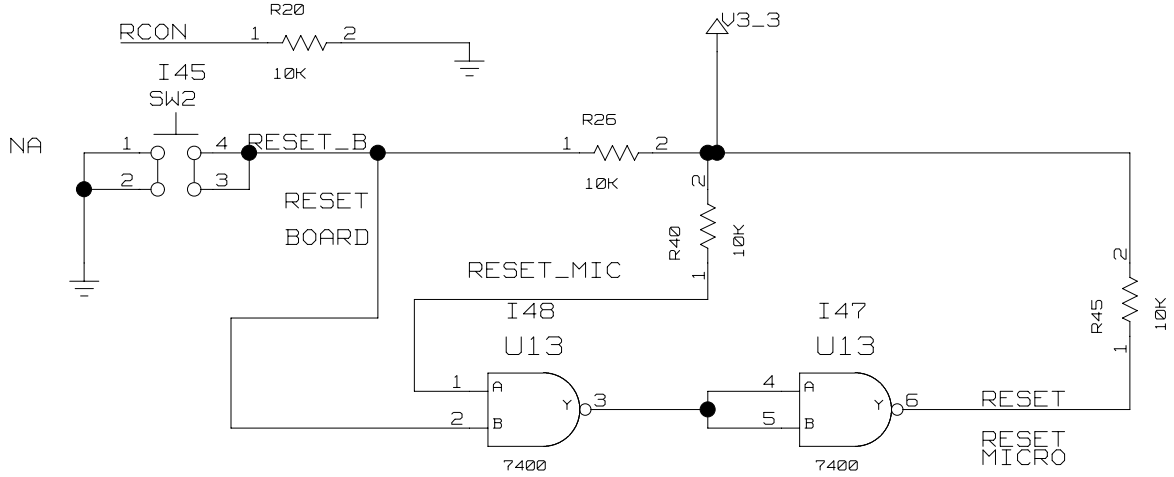


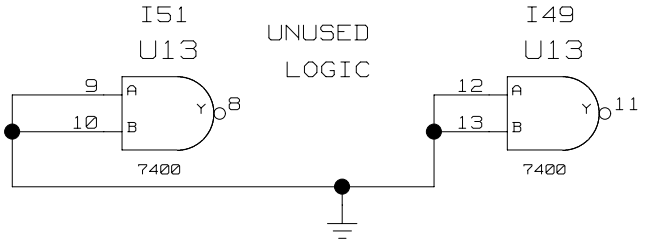
JTAG

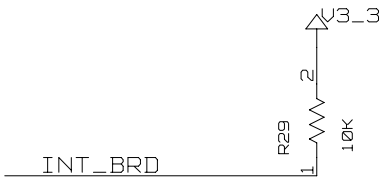


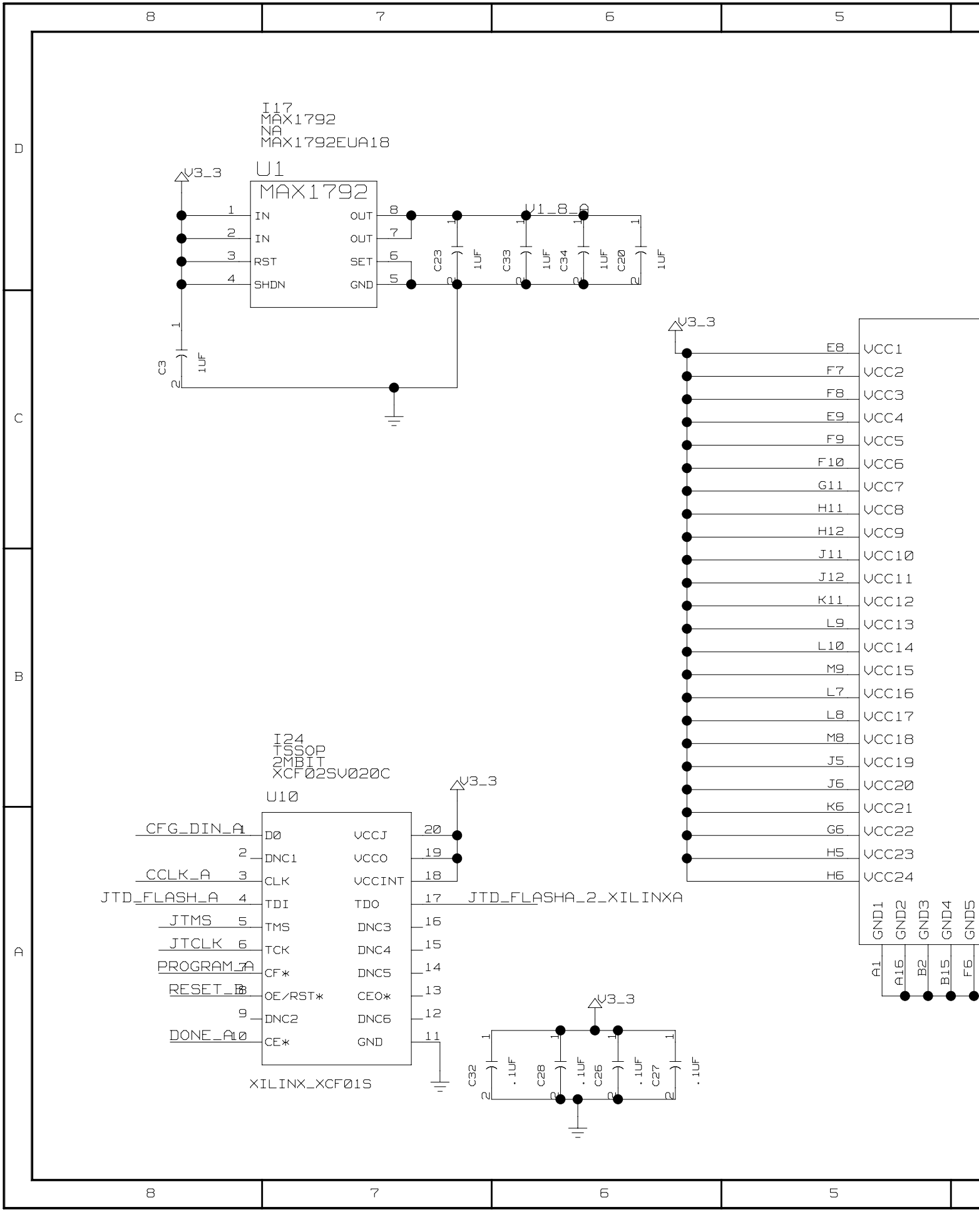
RESET CONFIGURATION

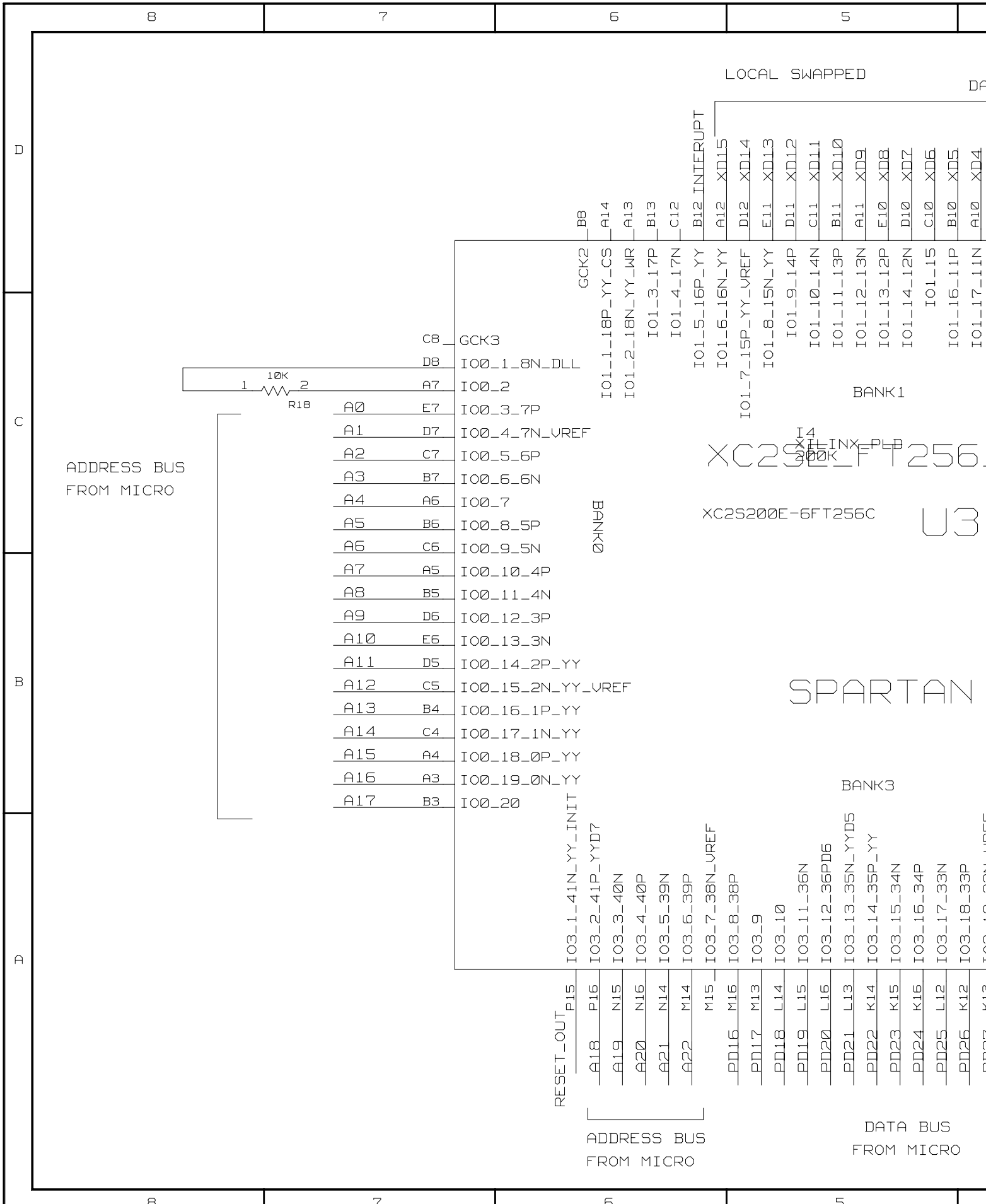


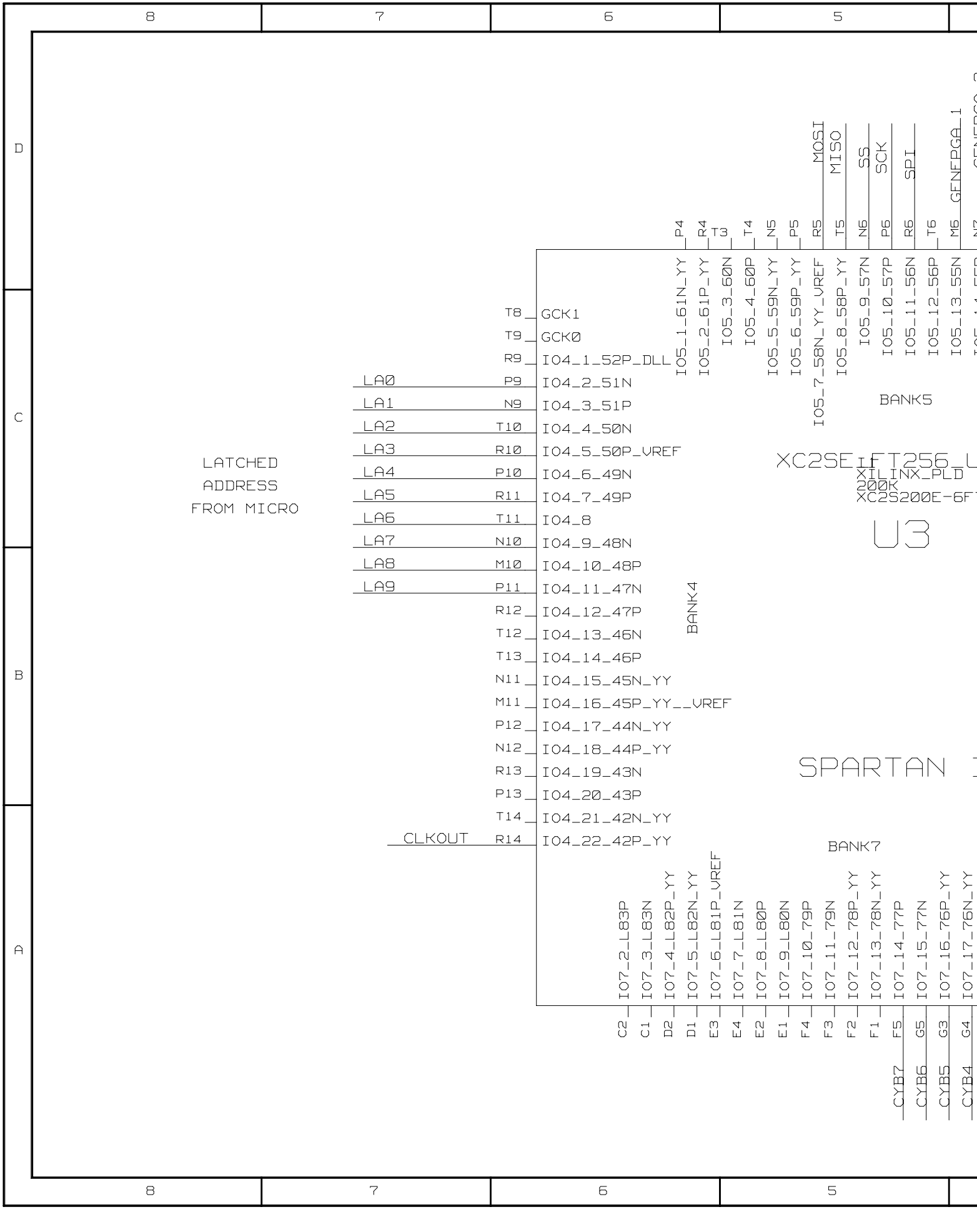


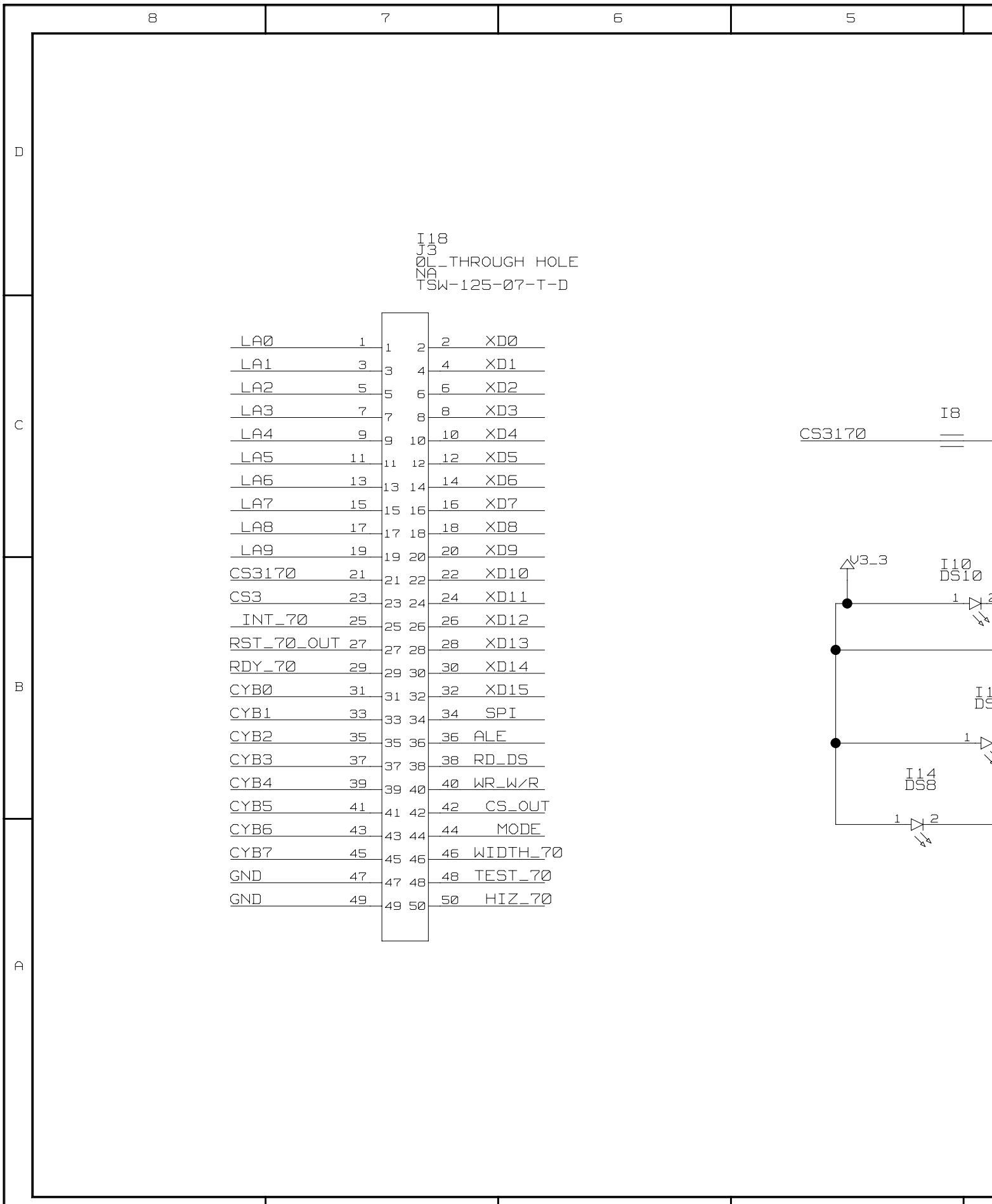


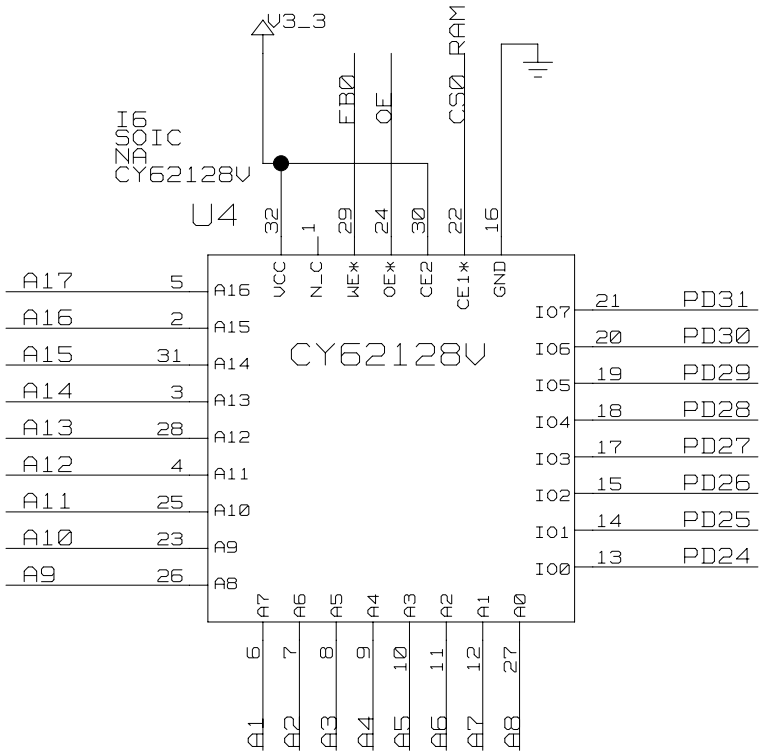


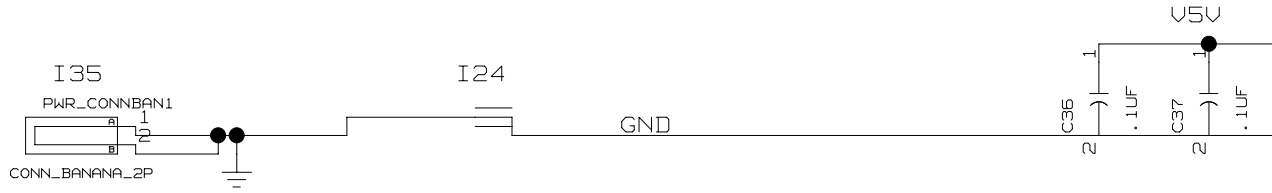

I17
MAX1792
NA
MAX1792EUA18
U1
MAX1792
V3_3
IN
IN
RST
SHDN
OUT
OUT
SET
GND
V1_8_D
C3
C23
C33
C34
C20
1UF
I24
TSSOP
2MBIT
XCF02SV020C
U10
V3_3
CFG_DIN_A
CCLK_A
JTD_FLASH_A
JTMS
JTCLK
PROGRAM_A
RESET_B
DONE_A
D0
DNC1
CLK
TDI
TMS
TCK
CF*
OE/RST*
DNC2
CE*
VCCJ
VCCO
VCCINT
TDO
DNC3
DNC4
DNC5
CEO*
DNC6
GND
JTD_FLASHA_2_XILINXA
XILINX_XCF01S
C32
C28
C26
C27
.1UF
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
GND1
GND2
GND3
GND4
GND5
A1
A16
B2
B15
F6

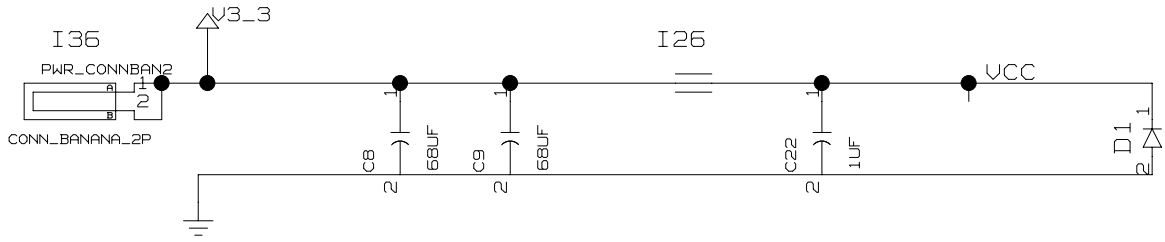

LOCAL SWAPPED
BANK1
BANK0
BANK3
XILINX PLD
XC2S200E-6FT256C
SPARTAN
ADDRESS BUS
FROM MICRO
DATA BUS
FROM MICRO
10K
R18
I4
U3

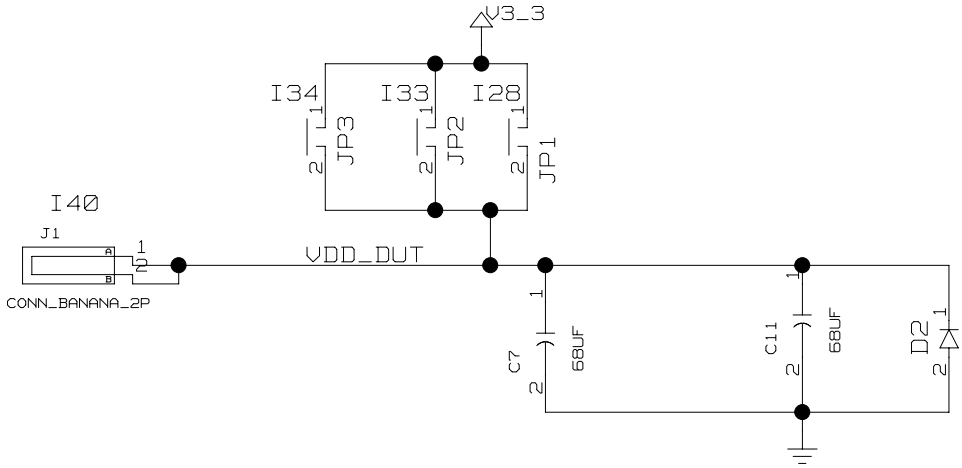

LATCHED
ADDRESS
FROM MICRO
LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
CLKOUT
BANK4
BANK5
BANK7
XC2SE
FT256_L
XILINX_PLD
XC2S200E-6F
U3
SPARTAN
MOSI
MISO
SS
SCK
SPI
GFNFPGA_1


I18
J3
0L_THROUGH HOLE
NA
TSW-125-07-T-D
LA0 1
LA1 3
LA2 5
LA3 7
LA4 9
LA5 11
LA6 13
LA7 15
LA8 17
LA9 19
CS3170 21
CS3 23
INT_70 25
RST_70_OUT 27
RDY_70 29
CYB0 31
CYB1 33
CYB2 35
CYB3 37
CYB4 39
CYB5 41
CYB6 43
CYB7 45
GND 47
GND 49
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34
35 36
37 38
39 40
41 42
43 44
45 46
47 48
49 50
2 XD0
4 XD1
6 XD2
8 XD3
10 XD4
12 XD5
14 XD6
16 XD7
18 XD8
20 XD9
22 XD10
24 XD11
26 XD12
28 XD13
30 XD14
32 XD15
34 SPI
36 ALE
38 RD_DS
40 WR_W/R
42 CS_OUT
44 MODE
46 WIDTH_70
48 TEST_70
50 HIZ_70
I8
CS3170
V3_3
I10
DS10
I14
DS8


V3_3
CS0_RAM
FB0
OE
I6
SSDOIC
CY62128V
U4
32
1
29
24
30
22
16
VCC
N_C
WE*
OE*
CE2
CE1*
GND
A17
A16
A15
A14
A13
A12
A11
A10
A9
5
2
31
3
28
4
25
23
26
A16
A15
A14
A13
A12
A11
A10
A9
A8
CY62128V
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
21
20
19
18
17
15
14
13
PD31
PD30
PD29
PD28
PD27
PD26
PD25
PD24
A7
A6
A5
A4
A3
A2
A1
A0
6
7
8
9
10
11
12
27
A1
A2
A3
A4
A5
A6
A7
A8


I35
PWR_CONNBAN1
CONN_BANANA_2P
I24
GND
V5V
C36
.1UF
C37
.1UF


I36
PWR_CONNBAN2
CONN_BANANA_2P
V3_3
I26
VCC
C8
68UF
C9
68UF
C22
1UF
D1


V3_3
I34
I33
I28
JP3
JP2
JP1
I40
J1
CONN_BANANA_2P
VDD_DUT
C7
68UF
C11
68UF
D2

8 7 6 5

D

C

B

A

DESIGN NOTES:

1. 1/20/05 DESIGN / LAYOUT

8 7 6 5

*** Signal Cross-Reference for the entire design ***

A0	12A4<> 16C7<>
A1	12A4<> 16C7<> 19A3<> 19A7<>
A2	12A4<> 16C7<> 19A3<> 19A7<>
A3	12A4<> 16C7<> 19A3<> 19A7<>
A4	12A4<> 16C7<> 19A3<> 19A6<>
A5	12A4<> 16C7<> 19A3<> 19A6<>
A6	12A4<> 16B7<> 19A3<> 19A6<>
A7	12B4<> 16B7<> 19A3<> 19A6<>
A8	12B4<> 16B7<> 19A3<> 19A6<>
A9	12B4<> 16B7<> 19B4<> 19B7<>
A10	12B4<> 16B7<> 19B4<> 19B7<>
A11	12B4<> 16B7<> 19B4<> 19B7<>
A12	12B4<> 16B7<> 19B4<> 19B7<>
A13	12B4<> 16B7<> 19B4<> 19B7<>
A14	12B4<> 16B7<> 19B4<> 19B7<>
A15	12B4<> 16B7<> 19B4<> 19B7<>
A16	12B4<> 16B7<> 19B4<> 19B7<>
A17	12B4<> 16B7<> 19B4<> 19B7<>
A18	12B4<> 16A6<>
A19	12C4<> 16A6<>
A20	12C4<> 16A6<>
A21	12C4<> 16A6<>
A22	12C4<> 16A6<>
ALE	9C2<> 16B2<> 18B6<> 2D6<
BNC50_OHM	7B7<>
BOOT_SEL	14C3<> 16B2<> 14B6<
BUF_E3	7C5<> 7C6<> 9A5<> 7C2<
BUF_STS1	7B5<> 7C6<> 10D4<> 7C1<
BUF_T3	7C5<> 7C6<> 10A4<> 7C2<
CCLK_A	15A8<> 15B1<
CCLK_B	8A8<> 8B1<
CFG_DIN_A	15A8<> 16A2<>
CFG_DIN_B	8A8<> 9A2<>
CLKO	2D4> 7A8<
CLKOUT	17A7<> 11B4<
CS0	17A2<> 18C4>
CS0_RAM	11B5<> 19C3<> 19C6<>
CS2_BOARD	11B5<> 16B2<>
CS3	9C2<> 17B2<> 18B8<>
CS3170	18B8<> 2D6< 18C5<
CS_OUT	17A2<> 18B6<>
CYB0	9B2<> 17A4<> 18B8<>
CYB1	9B2<> 17A4<> 18B8<>
CYB2	9B2<> 17A4<> 18B8<>
CYB3	9B2<> 17A4<> 18B8<>
CYB4	9B2<> 17A4<> 18B8<>
CYB5	9A2<> 17A5<> 18B8<>
CYB6	9A2<> 17A5<> 18A8<>
CYB7	9A2<> 17A5<> 18A8<>
DONE_A	15A2<> 15A8<> 15B1<
DONE_B	8A2<> 8A8<> 8B2<
EB0	11C7<> 16C2<> 19C7<>
EB1	11C7<> 16C2<> 19C3<>
EB2	11C7<> 16C2<>
EB3	11C7<> 16C2<>
FLASH_VPP	14A3<> 12D5<
FPGA_EN	14D3<> 17C3<>
GENFPGA_1	14D3<> 17D4<>
GENFPGA_2	14D3<> 17D4<>
GPIO_1	2A4<> 5A6<> 5C2<> 5C8<
GPIO_2	2A4<> 5A5<> 5C2<> 5B8<
GPIO_3	2A4<> 5A6<> 5B2<> 5B8<
GPIO_4	2A4<> 5A5<> 5B2<> 5A8<
GPIO_5	2A4<> 5A6<> 5B2<> 5A8<
GPIO_6	2A4<> 5A2<> 5A5<> 5B2<> 5A8<
GPIO_7	2A4<> 5A6<> 5B2<> 5C6<
GPIO_8	2A4<> 5A2<> 5A5<> 5B2<> 5B6<
HIZ_70	16B2<> 18A6<> 2A3< 18B2<
ICOC23	11C8<> 16C2<>
INTERUPT	11A7<> 16D6<>
INT_70	2A6<> 16C2<> 18B8<> 5C8<
INT_BRD	9A7<> 16C2<> 14A6<
JDE_B	11B5<> 13C2<>
JRST	2D5< 13B1<

JTCLK	8A8<> 11A6<> 13C3<> 15A8<> 2D5< 8C2< 15B1<
JTDI	11C6<> 13C3<>
JTDO	2D5<> 13C4<
JTD_FLASHA_2_XILINXA	15A6<> 15C1<
JTD_FLASHB_2_XILINXB	8A6<> 8C2<
JTD_FLASH_A	15A8<> 13C4<
JTD_XILINXA_2_FLASHB	8A8<> 15B1>
JTD_XILINXB_2_DS3170	8B2> 2D5<
JTMS	8A8<> 8C2<> 13B4<> 15A8<> 15C1<> 2D5<
JTMS_MIC	11A6<> 13B4<> 13C2<>
JTRST_B	11A6<> 13B2<>
LA0	9C7<> 17C7<> 18C8<> 2C7<
LA1	9C7<> 17C7<> 18C8<> 2C7<
LA2	9C7<> 17C7<> 18C8<> 2C7<
LA3	9B7<> 17C7<> 18C8<> 2C7<
LA4	9B7<> 17C7<> 18C8<> 2C7<
LA5	9B7<> 17C7<> 18C8<> 2C7<
LA6	9B7<> 17C7<> 18C8<> 2C7<
LA7	9B7<> 17B7<> 18C8<> 2C7<
LA8	9B7<> 17B7<> 18C8<> 2C7<
LA9	9B7<> 17B7<> 18B8<>
MISO	11A6<> 17D5<>
MODE	9B2<> 16B2<> 18A6<> 2A6< 18B3<
MOSI	11A6<> 17D5<>
OE	12D6<> 16B2<> 19C3<> 19C6<>
ONCE_TDO	11C6<> 13C4<
OSCE3	7C6<> 7C7<
OSCSTS1	7B6<> 7B6<
OSCT3	7C6<> 7C7<
OSC_MCU	11A6<> 11C2<
PD16	12A7<> 16A5<> 19B2<> 14D7<
PD17	12B7<> 16A5<> 19B2<> 14D7<
PD18	12B7<> 16A5<> 19B2<> 14B7<
PD19	12B7<> 16A5<> 19B2<> 14C7<
PD20	12B7<> 16A5<> 19B2<>
PD21	12B7<> 16A5<> 19B2<> 14C7<
PD22	12B7<> 16A5<> 19B2<> 14C7<
PD23	12B7<> 16A5<> 19B2<> 14C7<
PD24	12B7<> 16A5<> 19B5<>
PD25	12B7<> 16A5<> 19B5<>
PD26	12B7<> 16A4<> 19B5<> 14D7<
PD27	12B7<> 16A4<> 19B5<>
PD28	12B7<> 16A4<> 19B5<> 14C7<
PD29	12C7<> 16A4<> 19B5<>
PD30	12C7<> 16A4<> 19B5<>
PD31	12C7<> 16A4<> 19B5<>
PROGRAM_A	15A8<> 15B1<
PROGRAM_B	8A8<> 8B1<
RCLKO70	2A2> 4A7<
RCLKO_FPGA	4A6<> 9D6<
RCON	12D6<> 14B8<
RDY_70	2A6<> 17B3<> 18B8<>
RD_DS	9B2<> 16C2<> 18B6<> 2D6<
REFCLK70	7C4<> 2D4<
REFCLK_OUTPUT	7C3<> 9A4<>
RESET	11B5<> 14A5<>
RESET_B	8A8<> 9A2<> 9B2<> 14B7<> 15A8<> 16A2<>
RESET_MIC	13C3<> 14A7<
RESET_OUT	11B5<> 16A6<>
RLCLK70	4C7<> 2C2< 10C8<
RNEG_70	4A3<> 9D6<> 2C2<
ROH70	2B2> 6C5<
ROHCLK70	2B2> 6C5<
ROHCLK_I_3	6C4<> 10D5<>
ROHSOF70	2B2> 6C5<
ROHSOF_I_3	6C4<> 9C2<>
ROH_I_3	6C4<> 10B2<>
RPOS_70	4B3<> 9B7<> 2C2<
RSER70	2A2> 6B5<
RSER_I_3	6B4<> 10A6<>
RSOFO70	2A2> 6B5<
RSOFO_I_3	6B4<> 10B8<>
RST_70	5D8<> 16A2<>
RST_70_OUT	16B2<> 18B8<> 2A3<

RUN_KIT_USR
RW
RXN_70
RXP_70
SCI1_IN
SCI1_OUT
SCI2_IN
SCI2_OUT
SCK
SPI
SS
TA
TCLKI70
TCLKO70
TCLKO_FPGA
TEA
TEST
TEST_70
TIM_16H_8L
TLCLK70
TLCLK_FPGA
TNEG_70
TNEG_I_3
TOH70
TOHCLK70
TOHCLK_I_3
TOHEN70
TOHEN_O_3
TOHSOF70
TOHSOF_I_3
TOH_O_3
TPOS_70
TPOS_I_3
TSER70
TSER_O_3
TSOFI70
TSOFI_O_3
TSOFO70
TSOFO_I_3
TXN_70
TXP_70
USER_IN1
USER_IN2
USER_LED1
USER_LED2
V1_8_A
V1_8_C
V5V
VDDSYN
VDD_DUT
VSSSSYN
WIDTH_70
WR_W/R
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XD8
XD9
XD10
XD11
XD12
XD13
XD14
XD15
XTAL

*** Part Cross-Reference for the entire design ***

C1	CAP1	20B4
C2	CAP1	20C3
C3	CAP1	15C8
C4	CAP1	2C8
C5	CAP1	2B2
C6	CAP1	2B1
C7	CAP1	20B7
C8	CAP1	20C7
C9	CAP1	20C6
C10	CAP1	20B3
C11	CAP1	20B6
C12	CAP	11C4
C13	CAP	11C3
C14	CAP1	11A4
C15	CAP1	11A5
C16	CAP1	2C8
C17	CAP1	20C2
C18	CAP1	20A4
C19	CAP1	20A3
C20	CAP1	15D6
C21	CAP1	20A4
C22	CAP1	20C6
C23	CAP1	15D7
C24	CAP1	11A5
C25	CAP1	20B4
C26	CAP1	15A6
C27	CAP1	15A6
C28	CAP1	15A6
C29	CAP1	11A4
C30	CAP1	20A3
C31	CAP1	20A4
C32	CAP1	15A7
C33	CAP1	15D6
C34	CAP1	15D6
C35	CAP	20D4
C36	CAP1	20D5
C37	CAP1	20D5
C38	CAP1	7B2
C39	CAP1	20B3
C40	CAP1	8C8
C41	CAP1	20B4
C42	CAP1	8D6
C43	CAP1	8D6
C44	CAP1	8B8
C45	CAP1	8B8
C46	CAP1	8B7
C47	CAP1	8B7
C48	CAP1	8D7
C49	CAP1	8D6
C50	CAP1	7B3
C51	CAP1	2B8
C52	CAP1	7B5
C53	CAP1	7B5
C54	CAP1	7B3
C55	CAP1	7A3
C56	CAP1	7B4
C57	CAP1	20C4
C58	CAP1	20B3
C59	CAP1	7B3
C60	CAP1	7A3
C61	CAP1	7B4
C62	CAP1	2B8
C63	CAP1	2C7
C64	CAP1	2B1
C65	CAP1	2C8
C66	CAP1	2B8
C67	CAP1	2B7
C68	CAP1	7A3
C69	CAP1	20C4
C70	CAP1	7A3
C71	CAP1	3B5
C72	CAP1	3A5
C73	CAP1	7A2
C74	CAP1	20A3
C75	CAP1	2B2
C76	CAP1	20B2
D1	DIODE	20C5
D2	DIODE	20B5
DS1	LED	14C2
DS2	LED	15A1
DS3	LED	14A3
DS4	LED	14B2
DS5	LED	14B2
DS6	LED	8A1
DS7	LED	18B4
DS8	LED	18B5
DS9	LED	18B4
DS10	LED	18B5
DS11	LED	5C7
DS12	LED	5B7
DS13	LED	5B7
DS14	LED	5B7
DS15	LED	5C7
DS16	LED	5A7
DS17	LED	5A7
DS18	LED	5C5
DS19	LED	5B5
H1	4_40_HDWR_U	20D2
H2	4_40_HDWR_U	20D3
H3	4_40_HDWR_U	20C3
H4	4_40_HDWR_U	20C2
J1	CONN_BANANA_2P	20B8
J2	CONN_DB9P	13B6
J3	CONN_50P2	18D7
J4	CONN_4_PIN	13C4
J5	CONN_BNC_5P	7B7
J6	CONN_10P	7D6
J7	CONN_10P	5A5
J8	CONN_BNC_5P	3A6
J9	CONN_BNC_5P	3C6
JP1	JMP	20B6
JP2	JMP	20B7
JP3	JMP	20B7
JP4	CON14P	13C3
JP5	JMP	13B4
JP6	JMP3	5A2
JP7	JMP	3A6
JP8	JMP	3C6
L1	COIL_2P	12C5
PWR_CONNBAN1	CONN_BANANA_2P	20D8
PWR_CONNBAN2	CONN_BANANA_2P	20C8
R1	RES1	7D2
R2	RES1	7C2
R3	RES1	4B4
R4	RES1	4A4
R5	RES1	4C3
R6	RES1	6B4
R7	RES1	6B6
R8	RES1	4A7
R9	RES1	3A4
R10	RES1	7A7
R11	RES1	3C4
R12	RES1	7C4
R13	RES1	11C2
R14	RES1	14C6
R15	RES1	11B5
R16	RES1	14C2
R17	RES1	14D6
R18	RES1	16C7
R19	RES1	14C6
R20	RES1	14B7
R21	RES1	14C6
R22	RES1	15A1
R23	RES1	14D6
R24	RES1	14D6
R25	RES1	5D7
R26	RES1	14B6
R27	RES1	14C6
R28	RES1	14C6
R29	RES1	14A5
R30	RES1	14A3
R31	RES1	14D3
R32	RES1	
R33	RES1	
R34	RES1	
R35	RES1	
R36	RES1	
R37	RES1	
R38	RES1	
R39	RES1	
R40	RES1	
R41	RES1	
R42	RES1	
R43	RES1	
R44	RES1	
R45	RES1	
R46	RES1	
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R99	RES1	
R100	RES1	
R101	RES1	
R102	RES1	
R103	RES1	
R104	RES1	
R105	RES1	
R106	RES1	
R107	RES1	
R108	RES1	