



DS26303DK

3.3V, E1/T1/J1, Short-Haul, Octal LIU Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26303DK is a fully integrated design kit for the DS26303 3.3V, 8-port, E1/T1/J1 line interface unit (LIU). This design kit contains all the necessary circuitry to evaluate the DS26303 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

DS26303DK Board
5V AC/DC Adapter
3ft USB Cable

Download:

ChipView Software
DS26303DK.def Definition Files
DS26303DK Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS26303DK	DS26303 Design Kit Board

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Demonstrates Key Functions of the DS26303
- Includes DS26303 x 8-Port LIU, Transformers, 75Ω BNC Connectors, RJ-48 Connectors, and Termination Passives
- Communicates Directly with any PC with a USB or RS-232 Serial Interface
- High-Level Windows®-Based Software Provides Visual Access to All Registers
- Software-Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing
- Precision Test Points for All Clocks and Signals
- On-Board T1 and E1 Crystal Oscillators for Stable Clock Generation
- On-Board BERT for Testing and Pattern Generation

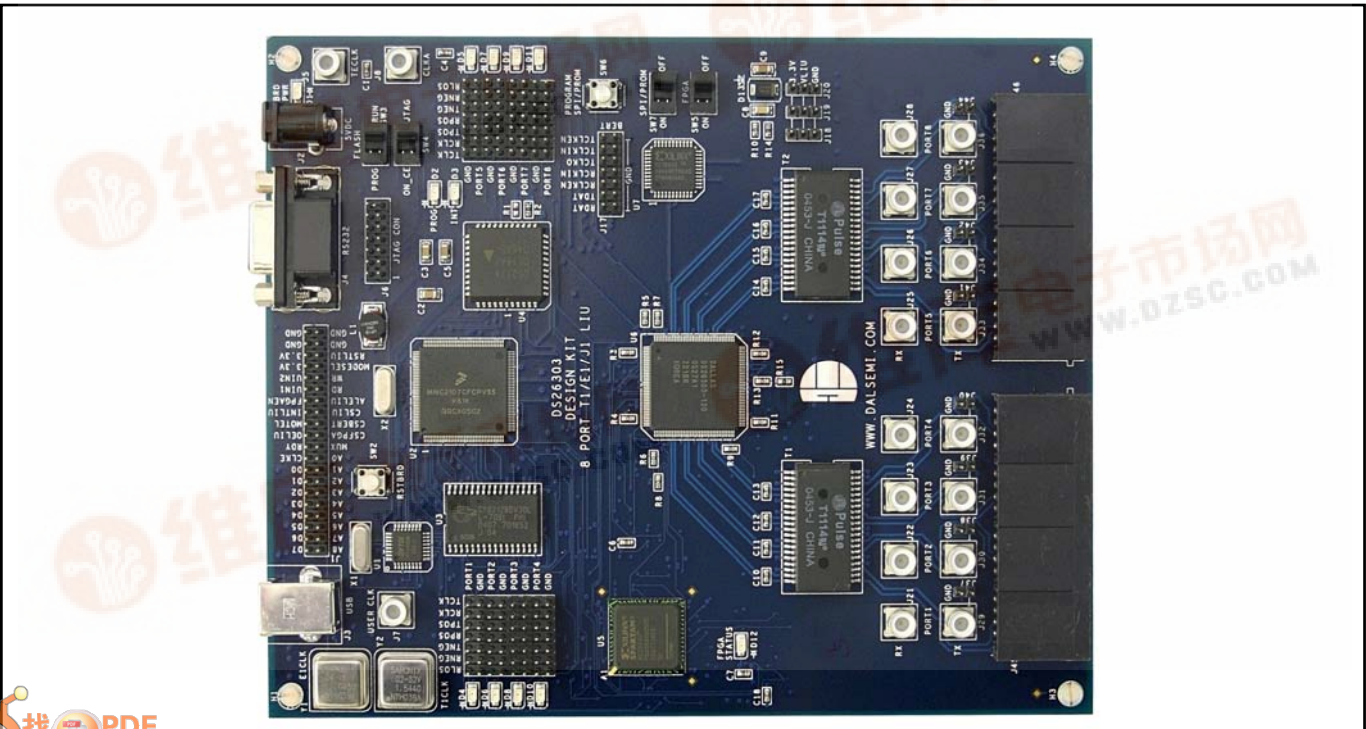


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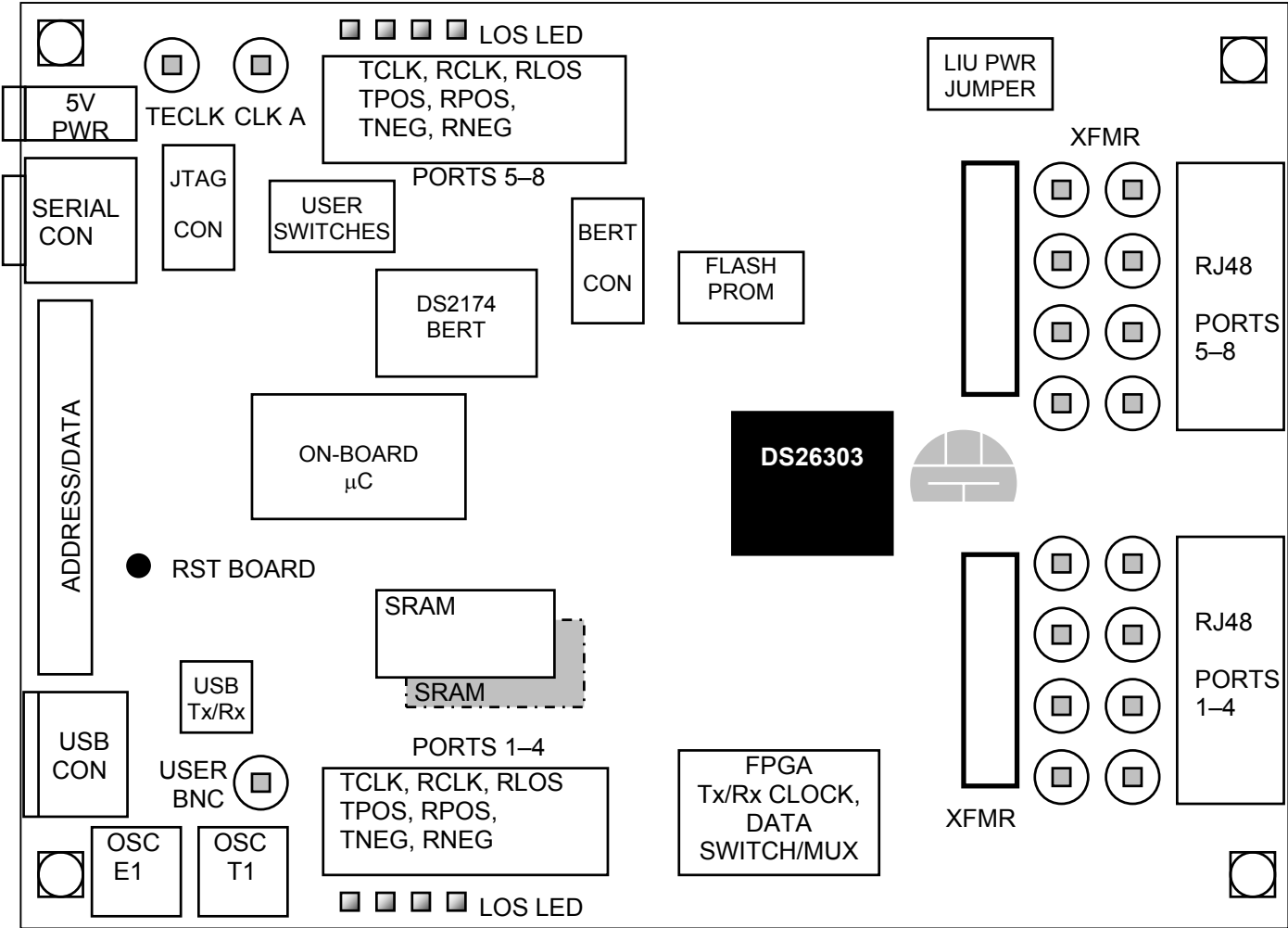
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
C1, C4, C6, C7, C18, C24, C26, C34, C36, C37, C38, C41, C43– C47, C49, C50, C51, C53–C59, C61–C83, C85, C86, C90	53	0.1 μ F \pm 20%, 16V X7R ceramic capacitors (0603)	AVX 0603YC104MAT
C2, C3, C22, C30, C35, C40, C42, C48, C52, C60, C84, C88, C89	13	1 μ F \pm 10%, 16V ceramic capacitors (1206)	Panasonic ECJ-3YB1C105K
C5, C9, C19, C21, C27, C28, C87	7	10 μ F \pm 20%, 10V ceramic capacitors (1206)	Panasonic ECJ-3YB1A106M
C8	1	6.8 μ F \pm 10%, 6.3V X5R ceramic capacitor (1206)	Panasonic ECJ-3YB0J685K
C10–C17	8	470pF \pm 10%, 100V ceramic capacitors (0603)	Panasonic ECJ-1VB2A471K
C20, C23, C25, C91, C92	5	68 μ F \pm 20%, 16V tantalum capacitors (D case)	Panasonic ECS-T1CD686R
C29, C31, C39	3	22pF \pm 5%, 25V ceramic capacitors (0603)	AVX 06033A220JAT
C32, C33	2	10pF \pm 5%, 50V ceramic capacitors (1206) (tall case)	Phycomp 1206CG100J9B200
D1, D12	2	Green LEDs (SMD)	Panasonic LN1351C
D2–D11	10	Red LEDs (SMD)	Panasonic LN1251C
D13, D14, D15	3	1A, 40V Schottky diodes	International Rectifier 10BQ040
H1–H4	4	KIT, 4-40 hardware 0.75 nylon standoff and 0.25 nylon screw	Not applicable 4-40KIT2
J1	1	40-pin terminal strip (dual row, vertical)	Samtec TSW-120-07-T-D
J2	1	2.1mm/5.5mm connector Power jack, right-angle PC board mount; closed frame, high current, 24V DC at 5A	CUI, Inc. PJ-002AH
J3	1	Black, single right angle (Type B)	Molex Not applicable
J4	1	DB9 right-angle connector (short case)	AMP 788750-2
J5, J7, J8, J21–J36	19	5-pin SMB connectors 50 Ω , vertical, gold	AMP 413990-1
J6, J9–J17	10	14-pin headers (dual row, vertical)	Samtec TSW-107-14-T-D
J18, J19, J20	3	100-mil 3-position jumpers	Samtec Not applicable
J37–J44	8	2-pin headers, 0.100in centers (vertical)	Samtec TSW-102-07-T-S
J45, J46	2	8-pin 4-port RJ45 jacks (right angle)	Molex 43223-8140
L1	1	1.0 μ H \pm 20%, 2-pin SMT inductor	Coiltronics UP1B-1R0

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
R1, R58, R87	3	Resistors (0603) DO NOT POPULATE	—
R2, R14–R26, R28, R32–R43, R46– R50, R52, R54– R57, R63–R66, R68, R69, R71, R72, R73, R76, R77, R82, R85, R86, R88, R91, R93, R96, R97, R130	57	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
R3–R9, R11, R12, R13, R29, R31, R44, R45, R60, R61, R62, R78, R79, R94, R95, R98–R102, R104, R117, R120, R121, R124–R129	36	33 Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ330V
R10	1	22k Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ223V
R27, R67, R70, R74, R75, R80, R81, R83, R84, R89, R90, R123	12	330 Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ331V
R30, R59	2	15k Ω \pm 5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ153V
R51	1	Resistor (1206) DO NOT POPULATE	—
R53	1	470 Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ471V
R92	1	51 Ω \pm 5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ510V
R103, R105–R116, R118, R119, R122	16	60.4 Ω \pm 1%, 1/16W resistors (0603)	Panasonic ERJ-3EKF60R4V
SW2, SW6	2	4-pin single-pole switch	Panasonic EVQPAE04M
SW3, SW4, SW5, SW7	4	6-pin slide switches (DPDT, through hole)	Tyco Electronics SSA22
T1, T2	2	Transformers (1:2 count transmitter/1:1 count receiver) (40-pin wide SO, -40°C to +85°C)	Pulse Engineering T1114
U1	1	8-bit FIFO USB UART (32-pin LQFP)	FTDI FT245BM
U2	1	MCORE Microcontroller (144-pin LQFP)	Motorola MMC2107PV
U3, U11	2	128k x 8 SRAM (32-pin SO)	Cypress CY62128VL-70SC
U4	1	DS2174 EBERT (44-pin PLCC, 0°C to +70°C)	Dallas Semiconductor DS2174Q
U5	1	Spartan-II 2.5V FPGA, 200k gate (256-pin BGA)	Xilinx XC2S200-5FG256C
U6	1	3.3V, E1/T1/J1 long-haul octal LIU (144-pin eLQFP, 0°C to +70°C)	Dallas Semiconductor DS26303L

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
U7	1	PROM for FPGA (44-pin TQFP)	Xilinx XC18V02VQ44C
U8	1	Dual RS-232 transmitter/receiver (150-mil, 16-pin SO)	Dallas Semiconductor DS232AR
U9, U12	2	High-speed buffers	Fairchild Semiconductor NC7SZ86
U10, U18	2	1.5W, 3.3V or adj, 1A linear regulators (16-pin TSSOP-EP)	Maxim MAX1793EUE-33
U13, U15	2	Hex inverters (14-pin SO)	Toshiba TC74HC04AFN
U14	1	Quad 2-input NAND gate (14-pin SO)	Toshiba TC74HC00AFN
U16	1	Switch debouncer (4-pin SOT143)	Maxim MAX6816EUS-T
U17	1	2.5V or adj linear regulator (8-pin μ MAX/SO)	Maxim MAX1792EUA25
U19	1	Platform flash in-system programmable configuration PROM (2Mb, 20-pin TSSOP)	Xilinx XCF02SVO20C
X1	1	6.00MHz low-profile crystal	Pletronics LP49-26-6.00M
X2	1	8.000MHz low-profile crystal	Ecliptek Corp. EC1-8.000M
Y1	1	Oscillator, crystal clock 5V, 2.048MHz	SaRonix NTH039A-2.0480
Y2	1	Oscillator, crystal clock 5V, 1.544MHz	SaRonix NTH039A-1.5440

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26303DK.

The support files are used with an evaluation program called ChipView, which is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings—Single Power Supply)

- For single power-supply operation, short jumpers J18, J19, and J20 between the 3.3V pin and the VLIU pin. This connects VDD of the DS26303 to the 3.3V supply on the design kit.
- Ensure that the FLASH switch (SW3) is in the *RUN* position.
- Ensure that the FPGA switch (SW5) is in the *ON* position.
- Ensure that the SPI/PROM switch (SW7) is in the *OFF* position.
- If using the serial port, connect a RS-232 serial cable from DS26303DK (J4) to the PC.
- If using the USB port, connect a USB cable from DS26303DK (J3) to the PC.
- Connect AC/DC adapter with an AC power source and the DS26303DK (J2). PWR LED should be on.

JTAG Configuration

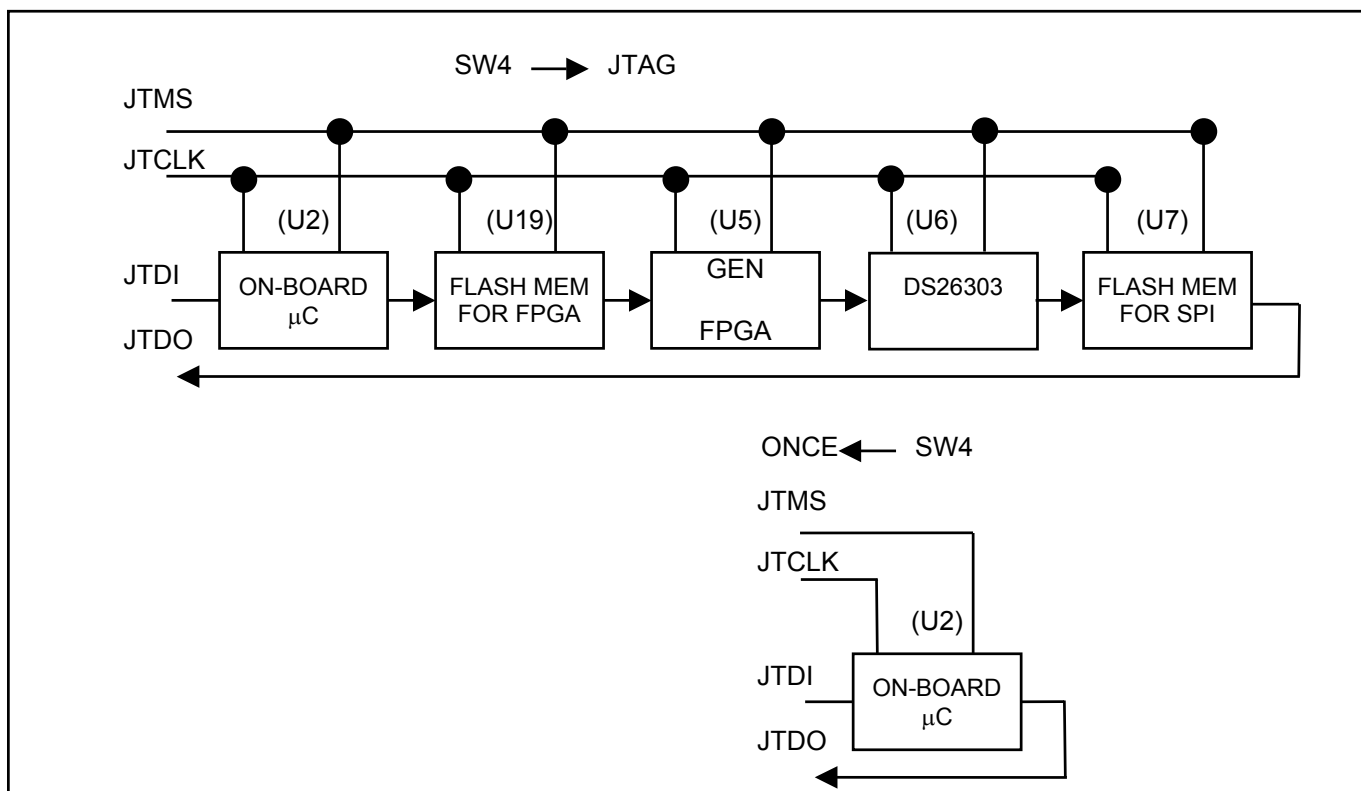
The JTAG chain is controlled by the connector JTAG CON (J6) and two on-board switches: FLASH (SW3) and ONCE/JTAG (SW4). Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the JTAG CON connector can be used and the switches can be configured to accomplish the desired task. For information on programming the internal flash of the on-board microcontroller, refer to the MMC2107 microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. [Figure 1](#) shows the complete chain as well as what order the devices appear during boundary scan. [Table 1](#) shows the pinout of the JTAG connector. Connect any JTAG cable to the connector to perform all operations. Note the JTAG chain changes depending on the switch SW4. The ONCE location of SW4 is used for programming the on-board microcontroller only.

Table 1. JTAG Connector (J6) Pinout

PIN	NAME
1	JTDI
2, 4, 6, 7	GND
3	JTDO
5	JTCLK
8	ALIGN KEY
9	BRD RST
10	JTMS
11	BRD V3.3
12	JDE
13	N.C.
14	JTRST

Figure 1. DS26303DK JTAG Chain



Address/Data Bus Connector

The DS26303DK has a connector (J1) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If the FPGA switch (SW5) is in the “OFF” position, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS26303 into another system without making any modifications to the hardware. See [Table 2](#) for specific pin information for connector J1.

Table 2. Address/Data Connector Pinout

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	A8	Local Address Bit 8	2	D0	Local Data Bit 0
3	A7	Local Address Bit 7	4	D1	Local Data Bit 1
5	A6	Local Address Bit 6	6	D2	Local Data Bit 2
7	A5	Local Address Bit 5	8	D3	Local Data Bit 3
9	A4	Local Address Bit 4	10	D4	Local Data Bit 4
11	A3	Local Address Bit 3	12	D5	Local Data Bit 5
13	A2	Local Address Bit 2	14	D6	Local Data Bit 6
15	A1	Local Address Bit 1	16	D7	Local Data Bit 7
17	A0	Local Address Bit 0	18	CLKE	SPI Clock Edge Select
19	MUX	Mux	20	RDY	Ready Handshake from LIU
21	CSFPGA	Chip Select FPGA	22	OE	Output Enable LIU
23	CSBERT	Chip Select DS2174	24	MOTEL	Motorola/Intel Select
25	CSLIU	Chip Select DS26303	26	INT	Interrupt for DS26303
27	ALELIU	Address Latch Enable	28	FPGAEN	FPGA Enable Pin
29	RD	Read Signal	30	UIN1	User Input 1
31	WR	Write Signal	32	UIN2	User Input 2
33	MODESEL	Mode Select	34, 36	3.3V	Board 3.3V
35	—	Not Used	37–40	GND	Ground

Telecom Clock and Data Test Points

The DS26303DK has high-impedance test points for all the telecom signals that are related to the LIU. These signals are split up by port number and marked with easy to read silkscreen labels. [Table 3](#) shows the telecom connector for port 1. The pinout for this connector is repeated for all 8 ports.

Table 3. Telecom Connector Pinout

PIN	NAME	FUNCTION
1	TCLK	Transmit Clock Input
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	RCLK	Receive Clock Output
5	TPOS	Transmit Positive Data Input
7	RPOS	Receive Positive Data Output
9	TNEG	Transmit Negative Data Input
11	RNEG	Receive Positive Data Output
13	RLOS	Receive Loss-of-Signal Output

Note that the input signals in the telecom connector go from the connector to the on-board FPGA, then to the DS26303. The FPGA was designed to perform specific signal routing functions such as looping back RPOS to TPOS on a particular port or transferring data from the on-board BERT. If you are using user-defined data and drive the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA!**

On-Board Bit Error-Rate Tester (BERT)

The DS26303DK has an on-board bit error-rate tester (BERT) to generate and detect errors in either pseudorandom or user-defined patterns. The BERT on the DS26303DK is the DS2174. A header for the relevant signals related to the BERT is located on the board (J17). See [Table 4](#) for the pinout of the BERT connector. The BERT signals are routed into the FPGA and can be muxed into any of the 8 DS26303 LIU ports under software control. For all questions concerning the operation of the on-board BERT, refer to the device data sheet available online at www.maxim-ic.com/telecom. If you are using user-defined data and driver the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA!**

Table 4. BERT Connector Pinout

PIN	NAME	FUNCTION
1	TCLK_EN	BERT TCLK Enable
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	TCLKIN	BERT TCLK Input
5	TCLKO	BERT TCLK Output
7	RCLKIN	BERT RCLK Input
9	RCLKEN	BERT RCLK Enable
11	TDAT	BERT TDAT Output
13	RDAT	BERT RDAT Input

PROM SPI Configuration

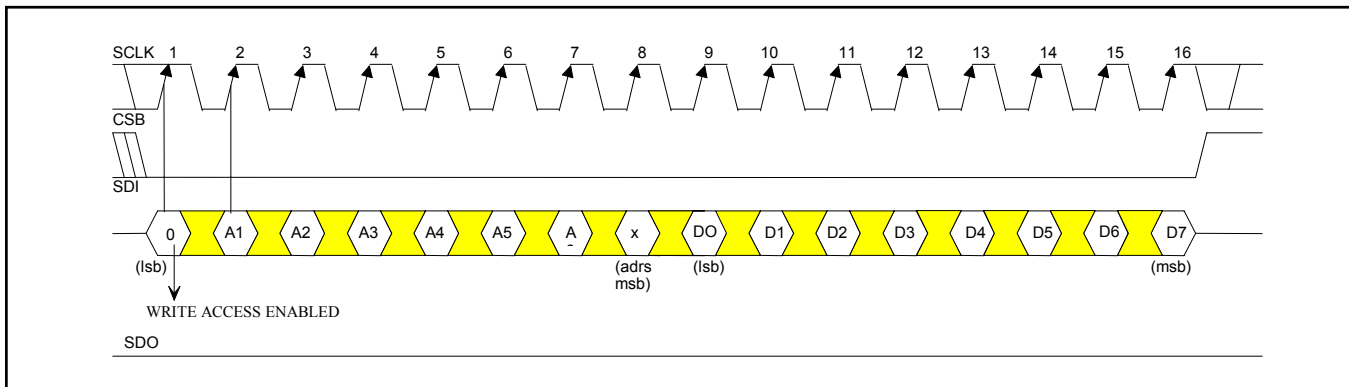
In software mode, it is possible to configure the DS26303 using a parallel interface or a serial peripheral interface (SPI). Most advanced microcontrollers have both a parallel interface and SPI interface such as the microcontroller on the DS26303DK. The command you send to the microcontroller through either the USB or serial port determines if that data is placed on the parallel or SPI bus. Refer to the data sheet for [Chipview](#) on the particular commands required to switch data ports.

A unique feature with the SPI port is that a PROM can be used to provide the LIU with the specific data needed for configuration. If the data in the PROM is formatted a certain way, it can seem as the PROM is acting like a controller with a SPI interface in master mode.

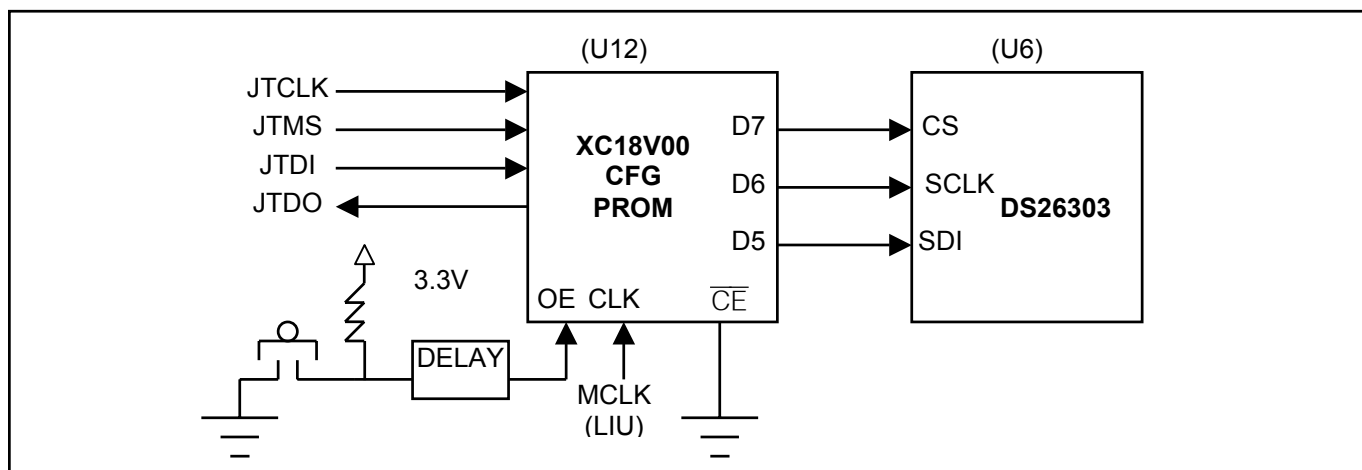
The most common PROMs to use for this type of application are those with an internal address accumulator. This feature for the PROM is important because the device must automatically jump to the next available address in the configuration memory. The Xilinx XC18V00 device family is a byte-wide nonvolatile memory with an autoincrement address function. The family of devices is available in 1Mb, 2Mb, and 4Mb densities. The PROM is also useful because the device can perform in-circuit programming with the JTAG port. Refer the data sheet for the XC18V00 for the JTAG codes for programming the configuration memory.

[Figure 2](#) shows a general relationship of the timing for a SPI bus. For this case, all data is clocked into the slave device on the rising edge of SCLK. This feature can be configurable on the DS26303.

Figure 2. SPI Timing Diagram



[Figure 3](#) shows a simplified diagram of the XC18V00 device and the DS26303 in SPI (serial) mode. Notice a few key points about this diagram. First, the CLK for the XC18V00 is the MCLK for the LIU, but this is not the SCLK for the SPI interface. The SCLK can be programmed as needed. See [Table 5](#) for an example of the memory map. Second, the programming for this device begins when OE on the XC18V00 goes high. Therefore, consideration must be taken if some delay is necessary. Generally, it is sufficient for the OE pin to be connected to some power-up delay device. The OE delay is not necessary on this DK.

Figure 3. SPI Configuration with PROM**Table 5. Configuration Memory**

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
	CSB	SCLK	SDI	X	X	X	X	X
0x00	1	0	0	Start of Write Cycle				
0x01	0	0	0	Bit A0				
0x02	0	1	0	(Always a "0" for a write)				
0x03	0	0	1	Bit A1				
0x04	0	1	1	Bit A2				
0x05	0	0	0	Bit A3				
0x06	0	1	0	Bit A4				
0x07	0	0	0	Bit A5				
0x08	0	1	0	Bit A6				
0x09	0	0	0	Bit A7				
0x0A	0	1	0	Bit D0 (LSB)				
0x0B	0	0	0	Bit D1				
0x0C	0	1	0	Bit D2				
0x0D	0	0	0	Bit D3				
0x0E	0	1	0	Bit D4				
0x0F	0	0	0	Bit D5				
0x10	0	1	0	Bit D6				
0x11	0	0	0	Bit D7				
0x12	0	1	0	End of Write Cycle				
0x13	0	0	1					
0x14	0	1	1					
0x15	0	0	1					
0x16	0	1	1					
0x17	0	0	0					
0x18	0	1	0					
0x19	0	0	0					
0x1A	0	1	0					
0x1B	0	0	1					
0x1C	0	1	1					
0x1D	0	0	1					
0x1E	0	1	1					
0x1F	0	0	0					
0x20	0	1	0					
0x21	1	0	X					
0x22	1	X	X					

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Configuration).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.exe. If the default installation options were used, click the Start button on the Windows toolbar and select Programs -> ChipView -> ChipView.
- Load the DS26303DK.def file.
- Make sure that all the register settings are correct for the proper function desired for the DS26303DK.
- Refer to the DS26303 data sheet for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given below are relative to the beginning of the user address space.

Table 6. DS26303DK Relative Address Map

REF DES	DEVICE	OFFSET
U5	General-Purpose FPGA Tx/Rx Clock, Data Switch/Mux	0x0000
U4	DS2174 BERT	0x1000
U6	DS26303 8-Port T1/E1/J1 LIU	0x2000

All device registers can be easily modified using the ChipView.exe host-based user-interface software.

Table 7. General-Purpose FPGA Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read-Only	Board ID
0x02	DSIDH	Read-Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read-Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read-Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read-Only	Board Rev
0x06	ASMREV	Read-Only	Assembly Rev
0x07	FPGAREV	Read-Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Register 1
0x0A	ABSP	Control	Address Bank Select Pointer
0x0B	BTCLK	Control	BERT TCLK Input
0x0C	BRCLK	Control	BERT RCLK Input
0x0D	BRDAT	Control	BERT RDAT Input
0x10	TCLK	Control	Indirect Register for TCLK Source Control
0x11	TPOS	Control	Indirect Register for TPOS Source Control
0x12	TNEG	Control	Indirect Register for TPOS Source Control

ID REGISTERS

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: FPGA REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: **CTRL_1**

Register Description: **DS26303DK FPGA CONTROL REGISTER 1**

Register Offset: **0x08**

Bit #	7	6	5	4	3	2	1	0
Name	INT303	ENRLOS1	CLKE	SPI_SWAP	SPI	OE	MCLK1	MCLK0

Bit 7: INT303. This bit indicates the status of the INT303 line.

If INT303 = LOW, there is no hardware interrupt on the DS26303.

If INT303 = HIGH, there is a hardware interrupt on the DS26303.

Bit 6: ENRLOS1. This bit enables the RLOS1 LED. This should not be enabled when driving TECLK from the DS26303.

If ENRLOS1 = LOW, the RLOS1 LED is not enabled.

If ENRLOS1 = HIGH, the RLOS1 LED is enabled and lights when RLOS1 is high.

Bit 5: CLKE. This bit sets the CLKE pin on the DS26303. This is only active when SPI (Bit 0) is HIGH. If SPI (Bit 0) is low, CLKE is always low.

If CLKE = LOW, SDO is clocked out on the rising edge of SCLK.

If CLKE = HIGH, SDO is clocked out on the falling edge of SCLK.

Bit 4: SPI_SWAP. This bit sets the BSWP/A5 pin on the DS26303. This is only active when SPI (Bit 0) is HIGH.

If SPI_SWAP = LOW, the SPI bus is LSB first.

If SPI_SWAP = HIGH, the SPI bus is MSB first.

Bit 3: SPI. This bit sets up the FPGA to use serial mode. This bit also changes the mode pin on the DS26303.

If SPI = LOW, the parallel bus is used for all read/write access. This also sets the MODE pin on the DS26303 to logic 1.

If SPI = HIGH, the SPI bus is used for all read/write access. This also sets the MODE pin on the DS26303 to logic 0.

Bit 2: OE. This bit controls the OE pin to the DS26303.

Bits 1 and 0: MCLK1 and MCLK0. These bits control the MCLK pin to the DS26303.

MCLK1	MCLK0	DESCRIPTION OF MCLK
0	0	MCLK = high-impedance mode
0	1	MCLK = on-board T1 oscillator
1	0	MCLK = on-board E1 oscillator
1	1	MCLK = user clock input

Register Name: **ABSP**

Register Description: **ADDRESS BANK SWAP POINTER**

Register Offset: **0x0A**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the address bank for address 0x10 (TCLK N), 0x11 (TPOS), and 0x12 (TNEG).

ABSP	DESCRIPTION
0x00	Bank Address Value for Port 1
0x01	Bank Address Value for Port 2
0x02	Bank Address Value for Port 3
0x03	Bank Address Value for Port 4
0x04	Bank Address Value for Port 5
0x05	Bank Address Value for Port 6
0x06	Bank Address Value for Port 7
0x07	Bank Address Value for Port 8

Register Name: **BTCLK**Register Description: **BERT TCLK SOURCE**Register Offset: **0x0B**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the TCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRCLK**Register Description: **BERT RCLK SOURCE**Register Offset: **0x0C**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRDAT**Register Description: **BERT RDAT SOURCE**Register Offset: **0x0D**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RDAT for the BERT. Note that the DS26303 must be in single-rail mode for BERT to function properly.

BRDAT	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TCLK**
 Register Description: **PORT TCLK SOURCE**
 Register Offset: **0x10**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: This is an indirect register that is related to ABSP (0x0A). See register description.

Bits 7 to 0: D7 to D0. These bits control the source of the port TCLK for the DS26303.

TCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TPOS**

Register Description: **PORT TPOS SOURCE**

Register Offset: **0x11**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: This is an indirect register that is related to ABSP (0x0A). See register description.

Bits 7 to 0: D7 to D0. These bits control the source of the port TPOS for the DS26303.

TPOS	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	TDATBERT OUT
0x16–0xFF	HI-Z

Register Name: **TNEG**Register Description: **PORT TNEG SOURCE**Register Offset: **0x12**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: This is an indirect register that is related to ABSP (0x0A). See register description.

Bits 7 to 0: D7 to D0. These bits control the source of the port TNEG for the DS26303.

TNEG	DESCRIPTION
0x00	RNEG Port 1
0x01	RNEG Port 2
0x02	RNEG Port 3
0x03	RNEG Port 4
0x04	RNEG Port 5
0x05	RNEG Port 6
0x06	RNEG Port 7
0x07	RNEG Port 8
0x08	HI-Z
0x09	HI-Z
0x0A	HI-Z
0x0B	HI-Z
0x0C	HI-Z
0x0D	HI-Z
0x0E	HI-Z
0x0F	HI-Z
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26303
0x14	TECLK DS26303
0x15	Drive Logic "0"
0x16–0xFF	HI-Z

DS26303 INFORMATION

For more information about the DS26303, refer to the DS26303 data sheet available on our website at www.maxim-ic.com/DS26303.

DS26303DK INFORMATION

For more information about the DS26303DK including software downloads, go to www.maxim-ic.com/DS26303DK.

TECHNICAL SUPPORT

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

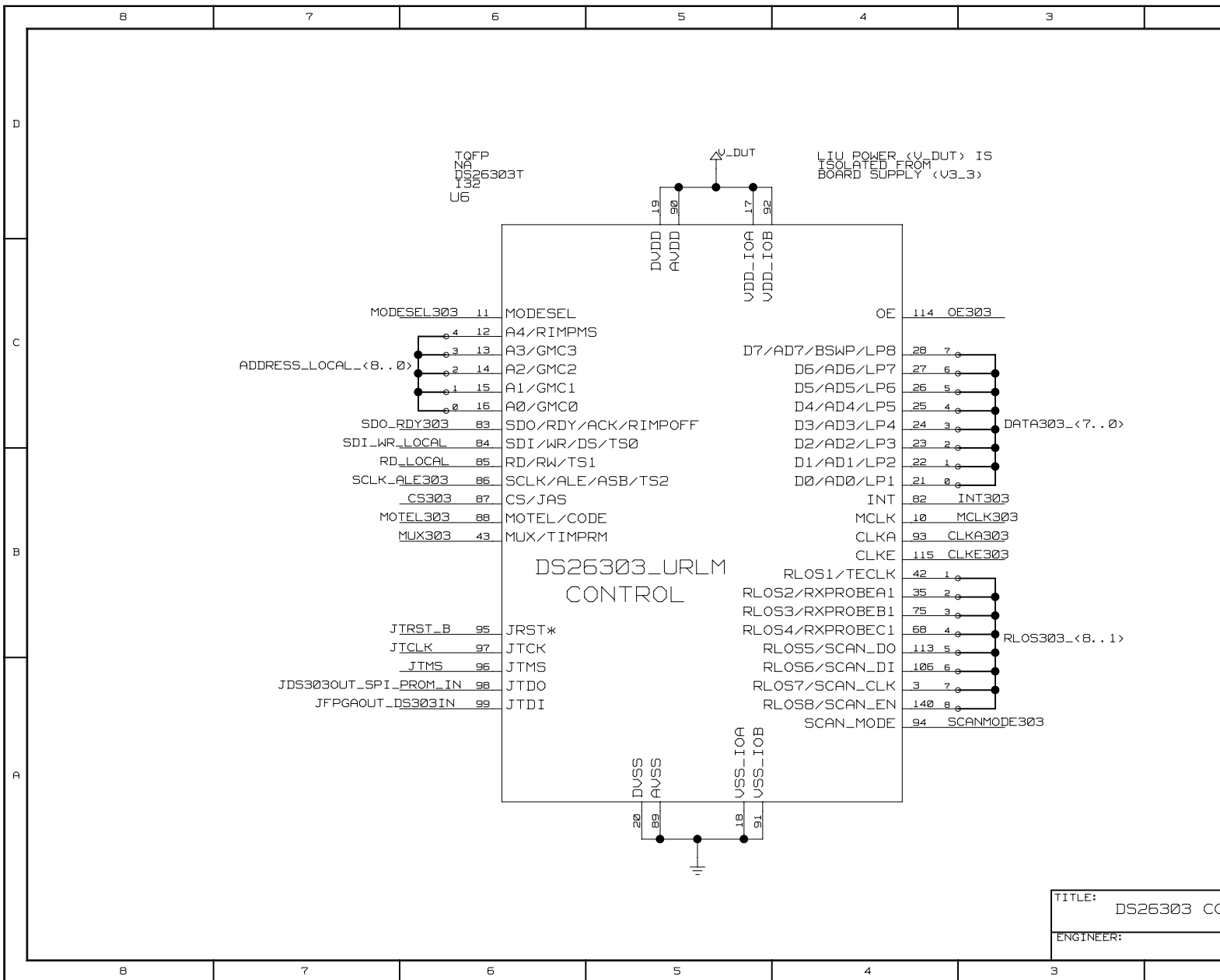
The DS26303DK schematics are featured in the following 22 pages.

DS26303 DESIGN KIT
SCHEMATIC
DALLAS SEMICONDUCTOR / MAXIM
AUGUST 2005

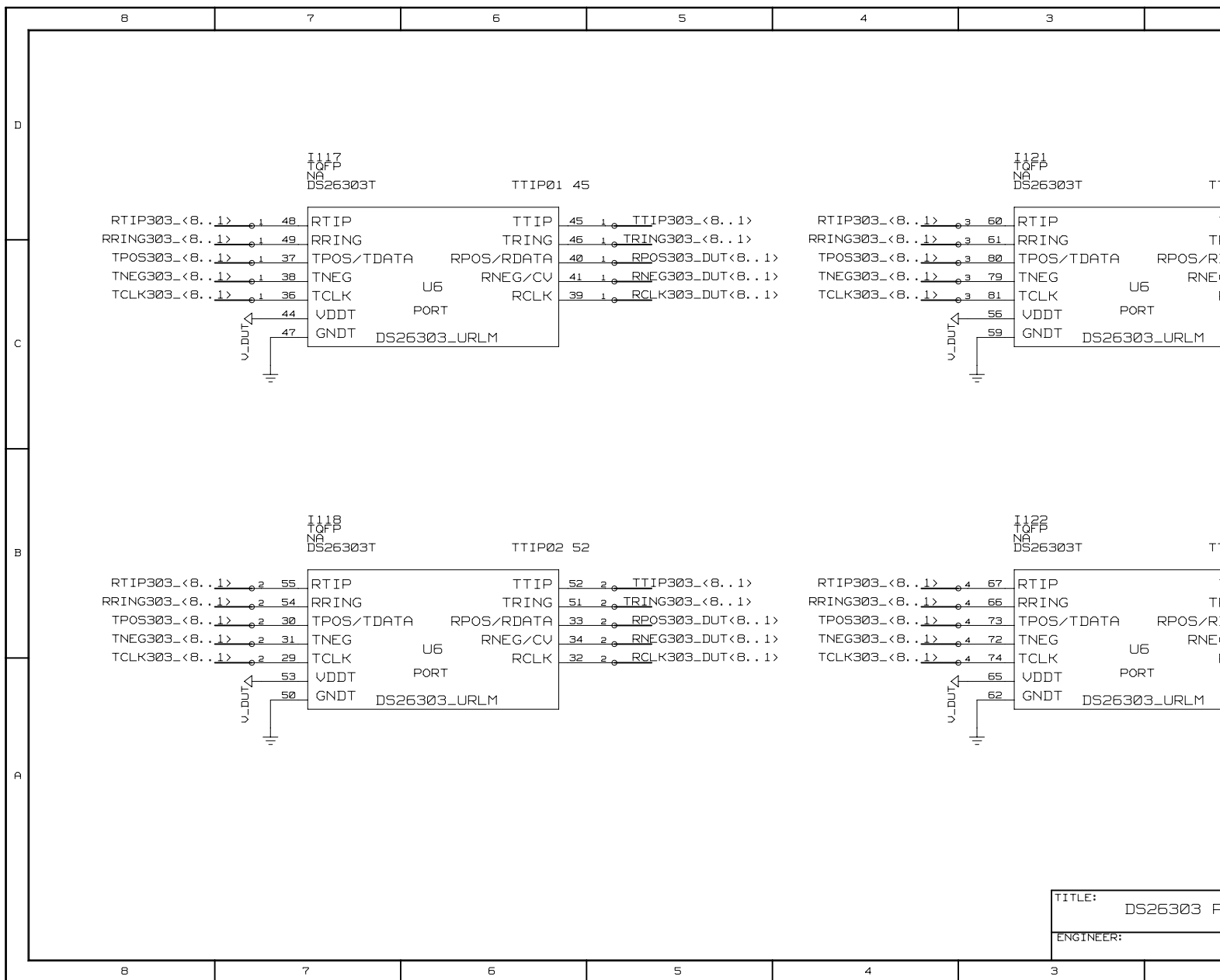
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3. DS26303 PORT 1-4	11. FPGA PORT B	19. NOTES
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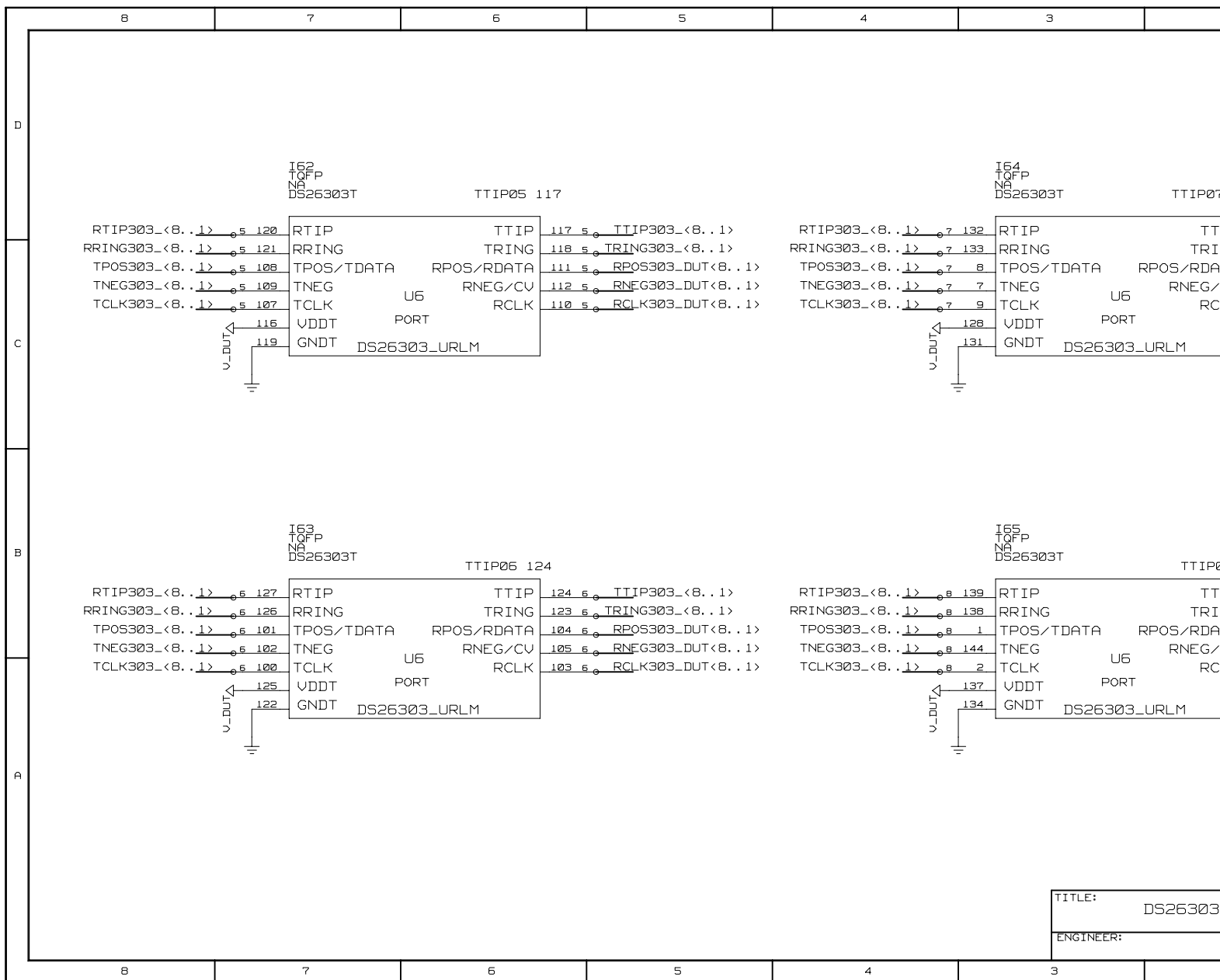
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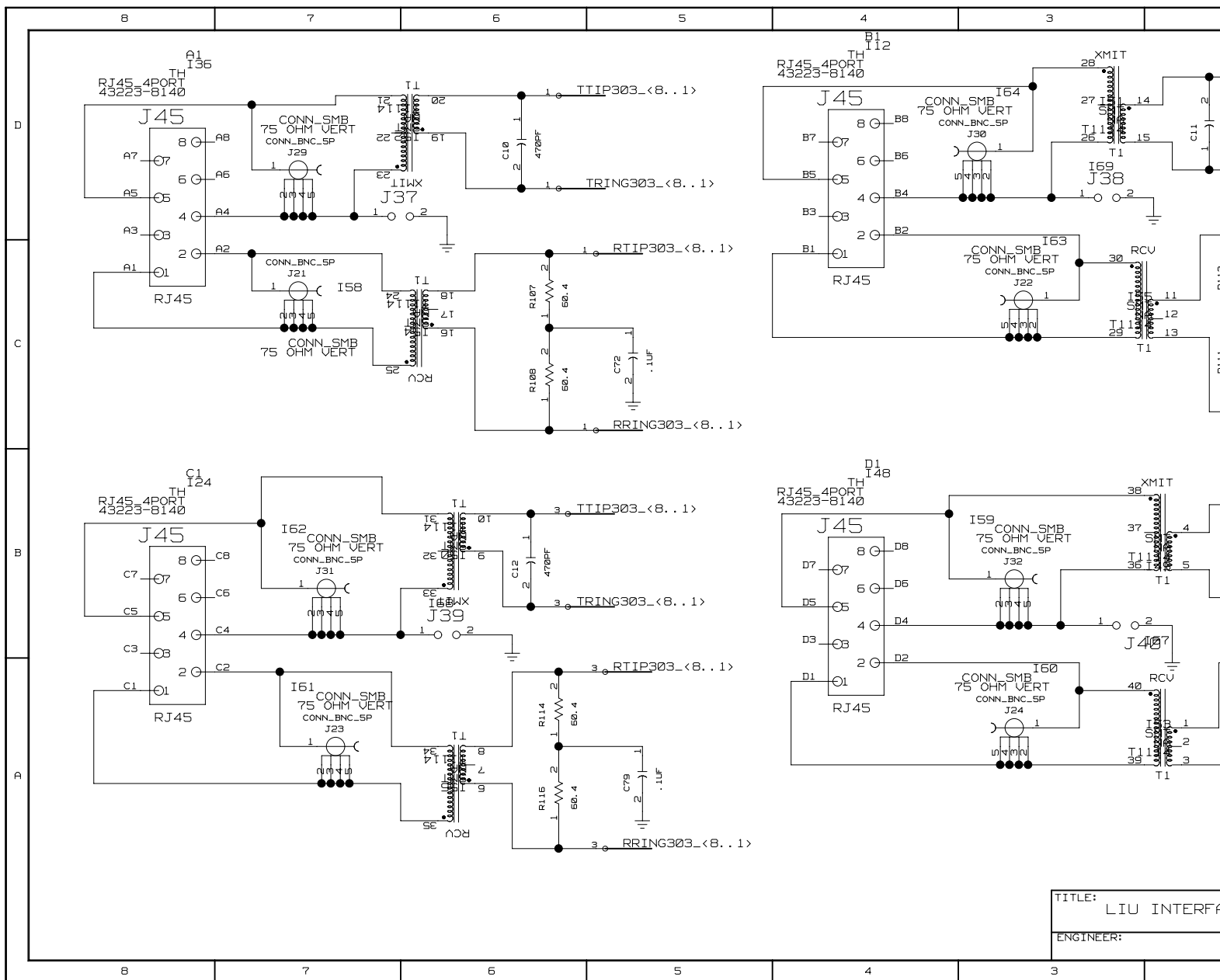
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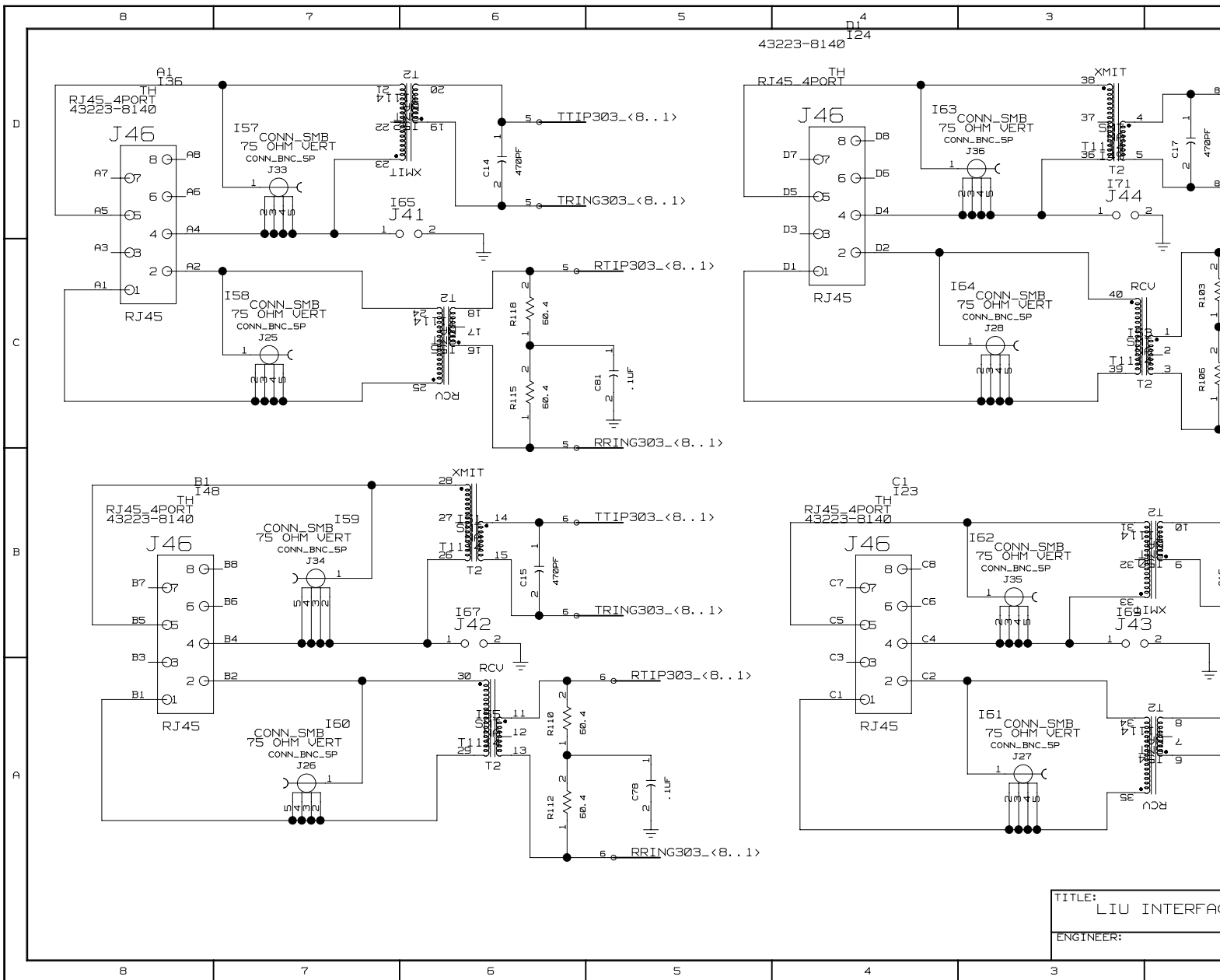
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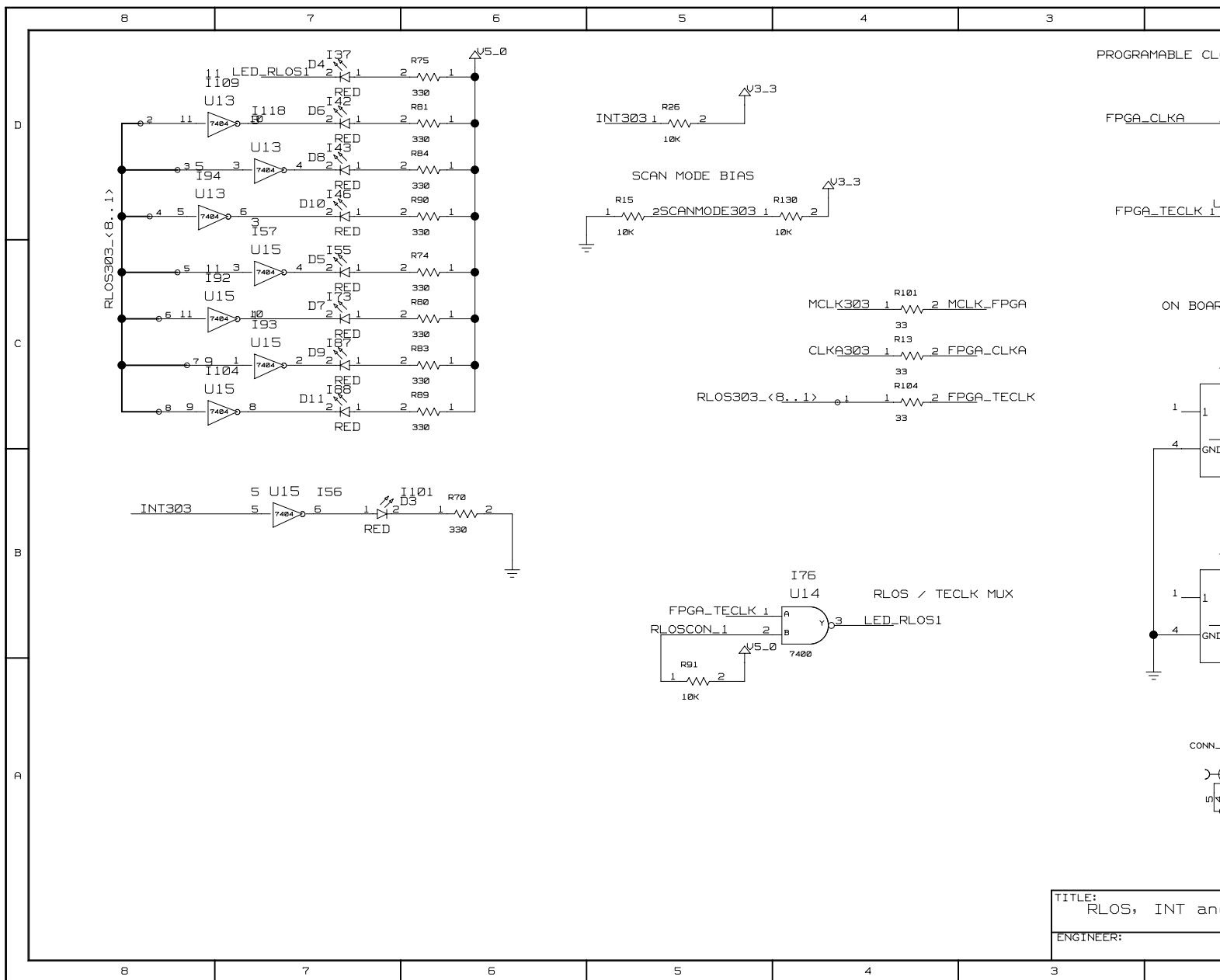
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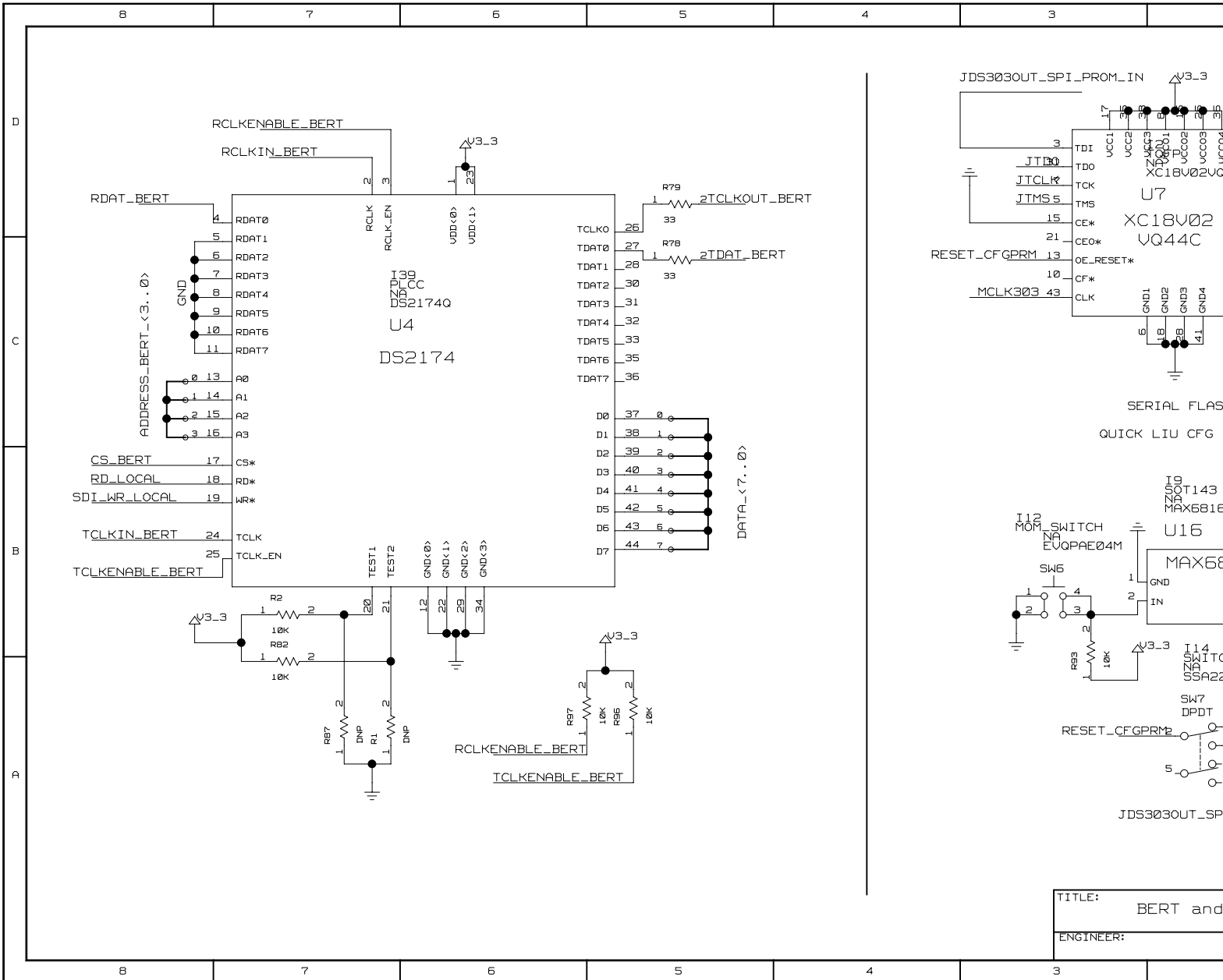
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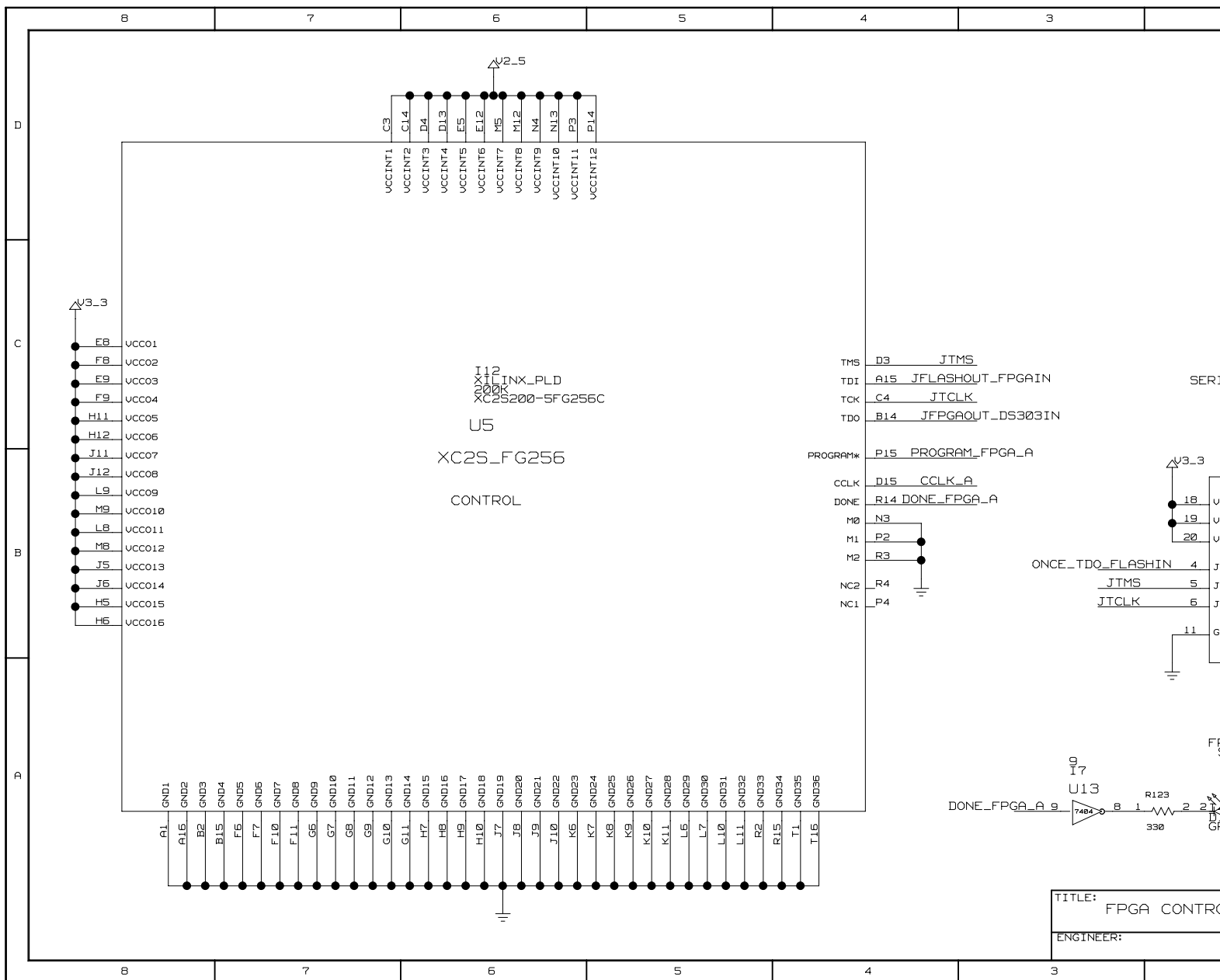
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 ENGINEER:



TITLE:
 RLOS, INT and
 ENGINEER:



TITLE: BERT and
ENGINEER:



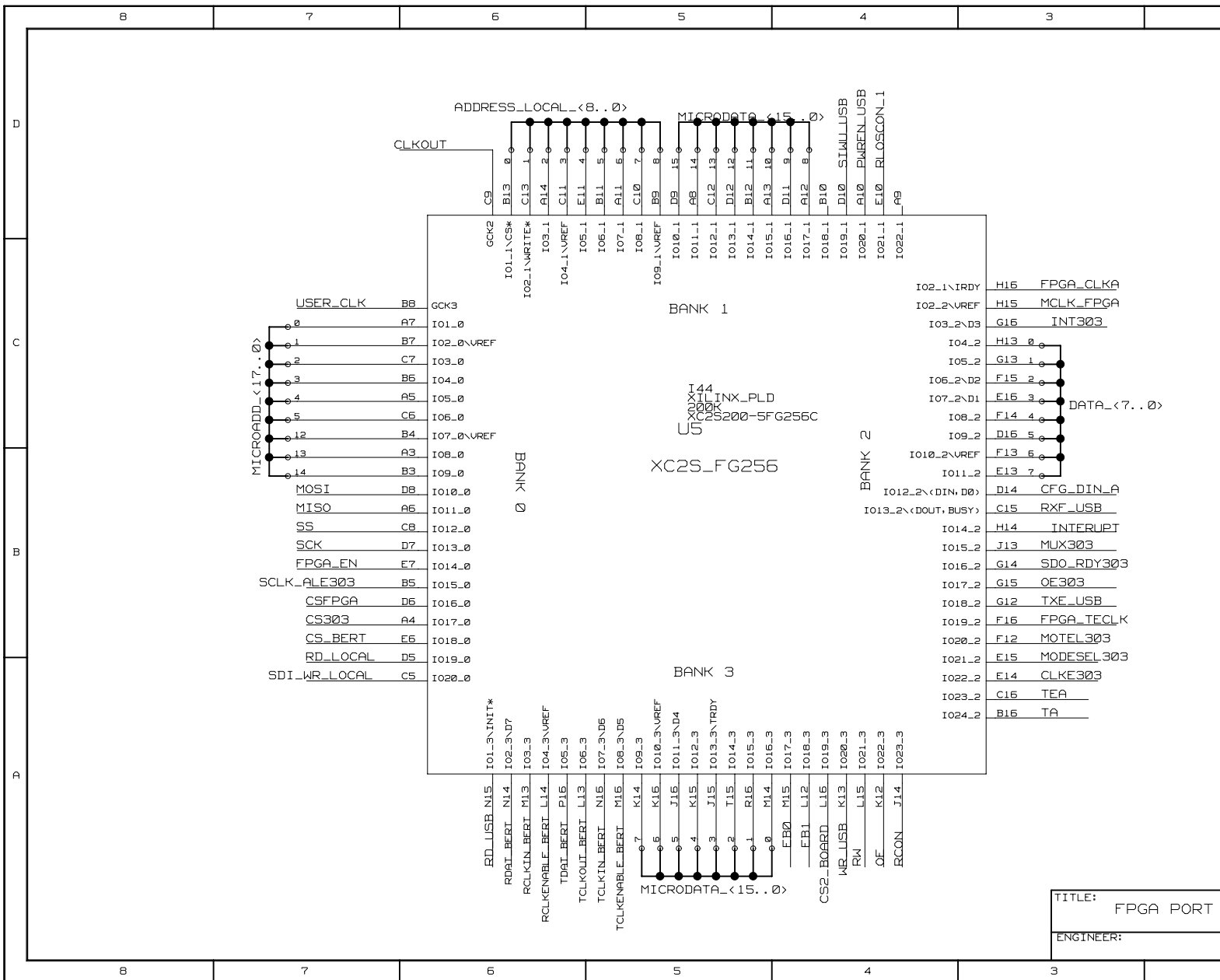
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 200k
 J11 INX_PLD
 J12
 XC2S200-5FG256C
 U5
 XC2S_FG256

CONTROL

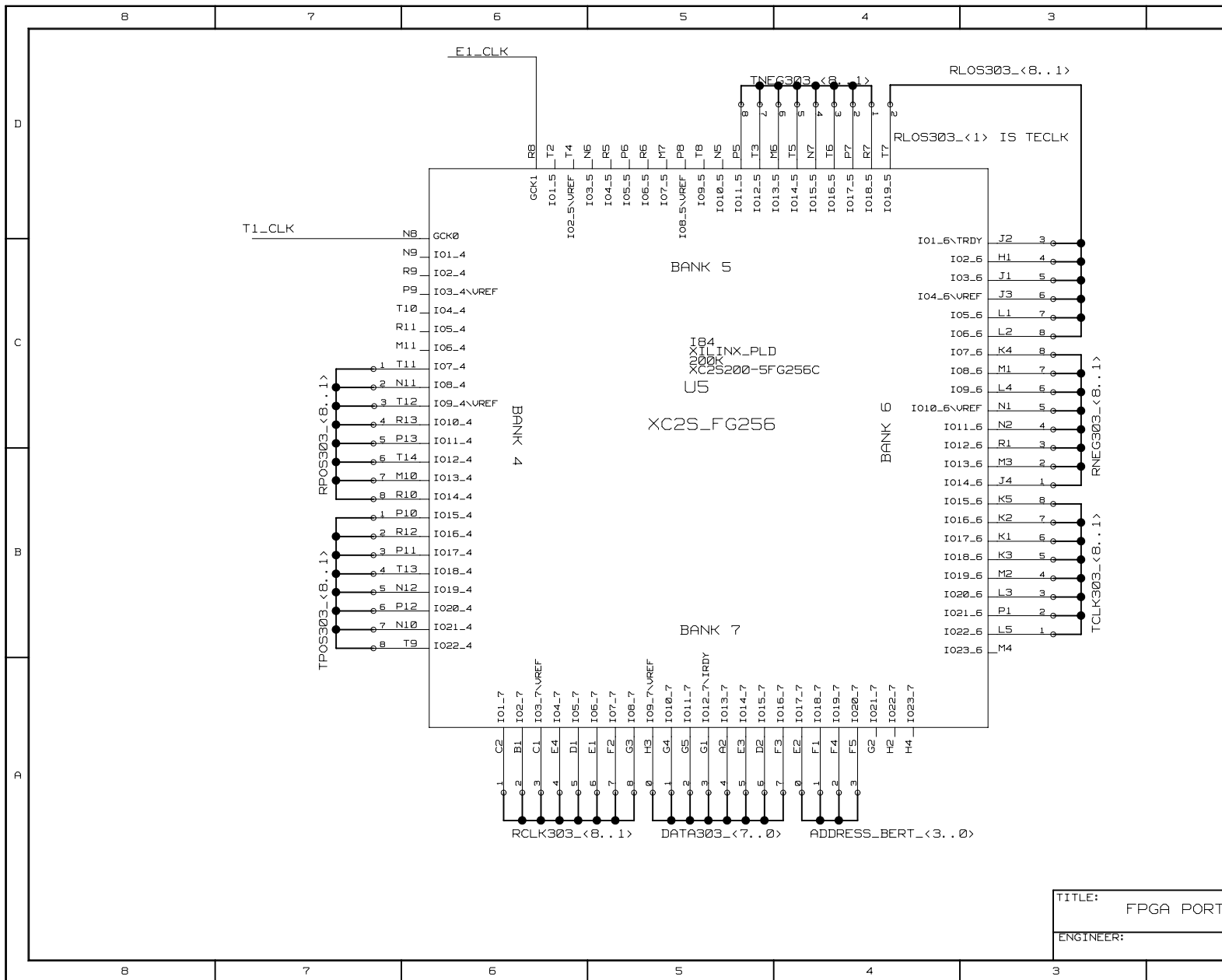
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 TDI A15 JFLASHOUT_FPGA_A
 TCK C4 JTCLK
 TDO B14 JFPGAOUT_DS3031N
 PROGRAM* P15 PROGRAM_FPGA_A
 CCLK D15 CCLK_A
 DONE R14 DONE_FPGA_A
 M0 N3
 M1 P2
 M2 R3
 NC2 R4
 NC1 P4

U13
 7404
 330
 R123
 11
 GND
 V3_3
 18
 19
 20
 V3_3
 ONCE_TDO_FLASHIN 4 J
 JTMS 5 J
 JTCLK 6 J

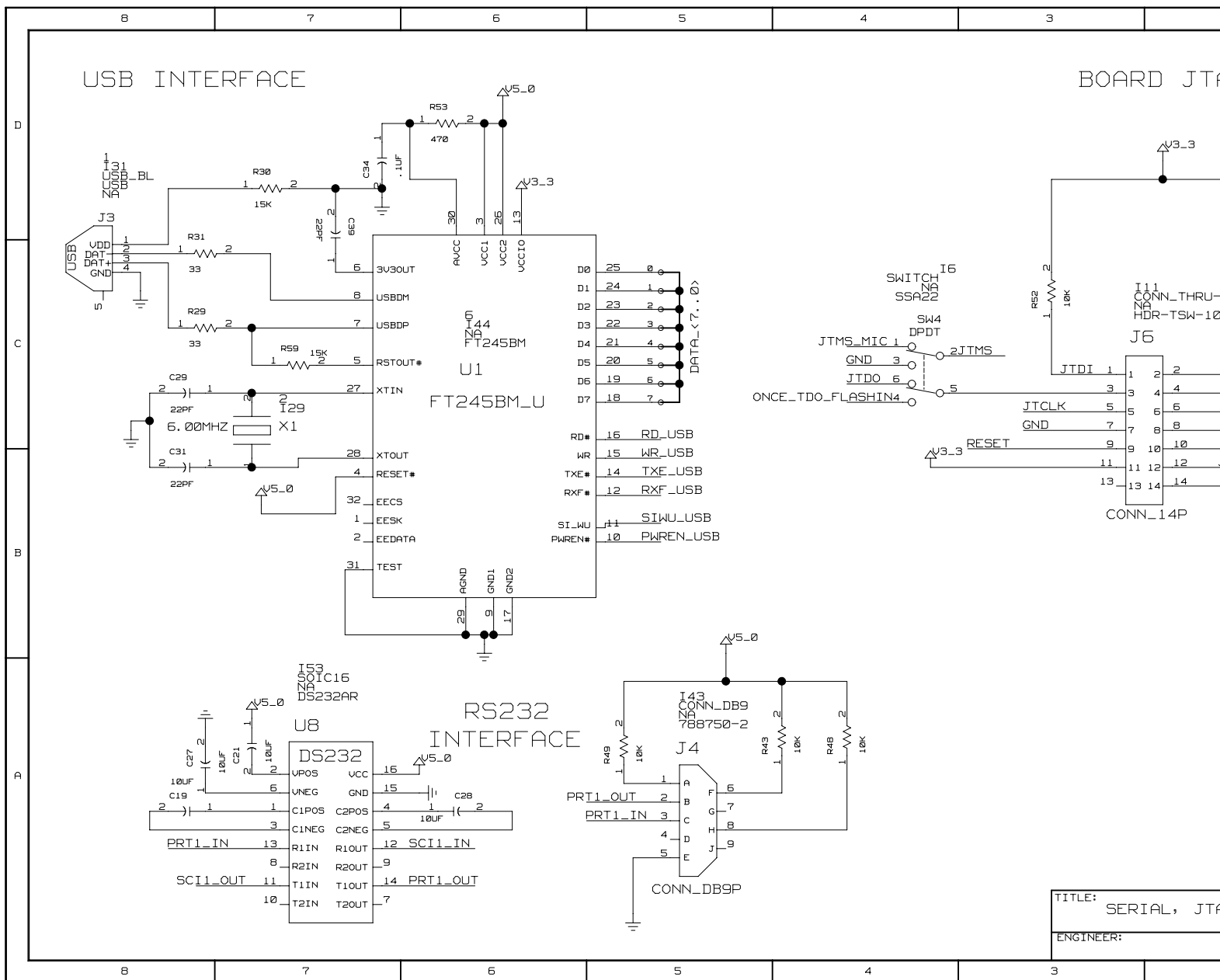
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TITLE: FPGA PORT
ENGINEER:



TITLE: FPGA PORT
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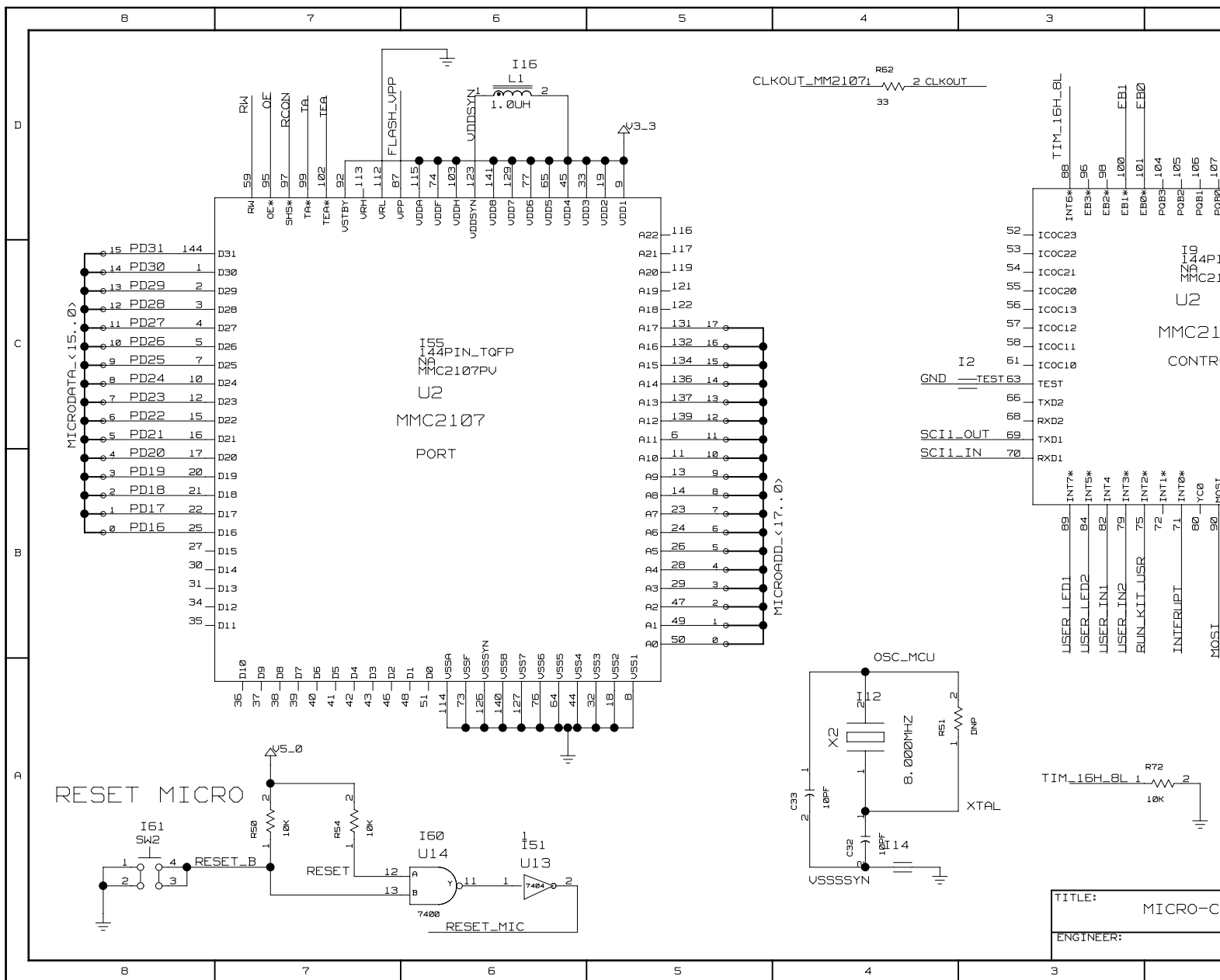


USB INTERFACE

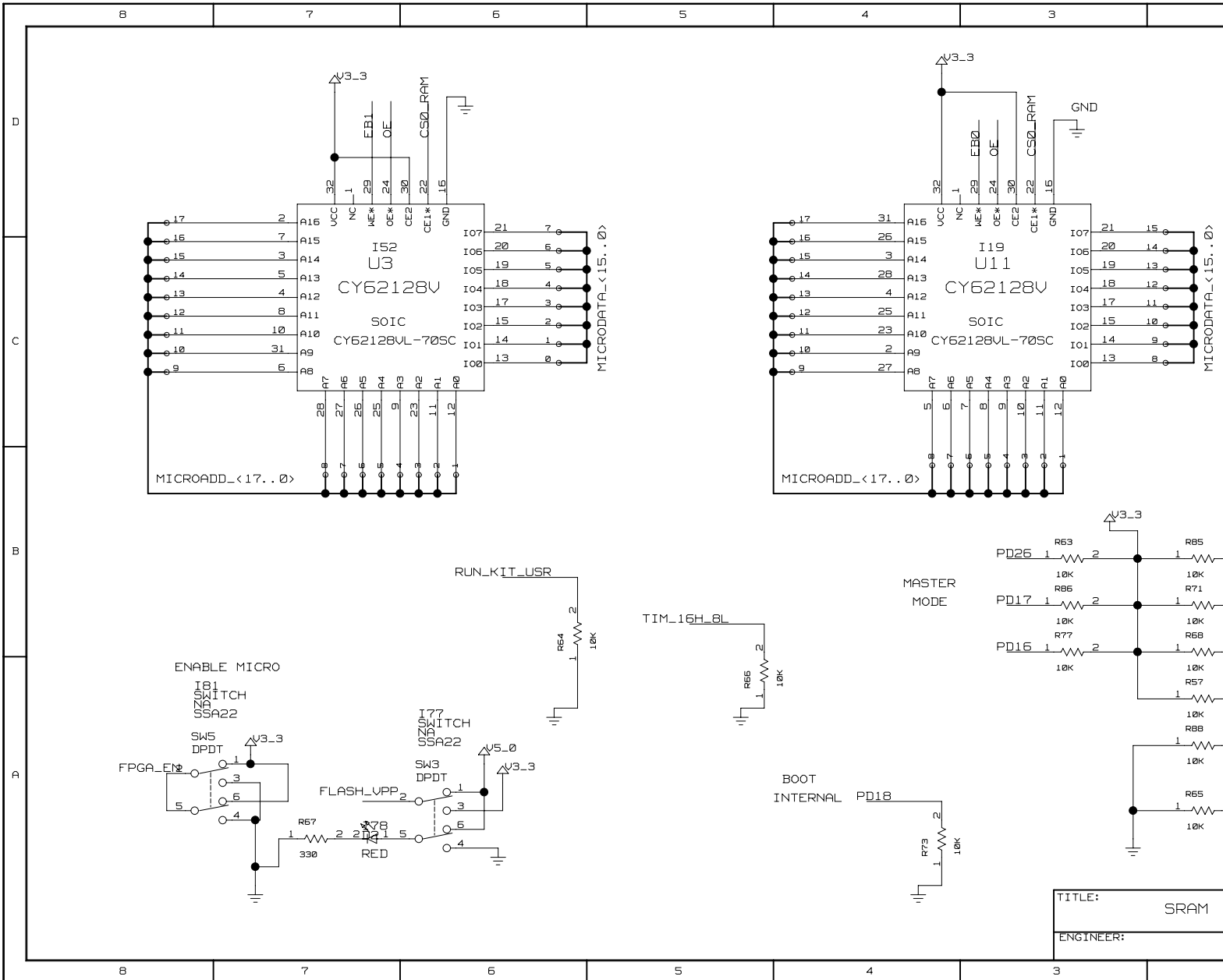
BOARD JTAG

RS232 INTERFACE

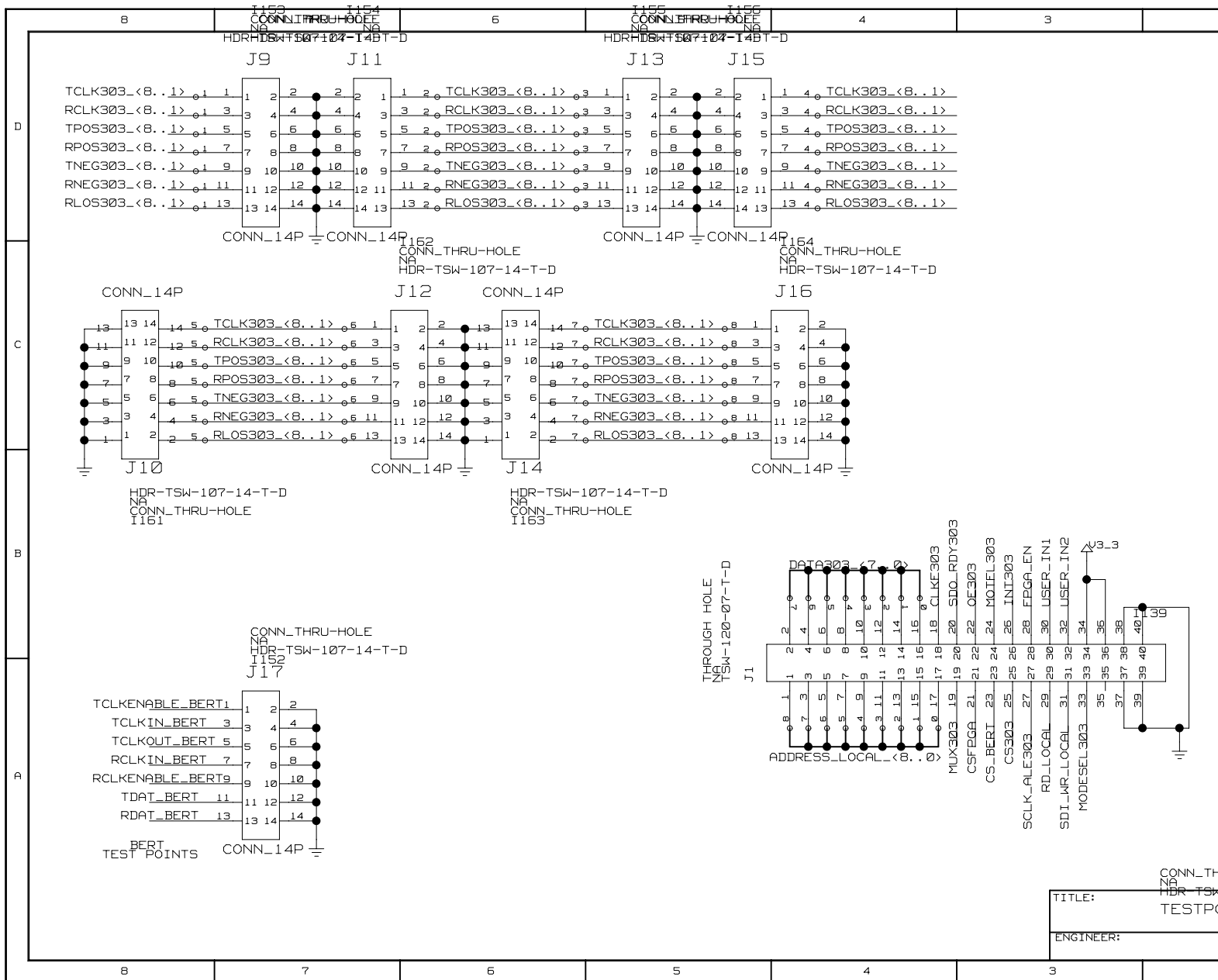
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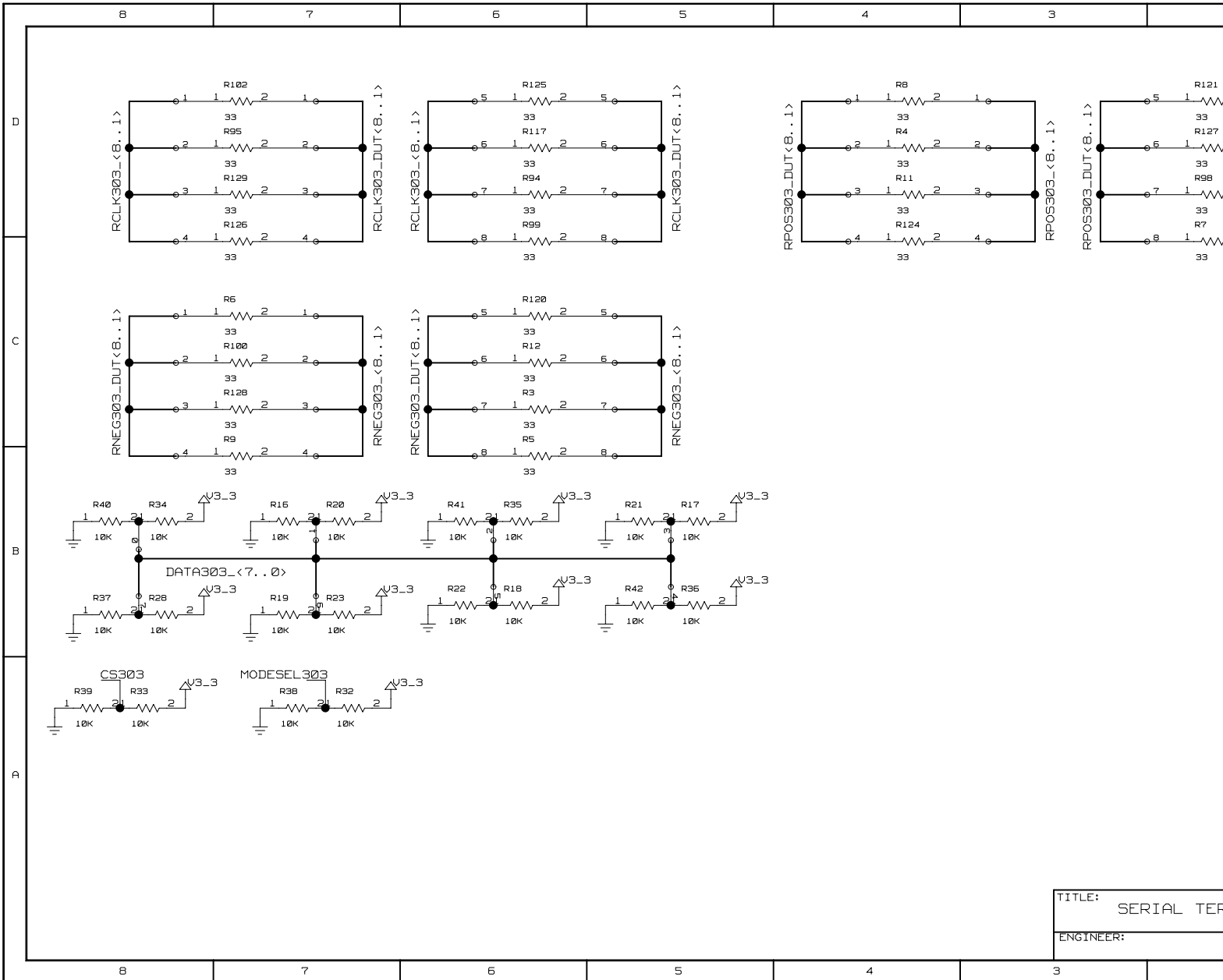
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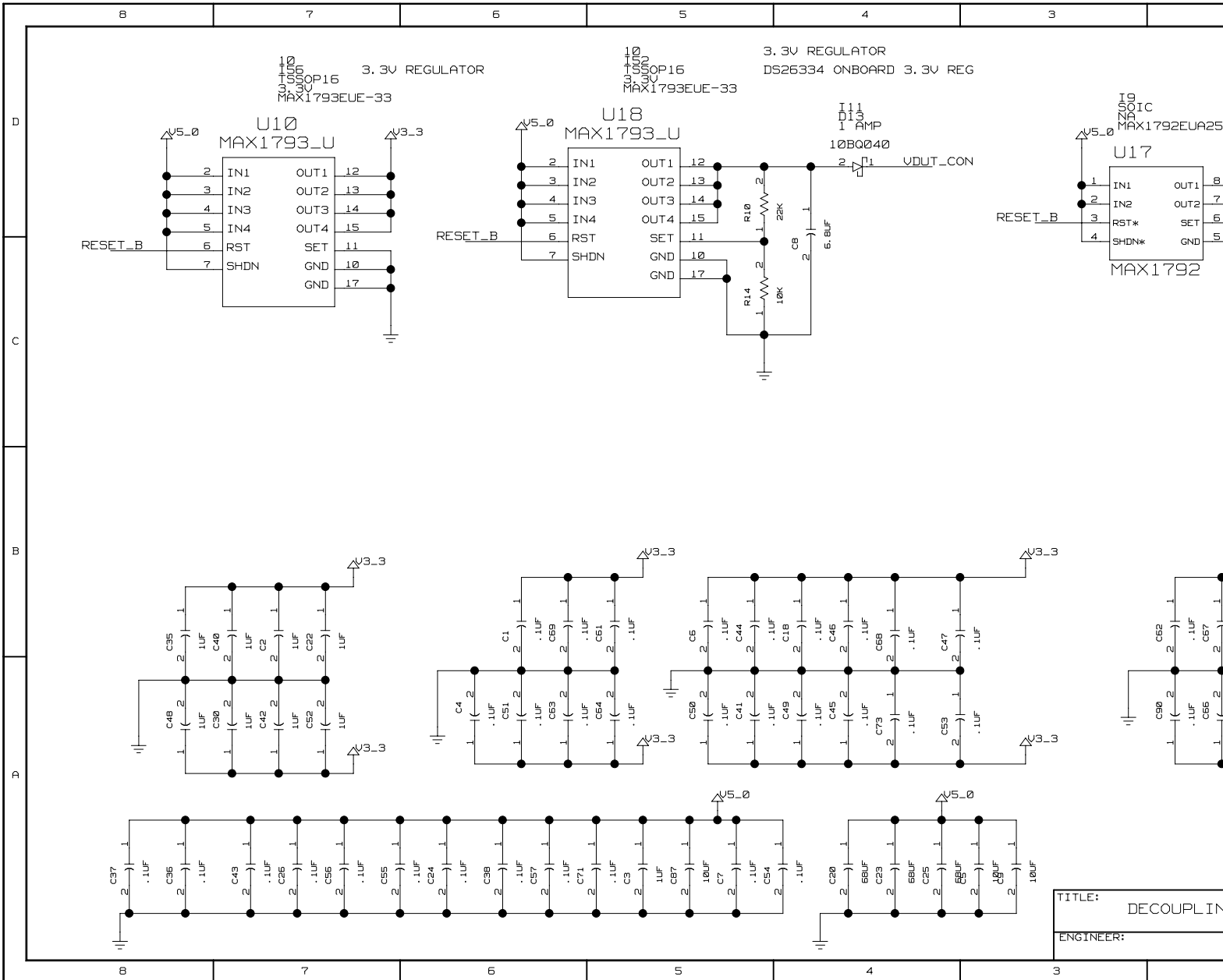
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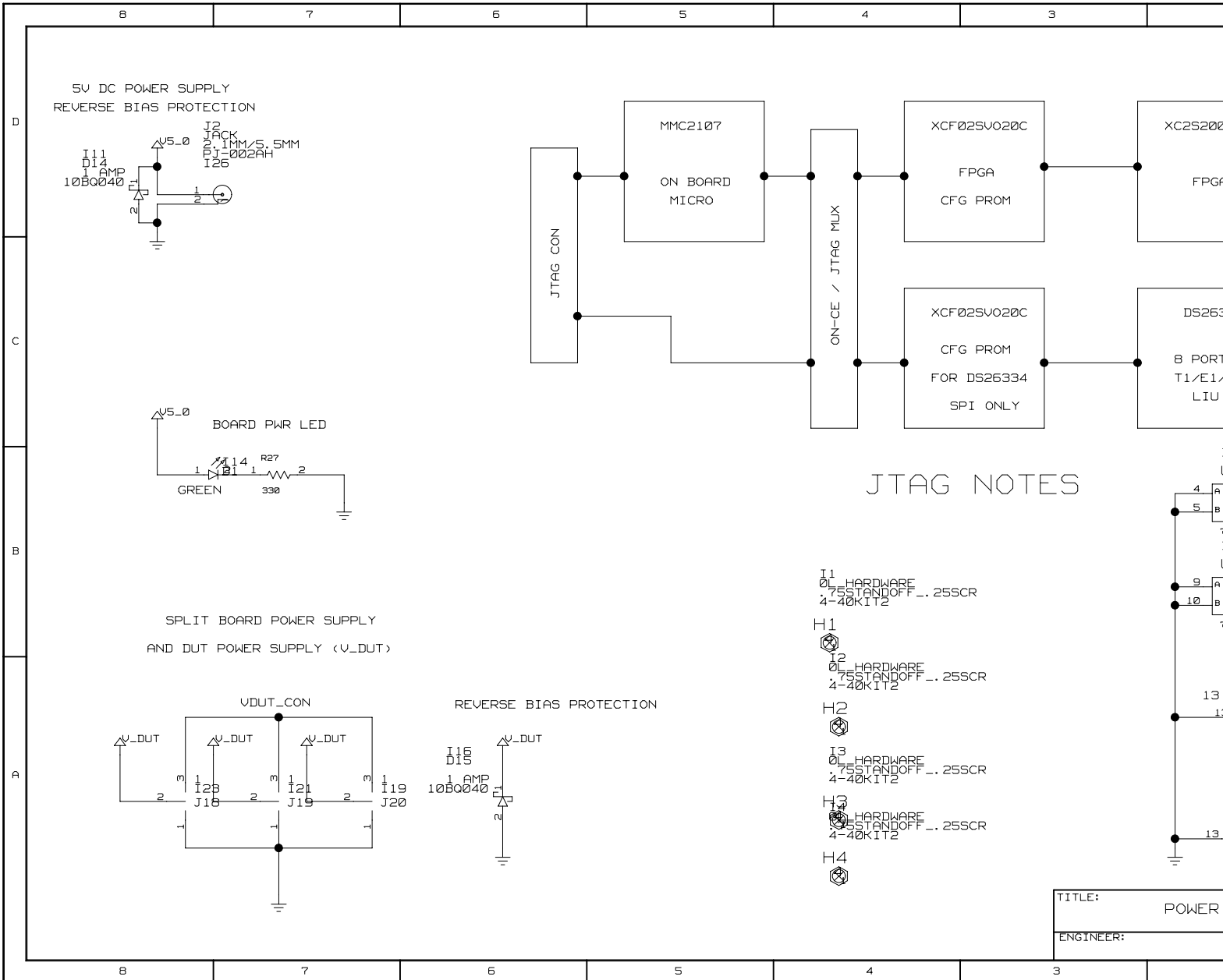
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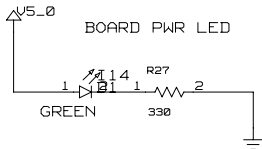
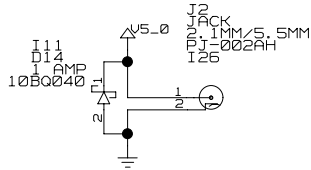
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ENGINEER:



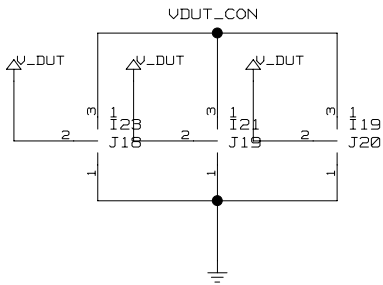
TITLE: DECOUPL IN
 ENGINEER:



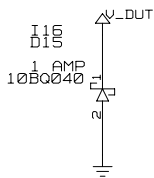
5V DC POWER SUPPLY
REVERSE BIAS PROTECTION



SPLIT BOARD POWER SUPPLY
AND DUT POWER SUPPLY (V_DUT)



REVERSE BIAS PROTECTION



JTAG NOTES

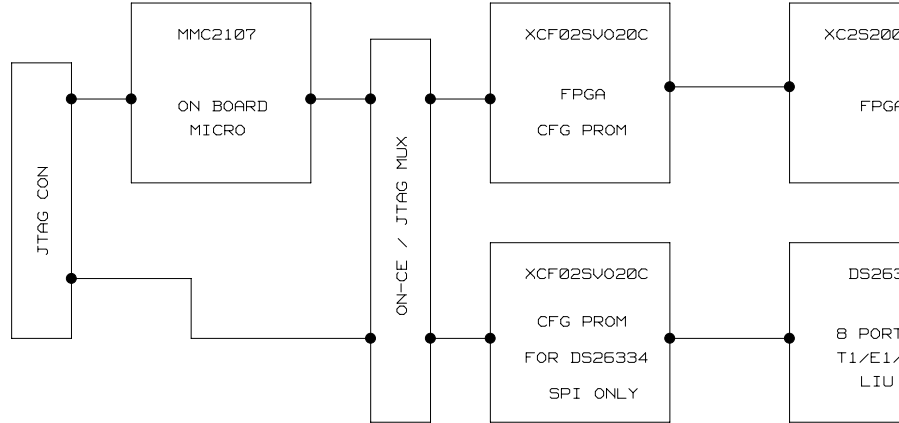
I1
01 HARDWARE
75 STANDOFF .. 25SCR
4-40KIT2

H1
01 HARDWARE
75 STANDOFF .. 25SCR
4-40KIT2

H2
01 HARDWARE
75 STANDOFF .. 25SCR
4-40KIT2

H3
01 HARDWARE
75 STANDOFF .. 25SCR
4-40KIT2

H4
01 HARDWARE
75 STANDOFF .. 25SCR
4-40KIT2



TITLE: POWER
ENGINEER:

NOTES:

D

C

B

A

8

7

6

5

4

3

8

7

6

5

4

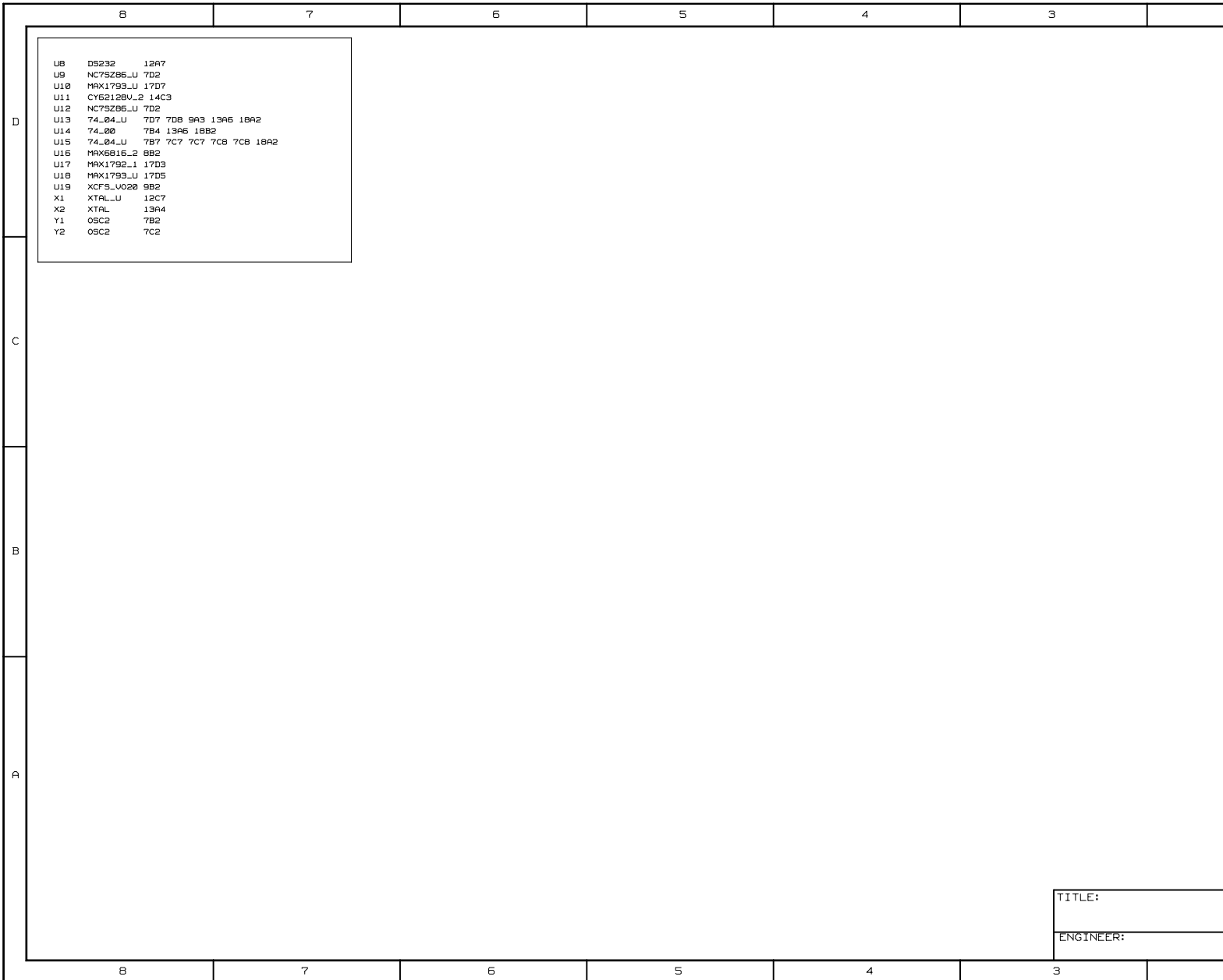
3

TITLE: NOTES

ENGINEER:

	8	7	6	5	4	3
D	<p>*** Signal Cross-Reference for the entire design ***</p> <p>ADDRESS_BERT<3..0> 8C8 11A4 ADDRESS_LOCAL<8..0> 2C7 10D6 15A5 CLK_A 9B1< 9B3<> CFG_DIN_A 9B1< 10B3<> CLKA303 2B3< 7C4< CLKE303 2B3< 10A3<> 15B4<> CLKOUT 10D7< 13D3< CLKOUT_MM2107 13C1< 13D4< CS0_RAM 13C1< 14D3< 14D5< CS2_BOARD 10A4< 13C1<> CS303 2B7< 8C1< 10B7<> 15A3<> 16A8< CSFPGA 10B7<> 15A3<> CS_BERT 8B8< 10B7<> 15A3<> DATA303<7..0> 2C3 11A5 15B4 16B8 DATA<7..0> 8B5 10C3 12C5 DONE_FPGA_A 9A3< 9B1< 9B3<> E1_CLK 7B1< 11D6< EB0 10A4< 13D3<> 14D3< EB1 10A4< 13D3<> 14D7< FLASH_VPP 13D7< 14A7<> FPGA_CLKA 7C3< 7D3< 10C3<> FPGA_EN 10B7<> 14A8<> 15B3<> FPGA_TECLK 7B5< 7C3< 7D3<> 10B3<> INT303 2B3< 7B8< 7D5< 10C3<> 15B3<> INTERUPT 10B3<> 13B2<> JDE_B 12B2<> 13B1<> JDS303OUT_SPI_PROM_IN 2A7< 8A2< 8D3< JFLASHOUT_FPGAIN 9B1< 9C3< JFPGAOUT_DS303IN 2A7< 9C3< JTCLK 2B7< 8D3< 9B3< 9C3< 12B2< 12C3<> 13B2<> JTD1 12C3<> 13D2<> JTDO 9A1< 8D3< 12C4<> JTMS 2A7< 8D3< 9B3< 9C3< 12B1< 12C3<> JTMS_MIC 12B2<> 12C4<> 13B2<> JTAST_B 2B7< 12B2<> 13B2<> LED_RL0S1 7B4< 7D7<> MCLK303 2B3< 7C4< 8C3< MCLK_FPGA 7C3< 10C3<> MICROADD<17..0> 10B7 13B4 14B4 14B8 MICRODATA<15..0> 10A5 10D5 13B8 14C2 14C5 MISO 10B7<> 13A2<> MODESEL303 2C7< 10B3<> 15A3<> 16A7< MOS1 10B7<> 13A2<> MOTEL303 2B7< 10B3<> 15B3<> MUX303 2B7< 10B3<> 15A4<> OE 10A4<> 13D7<> 14D3< 14D7< OE303 2C3< 10B3<> 15B3<> ONCE_TDO_FLASHIN 9B3< 12C4<> 13D2<> OSC_MCU 13B2<> 13B4<> PD16 13B8<> 14B3< PD17 13B8<> 14B3< PD18 13B8<> 14A4< PD19 13B8<> 14A2< PD20 13B8<> PD21 13C8<> 14B2< PD22 13C8<> 14B2< PD23 13C8<> 14B2< PD24 13C8<> PD25 13C8<> PD26 13C8<> 14B3< PD27 13C8<> PD28 13C8<> 14A2< PD29 13C8<> PD30 13C8<> PD31 13C8<> PROGRAM_FPGA_A 9B1< 9B3< PRT1_IN 12A6< 12A8< PRT1_OUT 12A6< 12A6< PWREN_USB 10D4< 12B5< RCLK303<8..1> 11A6 15C5 15C8 15D3< 15D6 15D8< 16C6 16C8 RCLK303_DUT<8..1> 3B1< 3B4< 3C1< 3C4< 4B1< 4B5< 4C1< 4C5< 16C5 16C7 RCLKENABLE_BERT 8A6< 8D7< 10A6<> 15A8<></p>					
C	<p>RCLKIN_BERT 8D7< 10A6<> 15A8<> RCON 10A4<> 13D7<> 14A2< RDAT_BERT 8D8< 10A6<> 15A8<> RD_LOCAL 2B7< 8B8< 10B7<> 15A3<> RD_USB 10A6<> 12C5< RESET 12B3<> 13A7< RESET_B 9B1<> 19A8<> 17C5< 17C8< 17D3< RESET_CFGPRM 8A3<> 8C3<> RESET_MIC 13A6< 13C1<> RLOS303<8..1> 2B3 7C5< 7C8 11D4 15C5 15C8 15D3< 15D6 15D8< RLOSCON_1 7B5< 10D4<> RNEG303<8..1> 11B3 15C5 15C8 15D3< 15D6 15D8< 16B5 16B7 RNEG303_DUT<8..1> 3B1< 3B4< 3C1< 3C4< 4B1< 4B5< 4C1< 4C5< 16B6 16B8 RPOS303<8..1> 11B7 15C5 15C8 15D3< 15D6 15D8< 16C1 16C3 RPOS303_DUT<8..1> 3B1< 3B4< 3C1< 3C4< 4B1< 4B5< 4C1< 4C5< 16C3 16C4 RRING303<8..1> 3B4< 3B8< 3C4< 3C8< 4B4< 4B8< 4C4< 4C8< 5A1< 5A5< 5C1< 5C5< 6A1< 6A5< 6B5< 6C1<> RTIP303<8..1> 3B4< 3B8< 3D4< 3D8< 4B4< 4B8< 4C4< 4C8< 5A5< 5B1< 5C1< 5C5< 6A1< 6A5< 6C1< 6C5< RUN_KIT_USR 13B3<> 14B6< RW 10A4<> 13D7<> RXF_USB 10B3<> 12B5< R_PB_CFG 8A2<> 8B2< SCANMODE303 2A3< 7D5< SC11_IN 12A6< 13A4<> SC11_OUT 12A8< 13C4<> SCK 10B7<> 13C1<> CLK_RLE303 2B7< 8C1< 10B7<> 15A3<> SDI_LR_LOCAL 2B7< 8B8< 8C1< 10A7<> 15A3<> SDO_RDY303 2C7< 10B3<> 15B4<> SIW_USB 10D4<> 12B5< SS 10B7<> 13B1<> T1_CLK 7B1< 11C7< TA 10A3<> 13D7<> TCLK303<8..1> 3B4< 3B8< 3C4< 3C8< 4A4< 4A8< 4C4< 4C8< 11B3 15C5 15C8 15D3< 15D6 15D8<</p>					
B	<p>TCLKENABLE_BERT 8A6< 8B8< 10A5<> 15A8<> TCLKIN_BERT 8B8< 10A5<> 15A8<> TCLKOUT_BERT 8D5< 10A6<> 15A8<> TDAT_BERT 8C5< 10A6<> 15A8<> TEA 10A3<> 13D7<> TEST 13C3<> TIM_16H_8L 13A3< 13D3<> 14B5< TNEG303<8..1> 3B4< 3B8< 3C4< 3C8< 4B4< 4B8< 4C4< 4C8< 11D5 15C5 15C8 15D3< 15D6 15D8<</p>					
A	<p>TPOS303<8..1> 3B4< 3B8< 3C4< 3C8< 4B4< 4B8< 4C4< 4C8< 11A7 15C5 15C8 15D3< 15D6 15D8<</p> <p>TRING303<8..1> 3B1< 3B5< 3C1< 3C5< 4B1< 4B5< 4C1< 4C5< 5B1< 5B5< 5D1< 5D5< 6B1< 6B5< 6D1< 6D5< TTIP303<8..1> 3B1< 3B5< 3D1< 3D5< 4B1< 4B5< 4C1< 4C5< 5B1< 5B5< 5D1< 5D5< 6B1< 6B5< 6D1< 6D5<</p> <p>TXE_USB 10B3<> 12B5< USER_CLK 7A2<> 10C7< USER_IN1 13A2< 13B3<> 15B3<> USER_IN2 13A2< 13B3<> 15B3<> USER_LED1 13A2< 13B3<> USER_LED2 13A2< 13B3<> VDDSYN 13D5<> VDUT_CON 17D4<> 10A7<> VSSSYN 13A4< WR_USB 10A4<> 12B5< XTAL 13A3<> 13B2<></p>					
	8	7	6	5	4	3

TITLE:
ENGINEER:



- U8 DS232 12A7
- U9 NC75Z86.U 7D2
- U10 MAX1793.U 17D7
- U11 CY62128V.2 14C3
- U12 NC75Z86.U 7D2
- U13 74.04.U 7D7 7D8 9A3 13A6 18A2
- U14 74.00 7B4 13A6 18B2
- U15 74.04.U 7B7 7C7 7C7 7C8 7C8 18A2
- U16 MAX6816.2 8B2
- U17 MAX1792.1 17D3
- U18 MAX1793.U 17D5
- U19 XCFS_V020 9B2
- X1 XTAL.U 12C7
- X2 XTAL 13A4
- Y1 OSC2 7B2
- Y2 OSC2 7C2

TITLE:
ENGINEER: