DS2433
4kb 1-Wire EEPROM

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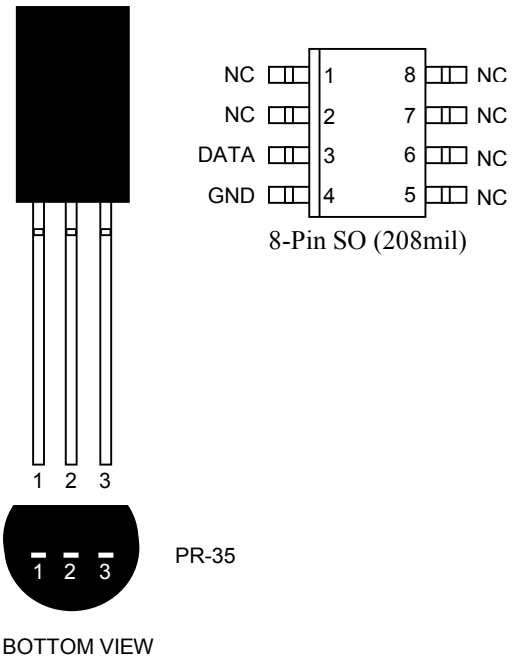
FEATURES

- 4096 bits Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute identity because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN™ products
- Memory partitioned into sixteen 256-bit pages for packetizing data
- 256-bit scratchpad with strict read/write protocols ensures integrity of data transfer
- Reduces control, address, data, and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbps
- Overdrive mode boosts communication speed to 142kps
- 8-bit family code specifies DS2433 communication requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Low cost PR-35 or 8-pin SO surface mount package
- Reads and writes over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C

PIN ASSIGNMENT



PIN DESCRIPTION

	PR-35	SO
Pin 1	Ground	NC
Pin 2	Data	NC
Pin 3	NC	Data
Pin 4	—	Ground
Pin 5-8	—	NC

ORDERING INFORMATION

DS2433	PR-35 package
DS2433S	8-pin SOIC package
DS2433S/T&R	Tape & Reel version of DS2433S
DS2433X	Chip Scale Pkg., Tape & Reel
DS2433X-S	Chip-Scale Pkg, 2.5k pc., Tape & Reel

SILICON LABEL DESCRIPTION

The DS2433 4kb 1-Wire® EEPROM identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2433 consists of a factory-lasered registration

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number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (23h) plus 4096 bits of user-programmable EEPROM. The power to read and write the DS2433 is derived entirely from the 1-Wire communication line. The memory is organized as sixteen pages of 256 bits each. The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it may be read back for verification. A copy scratchpad command will then transfer the data to memory. This process insures data integrity when modifying the memory. The 64-bit registration number provides a guaranteed unique identity which allows for absolute traceability and acts as node address if multiple DS2433 are connected in parallel to form a local network. Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The PR-35 and SOIC packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, board identification and product revision status.

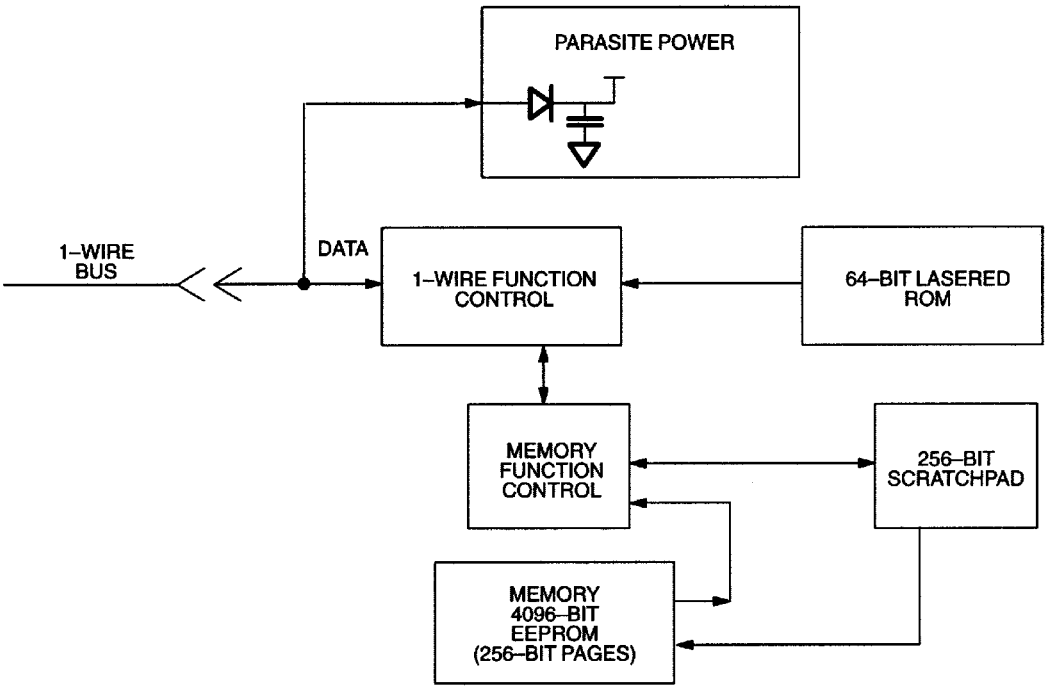
OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2433. The DS2433 has three main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, and 3) 4096-bit EEPROM. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the six ROM Function Commands, 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, 5) Overdrive-Skip ROM or 6) Overdrive-Match ROM. Upon completion of an overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry “steals” power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met.

Figure 1. DS2433 BLOCK DIAGRAM



64-BIT LASERED ROM

Each DS2433 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8+ X^5+ X^4+ 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the *Book of DS19xx iButton® Standards*.

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, then the serial number is entered. After the 48^{th} bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

MEMORY

The memory map in Figure 5 shows a 32-byte page called the scratchpad and additional 32-byte pages called memory. The DS2433 contains pages 0 through 15 that make up the 4096-bit EEPROM. The scratch-pad is an additional page that acts as a buffer when writing to memory.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS2433 employs three address registers, called TA1, TA2 and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and Transfer Status register. It is used to verify data integrity with write commands. Therefore, the master only has read access to this register. The lower five bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF, is set if the number of data bits sent by the master is not an integer multiple of 8 or if the data in the scratchpad is not valid due to a loss of power. A valid write to the scratchpad will clear the PF bit. Bit 6 has no function; it always reads 0. Note that the lowest five bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address (TA1) for a Write command is 03CH for example, then the scratchpad will store incoming data beginning at the byte offset 1CH and will be full after only four

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bytes. The corresponding ending offset in this example is 1FH. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1FH. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the Partial Flag support the master checking the data integrity after a Write command. The highest valued bit of the E/S register, called AA is valid only if the PF flag reads 0. If PF is 0 and AA is 1, a copy has taken place. The AA bit is cleared when the device receives a write scratchpad command.

WRITING WITH VERIFICATION

To write data to the DS2433, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Under certain conditions (see Write Scratchpad command) the master will receive an inverted CRC16 of the command, address and data at the end of the write scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated itself to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC16, it has to send the Read Scratchpad command to read back the scratchpad to verify data integrity. As preamble to the scratchpad data, the DS2433 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the Write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue reading and verifying every data byte. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2 and E/S. The master may obtain the contents of these registers by reading the scratchpad or derive it from the target address and the amount of data to be written. As soon as the DS2433 has received these bytes correctly, it will copy the data to the requested location beginning at the target address.

Figure 2. HIERARCHCAL STRUCTURE FOR 1-WIRE PROTOCOL

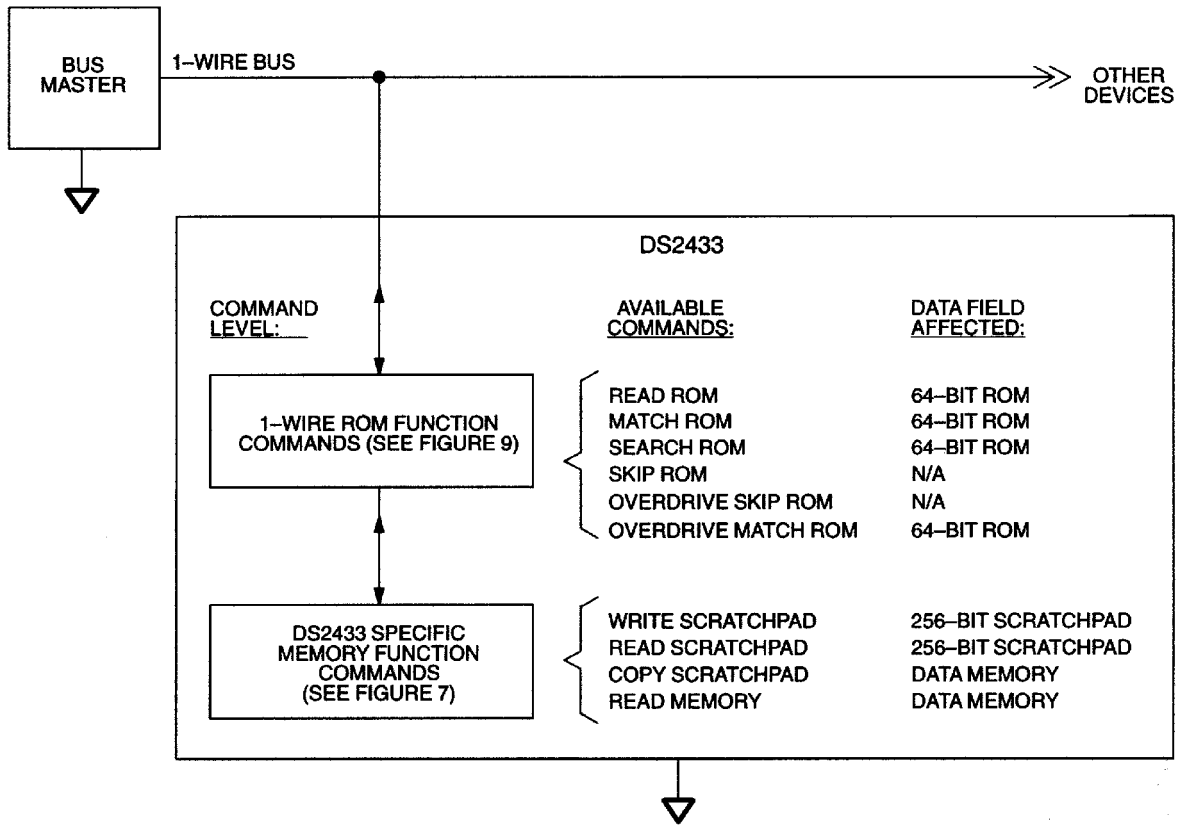


Figure 3. 64-BIT LASERED ROM

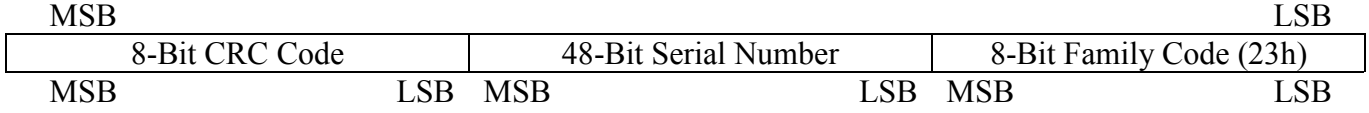
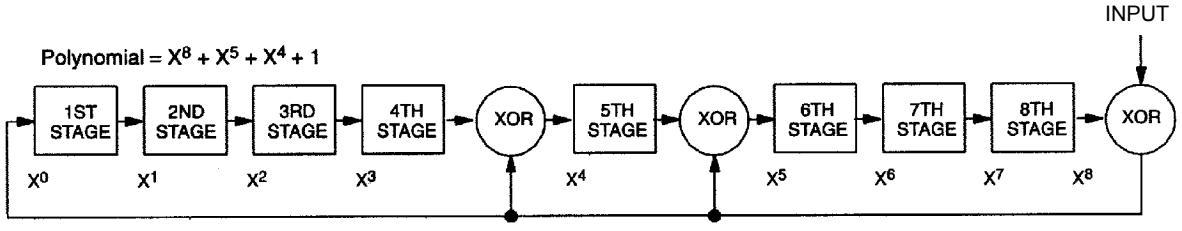


Figure 4. 1-WIRE CRC GENERATOR



MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 7) describes the protocols necessary for accessing the memory. An example follows the flowchart. The communication between master and DS2433 takes place either at regular speed (default, OD = 0) or at Overdrive Speed (OD = 1). If not explicitly set into the Overdrive Mode the DS2433 assumes regular speed.

WRITE SCRATCHPAD COMMAND [0FH]

After issuing the write scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4:E0) will be the byte offset at which the master stops

writing data. Only full data bytes are accepted. If the last data byte is incomplete its content will be ignored and the partial byte flag PF will be set.

When executing the Write Scratchpad command the CRC generator inside the DS2433 (see Figure 12) calculates a CRC over the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC16 polynomial by first clearing the CRC generator and then shifting in the command code (0FH) of the Write Scratchpad command, the Target Addresses TA1 and TA2 as supplied by the master and all the data bytes. The master may end the Write Scratchpad command at any time. However, if the ending offset is 11111b, the master may send 16 read time slots and will receive the CRC generated by the DS2433.

The memory address range of the DS2433 is 0000H to 01FFH. If the bus master sends a target address higher than this, the internal circuitry of the chip will set the seven most significant address bits to zero as they are shifted into the internal address register. The Read Scratchpad command will reveal the target address as it will be used by the DS2433. The master will identify such address modifications by comparing the target address read back to the target address transmitted. If the master does not read the scratchpad, a subsequent copy scratchpad command will not work since the most significant bits of the target address the master sends will not match the value the DS2433 expects.

READ SCRATCHPAD COMMAND [AAH]

This command is used to verify scratchpad data and target address. After issuing the read scratchpad command, the master begins reading. The first two bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4: T0). The master may read data until the end of the scratchpad after which the data read will be all logic 1's.

COPY SCRATCHPAD [55H]

This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the master must provide a 3-byte authorization pattern which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. Copy takes 5 ms maximum during which the voltage on the 1-Wire bus must not fall below 2.8V. A pattern of alternating 1s and 0s will be received after the data has been copied until a Reset Pulse is issued by the master.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command.

Figure 5. DS2433 MEMORY MAP

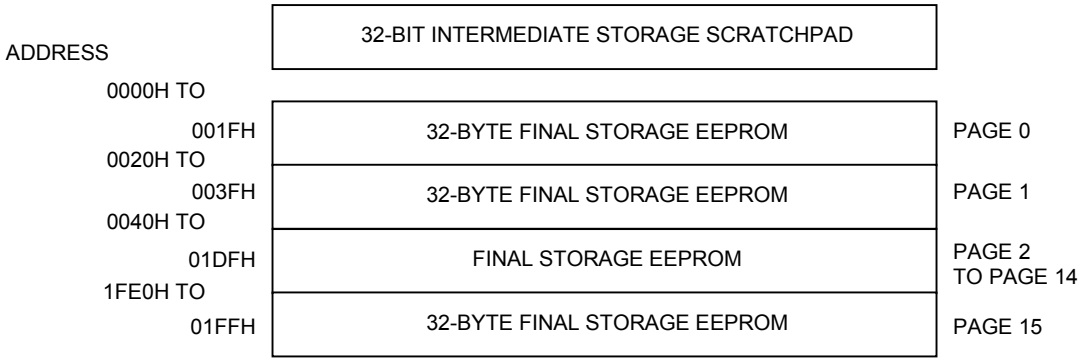
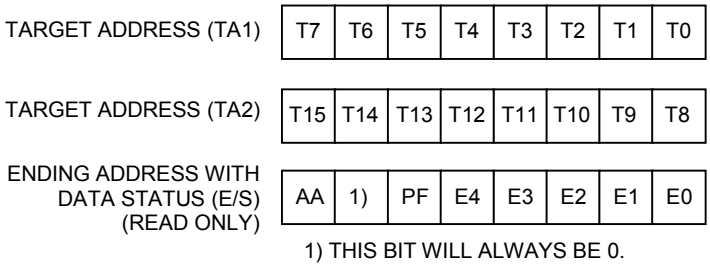


Figure 6. ADDRESS REGISTER



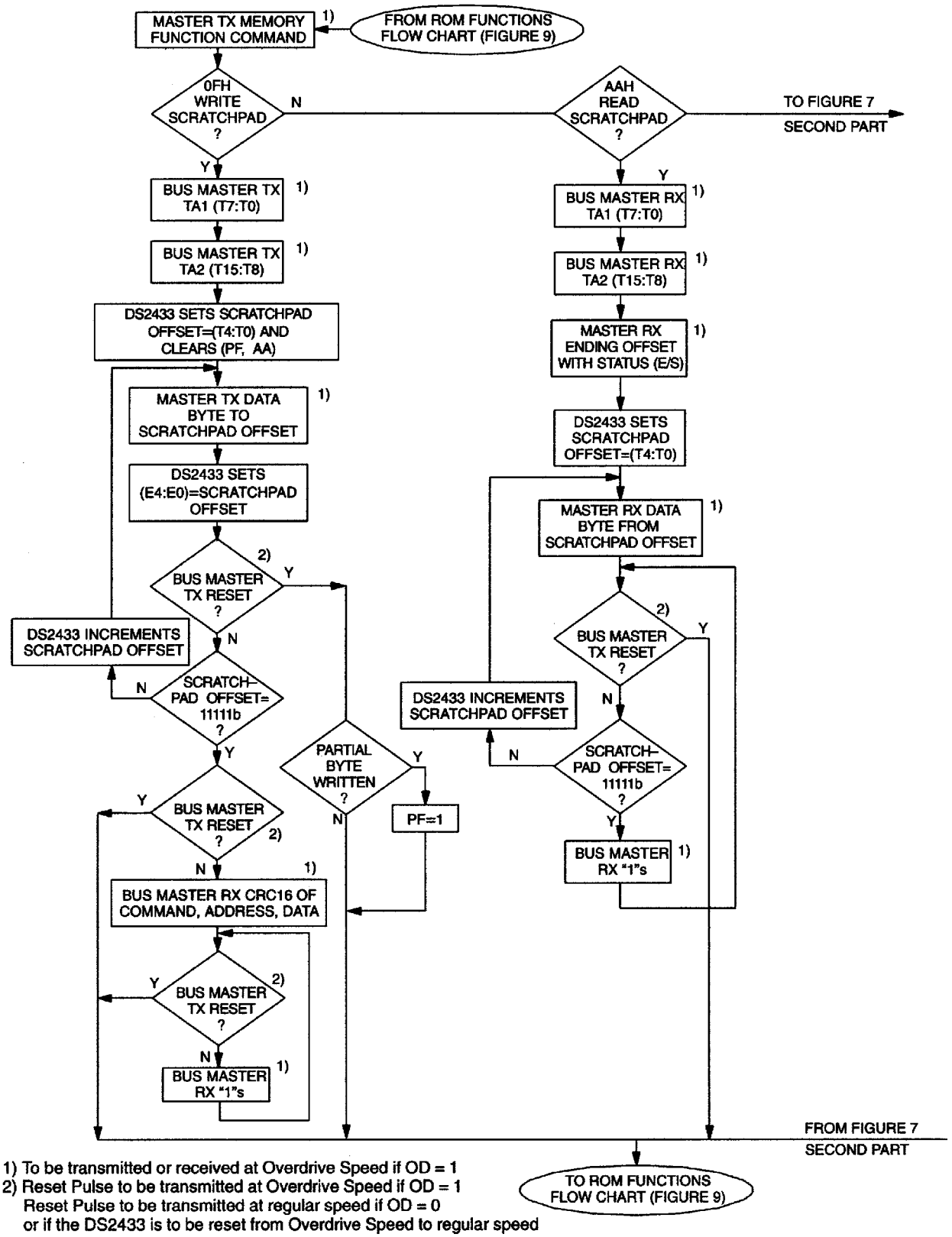
1) THIS BIT WILL ALWAYS BE 0.

READ MEMORY [F0H]

The read memory command may be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the two bytes, the master reads data beginning from the target address and may continue until the end of memory, at which point logic 1's will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

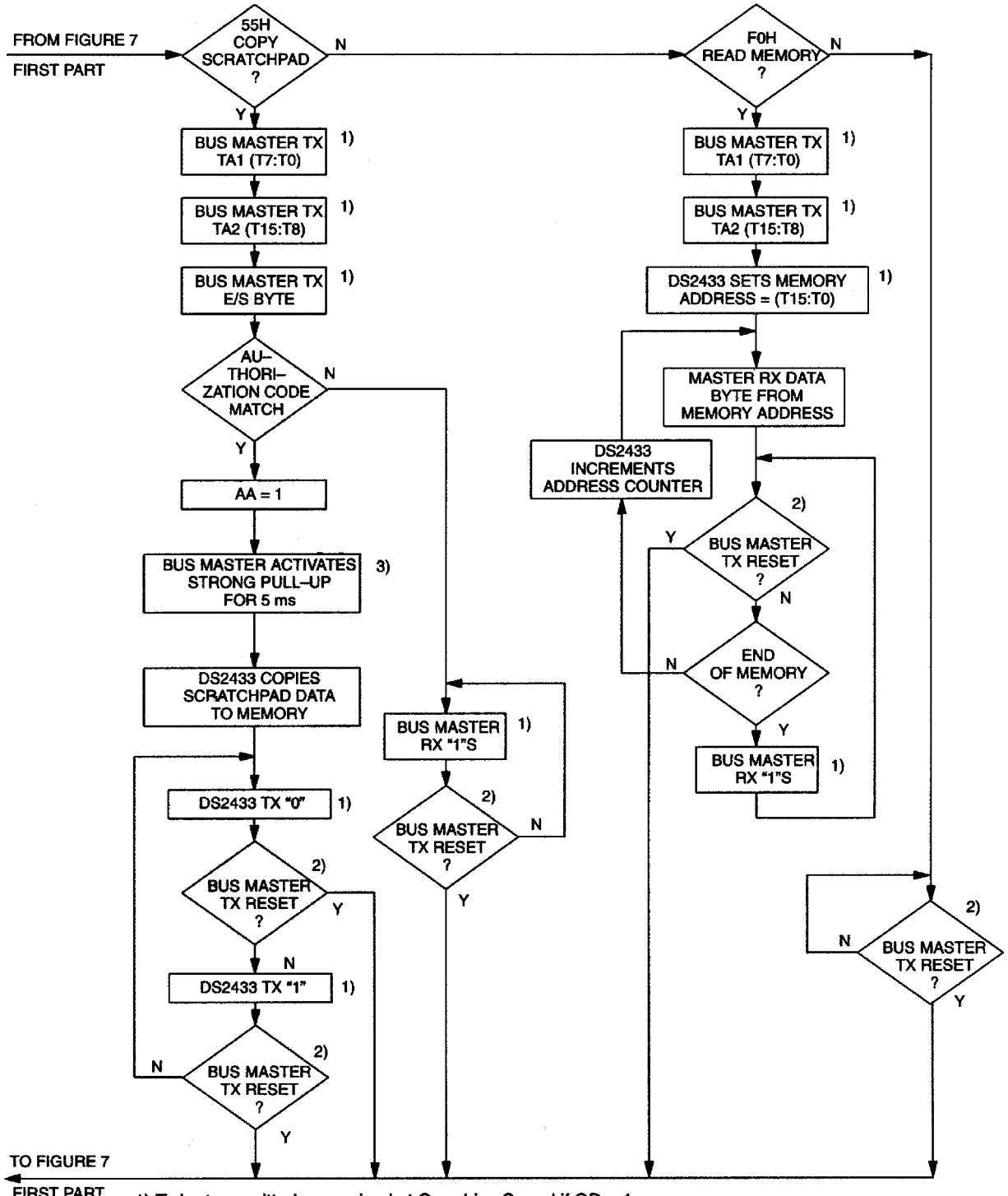
The hardware of the DS2433 provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to insure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the *Book of DS19xx iButton Standards*, Chapter 7 or *Application Note 114* for the recommended file structure.)

Figure 7. MEMORY FUNCTION FLOW CHART



1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS2433 is to be reset from Overdrive Speed to regular speed

Figure 7. MEMORY FUNCTION FLOW CHART (continued)



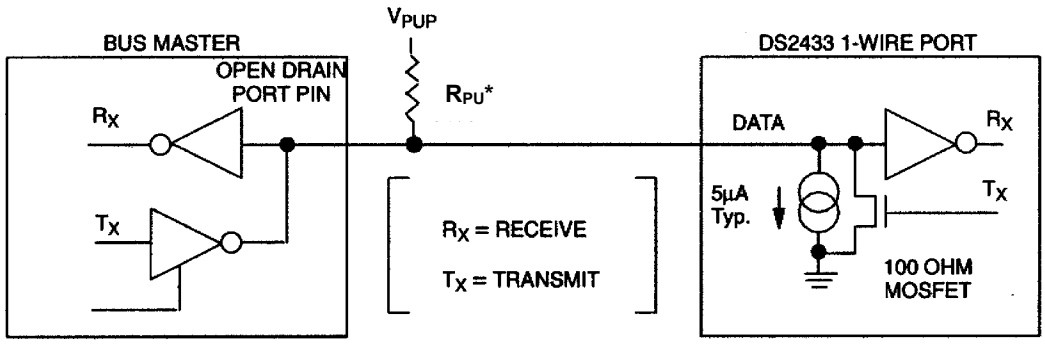
1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1 Reset Pulse to be transmitted at regular speed if OD = 0 or if the DS2433 is to be reset from Overdrive Speed to regular speed
3) The strong pull-up has to start within 3 µs after t_{LOW0}. (Figure 11)
With $V_{PUP} \geq 4.0V$ and $R_{PUP} \leq 2.2k\Omega$ the 1-Wire bus may be left idle high for 5 ms, instead.

MEMORY FUNCTION EXAMPLE

Example: Write two data bytes to memory location 0026 and 0027. Read entire memory.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset Pulse (480 - 960 µs)
RX	Presence	Presence Pulse
TX	CCH	Issue Skip ROM Command
TX	0FH	Issue Write Scratchpad command
TX	26H	TA1, beginning offset = 26H
TX	00H	TA2, address = 0026H
TX	<2 data bytes>	Write 2 bytes of data to scratchpad
TX	Reset	Reset Pulse
RX	Presence	Presence Pulse
TX	CCH	Issue Skip ROM Command
TX	AAH	Issue Read Scratchpad command
RX	26H	Read TA1, beginning offset = 26H
RX	00H	Read TA2, address = 0026H
RX	07H	Read E/S, ending offset = 7H, flags = 0H
RX	<2 data bytes>	Read scratchpad data and verify
TX	Reset	Reset Pulse
RX	Presence	Presence Pulse
TX	CCH	Issue Skip ROM Command
TX	55H	Issue Copy Scratchpad command
TX	26H	TA1
TX	00H	TA2 AUTHORIZATION CODE
TX	07H	E/S
TX	<idle or strong pullup>	Wait 5ms
TX	Reset	Reset Pulse
RX	Presence	Presence Pulse
TX	CCH	Issue Skip ROM Command
TX	F0H	Issue Read Memory command
TX	00H	TA1, beginning offset = 0
TX	00H	TA2, address = 0000H
RX	<512 bytes>	Read entire memory
TX	Reset	Reset Pulse
RX	Presence	Presence Pulse, done

Figure 8. HARDWARE CONFIGURATION



*5kΩ is adequate for reading the DS2433. To write to a single device, a 2.2kΩ resistor and V_{PUP} of at least 4.0V is sufficient. For writing multiple DS2433s simultaneously or operation at low V_{PUP}, the R_{PU} should be bypassed by a low-impedance pullup to V_{PUP} while the device copies the scratchpad to EEPROM. Depending on the 1-Wire communication speed and the bus-load characteristics, the optimal pullup resistor (R_{PU}) value will be in the 1.5kΩ to 5kΩ range.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS2433 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the *Book of DS19xx iButton Standards*.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2433 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3kbps. The speed can be boosted to 142kbps by activating the Overdrive Mode. The 1-Wire bus requires a pullup resistor of approximately 5kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (Overdrive Speed) or more than 120µs (regular speed), one or more devices on the bus may be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2433 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a Reset Pulse transmitted by the bus master followed by Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that the DS2433 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the six ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 9):

READ ROM [33H]

This command allows the bus master to read the DS2433's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS2433 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

MATCH ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2433 on a multidrop bus. Only the DS2433 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a Reset Pulse. This command can be used with a single or multiple devices on the bus.

SKIP ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

SEARCH ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the *Book of DS19xx iButton Standards* for a comprehensive discussion of a search ROM, including an actual example.

OVERDRIVE SKIP ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2433 in the Overdrive Mode (OD = 1). All communication following this

command has to occur at Overdrive Speed until a Reset Pulse of minimum 480µs duration resets all devices on the bus to regular speed (OD = 0).

When issued on a multidrop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a Reset Pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wire-AND result).

OVERDRIVE MATCH ROM [69H]

The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive Speed, allows the bus master to address a specific DS2433 on a multidrop bus and to simultaneously set it in Overdrive Mode. Only the DS2433 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All overdrive-capable slaves will return to regular speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

Figure 9. ROM FUNCTIONS FLOW CHART (first part)

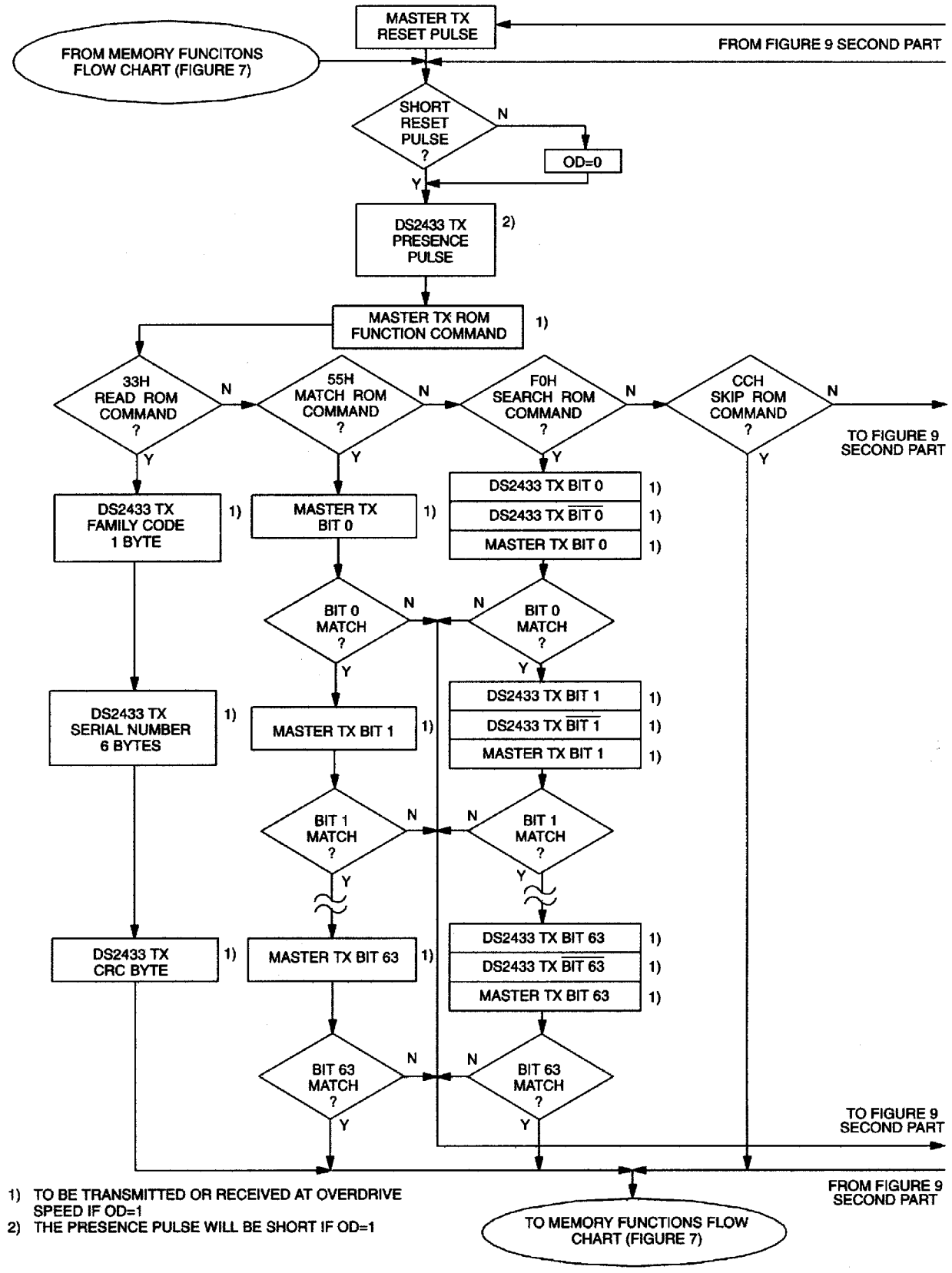
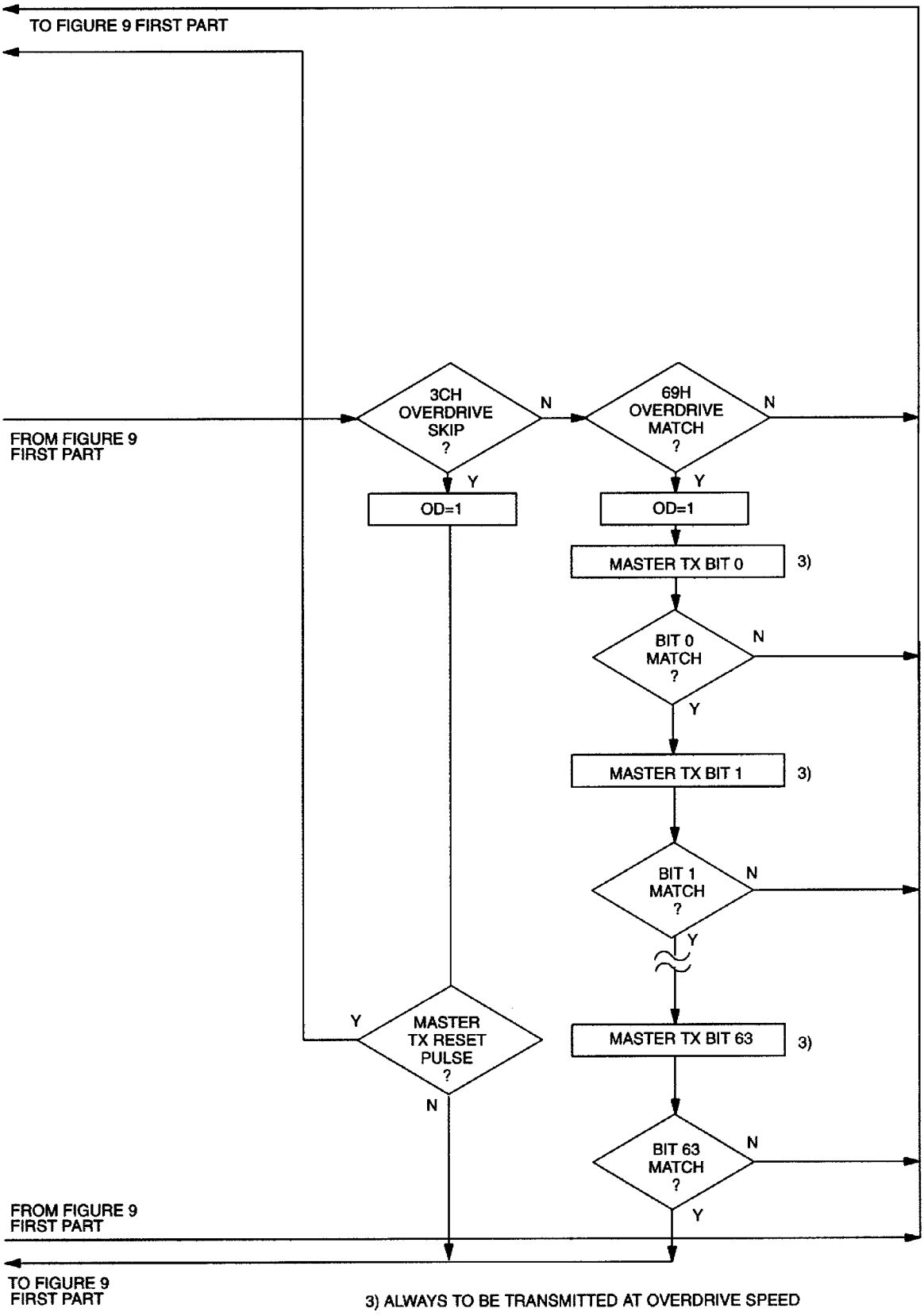


Figure 9. ROM FUNCTIONS FLOW CHART (continued)



1-WIRE SIGNALING

The DS2433 requires strict protocols to insure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except Presence Pulse are initiated by the bus master. The DS2433 can communicate at two different speeds, regular speed and Overdrive Speed. If not explicitly set into the overdrive mode, the DS2433 will communicate at regular speed. While in Overdrive Mode the fast timing applies to all wave forms.

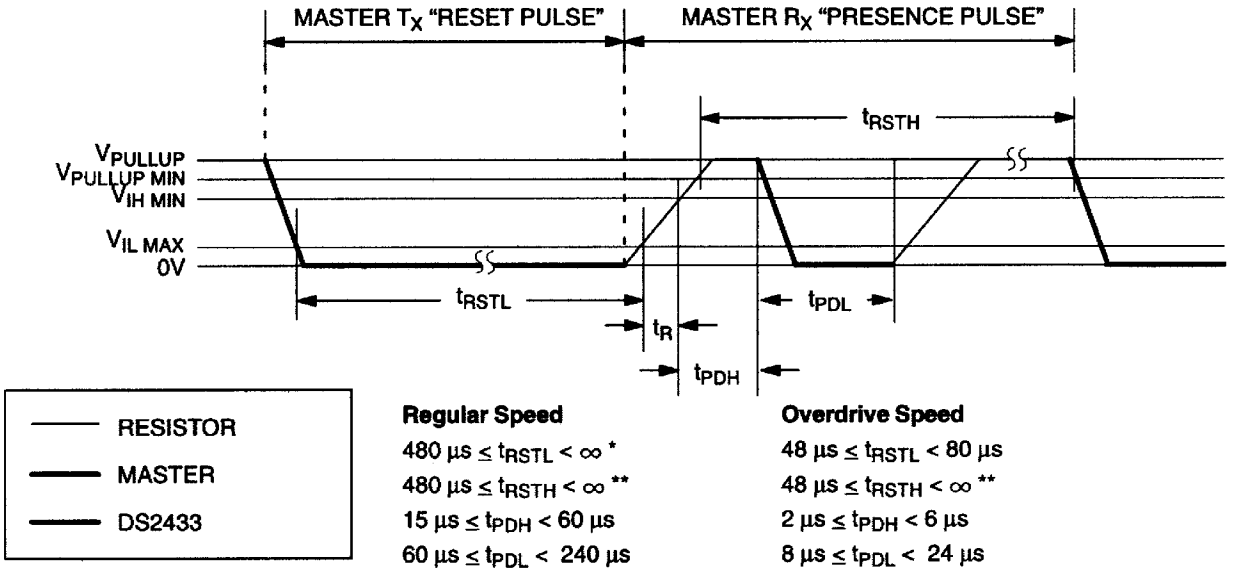
The initialization sequence required to begin any communication with the DS2433 is shown in Figure 10. A Reset Pulse followed by a Presence Pulse indicates the DS2433 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (TX) a Reset Pulse (t_{RSTL}, minimum 480µs at regular speed, 48µs at Overdrive Speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS2433 waits (t_{PDH}, 15-60µs at regular speed, 2-6µs at Overdrive speed) and then transmits the Presence Pulse (t_{PDL}, 60-240µs at regular speed, 8-24µs at Overdrive Speed).

A Reset Pulse of 480 µs or longer will exit the Overdrive Mode returning the device to regular speed. If the DS2433 is in Overdrive Mode and the Reset Pulse is no longer than 80µs the device will remain in Overdrive Mode.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2433 to the master by triggering a delay circuit in the DS2433. During write time slots, the delay circuit determines when the DS2433 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2433 will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the device will leave the read data time slot unchanged.

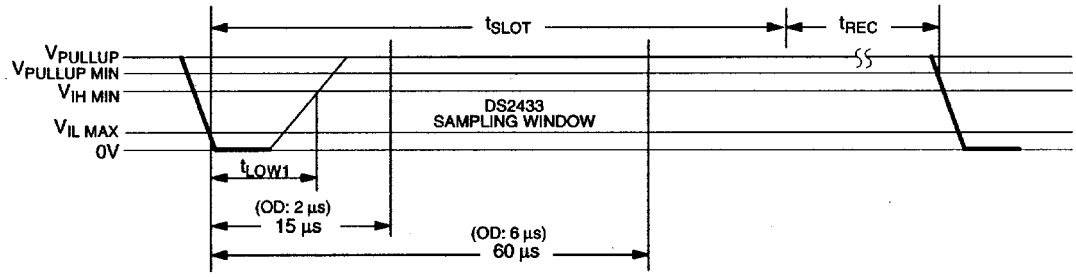
Figure 10. INITIALIZATION PROCEDURE RESET AND PRESENCE PULSES



*In order not to mask interrupt signalling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960µs.
** Includes recovery time.

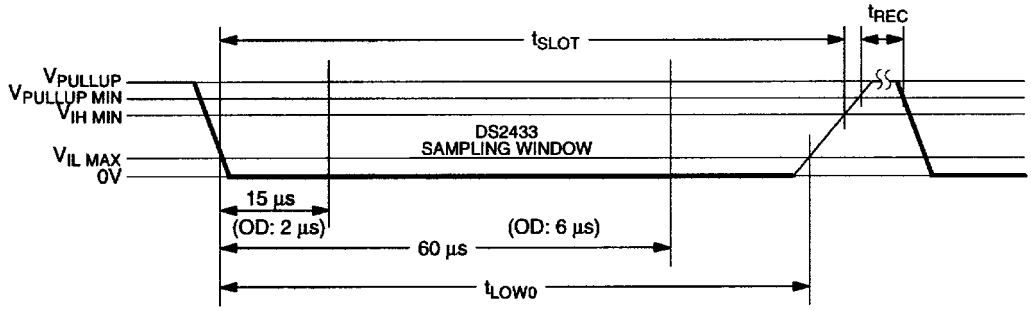
Figure 11. READ/WRITE TIMING DIAGRAM

Write-one Time Slot



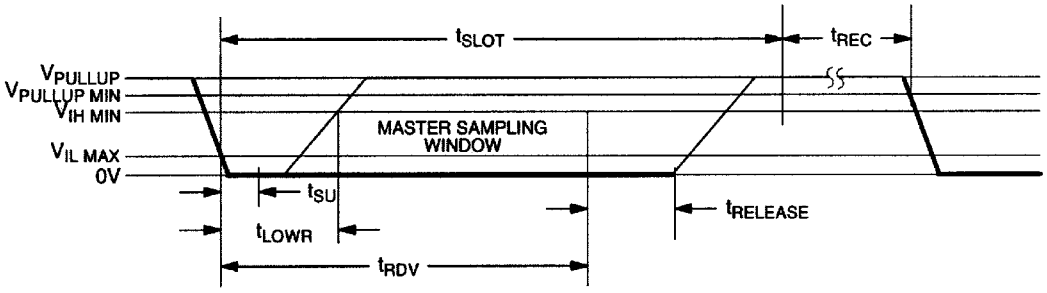
Regular Speed	Overdrive Speed
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1 µs ≤ t_{LOW1} < 15 µs	1 µs ≤ t_{LOW1} < 2 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞

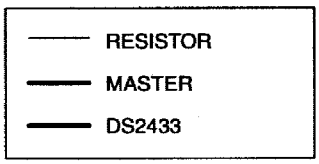
Write-zero Time Slot



Regular Speed	Overdrive Speed
60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs	6 µs ≤ t_{LOW0} < t_{SLOT} < 16 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞

Read-data Time Slot





Regular Speed	Overdrive Speed
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1 µs ≤ t_{LOWR} < 15 µs	1 µs ≤ t_{LOWR} < 2 µs
0 ≤ $t_{RELEASE}$ < 45 µs	0 ≤ $t_{RELEASE}$ < 4 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs	t_{RDV} = 2 µs
t_{SU} < 1 µs	t_{SU} < 1 µs

CRC GENERATION

With the DS2433 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS2433 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8+ X^5+ X^4+ 1$. This 8-bit CRC is received in the true (non-inverted) form when reading the ROM of the DS2433. It is computed at the factory and lasered into the ROM.

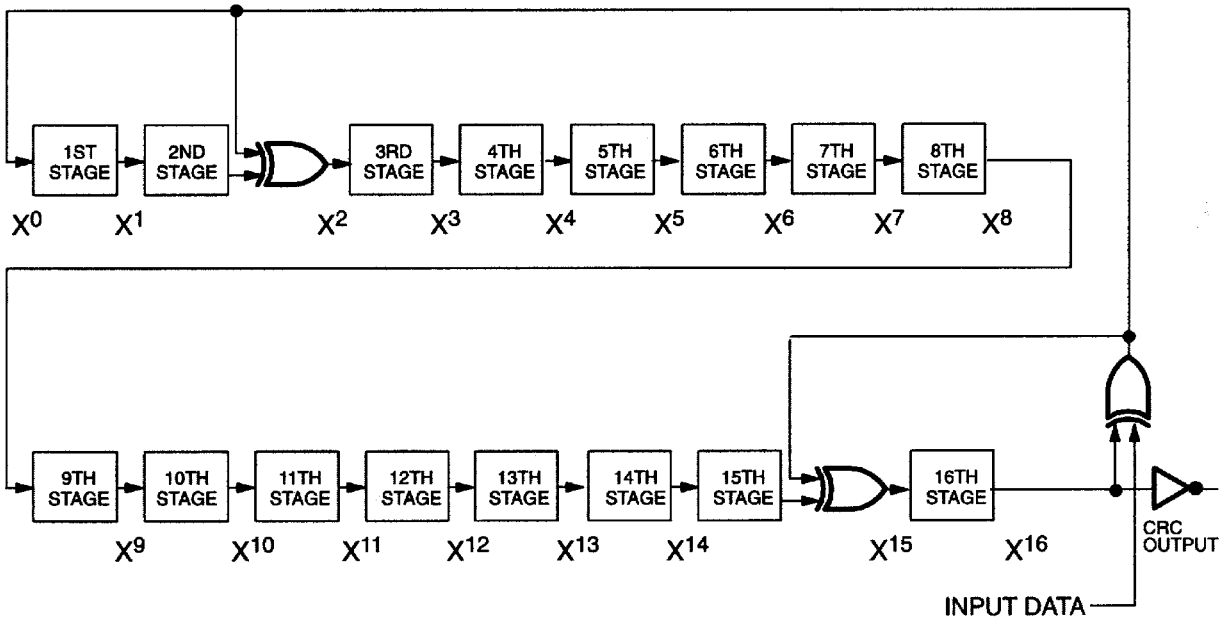
The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function $x^{16}+ x^{15}+x^2+ 1$. This CRC is used for fast verification of a data transfer when writing to the scratchpad. It is the same type of CRC as is used with NV RAM based iButtons for error detection within the iButton Extended File Structure. In contrast to the 8-bit CRC, the 16-bit CRC is always returned or sent in the complemented (inverted) form. A CRC-generator inside the DS2433 chip (Figure 12) will calculate a new 16-bit CRC as shown in the command flow chart of Figure 7. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation.

With the Write Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2 and all the data bytes. The DS2433 will transmit this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data may start at any location within the scratchpad.

For more details on generating CRC values including example implementations in both hardware and software, see the *Book of DS19xx iButton Standards.*

Figure 12. CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL

(Polynomial $X^{16}+ X^{15}+ X^2+ 1$)



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STC-020A Specification

** This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

DC ELECTRICAL CHARACTERISTICS (V_{PUP} =2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 8
Logic 0	V_{IL}	-0.3		+0.8	V	1, 9
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Programming Current	I_{LPROG}		500		µA	10

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

ENDURANCE (V_{PUP} = 5.0V; T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write/Erase Cycles	N_{CYCLE}	50k			——	11

AC ELECTRICAL CHARACTERISTICS
REGULAR SPEED (V_{PUP} = 2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	13
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	13
Read Data Valid	t_{RDV}		15		µs	12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	7
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	

AC ELECTRICAL CHARACTERISTICS

OVERDRIVE SPEED (V_{PUP} = 2.8V to 6.0V;-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	13
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	13
Read Data Valid	t_{RDV}		2		µs	12
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	4
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDHIGH}	2		6	µs	
Presence Detect Low	t_{PDLOW}	8		24	µs	

NOTES:

1) All voltages are referenced to ground.

2) V_{PUP} = external pullup voltage.

3) Input load is to ground.

4) An additional reset or communication sequence cannot begin until the reset high time has expired.

5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

6) Capacitance on the data pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied the parasite capacitance will not affect normal communications.

7) The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

8) V_{IH} is a function of the external pullup resistor and V_{PUP}.

9) Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.

10) The Copy Scratchpad takes 5ms maximum during which the voltage on the 1-Wire bus must not fall below 2.8V.

11) During the execution of the Copy Scratchpad command the DS2433 automatically erases the memory locations to be written to. No extra steps need to be taken by the bus master.

12) The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a read-one time slot, this maximizes the amount of time for