Rev 0; 5/05

DALLAS SEMICONDUCTOR MAXIM

Full Laser Control with Fault Management

General Description

The DS1861 is a laser-driver control IC designed to reduce the production cost of fiber optics circuits by eliminating multiple temperature tests. It works with nearly all laser-driver ICs to provide automatic power control (APC) and automatic extinction ratio control (AERC), which improves the performance of the system over temperature and aging. It also has built-in monitoring capability to provide early fault detection, which can be configured to latch the IC into a shutdown condition. Settings programmed into the DS1861 are stored in password-protected EEPROM memory, which write-protects calibration data. Programming is accomplished through an I²C-compatible interface, which can also be used to read diagnostic information.

Features

- ♦ Automatic Power Control (APC)
- ♦ Automatic Extinction Ratio Control (AERC) Across Temperature and Laser Aging
- ♦ Works in AC-Coupled Laser Systems
- ♦ Configurable Latched Automatic Shutdown with Tx-Fault and Tx-Disable
- ♦ Programmable Fast Alarm Conditions
- ♦ I²C-Compatible Serial Interface Allows Up to Eight Devices on the Same Serial Bus
- ♦ Operates Over Wide Supply-Voltage Range
- ♦ Nonvolatile Memory for Device Settings
- ♦ Small, 14-Pin TSSOP Package
- ♦ -40°C to +95°C Operating Temperature Range

Applications

Optical Transceivers

Optical Transponders

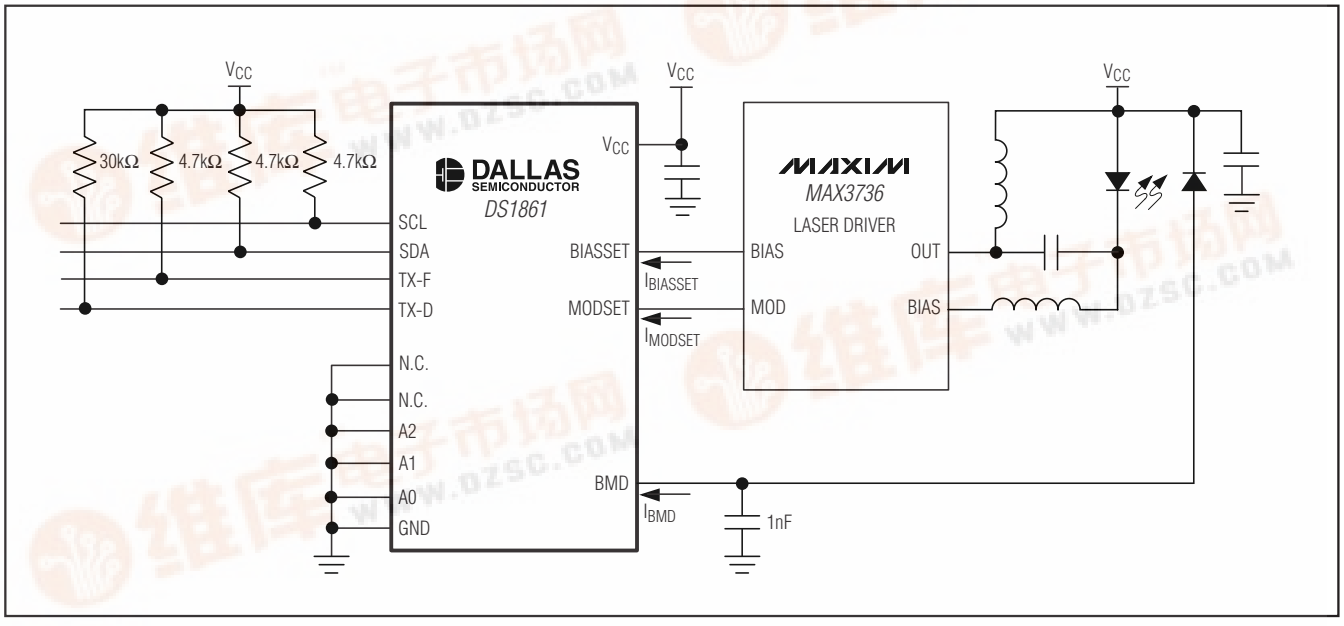
Pin Configuration appears at end of data sheet.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1861E	-40°C to +95°C	14 TSSOP (173 mils)
DS1861E+	-40°C to +95°C	14 TSSOP (173 mils)

+Denotes lead free.

Typical Operating Circuit



Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Full Laser Control with Fault Management

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, SDA, and SCL Pins Relative to Ground.....-0.5V to +6.0V
Voltage Range on A_0, A_1, A_2, Tx-Fault, Tx-Disable, BIASSET, MODSET, and BMD Relative to Ground.....-0.5V to (V_{CC} + 0.5V), not to exceed +6.0V
Operating Temperature Range .....-40°C to +95°C
EEPROM Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.85		5.50	V
Input Logic 1 (SDA, SCL, A_2, A_1, A_0)	V_{IH1}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL, A_2, A_1, A_0)	V_{IL1}		-0.3		+0.3 x V_{CC}	V
Input Logic 1 (TX-D)	V_{IH2}		1.5			V
Input Logic 0 (TX-D)	V_{IL2}				0.9	V
Voltage at BIASSET and MODSET			0.6		3.0	V
I_{TH}/I_{APC} Ratio		(Note 2)			7:1	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 3)		5	7	mA
Input Leakage	I_{LI}		-1		+1	µA
Output Leakage (TX-F, SDA)	I_{LO}	High impedance	-1		+1	µA
Low-Level Output Voltage (TX-F, SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	
I/O Capacitance	$C_{I/O}$				10	pF
Input Current Each I/O Pin		0.4 < $V_{I/O}$ < 0.9 x V_{DD}	-10		+10	µA

ANALOG OUTPUT CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V; T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIASSET Current Range	$I_{BIASSET}$		0.01		1.50	mA
BIASSET Shutdown Current				10	100	nA
MODSET Current Range	I_{MODSET}		0.01		1.20	mA
MODSET Shutdown Current				10	100	nA
APC Calibration Accuracy (Error in Setting I_{BMD})		(Note 4)			3	%
APC Temp Drift (% Drift in I_{BMD})		(Note 5)		±2	±4	%
N Temp Drift		40µA < I_{MODSET} < 100µA at +25°C (Note 6)		±1	±4	%
		100µA < I_{MODSET} < 400µA at +25°C (Note 6)		±1	±3	
		I_{MODSET} > 400µA at +25°C (Note 6)		±1	±2.75	
Extinction Ratio Calibration Accuracy		At 10dB extinction ratio			0.22	dB
Loop Transient Settling Error		$I_{BIASSET}$ and I_{MODSET} after 300ms			3	%
Extinction Ratio Update Frequency	f_{ERU}		5		25	Hz
Peak BMD Disturbance Current	I_{DIST}	Percent increase above I_{BMD}		3.33	3.60	%

ANALOG INPUT CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BMD Current—Source or Sink (±)	I_{SET}	(Note 7)		0.05		1.50	mA
BMD Voltage	V_{BMD}	I_{BMD} = 0.5x to 2x I_{SET}		1.0	1.24	1.5	V
BMD Input Resistance	R_{BMD}	I_{BMD} = I_{SET} ±10% (I_{SET})	Gain = 16	175	265	350	Ω
			Gain = 8	350	530	700	
			Gain = 4	700	1060	1400	
			Gain = 2	1400	2120	2800	
			Gain = 1	2800	4240	5600	
Reference Voltage	V_{REF}				1.24		V

FAST ALARMS AND V_{CC} MONITOR CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Bias Alarm LSB		255 settings (includes off)		8.2		µA
High Bias Alarm Threshold Accuracy		High bias settings > 100µA			10	%
LTXP Alarm Threshold Multiplier (I_{SET} Multiplier Shown, Note 8)		**LTXP_Thres (bin)**				mA/mA
		XXXXX000		LTXP Alarm OFF		
		XXXXX001		Do not use		
		XXXXX010		0.81		
		XXXXX011		0.76		
		XXXXX100		0.54		
		XXXXX101		0.41		
		XXXXX110		0.28		
		XXXXX111		0.14		
HTXP Alarm Threshold Multiplier (I_{SET} Multiplier Shown, Note 8)		**HTXP_Thres (bin)**				mA/mA
		XXXXX000		HTXP Alarm OFF		
		XXXXX001		Do not use		
		XXXXX010		1.30		
		XXXXX011		1.43		
		XXXXX100		1.56		
		XXXXX101		1.69		
		XXXXX110		1.82		
		XXXXX111		1.95		
V_{CC} Power Good	V_{POA}		2.15		2.70	V
Vcc Fault Deassert Delay	t_{POAR}		360		700	µs
Digital Power-On Reset Voltage	V_{POD}		1.0		2.2	V

I^2C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Figure 14)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 9)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs

I²C AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Figure 14)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 10)			400	pF
EEPROM Write Time	t_W	(Note 11)		10	20	ms

POWER-SUPPLY AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Slew Rate	dV/dt ↑ Vcc	V_{CC} = 0 to 5.5 (Note 12)			30	V/ms

SHUTDOWN AND FAULT AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIASSET and MODSET Disable (10% of Active Level)	t_{OFF}	From rising edge of TX-D			5	µs
APC Recovery From Normal Disable (to I_{BMD} 90% Level)	$t_{ON:B}$	From falling edge of TX-D (Note 13)			0.8	ms
Modulation Recovery From Normal Disable (to $I_{MODDRIVER}$ 90% Level)	$t_{ON:M}$	From falling edge of TX-D (Note 14)			0.2	ms
APC Recovery After Power-Up or Shutdown (to I_{BMD} 90% Level)	$t_{INIT:B}$	(Note 13)			0.8	ms
Modulation Recovery After Power-Up or Shutdown (to $I_{MODDRIVER}$ 90% Level)	$t_{INIT:M}$				100	ms
Fault Reset Time (to TX-Fault = 0)	$t_{INIT:F}$		100		150	ms
Shutdown Time (to 10% $I_{BIASSET}$, 10% I_{MODSET}, TX-F High)	t_{FAULT}	I_{BMD} > HTXP Threshold, or I_{BIAS} ≥ HBIAS Threshold, or I_{BMD} < LTXP Threshold			50	µs
Minimum Reset Pulse Width	t_{RESET}		1			µs

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to 5.5V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Writes		+70°C (Note 15)	50,000			

Note 1: All voltages are referenced to ground. Currents into the IC are positive, out of the IC negative.

Note 2: The threshold current (I_{TH}) to light producing current (I_{APC}) ratio should remain below 7:1. This limits overshoot to under 10% and ensures the data sheet accuracies are met.

Note 3: Max I_{CC} is dependent on SCL clock rates.

Note 4: Calibration accuracy refers to the accuracy achieved at the end of calibration.

Note 5: This specification refers to the error contribution due to this chip, and does not include the error due to the drift of the monitor-diode responsivity with temperature.

Note 6: The N Temperature Drift specification includes error caused by changes in modulation current due to system temperature variation. After the part is calibrated at +25°C, this spec allows for modulation current changes of up to +65% with increasing temperature and -25% with decreasing temperature. Larger modulation current variations would have increased drift, but this range accommodates a reasonable change (up to 2x across temperature) in laser diode slope efficiency. Calibration is assumed to take place at +25°C for the purposes of this spec. This does not imply that the system must be calibrated at +25°C.

Note 7: Within the APC calibration accuracy.

Note 8: Values in the table are multiplied times the I_{BMD} set point (set by APC register) to determine the threshold limits.

Note 9: I^2C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I^2C standard-mode timing.

Note 10: C_B—total capacitance of one bus line in pF.

Note 11: EEPROM write begins after a stop condition occurs.

Note 12: If the supply ramps up at slew rates within the specification, the device will be functional after V_{CC} exceeds V_{POA} and the power-up time (t_{POAR}) elapses.

Note 13: On power-up and when TX-D is deasserted, IBIASSET ramps up from zero current to its final value with ≤10% APC overshoot during the transient.

Note 14: Modulation is applied at the level it was at before disable. If the time from disable is so long that the laser has cooled down, then meeting ER accuracy is contingent upon completion of the first ER update. The MODLOAD enable bit and MODLOAD register can be used to load a predetermined I_{MODSET} value if desired. See the *Detailed Register Descriptions* section for more information.

Note 15: This parameter is guaranteed by design.

Timing Diagrams

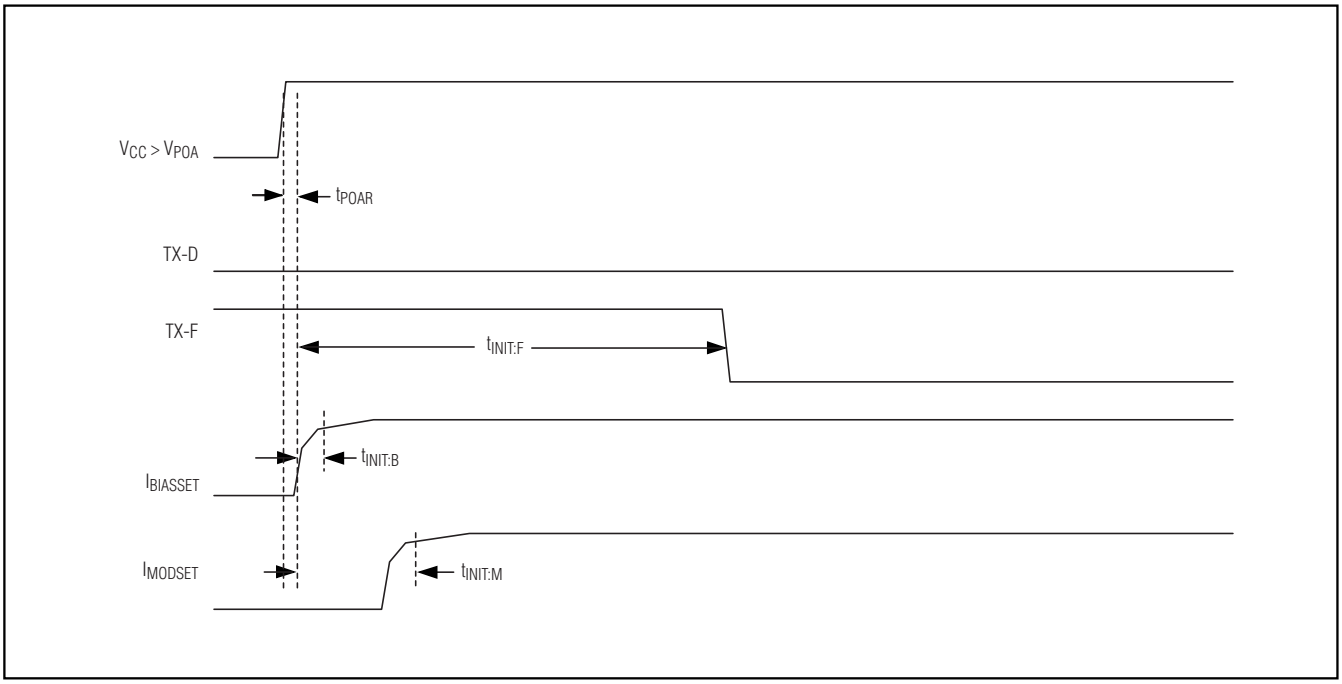


Figure 1. Power-Up Timing with TX-D Not Asserted (Including Hotplug)

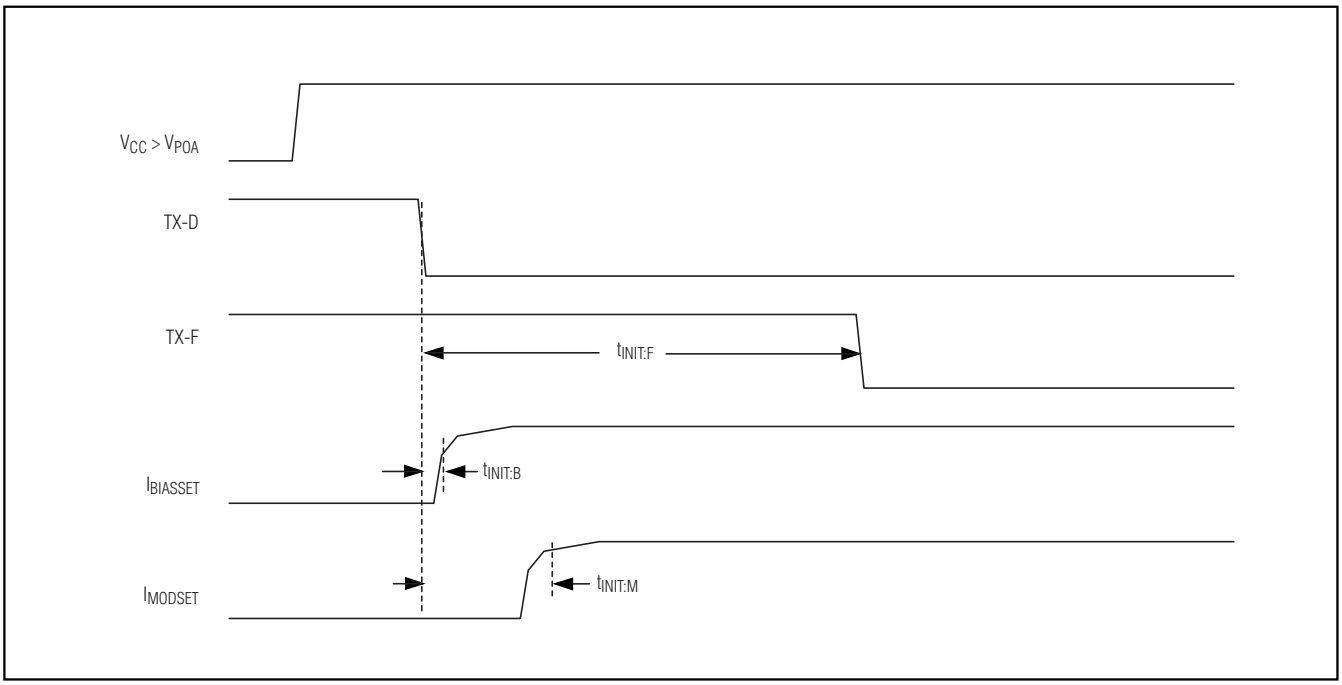


Figure 2. Power-Up Timing with TX-D Asserted

Timing Diagrams (continued)

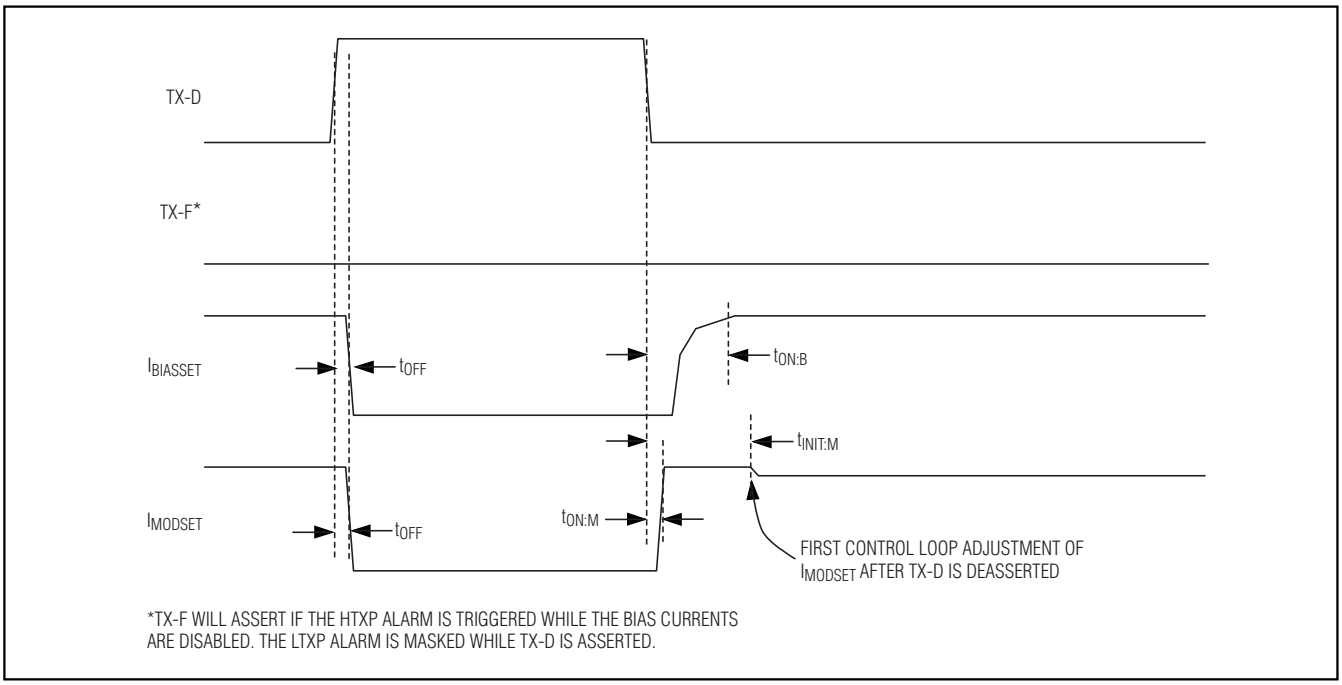


Figure 3. TX-D Timing During Normal Operation

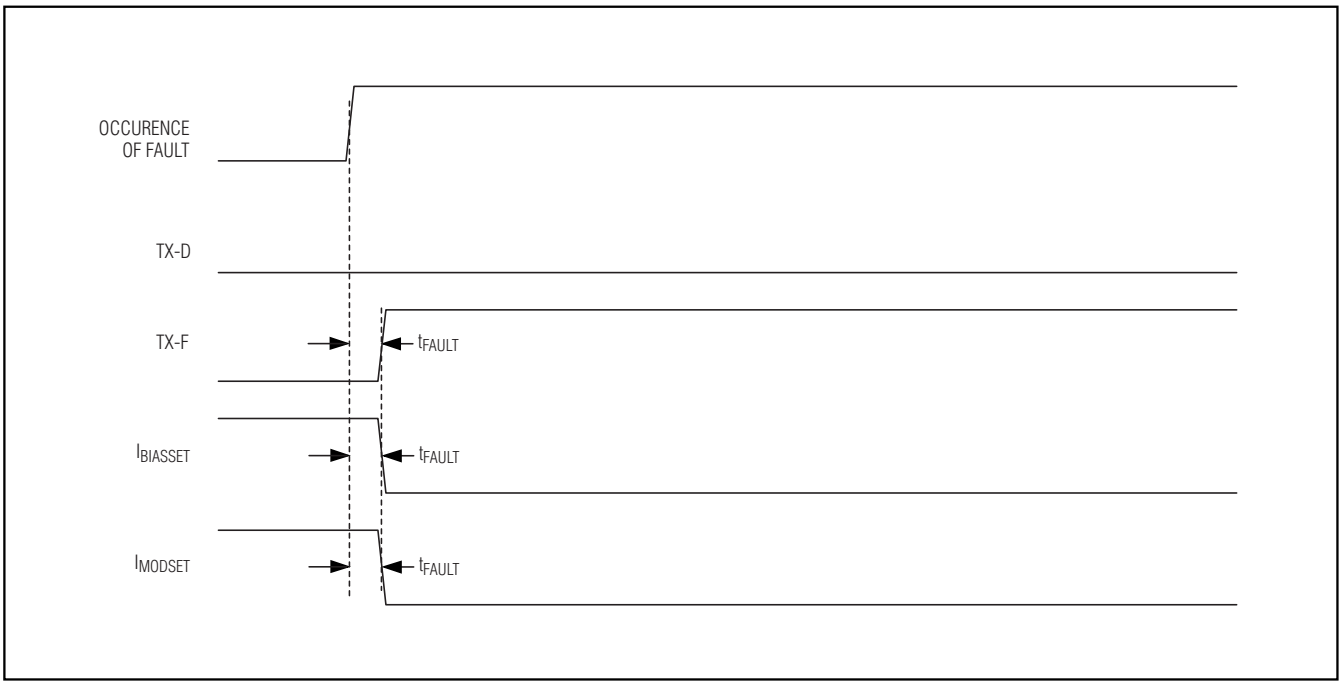


Figure 4. Detection of Transmitter Safety Fault Condition

Timing Diagrams (continued)

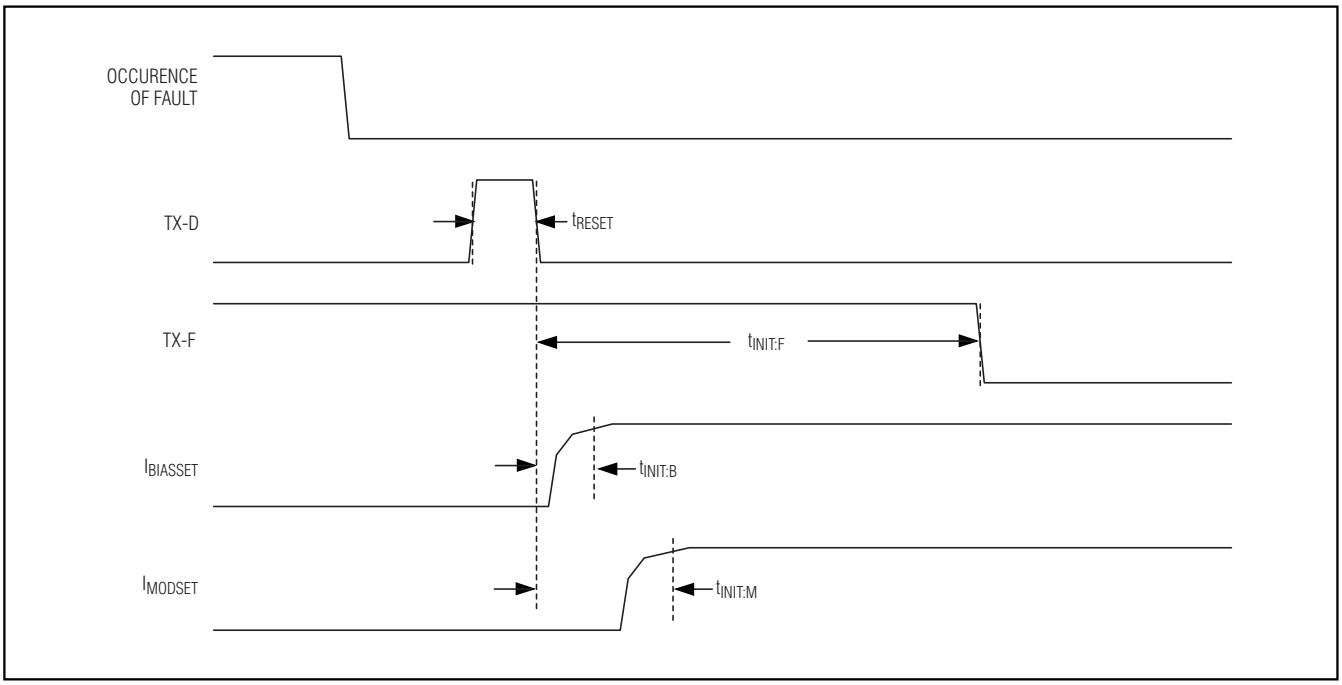


Figure 5. Successful Recovery from Transmitter Safety Fault Condition

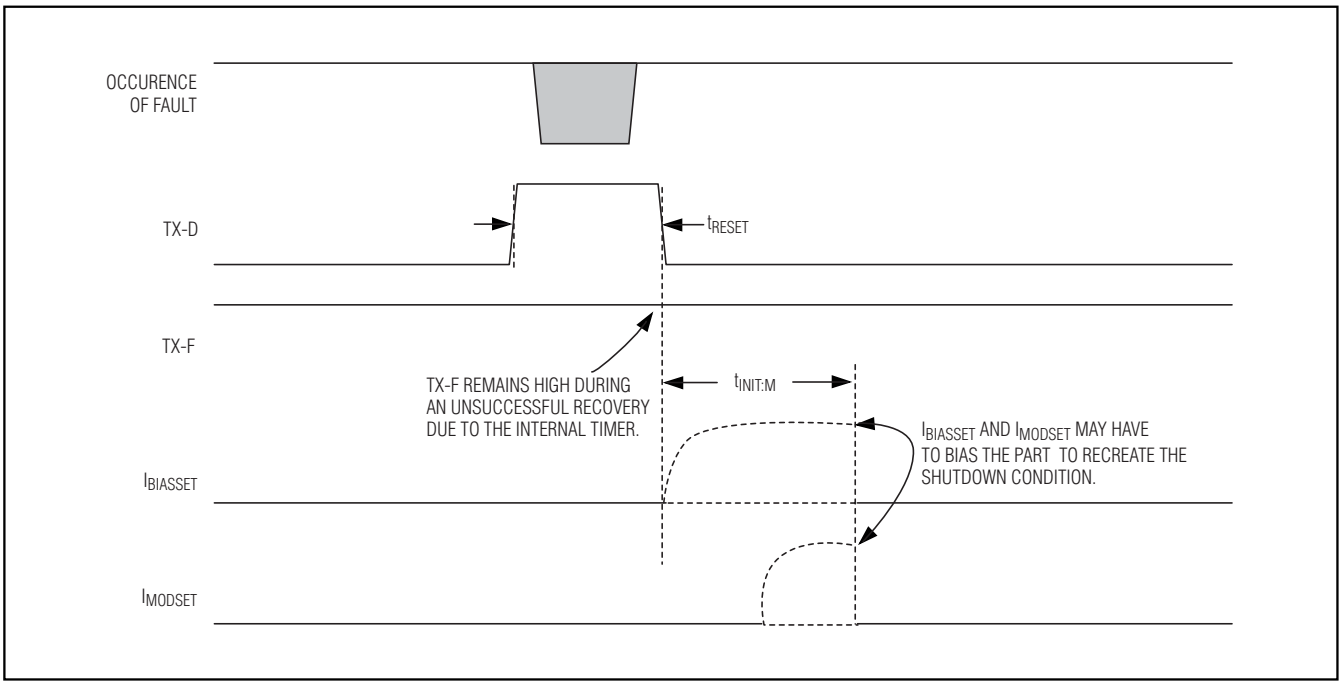


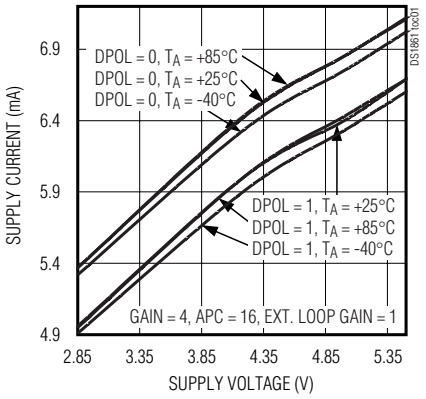
Figure 6. Unsuccessful Recovery from Transmitter Safety Fault Condition

Full Laser Control with Fault Management

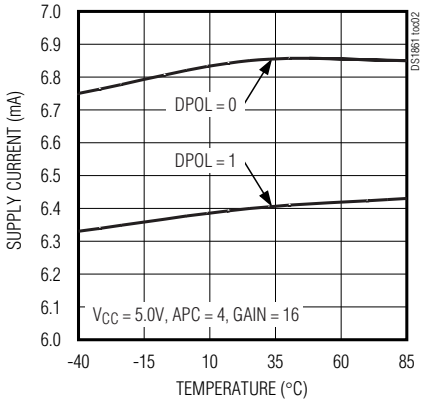
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

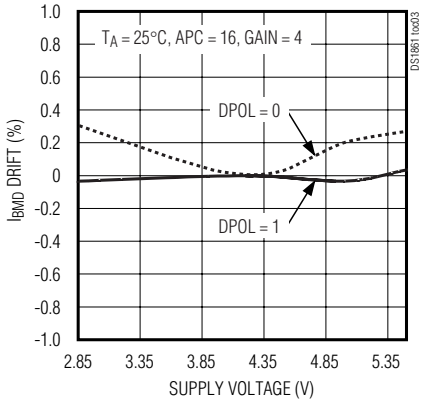
SUPPLY CURRENT vs. SUPPLY VOLTAGE



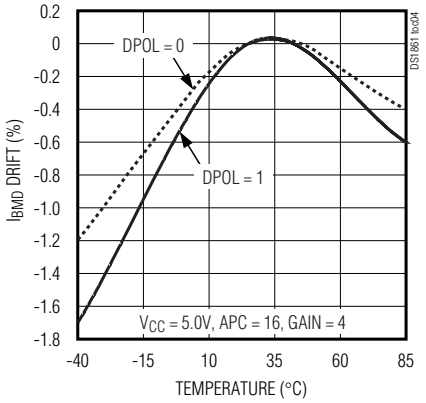
SUPPLY CURRENT vs. TEMPERATURE



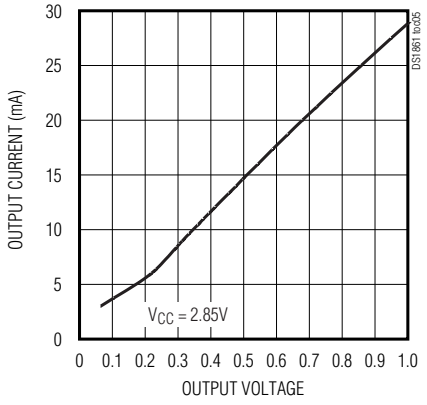
I_{BMD} DRIFT vs. SUPPLY VOLTAGE



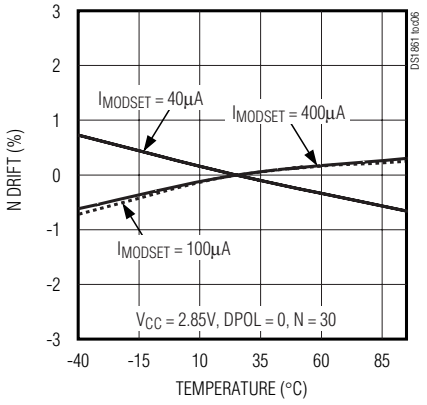
I_{BMD} DRIFT vs. TEMPERATURE



TX-F OUTPUT CURRENT vs. OUTPUT VOLTAGE



N DRIFT vs. TEMPERATURE

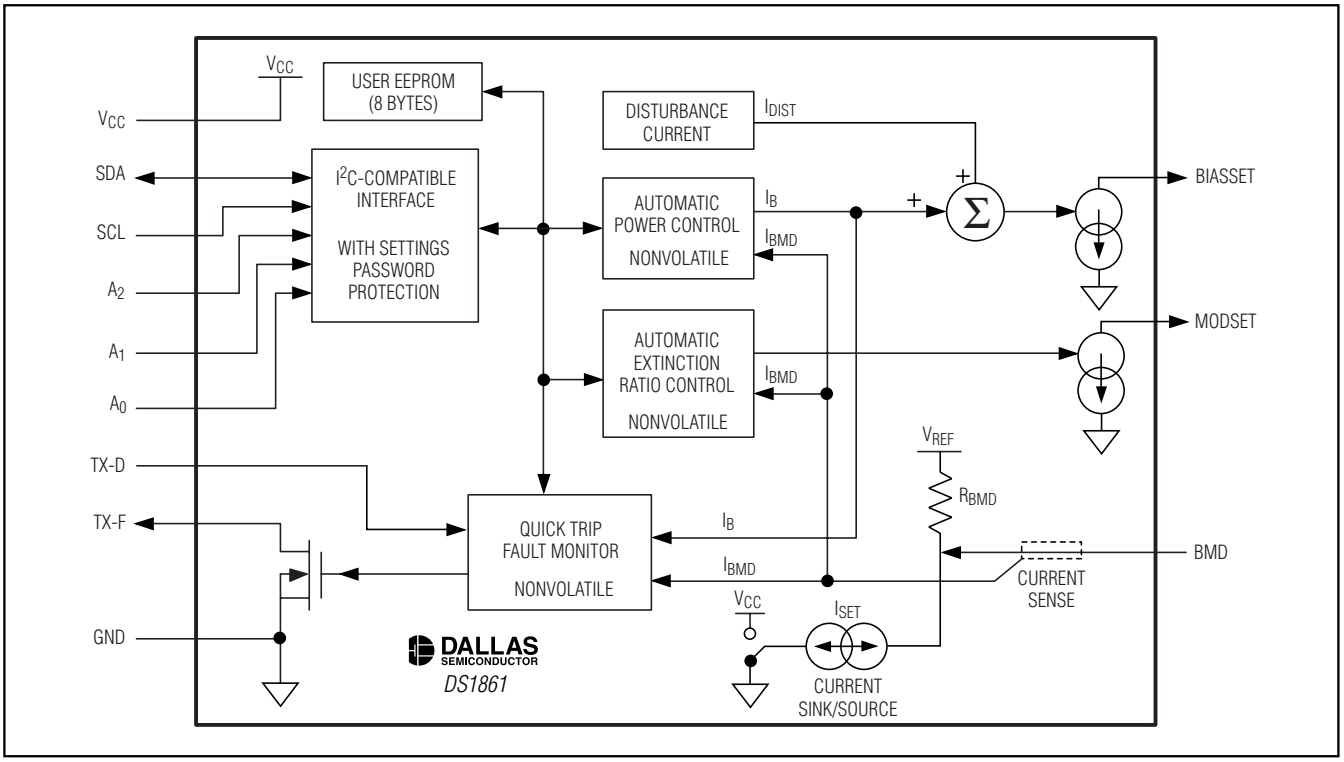


Pin Description

PIN	NAME	FUNCTION
1	SDA	Serial Data Input/Output. I^2C bidirectional data pin, which requires a pullup resistor to realize high logic levels.
2	SCL	Serial Clock Input. I^2C clock input.
3	TX-F	Transmit Fault Output. Open-collector output that indicates an alarm condition has occurred. A pullup resistor is required on this pin to realize high logic levels.
4	TX-D	Transmit Disable Input
5, 8	N.C.	No Connection
6	BMD	Photodiode Current Input
7	GND	Ground
9	BIASSET	Bias Current Output
10	A_0	I^2C Address Inputs. These inputs determine the slave address of the device. The slave address in binary is $1010A_2A_1A_0$.
11	A_1	
12	A_2	
13	MODSET	Modulation Current Ouput
14	V_{CC}	Power Supply

Full Laser Control with Fault Management

Functional Diagram



Detailed Description

Automatic Power Control

The DS1861 APC is accomplished by adjusting the bias current (I_{BIAS}) until the feedback current (I_{BMD}) from a photodiode matches the value determined by the APC register. The relationship between the APC register and I_{BMD} is given by:

$$I_{SET} = 1.525\mu A \text{ Gain (APC<4:0> + 32)}$$

where APC<4:0> is the numerical value determined by the five least significant bits of the APC register, and the gain value is determined by the upper three bits of the APC register, as shown in the truth table below. See Figure 7 for a graph of the BMD current-set point vs. the APC register value.

APC<7:5>	GAIN
000	1
001	2
010	4
011	8
1xx	16

The BMD pin appears to the photodiode as a voltage source (V_{REF}) with an output resistance equal to R_{BMD} in parallel with a current source (I_{SET}) equal to the I_{BMD} setpoint. When the control loop is at its steady state value, the voltage at the BMD pin (V_{BMD}) is equal to V_{REF}, and the BMD current will all be sourced by I_{SET}. When an imbalance causes the feedback current to differ from the set current, the difference in the currents causes the DS1861 to adjust the BIASSET and the MODSET currents to new settings so the input current matches the set current. During transient periods, the difference in the I_{SET} and I_{BMD} currents causes a small current to pass through R_{BMD}. This causes a slight increase or decrease in the V_{BMD} voltage. The current source can sink and source current, which must be configured using the DPOL bit in the control byte for proper operation. This allows the photodiode to be referenced to either V_{CC} or GND. See the *Memory Map* and *Detailed Register Descriptions* sections for more detail.

Reading the BIASSET and MODSET Registers

The $I_{BIASSET}$ and I_{MODSET} currents are generated by embedded 18-bit and 12-bit DACs, respectively, and their output currents can be read when the DS1861 has been halted using the halt bit, and the password has been entered. See the *Detailed Register Descriptions* section for information on calculating the output current from the register's value.

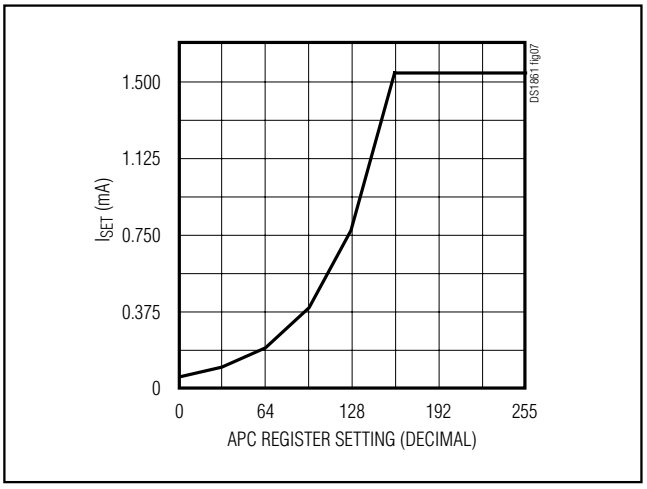


Figure 7. BMD Current Setpoint vs. APC Register Setting

Automatic Extinction Ratio Control

The DS1861 injects a small disturbance current to measure the gain (light/mA) of the laser driver and laser diode pairing. This control methodology makes the extinction ratio insensitive to changes in the photodiode's responsivity due to temperature and aging effects, as long as the ratio of the laser driver's bias current gain (A_D) and modulation current gain (A_M) remains constant (Figure 8).

The disturbance current is automatically scaled as the BMD current-set point is adjusted, so the peak disturbance current always increases I_{BMD} by approximately 3.3%. See Figure 9 for details.

To understand how the MODSET and BIASSET currents control the extinction ratio, the extinction ratio equation (extinction ratio = P1/P0) must first be expressed in terms of the modulation power (P_{MOD}) and average power (P_{AVG}). Figure 10 shows the current and power levels that correspond to the optical logic 1 (P1) and logic 0 (P0) levels.

$$\text{Extinction Ratio} = \frac{P_1}{P_0} = \frac{P_{AVG} + \frac{1}{2}P_{MOD}}{P_{AVG} - \frac{1}{2}P_{MOD}}$$

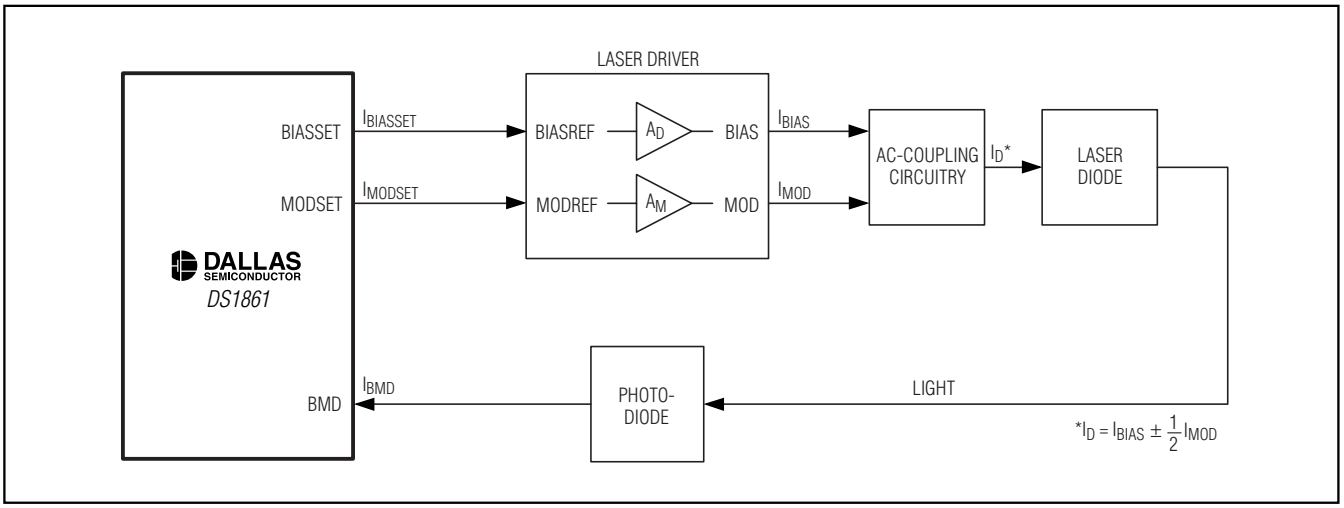


Figure 8. AERC Block Diagram

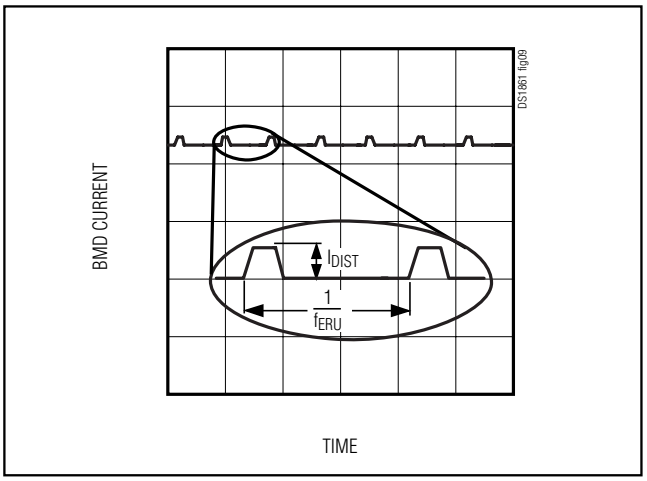


Figure 9. BMD Disturbance Current

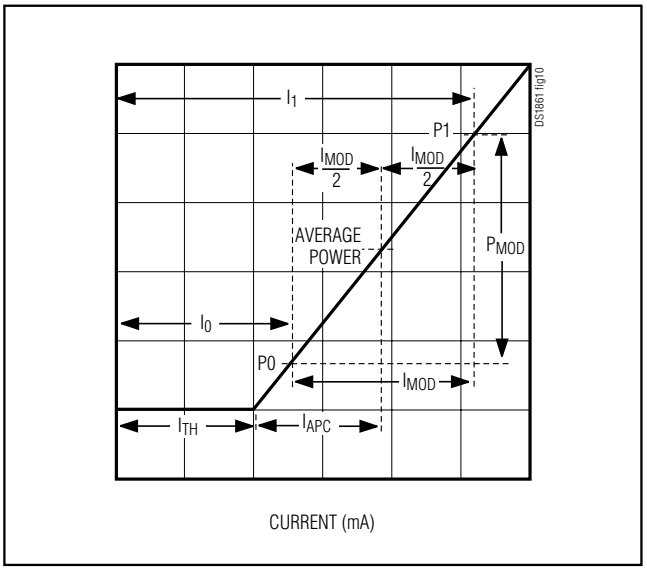


Figure 10. Laser Diode Bias Current Definitions

Once the extinction ratio is expressed as a function of the average power and the modulation power, the equation can then be written in terms of the modulation and average power currents. The modulation current (I_{MOD}) is defined as the difference between the I_1 and I_0 currents ($I_{MOD} = I_1 - I_0$). The average power current (I_{APC}) is the arithmetic mean of the I_1 and I_0 currents referenced to the threshold current ($I_{APC} = 1/2\ I_1 + 1/2\ I_0 - I_{TH}$). After defining these currents, the equation can now be rewritten as the following equations.

$$\text{Extinction Ratio} = \frac{I_{APC} + \frac{1}{2} I_{MOD}}{I_{APC} - \frac{1}{2} I_{MOD}} = \frac{1 + \frac{1}{2} \times \frac{I_{MOD}}{I_{APC}}}{1 - \frac{1}{2} \times \frac{I_{MOD}}{I_{APC}}}$$

The APC loop is already controlling I_{APC} to keep the average power at a constant value, so the DS1861 outputs I_{MODSET} so that I_{MOD}/I_{APC} remains constant to control the extinction ratio. The DS1861 determines the I_{MOD}/I_{APC} ratio according to the following formula, where N is a variable gain that can be used to adjust the extinction ratio.

$$\frac{I_{MOD}}{I_{APC}} = \frac{N}{30} \times \frac{A_M}{A_D}$$

Substituting into the previous extinction ratio equation yields the extinction ratio as a function of N.

$$\text{Extinction Ratio} = \frac{1 + \frac{1}{2} \times \frac{N}{30} \times \frac{A_M}{A_D}}{1 - \frac{1}{2} \times \frac{N}{30} \times \frac{A_M}{A_D}} = \frac{60 + N\frac{A_M}{A_D}}{60 - N\frac{A_M}{A_D}}$$

Figure 11 shows the extinction ratios (expressed in decibels) as a function of N for several A_M/A_D ratios.

Note the actual extinction ratio value is determined by the ratio A_M/A_D in addition to N. If the A_M/A_D ratio varies due to voltage, temperature, or aging effects, it becomes an additional error source when determining the overall extinction ratio variance. The DS1861 is meant to be used with a monolithic laser driver, where A_M and A_D are generated on the same chip, so changes in the ratio of A_M to A_D are minimal.

The N value itself is determined by the extinction ratio register. There are two components of the ER register used to calculate N. The range select bit (RSEL), which selects the high (RSEL = 1) or low (RSEL = 0) range of N, is the MSB of the register. The lower seven bits of the register (ER<6:0>) determine the value of N within the selected range. The value of N is given by:

$$N = \begin{cases} \dfrac{ER<6:0>+32}{2} & \text{when RSEL} = 0 \\ ER<6:0>+32 & \text{when RSEL} = 1 \end{cases}$$

The ER<6:0> value should be programmed to values between 28 and 104 (decimal), regardless if the high or low range is selected, to ensure that the N value remains accurate and constant as intended. These limits allow the N values of the high and low range to overlap to ensure that all N values can be attained, but prevents potential errors that can be caused by using the extremes of each RSEL range. Figure 12 shows the N values as a function of the ER register setting.

The Convergence Algorithm and Overshoot Control

The DS1861 uses a tiered slew-rate control system that adjusts the DAC update rate and the number of LSBs it increases/decreases per update cycle when the control loop is seeking to converge to its steady state value. For the APC loop, it makes its decision on the required convergence rate based on the percent error between the present BMD current and the BMD current-set point. The modulation current slew rate is adjusted based solely on the difference between its present code and the code-set point that is determined by the AERC circuitry. Both update rates are designed to prevent any overshoot during large set-point changes in excess of 10%, which assumes (see the following) the ratio of the laser diode's threshold current (I_{TH}) to the average power current (I_{APC}) is below 7:1. Most systems do not exhibit any overshoot when using the DS1861.

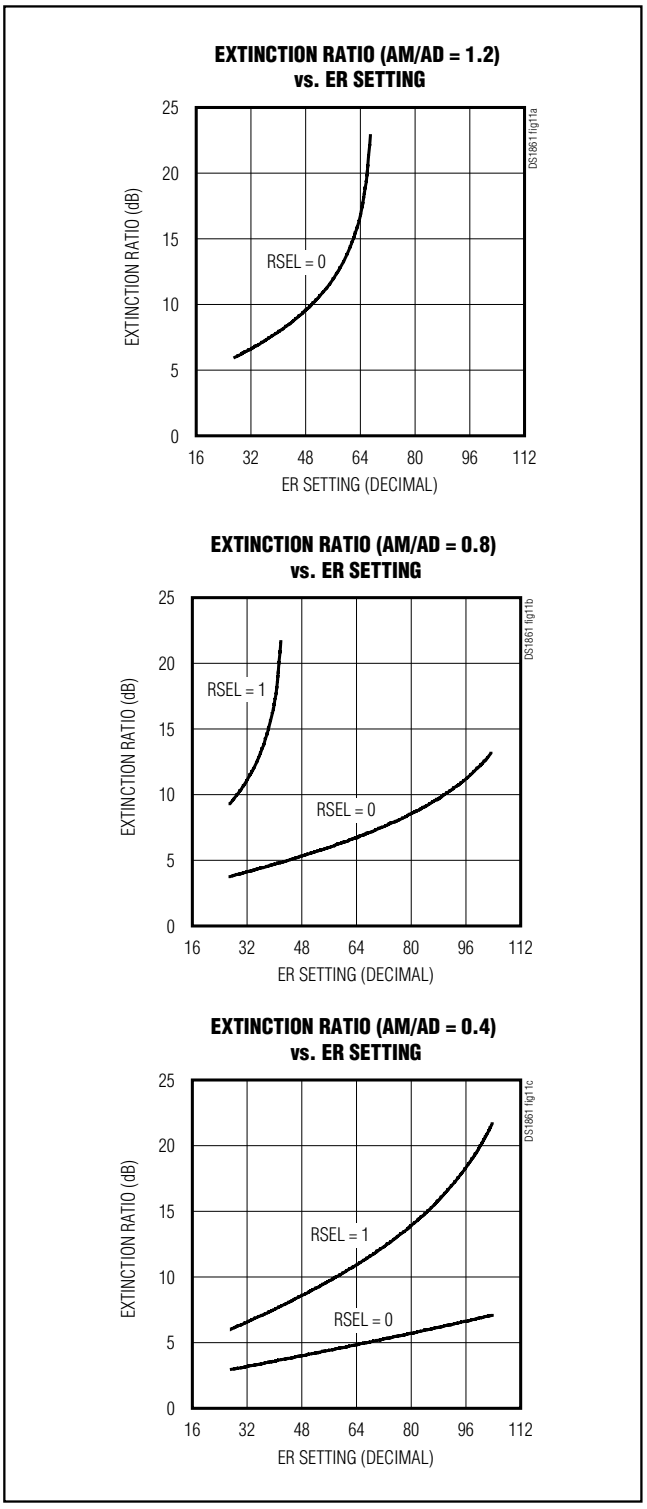


Figure 11. Typical Extinction Ratios vs. N Codes

Full Laser Control with Fault Management

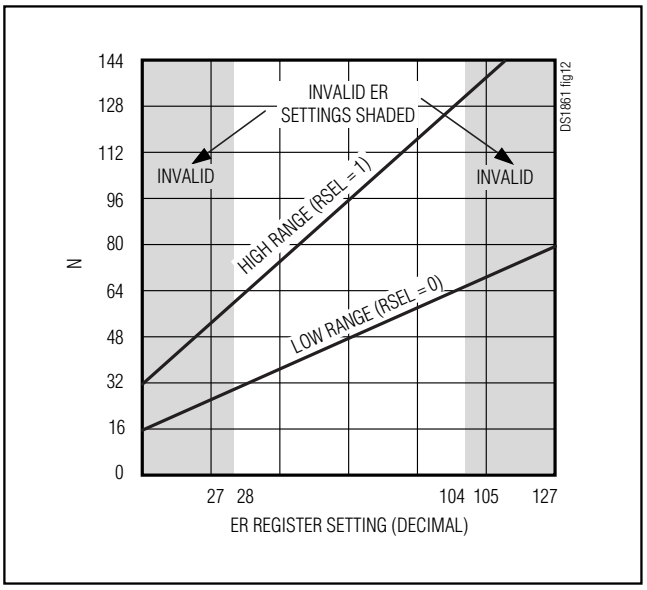


Figure 12. Setting N Using the ER Register

The average power current is defined as the difference between the current required to reach the average power output and the threshold current of the laser diode. The average power output is defined as the mean of the power used to transmit a high logic level (P1) and the power used to transmit a low power level (P0). Figure 10 graphically shows the threshold and average power currents as they relate to the light output of a laser diode.

Fault Monitors and Shutdown

The DS1861 has a V_{CC} monitor plus three programmable quick-trip (QT) fault monitors (Figure 13) that can trigger the TX-F output. The QTs monitor for high transmit power (HTXP), low transmit power (LTXP), and for high bias current (HBIAS). All the QTs feature programmable trip levels, an alarm disable, and a shutdown enable to determine if the enabled QT alarm shuts off the $I_{BIASSET}$ and I_{MODSET} outputs.

V_{CC} is monitored against two internal voltage levels to ensure that V_{CC} is at an adequate level for the part to

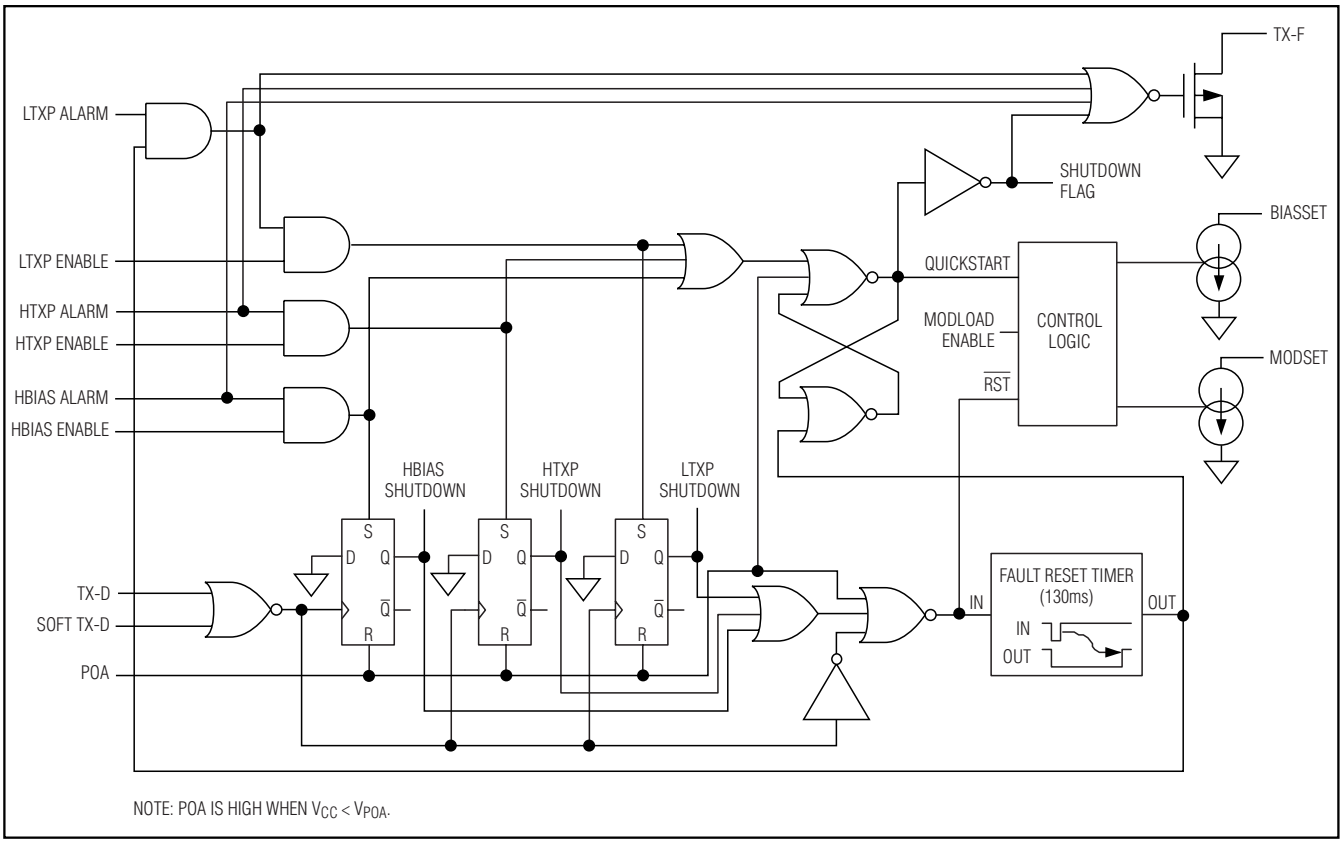


Figure 13. Quick Trip Logic Diagram

communicate over the I²C bus and for the analog circuitry to function properly. The first monitoring level, the power-on digital voltage (V_{POD}), inhibits the part's I²C functionality when V_{CC} is below V_{POD}. The second monitoring level is the power-on analog voltage (V_{POA}). The DS1861 disables $I_{BIASSET}$ and I_{MODSET} and asserts the TX-F output whenever V_{CC} is below V_{POA}. Both V_{CC} monitors are nonmaskable, so there is no way to force the chip to function when V_{CC} is not at an adequate level to assure the DS1861 operates properly.

The high and low transmit power quick-trip thresholds are each programmed by 3 bits that select one of seven different levels as a function of the expected I_{BMD} current. Each QT monitor can be disabled by programming all three bits to zero. Disabling a QT by programming its control bits to zero prevents the QT alarm flags from ever being set, which consequently prevents that monitor from asserting the TX-F output, latching the device into a shutdown condition, or setting the alarm bits in the Status register. The HTXP and LTXP enable bits can be used to prevent the transmit power level QTs from causing shutdown while allowing the TX-F output to be set to flag the system of a transmit power fault condition. Figure 13 shows the shutdown logic. Tables 1 and 2 show the QT thresholds as a function of I_{BMD} current-set point.

The high-bias, quick-trip alarm features an 8-bit threshold setting with an LSB of 8.2µA. Programming the HBIAS threshold to zero inhibits the HBIAS alarm flag, preventing TX-F from being asserted, the HBIAS alarm from causing a shutdown, and the HBIAS alarm bit in Status from being set. The HBIAS enable bit can be used to prevent shutdown from occurring while allowing the HBIAS alarm flag to trigger TX-F.

Table 1. HTXP Threshold Settings

HTXP_Thresh<2:0>	HIGH-TRANSMIT POWER THRESHOLD (I_{SET})
000	Disabled*
001	Do not use
010	1.30
011	1.43
100	1.56
101	1.69
110	1.82
111	1.95

**Disabled inhibits the HTXP QT from causing a shutdown or asserting TX-F.*

Table 2. LTXP Threshold Settings

LTXP_Thresh<2:0>	LOW-TRANSMIT POWER THRESHOLD (I_{SET})
000	Disabled*
001	Do not use
010	0.81
011	0.76
100	0.54
101	0.41
110	0.28
111	0.14

**Disabled inhibits the LTXP QT from causing a shutdown or asserting TX-F.*

Password Protection

The DS1861 has two 16-bit password entry registers (used as a 32-bit value) and two 16-bit password registers (used as 32-bit value) that can be used to write-protect all the configuration settings. The password entry registers, PWE High and PWE Low, are the locations where the user enters the password to disable the write protection and change the device settings. The password bytes, PW High and PW Low, set the password to a new value. When the device is write-protected, the only bytes that can be written are the password entry bytes.

To secure the password, the PW bytes always read as 0s when the PWE bytes do not match the PW bytes. Once the correct password has been entered into the PWE bytes, the password can also be read from the PW registers. Because the PWE bytes can be read all the time, it is recommended that the PWE bytes are written to all 1s once the desired settings are modified to prevent anyone from simply reading PWE to attain the password. The PWE bytes are SRAM, so they reset themselves to 1s if V_{CC} drops below V_{POA}.

In addition to write protection, the password must also be entered and the DS1861 must be HALTed to read the $I_{BIASSET}$ and I_{MODSET} DAC codes. See the *Reading the BIASSET and MODSET Registers* section for more information about reading the DAC codes.

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DS1861 Memory Map

BASE ADDR	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
78h	Password Entry	Status	*SRAM*	*SRAM*	PWE High		PWE Low		*Reserved*
B0h	APC Config	*User EE*	*User EE*	APC	*User EE*	ER (N)	MODLOAD		Control
B8h	Fast Comp	HTXP Threshold	LTXP Threshold	HBIAS Threshold	*User EE*	*User EE*	*User EE*	*User EE*	*User EE*
C0h	Password	*Reserved*	*Reserved*	*Reserved*	PW High		PW Low		*Reserved*
D0h	DAC Codes	*Reserved*	$I_{BIASSET}$ Code	*Reserved*	*Reserved*	*Reserved*	*Reserved*	I_{MODSET} Code	

KEY:	SRAM	EEPROM

EXPANDED BYTES																	
BYTE ADDR	BYTE NAME	BIT 7		BIT 6		BIT 5		BIT 4		BIT 3		BIT 2		BIT 1		BIT 0	
		bit_{15}	bit_{14}	bit_{13}	bit_{12}	bit_{11}	bit_{10}	bit_9	bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1	bit_0
78h	Status	Shutdown Flag		HTXP Shutdown		LTXP Shutdown		HBIAS Shutdown		POA		HTXP Alarm		LTXP Alarm		HBIAS Alarm	
7Bh	PWE High	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
7Dh	PWE Low	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
B2h	APC	GAIN2		GAIN1		GAIN0		2^4		2^3		2^2		2^1		2^0	
B4h	ER (N)	RSEL		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
B5h	MODLOAD	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	*EE*	*EE*	*EE*	*EE*
B7h	Control	MODLOAD Enable		HTXP Enable		LTXP Enable		HBIAS Enable		DPOL		Soft TX-D		Excite Disable		HALT	
B8h	High TX-P Alarm Threshold	*EE*		*EE*		*EE*		*EE*		*EE*		2^2		2^1		2^0	
B9h	Low TX-P Alarm Threshold	*EE*		*EE*		*EE*		*EE*		*EE*		2^2		2^1		2^0	
BAh	High BIAS Alarm Threshold	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
C3h	PW High	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
C5h	PW Low	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
D1h	$I_{BIASSET}$ Code	2^7		2^6		2^5		2^4		2^3		2^2		2^1		2^0	
D6h	I_{MODSET} Code	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	0	0	0

Note: *0 indicates an unused bit that reads as 0.*

Detailed Register Description Conventions

Name of Row

• *Name of Byte...*<**Write Access**><**Volatility**><**Power-Up/Factory Default Value**>

0. Name of bit 0.....Bit 0 Description

1. Name of bit 1.....Bit 1 Description

2 to 7. Bit names.....Bit 2 to 7 Descriptions

Write Access: W is write-only access, R is read-only access, and R/W is read/write access. A password may be required for write access on R/W registers. See the memory map for complete access code descriptions.

Volatility: V is volatile (SRAM), NV is nonvolatile (EEPROM).

Power-Up/Factory Default Value: For SRAM registers, this value is always the power-up value. For EEPROM registers, this is the factory default value. These can be permanently modified by entering the password and writing the register. N/A is used for hardware-dependent values, such as alarm flags.

Password Entry

• *Status* <R><V><N/A, depends on power-up condition>

0. HBIAS Alarm.....High Bias-Current Alarm. This flag is high when $I_{BIASSET} \geq$ HBIAS Alarm Threshold. This flag is updated every 4µs or 16µs depending on the state of the convergence algorithm. Programming HBIAS threshold byte to zero disables the HBIAS Alarm.
1. LTXP Alarm.....Low Transmitted Power Alarm. This flag is high when the I_{BMD} current drops below the value set by the LTXP threshold. This flag is updated every 16µs. Programming LTXP threshold to zero disables this flag. This flag willl be high when TX-D = 1 unless the alarm has been disabled.
2. HTXP Alarm....High Transmitted Power Alarm. This flag is high when the I_{BMD} current rises above the value set by the HTXP threshold. This flag is updated every 16µs. Programming HTXP Threshold to zero disables this flag.
3. POA....Analog Power-On Reset Alarm (V_{CC} Power Good). This flag is set when $V_{CC} < V_{POA}$.
4. HBIAS Shutdown....This flag goes high when a HBIAS safety fault is generated and HBIAS Enable is high. *HBIAS Shutdown* goes low with POA or a falling edge of the TX-D pin, providing the safety fault is no longer present.
5. LTXP Shutdown....This flag goes high when a LTXP safety fault is generated and LTXP Enable is high. *LTXP Shutdown* goes low with POA or a falling edge of TX-D, providing the safety fault is no longer present.
6. HTXP Shutdown....This flag goes high when a HTXP safety fault is generated and HTXP Enable is high. *HTXP Shutdown* goes low with POA or a falling edge of TX-D, providing the safety fault is no longer present.
7. Shutdown Flag....This flag is high when any of the three latched safety faults are high (*HBIAS Shutdown, LTXP Shutdown,* or *HTXP Shutdown*), and it remains high after the individual flag's are reset until fault reset time has elapsed.

• *PWE High & Low*....<R/W><V><FFFFh> Until the correct 32-bit password is written to PWE, the PWE bytes are the only locations that can be written. PWE should be written to a value other than the password once the device's configuration has been updated to prevent the password from being read from PWE. After a power cycle these locations will each be reset to FFFFh.

APC Config

• *APC*....<R/W><NV><00h> Sets the desired value of the feedback current into the I_{BMD} pin. The 3 MSB's determine the input GAIN value according to this table:

APC<7:5>	GAIN
000	1
001	2
010	4
011	8
1xx	16

The remaining 5 LSBs determine the I_{BMD} current setpoint (I_{SET}) assuming a *GAIN* of 1. The formula for the I_{BMD} current setpoint with the gain is then given by:

$$I_{SET} = 1.525\mu A \text{ GAIN } (APC\langle 4{:}0\rangle + 32)$$

If values greater than 10011111b (9Fh) are programmed into the APC register, the DS1861 will clamp I_{SET} to its maximum value, equivalent to if the register was set to 10011111b.

• *ER (N)*....<R/W><NV><1Ch> Sets the gain *(N)* on the measured excitation current used to generate I_{MODSET}. This sets the extinction ratio of the system. Higher N values increase the excitation ratio. The MSB of this register (RSEL) is a flag that selects a high (RSEL = 1) or low (RSEL = 0) range for *N*. The 7 LSBs of the register determine the actual N code. The value of N can be calculated by the following equation:

Full Laser Control with Fault Management

$$N = \begin{cases} \frac{ER<6:0>+32}{2} & RSEL = 0 \\ ER<6:0>+32 & RSEL = 1 \end{cases}$$

The default setting of ER = 1Ch corresponds to N = 30, which is the minimum useable value. The maximum useable value is N = 136 (ER = E8h). For more information refer to the *Automatic Extinction Ration Control* section.

• *MODLOAD*.....<R/W><NV><0000h> This register determines the startup value of I_{MODSET} following a falling edge of TX-D when MODLOAD_Enable = 1 and no fault condition has occurred. This 12-bit register value is left justified in a 16-bit register. The 4 LSBs default to 0s.

• *Control*.....<R/W><NV><70h> This byte is used to enable/disnable the shutdown alarms and configure several other settings. Writing to this byte causes an EEPROM write cycle, even if only the HALT bit (SRAM) is changed. It should not be modified more than the specified number of write cycles.

0. HALT.....Setting this bit high stops the control loop and freezes the outputs at their present state. Once the control loop is stopped the $I_{BIASSET}$ and I_{MODSET} output registers can be read. This bit is SRAM and resets to zero when V_{CC} drops below V_{POAF}.
1. Excite_Disable.....Setting this bit high prevents the DS1861 from entering the excitation state (it does not add the disturbance current), which disables automatic extinction ratio control. I_{MODSET} will remain at its last value until reset by a fault or set to MODLOAD.
2. Soft_TX-Disable.....This bit is ORed with the TX-D pin to create the internal TX-Disable signal. So asserting either Soft_TX-Disable or the TX-D pin will disable the outputs. Both Soft_TX-Disable and TX-D must be deasserted for the outputs to operate.
3. DPOL.....Diode Polarity. Set to 0 to have the BMD pin source current. Set to 1 to have BMD sink current.
4. HBIAS_Enable.....Set high to allow a safety fault caused by high bias alarm shut the part down.
5. LTXP_Enable.....Set high to allow a safety fault caused by low transmitted power alarm shut the part down.
6. HTXP_Enable.....Set high to allow a safety faultl caused by high transmitted power alarm shut the part down.
7. MODLOAD_Enable.....If high, I_{MODSET} loads the value in MODLOAD on the falling edge of TX-D when no fault condition is present. Otherwise, I_{MODSET} will return to operation with its value prior to when TX-D was asserted.

Quick-Trip Monitors

• *HTXP Threshold*.....<R/W><NV><00h> Sets the threshold current for the HTXP alarm. The alarm trips when $I_{BMD} > I_{BMD\ SETPOINT} \cdot [1 + (HTXP\ Threshold<2:0>)\ 0.125]$. Set to 00h to disable the alarm.

• *LTXP Threshold*.....<R/W><NV><00h> Sets the threshold current for the LTXP alarm. The alarm trips when $I_{BMD} < I_{BMD\ SETPOINT} \cdot [1 - (LTXP\ Threshold<2:0>)\ 0.125]$. Set to 00h to disable the alarm.

• *HBIAS Threshold*.....<R/W><NV><00h> Sets the threshold current for the high bias current alarm. The alarm trips when BIAS current is ≥7.625µA x (*HBIAS Threshold)*. This register value is compared directly against the $I_{BIASSET}$ code value in register D1h to determine if an alarm condition has occurred. Set HBIAS threshold to 00h to disable this alarm.

Password

• *PW High and Low*.....<R/W><NV><0000h> The PWE value is compared against the value written to these locations to determine if the user has write access to password-protected memory locations. These locations read as zeros unless the password has been entered into PWE to ensure the password remains secure.

DAC Codes

• $I_{BIASSET}$ *Code*.....<R/W><V><00h> This is the most signicant byte of the 18-bit $I_{BIASSET}$ DAC code. $I_{BIASSET}$ = 7.625µA x ($I_{BIASSET}$ code). The part must be halted and the password must be entered to read this value.

• I_{MODSET} *Code*.....<R/W><V><0000h> The I_{MODSET} DAC code. The LSB weight of the I_{MODSET} DAC code is 477nA. Thus, I_{MODSET} = 477nA x (I_{MODSET} code). The part must be halted and the password entered to read this value. The four least significant bytes of this register read as 0s.

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, and start and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic-high states.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition. See the timing diagram for applicable timing.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition. See the timing diagram for applicable timing.

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 14). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 14) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 14) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

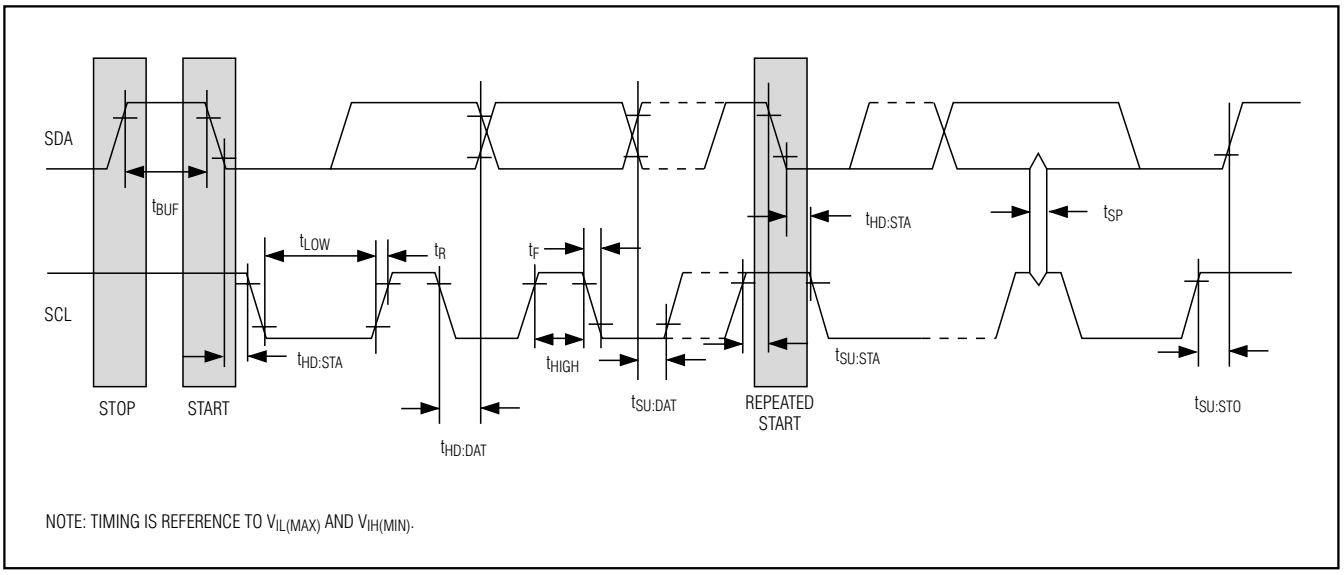


Figure 14. I²C Timing Diagram

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave addressing byte sent immediately following a start condition. The slave address byte (Figure 15) contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1861's slave address is 1010$A_2A_1A_0$ (binary), where A_2, A_1, and A_0 are the values of the address pins. The address pins allow the device to respond to one of eight possible slave addresses. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$ = 1, the master will read data from the slave. If an incorrect slave address is written, the DS1861 assumes the master is communicating with another I²C device and ignore the communications until the next start condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a start condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data and generate a stop condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave the master generates a start condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes and generates a stop condition.

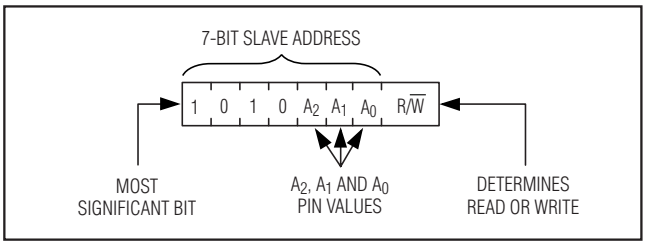


Figure 15. Slave Address Byte

The DS1861 can write 1 to 8 bytes (referred to as 1 row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one row of the memory map. Attempts to write to additional memory rows without sending a stop condition between rows will result in the address counter wrapping around to the beginning address of the present row.

Example: A 3-byte write starts at address BEh and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result would be addresses BEh and BFh would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address B8h.

To prevent address wrapping from occurring, the master must send a stop condition at the end of the row, and then wait for the bus free or EEPROM write time to elapse. Then the master can generate a new start condition, write the slave address byte (R/$\overline{W}$ = 0), and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time EEPROM is written, the DS1861 requires the EEPROM write time (t_W) after the stop condition to write the contents of the row to EEPROM. During the EEPROM write time, the DS1861 does not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS1861, which allows the next row to be written as soon as the DS1861 is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_W to elapse before attempting to write again to the DS1861.

EEPROM Write Cycles: When EEPROM writes occur, the DS1861 will write the whole EEPROM memory row even if only a single byte on the row was modified. Writes that do not modify all 8 bytes on the row are allowed and do not corrupt the remaining bytes of memory on the same row. Because the whole row is written, bytes on the row that were not modified during the transaction are still subject to a write cycle. This

can result in a whole row being worn out over time by writing a single byte repeatedly. Writing a row one byte at a time will wear out the EEPROM eight times faster than writing the entire row at once. The DS1861's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave at the location currently in the address counter; the master generates a start condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a start condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated start condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a stop condition.

Figure 16 shows a read example using the repeated start condition to specify the starting memory location.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte, it NACKs to indicate the end of the transfer and generates a stop condition. This can be done with or without modifying the address counter's location before the read cycle.

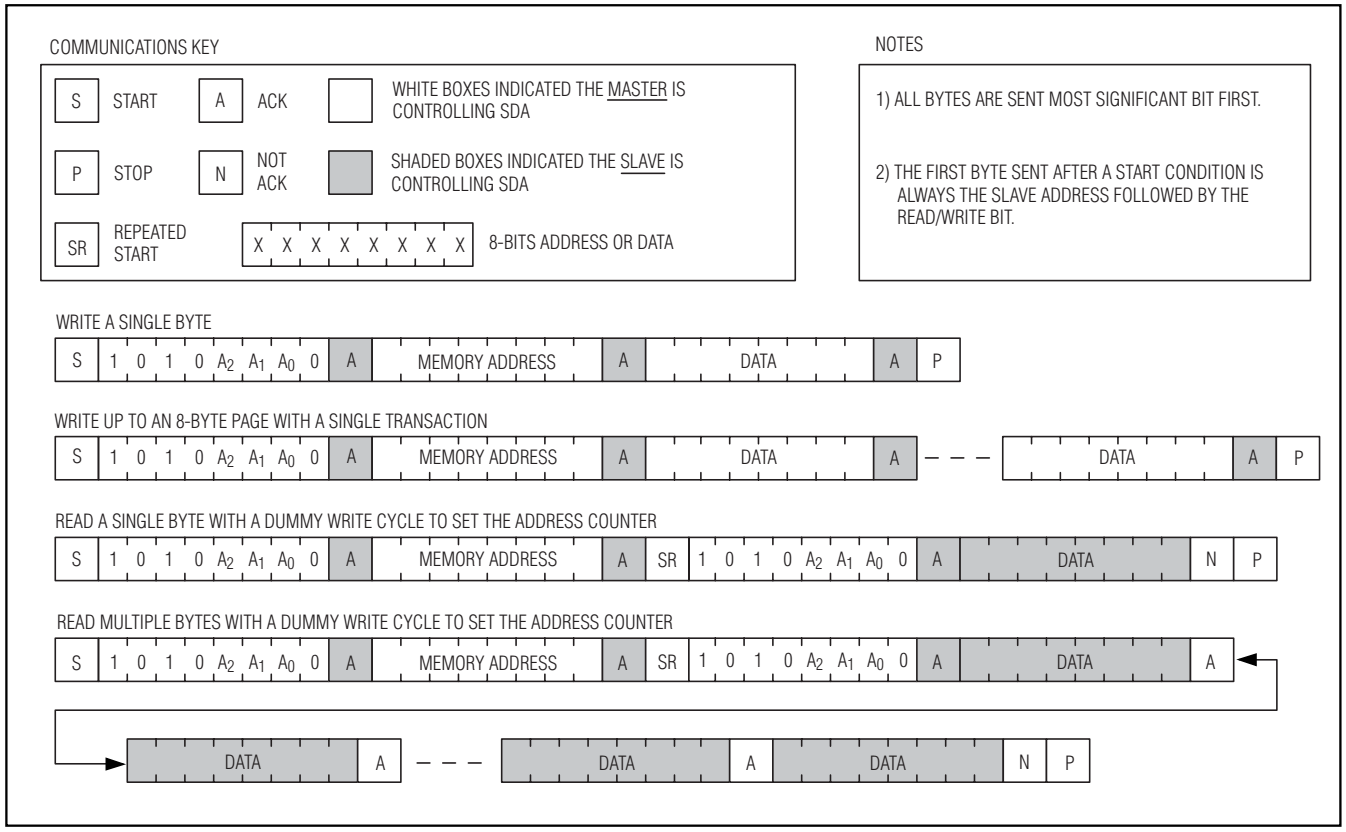


Figure 16. I²C Communications Examples

Full Laser Control with Fault Management

Applications Information

Calibrating APC and Extinction Ratio

Before calibrating, the APC register should be set to a low value to ensure the laser's maximum power level is not exceeded before the power level is calibrated. Additionally, the ER register should be set to its minimum value (28 decimal) to ensure that a data test pattern does not cause the laser to shut off. Once the APC and ER registers are at minimal values, enable a data pattern and calibrate the average power level first.

Calibrating the Average Power Level

While sending data through the laser diode, increase the value in the APC register until the light output matches the desired average power level. The average power level is the arithmetic average of the 1 and 0 power levels.

Calibrating the Extinction Ratio

While sending data through the laser diode, begin increasing the ER register from its minimum value of 28 decimal (1Ch), until the proper extinction ratio is reached or the maximum setting (104 decimal or 68h) of the low range is reached. If the maximum low range value is reached, write the ER register to 156 decimal (9Ch), which switches the extinction ratio value to the minimum value of the high range. Continue increasing the ER setting until the proper extinction ratio is reached. If the maximum value of the high range setting is reached (232 decimal or E8h) without reaching the proper extinction ratio, then either the desired extinction ratio cannot be reached or a problem is preventing the system from operating properly.

Addressing Multiple DS1861s on a Common I²C Bus

Up to eight DS1861s can be addressed on a single I²C bus by using the device's address inputs (A_2, A_1, A_0) to change its slave address. For information about device addressing, see the *I²C Communications s*ection.

Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize lead inductance.

BMD Shunt Capacitor

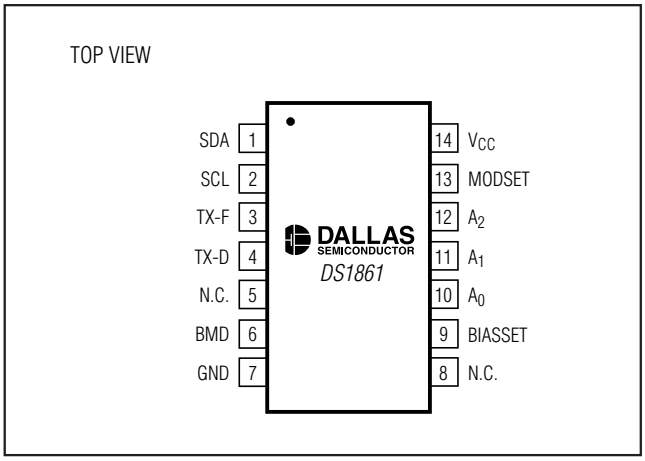
The BMD shunt capacitor works with the internal resistance of the BMD input to provide a lowpass filter that reduces the effects of noise on the APC loop. Its capacitance value must be chosen carefully to ensure that it is both large enough to provide good filtering of high-frequency noise and small enough that it does not cause the control loop to become unstable. A 1nF, 10% tolerant, X7R ceramic capacitor is recommended.

SDA and SCL Pullup Resistors

SDA is an open-collector bidirectional data pin on the DS1861 that requires a pullup resistor to realize high logic levels. Either an open-collector output with a pullup resistor or a push-pull output driver can be used for the SCL input. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *AC Electrical Characteristics* table are within specification.

Full Laser Control with Fault Management

Pin Configuration



Chip Information

TRANSISTOR COUNT: 55,677

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.