February 2006

FSDH0170RNB/FSDH0270RNB/FSDH0370RNB
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged 700V Sense FET
- Consumes only 0.8W at 230 VAC & 0.5W load with Burst-Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency, 100kHz
- Internal Start-up Circuit and Built-in Soft Start
- Pulse-by-Pulse Current Limiting and Auto-Restart Mode
- Over Voltage Protection (OVP), Over Load Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit

Applications

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD & DVCD Player
- SMPS for Printer, Facsimile & Scanner
- Adapter for Camcorder

Related Application Notes

- AN-4137, AN-4141, AN-4147 (Flyback)
- AN-4134 (Forward)

Description

The FSDH0170RNB/FSDH0270RNB/FSDH0370RNB consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche rugged 700V Sense FET. It is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry. Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDH0170RNB/FSDH0270RNB/FSDH0370RNB reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, as in PC auxiliary power supplies.

Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$ (MAX.)
FSDH0170RNB	8DIP	DH0170R	700V	100KHz	11Ω
FSDH0270RNB	8DIP	DH0270R	700V	100KHz	7.2Ω
FSDH0370RNB	8DIP	DH0370R	700V	100KHz	4.75Ω

FPS™ is a trademark of Fairchild Semiconductor Corporation.

Typical Circuit

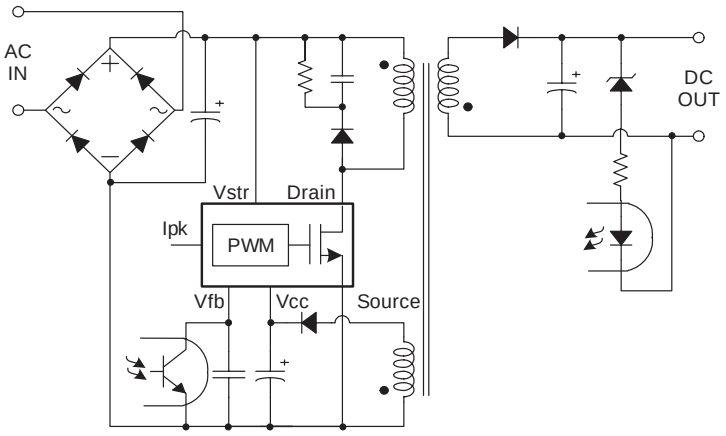


Figure 1. Typical Flyback Application

Output Power Table[4]

Product	230VAC ±15%[3]		85–265VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
FSDH0170RNB	14W	20W	9W	13W
FSDH0270RNB	17W	24W	11W	16W
FSDH0370RNB	20W	27W	13W	19W

Notes:
1. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.
4. The maximum output power can be limited by junction temperature.

Internal Block Diagram

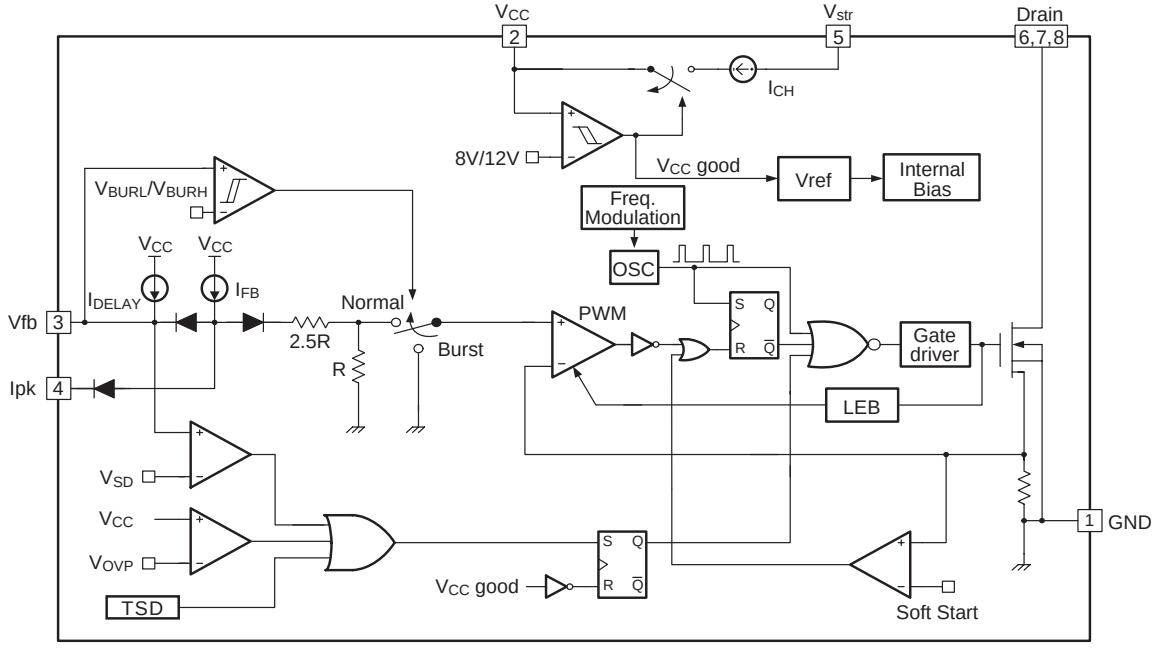


Figure 2. Functional Block Diagram of FSDH0170RNB/FSDH0270RNB/FSDH0370RNB

Pin Configuration

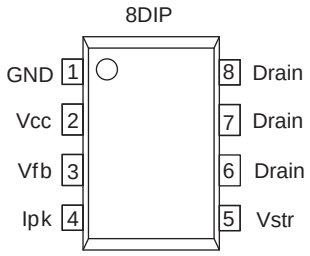


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram Section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers overload protection (OLP). There is a time delay while charging external capacitor Cfb from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	Ipk	This pin adjusts the peak current limit of the Sense FET. The 0.9mA feedback current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin. This determines the peak current limit. If this pin is tied to Vcc or left floating, the typical peak current limit will be 0.8A (FSDH0170RNB), 0.9A (FSDH0270RNB), or 1.1A (FSDH0370RNB).
5	Vstr	This pin connects to the rectified AC line voltage source. At start-up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is opened.
6, 7, 8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 700V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Characteristic		Symbol	Value	Unit
Drain Pin Voltage		V_{DRAIN}	700	V
Vstr Pin Voltage		V_{STR}	700	V
Drain Current Pulsed[5]	FSDH0170RNB	I_{DM}	4	A
	FSDH0270RNB	I_{DM}	8	A
	FSDH0370RNB	I_{DM}	12	A
Single Pulsed Avalanche Energy[6]	FSDH0170RNB	E_{AS}	50	mJ
	FSDH0270RNB	E_{AS}	140	mJ
	FSDH0370RNB	E_{AS}	230	mJ
Supply Voltage		V_{CC}	20	V
Feedback Voltage Range		V_{FB}	-0.3 to V_{CC}	V
Total Power Dissipation		P_D	1.5	W
Operating Junction Temperature		T_J	Internally limited	°C
Operating Ambient Temperature		T_A	-25 to +85	°C
Storage Temperature		T_{STG}	-55 to +150	°C

Thermal Impedance

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
8 DIP			
Junction-to-Ambient Thermal[7]	θ_{JA}	80	°C/W
Junction-to-Case Thermal[8]	θ_{JC}	20	°C/W
Junction-to-Top Thermal[9]	ψ_{JT}	35	°C/W

All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Notes:

5. Non-repetitive rating: Pulse width is limited by maximum junction temperature.
6. L = 51mH, starting Tj = 25°C.
7. Free standing with no heatsink; Without copper clad.
8. Measured on the DRAIN pin close to plastic interface.
9. Measured on the PKG top surface.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET Section[11]							
Zero-Gate-Voltage Drain Current		I_{DSS}	V_{DS} = 700V, V_{GS} = 0V	–	–	50	μA
			V_{DS} = 560V, V_{GS} = 0V, T_C = 125°C	–	–	200	
Drain-Source On-State Resistance[10]	FSDH0170RNB	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 0.5A	–	8.8	11	Ω
	FSDH0270RNB			–	6.0	7.2	
	FSDH0370RNB			–	4.0	4.75	
Input Capacitance	FSDH0170RNB	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	250	–	pF
	FSDH0270RNB			–	550	–	
	FSDH0370RNB			–	315	–	
Output Capacitance	FSDH0170RNB	C_{OSS}		–	25	–	
	FSDH0270RNB			–	38	–	
	FSDH0370RNB			–	47	–	
Reverse Transfer Capacitance	FSDH0170RNB	C_{RSS}		–	10	–	
	FSDH0270RNB			–	17	–	
	FSDH0370RNB			–	9	–	
Turn-On Delay Time	FSDH0170RNB	$t_{d(on)}$	V_{DS} = 350V, I_D = 1.0A	–	12	–	ns
	FSDH0270RNB			–	20	–	
	FSDH0370RNB			–	11.2	–	
Rise Time	FSDH0170RNB	t_r		–	4	–	
	FSDH0270RNB			–	15	–	
	FSDH0370RNB			–	34	–	
Turn-Off Delay Time	FSDH0170RNB	$t_{d(off)}$		–	30	–	
	FSDH0270RNB			–	55	–	
	FSDH0370RNB			–	28.2	–	
Fall Time	FSDH0170RNB	t_f		–	10	–	
	FSDH0270RNB			–	25	–	
	FSDH0370RNB			–	32	–	
Control Section							
Switching Frequency		f_{OSC}		92	100	108	KHz
Switching Frequency Modulation		Δf_{MOD}		±2	±3	±4	KHz
Switching Frequency Variation[11]		Δf_{OSC}	-25°C ≤ T_A ≤ 85°C	–	±5	±10	%
Maximum Duty Cycle		D_{MAX}		62	67	72	%
Minimum Duty Cycle		D_{MIN}		0	0	0	%
UVLO Threshold Voltage		V_{START}	V_{FB} = GND	11	12	13	V
		V_{STOP}	V_{FB} = GND	7	8	9	
Feedback Source Current		I_{FB}	V_{FB} = GND	0.7	0.9	1.1	mA
Internal Soft Start Time[11]		$t_{S/S}$	V_{FB} = 4V	–	10	–	ms

Electrical Characteristics (Continued)

(T_A = 25°C unless otherwise specified)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Burst Mode Section							
Burst Mode Voltage		V_{BURH}	Tj = 25°C	0.5	0.6	0.7	V
		V_{BURL}		0.3	0.4	0.5	V
		$V_{BUR(HYS)}$		100	200	300	mV
Protection Section							
Peak Current Limit	FSDH0170RNB	I_{LIM}	di/dt = 170mA/µs	0.70	0.80	0.90	A
	FSDH0270RNB		di/dt = 200mA/µs	0.79	0.90	1.01	
	FSDH0370RNB		di/dt = 240mA/µs	0.97	1.10	1.23	
Current Limit Delay Time[11]		t_{CLD}		–	500	–	ns
Thermal Shutdown Temperature[11]		T_{SD}		125	140	–	°C
Shutdown Feedback Voltage		V_{SD}		5.5	6.0	6.5	V
Over Voltage Protection		V_{OVP}		18	19	–	V
Shutdown Delay Current		I_{DELAY}	V_{FB} = 4V	3.5	5.0	6.5	µA
Leading Edge Blanking Time[11]		t_{LEB}		200	–	–	ns
Total Device Section							
Operating Supply Current (control part only)		I_{OP}	V_{CC} = 14V	1	3	5	mA
Start-Up Charging Current		I_{CH}	V_{CC} = 0V	0.7	0.85	1.0	mA
Vstr Supply Voltage		V_{STR}	V_{CC} = 0V	35	–	–	V

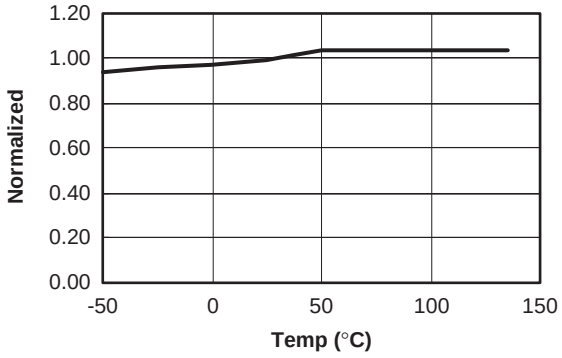
Notes:

10. Pulse test: Pulse width ≤ 300µs, duty ≤ 2%
11. These parameters, although guaranteed, are not 100% tested in production

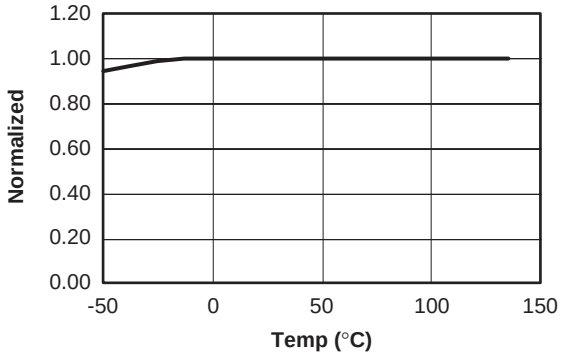
Typical Performance Characteristics (Control Part)

(These characteristic graphs are normalized at T_A = 25°C)

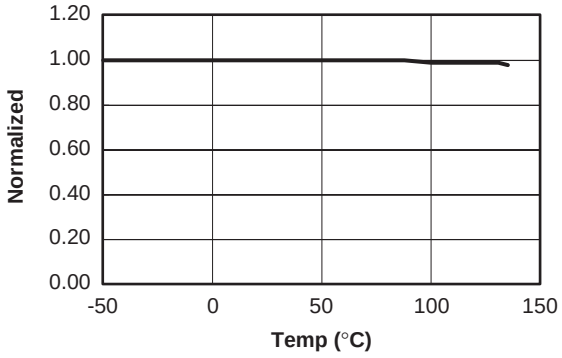
Operating Frequency (fosc) vs. T_A



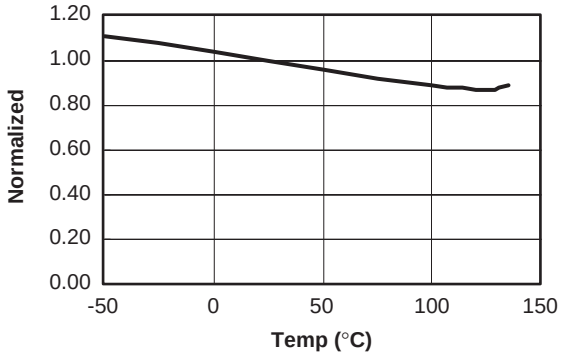
Frequency Modulation (Δf_{MOD}) vs. T_A



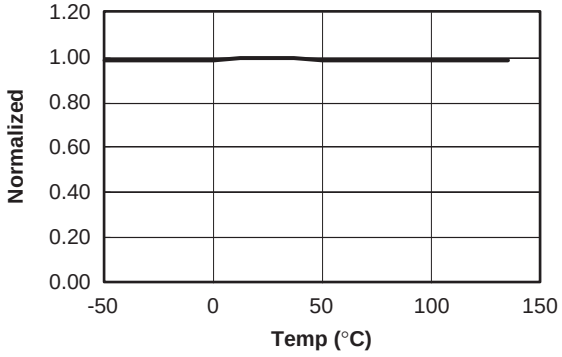
Maximum Duty Cycle (D_{MAX}) vs. T_A



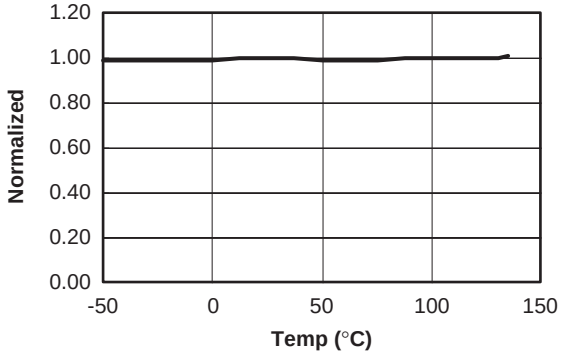
Operating Supply Current (I_{OP}) vs. T_A



Start Threshold Voltage (V_{START}) vs. T_A

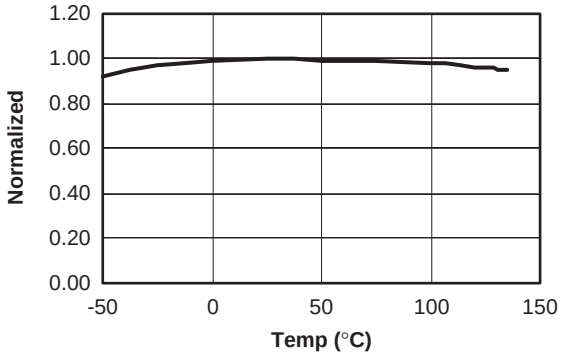


Stop Threshold Voltage (V_{STOP}) vs. T_A

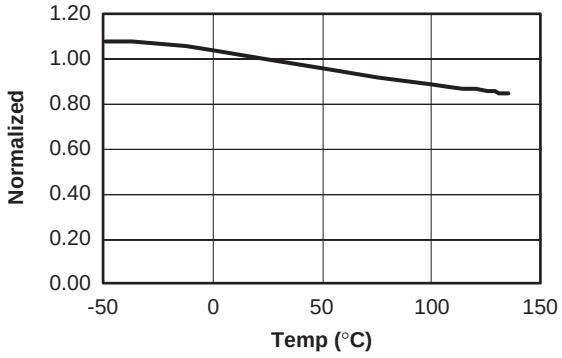


Typical Performance Characteristics (Continued)

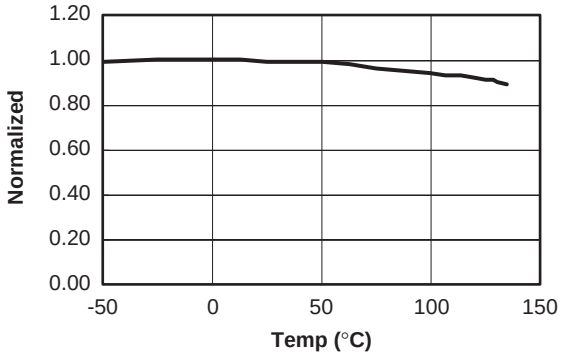
Feedback Source Current (I_{FB}) vs. T_A



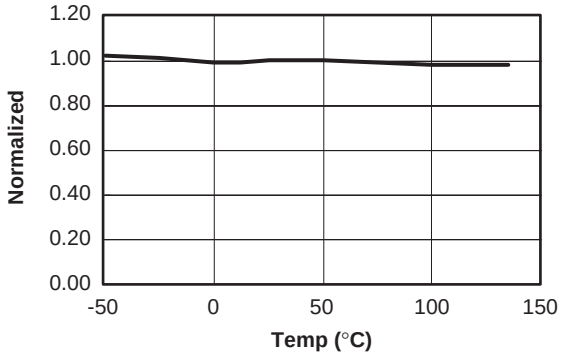
Start Up Charging Current (I_{CH}) vs. T_A



Peak Current Limit (I_{LIM}) vs. T_A



Over Voltage Protection (V_{OVP}) vs. T_A



Functional Description

1. Startup: In previous generations of Fairchild Power Switches (FPS™) the Vstr pin required an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off 10ms after the supply voltage, Vcc, goes above 12V. The source turns back on if Vcc drops below 8V.

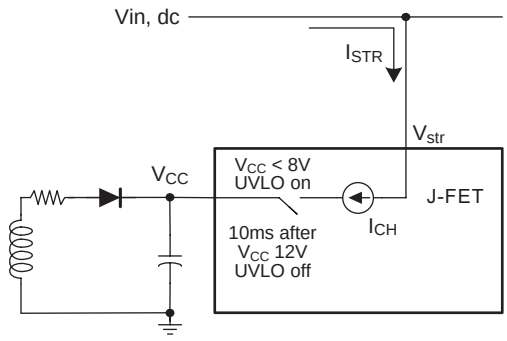


Figure 4. High Voltage Current Source

2. Feedback Control: The 700V FPS series employs current mode control, as shown in Figure 5. An optocoupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor of Sense FET plus an offset voltage makes it possible to control the switching duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the optocoupler LED current increases, the feedback voltage Vfb is pulled down and thereby reduces the duty cycle. This typically happens when the input voltage increases or the output load decreases.

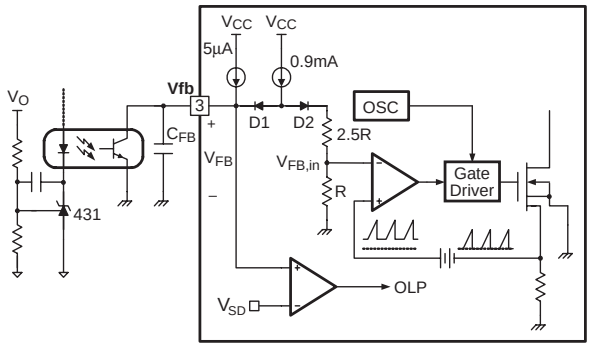
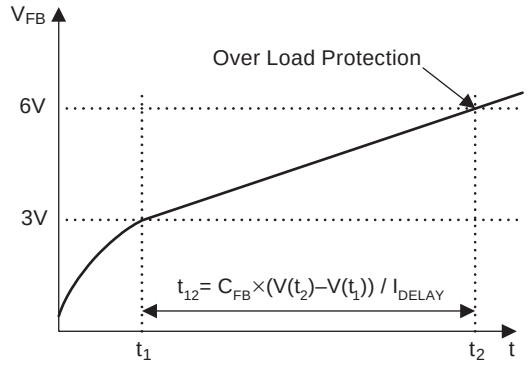


Figure 5. Pulse Width Modulation (PWM) Circuit

3. Leading Edge Blanking (LEB): When the internal Sense FET is turned on; the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a Leading Edge Blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuits: The FPS has several protective functions such as Over Load Protection (OLP), Over Voltage Protection (OVP), Under Voltage Lock Out (UVLO), and Thermal Shut Down (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage, V_{STOP} (typically 8V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage, V_{START} (typically 12V), the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

4.1 Over Load Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the Over Load Protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below its nominal voltage. This reduces the current through the optocoupler LED, which also reduces the optocoupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to slowly charge Cfb up to Vcc. In this condition, V_{FB} increases until it reaches 6V, when the switching operation is terminated as shown in Figure 6. The shutdown delay time is the time required to charge Cfb from 3V to 6V with 5μA current source.



$$t_{12} = C_{FB}\frac{V(t_2)-V(t_1)}{I_{DELAY}};\quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 6V$$

Figure 6. Over Load Protection (OLP)

4.2 Thermal Shutdown (TSD): The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Over Voltage Protection (OVP): In the event of a malfunction in the secondary side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto coupler transistor becomes almost zero (refer to Figure 5). Then, V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an Over Voltage Protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

5. Soft Start: The FPS has an internal soft start circuit that slowly increases the Sense FET current after startup as shown in Figure 7. The typical soft start time is 10ms, where progressive increments of the Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

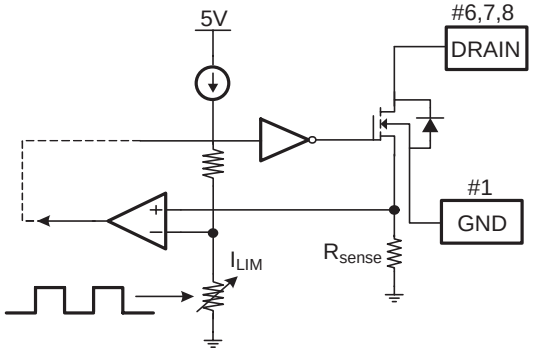


Figure 7. Soft Start Function

6. Burst Operation: In order to minimize power dissipation in standby mode, the FPS enters burst mode operation. Feedback voltage decreases as the load decreases and as shown in Figure 8, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} (typically 600mV). Switching still continues until the feedback voltage drops below V_{BURL} (typically 400mV). At this point switching stops and the output voltage start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process is repeated. Burst mode operation alternately enables and disables switching of the Sense FET and reduces switching loss in standby mode.

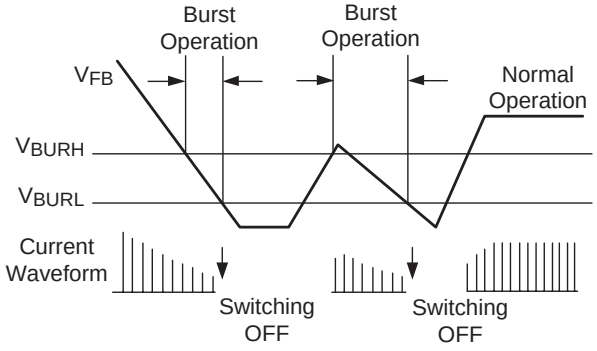


Figure 8. Burst Operation Function

7. Frequency Modulation: Modulating the switching frequency of a switched power supply can reduce EMI. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 9, the frequency changes from 97KHz to 103KHz in 4ms for the 700V FPS series. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

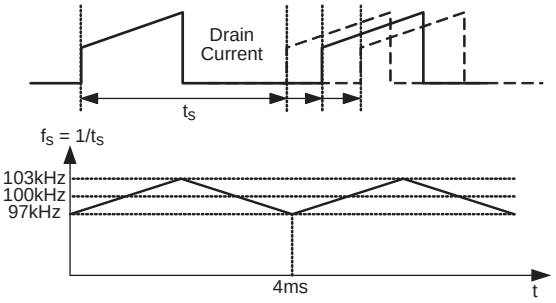


Figure 9. Frequency Modulation Waveform

8. Adjusting Peak Current Limit: As shown in Figure 10, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA.

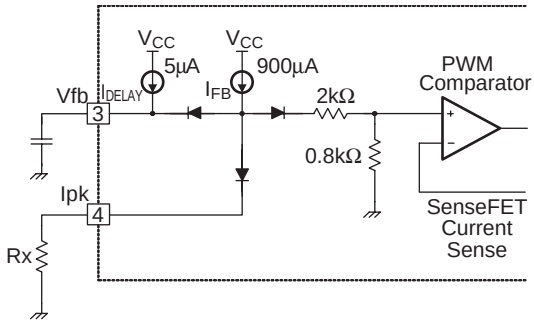


Figure 10. Peak Current Limit Adjustment

For example, FSDH0270RNB has a typical Sense FET peak current limit (I_{LIM}) of 0.9A. I_{LIM} can be adjusted to 0.6A by inserting Rx between the Ipk pin and the ground. The value of the Rx can be estimated by the following equations:

0.9A : 0.6A = 2.8kΩ : XkΩ,

X = Rx || 2.8kΩ.

(X represents the resistance of the parallel network)

Application Tips

1. Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can make noise depending on the load condition. Here are three methods to reduce noise:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. Glue or varnish can also can crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. Another consideration is to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4KHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4KHz. When the fundamental frequency of noise is located in this range, the noise sounds louder although the noise intensity level is identical. Refer to Figure 11.

When FPS acts in Burst mode and the Burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst mode operation lies in the range of 2~4KHz, adjusting the feedback loop can shift the Burst operation frequency. In order to reduce the Burst operation frequency, increase a feedback gain capacitor (C_F), optocoupler supply resistor (R_D) and feedback capacitor (C_B) and decrease a feedback gain resistor (R_F) as shown in Figure 12.

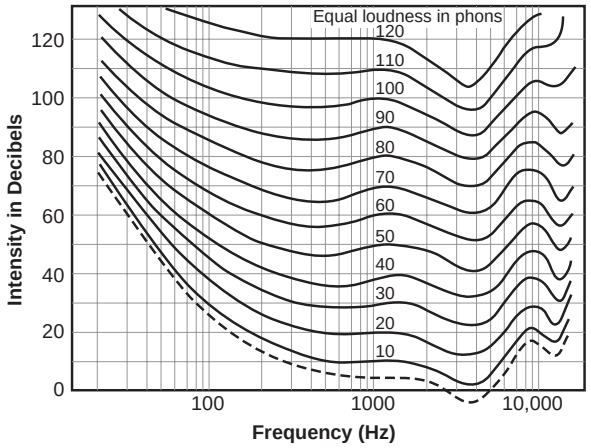


Figure 11. Equal Loudness Curves

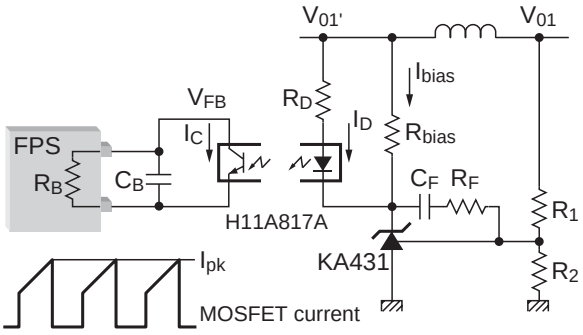


Figure 12. Typical Feedback Network of FPS

2. Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS Applications

Typical Application Circuit

Application	Output power	Input voltage	Output Voltage (Max current)
PC Auxiliary Power Supply (Using FSDH0270RNB)	15W	Universal input (85–265 Vac)	5V (3A)

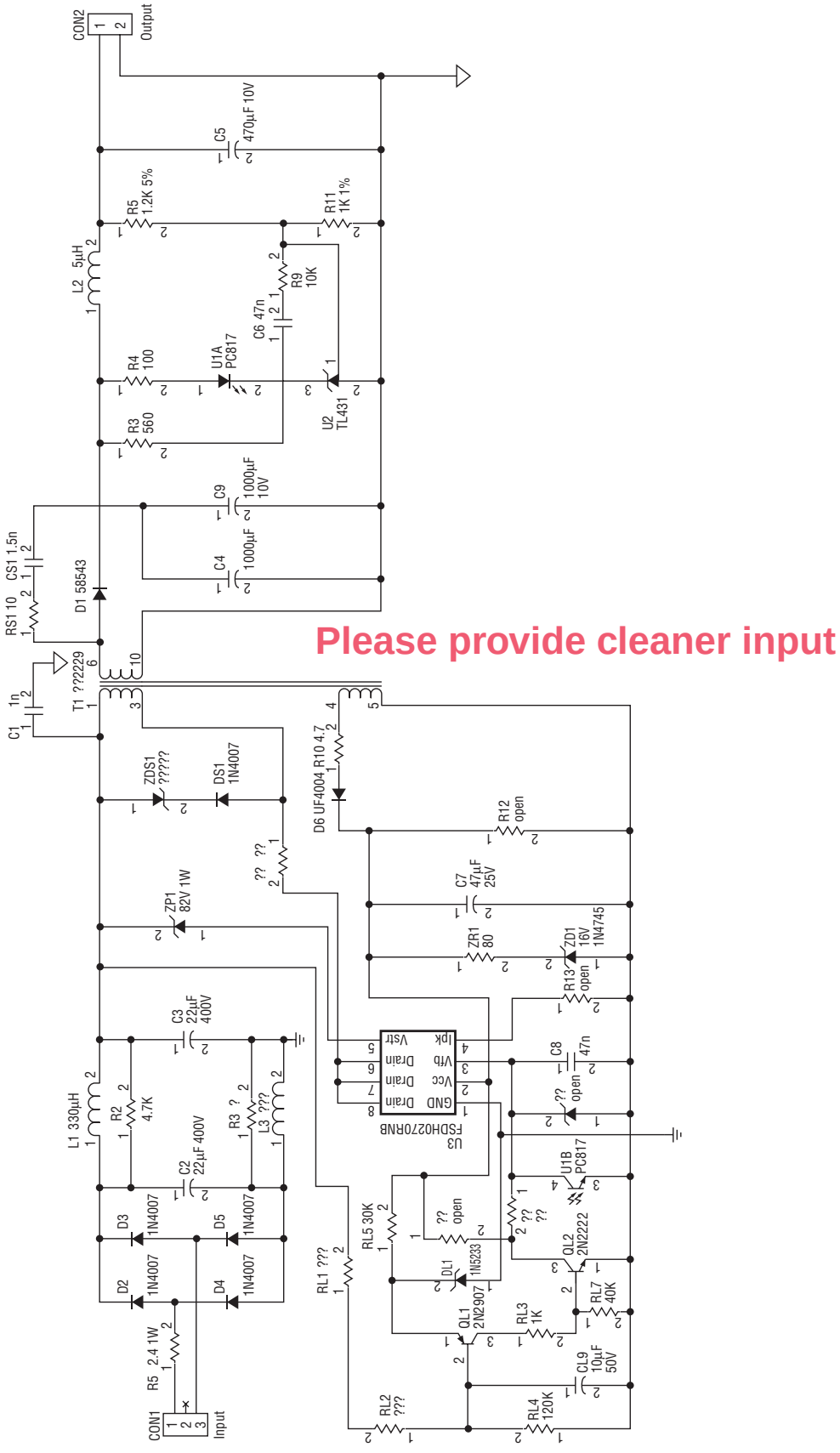
Features

- High efficiency (> 78% at 115 Vac and 230 Vac input)
- Low standby mode power consumption (< 0.8W at 230 Vac input and 0.5W load)
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft-start (10ms)
- Line UVLO function can be achieved using external component

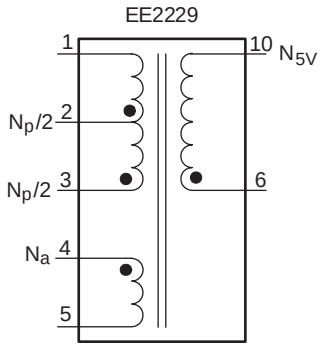
Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C8 of 47nF. If faster/slower triggering of OLP is required, C8 can be changed to a smaller/larger value (e.g. 100nF for about 60ms).
- ZP1, DL1, RL1, RL2, RL3, RL4, RL5, RL7, QL1, QL2, and CL9 build a Line Under Voltage Lock Out block (UVLO). The zener voltage of ZP1 determines the input voltage which makes FPS turn on. RL5 and DL1 provide a reference voltage from V_{CC}. If the input voltage divided by RL1, RL2, and RL4 is lower than the zener voltage of DL1, QL1 and QL2 turn on and pull down Vfb to ground.
- This evaluation board and corresponding test report can be provided.

1. Schematic


Please provide cleaner input
CON2
Output
C5 470µF 10V
R5 1.2K 5%
R11 1K 1%
L2 5µH
R9 10K
C6 47n
R4 100
U1A PC817
U2 TL431
R3 560
C9 1000µF 10V
C4 1000µF 10V
CS1 1.5n
RS1 10
D1 58543
T1 ??2229
C1 1n
ZDS1 ????
DS1 1N4007
D6 UF4004
R10 4.7
R12 open
C7 47µF 25V
ZP1 82V 1W
ZR1 80
ZD1 16V 1N4745
R13 open
C3 22µF 400V
C8 47n
U3 FSDH0270RNB
GND Drain Vcc Drain Vfb Ipk Vstr
L1 330µH
R2 4.7K
R3 ? ???
L3 ???
C2 22µF 400V
U1B PC817
D3 1N4007
D5 1N4007
D2 1N4007
D4 1N4007
RL5 30K
RL1 ???
DL1 1N5233
QL2 2N2222
RL7 40K
QL1 2N2907
RL3 1K
CL9 10µF 50V
R5 2.4 1W
CON1
Input
RL2 ???
RL4 120K

2. Transformer Schematic Diagram



3. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
N_a	4 → 5	0.3φ × 1	22	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 1 Layers				
$N_p/2$	3 → 2	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
N_{5V}	6 → 10	0.65φ × 3	8	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
$N_p/2$	2 → 1	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				

4. Electrical Characteristics

	Pin	Spec.	Remark
Inductance	1–3	1.20mH ± 10%	100kHz, 1V
Leakage	1–3	< 35μH Max	Short all other pins

5. Core & Bobbin

Core: EE2229 (Material: PL-7, Ae = 35.7 mm^2)

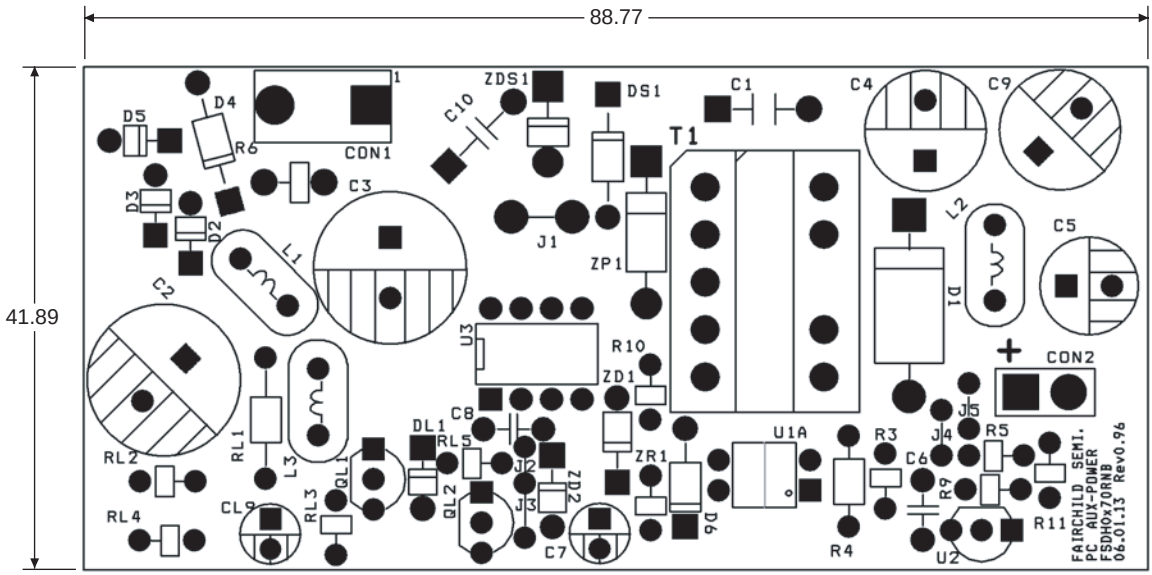
Bobbin: BE2229

6. Demo Circuit Part List

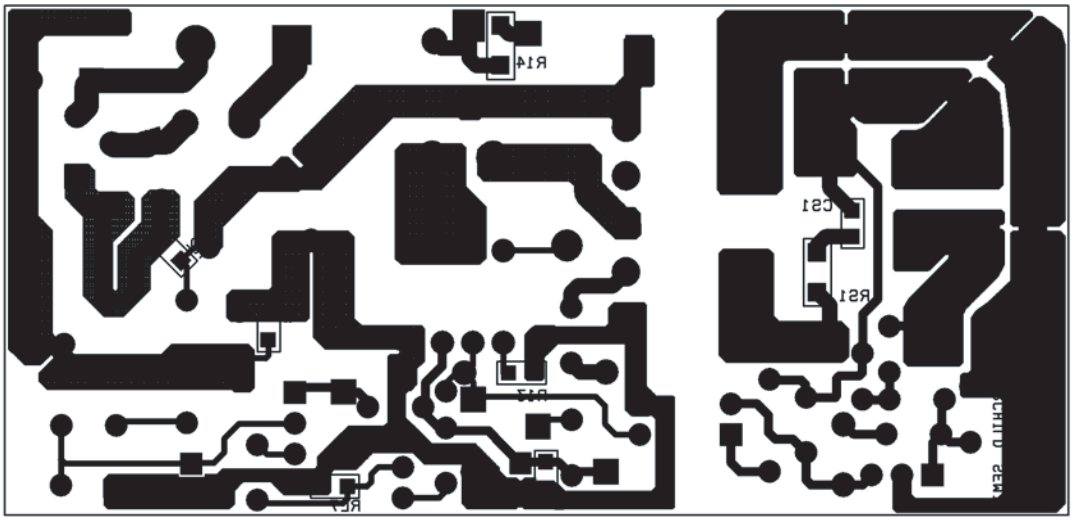
Part Number	Value	Quantity	Description (Manufacturer)
C6, C8	47nF	2	Ceramic Capacitor
C1	2nF (1KV)	1	Ceramic Capacitor
C10	1nF (200V)	1	Mylar Capacitor
CS1	1.5nF (50V)	1	SMD Ceramic Capacitor
C2, C3	22µF (400V)	2	Low Impedance Electrolytic Capacitor KMX series (Samyoung Elec.)
C4, C9	1000µF (16V)	2	Low ESR Electrolytic Capacitor NXC series (Samyoung Elec.)
C5	470µF (10V)	1	General Electrolytic Capacitor
C7	47µF (25V)	1	General Electrolytic Capacitor
CL9	10µF (50V)	1	General Electrolytic Capacitor
L1	330µH	1	Inductor
L2	5µH	1	Inductor
R6	2.4 (1W)	1	Fusible Resistor
J1, J2, J4	0	2	Jumper
R2	4.7k	1	Resistor
R3	560	1	Resistor
R4	100	1	Resistor
R5	1.2k	1	Resistor
R9	10k	1	Resistor
R10	4.7	1	Resistor
R14	30	1	Resistor
R11, RL3	1k	2	Resistor
RL1, RL2	1 Mega	2	Resistor
RL4	120k	1	Resistor
RL5	30k	1	Resistor
RL7	40k	1	Resistor
RS1	10	1	Resistor
ZR1	80	1	SMD Resistor
U1	PC817	1	IC (Fairchild Semiconductor)
U2	TL431	1	IC (Fairchild Semiconductor)
U3	FSDH0270RNB	1	IC (Fairchild Semiconductor)
QL1	2N2907	1	IC (Fairchild Semiconductor)
QL2	2N2222	1	IC (Fairchild Semiconductor)
D2, D3, D4, D5, D6, DS1	1N4007	6	Diode (Fairchild Semiconductor)
D1	SB540	1	Schottky Diode (Fairchild Semiconductor)
ZD1	1N4745	1	Zener Diode (Fairchild Semiconductor)
DL1	1N5233	1	Zener Diode (Fairchild Semiconductor)
ZP1	82V (1W)	1	Zener Diode (Fairchild Semiconductor)
ZDS1	P6KE180A	1	TVS (Fairchild Semiconductor)
T1	EE2229	1	PL-7 Core (Samwha Elec.)

7. Layout

7.1 Top image of PCB

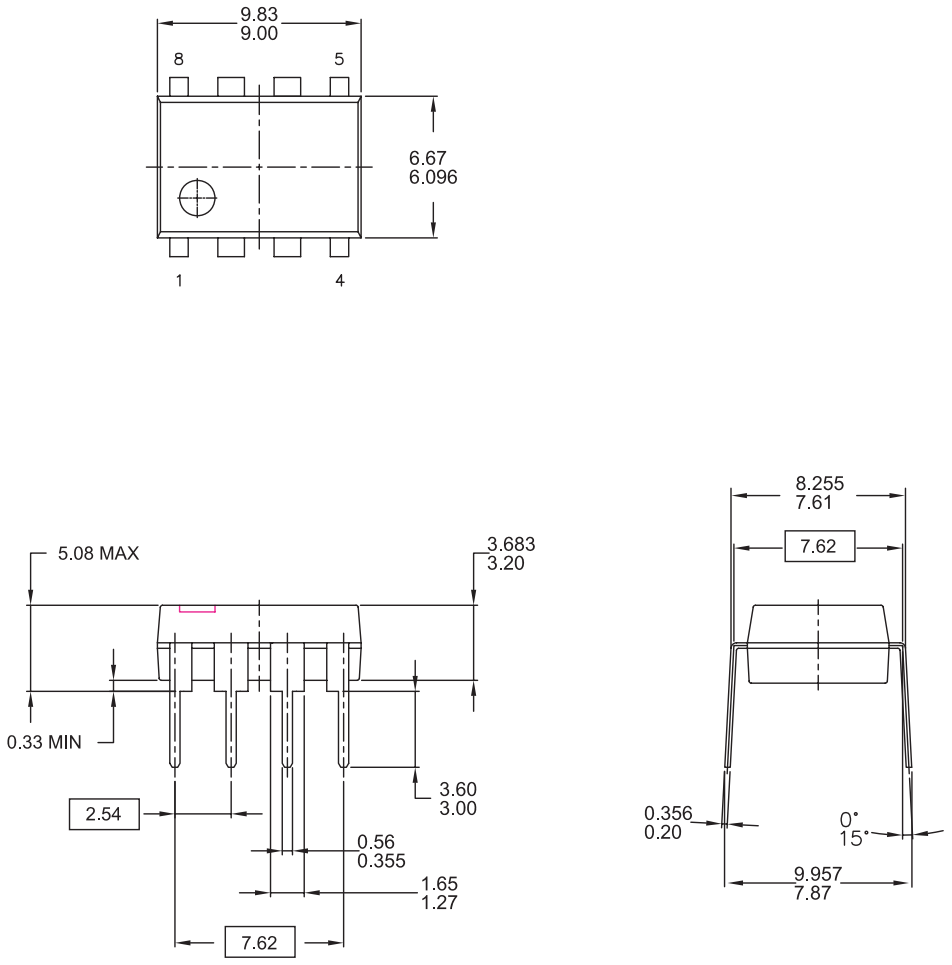


7.2 Bottom image of PCB



Package Dimensions

8-Pin DIP



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Programmable Active Droop™		Power247™	SuperFET™	
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