

1.5A Low-Dropout Linear Regulator with Programmable Sequencing

FEATURES

- 1.5A LDO Regulator with Programmable Sequencing
- Track and Power-Good (PG) Allows Three Types of Sequencing:
 - Simultaneous, Sequential, and Ratiometric
- Supports Input Voltages as Low as 0.9V
- Adjustable Output (0.8V to 3.3V)
- Ultra-Low Dropout: 60mV at 1.5A (typ)
- 1% Accuracy Over Line, Load, and Temperature
- Stable with Any or No Output Capacitor
- Active High Enable
- Open-Drain Power-Good (5 × 5 QFN)
- Available in 5mm × 5mm × 1mm QFN and DDPAK-7 Packages
- External BIAS Permits Low V_{IN} Operation with Excellent Transient Response

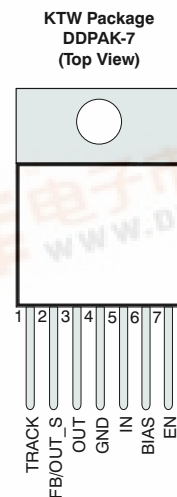
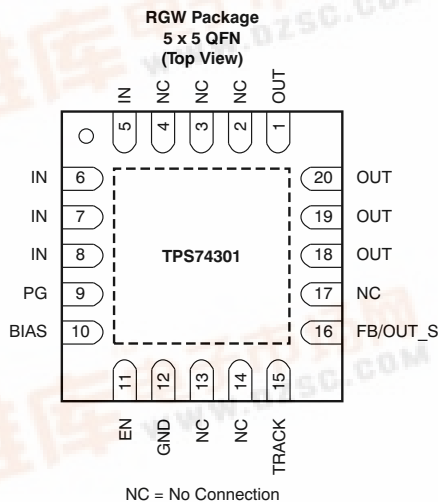
DESCRIPTION

The TPS74301 low dropout (LDO) linear regulator provides an easy-to-use power management solution for many high-current applications. The Track input allows user-programmed sequencing to minimize the voltage difference among supply rails during startup. The enable input (EN) and power-good (PG) outputs allow easy sequential sequencing with external regulators. This complete flexibility permits the user to configure a solution that will meet the sequencing requirements of FPGAs, DSPs, and other applications with special startup requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. The LDO regulator is stable with any or no output capacitor and is fully specified from -40°C to $+125^{\circ}\text{C}$. The TPS74301 is offered in a small 5mm × 5mm QFN package, yielding a highly compact total solution size. For applications that require additional power dissipation, the DDPAK (KTW) package is also available.

APPLICATIONS

- FPGA Applications
- DSP Core and I/O Voltages
- Post-Regulation Applications
- Applications with Special Start-up time Requirements



PRODUCT PREVIEW



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾	PACKAGE-LEAD	ORDERING NUMBER
TPS74301	Adjustable	5 × 5 QFN ⁽³⁾	TPS74301RGWT
			TPS74301RGWR
TPS74301	Adjustable	DDPAK-7 ⁽⁴⁾	TPS74301KTWT
			TPS74301KTWR

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Other output voltages are available, minimum order quantities may apply. See available output voltage options table for details; contact factory for availability.
- (3) The **T** suffix indicates 250-piece tape and reel; the **R** suffix indicates 3000-piece tape and reel quantities.
- (4) The **T** suffix indicates 50-piece tape and reel; the **R** suffix indicates 500-piece tape and reel quantities.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

At T_A = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

	TPS74301	UNIT
V _{IN} , V _{BIAS} Input voltage range	–0.3 to +6	V
V _{EN} Enable voltage range	–0.3 to +6 or V _{IN} + 0.3, whichever is greater	V
V _{PG} Power-good voltage range	–0.3 to +6	V
V _{OUT} Output voltage range	–0.3 to V _{IN}	V
I _{OUT} Maximum output current	Internally limited	
Output short circuit duration	Indefinite	
P _{DISS} Continuous total power dissipation	See Dissipation Ratings	
T _J Operating junction temperature range	–40 to +150	°C
T _{STG} Storage junction temperature range	–55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	θ _{JA}	θ _{JC}	T _A < +25°C POWER RATING	DERATING FACTOR ABOVE T _A = +25°C
RGW (QFN)	31.4°C/W	1.25°C/W	3.183W	0.0318W/°C
KTW (DDPAK)	TBD	TBD	TBD	TBD

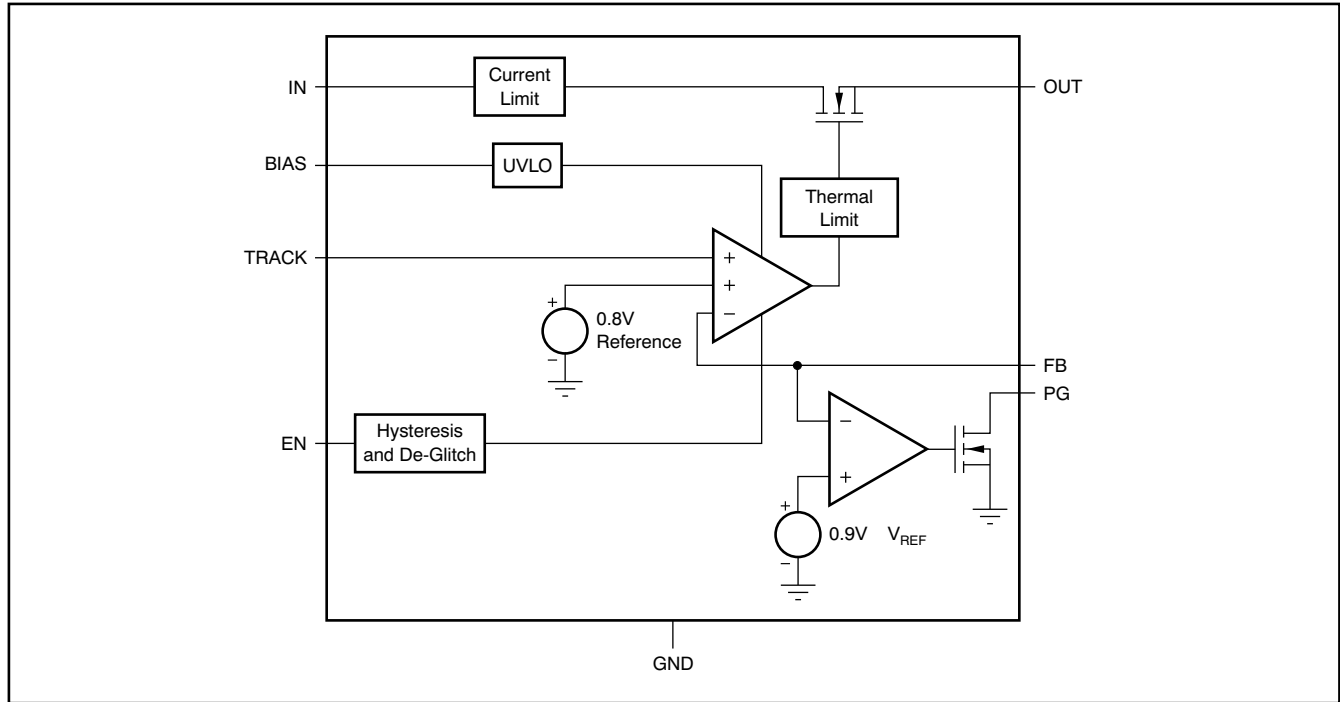
ELECTRICAL CHARACTERISTICS

 At $T_A = +25^\circ\text{C}$, $V_{EN} = 1.1\text{V}$, $V_{IN} = V_{OUT} + 0.3\text{V}$, $C_{IN} = C_{BIAS} = 0.1\mu\text{F}$, $C_{OUT} = 10\mu\text{F}$, $I_{OUT} = 50\text{mA}$, $V_{BIAS} = 3.3\text{V}$, and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS74301			UNIT
			MIN	TYP	MAX	
V_{IN}	Input Voltage Range		$V_{OUT(NOM)} + V_{DO(MAX)}$		5.5	V
V_{REF}	Internal Reference (Adj.)		0.796	0.8	0.804	V
V_{BIAS}	Bias Pin Voltage Range ⁽¹⁾		2.375		5.5	V
V_{OUT}	Output Voltage Range	$V_{IN} = V_{OUT} + 1\text{V}$, $I_{OUT} = 1.5\text{A}$, $V_{BIAS} = 5\text{V}$	V_{REF}		3.3	V
	Accuracy	Nominal, $T_J = +25^\circ\text{C}$	-0.5		+0.5	%
		$2.97\text{V} \leq V_{BIAS} \leq 5.5\text{V}$, $50\text{mA} \leq I_{OUT} \leq 1.5\text{A}$	-1	± 0.5	1	
V_{OUT}/V_{IN}	Line Regulation	$V_{OUT(NOM)} + 0.3 < V_{IN} < 5.5\text{V}$		TBD	TBD	%/V
V_{OUT}/I_{OUT}	Load Regulation	$50\text{mA} \leq I_{OUT} \leq 1.5\text{A}$		TBD	TBD	%/A
V_{DO}	Dropout Voltage (External Bias)	$I_{OUT} = 1.5\text{A}$, $V_{BIAS} - V_{OUT(NOM)} \geq 1.62\text{V}$, QFN		60	110	mV
		$I_{OUT} = 1.5\text{A}$, $V_{BIAS} - V_{OUT(NOM)} \geq 1.62\text{V}$, DDPK		70	160	mV
	Dropout Voltage ($V_{IN} = V_{BIAS}$)	$I_{OUT} = 1.5\text{A}$			1.4	V
I_{BIAS}	Bias Pin Current	$I_{OUT} = 0\text{mA}$ to 1.5A		3	5	mA
I_{SHDN}	Shutdown Supply Current (IN)	$V_{EN} \leq 0.4\text{V}$, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$		50	100	μA
I_{CL1}	Current Limit	$V_{OUT} = 90\% \times V_{OUT(NOM)}$	2.1		3.5	A
I_{FB}	Feedback Pin Current			10	200	nA
PSRR	Power-Supply Rejection (V_{IN} to V_{OUT})	1kHz, $I_{OUT} = 1.5\text{A}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 1.5\text{V}$, $V_{BIAS} = 3.3\text{V}$, $C_{OUT} = 10\mu\text{F}$		60		dB
		300kHz, $I_{OUT} = 1.5\text{A}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 1.5\text{V}$, $V_{BIAS} = 3.3\text{V}$, $C_{OUT} = 10\mu\text{F}$		30		
	Power-Supply Rejection (V_{BIAS} to V_{OUT})	1kHz, $I_{OUT} = 1.5\text{A}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 1.5\text{V}$, $V_{BIAS} = 3.3\text{V}$, $C_{OUT} = 10\mu\text{F}$		50		dB
		300kHz, $I_{OUT} = 1.5\text{A}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 1.5\text{V}$, $V_{BIAS} = 3.3\text{V}$, $C_{OUT} = 10\mu\text{F}$		30		
Noise	Output Noise Voltage	100Hz to 100kHz, $I_{OUT} = 1.5\text{A}$		$35 \times V_{OUT}$		μV_{RMS}
t_{STR}	Minimum Startup Time	$I_{OUT} = 1.5\text{A}$		100		μs
V_{TRACK}	Tracking Voltage Accuracy	$V_{TRACK} = 0.4\text{V}$		5	20	mV
$V_{EN, HI}$	Enable Input High Level		1.1		V_{BIAS}	V
$V_{EN, LO}$	Enable Input Low Level		0		0.4	V
V_{ENHYS}	Enable Pin Hysteresis			50		mV
V_{ENDG}	Enable Pin De-Glitch Time			20		μs
I_{EN}	Enable Pin Current	$V_{EN} = 5\text{V}$		0.1	1.0	μA
V_{IT}	PG Trip Threshold	V_{OUT} Decreasing	88	90	92	$\%V_{OUT}$
V_{HYS}	PG Trip Hysteresis			3		$\%V_{OUT}$
$V_{PG, LO}$	PG Output Low Voltage	$I_{PG} = 1\text{mA}$ (sinking), $V_{OUT} < V_{IT}$, $2.375\text{V} \leq V_{BIAS} \leq 5.5\text{V}$			0.3	V
$I_{PG, LKG}$	PG Leakage Current	$V_{PG} = 5\text{V}$, $V_{OUT} > V_{IT}$		0.1	1.0	μA
T_J	Operating Junction Temperature		-40		+125	$^\circ\text{C}$
T_{SD}	Thermal Shutdown Temperature	Shutdown, Temperature Increasing		+165		$^\circ\text{C}$
		Reset, Temperature Decreasing		+140		

 (1) Minimum $V_{BIAS} = 2.375\text{V}$ or $V_{OUT} + V_{DO}$, whichever is greater.

BLOCK DIAGRAM



PIN DESCRIPTIONS

NAME	KTW (DDPAK)	RGW (QFN)	DESCRIPTION
IN	5	5-8	Unregulated input to the device.
EN	7	11	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
TRACK	1	15	Voltage tracking pin. The internal reference will track this voltage when it is below 0.8V.
BIAS	6	10	Bias voltage for error amplifier, reference, and internal control circuits.
PG	NA	9	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT} . When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, which would allow the PG output to attain voltages higher than V_{IN} .
FB	2	16	This pin is the feedback connection to an external resistor divider network that sets the output voltage.
OUT	3	1, 18-20	Regulated output voltage.
NC	NA	2-4, 13, 14, 17	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
PAD/TAB			Electrically isolated. Should be soldered to ground plane for heat sinking.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS74301KTWR	PREVIEW	DDPAK	KTW	7	1000	TBD	Call TI	Call TI
TPS74301KTWT	PREVIEW	DDPAK	KTW	7	50	TBD	Call TI	Call TI
TPS74301RGWR	PREVIEW	QFN	RGW	20	3000	TBD	Call TI	Call TI
TPS74301RGWT	PREVIEW	QFN	RGW	20	250	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

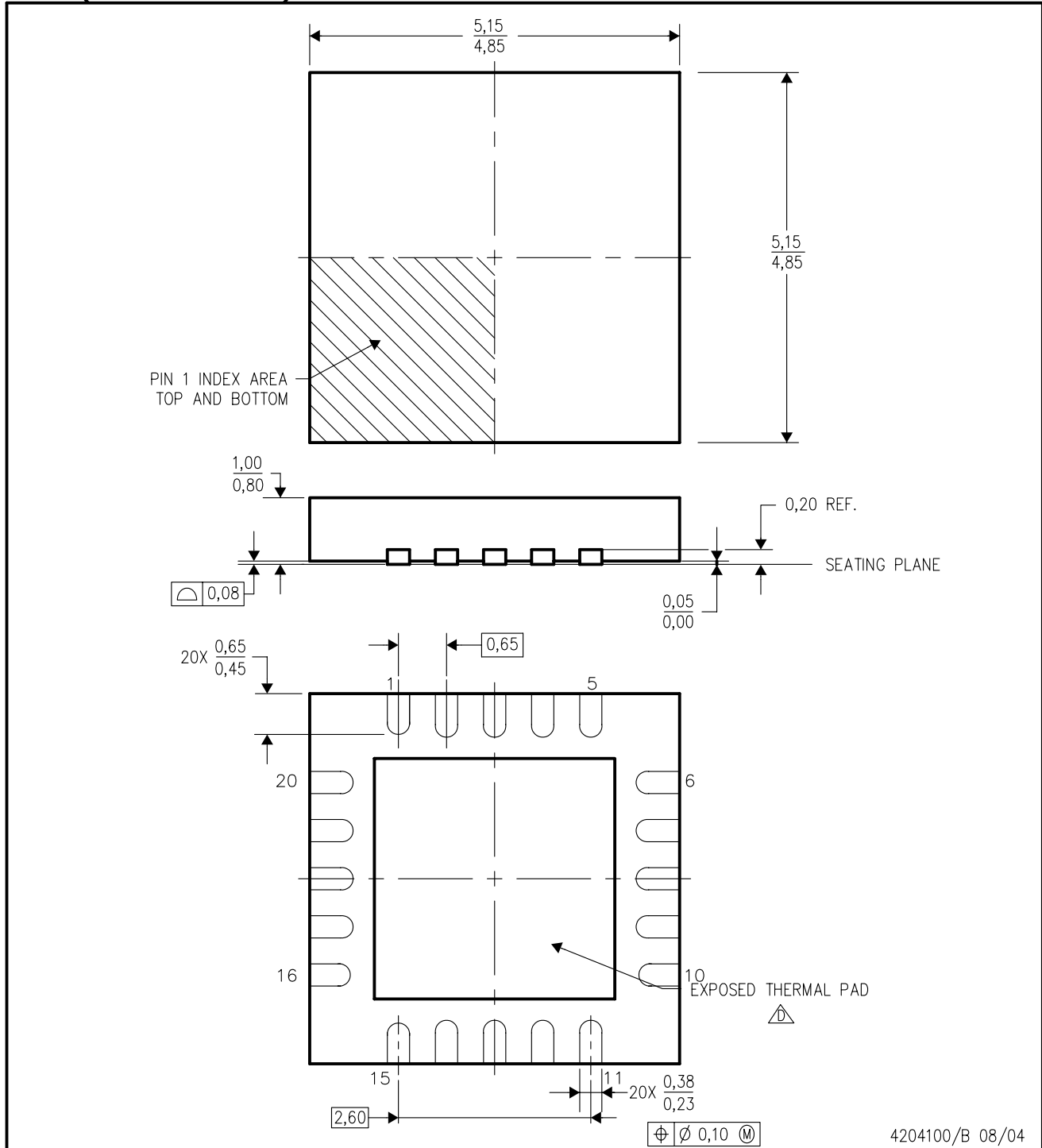
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MECHANICAL DATA

RGW (S-PQFP-N20)

PLASTIC QUAD FLATPACK



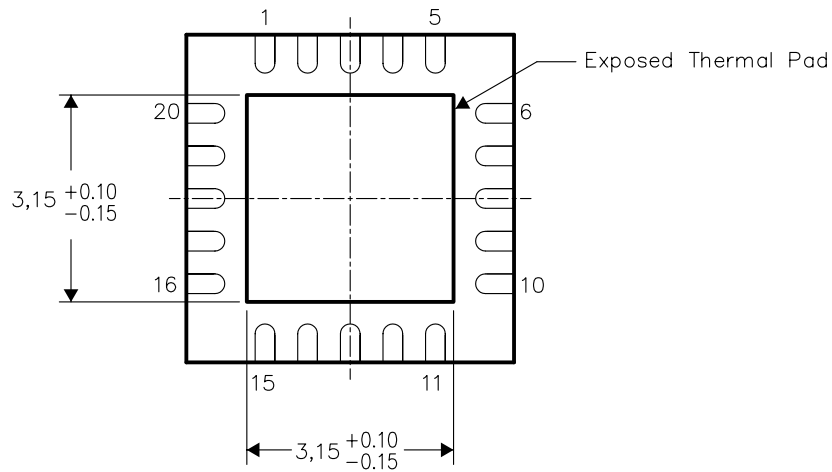
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flat pack, No-leads (QFN) package configuration
 - △ The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

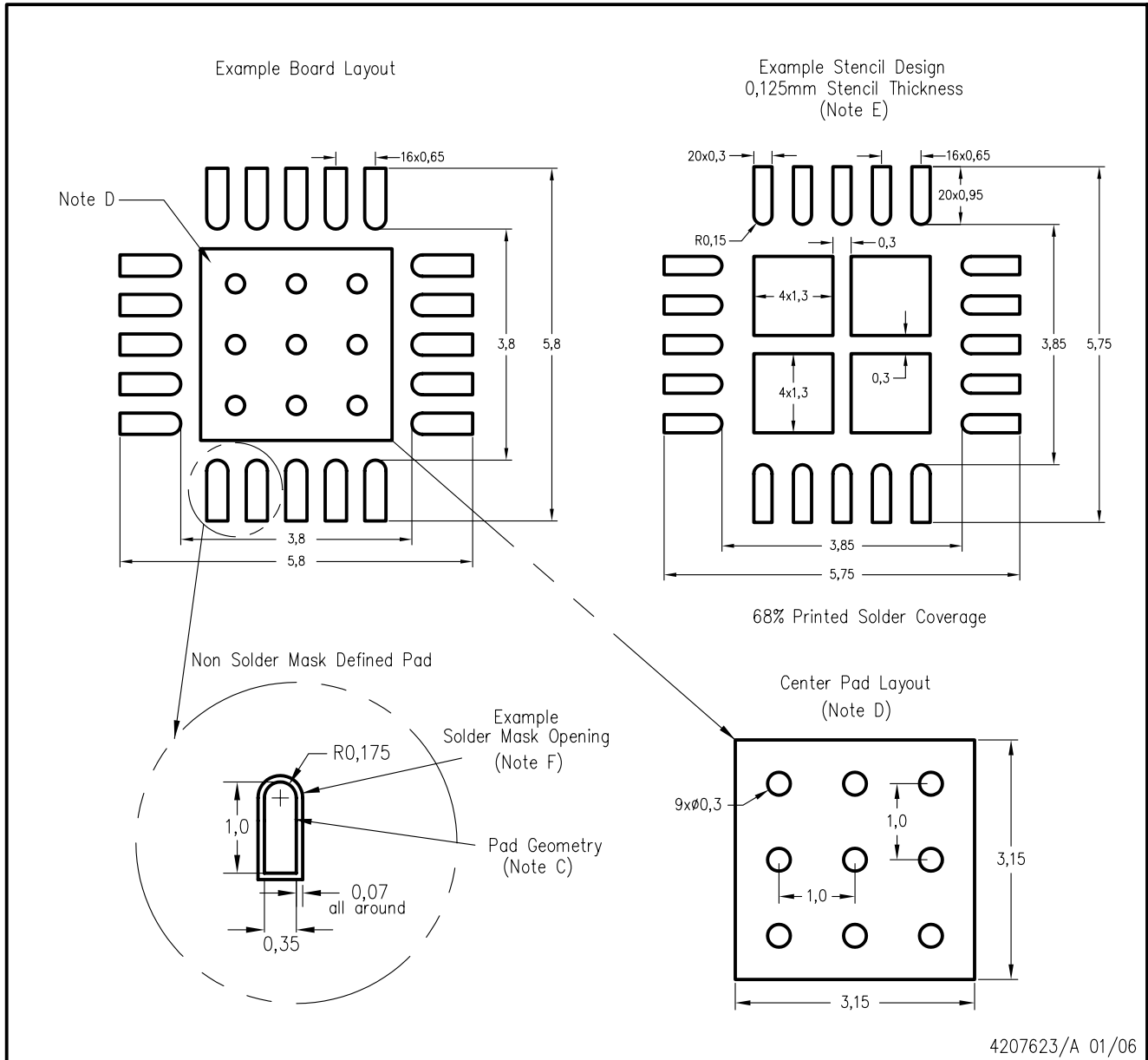


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGW (S-PQFP-N20)



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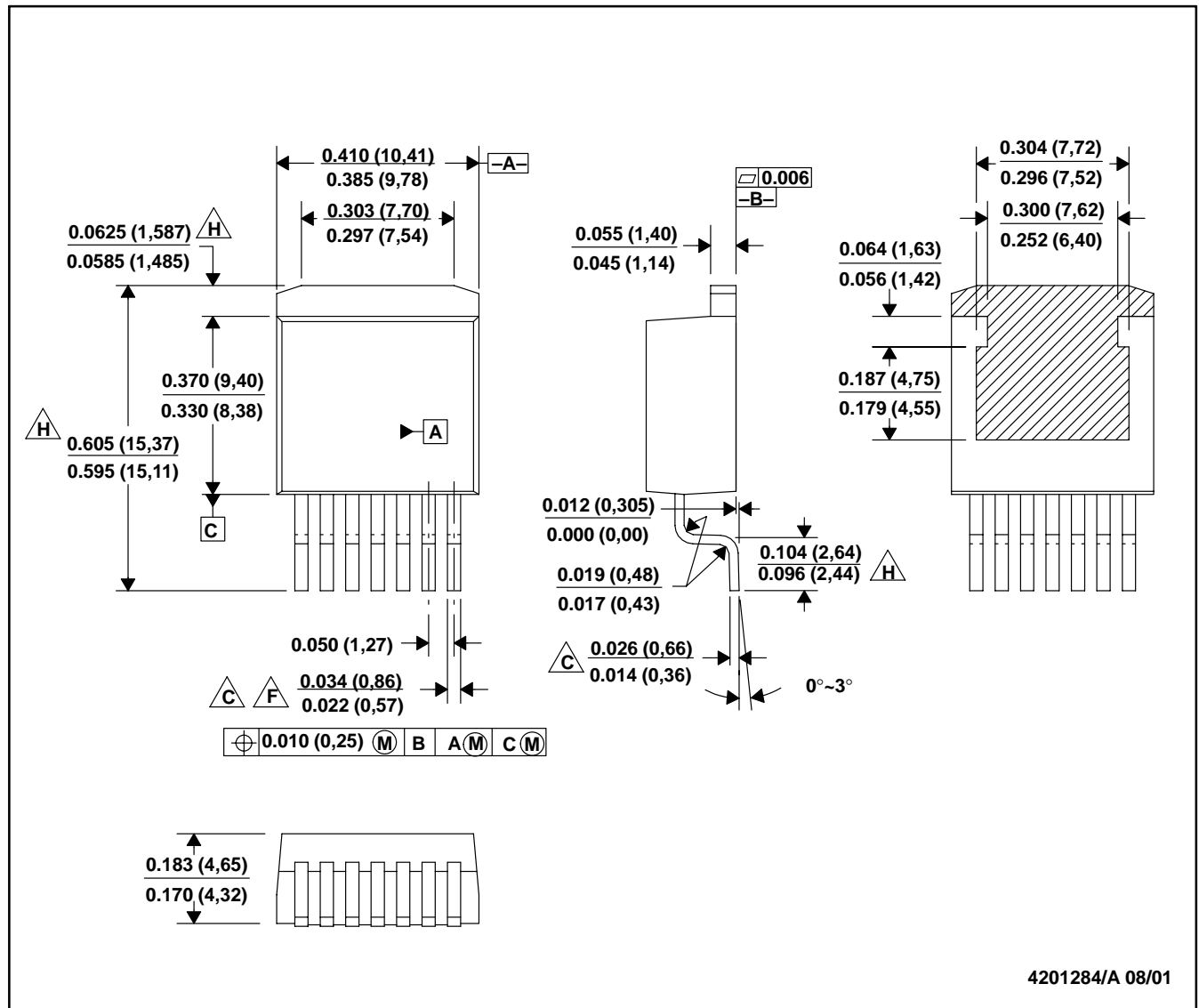
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

MECHANICAL DATA

MPSF015 – AUGUST 2001

KTW (R-PSFM-G7)

PLASTIC FLANGE-MOUNT



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Lead width and height dimensions apply to the plated lead.
 D. Leads are not allowed above the Datum B.
 E. Stand-off height is measured from lead tip with reference to Datum B.
 F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003".
 G. Cross-hatch indicates exposed metal surface.
 H. Falls within JEDEC MO-169 with the exception of the dimensions indicated.

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