

Dual 250 mA Output, UltraLow Noise, High PSRR, Low-Dropout Linear Regulator

FEATURES

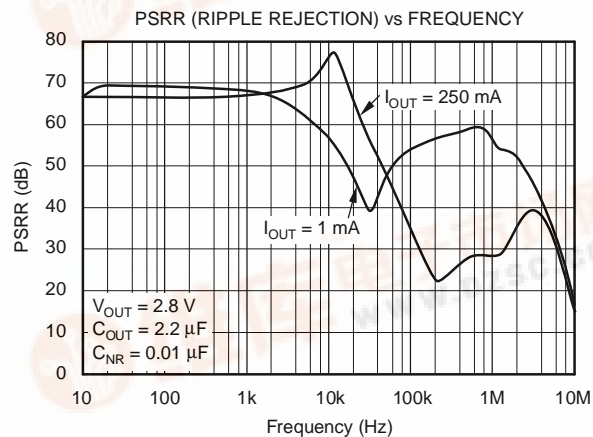
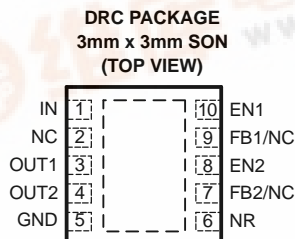
- Dual 250 mA High-Performance RF LDOs
- Available in Fixed and Adjustable Voltage Options (1.2 V to 5.5 V)
- High PSRR: 65 dB at 10 kHz
- UltraLow Noise: 32 μ Vrms
- Fast Start-Up Time: 60 μ s
- Stable with 2.2 μ F Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage: 125 mV at 250 mA
- Independent Enable Pins
- Thermal Shutdown and Independent Current Limit
- Available in Thermally-Enhanced SON Package: 3mm x 3mm x 1mm

APPLICATIONS

- Cellular and Cordless Phones
- Wireless PDA/Handheld Products
- PCMCIA/Wireless LAN Applications
- Digital Camera/Camcorder/Internet Audio
- DSP/FPGA/ASIC/Controllers and Processors

DESCRIPTION

The TPS712xx family of low-dropout (LDO) voltage regulators is tailored to noise-sensitive and RF applications. These products feature dual 250 mA LDOs with ultralow noise, high power-supply rejection ratio (PSRR), and fast transient and start-up response. Each regulator output is stable with low-cost 2.2 μ F ceramic output capacitors and features very low dropout voltages (125 mV typical at 250 mA). Each regulator achieves fast start-up times (approximately 60 μ s with a 0.001 μ F bypass capacitor) while consuming very low quiescent current (300 μ A typical with both outputs enabled). When the device is placed in standby mode, the supply current is reduced to less than 0.3 μ A typical. Each regulator exhibits approximately 32 μ Vrms of output voltage noise with $V_{OUT} = 2.8$ V and a 0.01 μ F noise reduction (NR) capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, will benefit from high PSRR, low noise, and fast line and load transient features. The TPS712 family is offered in a thin 3mm x 3mm SON package and is fully specified from -40°C to +125°C (T_J).





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | VOLTAGE (T _J) | | PACKAGE-LEAD DESIGNATOR | SPECIFIED TEMPERATURE RANGE (T _J) | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|----------|---------------------------|-------------------|-------------------------|---|-----------------|-----------------|---------------------------|
| | V _{OUT1} | V _{OUT2} | | | | | |
| TPS71202 | Adjustable | Adjustable | SON-10 (DRC) | -40°C to +125°C | ARQ | TPS71202DRCT | Tape and Reel, 250 |
| | | | | | | TPS71202DRCR | Tape and Reel, 3000 |
| TPS71219 | 1.8 V | Adjustable | SON-10 (DRC) | -40°C to +125°C | ARW | TPS71219DRCT | Tape and Reel, 250 |
| | | | | | | TPS71219DRCR | Tape and Reel, 3000 |
| TPS71229 | 2.8 V | Adjustable | SON-10 (DRC) | -40°C to +125°C | ARU | TPS71229DRCT | Tape and Reel, 250 |
| | | | | | | TPS71229DRCR | Tape and Reel, 3000 |
| TPS71247 | 1.8 V | 2.85 V | SON-10 (DRC) | -40°C to +125°C | ARS | TPS71247DRCT | Tape and Reel, 250 |
| | | | | | | TPS71247DRCR | Tape and Reel, 3000 |
| TPS71256 | 2.8 V | 2.8 V | SON-10 (DRC) | -40°C to +125°C | ARV | TPS71256DRCT | Tape and Reel, 250 |
| | | | | | | TPS71256DRCR | Tape and Reel, 3000 |
| TPS71257 | 2.85 V | 2.85 V | SON-10 (DRC) | -40°C to +125°C | ART | TPS71257DRCT | Tape and Reel, 250 |
| | | | | | | TPS71257DRCR | Tape and Reel, 3000 |

(1) For the most current package and ordering information, see the Package Ordering Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted⁽¹⁾

| | TPS712xx | UNIT |
|--|-------------------------------|------|
| V _{IN} range | -0.3 to 6.0 | V |
| V _{EN1} , V _{EN2} range | -0.3 to V _{IN} + 0.3 | V |
| V _{OUT} range | -0.3 to 6.0 | V |
| Peak output current | Internally limited | |
| Output short-circuit duration | Indefinite | |
| Continuous total power dissipation | See Dissipation Ratings Table | |
| Junction temperature range, T _J | -40 to +150 | °C |
| Storage temperature range | -65 to +150 | °C |
| ESD rating, HBM | 2 | kV |
| ESD rating, CDM | 500 | V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

| BOARD | PACKAGE | R _{θJC} | R _{θJA} | DERATING FACTOR ABOVE T _A = 25°C | T _A ≤ 25°C POWER RATING | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|-----------------------|---------|------------------|------------------|---|------------------------------------|------------------------------------|------------------------------------|
| High-K ⁽¹⁾ | DRC | 48 | 52 | 19 mW/°C | 1.92 W | 1.06 W | 0.77 W |

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), V_{IN} = highest $V_{OUT(nom)} + 1.0$ V or 2.7 V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN1, 2} = 1.2$ V, $C_{OUT} = 10$ μF , $C_{NR} = 0.01$ μF , and adjustable LDOs are tested at $V_{OUT} = 3.0$ V, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

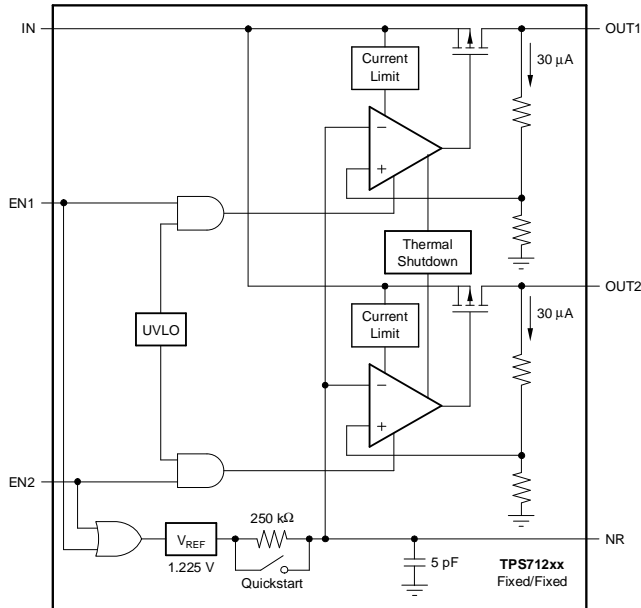
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|---|----------|-----------------------|----------|------------------|
| V_{IN} | Input voltage range ⁽¹⁾ | | 2.7 | | 5.5 | V |
| V_{FB} | Internal reference (adjustable LDOs) | | 1.200 | 1.225 | 1.250 | V |
| V_{OUT} | Output voltage range (adjustable LDOs) | | V_{FB} | 5.5 - V_{DO} | | V |
| | Accuracy ⁽¹⁾ | Nominal $T_J = 25^\circ\text{C}$, $I_{OUT} = 0$ mA Over V_{IN} , I_{OUT} , and T $V_{OUT} + 1.0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$, $0 \mu\text{A} \leq I_{OUT} \leq 250 \text{ mA}$ | -1.5 | ± 1 | +1.5 | % |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation ⁽¹⁾ | $V_{OUT} + 1.0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$ | | 0.05 | | %/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $0 \mu\text{A} \leq I_{OUT} \leq 250 \text{ mA}$ | | 0.8 | | %/mA |
| V_{DO} | Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{V}$) | 2.8 V, 2.85 V Adjustable $I_{OUT1} = I_{OUT2} = 250 \text{ mA}$ | | 125 | 230 | mV |
| I_{CL} | Output current limit | $V_{OUT} = 0.9 \times V_{OUT(nom)}$ | 400 | 600 | 800 | mA |
| I_{GND} | Ground pin current | One LDO enabled $I_{OUT} = 1$ mA (enabled channel) | | 190 | 250 | μA |
| | | Both LDOs enabled $I_{OUT1} = I_{OUT2} = 1$ mA to 250 mA | | 300 | 600 | |
| I_{SHDN} | Shutdown current ⁽³⁾ | $V_{EN} \leq 0.4 \text{ V}$, $0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$ | | 0.3 | 2.0 | μA |
| I_{FB} | FB pin current (adjustable LDOs) | | | 0.1 | 1 | μA |
| V_n | Output noise voltage, BW = 10 Hz - 100 kHz | No C_{NR} , $I_{OUT} = 250$ mA | | $80.0 \times V_{OUT}$ | | μVrms |
| | | $C_{NR} = 0.01$ μF , $I_{OUT} = 250$ mA | | $11.8 \times V_{OUT}$ | | |
| PSRR | Power-supply rejection ratio (ripple rejection) | $f = 100$ Hz, $I_{OUT} = 250$ mA | | 65 | | dB |
| | | $f = 10$ kHz, $I_{OUT} = 250$ mA | | 65 | | |
| t_{STR} | Startup time | $V_{OUT} = 2.85 \text{ V}$, $R_L = 30\Omega$, $C_{NR} = 0.001$ μF | | 60 | | μs |
| V_{IH} | Enable threshold high (EN1, EN2) | | 1.2 | | V_{IN} | V |
| V_{IL} | Enable threshold low (EN1, EN2) | | 0 | | 0.4 | V |
| I_{EN} | Enable pin current (EN1, EN2) | $V_{IN} = V_{EN} = 5.5 \text{ V}$ | -1 | | 1 | μA |
| T_{SD} | Thermal shutdown temperature | Shutdown Temp increasing | | +160 | | $^\circ\text{C}$ |
| | | Reset Temp decreasing | | +140 | | |
| UVLO | Undervoltage lockout threshold | V_{IN} rising | 2.25 | | 2.65 | V |
| | Undervoltage lockout hysteresis | V_{IN} falling | | 100 | | mV |

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.

(2) V_{DO} is not measured for 1.8 V regulators since minimum $V_{IN} = 2.7$ V.

(3) For the adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions from high to low.

**FUNCTIONAL BLOCK DIAGRAM —
FIXED VERSION**



**FUNCTIONAL BLOCK DIAGRAM —
ADJUSTABLE VERSION**

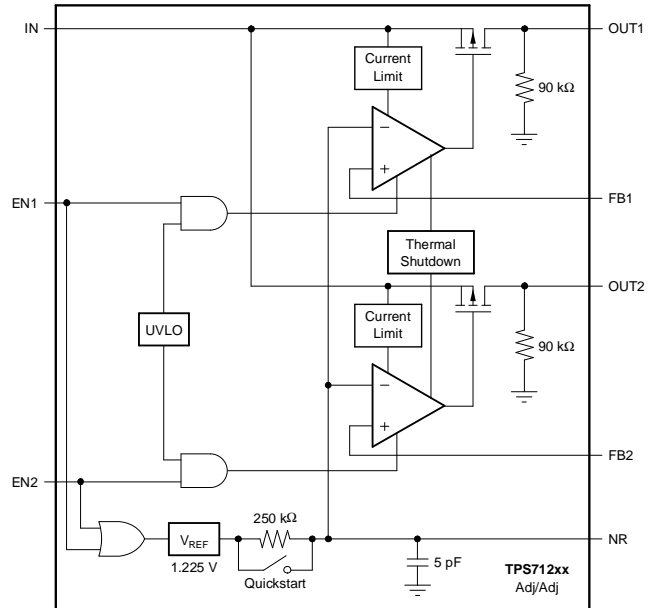


Table 1. TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|----------|--------|--|
| NAME | DRC | |
| IN | 1 | Unregulated input supply. A small 0.1 µF capacitor should be connected from IN to GND. |
| GND | 5, Pad | Ground |
| OUT1 | 3 | Output of the regulator. A small 2.2 µF ceramic capacitor is required from this pin to ground to assure stability. |
| OUT2 | 4 | Same as OUT1 but for LDO2. |
| EN1 | 10 | Driving the enable pin (EN) high turns on LDO1. Driving this pin low puts LDO1 into shutdown mode, reducing operating current. The enable pin should be connected to IN if not used. |
| EN2 | 8 | Same as EN1 but controls LDO2. |
| FB1/NC | 9 | Feedback for CH1 adjustable version; no connection for non-adjustable CH1. |
| FB2/NC | 7 | Feedback for CH2 adjustable version; no connection for non-adjustable CH2. |
| NR | 6 | Noise reduction pin; connect an external bypass capacitor to reduce LDO output noise. |
| NC | 2 | No connection. |

TYPICAL CHARACTERISTICS

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 1.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $C_{NR} = 0.01\text{ }\mu\text{F}$, unless otherwise noted.

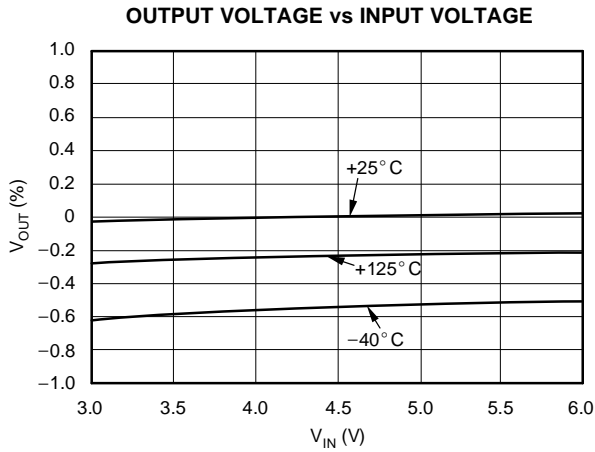


Figure 1.

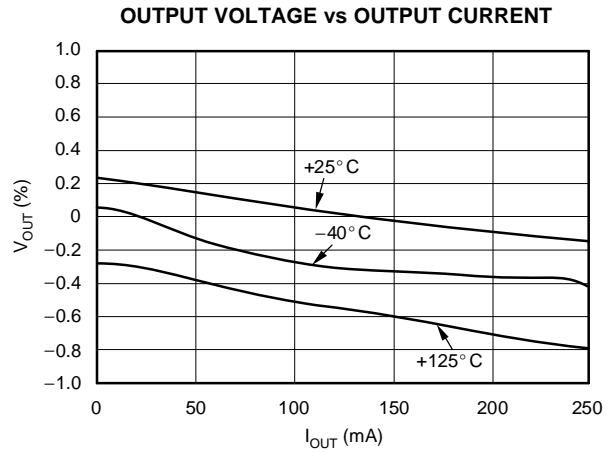


Figure 2.

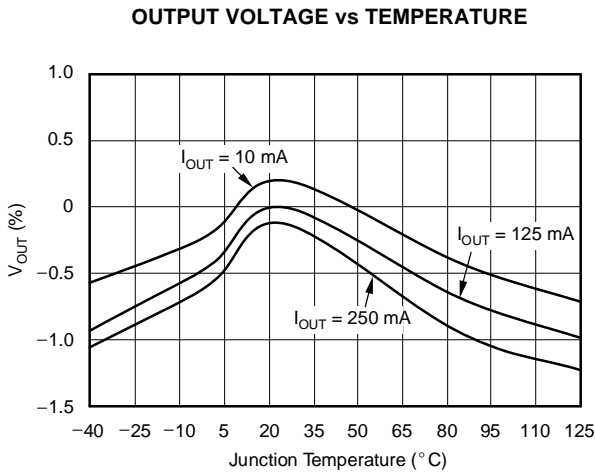


Figure 3.

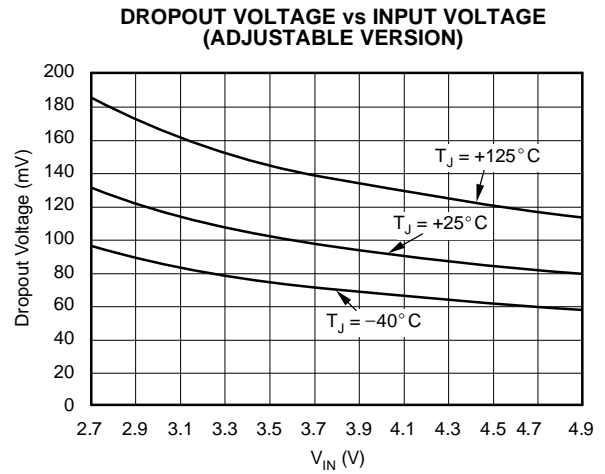


Figure 4.

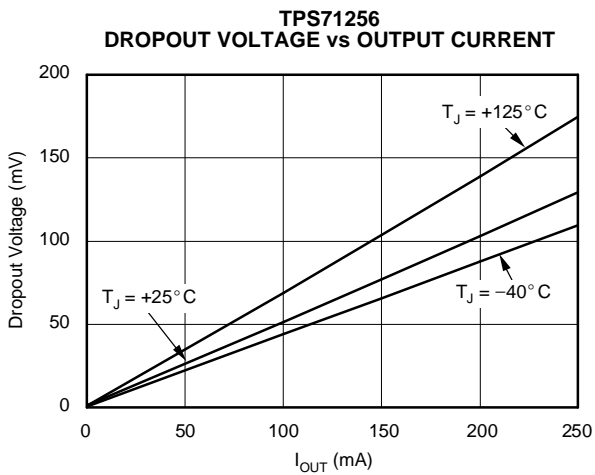


Figure 5.

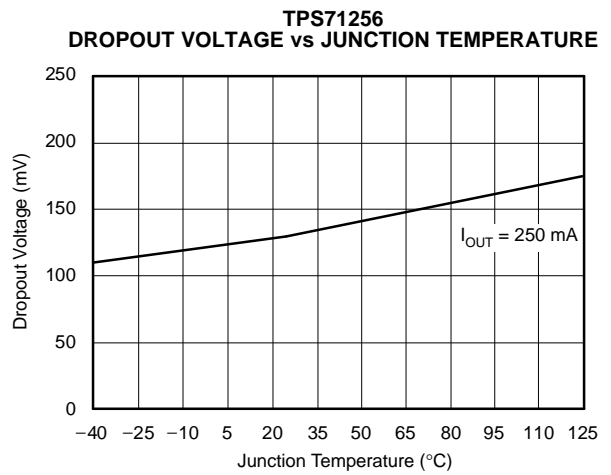


Figure 6.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 1.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $C_{NR} = 0.01\text{ }\mu\text{F}$, unless otherwise noted.

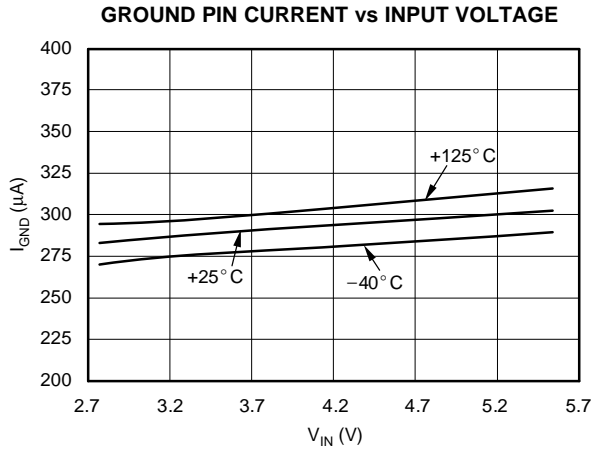


Figure 7.

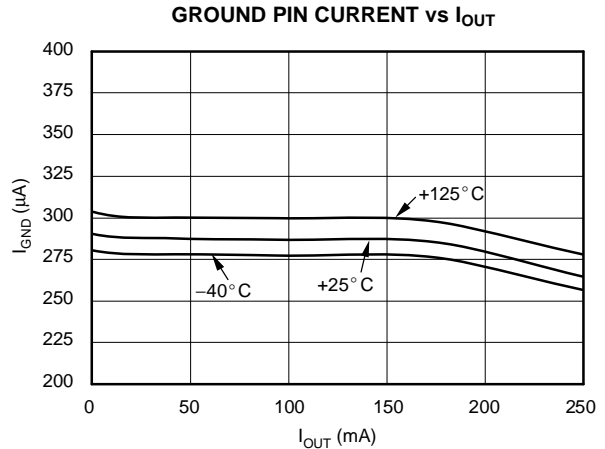


Figure 8.

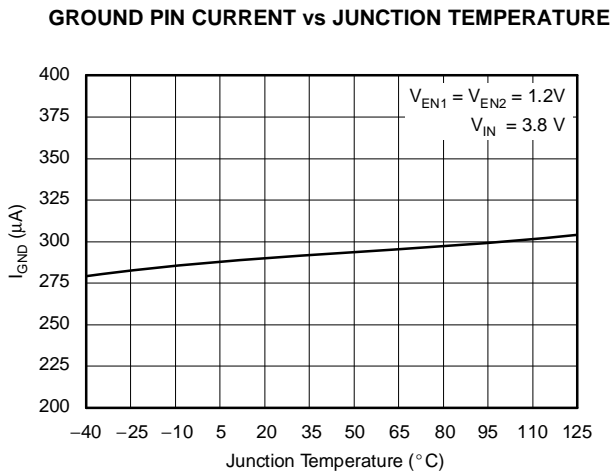


Figure 9.

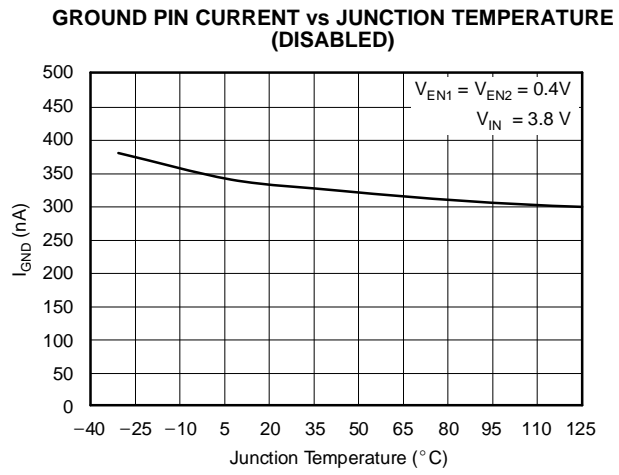


Figure 10.

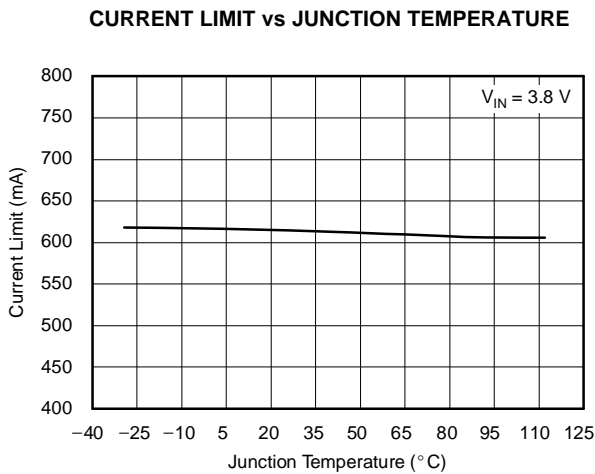


Figure 11.

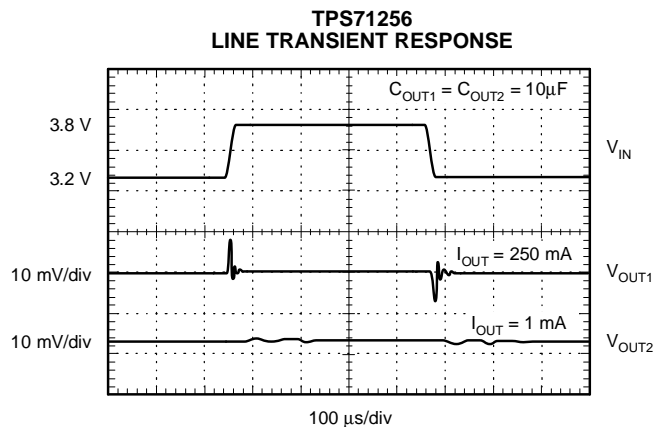


Figure 12.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 1.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $C_{NR} = 0.01\text{ }\mu\text{F}$, unless otherwise noted.

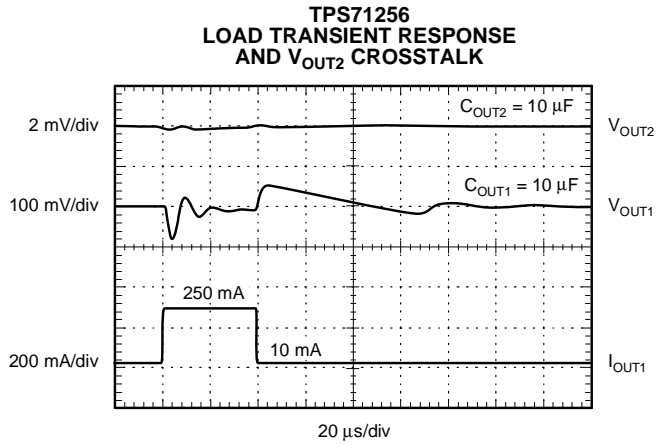


Figure 13.

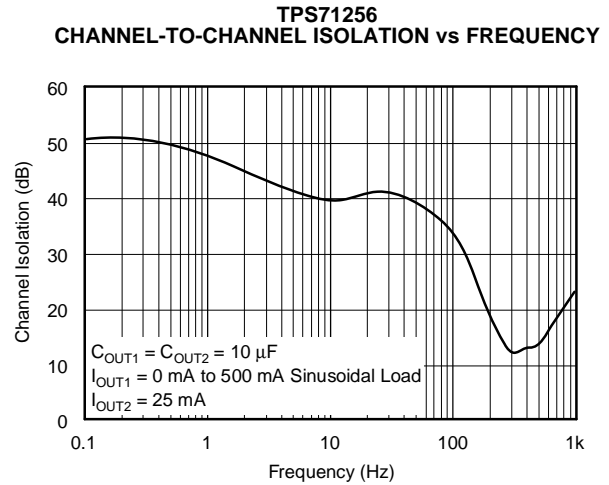


Figure 14.

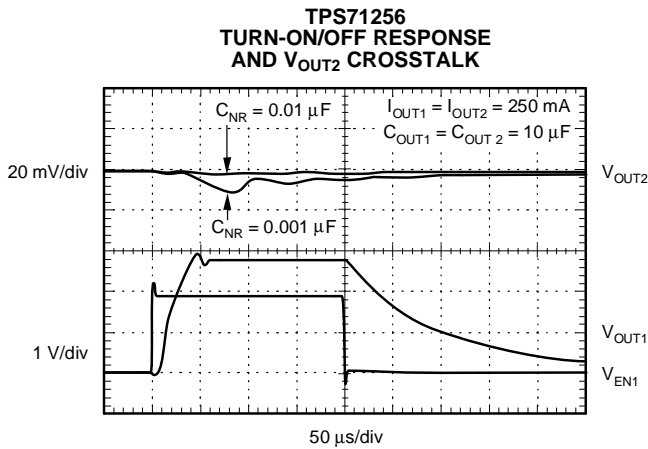


Figure 15.

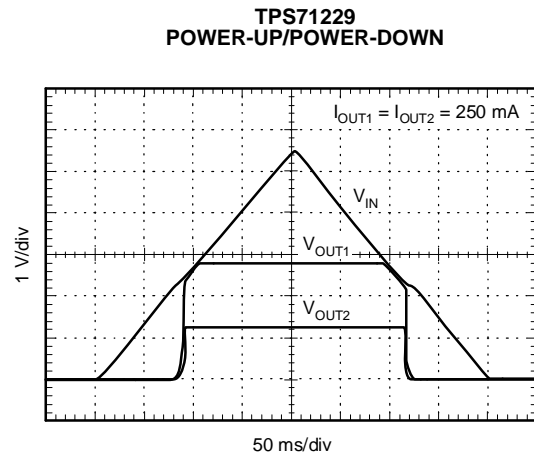


Figure 16.

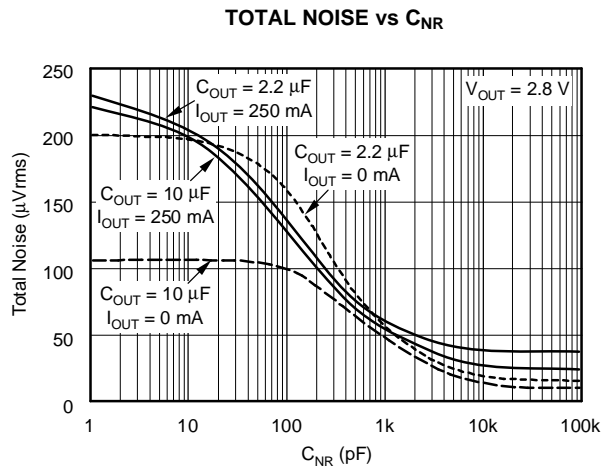


Figure 17.

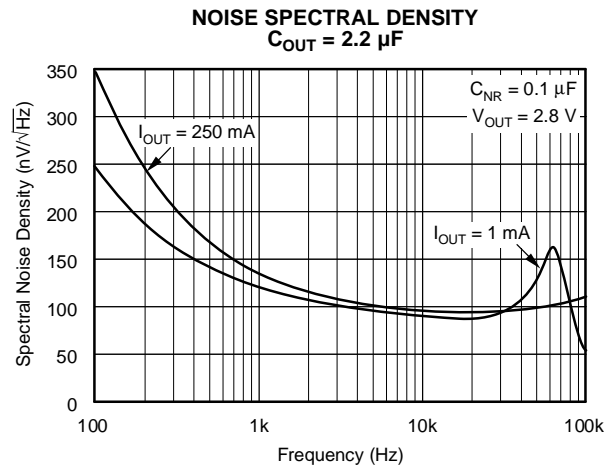


Figure 18.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{EN} = 1.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $C_{NR} = 0.01\text{ }\mu\text{F}$, unless otherwise noted.

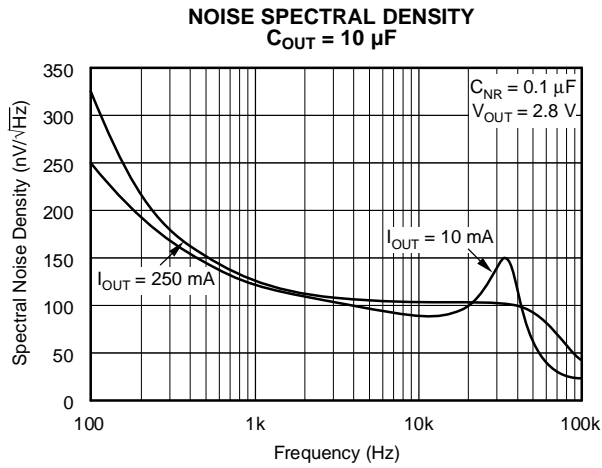


Figure 19.

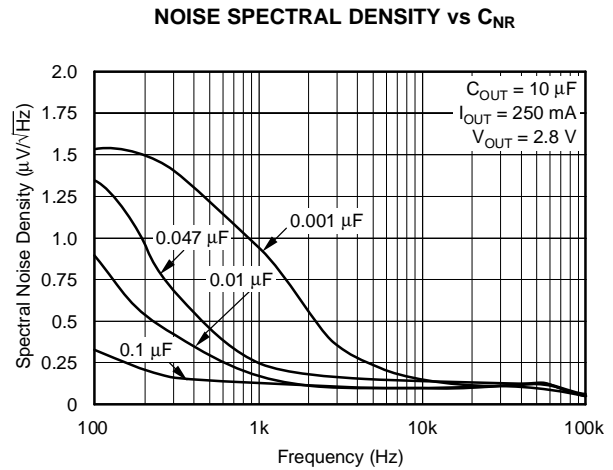


Figure 20.

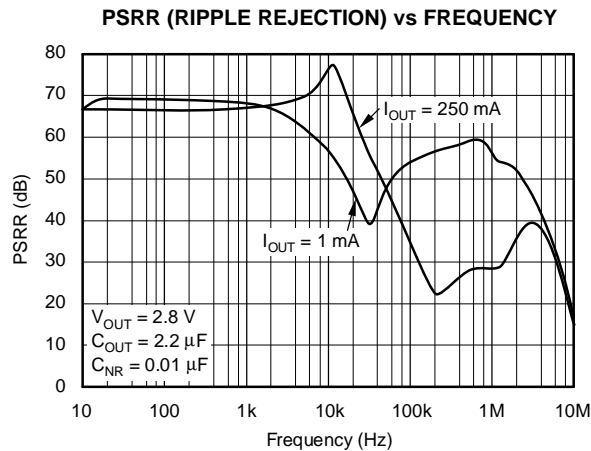


Figure 21.

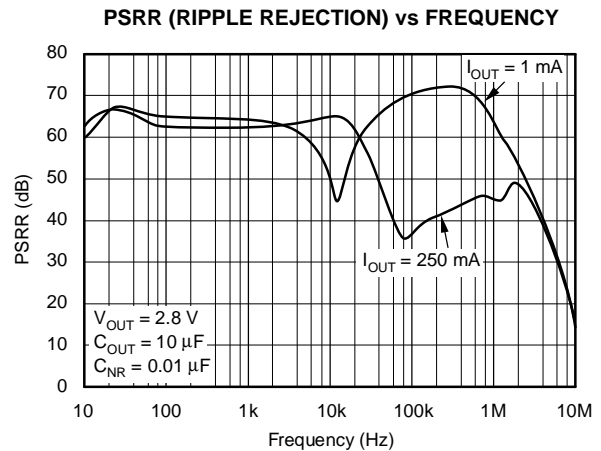


Figure 22.

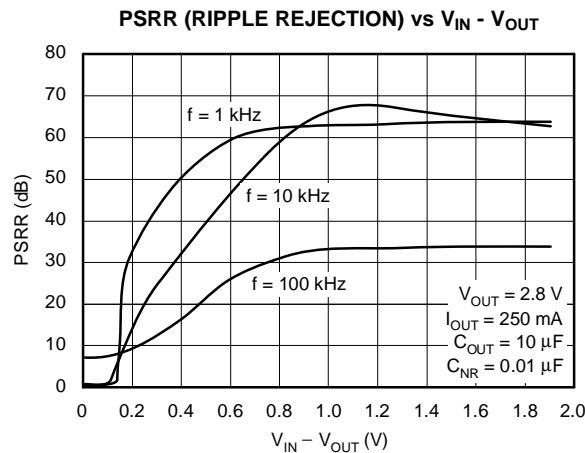


Figure 23.

APPLICATION INFORMATION

The TPS712xx family of dual low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout, high PSRR, ultralow output noise, and low quiescent current (190 μ A typical per channel). When both outputs are disabled, the supply currents are reduced to less than 2 μ A. A typical application circuit is shown in Figure 24.

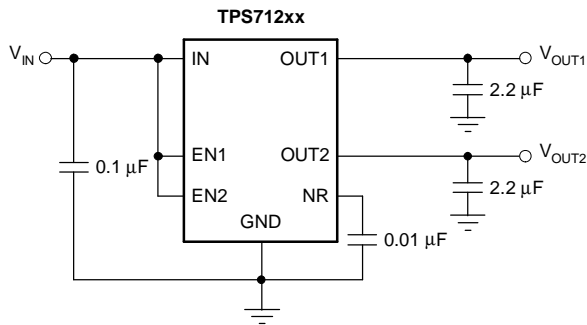


Figure 24. Typical Application Circuit (fixed-voltage versions)

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

A 0.1 μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS712xx, is required for stability. It improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS712xx requires an output capacitor connected between the outputs and GND to stabilize the internal control loops. The minimum recommended output capacitor is 2.2 μ F. If an output voltage of

1.8 V or less is chosen, the minimum recommended output capacitor is 4.7 μ F. Any ceramic capacitor that meets the minimum output capacitor requirements is suitable. Capacitors with higher ESR may be used, provided the ESR is less than 1 Ω .

OUTPUT NOISE

The internal voltage reference is a key source of noise in an LDO regulator. The TPS712xx has an NR pin that is connected to the voltage reference through a 250 k Ω internal resistor. The 250 k Ω internal resistor, in conjunction with an external ceramic bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. To achieve a fast startup, the 250 k Ω internal resistor is shorted for 400 μ s after the device is enabled.

Because the primary noise source is the internal voltage reference, the output noise will be greater for higher output voltage versions. For the case where no noise reduction capacitor is used, the typical noise (μ Vrms) over 10 Hz to 100 kHz is 80 times the output voltage. If a 0.01 μ F capacitor is used from the NR pin to ground, the noise (μ Vrms) drops to 11.8 times the output voltage. For example, the TPS71256 exhibits only 33 μ Vrms of output voltage noise using a 0.01 μ F ceramic bypass capacitor and a 2.2 μ F ceramic output capacitor.

STARTUP CHARACTERISTICS

To minimize startup overshoot, the TPS712xx will initially target an output voltage that is approximately 80% of the final value. To avoid a delayed startup time, noise reduction capacitors of 0.01 μ F or less are recommended. Larger noise reduction capacitors will cause the output to hold at 80% until the voltage on the noise reduction capacitor exceeds 80% of the bandgap voltage. The typical startup time with a 0.001 μ F noise reduction capacitor is 60 μ s. Once one of the output voltages is present, the startup time of the other output will not be affected by the noise reduction capacitor.

PROGRAMMING THE TPS71202 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS71202 dual adjustable regulator is programmed using an external resistor divider, as shown in Figure 25. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where $V_{REF} = 1.225 \text{ V}$ (the internal reference voltage).

Resistors R2 and R4 should be chosen for approximately a 40 μA divider current. Lower value resistors can be used for improved noise performance, but will consume more power. Higher values should be avoided because leakage current at FB increases the output voltage error. The recommended design procedure is to choose $R2 = 30.1 \text{ k}\Omega$ to set the divider current at 40 μA , and then calculate R1 using Equation 2:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (2)$$

To improve the stability and noise performance of the adjustable version, a small compensation capacitor can be placed between OUT and FB.

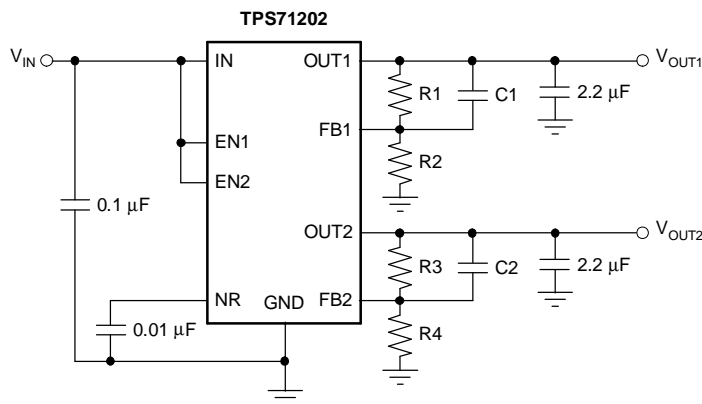
For voltages $\leq 1.8 \text{ V}$, the value of this capacitor should be 100 pF. For voltages $> 1.8 \text{ V}$, the approximate value of this capacitor can be calculated as Equation 3:

$$C1 = \frac{(3 \times 10^5) \times (R1 + R2)}{(R1 \times R2)} \quad (\text{pF}) \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in Figure 25. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage $\leq 1.8 \text{ V}$ is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF .

DROPOUT VOLTAGE

The TPS712xx uses a PMOS pass transistor to achieve extremely low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS, ON}$ of the PMOS pass element. Dropout voltages at lower currents can be approximated by calculating the effective $R_{DS, ON}$ of the pass element and multiplying that resistance by the load current. $R_{DS, ON}$ of the pass element can be obtained by dividing the dropout voltage by the rated output current. For the TPS71256, the $R_{DS, ON}$ of the pass element is 84 m Ω . The dropout voltage of the TPS712xx will be less for higher output voltage versions. This is because the PMOS pass element will have lower on-resistance due to increased gate drive.



Output Voltage Programming Guide

| V_{OUT} | R1/R3 | R2/R4 | C1/C2 |
|-----------|-----------------|-----------------|--------|
| 1.225 V | Short | Open | Open |
| 1.5 V | 7.15 k Ω | 30.1 k Ω | 100 pF |
| 2.5 V | 31.6 k Ω | 30.1 k Ω | 22 pF |
| 3.0 V | 43.2 k Ω | 30.1 k Ω | 15 pF |
| 3.3 V | 49.9 k Ω | 30.1 k Ω | 15 pF |
| 4.75 V | 86.6 k Ω | 30.1 k Ω | 15 pF |

Figure 25. TPS71202 Adjustable LDO Regulator Programming

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor will reduce over/undershoot magnitude but increase duration of the transient response. In the adjustable version, the addition of a capacitor, C_{FB} , from the output to the feedback pin will also improve stability and transient response. The transient response of the TPS712xx is enhanced with an active pull-down that engages when the output is over-voltaged. The active pull-down decreases the output recovery time when the load is removed. [Figure 13](#) in the *Typical Characteristics* section shows the output transient response.

SHUTDOWN

Both enable pins are active high and are compatible with standard TTL-CMOS levels. The device is only completely disabled when both EN1 and EN2 are logic low. In this state, the LDO is completely off and the ground pin current drops to approximately 100 nA. With one output disabled, the ground pin current is slightly greater than half the nominal value. When shutdown capability is not required, the enable pins should be connected to the input supply.

INTERNAL CURRENT LIMIT

The TPS712xx internal current limit helps protect the regulator during fault conditions. During current limit, the output will source a fixed amount of current that is largely independent of the output voltage.

The TPS712xx PMOS-pass transistors have a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (that is, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be appropriate.

THERMAL PROTECTION

Thermal protection disables both outputs when the junction temperature of either channel rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS712xx was designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS712xx into thermal shutdown will degrade device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for a JEDEC high-K board is shown in the Dissipation Ratings table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS71202DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71202DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71202DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71202DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71219DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71219DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71219DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71219DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71229DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71229DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71229DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71229DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71247DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71247DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71247DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71247DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71256DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71256DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71256DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71256DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71257DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71257DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71257DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS71257DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

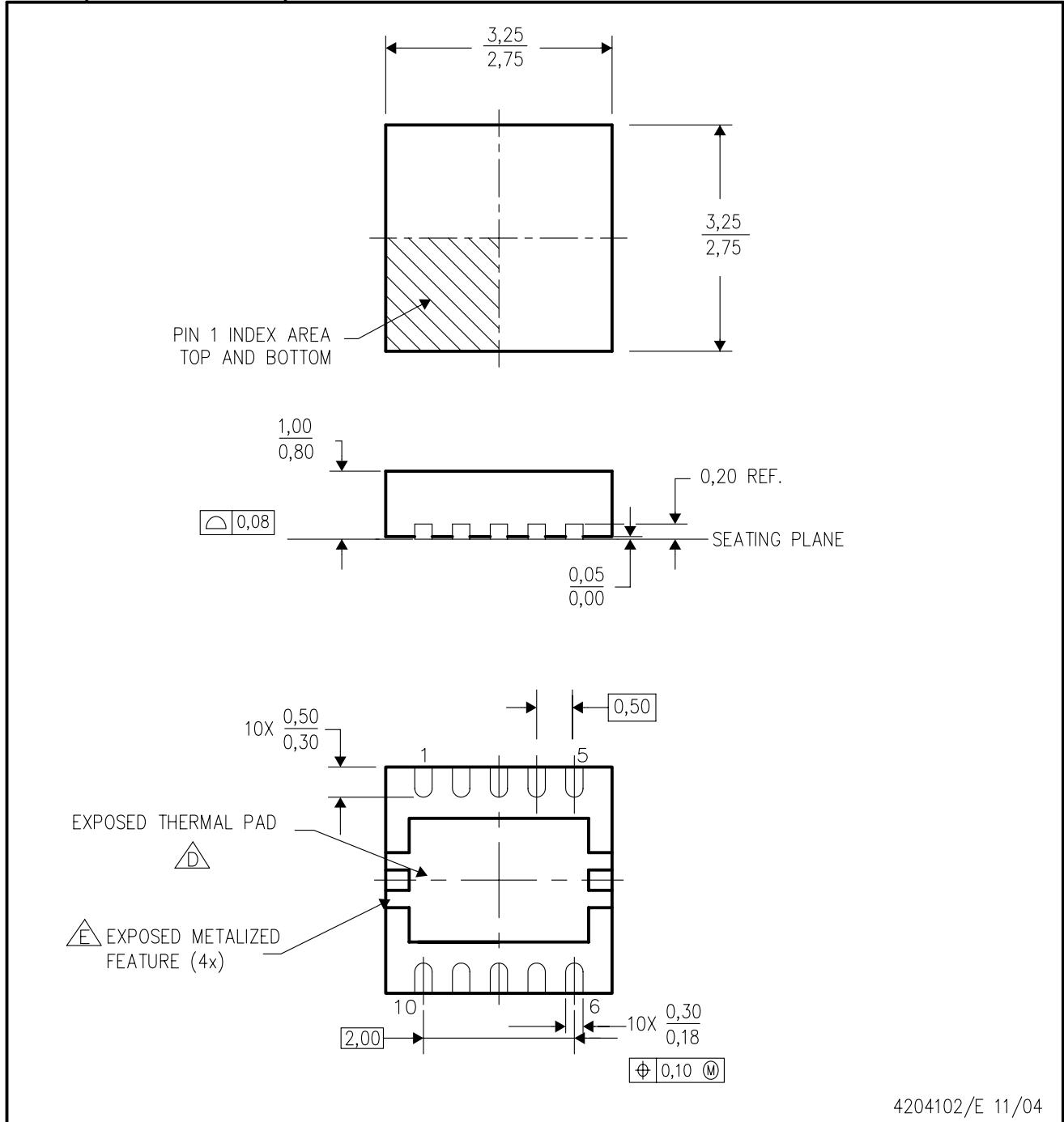
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

DRC (S-PDSO-N10)

PLASTIC SMALL OUTLINE



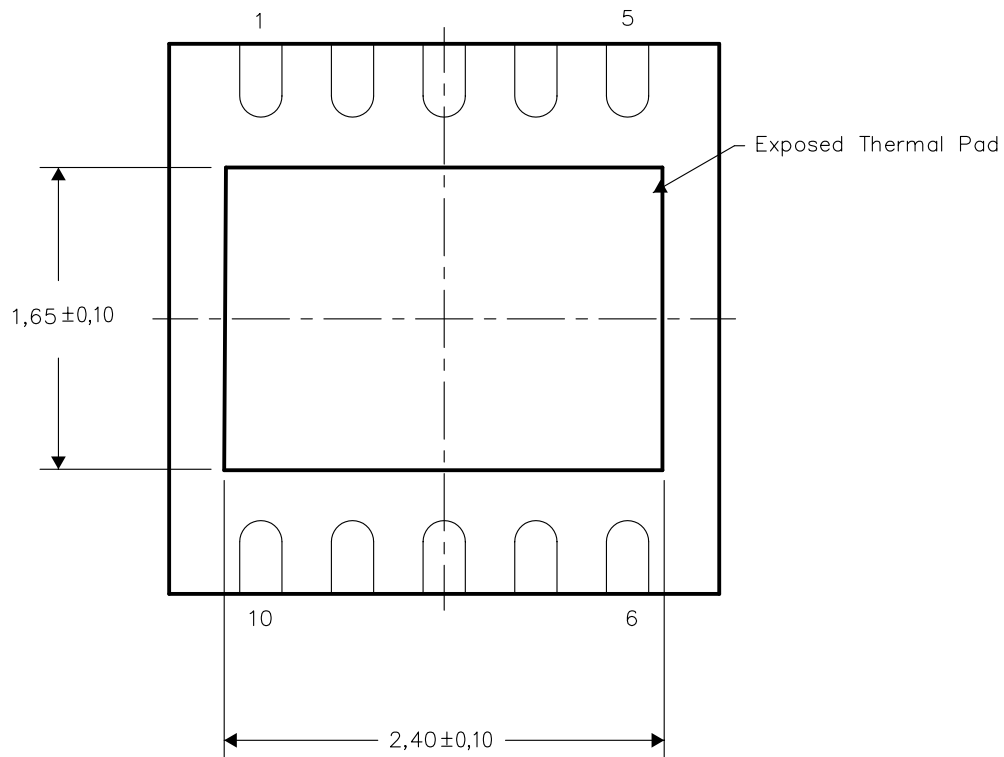
- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. Small Outline No-Lead (SON) package configuration.
 D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

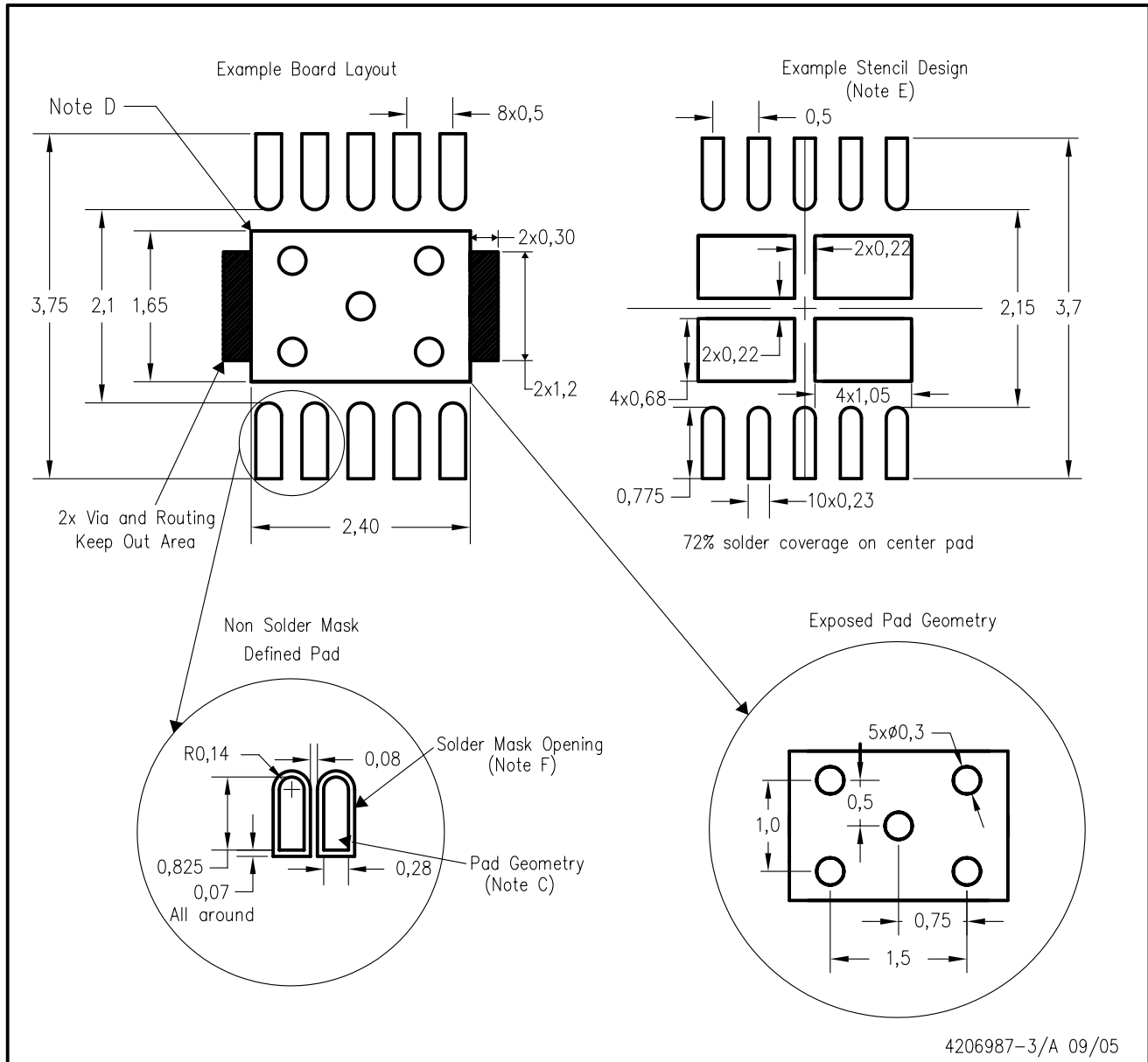


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S-PDSO-N10)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|------------------|--|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265