

## DUAL CHANNEL, SYNCHRONOUS STEP-DOWN PWM CONTROLLER

### FEATURES

- High Efficiency – No Current Sense Resistor Required,  $R_{DS(on)}$  Overcurrent Detection with Temperature Compensation
- Adjustable Output Voltage Down to 0.9 V
- Voltage-Mode PWM Control: Maximum 500-kHz Operation
- 180° Out-of-Phase Control
- Individual Standby and Soft-Start for Each Channel – Easy Power Sequencing
- Overvoltage and Undervoltage Protection
- Built-In Boot-Strap Diode
- Built-In 5-V Linear Regulator
- Accurate  $\pm 1\%$  0.85-V Reference

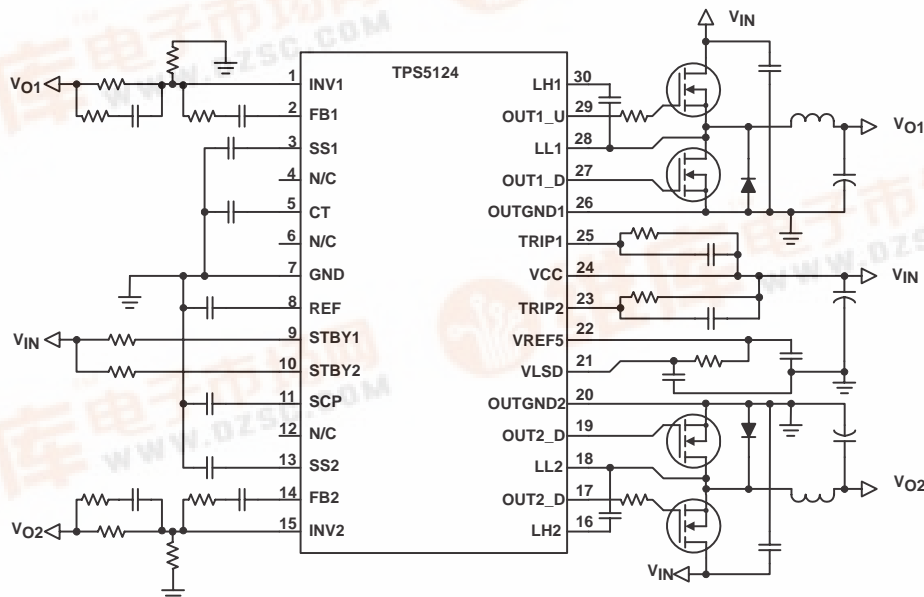
### APPLICATIONS

- Consumer Game Systems
- DSP Applications
- Digital Set-Top Box
- VGA and Sound Cards

### DESCRIPTION

The TPS5124 is dual independent high efficiency synchronous step-down controller. It supports a low-voltage/high-current power supply applications that use either a 5-V or 12-V bus voltage. Since both controllers of the TPS5124 operate 180 degree out-of-phase, the input current ripple is minimized resulting in a smaller input capacitance and reduced power supply cost.

The current protection circuit detects the drain-to-source voltage drop across the high-side and low-side power MOSFET while it is conducting. Also, the current protection circuit has a temperature coefficient to compensate for the  $R_{DS(on)}$  variation of the MOSFET. This resistor-less current protection and built-in boost diode simplify the system design and reduces the external parts count. Other features such as undervoltage lockout, overvoltage, undervoltage, and programmable short-circuit protection promote system reliability.



UDG-03123

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# TPS5124

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## ABSOLUTE MAXIMUM RATINGS

–40°C ≤ T<sub>A</sub> ≤ 85°C, all voltage values are with respect to the network ground terminal unless otherwise noted. (1)

		TPS5124	UNIT
Input voltage range	VCC, STBY1, STBY2, TRIP1, TRIP2	–0.3 to 16	V
	LH1, LH2 wrt GND	–0.3 to 22	
	LH1, LH2 (wrt the corresponding LL terminal)	–0.3 to 6	
	SS1, SS2, CT, INV1, INV2, SCP, VLSD	–0.3 to 6	
Output voltage range	OUT1_U, OUT2_U	–1 to 22	
	OUT1_U, OUT2_U (wrt the corresponding LL terminal)	–0.3 to 6	
	LL1, LL2	–1 to 16	
	OUT1_D, OUT2_D, VREF5, FB1, FB2	–0.3 to 6	
	OUTGND1, OUTGND2	–0.3 to 0.3	
	REF	–0.3 to 3	
Output current range	VREF5	50	mA
	VREF	5	
Operating free-air temperature range, T <sub>A</sub>		–40 to 85	°C
Storage temperature range, T <sub>stg</sub>		–55 to 150	
Junction temperature range, T <sub>J</sub>		–40	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>		6.5		15	V
	(when VLSD is connected to VCC)	4.5		5.5	
Input voltage range	INV1, INV2, CT, SS1, SS2, SCP, FB1, FB2, OUT1_D, OUT2_D, VLSD	–0.1		5.9	
	OUT1_U, OUT2_U, LH1, LH2	–0.1		21	
	TRIP1, TRIP2, LL1, LL2, STBY1, STBY2	–0.1		15	
Operating frequency, f <sub>OSC</sub>			300	500	
Operating free-air temperature range, T <sub>A</sub>		–40		85	°C

**ELECTRICAL CHARACTERISTICS**T<sub>J</sub> = -40°C to 85°C, V<sub>CC</sub> = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENTS</b>						
I <sub>CC</sub>	Supply current	T <sub>A</sub> = 25°C, V <sub>CT</sub> = V <sub>INV1</sub> = V <sub>INV2</sub> = 0 V		1.1	1.5	mA
I <sub>CCS</sub>	V <sub>IN</sub> standby current	V <sub>STBY1</sub> = V <sub>STBY2</sub> = 0 V		0.1	10.0	μA
<b>5-V REGULATOR</b>						
V <sub>VREF5</sub>	Output voltage	T <sub>A</sub> = 25°C, 7.5 V ≤ V <sub>CC</sub> ≤ 15 V, 0 mA ≤ I <sub>O</sub> ≤ 10 mA	4.8	5.0	5.2	V
V <sub>LN5</sub>	Line regulation	7.5 V ≤ V <sub>CC</sub> ≤ 15 V, I <sub>O</sub> = 10 mA			20	mV
V <sub>LD5</sub>	Load regulation	1 mA ≤ I <sub>O</sub> ≤ 10 mA			40	
I <sub>OS</sub>	Short-circuit output current	V <sub>REF5</sub> = 0 V, T <sub>A</sub> = 25°C	65			mA
V <sub>THH</sub>	UVLO threshold voltage	high-to-low	3.6		4.2	V
V <sub>THL</sub>		low-to-high	3.5		4.1	V
V <sub>HYS</sub>	Hysteresis		30		150	mV
<b>REFERENCE VOLTAGE</b>						
V <sub>REF</sub>	Reference voltage			0.85		V
V <sub>REF(td)</sub>	Reference voltage tolerance	I <sub>REF</sub> = 50 μA, T <sub>A</sub> = 25°C	-0.5%		0.5%	
V <sub>REF(ln)</sub>	Line regulation	6.5 V ≤ V <sub>CC</sub> ≤ 15 V, I <sub>REF</sub> = 50 μA		0.03	3.00	mV
V <sub>REF(ld)</sub>	Load regulation	0.1 μA ≤ I <sub>REF</sub> ≤ 1 mA		0.15	5.00	
<b>CONTROL</b>						
V <sub>IH</sub>	High-level input voltage	STBY1, STBY2	2.2			V
V <sub>IL</sub>	Low-level input voltage	STBY1, STBY2			0.3	
<b>OUTPUT VOLTAGE MONITOR</b>						
	OVP comparator threshold voltage		0.90	0.95	1.00	V
	UVP comparator threshold voltage		0.58	0.66	0.74	
	Timer latch current source	Overshoot protection	-4	-8	-12	μA
		Undervoltage protection	-1	-1.7	-2.3	
<b>OSCILLATOR</b>						
f <sub>OSC</sub>	Frequency	C <sub>T</sub> = 47 pF, T <sub>A</sub> = 25°C		300		kHz
V <sub>OSC(h)</sub>	High-level output voltage	DC	1.0	1.1	1.2	V
		f <sub>OSC</sub> = 300 kHz		1.14		
V <sub>OSC(l)</sub>	Low-level output voltage	DC	0.4	0.5	0.6	
		f <sub>OSC</sub> = 300 kHz		0.46		
<b>ERROR AMPLIFIER</b>						
V <sub>IO</sub>	Input offset voltage	T <sub>A</sub> = 25°C		2	10	mV
	Open-loop voltage gain		50			dB
	Unity gain bandwidth			2.5		MHz
I <sub>SINK</sub>	Output sink current	V <sub>O</sub> = 2.5 V	2	4		mA
I <sub>SRC</sub>	Output source current	V <sub>O</sub> = 2.5 V	-2	-4		
<b>DUTY CONTROL</b>						
	Maximum duty cycle	f <sub>OSC</sub> = 300 kHz, V <sub>(INV1)</sub> = V <sub>(INV2)</sub> = 0 V		80%		

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## ELECTRICAL CHARACTERISTICS(continued)

T<sub>J</sub> = -40°C to 85°C, V<sub>CC</sub> = 12 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT DRIVER</b>					
OUT_U sink current	V(OUT <sub>x_U</sub> ) - V(LL <sub>x</sub> ) = 3 V		1.2		A
OUT_U source current	V(LH <sub>x</sub> ) - V(OUT <sub>x_U</sub> ) = 3 V		-1.2		
OUT_D sink current	V(OUT <sub>x_D</sub> ) = 3 V		1.5		
OUT_D source current	V(OUT <sub>x_D</sub> ) = 2 V		-1.5		
<b>SOFT START</b>					
I <sub>SOFT</sub> Soft-start current		-1.3	-2.3	-2.9	μA
<b>CURRENT PROTECTION</b>					
I <sub>TRIP</sub> TRIP current	T <sub>A</sub> = 25°C	11	13	15	μA
TC TRIP current temperature coefficient	T <sub>A</sub> = 25°C		3400		ppm/°C

## AVAILABLE OPTIONS

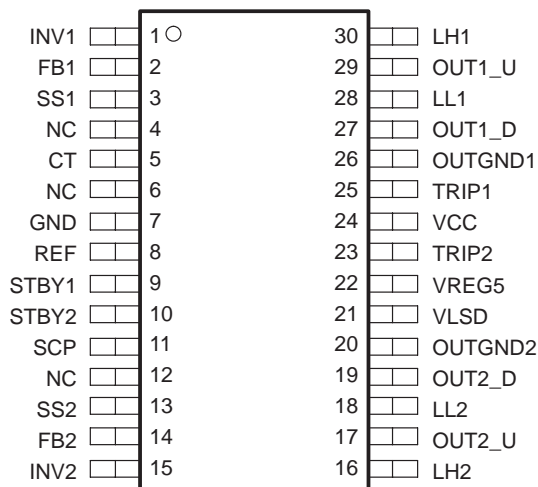
T <sub>A</sub>	PACKAGED DEVICES <sup>(1)</sup>
	PLASTIC TSSOP (DBT)
-40°C to 85°C	TPS5124DBT

(1) The DBT package is available taped and reeled. Add an R suffix to the device type (e.g. TPS5124DBTR) to order quantities of 2,000 devices per reel.

## DISSIPATION RATING TABLE

PACKAGE	T <sub>A</sub> < 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 85°C POWER RATING
30-pin DBT	874 mW	7.0 mW/°C	454 mW

### DBT PACKAGE (TOP VIEW)



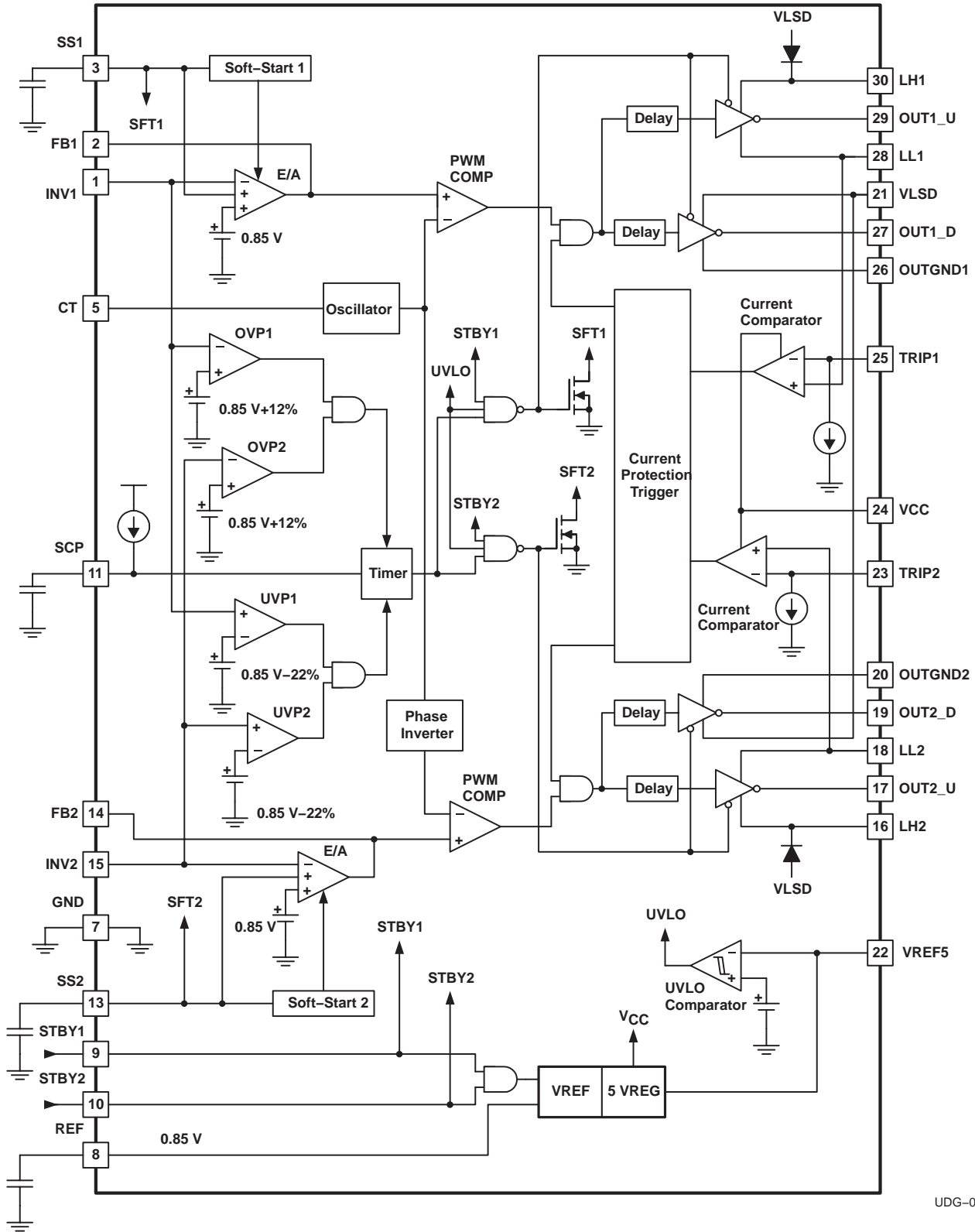
## TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CT	5	I/O	External capacitor from CT to GND adjusts frequency of the triangle oscillator.
FB1	2	O	Feedback output of SBRC–Channel 1 error amplifier.
FB2	14	O	Feedback output of SBRC–Channel 2 error amplifier.
GND	7	–	Signal GND.
INV1	1	I	Inverting inputs of Channel 1 error amplifier and OVP1/UVP1 comparator.
INV2	15	I	Inverting inputs of Channel 2 error amplifier and OVP2/UVP2 comparator.
LH1	30	I/O	Bootstrap capacitor connection for Channel 1 high-side gate driver.
LH2	16	I/O	Bootstrap capacitor connection for Channel 2 high-side gate driver.
LL1	28	I/O	CH1 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator.
LL2	18	I/O	CH2 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator.
NC	4,6,12	–	No connection.
OUT1_D	27	O	Gate drive output for Channel 1 low-side MOSFETs.
OUT2_D	19	O	Gate drive output for Channel 2 low-side MOSFETs.
OUT1_U	29	O	Gate drive output for Channel 1 high-side MOSFETs.
OUT2_U	17	O	Gate drive output for Channel 2 high-side MOSFETs.
OUTGND1	26	–	Ground for Channel 1 MOSFET drivers.
OUTGND2	20	–	Ground for Channel 2 MOSFET drivers.
REF	8	O	0.85-V reference voltage output. This 0.85-V reference voltage is used to set the output voltage and the reference for the overvoltage and undervoltage protections. This reference voltage is dropped down from the internal 5-V regulator.
SCP	11	I/O	Fault latch timer pin. An external capacitor connected between SCP and GND sets SCP enable time up.
SS1	3	I/O	Soft start control for Channel 1. Connect an external capacitor between this pin and GND to specify SOFT-START time.
SS2	13	I/O	Soft start control for Channel 2. Connect an external capacitor between this pin and GND to specify SOFT-START time.
STBY1	9	I	Standby control input for Channel 1. It can be switched into standby mode by grounding the STBY1 pin.
STBY2	10	I	Standby control input for Channel 2. It can be switched into standby mode by grounding the STBY2 pin.
TRIP1	25	I	External resistor connection for Channel 1 output current protection control.
TRIP2	23	I	External resistor connection for Channel 2 output current protection control.
VCC	24	I	Supply voltage input
VLSD	21	I	Supply voltage input for low side driver. Typically connected to VREF5 with R-C filter when $V_{VCC}$ is between 6.5V and 15V and connected to VCC with filter when $V_{VCC}$ is between 4.5 V and 5.5 V.
VREF5	22	O	5V linear regulator output. When $V_{VCC}$ is between 4.5V and 5.5V should be connected to VCC.

# TPS5124

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## FUNCTIONAL BLOCK DIAGRAM



UDG-03105

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## FUNCTIONAL DESCRIPTION

### INPUT VOLTAGE RANGE

TPS5124 supports two input voltage ranges. When  $V_{VCC}$  is between 6.5 V and 15 V, VLSD is connected to VREF5 with R-C filter (see Figure 1). When  $V_{VCC}$  is between 4.5 V and 5.5 V, VLSD is connected to VCC with R-C filter and VREF5 is connected to VCC. (see Figure2).

### REFERENCE VOLTAGE (0.85 V)

This 0.85-V reference voltage is used to set the output voltage and the reference for the overvoltage and undervoltage protections. This reference voltage is dropped down from the internal 5V regulator.

### PWM OPERATION

TPS5124 includes dual synchronous buck regulator controllers (SBRC) that operate 180° out of phase and same frequency. Both channels have individual standby and softstart controller.

### 5-V REGULATOR

An internal linear voltage regulator is used for the reference voltage and power supply of internal circuit. When this regulator is connected to the VLSD pin, it is used for powering the low-side driver and powering the high-side driver through the built-in bootstrap diode or external bootstrap circuit. It is active if either STBY1 or STBY2 is HIGH and has a tolerance of 4 %.

### ERROR AMPLIFIER

Each channel has its own error amplifier to regulate the output voltage of the synchronous buck converter. The unity gain bandwidth is 2.5 MHz. This decreases the amplifier delay during fast load transients and contributes to a fast transient response.

### LOW-SIDE DRIVER

The low-side driver is designed to drive high current and low  $R_{DS(on)}$  N-channel MOSFET(s). The maximum drive voltage is 5 V from the VLSD pin. The current rating of the driver is typically 1.5 A at source and sink.

### HIGH-SIDE DRIVER

The high-side driver is designed to drive high current and low  $R_{DS(on)}$  N-channel MOSFET(s). The current rating of the driver is 1.2 A (typ.) at source and sink. When configured as a floating driver a bias voltage is delivered from the VSLD pin through built-in bootstrap diode or external bootstrap circuit. When the MOSFET needs high gate threshold voltage, it is useful to add the external schottky diodes which provide a higher voltage for the gate drive than using the built-in diodes. The instantaneous drive current is supplied by the flying capacitor between the LH and LL pins since a bias power supply does not usually have low impedance. The maximum voltage between the OUTx\_U and LLx pins is about 5.5 V when the VSLD pin is connected to the VREF5 pin. The maximum voltage that can be applied between the LH and OUTGND pins is 22 V.

### DEAD-TIME

The internally defined dead-time prevents shoot-through current flowing through the main power MOSFETs during switching transitions.

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## FUNCTIONAL DESCRIPTION

### OVER CURRENT PROTECTION (OCP)

Over current protection (OCP) is achieved by comparing the drain-to-source voltage of the high-side and low-side MOSFET to a set-point voltage, which is defined by both the internal current source,  $I_{TRIP}$ , and the external resistor connected between the VCC and TRIP pins.  $I_{TRIP}$  has a typical value of 13  $\mu\text{A}$  at 25°C. When the low-side MOSFET's drain-to-source voltage exceeds the set-point voltage during low-side conduction, the high-side current comparator becomes active, and the low-side on pulse is extended until this voltage comes back below the threshold. If the set-point voltage is exceeded during high-side conduction in the following cycle, the current limit circuit terminates the high-side driver pulse. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated to latch both the high-side and low-side drivers OFF. In the TPS5124, trip current ( $I_{TRIP}$ ) has a temperature coefficient of 3400 ppm/°C in order to compensate for temperature drift of the MOSFET on-resistance.

### OVER VOLTAGE PROTECTION (OVP)

For over voltage protection (OVP), the TPS5124 monitors the INV pin voltage. When the INV pin voltage is higher than 0.95 V (0.85 V +12%), the OVP comparator output goes low and the SCP timer starts to charge an external capacitor connected to SCP pin. After a set time, the SCP circuit latches the high-side MOSFET driver to OFF state and low-side MOSFET drivers to ON state. The timer source current for the OVP latch is 8  $\mu\text{A}$ (typ.), and the time-up voltage is 1.185 V (typ.). The OVP timer is designed to be five times faster than the under voltage protection timer described below.

### UNDER VOLTAGE PROTECTION (UVP)

For under voltage protection (UVP), the TPS5124 monitors the INV pin voltage. When the INV pin voltage is lower than 0.66 V (0.85 V – 22%), the UVP comparator output goes low, and the SCP timer starts to charge the external capacitor connected to SCP pin. Also, when the current comparator triggers the OCP, the UVP comparator detects the under voltage output and starts the SCP capacitor charge, too. After a set time, the SCP circuit latches both of the MOSFET drivers to the OFF state. The timer latch source current for UVP is 1.6  $\mu\text{A}$  (typ.), and the time-up voltage is also 1.185 V (typ.).

### SCP (TIMER)

When an OVP or UVP comparator output goes low, the SCP circuit starts to charge the SCP capacitor. If the SCP pin voltage goes beyond a constant level, the TPS5124 latches the MOSFET drivers. At this time, the state of MOSFET is different depending on the OVP alert and the UVP alert. The enable time used to latch the MOSFET drivers is decided by the value of the SCP capacitor. The charging constant current value depends on whether it is an OVP alert or a UVP alert as shown in the following equation:

$$I_{SCP(ovp)} = I_{SCP(uvp)} \times 5 \quad (1)$$

### SOFT START

Soft-start ramp up of the SBRC is controlled by the SSx pin voltage. After the STBY pin is raised to a HIGH level, an internal current source charges up an external capacitor connected between the SSx and GND pins. The soft-start time is easily calculated by the supply current and the capacitance value.



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**FUNCTIONAL DESCRIPTION**
**STANDBY**

The SBRC controller can be switched into standby mode separately by grounding STBY pin.

**Table 1. Standby Logic**

STBY1	STBY2	SBRC (CH1)	SBRC (CH2)	5-V REGULATOR
L	L	DISABLED	DISABLED	DISABLED
L	H	DISABLED	ENABLED	ENABLED
H	L	ENABLED	DISABLED	ENABLED
H	H	ENABLED	ENABLED	ENABLED

**UNDERVOLTAGE LOCK OUT (UVLO)**

For undervoltage lock out (UVLO), the TPS5124 monitors VREF5 voltage. When the VREF5 voltage decreases below about 4.1 V, the output stages of both SBRC are turned off. This state is not latched and the operation recovers immediately after the input voltage becomes higher than about 4.2 V again. The typical hysteresis voltage is 40 mV.

**PHASE INVERTER**

The SBRC (CH2) of the TPS5124 operates in the same phase as the internal triangular oscillator output while the SBRC (CH1) operates 180° out of phase. When the SBRC (CH1) and the SBRC (CH2) share the same input power supply, the TPS5124 reduces input current ripple and enables the input capacitor value smaller.

**OSCILLATOR**

TPS5124 has a triangle oscillator generator internal to the device. The oscillation frequency is set by the size of the capacitor connected to the CT pin.

APPLICATION INFORMATION

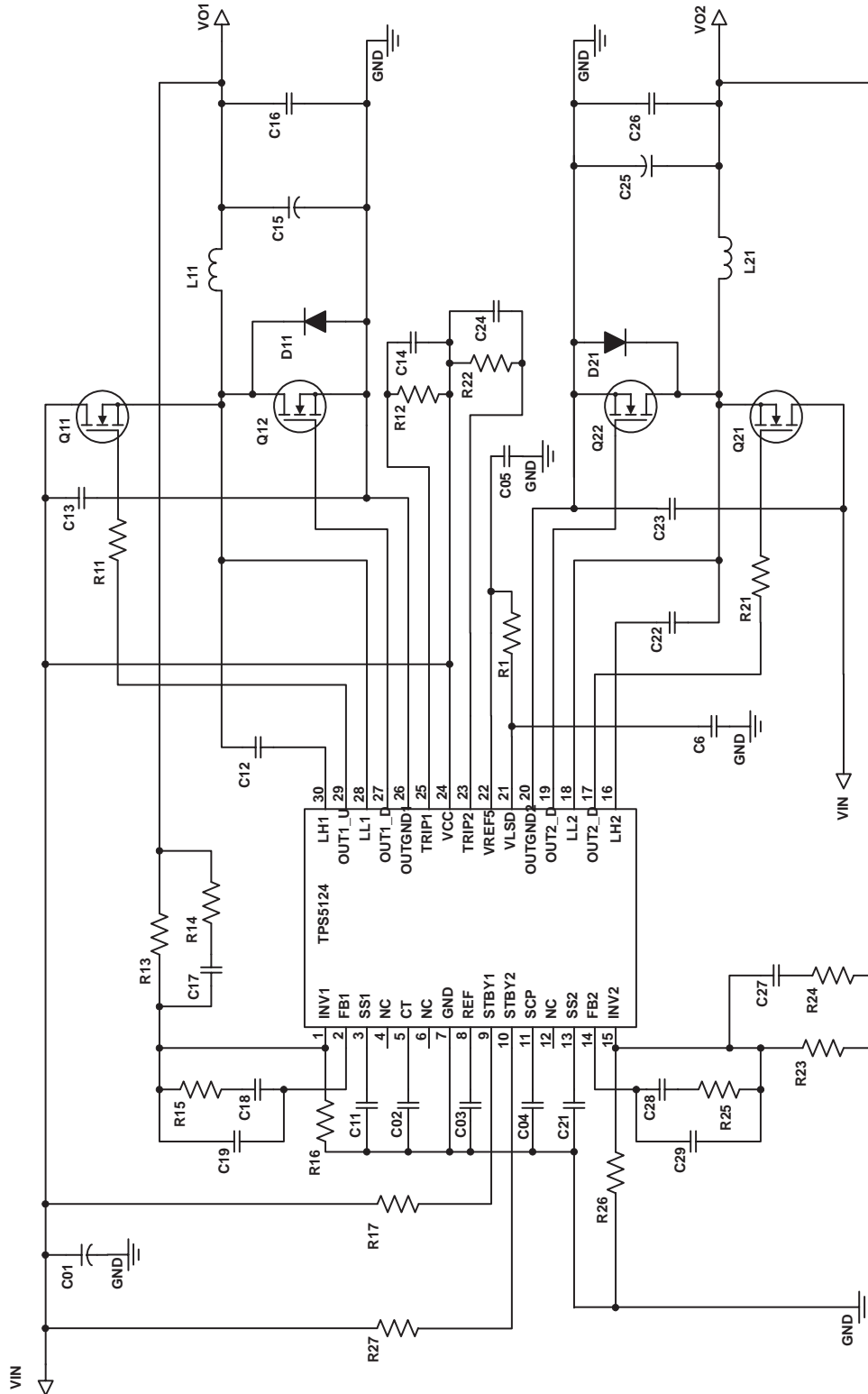


Figure 1. Simplified Application Schematic ( $V_{IN} = 12\text{ V[typ]}$ )

APPLICATION INFORMATION

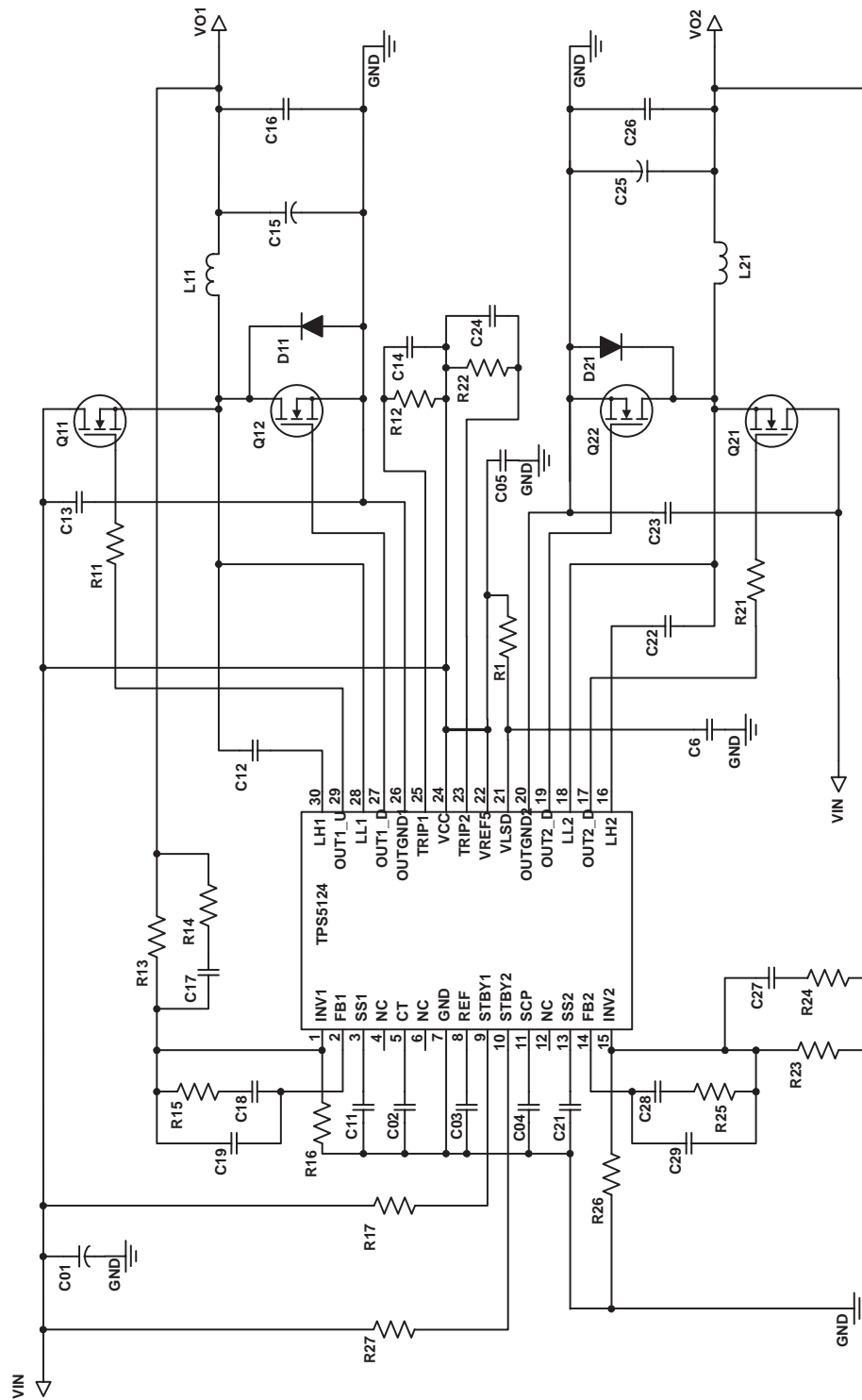


Figure 2. Simplified Application Schematic ( $V_{IN} = 5\text{ V[typ]}$ )

APPLICATION INFORMATION

SUPPLY CURRENT  
VS  
JUNCTION TEMPERATURE

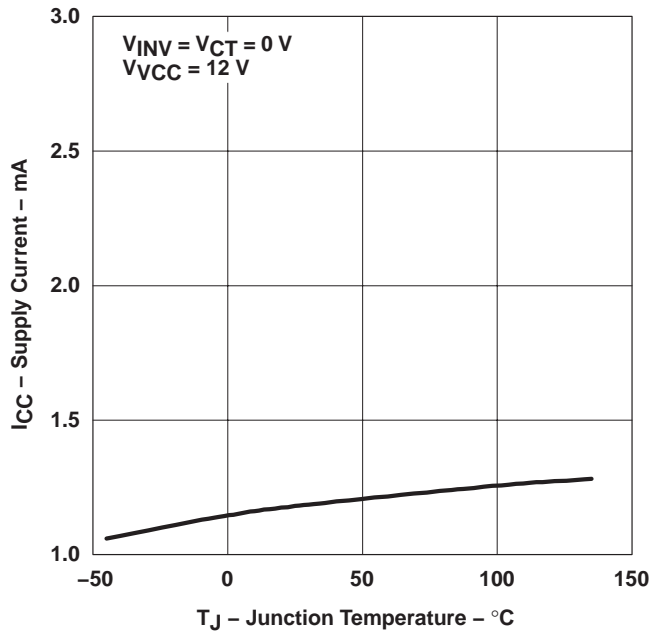


Figure 3

SHUTDOWN SUPPLY CURRENT  
VS  
JUNCTION TEMPERATURE

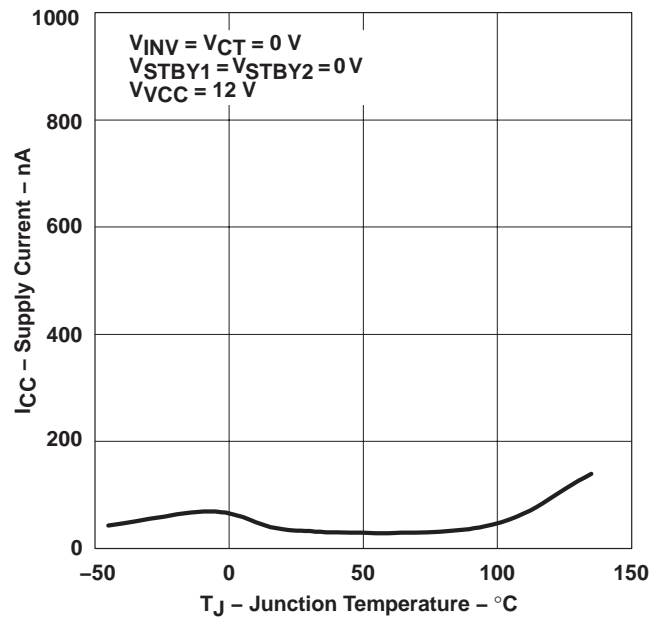


Figure 4

SCP CURRENT  
VS  
JUNCTION TEMPERATURE

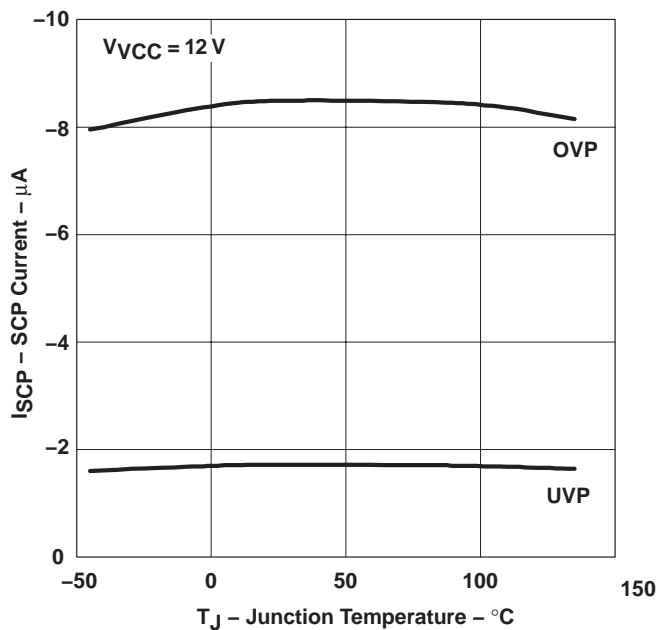


Figure 5

TRIP CURRENT  
VS  
JUNCTION TEMPERATURE

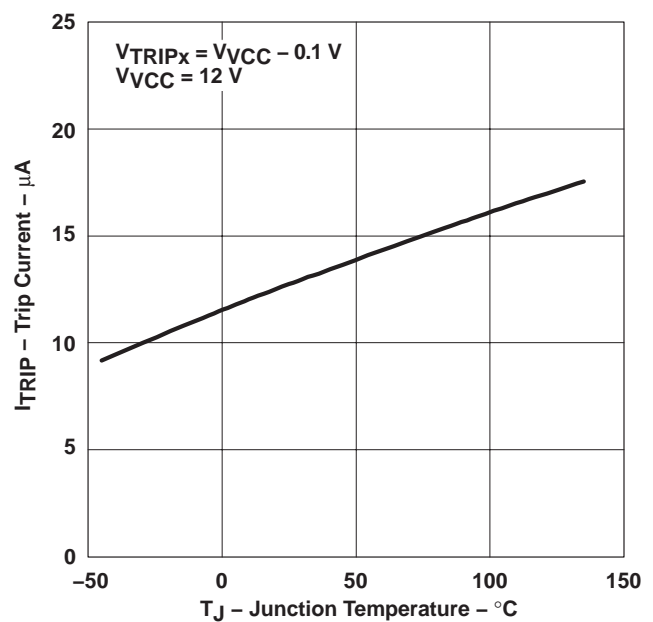


Figure 6

APPLICATION INFORMATION

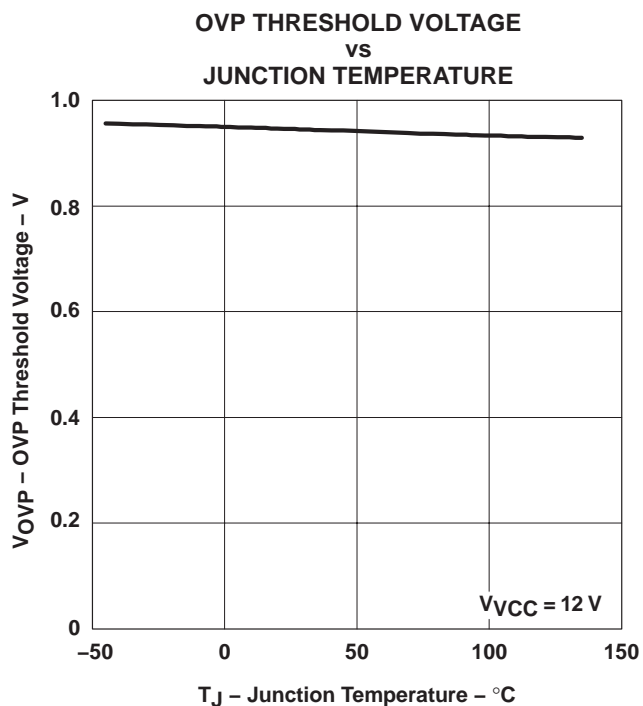


Figure 7

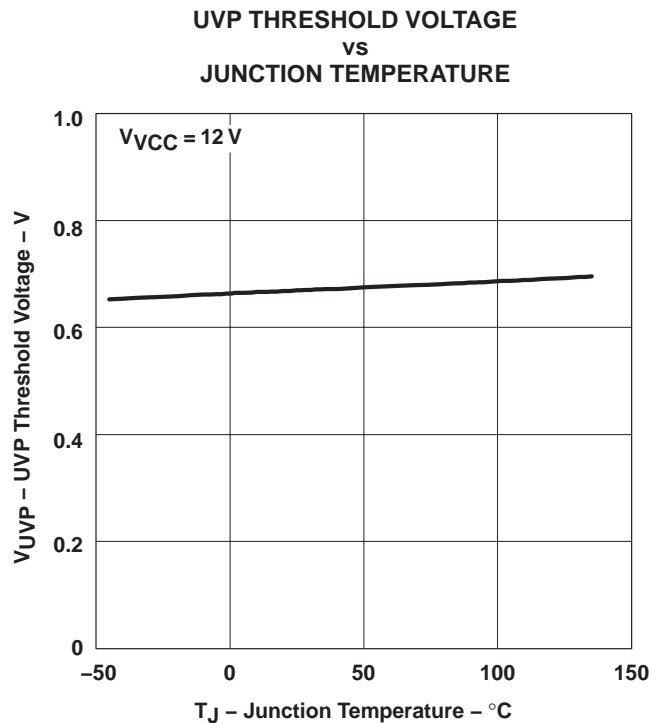


Figure 8

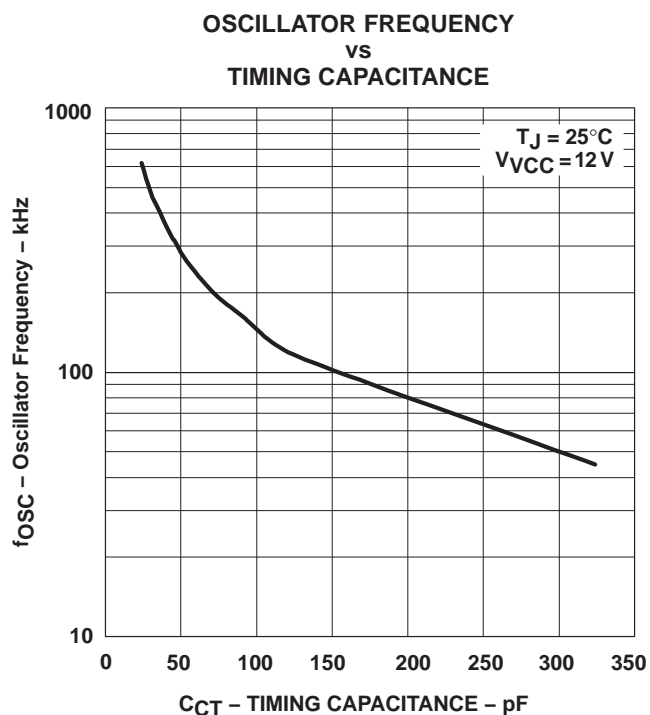


Figure 9

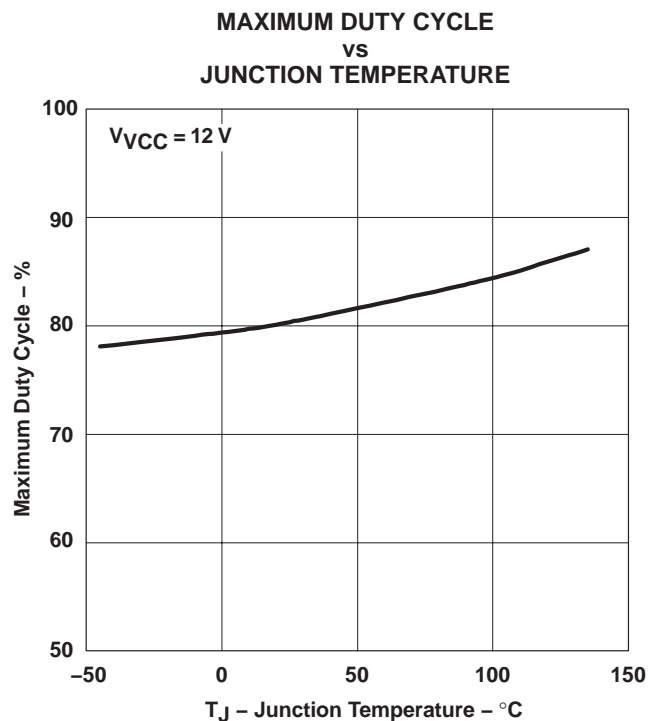


Figure 10

APPLICATION INFORMATION

SCP DELAY TIME  
vs  
SCP CAPACITANCE

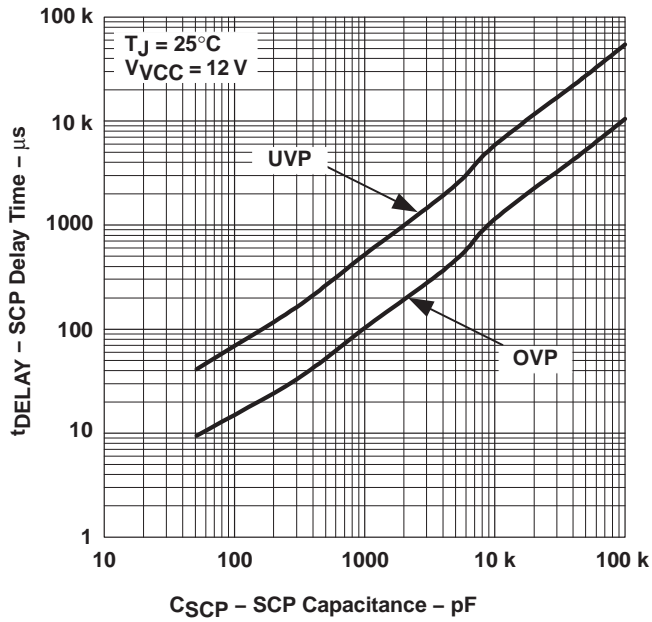


Figure 11

SOFT-START TIME  
vs  
SOFT-START CAPACITANCE

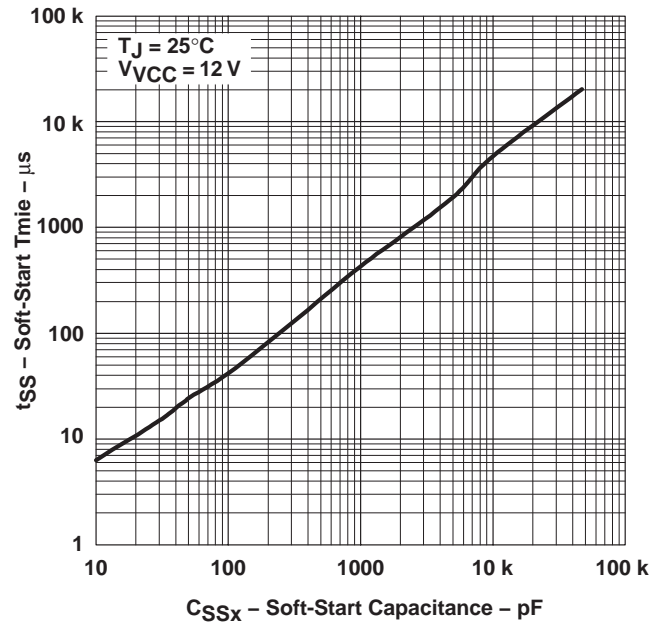


Figure 12

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS5124DBT	ACTIVE	SM8	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS5124DBTG4	ACTIVE	SM8	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS5124DBTR	ACTIVE	SM8	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS5124DBTRG4	ACTIVE	SM8	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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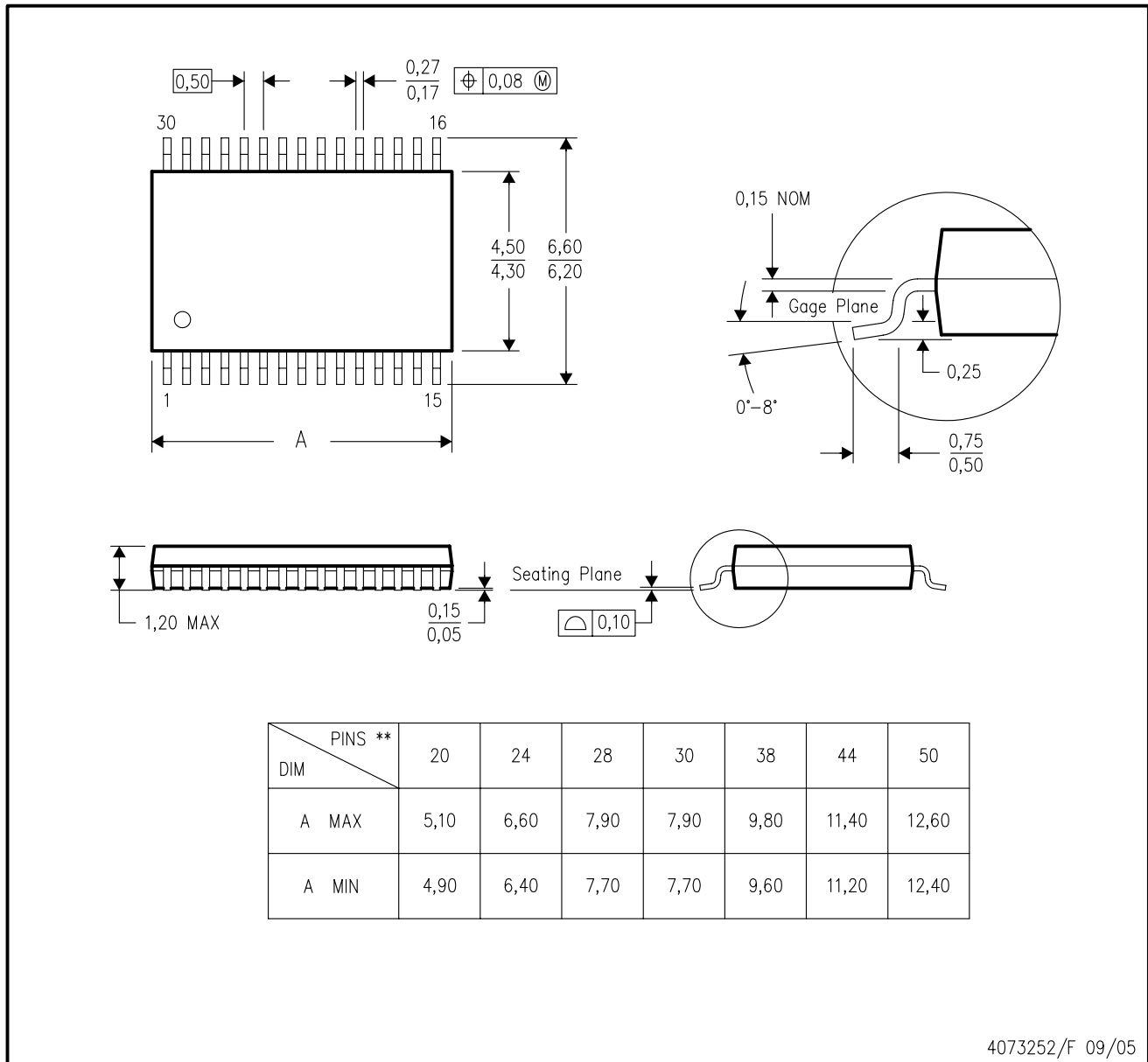
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# MECHANICAL DATA

## DBT (R-PDSO-G\*\*)

30 PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



4073252/F 09/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-153 except 44 pin package length.



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