WIDEBAND, LOW NOISE, LOW DISTORTION FULLY DIFFERENTIAL AMPLIFIER

FEATURES

- **Fully Differential Architecture**
- **Centered Input Common-mode Range**
- **Minimum Gain of 1V/V (0 dB)**
- **Bandwidth: 1600 MHz**
- **Slew Rate: 5100 V/μs**
- **1% Settling Time: 2.9 ns**
- **HD_2: –75 dBc at 70 MHz**
- **HD_3: –86 dBc at 70 MHz**
- **OIP_2: 77 dBm at 70 MHz**
- **OIP_3: 42 dBm at 70 MHz**
- **Input Voltage Noise: 2.2 nV/√Hz (f >10 MHz)**
- **Noise Figure: 19.8 dB**
- **Output Common-Mode Control**
- **Power Supply:**
  - **Voltage: 3 V (±1.5 V) to 5 V (±2.5 V)**
  - **Current: 37.7 mA**
- **Power-Down Capability: 0.65 mA**

APPLICATIONS

- **5 V Data Acquisition Systems High Linearity ADC Amplifier**
- **Wireless Communication**
- **Medical Imaging**
- **Test and Measurement**

DESCRIPTION

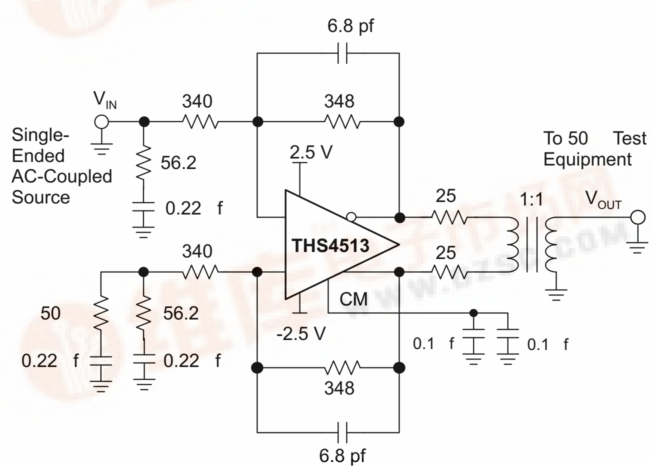
The THS4513 is a wideband, fully differential op amp designed for 3.3–5 V data acquisition systems. It has very low noise at 2.2 nV/√Hz, and extremely low harmonic distortion of –75 dBc HD_2 and –86 dBc HD_3 at 70 MHz with 2-Vpp output, G = 0 dB, and 200-Ω load. Slew rate is very high at 5100 V/μs and with settling time of 2.9 ns to 1% (2 V step) it is ideal for pulsed applications. It is designed for minimum gain of 0 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 5 mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4 mV differential offset voltage. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

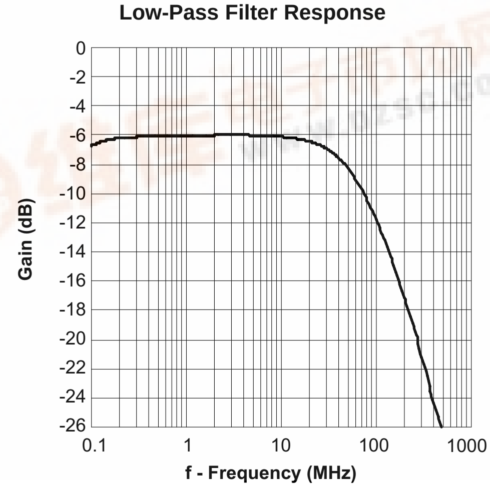
The input and output are optimized for best performance with their common-mode voltages set to mid-supply. Along with high performance at low power supply voltage, this makes for extremely high performance single supply 5 V data acquisition systems.

The THS4513 is offered in a Quad 16-pin leadless QFN package (RGT), and is characterized for operation over the full industrial temperature range from –40°C to 85°C.

60 MHz Low-Pass Filter



Low-Pass Filter Response



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION

TEMPERATURE	PACKAGED DEVICES			
		QUAD QFN(1)(2) (RGT-16)		SYMBOL
–40°C to 85°C		THS4513RGTT		–
		THS4513RGTR		

(1) This package is available taped and reeled. The R suffix standard quantity is 3000. The T suffix standard quantity is 250.
(2) The exposed thermal pad is electrically isolated from all other pins.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_{S-} to V_{S+}	Supply voltage		6 V
V_I	Input voltage		±VS
V_{ID}	Differential input voltage		4 V
I_O	Output current(1)		200 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature		150°C
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
	ESD ratings	HBM	2000
		CDM	1500
		MM	100

(1) The THS4513 incorporates a (QFN) exposed thermal pad on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the QFN thermally enhanced package.

DISSIPATION RATINGS TABLE PER PACKAGE

PACKAGE	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \leq 25°C$	$T_A = 85°C$
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

SPECIFICATIONS; $V_{S+} – V_{S–}$ = 5 V:

Test conditions unless otherwise noted: V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, G = 0 dB, CM = open, V_O = 2 Vpp, R_F = 348 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
Small-Signal Bandwidth	G = 0 dB, V_O = 100 mVpp			1.6		GHz	C
	G = 6 dB, V_O = 100 mVpp			1.4		GHz	
Gain-Bandwidth Product	G = 6 dB			2.8		GHz	
Bandwidth for 0-dB Flatness	G = 0 dB, V_O = 2 Vpp			150		MHz	
	G = 6 dB, V_O = 2 Vpp			700			
Large-Signal Bandwidth	G = 0 dB, V_O = 2 Vpp			1.4		GHz	
Slew Rate (Differential)	2V Step			5100		V/µs	
Rise Time Fall Time				0.5		ns	
				0.5			
Settling Time to 1%				2.9			
Settling Time to 0.1%				16			
2nd Order Harmonic Distortion	f = 10 MHz			–110		dBc	
	f = 50 MHz			–80			
	f = 100 MHz			–66			
3rd Order Harmonic Distortion	f = 10 MHz			–108		dBc	
	f = 50 MHz			–94			
	f = 100 MHz			–81			
2nd Order Intermodulation Distortion	V_O = 2 Vpp envelope, 200 kHz Tone Spacing, R_L = 100 Ω	f_C = 70 MHz		–78		dBc	
		f_C = 140 MHz		–55			
3rd Order Intermodulation Distortion		f_C = 70 MHz		–88			
		f_C = 140 MHz		–72			
2nd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω	f_C = 70 MHz		77		dBm	
		f_C = 140 MHz		53			
3rd Order Output Intercept Point		f_C = 70 MHz		42			
		f_C = 140 MHz		34			
1-dB Compression Point	f_C = 70 MHz			12.2		dBm	
	f_C = 140 MHz			10.8			
Noise Figure	50 Ω System, 10 MHz, G = 6 dB			19.8		dB	
Input Voltage Noise	f > 10 MHz			2.2		nV/√Hz	
Input Current Noise	f > 10 MHz			1.7		pA/√Hz	
DC PERFORMANCE							
Open-Loop Voltage Gain (A_{OL})				63		dB	C
Input Offset Voltage	T_A = 25°C			1	4	mV	A
	T_A = –40°C to 85°C			1	5	mV	
Average Offset Voltage Drift	T_A = –40°C to 85°C			2.6		µV/°C	B
Input Bias Current	T_A = 25°C			8	15.5	µA	A
	T_A = –40°C to 85°C			8	18.5		
Average Bias Current Drift	T_A = –40°C to 85°C			20		nA/°C	B
Input Offset Current	T_A = 25°C			1.6	3.6	µA	A
	T_A = –40°C to 85°C			1.6	7		
Average Offset Current Drift	T_A = –40°C to 85°C			4		nA/°C	B
INPUT							
Common-Mode Input Range High				1.75		V	B
Common-Mode Input Range Low				–1.75			
Common-Mode Rejection Ratio				90		dB	

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

SPECIFICATIONS; $V_{S+} - V_{S-}$ = 5 V: (continued)

Test conditions unless otherwise noted: V_{S+} = 2.5 V, V_{S-} = –2.5 V, G = 0 dB, CM = open, V_O = 2 Vpp, R_F = 348 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
OUTPUT							
Maximum Output Voltage High	Each output with 100 Ω to mid-supply	T_A = 25°C	1.2	1.4		V	A
		T_A = –40°C to 85°C	1.1	1.4			
Minimum Output Voltage Low		T_A = 25°C		–1.4	–1.2	V	
		T_A = –40°C to 85°C		–1.4	–1.1		
Differential Output Voltage Swing	T_A = 25°C		4.8	5.6		V	
	T_A = –40°C to 85°C		4.4	5.6			
Differential Output Current Drive	R_L = 10 Ω			96		mA	C
Output Balance Error	V_O = 100 mV, f = 1 MHz			–52		dB	
Closed-Loop Output Impedance	f = 1 MHz			0.3		Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-Signal Bandwidth				250		MHz	C
Slew Rate				110		V/µs	
Gain				1		V/V	
Output Common-Mode Offset from CM input	–1 V < CM < 1 V			5		mV	
CM Input Bias Current	–1 V < CM < 1 V			±40		µA	
CM Input Voltage Range				–1.5 to 1.5		V	
CM Input Impedance				23 || 1		kΩ || pF	
CM Default Voltage				0		V	
POWER SUPPLY							
Specified Operating Voltage			3	5	5.5	V	C
Maximum Quiescent Current	T_A = 25°C			37.7	40.9	mA	A
	T_A = –40°C to 85°C			37.7	41.9		
Minimum Quiescent Current	T_A = 25°C		34.5	37.7		mA	
	T_A = –40°C to 85°C		33.5	37.7			
Power Supply Rejection (±PSRR)				90		dB	C
POWERDOWN							
Enable Voltage Threshold	Referenced to V_{S-} ,Assured *on* above 2.1 V + V_{S-}			>2.1 + V_{S-}		V	C
Disable Voltage Threshold	Assured *off* below 0.7 V + V_{S-}			<0.7 + V_{S-}		V	
Powerdown Quiescent Current	T_A = 25°C			0.65	0.9	mA	A
	T_A = –40°C to 85°C			0.65	1		
Input Bias Current	$\overline{PD}$ = V_{S-}			100		µA	C
Input Impedance				50 || 2		kΩ || pF	
Turn-on Time Delay	Measured to output on			55		ns	
Turn-off Time Delay	Measured to output off			10		µs	

SPECIFICATIONS; $V_{S+} – V_{S–}$ = 3 V:

Test conditions unless otherwise noted: V_{S+} = 1.5 V, $V_{S–}$ = –1.5 V, G = 0 dB, CM = open, V_O = 1 Vpp, R_F = 348 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS		TYP	UNIT	TEST LEVEL (1)
AC PERFORMANCE					
Small-Signal Bandwidth	G = 0 dB, V_O = 100 mVpp		1.6	GHz	C
Small-Signal Bandwidth	G = 6 dB, V_O = 100 mVpp		1.3	GHz	C
Gain-Bandwidth Product	G = 6 dB		2.6	GHz	C
Bandwidth for 0-dB Flatness	G = 0 dB, V_O = 1 Vpp		135	MHz	C
Bandwidth for 0-dB Flatness	G = 6 dB, V_O = 1 Vpp		450	MHz	C
Large-Signal Bandwidth	G = 10 dB, V_O = 1 Vpp		1.4	GHz	C
Slew Rate (Differential)	1V Step		2700	V/µs	C
Rise Time	1V Step		0.25	ns	C
Fall Time	1V Step		0.25	ns	C
Settling Time to 1%	1V Step		2.9	ns	C
Settling Time to 0.1%	1V Step		16	ns	C
2nd Order Harmonic Distortion	f = 10 MHz		–116	dBc	C
2nd Order Harmonic Distortion	f = 50 MHz		–86	dBc	C
2nd Order Harmonic Distortion	f = 100 MHz		–60	dBc	C
3rd Order Harmonic Distortion	f = 10 MHz		–83	dBc	C
3rd Order Harmonic Distortion	f = 50 MHz		–61	dBc	C
3rd Order Harmonic Distortion	f = 100 MHz		–49	dBc	C
2nd Order Intermodulation Distortion	V_O = 1 Vpp 200 kHz Tone Spacing, R_L = 100 Ω	f_C = 70 MHz	–78	dBc	C
2nd Order Intermodulation Distortion	V_O = 1 Vpp 200 kHz Tone Spacing, R_L = 100 Ω	f_C = 140 MHz	–55	dBc	C
3rd Order Intermodulation Distortion	V_O = 1 Vpp 200 kHz Tone Spacing, R_L = 100 Ω	f_C = 70 MHz	–82	dBc	C
3rd Order Intermodulation Distortion	V_O = 1 Vpp 200 kHz Tone Spacing, R_L = 100 Ω	f_C = 140 MHz	–65	dBc	C
2nd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω	f_C = 70 MHz	70.2	dBm	C
2nd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω	f_C = 140 MHz	47	dBm	C
3rd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω	f_C = 70 MHz	32.7	dBm	C
3rd Order Output Intercept Point	200 kHz Tone Spacing R_L = 100 Ω	f_C = 140 MHz	24.7	dBm	C
1-dB Compression Point	f_C = 70 MHz		3	dBm	C
1-dB Compression Point	f_C = 140 MHz		2	dBm	C
Noise Figure	50 Ω System, 10 MHz, G = 6 dB		19.8	dB	C
Input Voltage Noise	f > 10 MHz		3.3	nV/√Hz	C
Input Current Noise	f > 10 MHz		1.7	pA/√Hz	C
DC PERFORMANCE					
Open-Loop Voltage Gain (A_{OL})			68	dB	C
Input Offset Voltage	T_A = 25°C		1	mV	C
Average Offset Voltage Drift	T_A = –40°C to 85°C		2.6	µV/°C	C
Input Bias Current	T_A = 25°C		6	µA	C
Average Bias Current Drift	T_A = –40°C to 85°C		20	nA/°C	C
Input Offset Current	T_A = 25°C		1.6	µA	C
Average Offset Current Drift	T_A = –40°C to 85°C		4	nA/°C	C
INPUT					
Common-Mode Input Range High			0.75	V	C
Common-Mode Input Range Low			–0.75	V	C
Common-Mode Rejection Ratio			90	dB	C

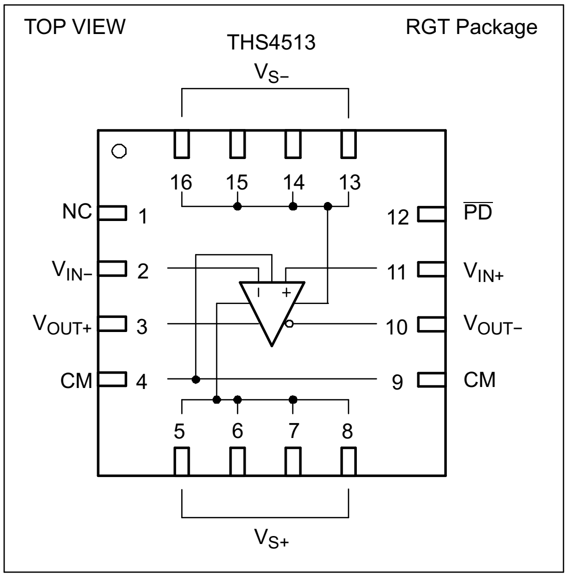
(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

SPECIFICATIONS; $V_{S+} – V_{S–}$ = 3 V: (continued)

Test conditions unless otherwise noted: V_{S+} = 1.5 V, $V_{S–}$ = –1.5 V, G = 0 dB, CM = open, V_O = 1 Vpp, R_F = 348 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS	TYP	UNIT	TEST LEVEL(1)
OUTPUT				
Maximum Output Voltage High	Each output with 100 Ω to mid-supply	0.45	V	C
Minimum Output Voltage Low		–0.45	V	
Differential Output Voltage Swing		1.8	V	
Differential Output Current Drive	R_L = 10 Ω	50	mA	
Output Balance Error	V_O = 100 mV, f = 1 MHz	–54	dB	
Closed-Loop Output Impedance	f = 1 MHz	0.3	Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL				
Small-Signal Bandwidth		150	MHz	
Slew Rate		60	V/µs	
Gain		1	V/V	
Output Common-Mode Offset from CM input	–0.5 V < CM < 0.5 V	4	mV	
CM Input Bias Current	–0.5 V < CM < 0.5 V	±40	µA	
CM Input Voltage Range		–1.5 to 1.5	V	
CM Input Impedance		20 || 1	kΩ || pF	
CM Default Voltage		0	V	
POWER SUPPLY				
Quiescent Current		34.8	mA	
Power Supply Rejection (±PSRR)		80	dB	
POWERDOWN				
Enable Voltage Threshold	Referenced to $V_{s–}$,Assured *on* above 2.1 V + $V_{S–}$	>2.1	V	
Disable Voltage Threshold	Assured *off* below 0.7 V + $V_{S–}$	<0.7	V	
Powerdown Quiescent Current		0.46	mA	
Input Bias Current	$\overline{PD}$ = $V_{S–}$	65	µA	
Input Impedance		50 || 2	kΩ || pF	
Turn-on Time Delay	Measured to output on	100	ns	
Turn-off Time Delay	Measured to output off	10	µs	

DEVICE INFORMATION



TERMINAL FUNCTIONS

TERMINAL (RGT PACKAGE)		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	V_{IN-}	Inverting amplifier input
3	V_{OUT+}	Non-inverted amplifier output
4,9	CM	Common-mode voltage input
5,6,7,8	V_{S+}	Positive amplifier power supply input
10	V_{OUT-}	Inverted amplifier output
11	V_{IN+}	Non-inverting amplifier input
12	$\overline{PD}$	Powerdown, $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation
13,14,15,16	V_{S-}	Negative amplifier power supply input

TYPICAL CHARACTERISTICS

TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 5$ V

Test conditions unless otherwise noted: V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 Vpp, R_F = 348 Ω, R_L = 200 Ω Differential, G = 0 dB, Single-Ended Input, Input and Output Referenced to Midsupply

Small-Signal Frequency Response	G = 0 dB, V_{OD} = 100 mV_{PP}		Figure 1
	G = 6 dB, V_{OD} = 100 mV_{PP}		Figure 2
Large Signal Frequency Response	G = 0 dB, V_{OD} = 2 V_{PP}		Figure 3
	G = 6 dB, V_{OD} = 2 V_{PP}		Figure 4
Harmonic Distortion	HD_2, G = 0 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 5
	HD_3, G = 0 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 6
	HD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 7
	HD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 8
	HD_2, G = 0 dB	vs Output Voltage	Figure 9
	HD_3, G = 0 dB	vs Output Voltage	Figure 10
	HD_2, G = 0 dB	vs CM Output Voltage	Figure 11
	HD_3, G = 0 dB	vs CM Output Voltage	Figure 12
Intermodulation Distortion	IMD_2, G = 0 dB	vs Frequency	Figure 13
	IMD_3, G = 0 dB	vs Frequency	Figure 14
Output Intercept Point	OIP_2	vs Frequency	Figure 15
	OIP_3	vs Frequency	Figure 16
S-Parameters		vs Frequency	Figure 17
Transition Rate		vs Output Voltage	Figure 18
Transient Response			Figure 19
Settling Time			Figure 20
Rejection Ratio		vs Frequency	Figure 21
Output Impedance		vs Frequency	Figure 22
Overdrive Recovery			Figure 23
Output Voltage Swing		vs Load Resistance	Figure 24
Turn-Off Time			Figure 25
Turn-On Time			Figure 26
Input Offset Voltage		vs Input Common-Mode Voltage	Figure 27
Open Loop Gain		vs Frequency	Figure 28
Input Referred Noise		vs Frequency	Figure 29
Noise Figure		vs Frequency	Figure 30
Quiescent Current		vs Supply Voltage	Figure 31
Power Supply Current		vs Supply Voltage in Powerdown Mode	Figure 32
Output Balance Error		vs Frequency	Figure 33
CM Input Impedence		vs Frequency	Figure 34
CM Small-Signal Frequency Response			Figure 35
CM Input Bias Current		vs CM Input Voltage	Figure 36
Differential Output Offset Voltage		vs CM Input Voltage	Figure 37
Output Common-Mode Offset		vs CM Input Voltage	Figure 38

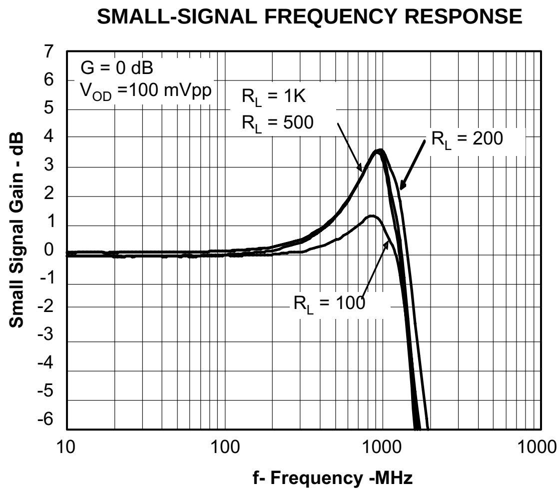


Figure 1.

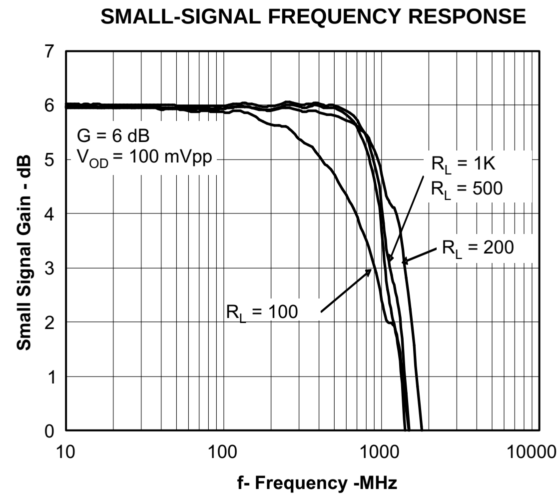


Figure 2.

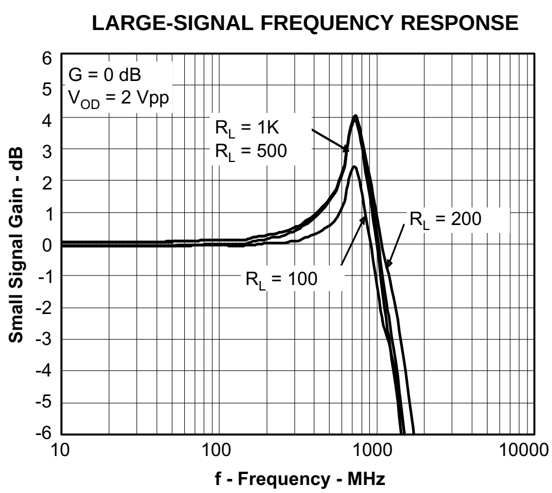


Figure 3.

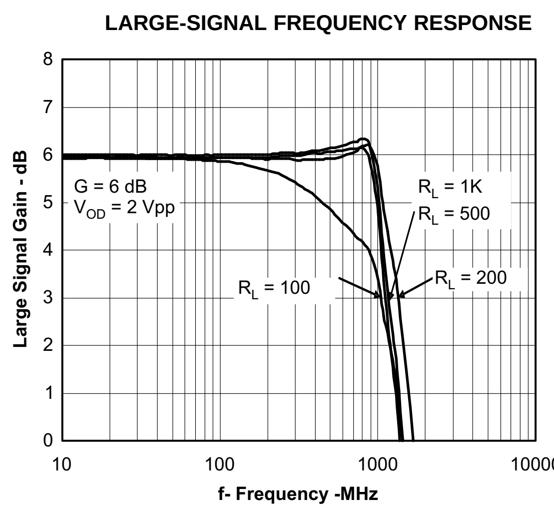


Figure 4.

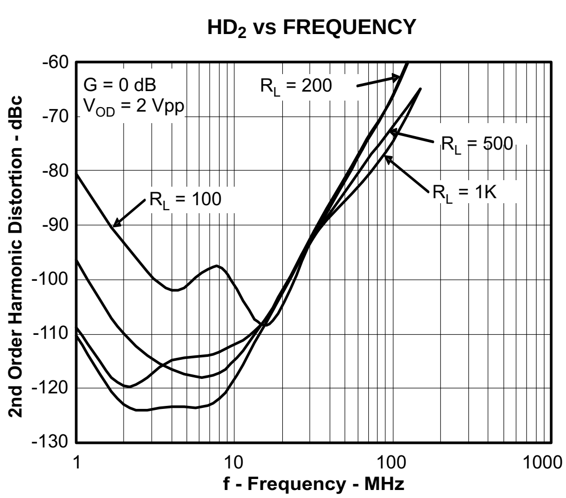


Figure 5.

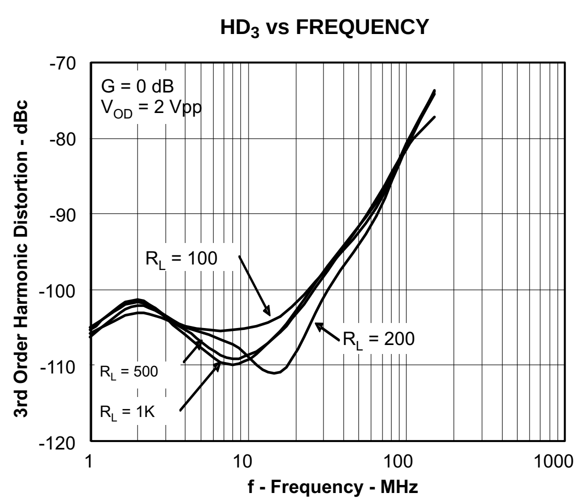


Figure 6.

HD_2 vs FREQUENCY

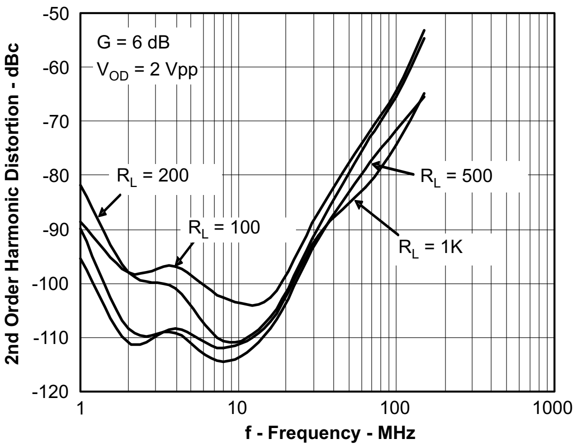


Figure 7.

HD_3 vs FREQUENCY

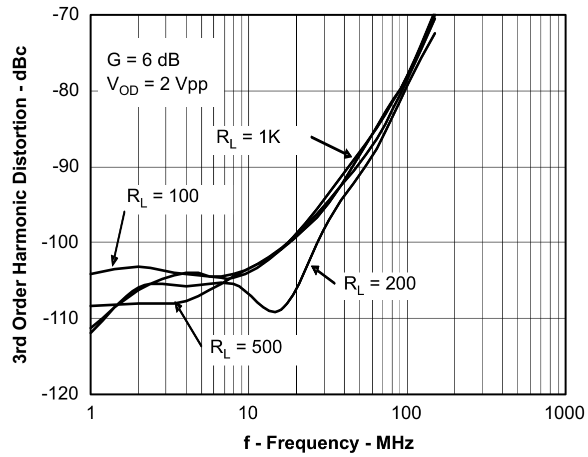


Figure 8.

HD_2 vs OUTPUT VOLTAGE

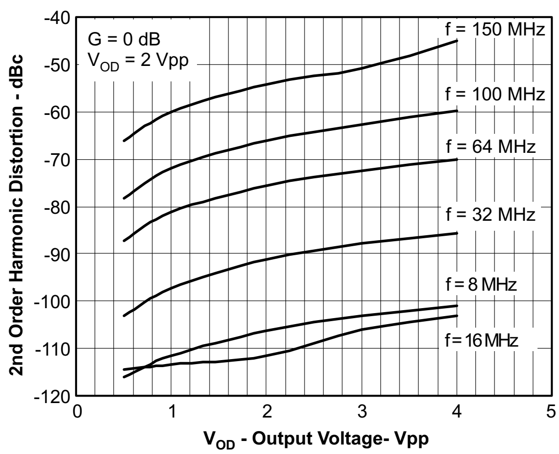


Figure 9.

HD_3 vs OUTPUT VOLTAGE

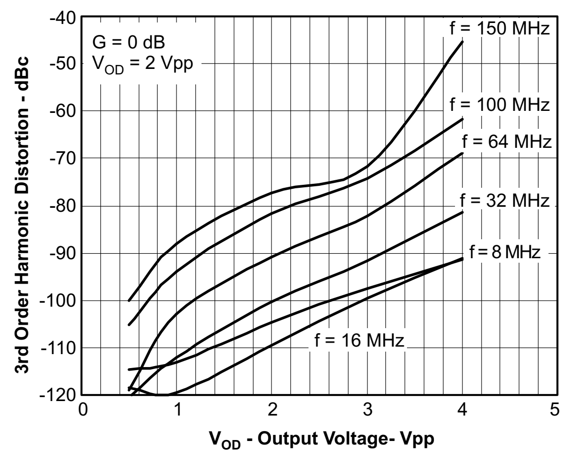


Figure 10.

HD_2 vs OUTPUT COMMON-MODE VOLTAGE

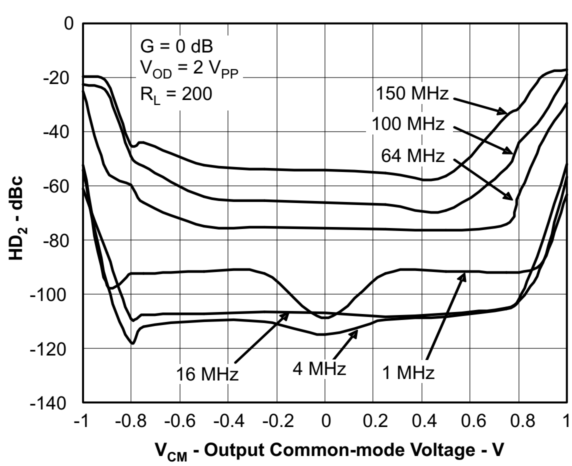


Figure 11.

HD_3 vs OUTPUT COMMON-MODE VOLTAGE

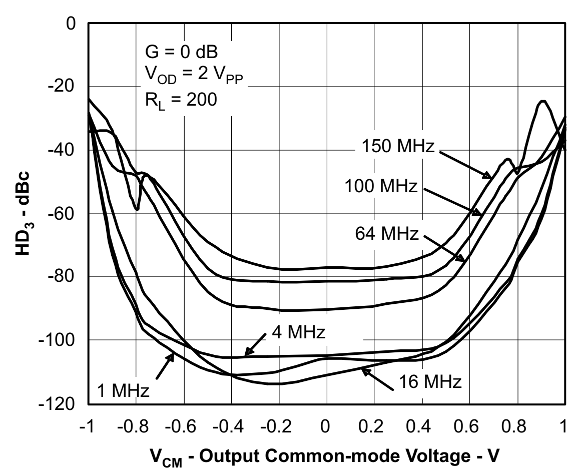


Figure 12.

IMD_2 vs FREQUENCY

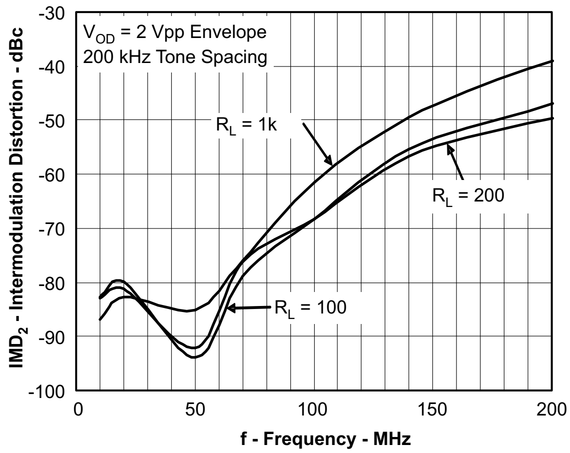


Figure 13.

IMD_3 vs FREQUENCY

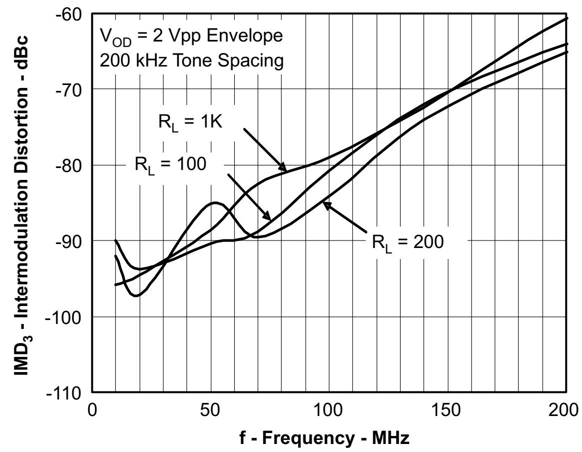


Figure 14.

OIP_2 vs FREQUENCY

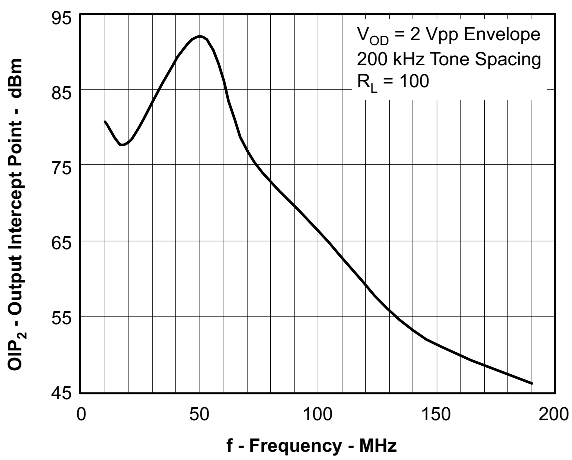


Figure 15.

OIP_3 vs FREQUENCY

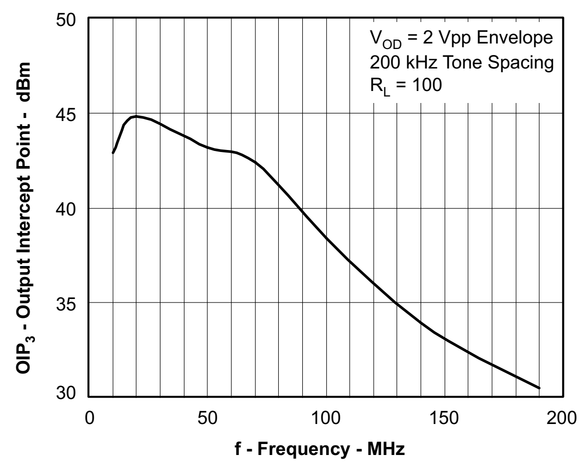


Figure 16.

S-PARAMETERS vs FREQUENCY

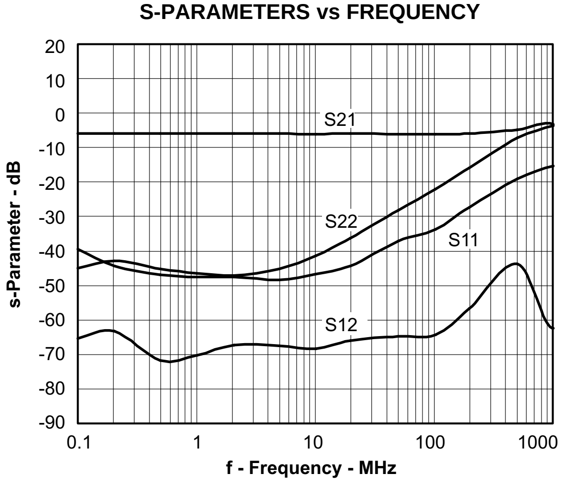


Figure 17.

TRANSITION RATE vs OUTPUT VOLTAGE

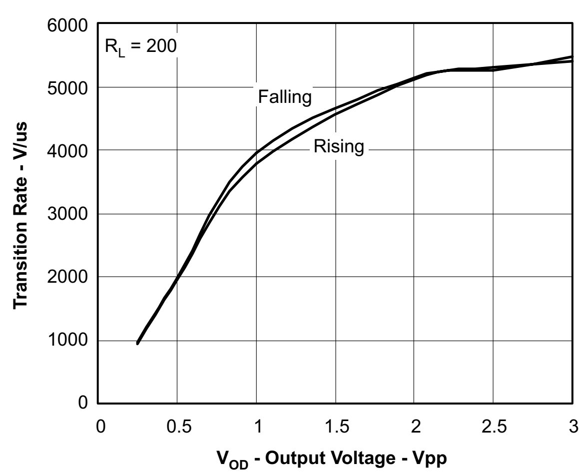


Figure 18.

TEXAS INSTRUMENTS
www.ti.com

TRANSIENT RESPONSE

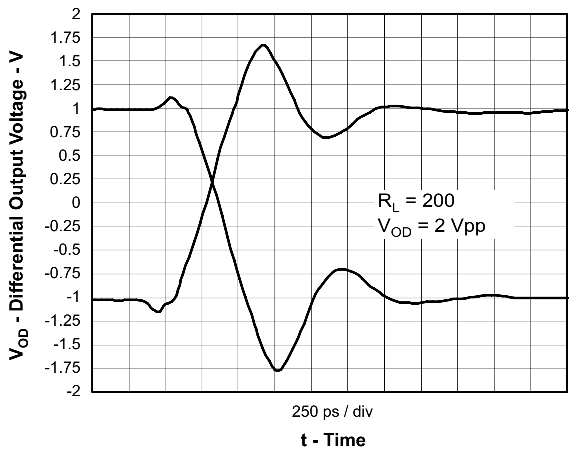


Figure 19.

SETTLING TIME

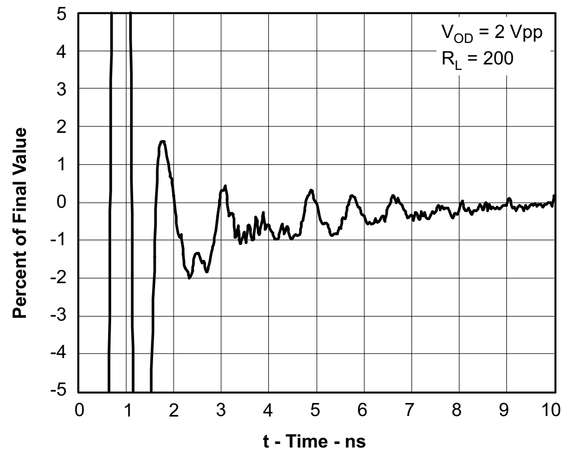


Figure 20.

REJECTION RATIO vs FREQUENCY

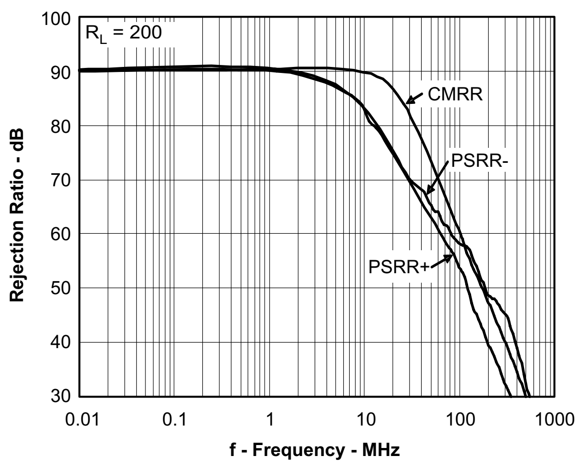


Figure 21.

OUTPUT IMPEDANCE vs FREQUENCY

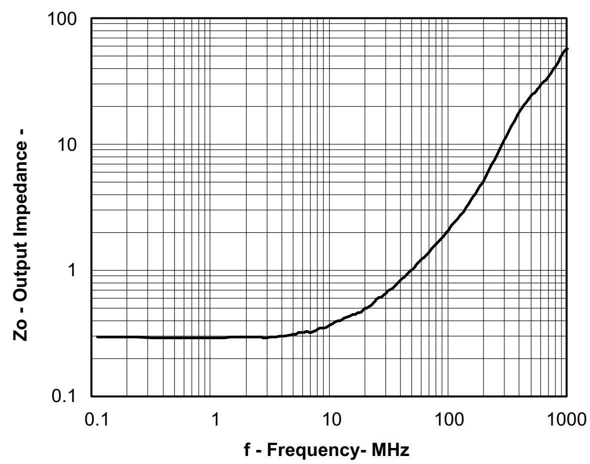


Figure 22.

OVERDRIVE RECOVERY

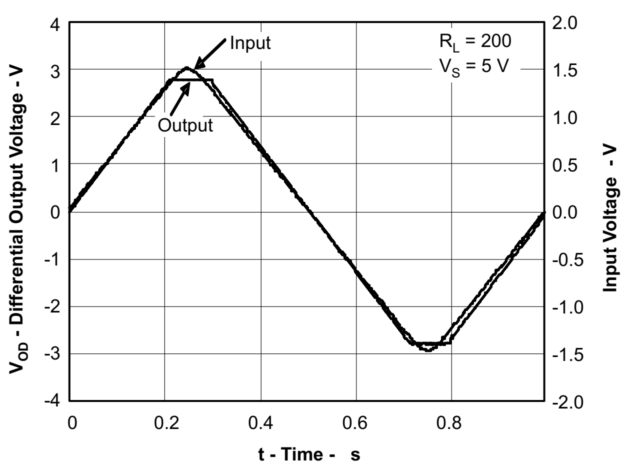


Figure 23.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

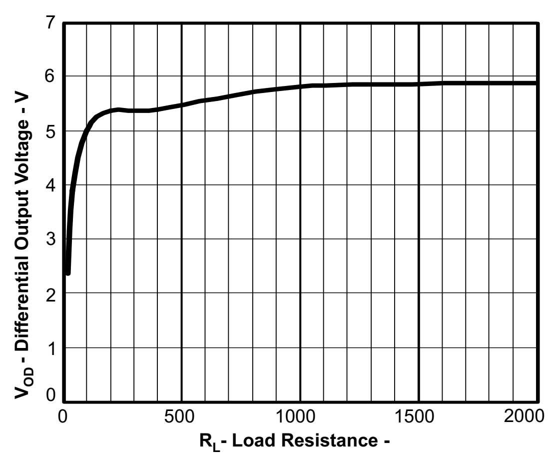


Figure 24.

TURN-OFF TIME

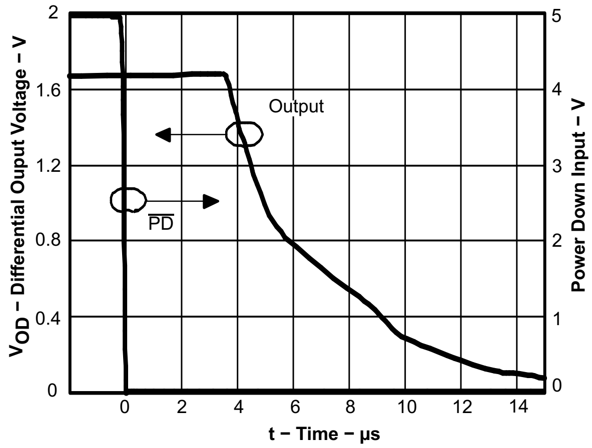


Figure 25.

TURN-ON TIME

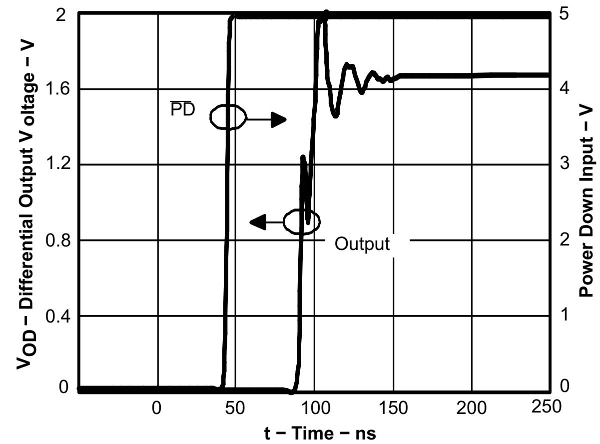


Figure 26.

INPUT OFFSET VOLTAGE vs
INPUT COMMON-MODE VOLTAGE

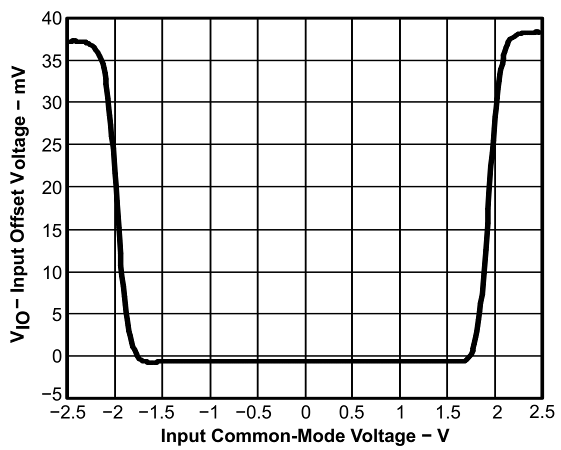


Figure 27.

OPEN-LOOP GAIN vs FREQUENCY

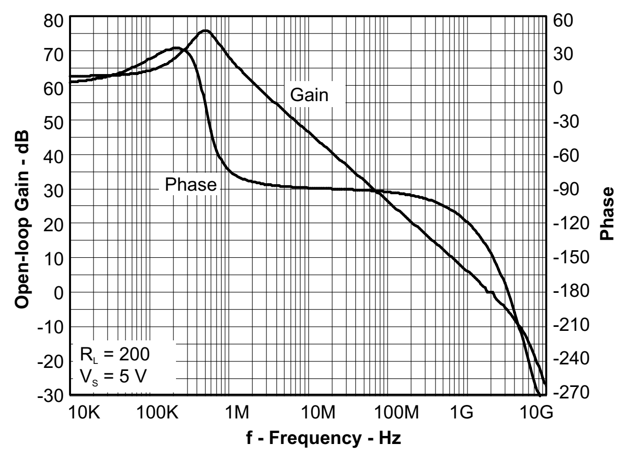


Figure 28.

INPUT REFERRED NOISE vs FREQUENCY

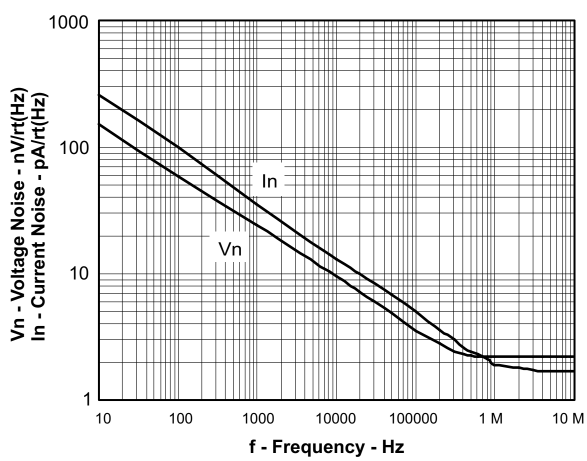


Figure 29.

NOISE FIGURE vs FREQUENCY

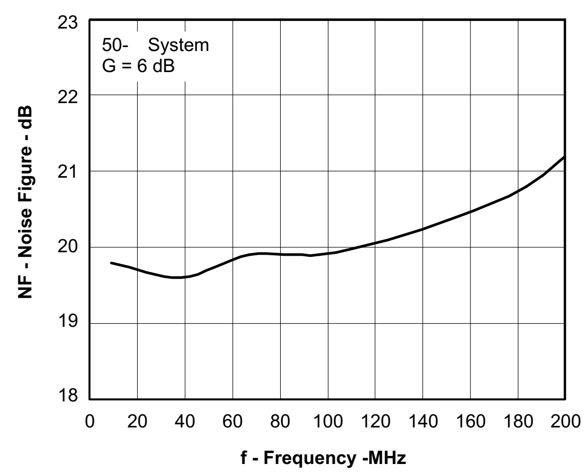


Figure 30.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

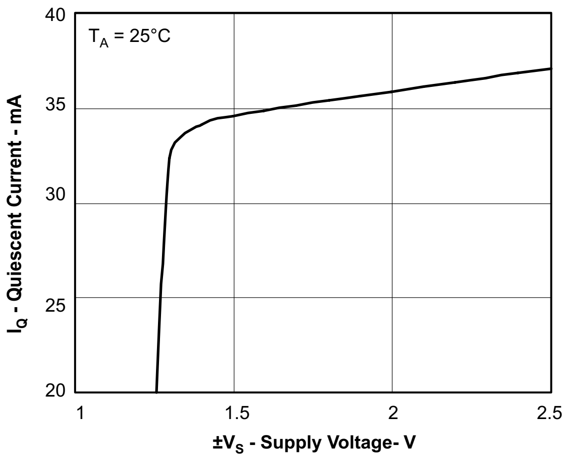


Figure 31.

POWERDOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

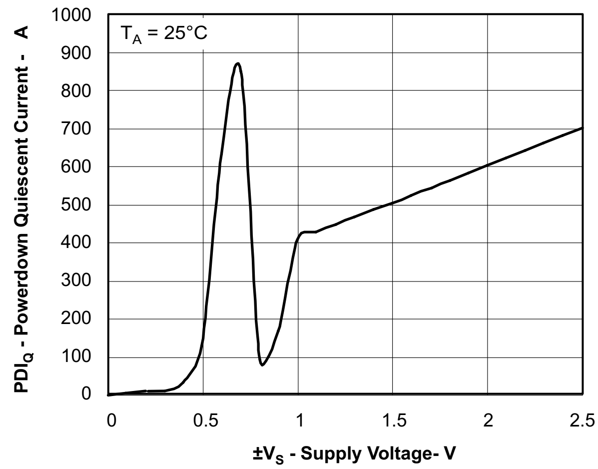


Figure 32.

OUTPUT BALANCE ERROR RESPONSE vs FREQUENCY

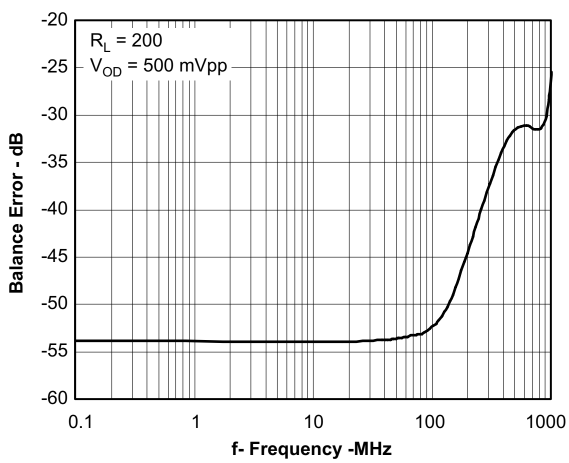


Figure 33.

CM INPUT IMPEDANCE vs FREQUENCY

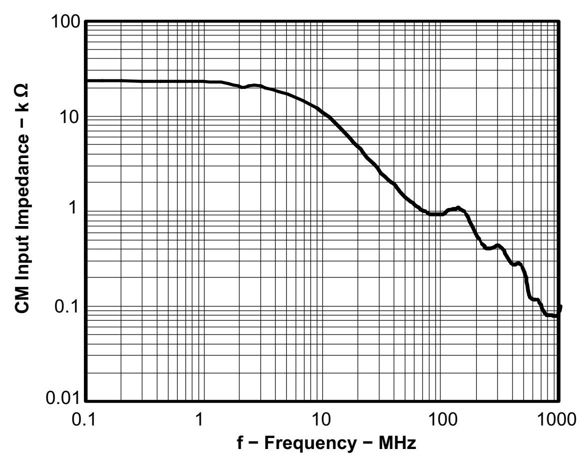


Figure 34.

CM SMALL SIGNAL FREQUENCY RESPONSE

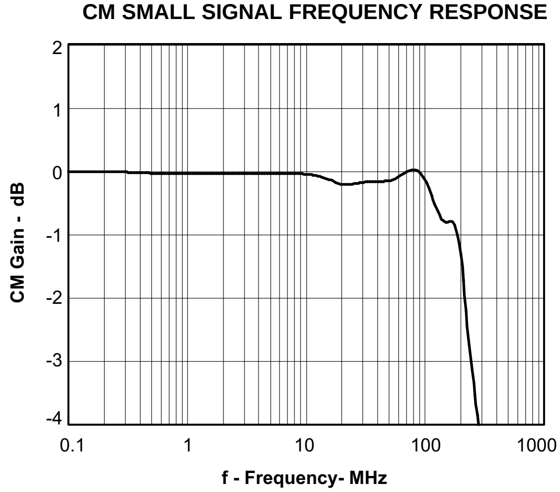


Figure 35.

CM INPUT BIAS CURRENT vs CM INPUT VOLTAGE

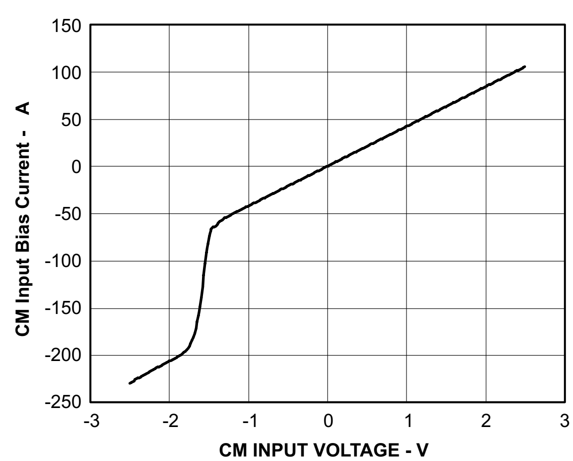


Figure 36.

DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs CM INPUT COMMON-MODE VOLTAGE

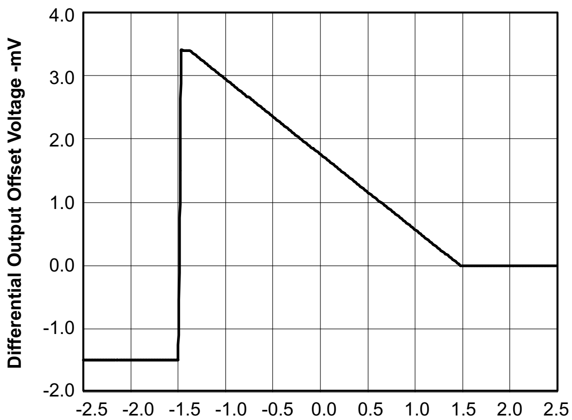


Figure 37.

OUTPUT COMMON-MODE OFFSET
vs CM INPUT VOLTAGE

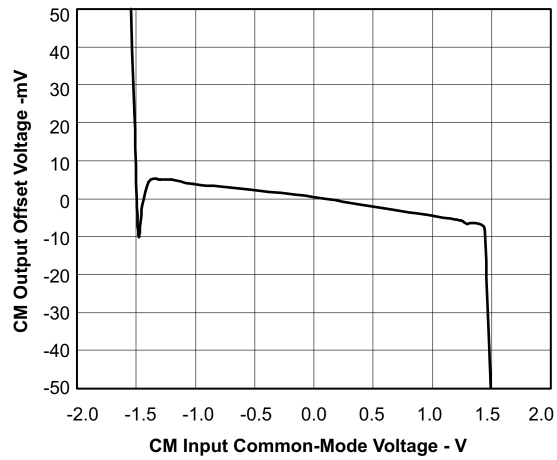


Figure 38.

TYPICAL AC PERFORMANCE: $V_{S+}– V_{S–}$ = 3 V

Test conditions unless otherwise noted: V_{S+} = +1.5 V, $V_{S–}$ = –1.5V, CM = open, V_{OD} = 1 Vpp, R_F = 348 Ω, R_L = 200 Ω Differential, G = 0 dB, Single-Ended Input, Input and Output Referenced to Midsuply

Small-Signal Frequency Response	G = 0 dB, V_{OD} = 100 mV_{PP}		Figure 39
	G = 6 dB, V_{OD} = 100 mV_{PP}		Figure 40
Large Signal Frequency Response	G = 0 dB, V_{OD} = 1 V_{PP}		Figure 41
	G = 6 dB, V_{OD} = 1 V_{PP}		Figure 42
Harmonic Distortion	HD_2, G = 0 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 43
	HD_3, G = 0 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 44
	HD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 45
	HD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 46
	HD_2, G = 0 dB	vs Output Voltage	Figure 47
	HD_3, G = 0 dB	vs Output Voltage	Figure 48
	HD_2, G = 0 dB	vs CM Output Voltage	Figure 49
	HD_3, G = 0 dB	vs CM Output Voltage	Figure 50
Intermodulation Distortion	IMD_2, G = 0 dB	vs Frequency	Figure 51
	IMD_3, G = 0 dB	vs Frequency	Figure 52
Ouput Intercept Point	OIP_2	vs Frequency	Figure 53
	OIP_3	vs Frequency	Figure 54
S-Parameters		vs Frequency	Figure 55
Transition Rate		vs Output Voltage	Figure 56
Transient Response			Figure 57
Settling Time			Figure 58
Output Voltage Swing		vs Load Resistance	Figure 59
Rejection Ratio		vs Frequency	Figure 60
Overdrive Recovery			Figure 61
Output Impedance		vs Frequency	Figure 62
Turn-Off Time			Figure 63
Turn-On Time			Figure 64
Ouput Balance Error		vs Frequency	Figure 65
Noise Figure		vs Frequency	Figure 66
CM Small-Signal Frequency Response			Figure 67
CM Input Impedance		vs Frequency	Figure 68
Differential Output Offset Voltage		vs CM Input Voltage	Figure 69
Output Common-Mode Offset		vs CM Input Voltage	Figure 70

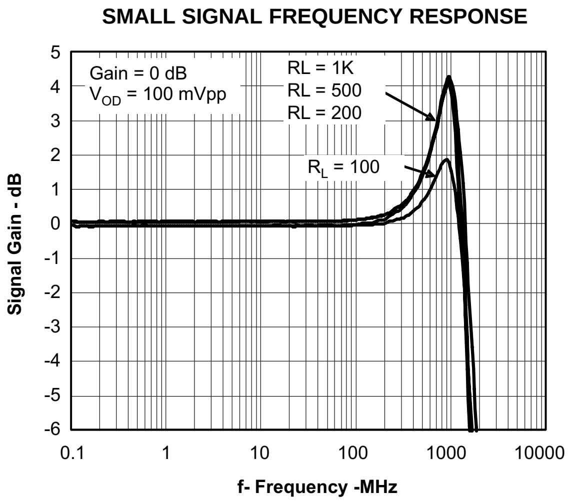


Figure 39.

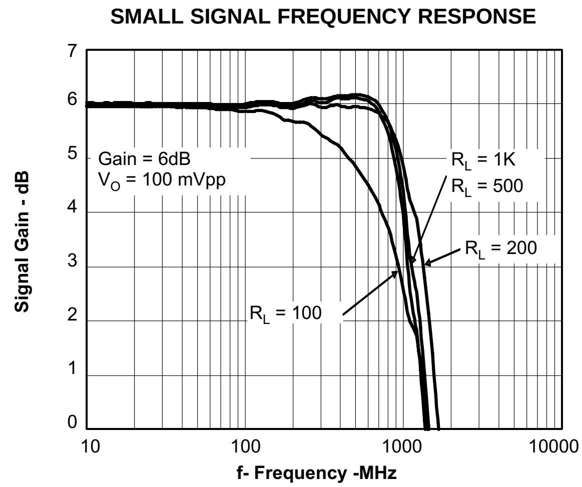


Figure 40.

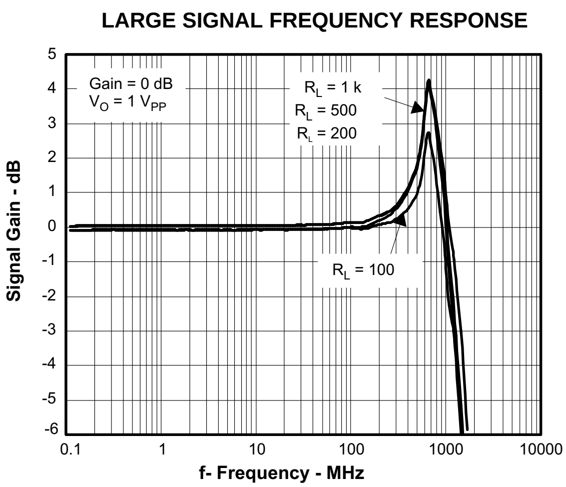


Figure 41.

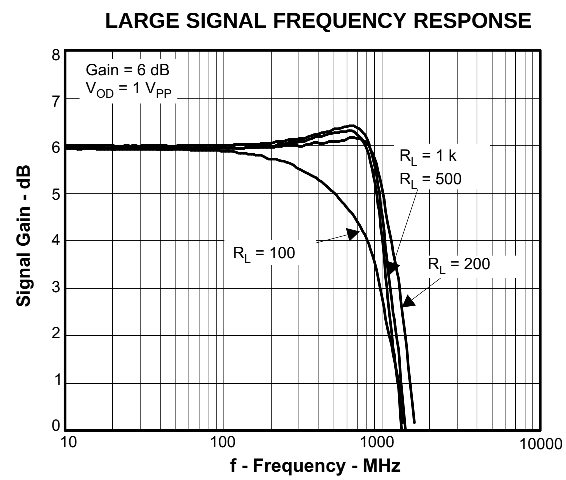


Figure 42.

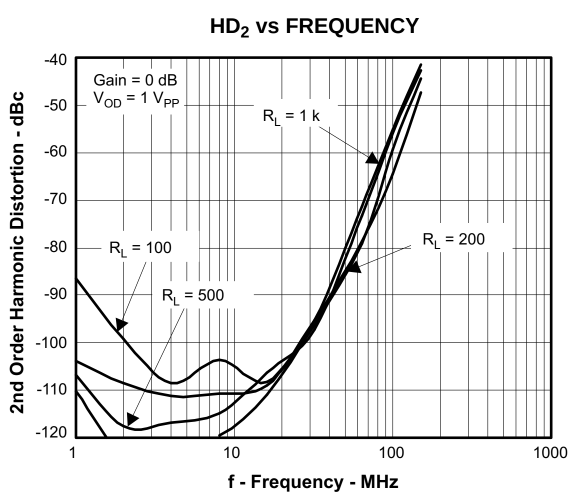


Figure 43.

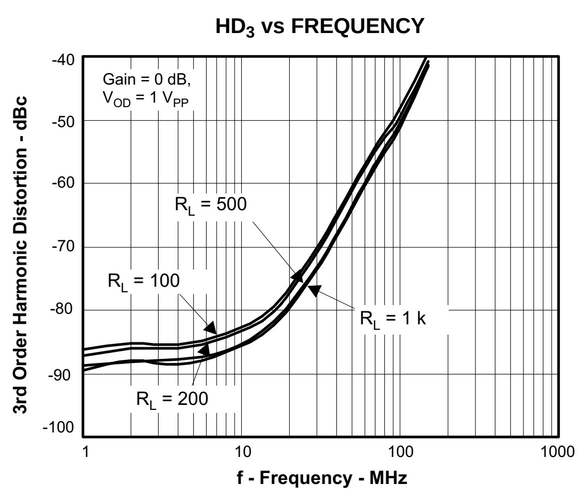


Figure 44.

HD_2 vs FREQUENCY

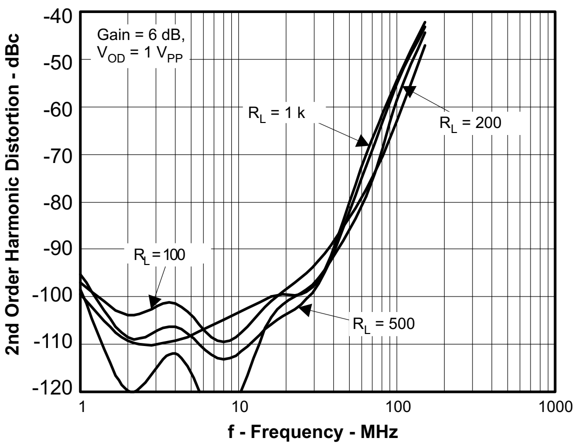


Figure 45.

HD_3 vs FREQUENCY

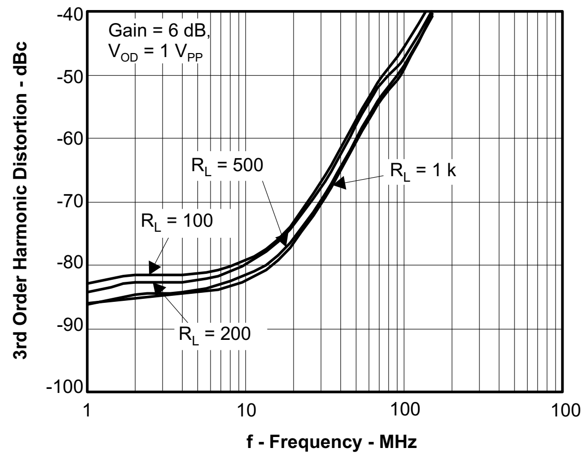


Figure 46.

HD_2 vs OUTPUT VOLTAGE

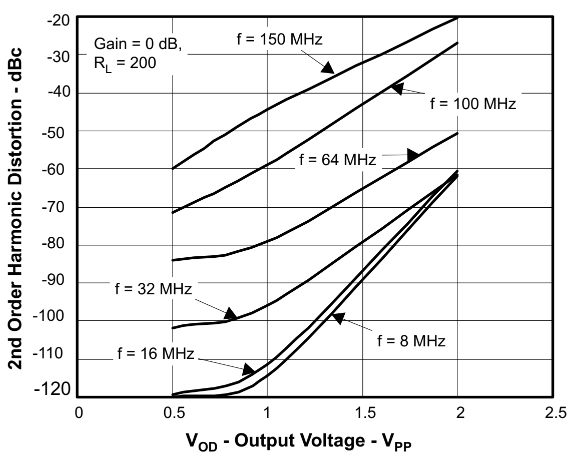


Figure 47.

HD_3 vs OUTPUT VOLTAGE

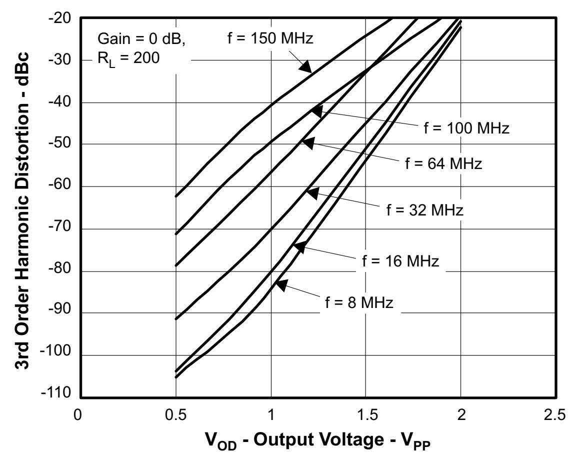


Figure 48.

HD_2 vs OUTPUT COMMON-MODE VOLTAGE

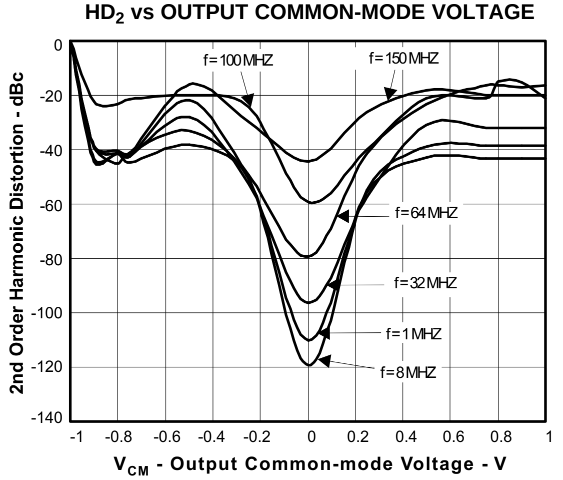


Figure 49.

HD_3 vs OUTPUT COMMON-MODE VOLTAGE

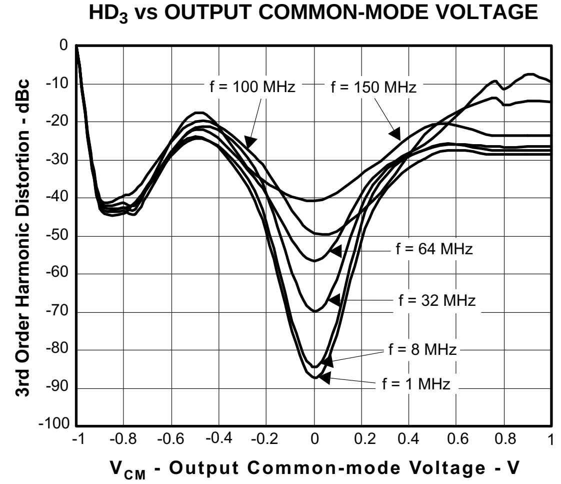


Figure 50.

IMD2 vs FREQUENCY

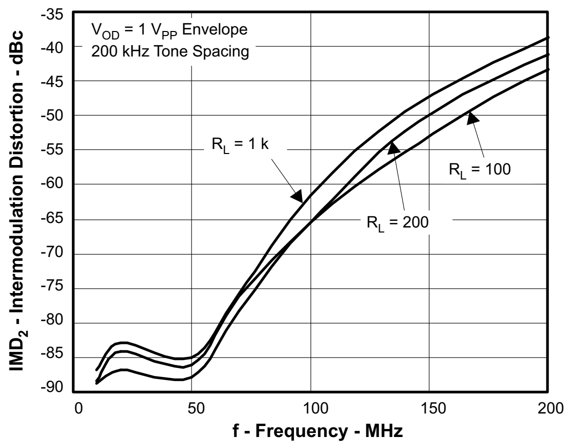


Figure 51.

IMD3 vs FREQUENCY

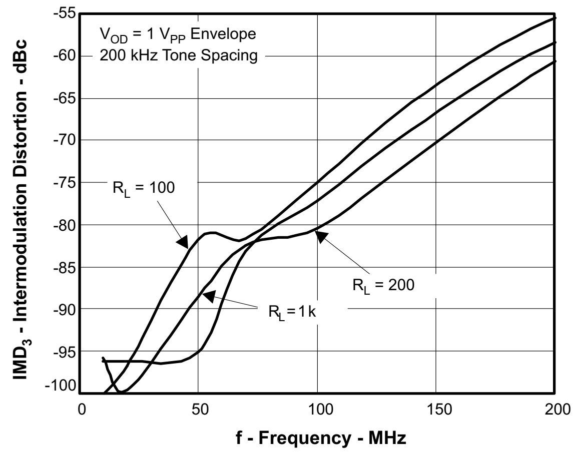


Figure 52.

OIP2 vs FREQUENCY

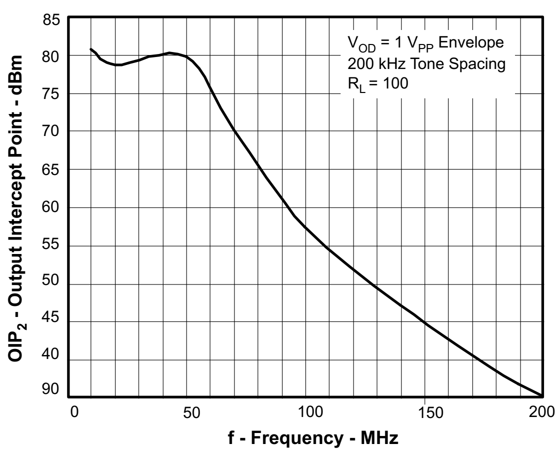


Figure 53.

OIP3 vs FREQUENCY

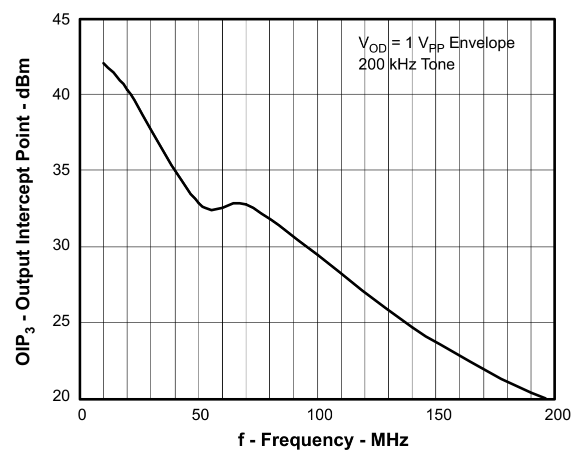


Figure 54.

S-PARAMETERS vs FREQUENCY

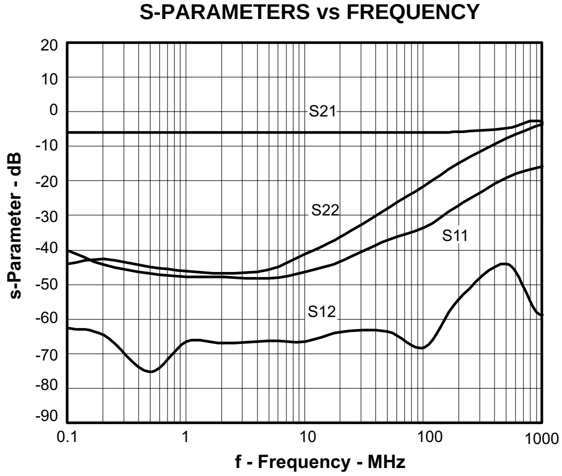


Figure 55.

TRANSITION RATE vs OUTPUT VOLTAGE

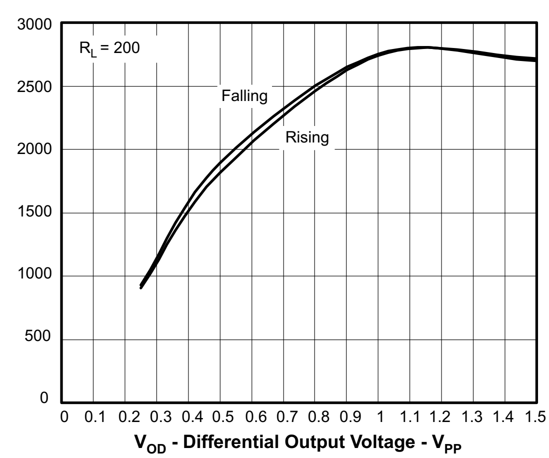


Figure 56.

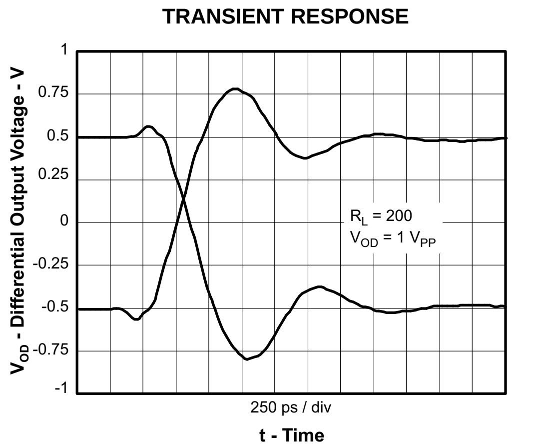


Figure 57.

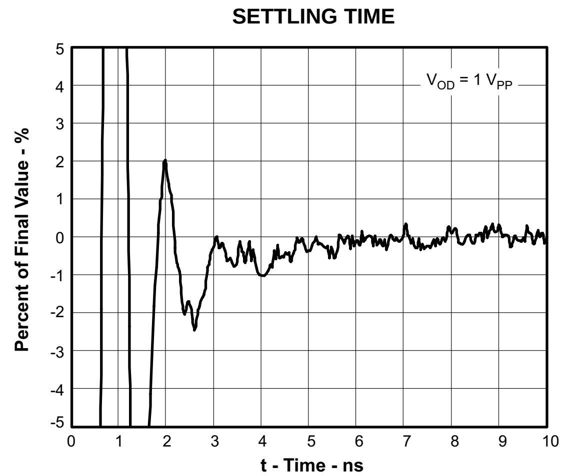


Figure 58.

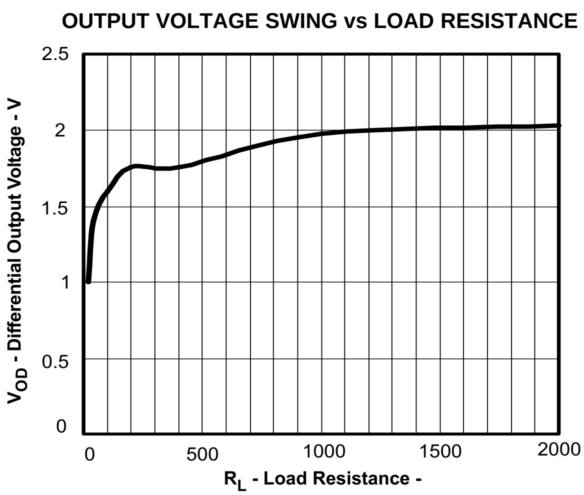


Figure 59.

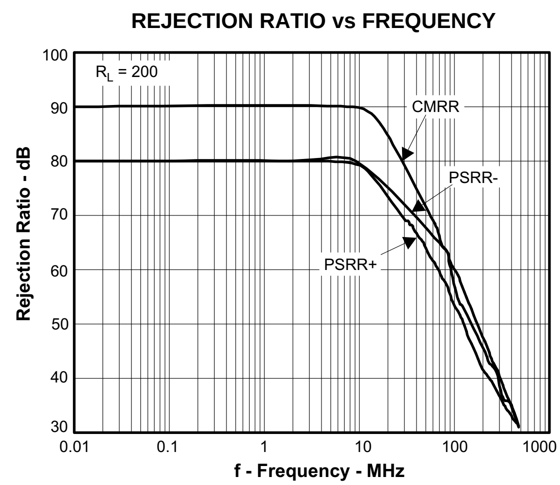


Figure 60.

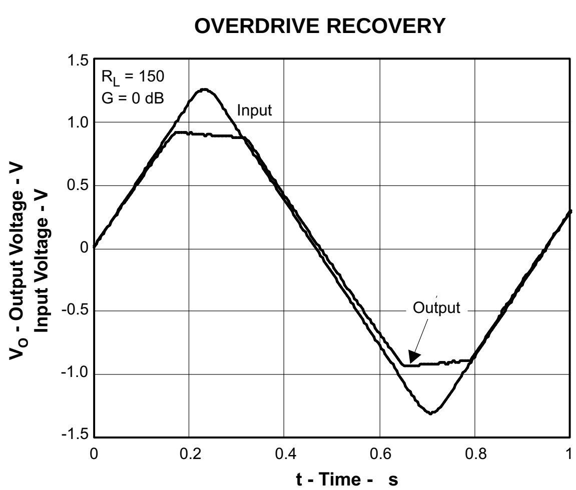


Figure 61.

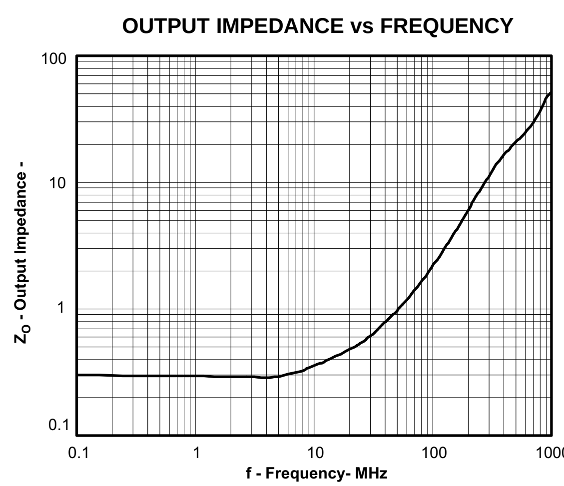


Figure 62.

TURN-OFF TIME

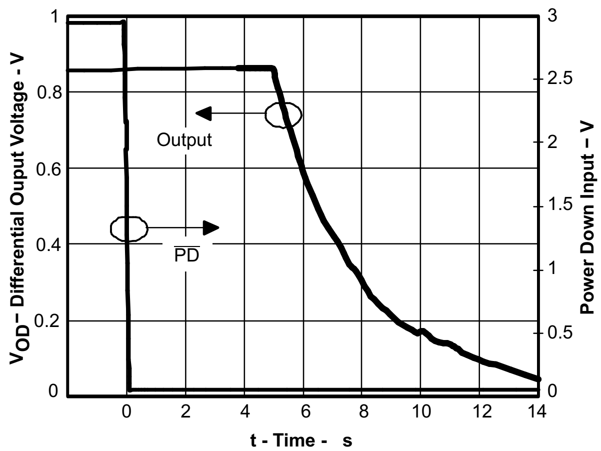


Figure 63.

TURN-ON TIME

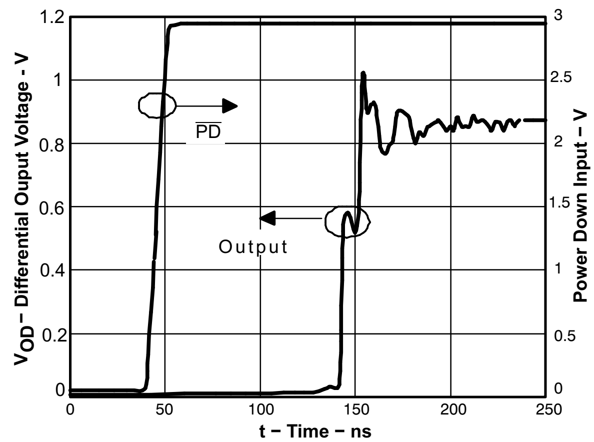


Figure 64.

OUTPUT BALANCE ERROR vs FREQUENCY

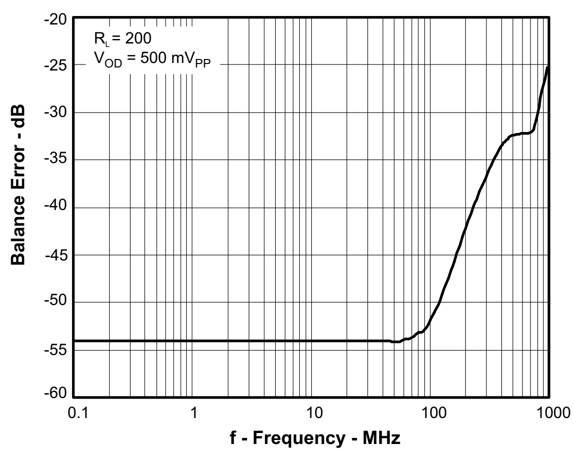


Figure 65.

NOISE FIGURE vs FREQUENCY

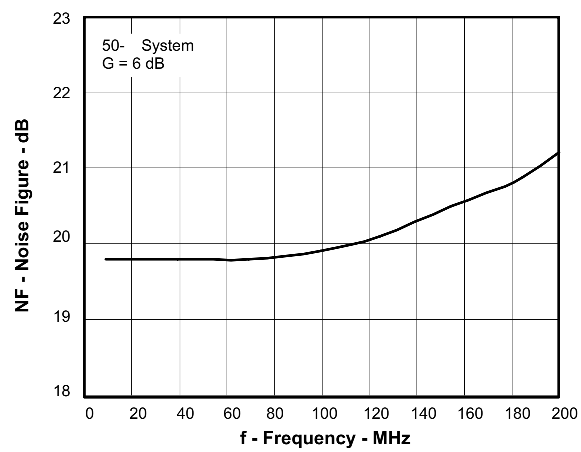


Figure 66.

CM SMALL SIGNAL FREQUENCY RESPONSE

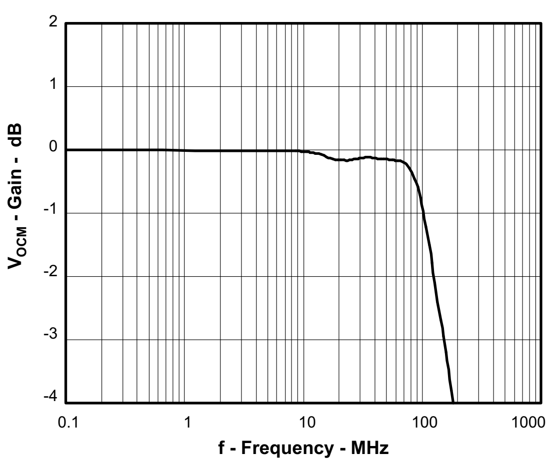


Figure 67.

CM INPUT IMPEDANCE vs FREQUENCY

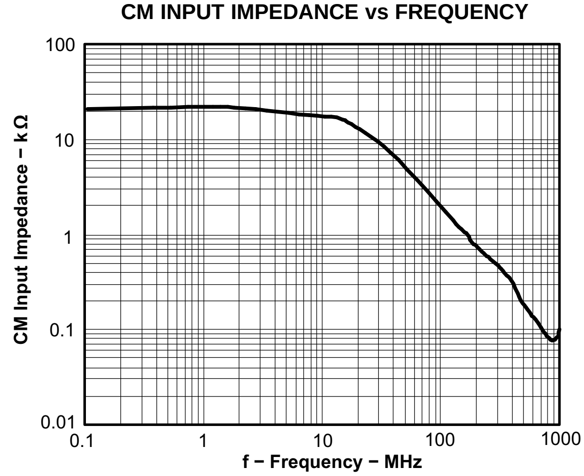


Figure 68.

DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs CM INPUT VOLTAGE

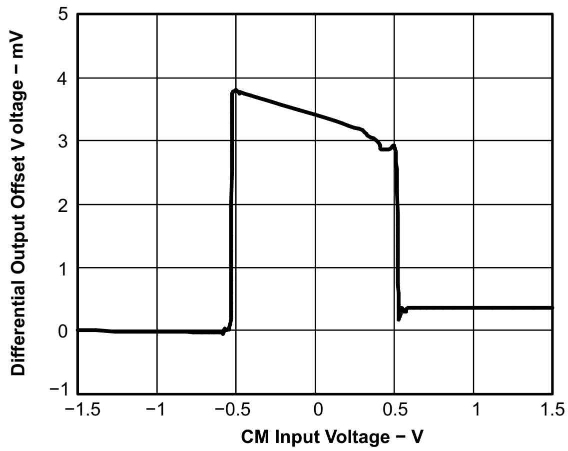


Figure 69.

OUTPUT COMMON-MODE OFFSET vs CM INPUT VOLTAGE

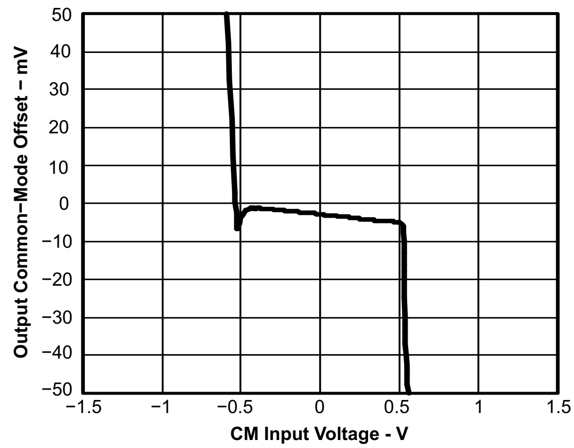


Figure 70.

TEST CIRCUITS

The THS4513 is tested with the following test circuits built on the EVM. For simplicity, power supply decoupling is not shown – see layout in the applications section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50-Ω sources and a 0.22-µF capacitor and a 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in the applications section with no impact on performance.

Table 1. Gain Component Values

GAIN	R_F	R_G	R_{IT}
0 dB	348 Ω	340 Ω	56.2 Ω
6 dB	348 Ω	66.5 Ω	61.4 Ω

Note the gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 2. Load Component Values

R_L	R_O	R_{OT}	Atten.
100 Ω	25 Ω	open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 72, the signal will see slightly more loss, and these numbers will be approximate.

Frequency Response

The circuit shown in Figure 71 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

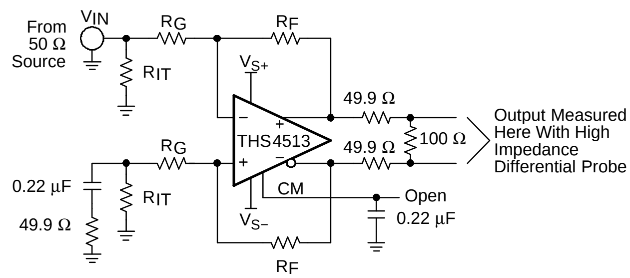


Figure 71. Frequency Response Test Circuit

Distortion and 1dB Compression

The circuit shown in Figure 72 is used to measure harmonic distortion, intermodulation distortion, and 1-db compression point of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1MHz.

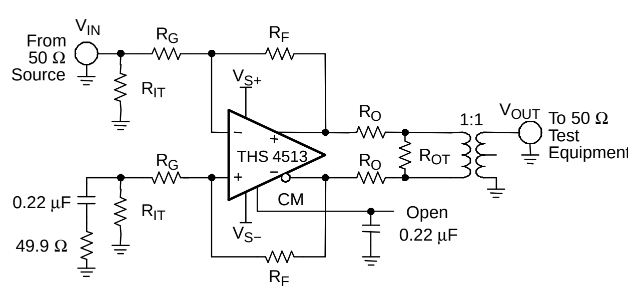


Figure 72. Distortion Test Circuit

The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or

100-Ω termination as shown in Table 2. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to refer to the amplifier output.

S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in Figure 73 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open and the drop across the 49.9 Ω resistor is used to calculate the impedance seen looking into the amplifier's output.

Because S_{21} is measured single-ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier's output as a differential signal.

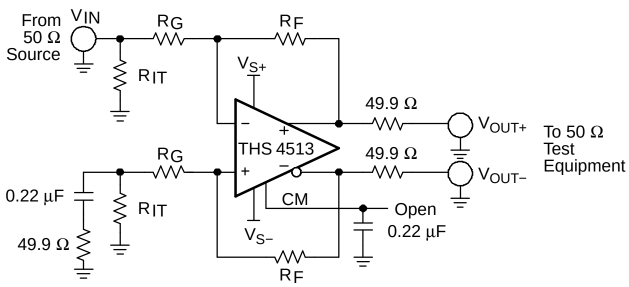


Figure 73. S-Parameter, SR, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turn-on/off Test Circuit

CM Input

The circuit shown in Figure 74 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at V_{OUT+} or V_{OUT-} with the input injected at V_{IN}, R_{CM} = 0 Ω and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

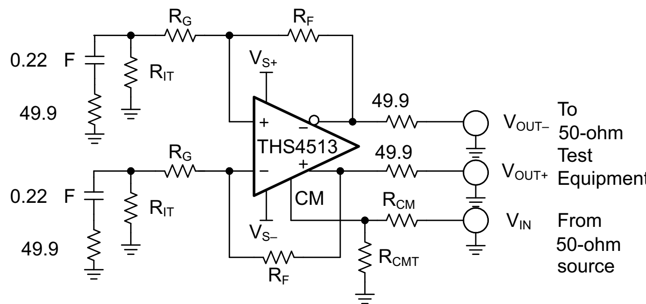


Figure 74. CM Input Test Circuit

CMRR and PSRR

The circuit shown in Figure 75 is used to measure the CMRR and PSRR of V_{S+} and V_{S-}. The input is switched appropriately to match the test being performed.

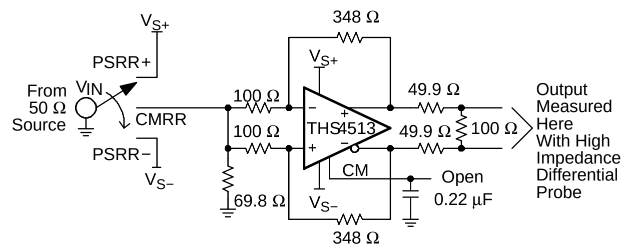


Figure 75. CMRR and PSRR Test Circuit

APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4513. For simplicity, power supply decoupling capacitors are not shown in these diagrams. Please see the SubSec2 0.1 section for recommendations. For more detail on the use and operation of fully differential op amps refer to application report *Fully-Differential Amplifiers* (SLOA054) .

Differential Input to Differential Output Amplifier

The THS4513 is a fully differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 76 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

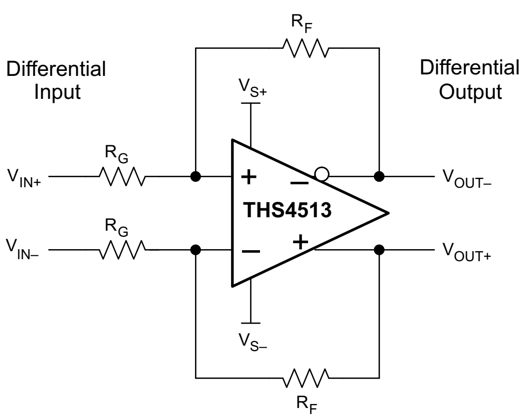


Figure 76. Differential Input to Differential Ouput Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

Single-Ended Input to Differential Output Amplifier

The THS4513 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 77 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

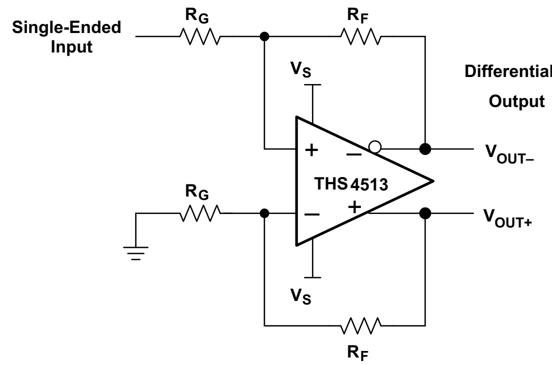


Figure 77. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-model voltage of a fully differential op amp is the voltage at the '+' and '–' input pins of the op amp.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} \quad V_{OUT} \quad \frac{R_G}{R_G \quad R_F} \quad V_{IN} \quad \frac{R_F}{R_G \quad R_F} \tag{1}$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typ) from the set voltage, when set within 0.5 V of mid-supply, with less than 4mV differential offset voltage. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 78 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} \quad \frac{2V_{CM} \quad V_S \quad V_S}{50\ k} \tag{2}$$

where V_{CM} is the voltage applied to the CM pin.

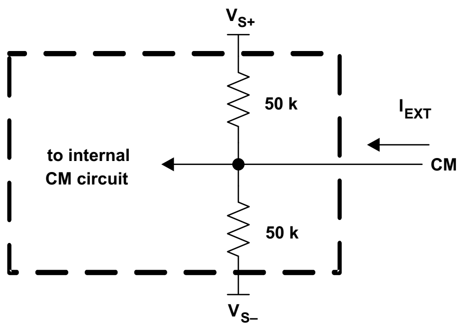


Figure 78. CM Input Circuit

Single-Supply Operation (3V to 5V)

To facilitate testing with common lab equipment, the THS4513 EVM allows split-supply operation, and the characterization data presented in this data sheet was taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 79, Figure 80, and Figure 81 show DC and AC-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to mid-supply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 79, the signal source is referenced to a voltage derived from the CM pin via a unity-gain wideband buffer such as the BUF602. V_{CM} is set to mid-supply by THS4513 internal circuitry. R_T along with the input impedance of the amplifier provides input termination, which is also referenced to V_{CM}.

Note that R_S and R_T are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value R_G+ $R_S||R_T$ on this input. This is also true of the circuits shown in Figure 80 and Figure 81.

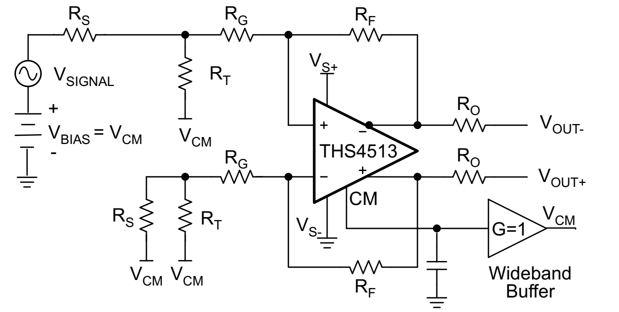


Figure 79. THS4513 DC Coupled Single-Supply with Input Biased to V_{CM}

In Figure 80 the source is referenced to ground and so is the input termination resistor. R_{PU} is added to the circuit to avoid violating the V_{ICR} of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} \quad \frac{V_{IC} \quad V_S}{V_{CM} \quad \frac{1}{R_F} \quad V_{IC} \quad \frac{1}{R_{IN}} \quad \frac{1}{R_F}} \tag{3}$$

V_{IC} is the desire input common-mode voltage, V_{CM} = CM, and R_{IN} = R_G+ $R_S||R_T$. To set to mid-supply, make the value of R_{PU} = R_G+ $R_S||R_T$.

Table 3 is a modification of Table 1 to add the proper values with R_{PU} assuming a 50 Ω source impedance and setting the input and output common-mode voltage to mid-supply.

There are two drawbacks to this configuration. One is it requires additional current from the power supply. Using the values shown for a gain of 0 dB requires 14 mA more current with 5 V supply, and 8.2 mA more current with 3 V supply.

The other drawback is this configuration also increases the noise gain of the circuit. In the 10 dB gain case, noise gain increases by a factor of 1.5.

Table 3. RPU Values for Various Gains

Gain	R_F	R_G	R_{IT}	R_{PU}
0 dB	348 Ω	340 Ω	56.2 Ω	365 Ω
6 dB	348 Ω	168 Ω	64.9 Ω	200 Ω

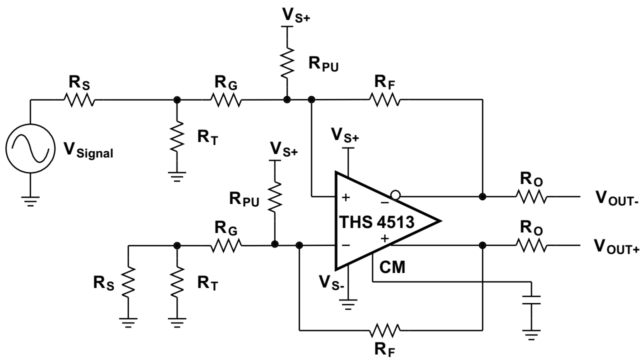


Figure 80. THS4513 DC Coupled Single-Supply with R_{PU} Used to Set V_{IC}

Figure 81 shows AC coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to mid-supply.

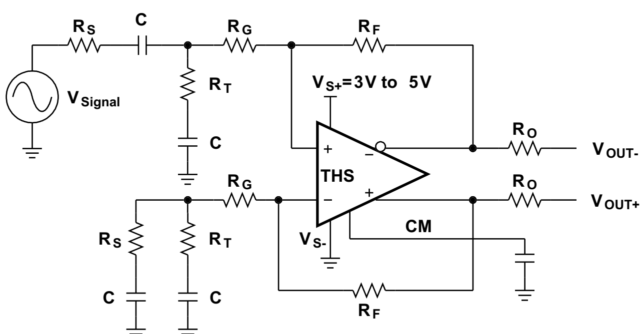


Figure 81. THS4513 AC Coupled Single-Supply

Low Pass Filter

One application for the THS4513 is as a unity-gain buffer with low-pass filtering. Figure 82 shows a circuit that is driven by an AC-coupled 50-Ω source. A 1:1 transformer converts the differential output of the THS4513 into a single-ended output capable of driving 50-Ω test equipment. The circuit as shown has an overall gain of -6dB due to the voltage divider on the device output, and has a roll-off frequency of approximately 60 MHz. The measured gain versus frequency response of the overall circuit is shown in Figure 83. The low-frequency roll-off is due to losses in the output transformer at those frequencies.

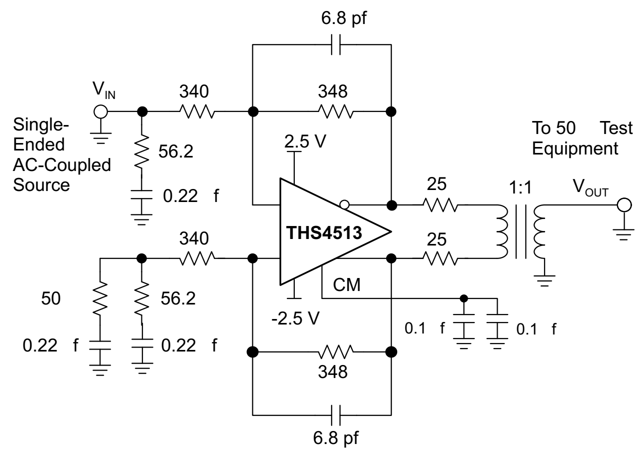


Figure 82. 60-MHz Low-Pass Filter

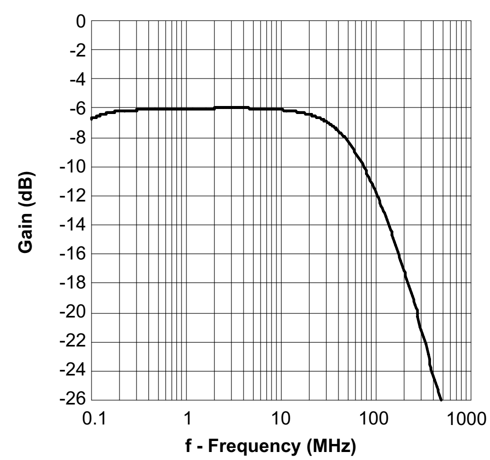


Figure 83. Low-Pass Filter Measured Frequency Response

THS4513 + ADS5500 Combined Performance

The THS4513 is designed to be a high performance drive amplifier for high performance data converters like the ADS5500 14-bit 125-MSPS ADC. Figure 84 shows a circuit combining the two devices. The THS4513 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500. The 100-Ω resistors and 2.7-pF capacitor between the THS4513 outputs and ADS5500 inputs along with the input capacitance of the ADS5500 limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an AC-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8-Ω resistor and 0.22-µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. Refer to Table 3 for component values to set proper 50-Ω termination for other common gains. A split power supply of +4V and -1V is used to set the input and output common-mode voltages to approximately mid-supply while setting the input common-mode of the ADS5500 to the recommended +1.55V. This maintains maximum headroom on the internal transistors of the THS4513 to insure optimum performance.

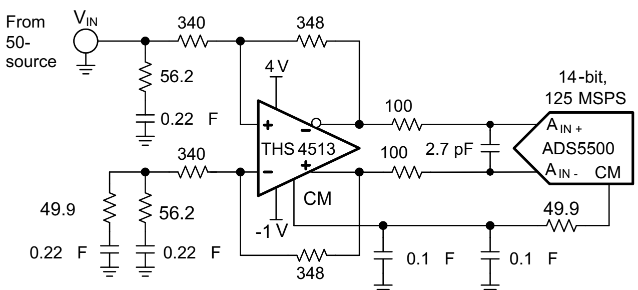


Figure 84. THS4513 + ADS5500 Circuit

Figure 85 shows the 2-tone FFT of the THS4513 + ADS5500 circuit with 65 MHz and 70 MHz input frequencies. The SFDR is 90 dBc.

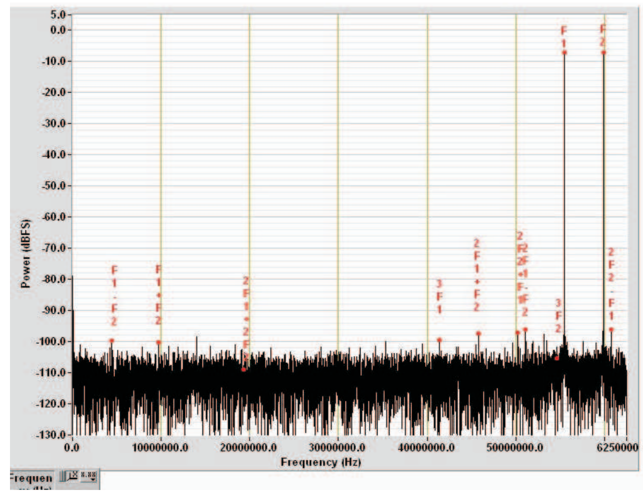


Figure 85. THS4513 + ADS5500 2-Tone FFT with 65 MHz and 70 MHz Input

THS4513 + ADS5424 Combined Performance

Figure 86 shows the THS4513 driving the ADS5424 ADC.

As before, the THS4513 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4513 + ADS5500 circuit.

The 225-Ω resistors and 2.7-pF capacitor between the THS4513 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100MHz (-3dB).

Since the ADS5424s recommended input common-mode voltage is 2.4 V, the THS4513 is operated from a single power supply input with V_{S+} = 5 V and V_{S-} = 0 V (ground).

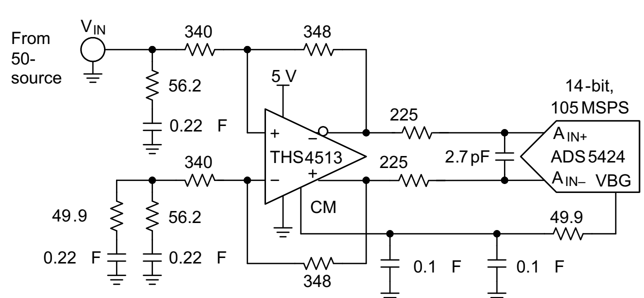


Figure 86. THS4513 + ADS5424 Circuit

Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the opamp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-µF and two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1-µF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4513 recommended PCB footprint is shown in Figure 87.

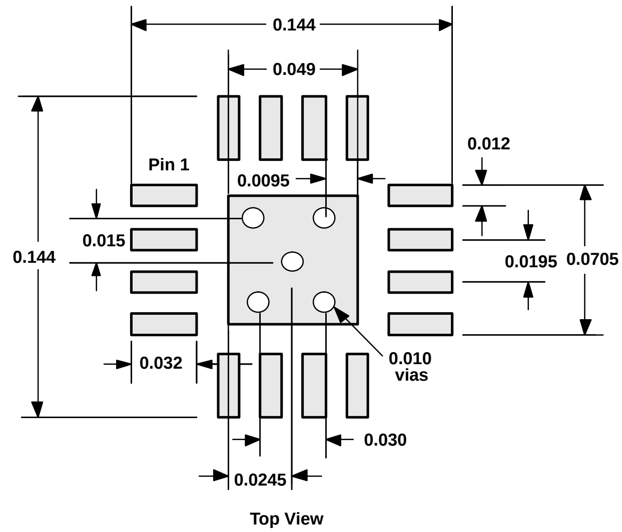


Figure 87. QFN Etch and Via Pattern

THS4513 EVM

Figure 88 is the THS4513 EVAL1 EVM schematic, layers 1 through 4 of the PCB are shown Figure 90, and Table 4 is the bill of material for the EVM as supplied from TI.

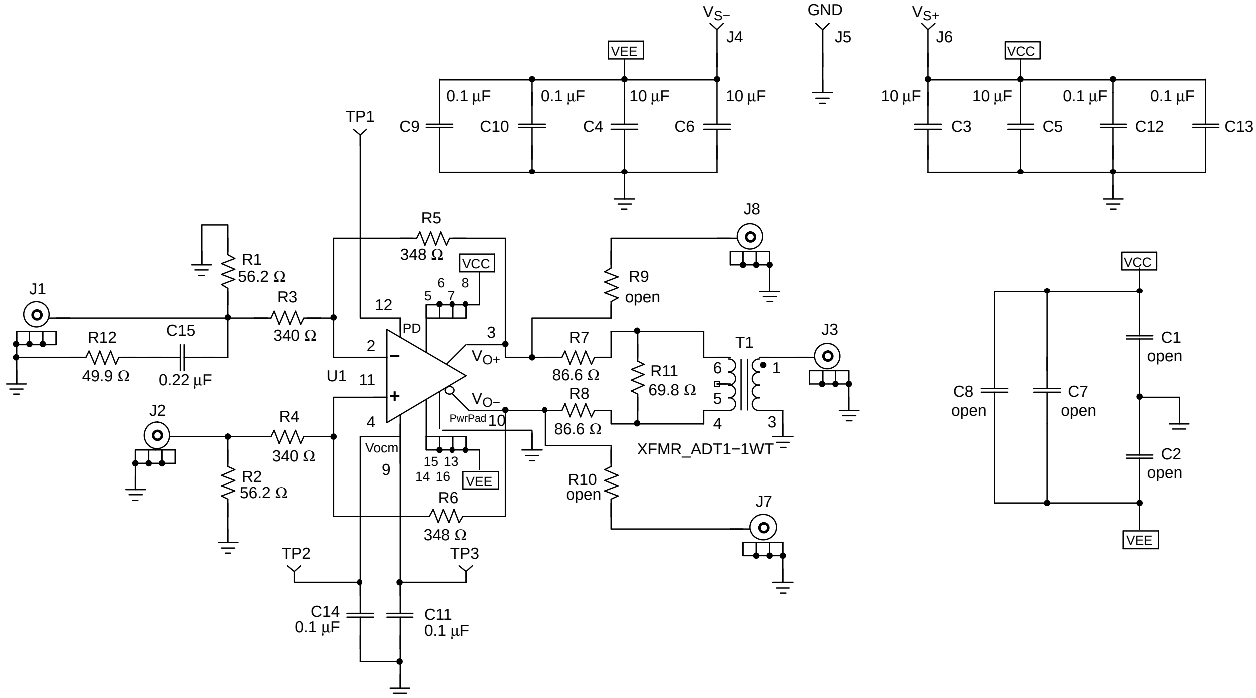


Figure 88. THS4513 EVAL1 EVM Schematic

Figure 89.

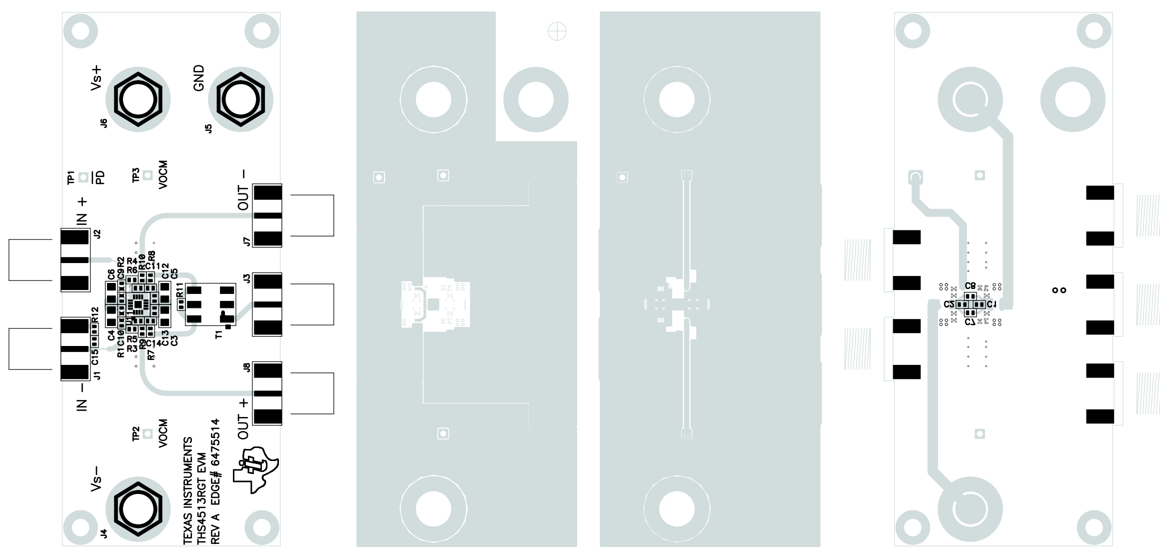


Figure 90. THS4513 EVAL1 EVM Layer 1 through 4

Table 4. THS4513 EVAL1 EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER
1	CAP, 10.0 µF, Ceramic, X5R, 6.3V	0805	C3, C4, C5, C6	4	(AVX) 08056D106KAT2A
2	CAP, 0.1 µF, Ceramic, X5R, 10V	0402	C9, C10, C11, C12, C13, C14	6	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 µF, Ceramic, X5R, 6.3V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8	4	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
7	Resistor, 56.2 Ω, 1/16W, 1%	0402	R1,R2	2	(KOA) RK73H1ETTP56R2F
8	Resistor, 69.8 Ω, 1/16W, 1%	0402	R11	1	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 340 Ω, 1/16W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP3400F
11	Resistor, 348 Ω, 1/16W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
13	Jack, banana receptance, 0.25" diameter hole		J4, J5, J6	3	(HH SMITH) 101
14	OPEN		J1, J7, J8	3	
15	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
16	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
17	IC, THS4513		U1	1	(TI) THS4513RGT
18	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
19	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
20	Printed circuit board			1	(TI) EDGE# 6475514

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THS4513RGTR	ACTIVE	QFN	RGT	16	3000	TBD	Call TI	Call TI
THS4513RGTT	ACTIVE	QFN	RGT	16	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

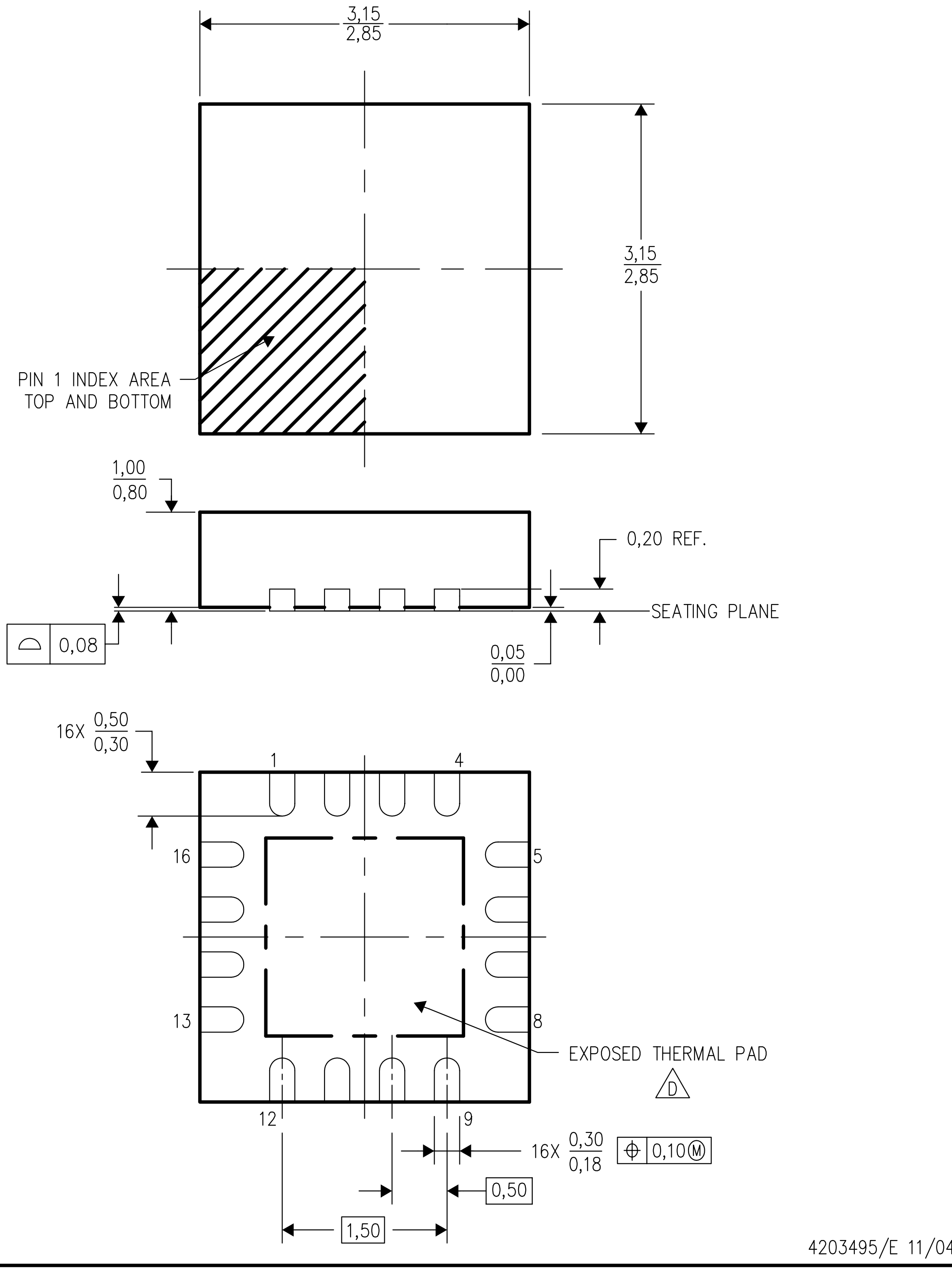
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



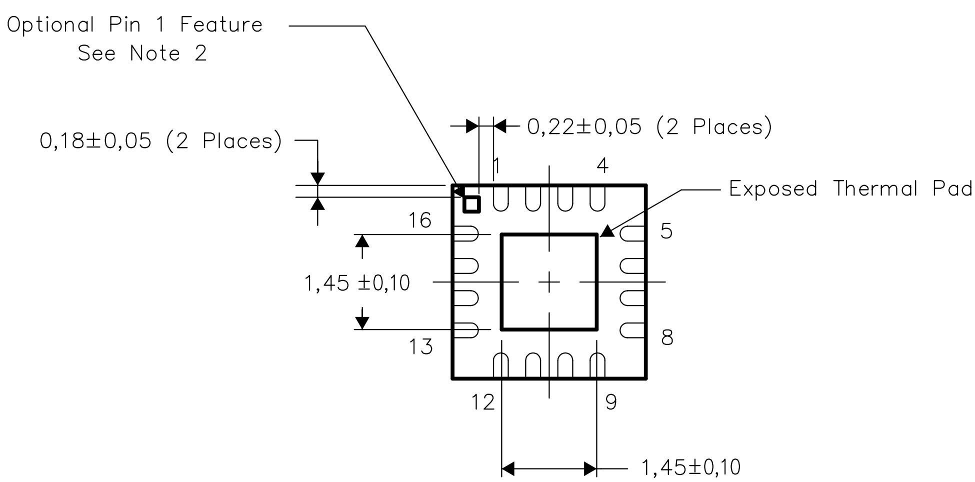
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

NOTES:
1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THS4513RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4513RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

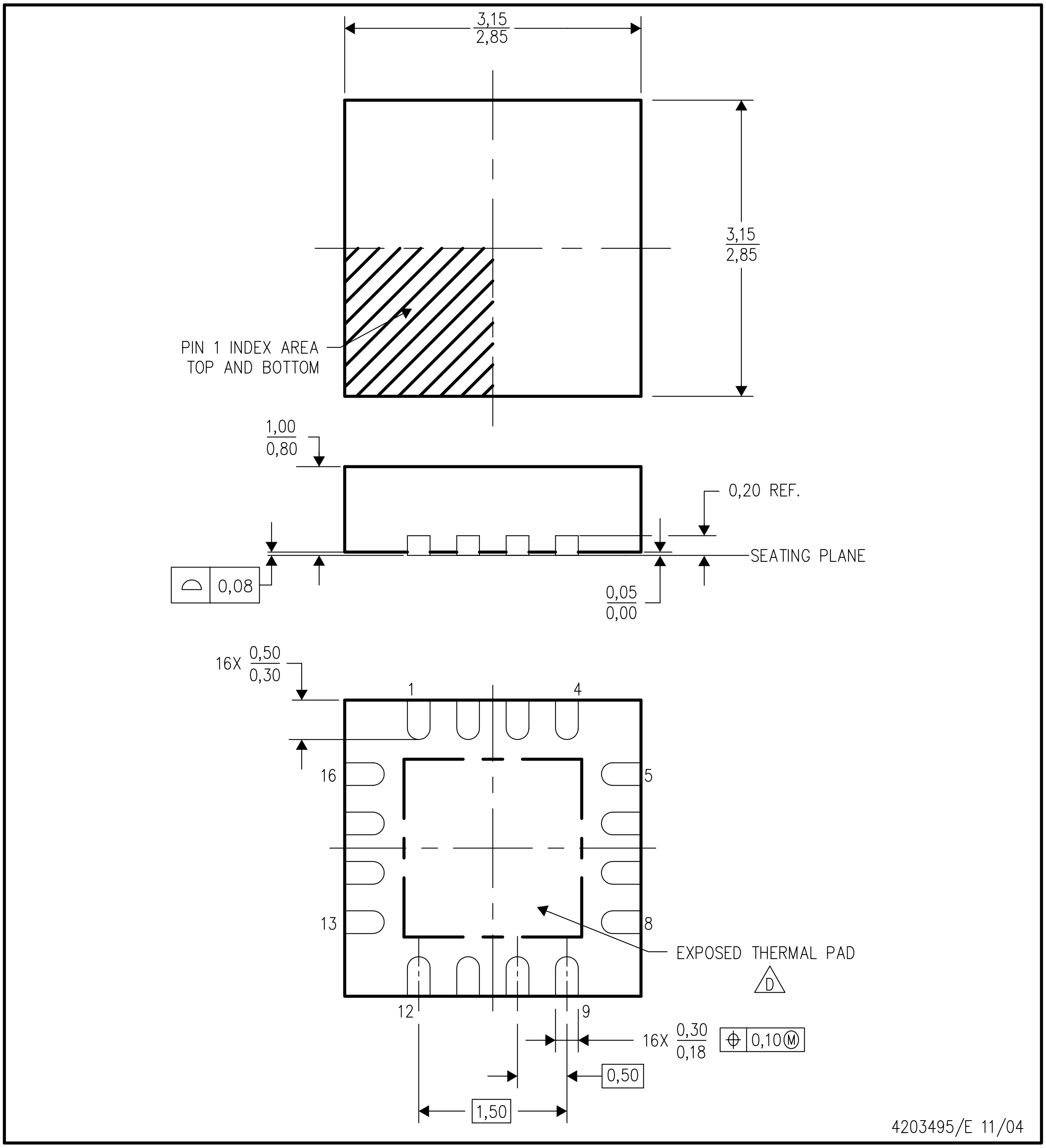
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265