

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 2.8 ns at 1.8 V
- Low Power Consumption, 20  $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

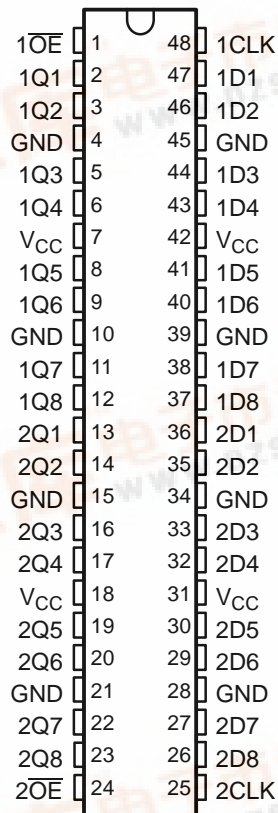
This 16-bit edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

DGG OR DGV PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AUCH16374DGGR	AUCH16374
	TVSOP – DGV	Tape and reel	SN74AUCH16374DGVVR	MJ374
	VFBGA – GQL	Tape and reel	SN74AUCH16374GQLR	MJ374

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

# SN74AUCH16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES404D—JULY 2002—REVISED MAY 2005

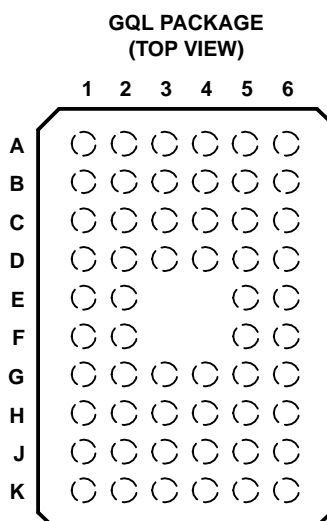


### DESCRIPTION/ORDERING INFORMATION(CONTINUED)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



### TERMINAL ASSIGNMENTS<sup>(1)</sup>

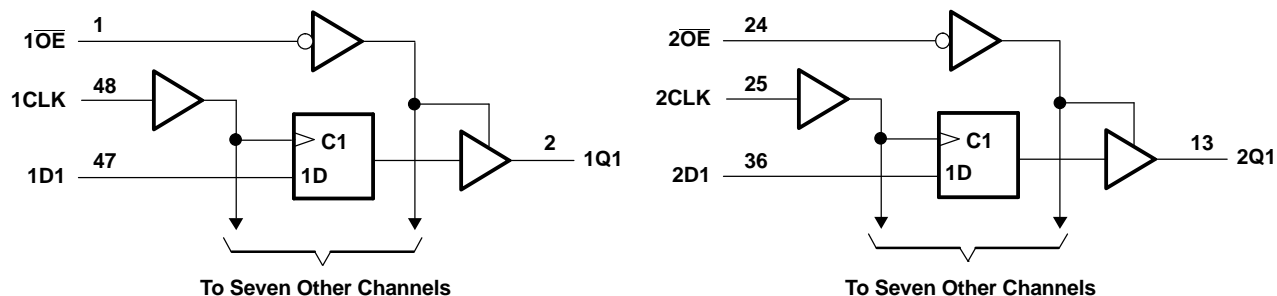
	1	2	3	4	5	6
<b>A</b>	$\overline{1OE}$	NC	NC	NC	NC	1CLK
<b>B</b>	1Q2	1Q1	GND	GND	1D1	1D2
<b>C</b>	1Q4	1Q3	$V_{CC}$	$V_{CC}$	1D3	1D4
<b>D</b>	1Q6	1Q5	GND	GND	1D5	1D6
<b>E</b>	1Q8	1Q7			1D7	1D8
<b>F</b>	2Q1	2Q2			2D2	2D1
<b>G</b>	2Q3	2Q4	GND	GND	2D4	2D3
<b>H</b>	2Q5	2Q6	$V_{CC}$	$V_{CC}$	2D6	2D5
<b>J</b>	2Q7	2Q8	GND	GND	2D8	2D7
<b>K</b>	$\overline{2OE}$	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

### FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG and DGV packages.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	3.6	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	3.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	3.6	V
$V_O$	Output voltage range <sup>(2)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		–50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50 mA
$I_O$	Continuous output current			±20 mA
Continuous current through each $V_{CC}$ or GND				±100 mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DGG package		70
		DGV package		58
		GQL package		42
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74AUCH16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES404D—JULY 2002—REVISED MAY 2005



### Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0.8	2.7	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>		V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V	0		V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.35 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
V <sub>I</sub>	Input voltage		0	3.6	V
V <sub>O</sub>	Output voltage	Active state	0	V <sub>CC</sub>	V
		3-state	0	3.6	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 0.8 V	−0.7		mA
		V <sub>CC</sub> = 1.1 V	−3		
		V <sub>CC</sub> = 1.4 V	−5		
		V <sub>CC</sub> = 1.65 V	−8		
		V <sub>CC</sub> = 2.3 V	−9		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V	0.7		mA
		V <sub>CC</sub> = 1.1 V	3		
		V <sub>CC</sub> = 1.4 V	5		
		V <sub>CC</sub> = 1.65 V	8		
		V <sub>CC</sub> = 2.3 V	9		
Δt/Δv	Input transition rise or fall rate			20	ns/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = –100 µA	0.8 V to 2.7 V	V <sub>CC</sub> – 0.1			V
		I <sub>OH</sub> = –0.7 mA	0.8 V	0.55			
		I <sub>OH</sub> = –3 mA	1.1 V	0.8			
		I <sub>OH</sub> = –5 mA	1.4 V	1			
		I <sub>OH</sub> = –8 mA	1.65 V	1.2			
		I <sub>OH</sub> = –9 mA	2.3 V	1.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	0.8 V to 2.7 V	0.2			V
		I <sub>OL</sub> = 0.7 mA	0.8 V	0.25			
		I <sub>OL</sub> = 3 mA	1.1 V	0.3			
		I <sub>OL</sub> = 5 mA	1.4 V	0.4			
		I <sub>OL</sub> = 8 mA	1.65 V	0.45			
		I <sub>OL</sub> = 9 mA	2.3 V	0.6			
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V			±5	µA
I <sub>BHL</sub> <sup>(2)</sup>		V <sub>I</sub> = 0.35 V	1.1 V	10			µA
		V <sub>I</sub> = 0.47 V	1.4 V	15			
		V <sub>I</sub> = 0.57 V	1.65 V	20			
		V <sub>I</sub> = 0.7 V	2.3 V	40			
I <sub>BHH</sub> <sup>(3)</sup>		V <sub>I</sub> = 0.8 V	1.1 V	–5			µA
		V <sub>I</sub> = 0.9 V	1.4 V	–15			
		V <sub>I</sub> = 1.07 V	1.65 V	–20			
		V <sub>I</sub> = 1.7 V	2.3 V	–40			
I <sub>BHLO</sub> <sup>(4)</sup>		V <sub>I</sub> = 0 to V <sub>CC</sub>	1.3 V	75			µA
			1.6 V	125			
			1.95 V	175			
			2.7 V	275			
I <sub>BHHO</sub> <sup>(5)</sup>		V <sub>I</sub> = 0 to V <sub>CC</sub>	1.3 V	–75			µA
			1.6 V	–125			
			1.95 V	–175			
			2.7 V	–275			
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 2.7 V	0			±10	µA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	2.7 V			±10	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V			20	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V	3			pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V	5			pF

(1) All typical values are at T<sub>A</sub> = 25°C.

(2) The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

(3) The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

(4) An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

(5) An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

# SN74AUCH16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES404D—JULY 2002—REVISED MAY 2005



### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	85	250		250		250		250		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	5.9	1.9		1.9		1.9		1.9		ns
t <sub>su</sub>	Setup time, data before CLK↑	1.4	1.2		0.7		0.6		0.6		ns
t <sub>h</sub>	Hold time, data after CLK↑	0.1	0.4		0.4		0.4		0.4		ns

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			85	250		250		250			250		MHz
t <sub>pd</sub>	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t <sub>en</sub>	$\overline{OE}$	Q	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t <sub>dis</sub>	$\overline{OE}$	Q	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.5	2.2	ns

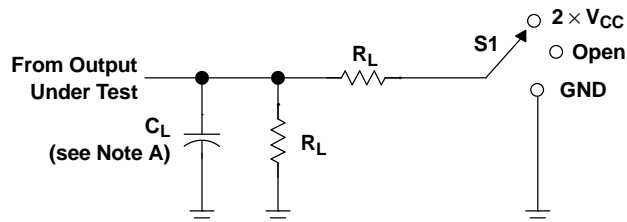
### Operating Characteristics<sup>(1)</sup>

T<sub>A</sub> = 25°C

PARAMETER			TEST CON- DITIONS	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C <sub>pd</sub> <sup>(2)</sup> (each output)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f <sub>data</sub> = 5 MHz, 1 f <sub>clk</sub> = 10 MHz, 1 f <sub>out</sub> = 5 MHz, $\overline{OE}$ = GND, C <sub>L</sub> = 0 pF	24	24	24.1	26.2	31.2	pF
C <sub>pd</sub> (Z)	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 f <sub>data</sub> = 5 MHz, 1 f <sub>clk</sub> = 10 MHz, f <sub>out</sub> = not switching, $\overline{OE}$ = V <sub>CC</sub> , C <sub>L</sub> = 0 pF	7.5	7.5	8	9.4	13.2	pF
C <sub>pd</sub> <sup>(3)</sup> (each clock)	Power dissipation capacitance	Outputs disabled, clock only switching	1 f <sub>data</sub> = 0 MHz, 1 f <sub>clk</sub> = 10 MHz, f <sub>out</sub> = not switching, $\overline{OE}$ = V <sub>CC</sub> , C <sub>L</sub> = 0 pF	13.8	13.8	14	14.7	17.5	pF

- (1) Total device C<sub>pd</sub> for multiple (n) outputs switching and (y) clocks inputs switching = {n \* C<sub>pd</sub> (each output)} + {y \* C<sub>pd</sub> (each clock)}.
- (2) C<sub>pd</sub> (each output) is the C<sub>pd</sub> for each data bit (input and output circuitry) as it operates at 5 MHz (Note: the clock is operating at 10 MHz in this test, but its I<sub>CC</sub> component has been subtracted out).
- (3) C<sub>pd</sub> (each clock) is the C<sub>pd</sub> for the clock circuitry only as it operates at 10 MHz.

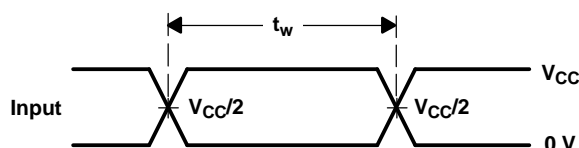
## PARAMETER MEASUREMENT INFORMATION



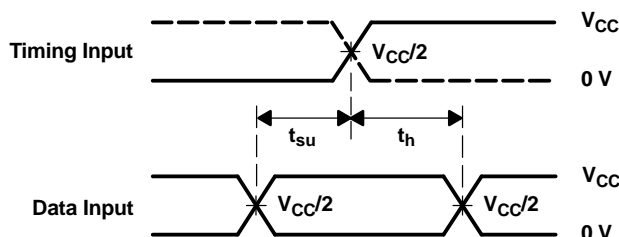
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

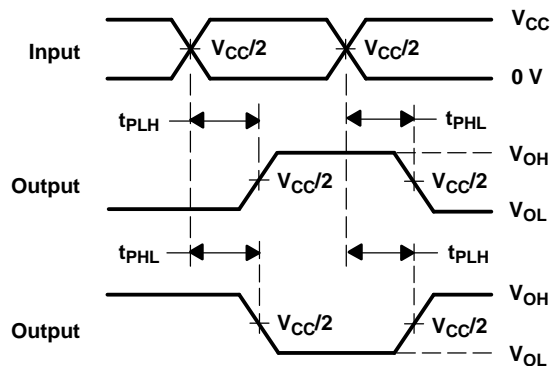
$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



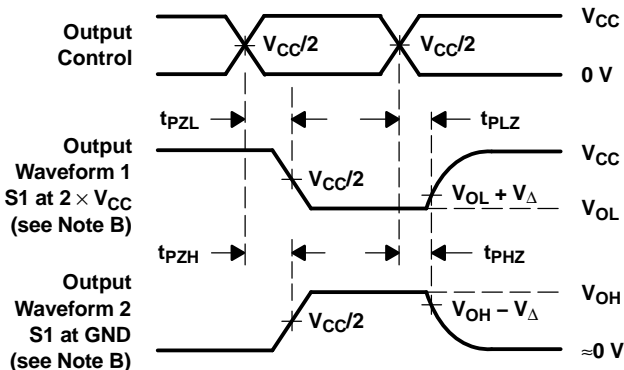
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AUCH16374DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AUCH16374DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUCH16374DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUCH16374DGV	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUCH16374GQLR	ACTIVE	BGA MI CROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74AUCH16374ZQLR	ACTIVE	BGA MI CROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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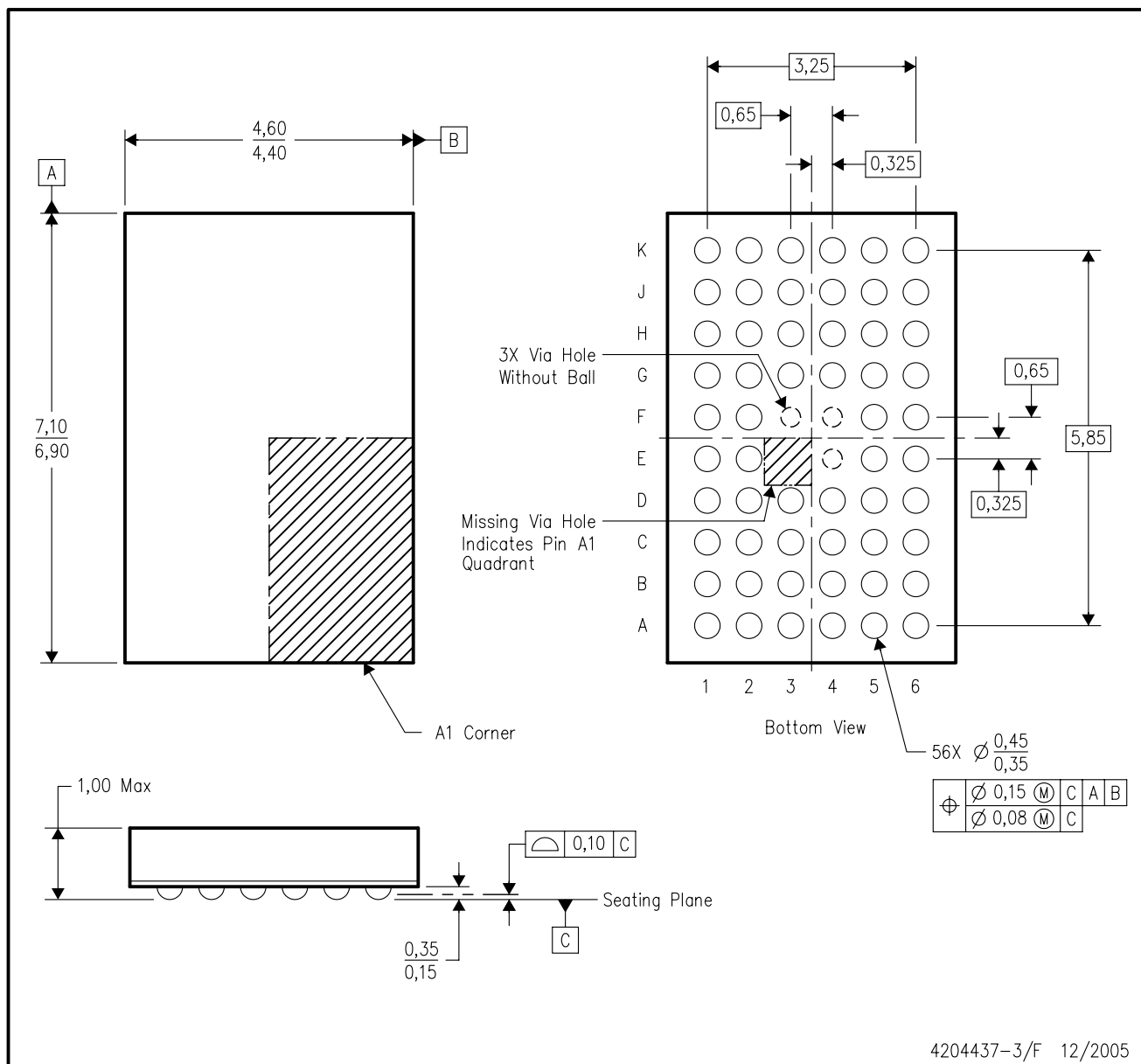
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



# MECHANICAL DATA

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-225 variation BA.
  - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

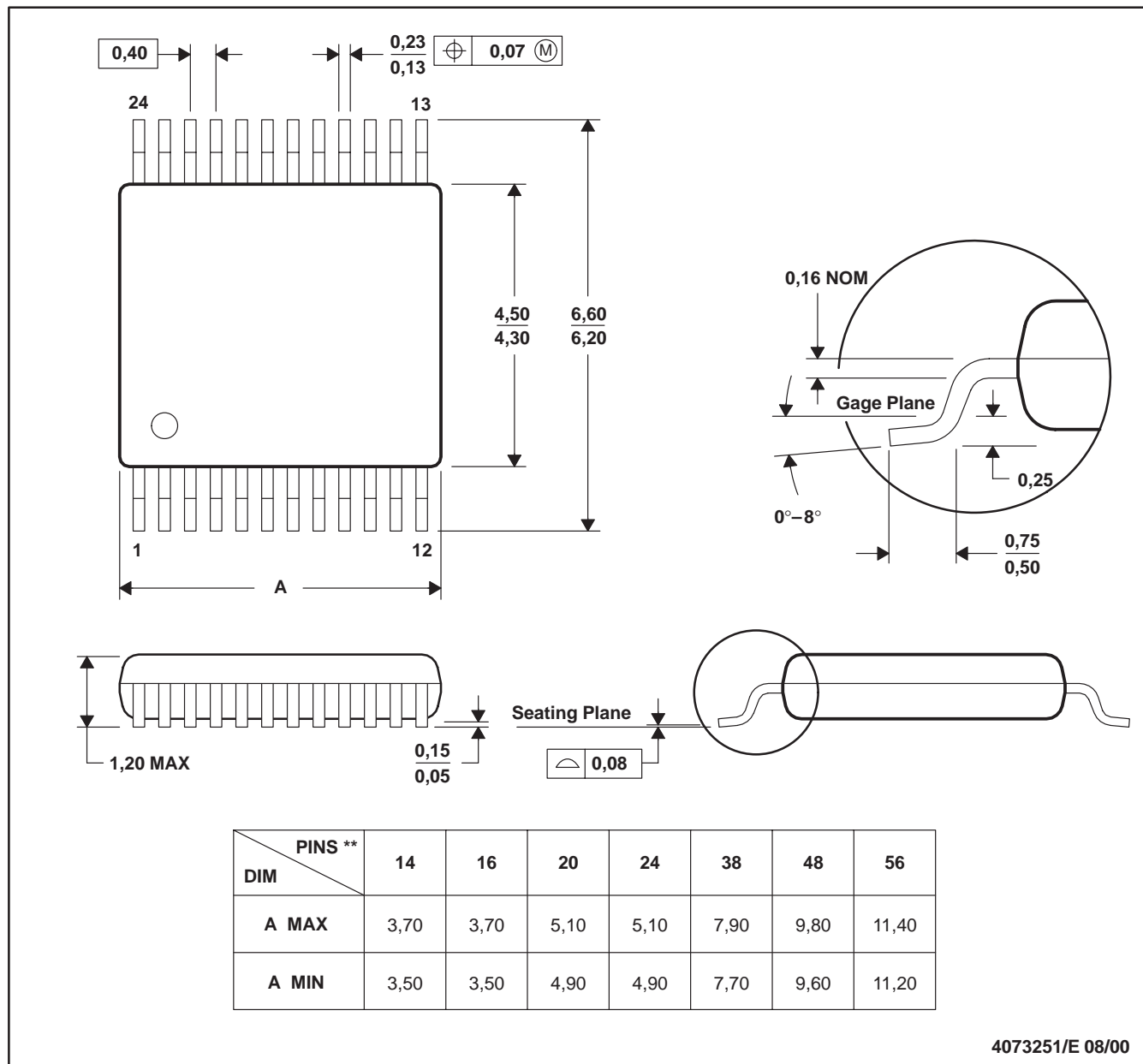
# MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

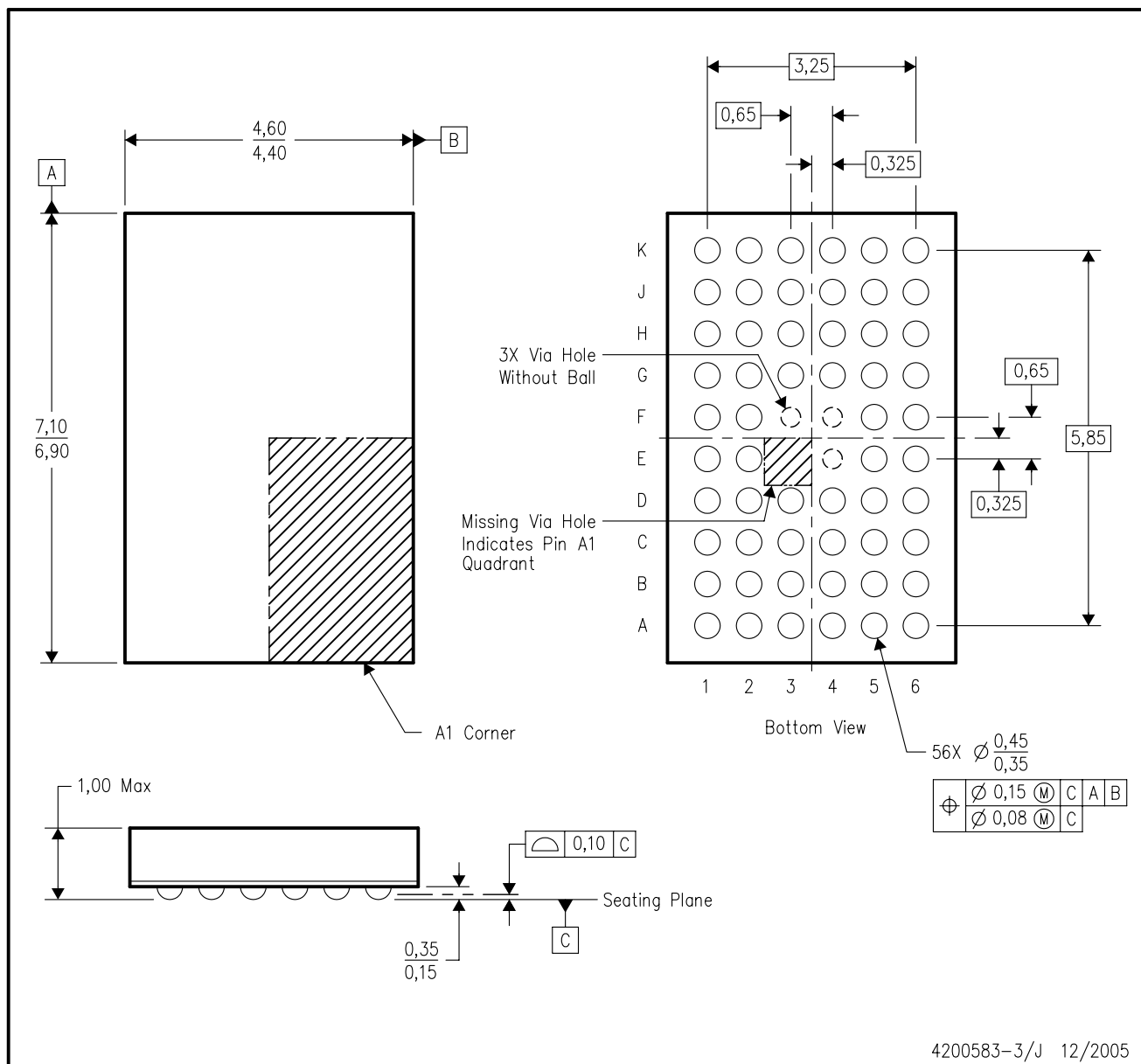


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/J 12/2005

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-225 variation BA.
  - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

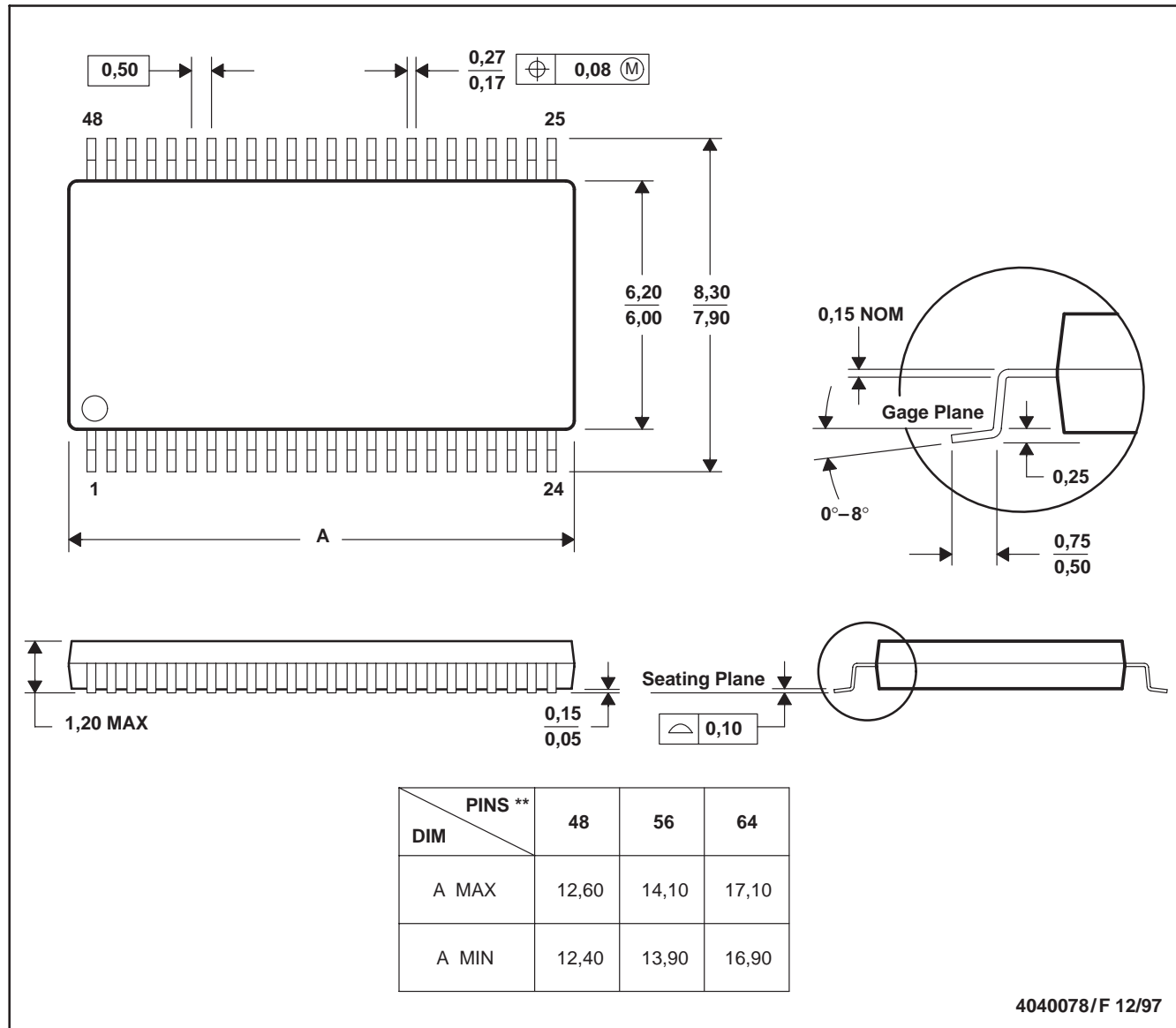
# MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153

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