8-A, 12-V INPUT NONISOLATED WIDE-OUTPUT ADJUST SIP MODULE

FEATURES

- **8 A Output Current**
- **12-V Input Voltage**
- **Wide-Output Voltage Adjust (1.2 V to 5.5 V)/(0.8 V to 1.8 V)**
- **Efficiencies up to 93%**
- **On/Off Inhibit**
- **Prebias Start Up**
- **Undervoltage Lockout**
- **Auto-Track™ Sequencing**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Operating Temperature: –40°C to 85°C**
- **Safety Agency Approvals: UL/cUL 60950, EN60950 VDE (Pending)**
- **POLA™ Alliance Compatible**

APPLICATIONS

- **Multivoltage Digital Systems**
- **High-End Computing**
- **Networking**
- **12-V Intermediate Bus Architectures**

DESCRIPTION

The PTV12010 series of non-isolated power modules are part of a new class of complete dc/dc switching regulator modules from Texas Instruments. These modules combine high performance with double-sided, surface mount construction to give designers the flexibility to power the most complex multiprocessor digital systems using off-the-shelf catalog parts.

The PTV12010 series is produced in an 8-pin, single in-line pin (SIP) package. The SIP footprint minimizes board space, and offers an alternate package option for space conscious applications. Operating from a 12-V input bus, the series provides step-down conversion to a wide range of output voltages, at up to 8 A of output current. The output voltage of the W-suffix parts can be set to any value over the range of 1.2 V to 5.5 V. The L-suffix parts have an adjustment range of 0.8 V to 1.8 V. The output voltage is set using a single external resistor.

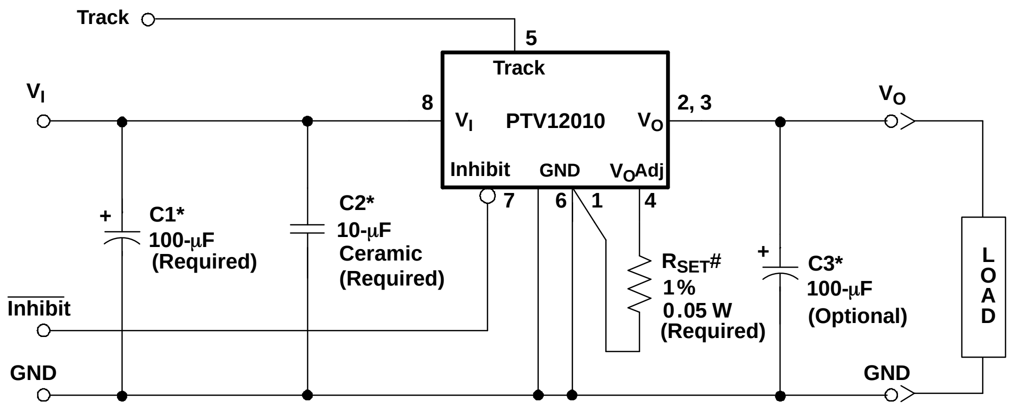
This series includes Auto-Track™. Auto-Track™ simplifies the task of supply-voltage sequencing in a power system by enabling the output voltage of multiple modules to accurately track each other, or any external voltage, during power up and power down.

Other operating features include an on/off inhibit, and the ability to start up into an existing output voltage or prebias. A nonlatching overcurrent trip and overtemperature shutdown provide protection against load faults.

Target applications include complex multivoltage, multiprocessor systems that incorporate the industry's high-speed DSPs, microprocessors, and bus drivers.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

STANDARD APPLICATION



*See the application information for capacitor recommendation.
#R_{SET} is Required to adjust the output voltage higher than its lowest value. See the application information for values.

ORDERING INFORMATION

PTV12010 (Basic Model)			
Output Voltage	**Part Number**	**DESCRIPTION**	**Package**(1)
1.2 V – 5.5 V (Adjustable)	PTV12010WAH	Horizontal T/H	EVA
0.8 V – 1.8 V (Adjustable)	PTV12010LAH	Horizontal T/H	EVA

(1) See the applicable package drawing for dimensions and PC board layout.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
$V_{(Track)}$	Track input		–0.3 V to V_I +0.3 V
T_A	Operating temperature range	Over V_I range	–40°C to 85°C
	Lead temperature	5 seconds	260°C (2)
T_{stg}	Storage temperature		–40°C to 125°C
$V_{(Inhabit)}$	Inhibit (pin 12) input voltage		–0.3 V to 7 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This product is not compatible with surface-mount reflow solder processes.

PACKAGE SPECIFICATIONS

PTV12010x (Suffix AH)			
Weight			2.6 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		500 Gs (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 Hz - 2000 Hz		15 Gs (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 12 V, V_O = 3.3 V, C1 = 100 µF, C2 = 10 µF, C3 = 0 µF, and I_O = I_O max (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		PTV12010W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Natural convection airflow		0		8 (1)	A
V_I	Input voltage range	Over I_O load range		10.8		13.2	V
V_O	Set-point voltage tolerance					±2% (2)	
	Temperature variation	–40°C < T_A < 85°C			±0.5%		
	Line regulation	Over V_I range			±10		mV
	Load regulation	Over I_O range			±12		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3 (2)	$\%V_o$
	Adjust range	Over V_I range		1.2		5.5	V
η	Efficiency	I_O = I_O max	R_{SET} = 280 Ω, V_O = 5 V		92%		
			R_{SET} = 2.0 kΩ, V_O = 3.3 V		90%		
			R_{SET} = 4.32 kΩ, V_O = 2.5 V		88%		
			R_{SET} = 11.5 kΩ, V_O = 1.8 V		85%		
			R_{SET} = 24.3 kΩ, V_O = 1.5 V		83%		
			R_{SET} = open cct., V_O = 1.2 V		80%		
	Output voltage ripple (peak-to-peak)	20-MHz bandwidth			20		mV_{PP}
I_O (trip)	Overcurrent threshold	Reset, followed by auto-recovery			16		A
	Transient response	1-A/µs load step, 50 to 100% I_O max, C3 = 100 µF					
			Recovery time		70		µs
			V_o over/undershoot		100		mV
	Track control (pin 5)	I_{IL} Input low current	Pin to GND			–0.13	mA
		Control slew-rate limit	C3 ≤ C3 (max)			1	V/ms
UVLO	Undervoltage lockout	V_I increasing			9.5	10.4	V
		V_I decreasing		8.8	9		
	Inhibit control (pin 7)	V_{IH} Input high voltage	Referenced to GND	2		Open (3)	V
		V_{IL} Input low voltage		–0.2		0.6	
		I_{IL} Input low current	Pin to GND		–0.24		mA
I_I (stby)	Input standby current	Inhibit (pin 7) to GND, Track (pin 5) open			10		mA
f_S	Switching frequency	Over V_I and I_O ranges		250	325	400	kHz
	External input capacitance		Nonceramic (C1)	100 (4)			µF
			Ceramic (C2)	10 (4)			
	External output capacitance (C3)	Capacitance value	Nonceramic	0	100 (5)	3,300 (6)	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4 (7)			mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		5			10^6 Hrs

(1) See thermal derating curves for safe operating area (SOA), or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C or better temperature stability.
(3) This control pin is pulled up to an internal supply voltage. To avoid risk of damage to the module, *do not* apply an external voltage greater than 7 V. If this input is left open-circuit, the module operates when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.
(4) A 10-µF high-frequency ceramic capacitor and 100-µF electrolytic input capacitor are required for proper operation. The electrolytic capacitor must be rated for the minimum ripple current rating. See the application information for further guidance on input capacitor selection.
(5) An external output capacitor is not required for basic operation. Adding 100 µF of distributed capacitance at the load improves the transient response.
(6) This is the calculated maximum. The minimum ESR limitation often results in a lower value. See the application information for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 12 V, V_O = 1.8 V, C1 = 100 µF, C2 = 10 µF, C3 = 0 µF, and I_O = I_O max (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PTV12010L MIN	TYP	MAX	UNIT
I_O	Output current	Natural convection airflow		0		8 [1]	A
V_I	Input voltage range	Over I_O load range		10.8		13.2	V
V_O	Set-point voltage tolerance					±2% [2]	
	Temperature variation	–40°C < T_A < 85°C			±0.5%		
	Line regulation	Over V_I range			±10		mV
	Load regulation	Over I_O range			±12		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3 [2]	$\%V_o$
	Adjust range	Over V_I range		0.8		1.8	V
η	Efficiency	I_O = I_O max	R_{SET} = 130 Ω, V_O = 1.8 V		87%		
			R_{SET} = 3.57 kΩ, V_O = 1.5 V		86%		
			R_{SET} = 12.1 kΩ, V_O = 1.2 V		84%		
			R_{SET} = 32.4 kΩ, V_O = 1 V		81%		
			R_{SET} = open cct., V_O = 0.8 V		78%		
	Output voltage ripple (pk-pk)	20-MHz bandwidth			15		mV_{PP}
I_O (trip)	Overcurrent threshold	Reset, followed by auto-recovery			16		A
	Transient response	1-A/µs load step, 50 to 100% I_O max, C3 = 100 µF					
		Recovery time			70		µs
		V_o over/undershoot			100		mV
	Track control (pin 5)	I_{IL} Input low current	Pin to GND			–0.13	mA
		Control slew-rate limit	C3 ≤ C3 (max)			1	V/ms
	Inhibit control (pin 7)	V_{IH} Input high voltage	Referenced to GND	2		Open [3]	V
		V_{IL} Input low voltage		–0.2		0.6	
		I_{IL} Input low current	Pin to GND		–0.24		mA
I_I (stby)	Input standby current	Inhibit (pin 7) to GND, Track (pin 5) open			10		mA
UVLO	Undervoltage lockout	V_I increasing			9.5	10.4	V
		V_I decreasing		8.8	9		
f_S	Switching frequency	Over V_I and I_O ranges		200	250	300	kHz
	External input capacitance	Nonceramic (C1)		100 [4]			µF
		Ceramic (C2)		10 [4]			
	External output capacitance (C3)	Capacitance value	Nonceramic	0	100 [5]	3,300 [6]	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4 [7]			mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		5			10^6 Hrs

(1) See thermal derating curves for safe operating area (SOA), or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C or better temperature stability.
(3) This control pin is pulled up to an internal supply voltage. To avoid risk of damage to the module, *do not* apply an external voltage greater than 7 V. If this input is left open-circuit, the module operates when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.
(4) A 10-µF high-frequency ceramic capacitor and 100-µF electrolytic input capacitor are required for proper operation. The electrolytic capacitor must be rated for the minimum ripple current rating. Consult the Application Information for guidance on input capacitor selection.
(5) An external output capacitor is not required for basic operation. Adding 100 µF of distributed capacitance at the load improves the transient response.
(6) This is the calculated maximum. The minimum ESR limitation often results in a lower value. Consult the Application Informaiton for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

PTV12010W Characteristic Data; 1.2 V to 5.5 V(8)(9)

EFFICIENCY vs OUTPUT CURRENT

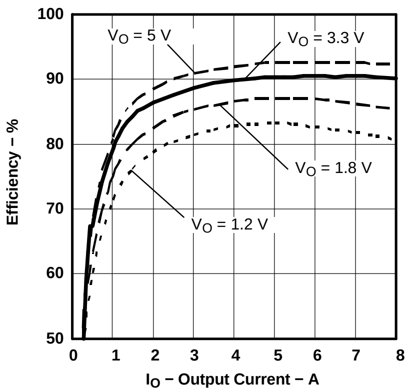


Figure 1.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

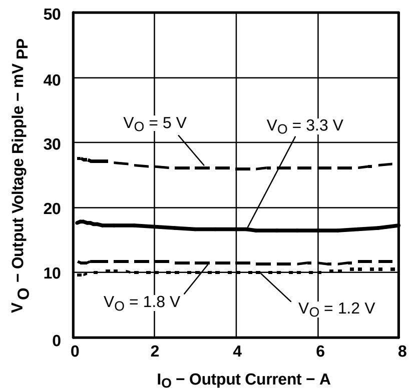


Figure 2.

POWER DISSIPATION vs OUTPUT CURRENT

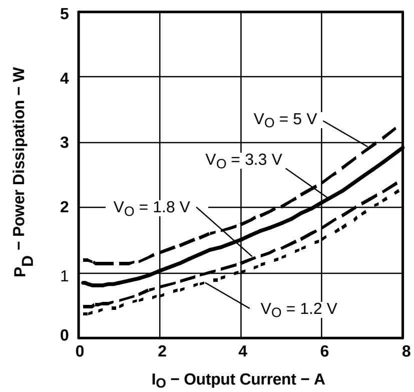


Figure 3.

TEMPERATURE DERATING vs OUTPUT CURRENT & AIRFLOW

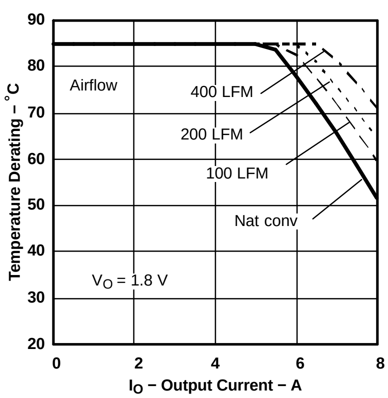


Figure 4.

TEMPERATURE DERATING vs OUTPUT CURRENT & AIRFLOW

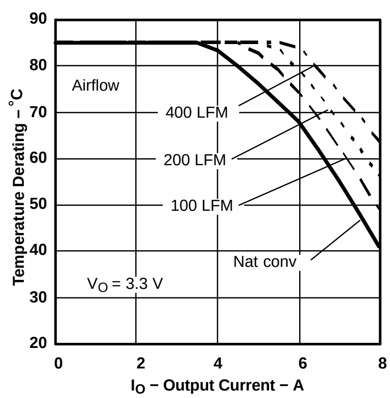


Figure 5.

TEMPERATURE DERATING vs OUTPUT CURRENT & AIRFLOW

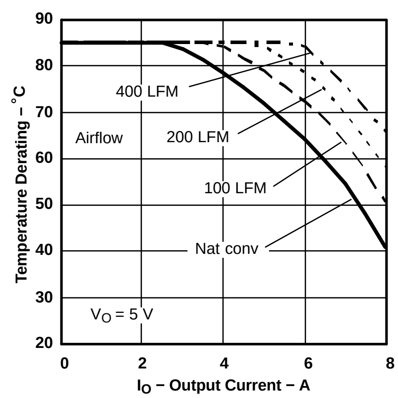


Figure 6.

(8) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(9) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 4, Figure 5, and Figure 6.

PTV12010L Characteristic Data; 0.8 V to 1.8 V (10) (11)

EFFICIENCY vs OUTPUT CURRENT

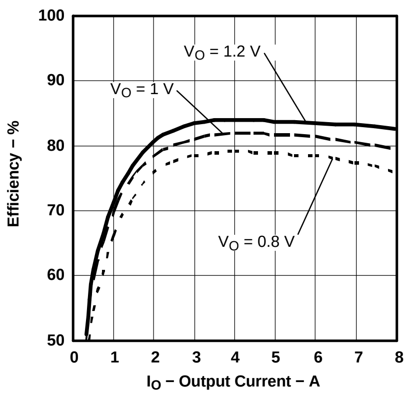


Figure 7.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

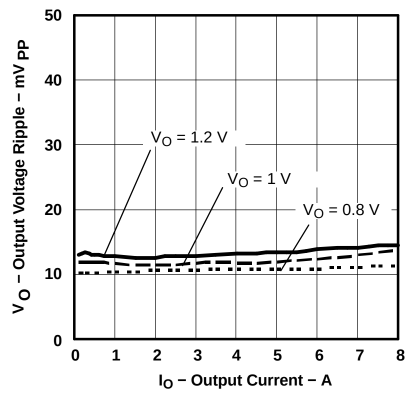


Figure 8.

POWER DISSIPATION vs OUTPUT CURRENT

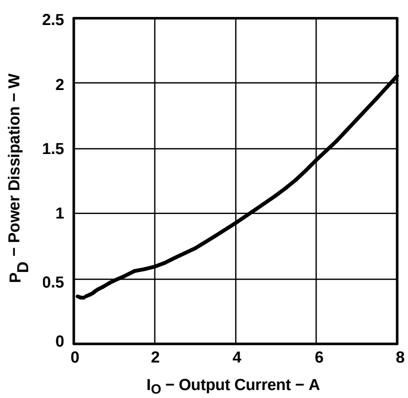


Figure 9.

TEMPERATURE DERATING vs OUTPUT CURRENT & AIRFLOW

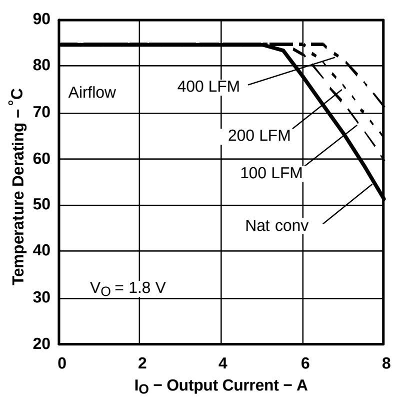


Figure 10.

(10) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 7, Figure 8, and Figure 9.
(11) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 10.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	8	The positive input voltage power node to the module, which is referenced to common GND.
V_O	2, 3	The regulated positive power output with respect to the GND node.
GND	1, 6	This is the common ground connection for the V_I and V_O power connections. It is also the 0 VDC reference for the control inputs.
Inhibit	7	The Inhibit pin is an open-collector/drain, active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the inhibit feature is not used, the control pin should be left open-circuit. The module then produces an output voltage whenever a valid input source is applied.
V_o Adjust	4	A 1% resistor must be connected directly between this pin and GND (pin 1) to set the output voltage of the module higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 1.2 V to 5.5 V for W-suffix devices and 0.8 V to 1.8 V for L-suffix devices. The resistor value required for a given output voltage may be calculated using a formula. If left open-circuit, the module output voltage defaults to its lowest value. For further information on output voltage adjustment, consult the related application note. The specification table gives the standard resistor values for a number of common output voltages.
Track	5	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range, the output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. *NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. Consult the related Application Information for further guidance.*

APPLICATION INFORMATION

Capacitor Recommendations for the PTV12010 Series of Power Modules

Input Capacitors

The required input capacitors are a combination of a 10-µF X5R/X7R ceramic, and a 100-µF electrolytic type. When V_O > 3 V the 100-µF electrolyitc capacitance must be rated for 700 mArms ripple current capability. For $V_O \leq$ 3 V, the ripple current rating must be at least 450 mArms. Where applicable, Table 1 gives the maximum output voltage and current limits for a capacitor's rms ripple current rating. The ripple current requirements for the electrolytic capacitance are *conditional* that the 10-µF ceramic capacitor is present.

The 10-µF ceramic capacitor is necessary to reduce both the magnitude of ripple current through the electroytic capacitor and the amount of ripple current reflected back to the input source. Ceramic capacitors should be located within 0.5 in. (1,3 cm) of the module input pins. Additional ceramic capacitors can be added to reduce the RMS ripple current requirement for the electrolytic capacitor.

Ripple current (Arms) rating, less than 100 mΩ of equivalent series resistance (ESR), and temperature are the major considerations when selecting input capacitors. Regular tantalum capacitors have a recommended minimum voltage rating of 2 × (max. dc voltage + ac ripple). This is standard practice to ensure reliability. Only a few tantalum capacitors were found to have sufficient voltage rating to meet this requirement. At temperatures below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

Output Capacitor (Optional)

For applications with load transients (sudden changes in load current), regulator response benefits from external output capacitance. The optional value defined is only required to meet the transient response specification. For most applications, a high-quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C. For operation below 0°C, tantalum, ceramic, or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 1.

In addition to electrolytic capacitance, adding a 10–µF ceramic capacitor across the output will further reduce the output ripple voltage and improve the regulator's transient response. The measurement of both the output ripple and transient response is also best achieved across a 10–µF ceramic capacitor.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have low ESR and a resonant frequency higher than the bandwidth of the regulator. They are recommended to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed approximately 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum-type capacitors can only be used on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable as they have reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered before the maximum capacitance value is reached.

APPLICATION INFORMATION (continued)

Capacitor Table

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

Note: This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

Table 1. Input/Output Capacitors

Capacitor Vendor, Type/Series (Style)	Capacitor Characteristics					Quantity		Vendor Part Number
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (Ω)	Max. Irms Ripple Current at 85°C (mA)	Physical Size (mm)	Input Bus	Optional Output Bus	
Panasonic, Aluminum	25	330	0.090	755	10 × 12.5	1	1	EEUFC1E331
FC (Radial)	35	180	0.090	755	10 × 12.5	1	1	EEUFC1V181
FK (SMD)	25	470	0.080	850	10 × 10.2	1	1	EEVFK1E471P
United Chemi-Con								
PXA, Poly-Aluminum (SMD)	16	150	0.026	3430	10 × 7.7	1	≤4	PXA16VC151MJ80TP
FP, Os-con (Radial)	20	120	0.024	3100	8 × 10.5	1	≤4	20FP120MG
FS, OS-con (SMD)	20	100	0.030	2740	8 × 10.5	1	≤4	20FS100M
LXZ, Aluminum (Radial)	35	220	0.090	760	10 × 12.5	1	1	LXZ35VB221M10X12LL
Nichicon, Aluminum								
HD (Radial)	25	220	0.072	760	8 × 11.5	1	1	UHD1E221MPR
PM (Radial)	35	220	0.090	770	10 × 15	1	1	UPM1V221MHH6
Panasonic, Poly-Aluminum								
WA (SMD)	16	100	0.039	2500	8 × 6.9	1	≤5	EEFWA1C101P
S/SE (SMD)	6.3 (1)	180	0.005	4000	7.3 × 4.3 × 4.2	N/R (2)	≤1	EEFSE0J181R (V_O ≤ 5.1 V)
Sanyo								
SVP, Os-Con (SMD)	20	100	0.024	>3300	8 × 12	1	≤4	20SVP100M
SP, Os-Con	20	120	0.024	>3100	8 × 10.5	1	≤4	20SP120M
TPE, Pos-cap (SMD)	10	220	0.025	>2400	7.3 × 5.7	1	≤4	10TPE220ML
AVX, Tantalum, TPS (SMD)	10	100	0.100	>1090	7.3 L × 5.7 W × 4.1 H	N/R (2)	≤5	TPSD107M010R0100
	10	220	0.100	>1414		N/R (2)	≤5	TPSV227M010R0100
	25	68	0.095	>1451		2	≤5	TPSV686M025R0095
Kemet (SMD)								
T520, Poly-Tant (SMD)	10	100	0.080	1200	7.3L × 5.7W × 4H	N/R (2)	≤5	T520D107M010AS
T495, Tantalum (SMD)	10	100	0.100	>1100		N/R (2)	≤1	T495X107M010AS
Vishay-Sprague								

(1) The voltage rating of this capacitor only allows it to be used for output voltages that are equal to, or less than, 5.1 V.
(2) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.

APPLICATION INFORMATION (continued)

Table 1. Input/Output Capacitors (continued)

Capacitor Vendor, Type/Series (Style)	Capacitor Characteristics					Quantity		Vendor Part Number
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (Ω)	Max. Irms Ripple Current at 85°C (mA)	Physical Size (mm)	Input Bus	Optional Output Bus	
594D, Tantalum (SMD)	10	150	0.090	1100	7.3L × 6W × 4.1H	N/R (2)	≤5	594D157X0010C2T
	25	68	0.095	1600		2	≤5	594D686X0025R2T
94SP, Organic (Radial)	16	100	0.075	2890	10 × 10.5	1	≤2	94SP107X0016FBP
Kemet, Ceramic X5R (SMD)	16	10	0.002	—		≥1 (3)	≤5	C1210C106M4PAC
	6.3	47	0.002		3225 mm	N/R (2)	≤5	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3	100	0.002	—	3225 mm	N/R (2)	≤3	GRM32ER60J107M
	6.3	47				N/R (2)	≤5	GRM32ER60J476M
	16	22				≥1 (3)	≤5	GRM32ER61C226K
	16	10				≥1 (3)	≤5	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3	100	0.002	—	3225 mm	N/R (2)	≤3	C3225X5R0J107MT
	6.3	47				N/R (2)	≤5	C3225X5R0J476MT
	16	22				≥1 (3)	≤5	C3225X5R1C226MT
	16	10				≥1 (3)	≤5	C3225X5R1C106MT

(3) Ceramic capacitors are required to complement electrolytic types at the input and to reduce high-frequency ripple current.

Adjusting the Output Voltage of the PTV12010x Series

The V_O Adjust control (pin 8) sets the output voltage of the PTV12010 product. The adjustment range is from 1.2 V to 5.5 V for the W-suffix modules and 0.8 V to 1.8 V for L-suffix modules. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_O Adjust and GND (pin 1 or 2). Table 2 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. Figure 11 shows the placement of the required resistor.

Table 2. Standard Values of R_{SET} for Common Output Voltages

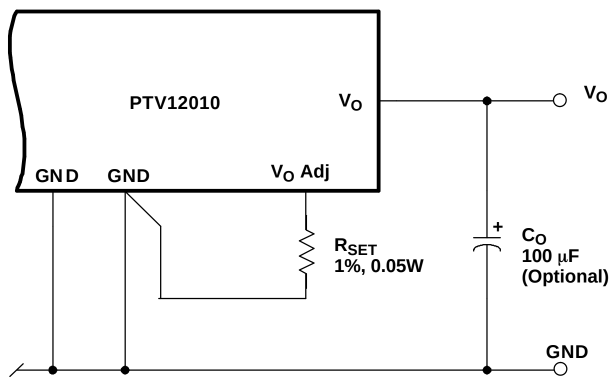
	PTV12010W		PTV12010L	
V_O (Required)	R_{SET} (Standard Value)	V_O (Actual)	R_{SET} (Standard Value)	V_O (Actual)
5 V	280 Ω	5.009 V	N/A	N/A
3.3 V	2.0 kΩ	3.294 V	N/A	N/A
2.5 V	4.32 kΩ	2.503 V	N/A	N/A
2 V	8.06 kΩ	2.010 V	N/A	N/A
1.8 V	11.5 kΩ	1.801 V	130 Ω	1.800 V
1.5 V	24.3 kΩ	1.506 V	3.57 kΩ	1.499 V
1.2 V	Open	1.200 V	12.1 kΩ	1.201 V
1.1 V	N/A	N/A	18.7 kΩ	1.101 V
1.0 V	N/A	N/A	32.4 kΩ	0.999 V
0.9 V	N/A	N/A	71.5 kΩ	0.901 V
0.8 V	N/A	N/A	Open	0.800 V

For other output voltages, the value of the required resistor can either be calculated or simply selected from the range of values given in Table 4. Equation 1 may be used for calculating the adjust resistor value. Select the appropriate value for the parameters, R_s and V_{min}, from Table 3.

$$R_{set} = 10\ k\Omega \times \frac{0.8\ V}{V_{out} - V_{min}} - R_S\ k\Omega \qquad (1)$$

Table 3. Adjust Formula Parameters

Pt. No.	PTV12010W	PTV12010L
V_{min}	1.2 V	0.8 V
V_{max}	5.5 V	1.8 V
R_s	1.82 kΩ	7.87 kΩ



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pin 8 and pins 1 or 2, using dedicated PCB traces.

(2) Never connect capacitors from V_oAdj to either GND or V_o. Any capacitance added to the V_oAdj pin affects the stability of the regulator.

Figure 11. V_O Adjust Resistor Placement

Table 4. Calculated Values of R_{SET} for Other Output Voltages

PTV12010W				PTV12010L	
V_{OUT}	R_{SET}	V_{OUT}	R_{SET}	V_{OUT}	R_{SET}
1.200	Open	2.70	3.51 kΩ	0.800	Open
1.250	158.0 kΩ	2.80	3.18 kΩ	0.825	312.0 kΩ
1.300	78.2 kΩ	2.90	2.89 kΩ	0.850	152.0 kΩ
1.350	51.5 kΩ	3.00	2.62 kΩ	0.875	98.8 kΩ
1.400	38.2 kΩ	3.10	2.39 kΩ	0.900	72.1 kΩ
1.450	30.2 kΩ	3.20	2.18 kΩ	0.925	56.1 kΩ
1.50	24.8 kΩ	3.30	1.99 kΩ	0.950	45.5 kΩ
1.55	21.0 kΩ	3.40	1.82 kΩ	0.975	37.8 kΩ
1.60	18.2 kΩ	3.50	1.66 kΩ	1.000	32.1 kΩ
1.65	16.0 kΩ	3.60	1.51 kΩ	1.025	27.7 kΩ
1.70	14.2 kΩ	3.70	1.38 kΩ	1.050	24.1 kΩ
1.75	12.7 kΩ	3.80	1.26 kΩ	1.075	21.2 kΩ
1.80	11.5 kΩ	3.90	1.14 kΩ	1.100	18.8 kΩ
1.85	10.5 kΩ	4.00	1.04 kΩ	1.125	16.7 kΩ
1.90	9.61 kΩ	4.10	939 Ω	1.150	15.0 kΩ
1.95	8.85 kΩ	4.20	847 Ω	1.175	13.5 kΩ
2.00	8.18 kΩ	4.30	761 Ω	1.200	12.1 kΩ
2.05	7.59 kΩ	4.40	680 Ω	1.250	9.91 kΩ
2.10	7.07 kΩ	4.50	604 Ω	1.300	8.13 kΩ
2.15	6.60 kΩ	4.60	533 Ω	1.350	6.68 kΩ
2.20	6.18 kΩ	4.70	466 Ω	1.400	5.46 kΩ
2.25	5.80 kΩ	4.80	402 Ω	1.450	4.44 kΩ
2.30	5.45 kΩ	4.90	342 Ω	1.50	3.56 kΩ
2.35	5.14 kΩ	5.00	285 Ω	1.55	2.8 kΩ
2.40	4.85 kΩ	5.10	231 Ω	1.60	2.13 kΩ
2.45	4.58 kΩ	5.20	180 Ω	1.65	1.54 kΩ
2.50	4.33 kΩ	5.30	131 Ω	1.70	1.02 kΩ
2.55	4.11 kΩ	5.40	85 Ω	1.75	551 Ω
2.60	3.89 kΩ	5.50	41 Ω	1.80	130 Ω
2.65	3.70 kΩ				

Features of the PTH/PTV Family of Non-Isolated, Wide-Output Adjust Power Modules

POLA™ Compatibility

The PTH/PTV family of non-isolated, wide-output adjustable power modules from Texas Instruments are optimized for applications that require a flexible, high-performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, non-isolated modules with the same footprint and form factor. POLA parts are also ensured to be interoperable, thereby providing customers with true second-source availability.

Soft-Start Power Up

The Auto-Track feature allows the power up of multiple PTH/PTV modules to be directly controlled from the Track pin. However, in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, V_i (see Figure 12).

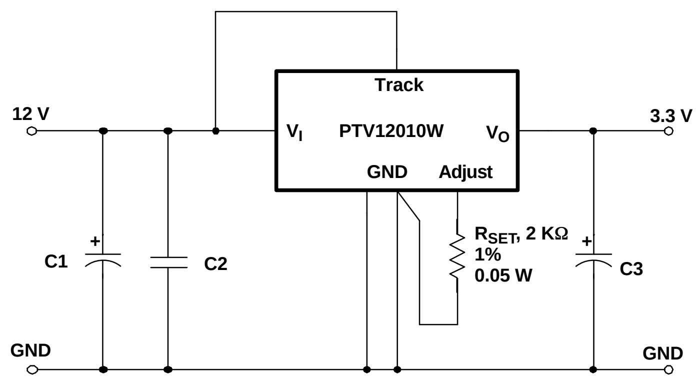


Figure 12.

When the *Track* pin is connected to the input voltage, the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set point at a quicker and more linear rate.

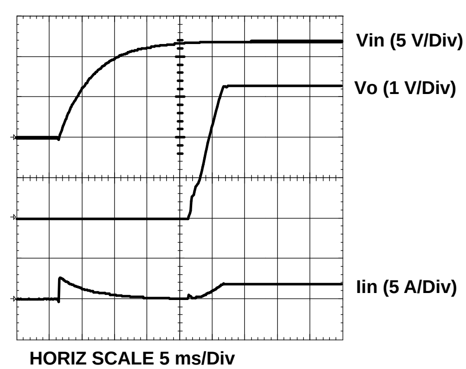


Figure 13.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms-15 ms) before allowing the output voltage to rise. The output then progressively rises to the module set-point voltage. Figure 13 shows the soft-start power-up characteristic of a PTH/PTV module, operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power up is complete within 25 ms.

Overcurrent Protection

For protection against load faults, the modules incorporate output overcurrent protection. Applying a load that exceeds the overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start power up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the modules incorporate an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* input is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 14 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The *Inhibit* input has its own internal pull up (see footnotes to electrical characteristics table). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

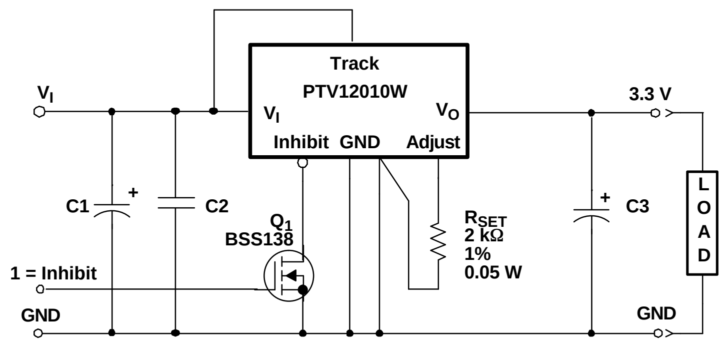


Figure 14.

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 25 ms. Figure 15 shows the typical rise in both the output voltage and input current, following the turnoff of Q1. The turnoff of Q1 corresponds to the rise in the waveform, Q1 V_{DS}. The waveforms were measured with a 5-A constant current load.

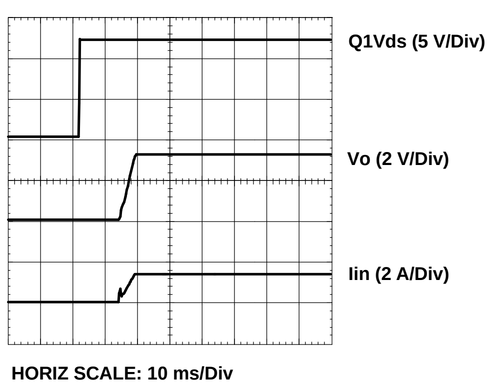


Figure 15.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the Track control pin [1]. This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set point [2]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC-ramp waveform, and allows them to be controlled through a single transistor or switch; see Q1 in Figure 16.

To initiate a power-up sequence, it is recommended that the Track control first be pulled to ground potential. This is done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic level high signal to the circuit On/Off Control turns Q1 on and applies a ground signal to the Track pins. After completing their internal soft-start intialization, the output of all modules remains at zero volts while Q1 is on.

Q1 may be turned off 10 ms after a valid input voltage has been applied to the modules. This allows the track control voltage to automatically rise to the module input voltage. During this period, the output voltage of each module rises in unison with other modules to its respective set-point voltage.

Figure 17 shows the output voltage waveforms from the circuit of Figure 16 after the On/Off Control is set from a high-level to a low-level voltage. The waveforms, V_O1 and V_O2 represent the output voltages from the two power modules, U1 (3.3 V) and U2 (2 V), respectively. V_O1 and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track slew rate capability, which is 1 V/ms. The components R1 and C1 in Figure 16 limit the rate at which Q1 pulls down the Track control voltage. The values of 100 kΩ and 0.1 µF correlate to a decay rate of about 0.17 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 18 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track control.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absloute maximum voltage that may be applied to the Track pin is the input voltage V_I.

4. The module does not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied to its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore, start up into an output prebias cannot be supported when a module is under Auto-Track control. ***Note:*** A prebias holdoff is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.
6. The Auto-Track function can be disabled by connecting the Track pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power is applied.

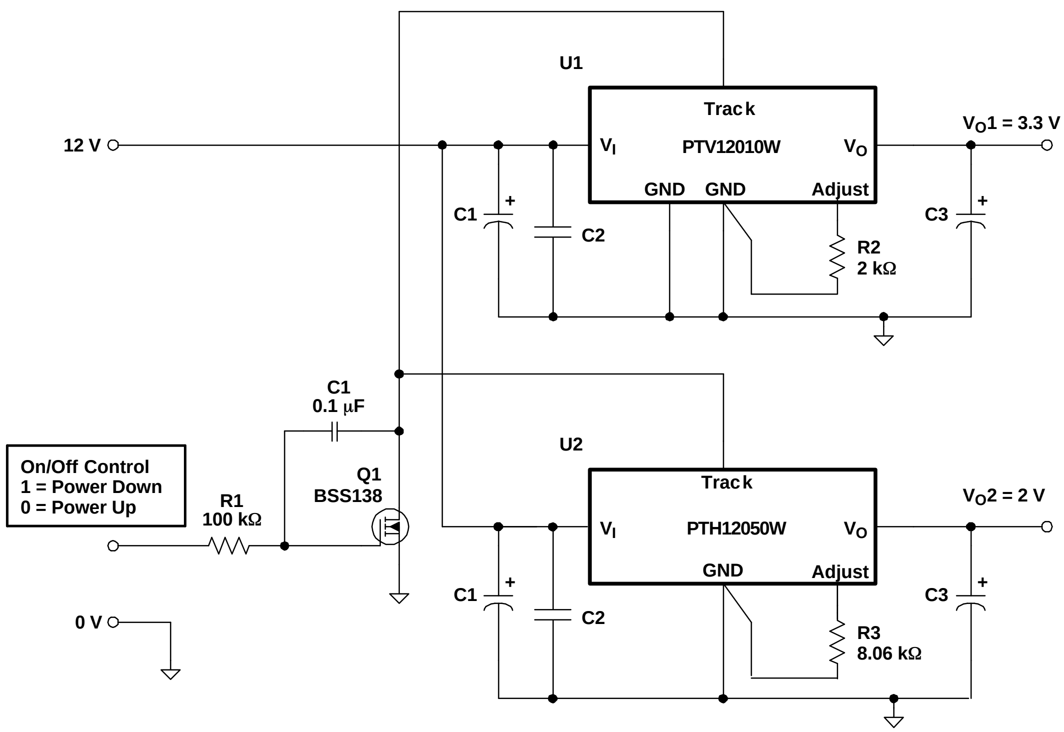


Figure 16. Sequenced Power Up and Power Down Using Auto-Track

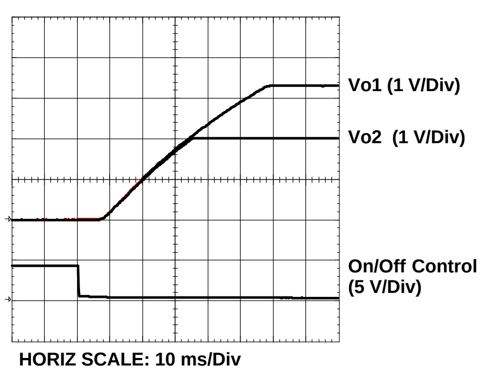


Figure 17. Simultaneous Power Up With Auto-Track Control

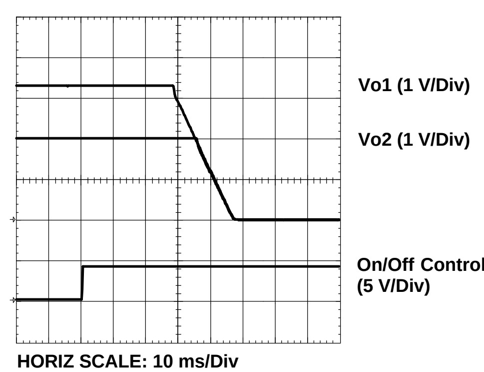


Figure 18. Simultaneous Power Down With Auto-Track Control

Prebias Start-Up Capability

A prebias start-up condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12-V input modules incorporate synchronous rectifiers, but do not sink current during start up, or whenever the *Inhibit* pin is held low. Start up includes an initial delay (approximately 8–15 ms), followed by the rise of the output voltage under the control of the module internal soft-start mechanism; see Figure 19.

Conditions for Prebias Holdoff

In order for the module to allow an output prebias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a prebias voltage when the *Inhibit* pin is held low, and whenever the output is allowed to rise under soft-start control. Power up under soft-start control occurs on the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled[2]. To further ensure that the regulator does not sink output current (even with a ground signal applied to its *Inhibit*), the input voltage must always be greater than the applied prebias source. This condition must exist throughout the power-up sequence[3].

The soft-start period is complete when the output begins rising above the prebias voltage. Once it is complete, the module functions as normal and sinks current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a prebias condition is not present, the soft-start period is complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module Track control pin, whichever is lowest, to its output.

Demonstration Circuit

Figure 20 shows the start-up waveforms for the demonstration circuit shown in Figure 21. The initial rise in V_O2 is the prebias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the module (I_O2) is negligible until its output voltage rises above the applied prebias.

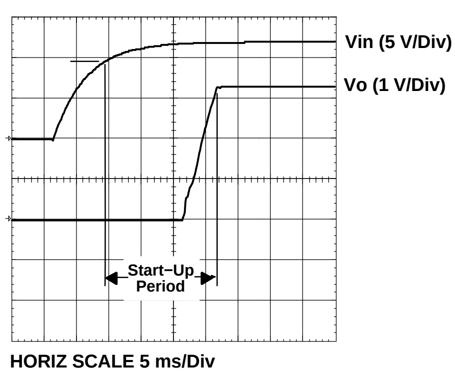


Figure 19. PTV12010W Start Up

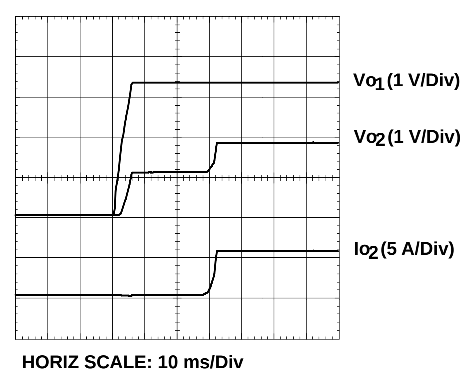


Figure 20. Prebias Start-Up Waveforms

NOTES:

1. The prebias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the *Track* control pin, the output sinks current during the period that the track control voltage is below that of the back-feeding source. For this reason, Auto-Track should be disabled when not being used. This is accomplished by connecting the *Track* pin to the input voltage, V_I. This raises the *Track* pin well above the set-point voltage prior to start up, thereby defeating the Auto-Track feature.
2. To further ensure that the regulator output does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage *must* always be greater than the applied prebias source. This condition must exist *throughout* the power-up sequence of the power system.

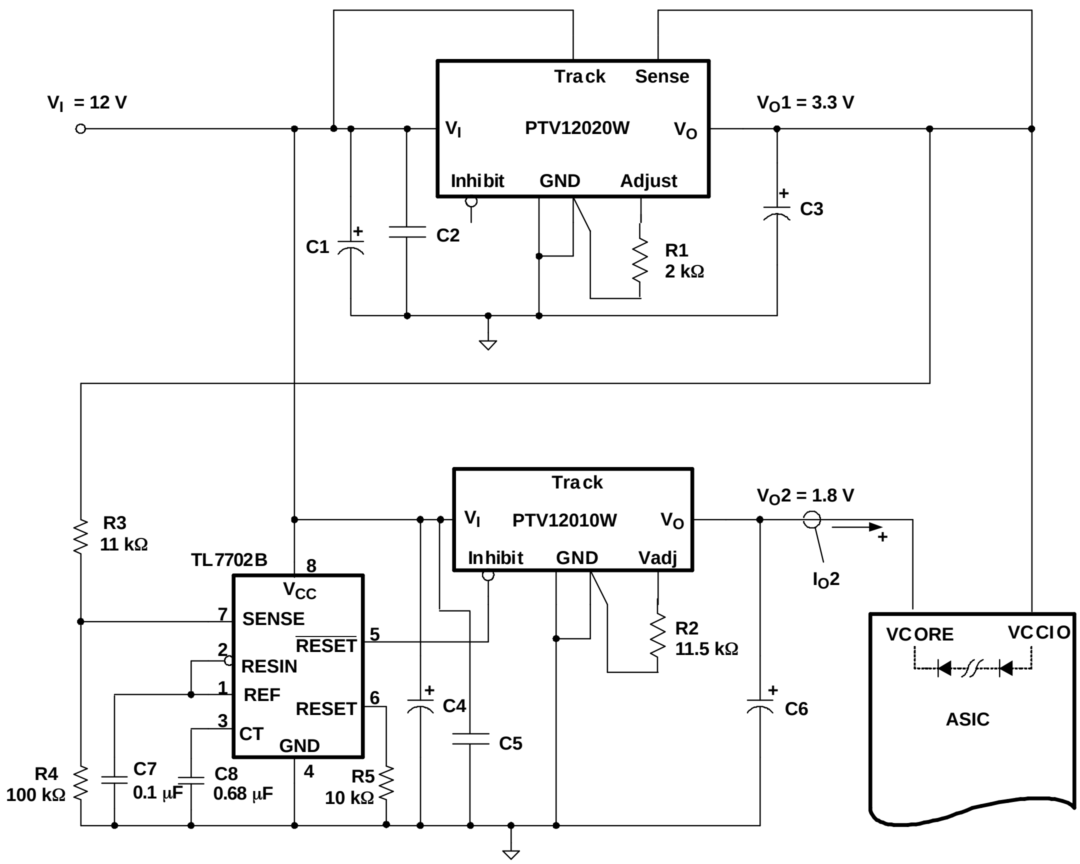


Figure 21. Application Circuit Demonstrating Prebias Startup

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PTV12010LAD	ACTIVE	SIP MOD ULE	EVA	8	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTV12010LAH	ACTIVE	SIP MOD ULE	EVA	8	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTV12010WAD	ACTIVE	SIP MOD ULE	EVA	8	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTV12010WAH	ACTIVE	SIP MOD ULE	EVA	8	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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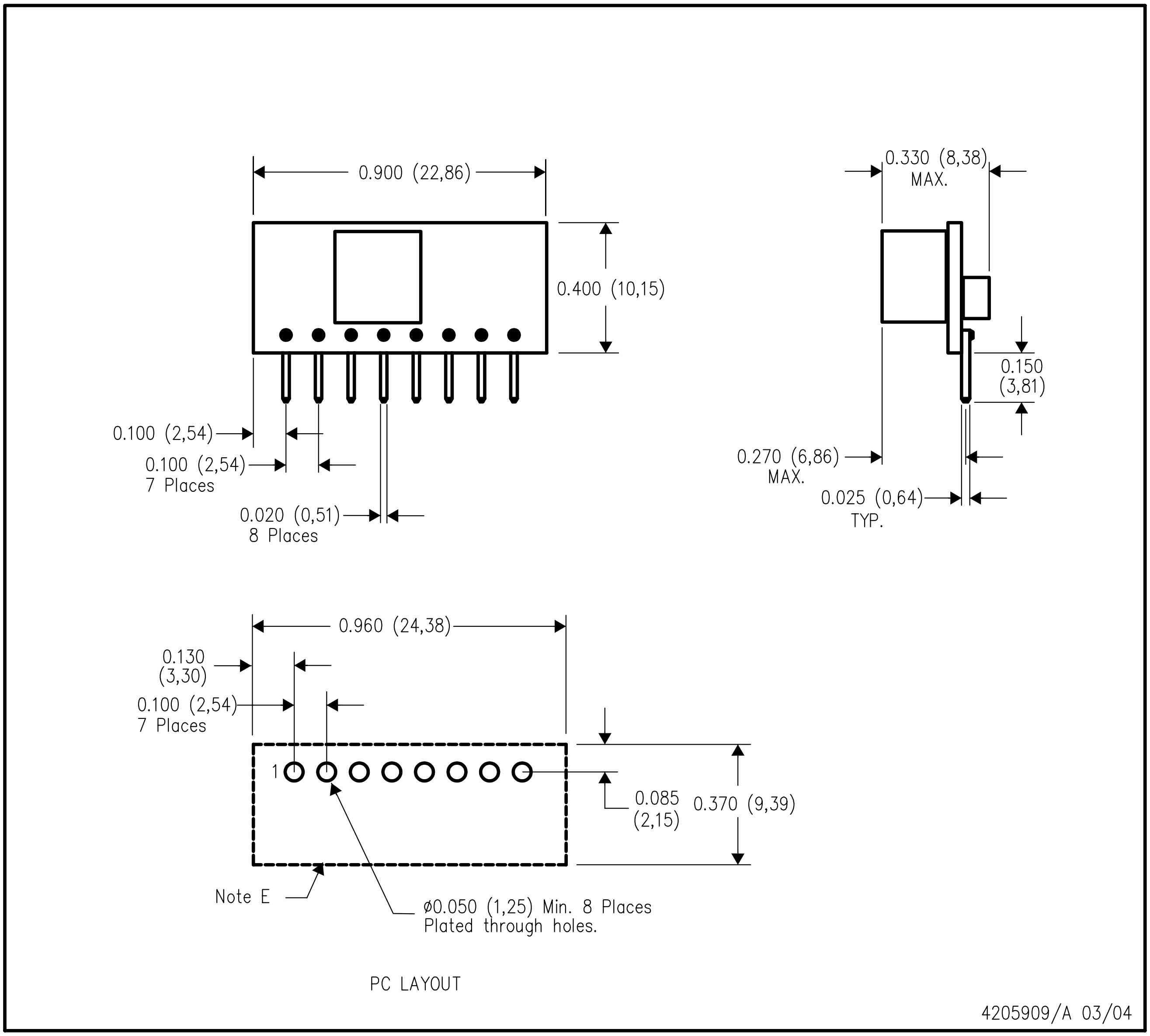
EVA (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0,51) x 0.025" (0,64).
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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