1.5-A, WIDE-INPUT ADJUSTABLE SWITCHING REGULATOR

FEATURES

- 1.5-A Output Current
- Wide-Input Voltage (7 V to 36 V) / (15 V to 36 V)
- Wide-Output Voltage Adjust (2.5 V to 12.6 V) / (11.85 V to 22 V)
- High Efficiency (Up to 95%)
- On/Off Inhibit
- Undervoltage Lockout
- Output Current Limit
- Overtemperature Shutdown
- Operating Temperature: –40°C to 85°C
- Surface Mount Package Available

APPLICATIONS

- General-Purpose, Industrial Controls, HVAC Systems, Test and Measurement, Medical Instrumentation, AC/DC Adaptors, Vehicles, Marine, and Avionics

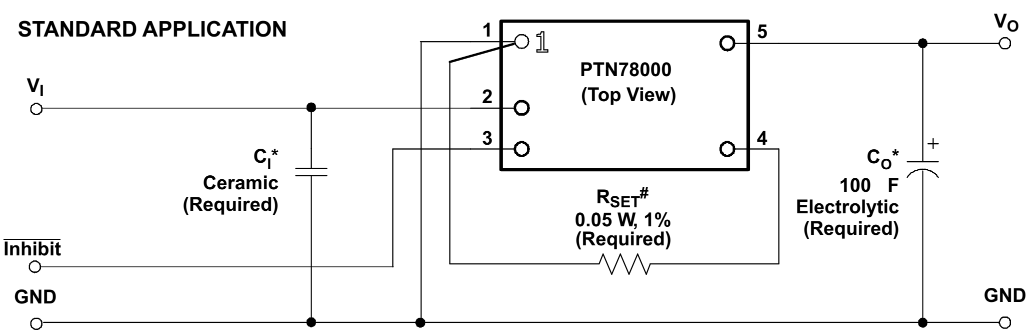
DESCRIPTION

The PTN78000 is a series of high-efficiency, step-down Integrated Switching Regulators (ISR), that represent the third generation in the evolution of the popular 78ST100 series of products. In new designs it should be considered in place of the 78ST100, PT78ST100, PT5100, and PT6100 series of single in-line pin (SIP) products. The PTN78000 is smaller and lighter than its predecessors, and has either similar or improved electrical performance characteristics. The case-less, double-sided package, also exhibits improved thermal characteristics, and is compatible with TI's roadmap for RoHS and lead-free compliance.

Operating from a wide-input voltage range, the PTN78000 provides high-efficiency, step-down voltage conversion for loads of up to 1.5 A. The output voltage is set using a single external resistor. The PTN78000W may be set to any value within the range, 2.5 V to 12.6 V, and the PTN78000H from 11.85 V to 22 V. The output voltage of the PTN78000W can be as little as 2 V lower than the input, allowing operation down to 7 V, with an output voltage of 5 V. The output voltage of the PTN78000H can be as little as 3 V lower than the input, alowing operation down to 15 V, with an output voltage of 12 V.

The PTN78000 has undervoltage lockout and an integral on/off inhibit. The modules are suited to a wide variety of general-purpose applications that operate off 12-V, 24-V, or 28-V dc power.

STANDARD APPLICATION



* See the *Application Information* section for capacitor recommendations. The minimum input capacitance is 2.2   F for PYN78000W, and 9.4   F (2 x 4.7   F) for PTN78000H.

\# R_{SET} is required to adjust the output voltage higher than 2.5 V for PTN78000W, and 11.824 V for PTN78000H. See the *Application Information* section for values.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PTN78000 (Basic Model)			
Output Voltage	**Part Number**	**Description**	**Package Designator**
2.5 V - 12.6 V	PTN78000WAH	Horizontal T/H	EUS
	PTN78000WAS (1)(2)	Horizontal SMD	EUT
	PTN78000WAZ (3)(2)		
11.85 V - 22 V	PTN78000HAH	Horizontal T/H	EUS
	PTN78000HAS (1)(2)	Horizontal SMD	EUT
	PTN78000HAZ (3)(2)		

(1) *Standard option* specifies Sn/Pb solder pin material.
(2) Add a T suffix for tape and reel option on SMD packages.
(3) *Lead (Pb) - free option* specifies Sn/Ag solder pin material.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range unless otherwise noted
all voltages with respect to GND (pin 1),

				UNIT
T_A	Operating free-air temperature	Over V_I range		–40°C to 85° C
	Solder reflow temperature	Surface temperature of module body or pins	Horizontal SMD (suffix AS)	235° C
			Horizontal SMD (suffix AZ)	260° C
T_{stg}	Storage temperature			–40° C to 125° C
V_I	Input surge voltage, 10 ms maximum			38 V
V_{INH}	Inhibit (pin 3) input voltage			–0.3 V to 5 V
P_O	Output power	$V_O \geq 15$ volts		22.5 W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Input voltage	PTN78000W	7	36	V
		PTN78000H	15	36	
T_A	Operating free-air temperature		–40	85	°C

PACKAGE SPECIFICATIONS

PTN78000x (Suffix AH, AS, and AZ)			
Weight			2 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		500 Gs (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Horizontal T/H (suffix AH)	20 Gs (1)
		Horizontal SMD (suffix AS and AZ)	15 Gs (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 20 V, V_O = 5 V, I_O = I_O (max), C_I = 2.2 µF, C_O = 100 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	PTN78000W			
				MIN	TYP	MAX	UNIT
I_O	Output current		T_A = 85°C, natural convection airflow	0		1.5	A
V_I	Input voltage range		Over I_O range	7 (1)		36 (2)	V
V_O	Set-point voltage tolerance		T_A = 25°C			±2% (3)	
	Temperature variation		–40°C to +85°C		±0.5%		
	Line regulation		Over V_I range		±10		mV
	Load regulation		Over I_O range		±10		mV
	Total output voltage variation		Includes set point, line, load –40°C < T_A < 85°C			±3% (3)	
V_O Adj	Output voltage adjust range		V_I < 12 V	2.5		V_I – 2	V
			12 V ≤ V_I ≤ 15.1 V	2.5		V_I – 2.5	
			15.1 V < V_I ≤ 25 V	2.5		12.6	
			V_I > 25 V	0.1 x V_I		12.6	
η	Efficiency		V_I = 24 V, R_{SET} = 732 Ω, V_O = 12 V		91%		
			V_I = 15 V, R_{SET} = 21 kΩ, V_O = 5 V		86%		
			V_I = 15 V, R_{SET} = 78.7 kΩ, V_O = 3.3 V		82%		
	Output voltage ripple		20 MHz bandwith		1% V_O		$V_{(PP)}$
$I_{O (LIM)}$	Current limit threshold		ΔV_O = –50 mV		3.2		A
	Transient response		1 A/µs load step from 50% to 100% $I_O$max				
			Recovery time		100		µs
			V_O over/undershoot		2.5		%V_O
UVLO	Undervoltage lockout		V_I increasing		5.5		V
			V_I decreasing		5.2		
	Inhibit control (pin 3)		Input high voltage (V_{IH})	1		Open (4)	V
			Input low voltage (V_{IL})	–0.1		0.3	
			Input low current (I_{IL})		–0.25		mA
$I_{I (STBY)}$	Input standby current		Pin 3 connected to GND		17		mA
F_S	Switching frequency		Over V_I and I_O ranges	440	550	660	kHz
C_I	External input capacitance		Ceramic	2.2 (5)			µF
C_O	External output capacitance		Nonceramic	100 (6)			µF
			Ceramic			200	
			Equiv. series resistance (nonceramic)	10 (7)			mΩ
MTBF	Calculated reliability		Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign	8.9			10^6 Hr

(1) For output voltages less than 10 V, the minimum input voltage is 7 V or (V_O + 2) V, whichever is greater. For output voltages of 10 V and higher, the minimum input voltage is (V_O + 2.5) V. See the Application Information section for further guidance.
(2) For output voltages less than 3.6 V, the maximum input voltage is 10 × V_O . See the Application Information section for further guidance.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with with 100 ppm/°C or better temperature stability.
(4) This control pin has an internal pullup, and if left open circuit, the module operates when input power is applied. The open-circuit voltage is typically 1.5 V. A smal,l low-leakage (< 100 nA) MOSFET is recommended for control. See the Application Information section for further guidance.
(5) An external 2.2-µF ceramic capacitor is required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
(6) 100 µF of output capacitance is required for proper operation. See the Application Information section for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 mΩ as the minimum when using maximum ESR values to calculate.

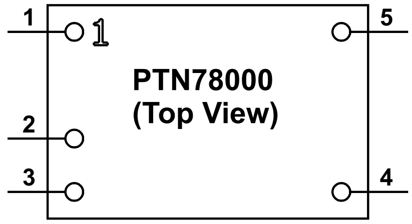
ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 24 V, V_O = 12 V, I_O = I_O (max), C_I = 2× 4.7 µF, C_O = 100 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PTN78000H MIN	TYP	MAX	UNIT
I_O	Output current	T_A = 85°C, natural convection airflow	V_O = 12 V	0.1		1.5	A
			V_O = 15 V	0.1		1.5 (1)	
			V_O = 22 V	0.1		1 (1)	
V_I	Input voltage range	Over I_O range		15 (2)		36	V
V_O	Set-point voltage tolerance	T_A = 25°C				±2% (3)	
	Temperature variation	–40°C to +85°C			±0.5%		
	Line regulation	Over V_I range			±10		mV
	Load regulation	Over I_O range			±10		mV
	Total output voltage variation	Includes set point, line, load –40°C < T_A < 85°C				±3% (3)	
V_O Adj	Output voltage adjust range		V_I < 19 V	11.85		V_I – 3	V
			19 V ≤ V_I ≤ 25 V	11.85		V_I – 4	
			V_I > 25 V	11.85		22	
η	Efficiency		V_I = 24 V, R_{SET} = 383 k Ω, V_O = 12 V		91%		
			V_I = 24 V, R_{SET} = 15 kΩ, V_O = 15 V		93%		
			V_I = 32 V, R_{SET} = 95.3 Ω, V_O = 22 V		94%		
	Output voltage ripple	20 MHz bandwith			1% V_O		$V_{(PP)}$
$I_{O\ (LIM)}$	Current limit threshold	ΔV_O = –50 mV, minimum V_I			2 × $I_{O\ (MAX)}$		A
	Transient response	1 A/µs load step from 50% to 100% $I_O$max					
			Recovery time		200		µs
			V_O over/undershoot		1		%V_O
UVLO	Undervoltage lockout	V_I increasing			12.2		V
		V_I decreasing			12		
	Inhibit control (pin 3)	Input high voltage (V_{IH})		1		Open (4)	V
		Input low voltage (V_{IL})		–0.1		0.3	
		Input low current (I_{IL})			–0.25		mA
$I_{I\ (STBY)}$	Input standby current	Pin 3 connected to GND			17		mA
F_S	Switching frequency	Over V_I and I_O ranges		440	550	660	kHz
C_I	External input capacitance	Ceramic		9.4 (5)			µF
C_O	External output capacitance	Nonceramic		100 (6)			µF
		Ceramic				200	
		Equiv. series resistance (nonceramic)		10 (7)			mΩ
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		8.9			10^6 Hr

(1) The maximum output current is 1.5 A or the maximum output power is 22.5 W, whichever is less.
(2) For output voltages less than 19 V, the minimum input voltage is 15 V or (V_O + 3) V, whichever is greater. For output voltages of 19 V and higher, the minimum input voltage is (V_O + 4) V. See the Application Information section for further guidance.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with with 100 ppm/°C or better temperature stability.
(4) This control pin has an internal pullup, and if left open circuit, the module operates when input power is applied. The open-circuit voltage is typically 1.5 V. A small, low-leakage (< 100 nA) MOSFET is recommended for control. See the Application Information section for further guidance.
(5) Two external 4.7-µF ceramic capacitors are required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
(6) 100 µF of output capacitance is required for proper operation. See the Application Information section for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 mΩ as the minimum when using maximum ESR values to calculate.

PIN ASSIGNMENT



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1	I/O	This is the common ground connection for the V_I and V_O power connections. It is also the 0 V_{dc} reference for the *Inhibit* and V_O *Adjust* control inputs.
V_I	2	I	The positive input voltage power node to the module, which is referenced to common GND.
Inhibit	3	I	The Inhibit pin is an open-collector/drain active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module will produce an output whenever a valid input source is applied.
V_O Adjust	4	O	A 1% resistor must be connected between this pin and GND (pin 1) to set the output voltage. If left open-circuit, the output voltage defaults to its minimum adjust value. The temperature stability of the resistor should be 100 ppm/°C (or better). The PTN78000W set-point range is 2.5 V to 12.6 V. The PTN78000H set-point range is 11.85 V to 22 V. The standard resistor value for a number of common output voltages is provided in the application information.
V_O	5	O	The regulated positive power output with respect to the GND node.

TYPICAL CHARACTERISTICS (7-V INPUT)(1)(2)

EFFICIENCY
vs
OUTPUT CURRENT

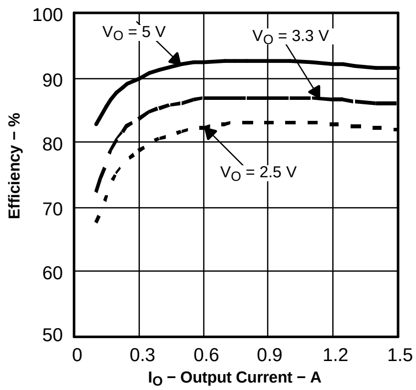


Figure 1.

OUTPUT VOLTAGE RIPPLE
vs
OUTPUT CURRENT

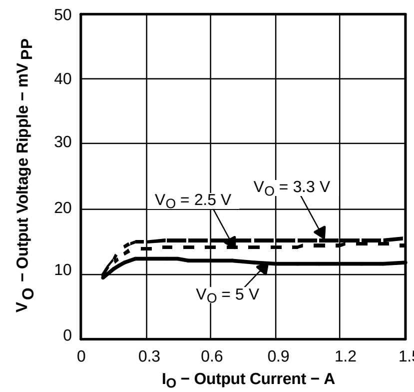


Figure 2.

POWER DISSIPATION
vs
OUTPUT CURRENT

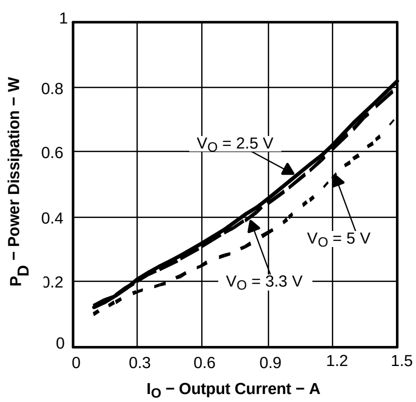


Figure 3.

TEMPERATURE DERATING
vs
OUTPUT CURRENT

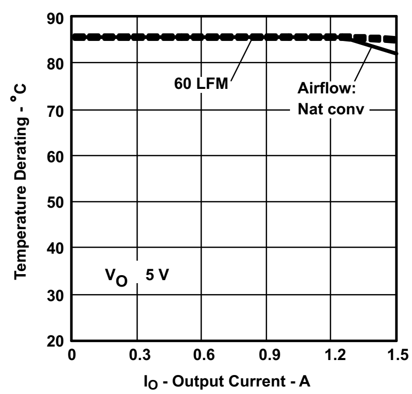


Figure 4.

(1) The electrical characteristic data has been developed from actual products tested at 25° C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 4.

TYPICAL CHARACTERISTICS (15-V INPUT)(1)(2)

EFFICIENCY vs OUTPUT CURRENT

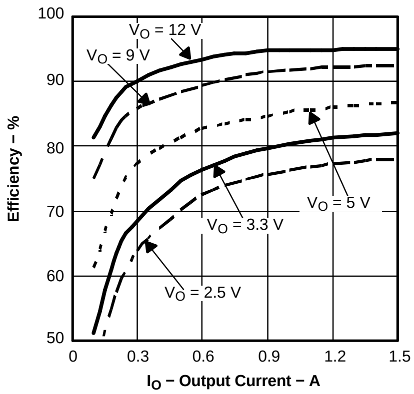


Figure 5.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

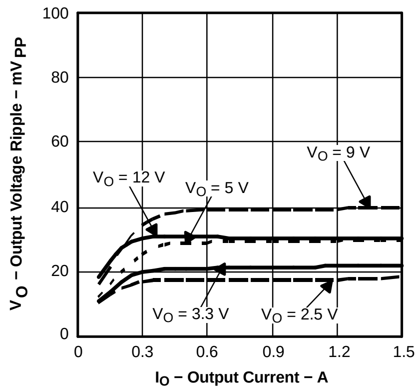


Figure 6.

POWER DISSIPATION vs OUTPUT CURRENT

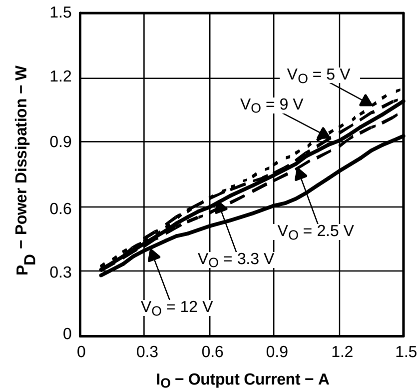


Figure 7.

TEMPERATURE DERATING vs OUTPUT CURRENT

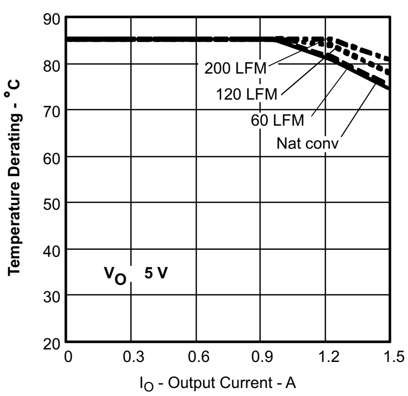


Figure 8.

TEMPERATURE DERATING vs OUTPUT CURRENT

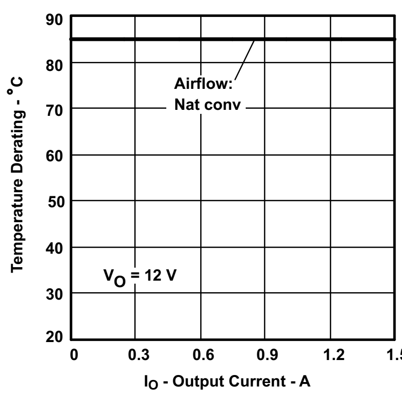


Figure 9.

(1) The electrical characteristic data has been developed from actual products tested at 25° C. This data is considered typical for the converter. Applies to Figure 5, Figure 6, and Figure 7.
(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 8 and Figure 9.

TYPICAL CHARACTERISTICS (24-V INPUT)(1)(2)

EFFICIENCY vs OUTPUT CURRENT

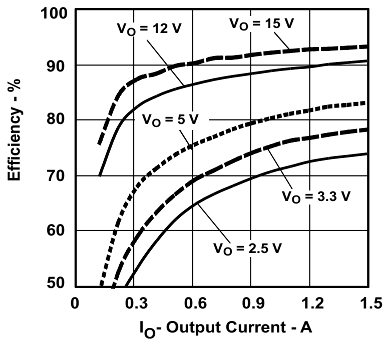


Figure 10.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

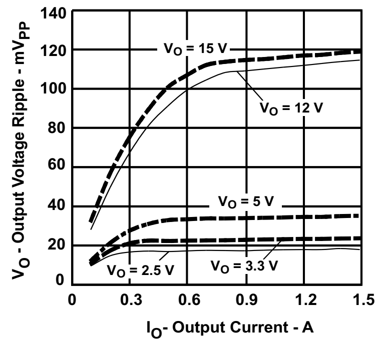


Figure 11.

POWER DISSIPATION vs OUTPUT CURRENT

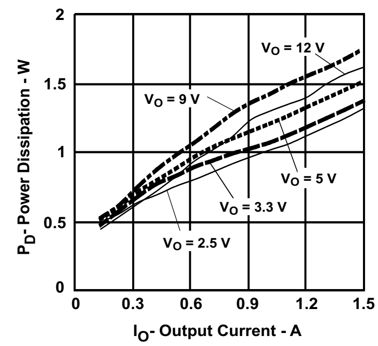


Figure 12.

TEMPERATURE DERATING vs OUTPUT CURRENT

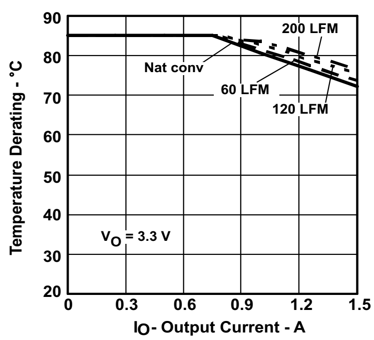


Figure 13.

TEMPERATURE DERATING vs OUTPUT CURRENT

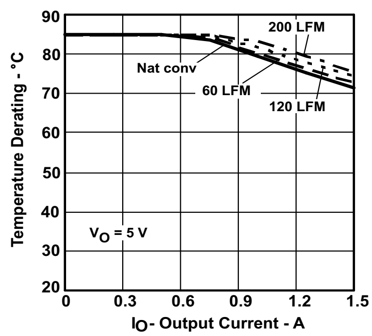


Figure 14.

TEMPERATURE DERATING vs OUTPUT CURRENT

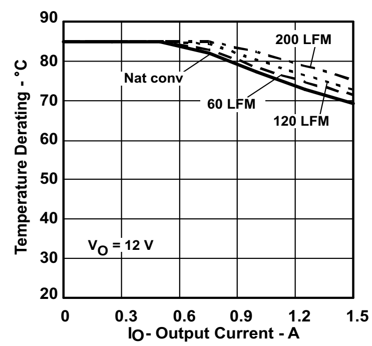


Figure 15.

TEMPERATURE DERATING vs OUTPUT CURRENT

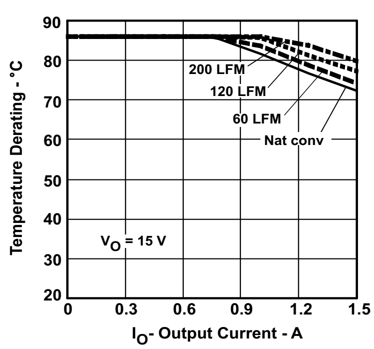


Figure 16.

TEMPERATURE DERATING vs OUTPUT CURRENT

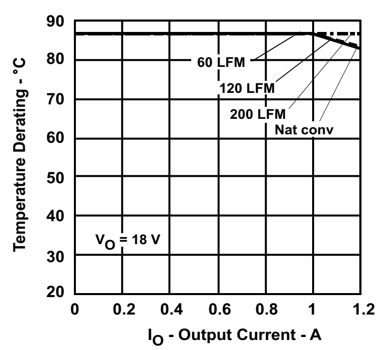


Figure 17.

(1) The electrical characteristic data has been developed from actual products tested at 25° C. This data is considered typical for the converter. Applies to Figure 10, Figure 11, and Figure 12.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 13 through Figure 17.

TYPICAL CHARACTERISTICS (32-V INPUT)(1)(2)

EFFICIENCY vs OUTPUT CURRENT

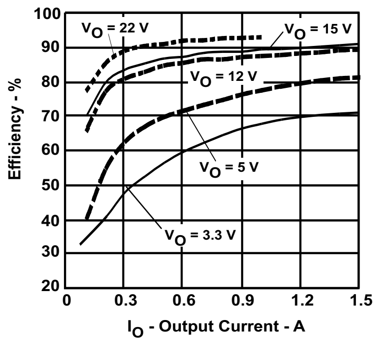


Figure 18.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

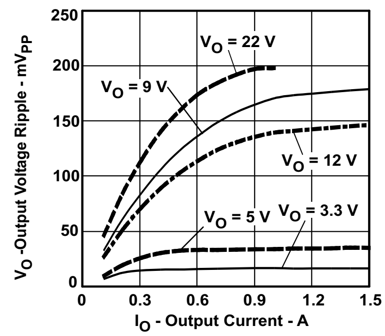


Figure 19.

POWER DISSIPATION vs OUTPUT CURRENT

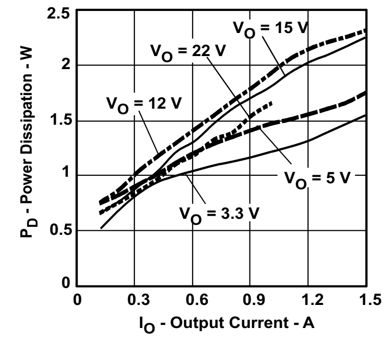


Figure 20.

TEMPERATURE DERATING vs OUTPUT CURRENT

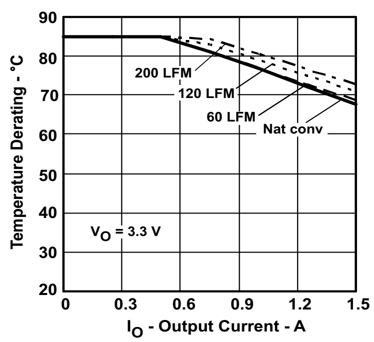


Figure 21.

TEMPERATURE DERATING vs OUTPUT CURRENT

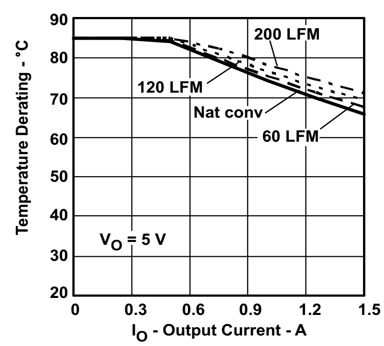


Figure 22.

TEMPERATURE DERATING vs OUTPUT CURRENT

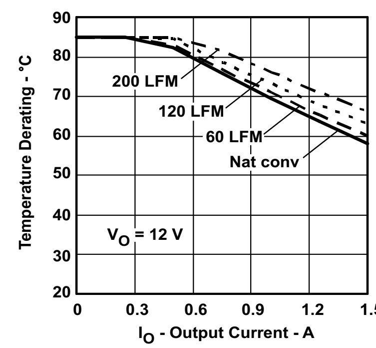


Figure 23.

TEMPERATURE DERATING vs OUTPUT CURRENT

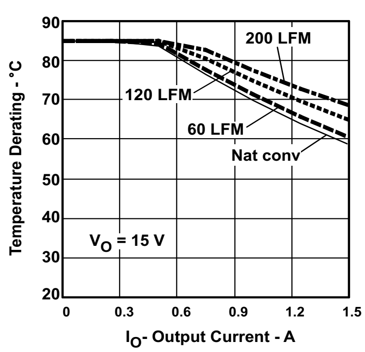


Figure 24.

TEMPERATURE DERATING vs OUTPUT CURRENT

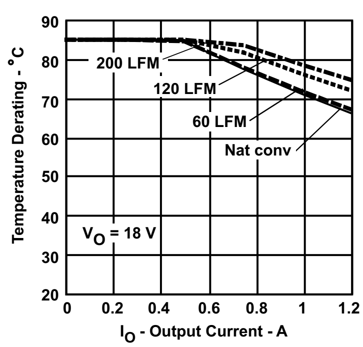


Figure 25.

TEMPERATURE DERATING vs OUTPUT CURRENT

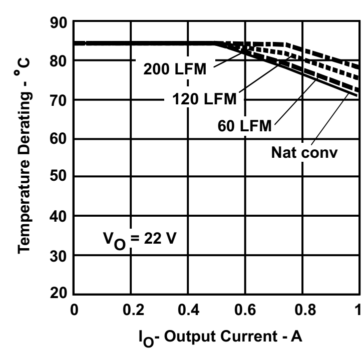


Figure 26.

(1) The electrical characteristic data has been developed from actual products tested at 25° C. This data is considered typical for the converter. Applies to Figure 18, Figure 19, and Figure 20.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 21 through Figure 26.

APPLICATION INFORMATION

Adjusting the Output Voltage of the PTN78000 Wide-Output Adjust Power Modules

General

A resistor must be connected between the V_O *Adjust* control (pin 4) and *GND* (pin 1) to set the output voltage. The adjustment range is from 2.5 V to 12.6 V for PTN78000W. The adjustment range is from 11.85 V to 22 V for PTN78000H. If pin 4 is left open, the output voltage defaults to the lowest value.

Table 2 gives the preferred value of the external resistor for several standard voltages, with the actual output voltage that the value provides. For other output voltages, the value of the required resistor can be calculated using Equation 1, and the constants for the applicable product in Table 1. Alternatilvey, R_{SET} can be simply selected from the range of values given in Table 3. Figure 27 shows the placement of the required resistor.

(1)

Table 1. R_{SET} Formula Constants

PRODUCT	V_{MIN}	R_P
PTN780x0W	2.5 V	6.49 kΩ
PTN780x0H	11.824 V	6.65 kΩ

Input Voltage Considerations

The PTN78000 is a step-down switching regulator. In order that the output remains in regulation, the input voltage must exceed the output by a minimum differential voltage. (Please refer to the input voltage range requirements in the electrical characteristics table.)

Another consideration is the pulse width modulation (PWM) range of the regulator's internal control circuit. For stable operation, its operating duty cycle should not be lower than some minimum percentage. This defines the maximum advisable ratio between the regulator input and output voltage magnitudes.

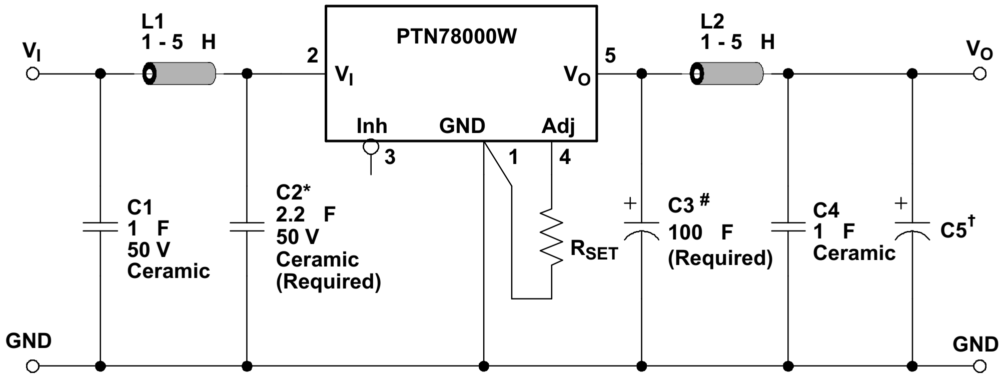
As an example, for satisfactory performance, the operating input voltage range of the PTN78000x must adhere to the following requirements.

1. For PTN78000W output voltages lower than 10 V, the minimum input voltage is (V_O + 2 V) or 7 V, whichever is higher.
2. For PTN78000W output voltages equal to 10 V and higher, the minimum input voltage is (V_O + 2.5 V) .
3. For PTN78000W, the maximum input voltage is (10 x V_O) or 36 V, whichever is less.
4. For PTN78000H output voltages lower than 19 V, the minimum input voltage is (V_O + 3 V) or 15 V, whichever is higher.
5. For PTN78000H output voltages equal to 19 V and higher, the minimum input voltage is (V_O + 4 V) .

As an example, Table 2 gives the operating input voltage range for the common output bus voltages. In addition, the Electrical Characteristics define the available output voltage adjust range for various input voltages.

Table 2. Standard Values of R_{set} for Common Output Voltages

PRODUCT	V_O (Required)	R_{SET} (Standard Value)	V_O (Actual)	Operating V_I Range
PTN780x0W	2.5 V	Open	2.5 V	7 V to 25 V
	3.3 V	78.7 kΩ	3.306 V	7 V to 33 V
	5 V	21 kΩ	4.996 V	7 V to 36 V
	12 V	732 Ω	12.002 V	14.5 V to 36 V
PTN780x0H	12 V	383 kΩ	12.000 V	15 V to 36 V
	15 V	15 kΩ	14.994 V	18 V to 36 V
	18 V	4.42 kΩ	18.023 V	21 V to 36 V
	22 V	95.3	21.998 V	26 V to 36 V



* See specifications for required value and type. For the PTN78000H, C2 is equal to 2x 4.7 F.
# See the Application Information for suggested value and type.
† Recommended when I_O is greater than 2 A.

Figure 33. Adding π Filters ($I_O \leq 3$ A)

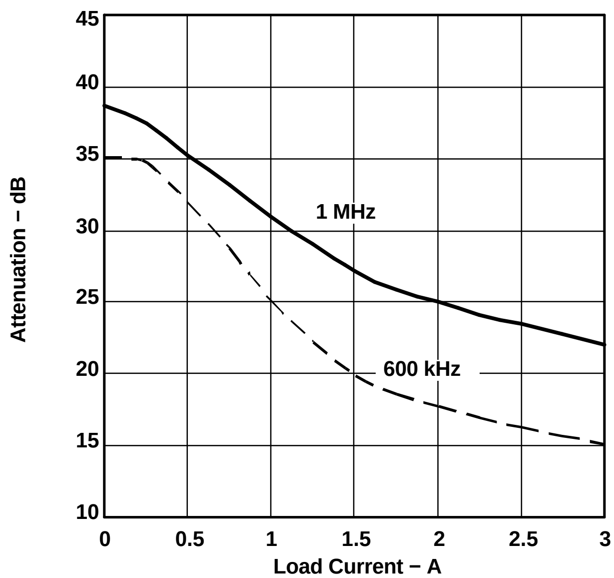


Figure 34. π-Filter Attenuation vs. Load Current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PTN78000HAH	ACTIVE	DIP MOD ULE	EUS	5	56	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTN78000HAS	ACTIVE	DIP MOD ULE	EUT	5	49	TBD	Call TI	Level-1-235C-UNLIM
PTN78000HAST	ACTIVE	DIP MOD ULE	EUT	5	250	TBD	Call TI	Level-1-235C-UNLIM
PTN78000HAZ	ACTIVE	DIP MOD ULE	EUT	5	49	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTN78000HAZT	ACTIVE	DIP MOD ULE	EUT	5	250	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTN78000WAH	ACTIVE	DIP MOD ULE	EUS	5	56	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTN78000WAS	ACTIVE	DIP MOD ULE	EUT	5	49	TBD	Call TI	Level-1-235C-UNLIM
PTN78000WAST	ACTIVE	DIP MOD ULE	EUT	5	250	TBD	Call TI	Level-1-235C-UNLIM
PTN78000WAZ	ACTIVE	DIP MOD ULE	EUT	5	49	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR
PTN78000WAZT	ACTIVE	DIP MOD ULE	EUT	5	250	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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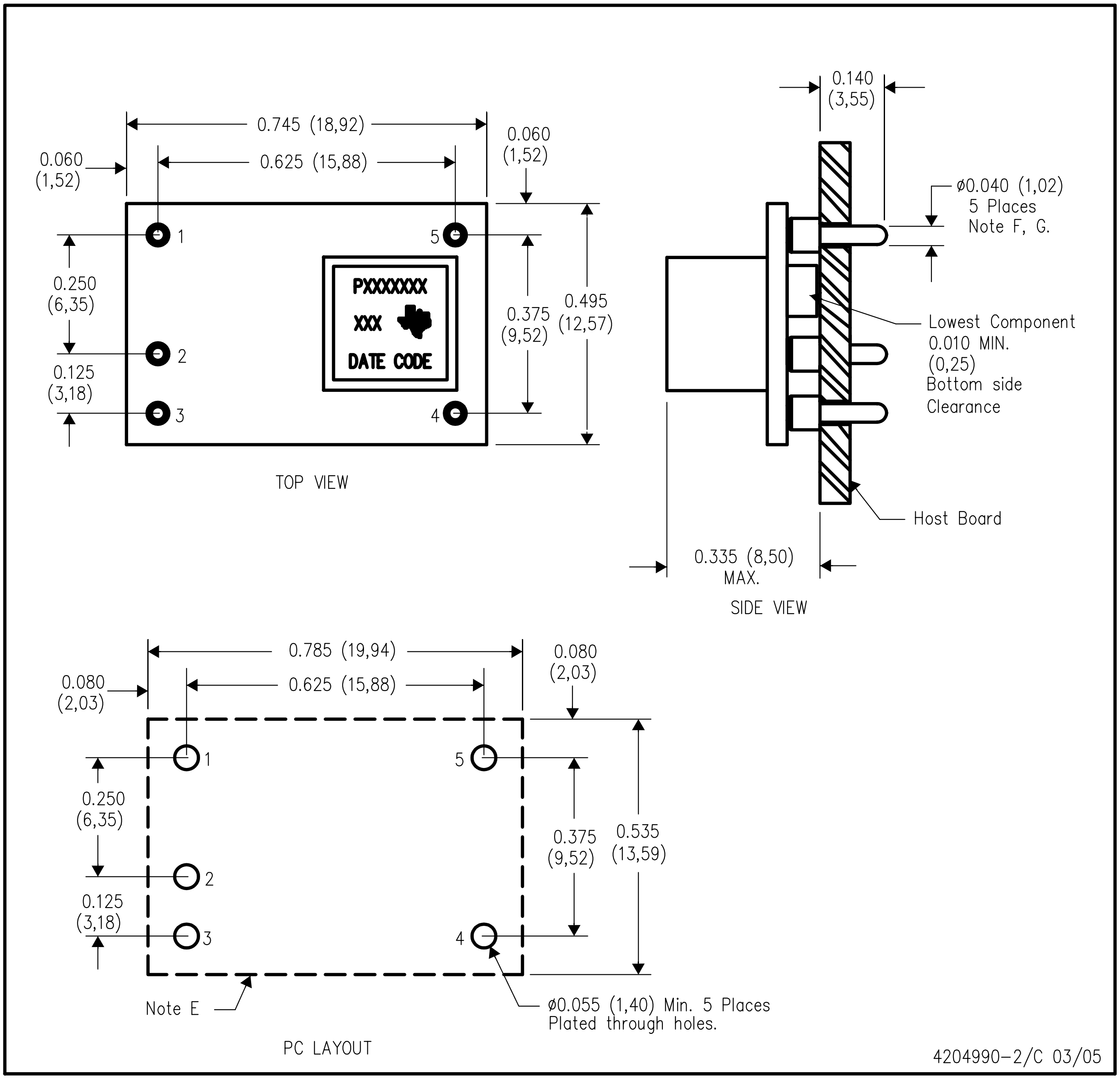
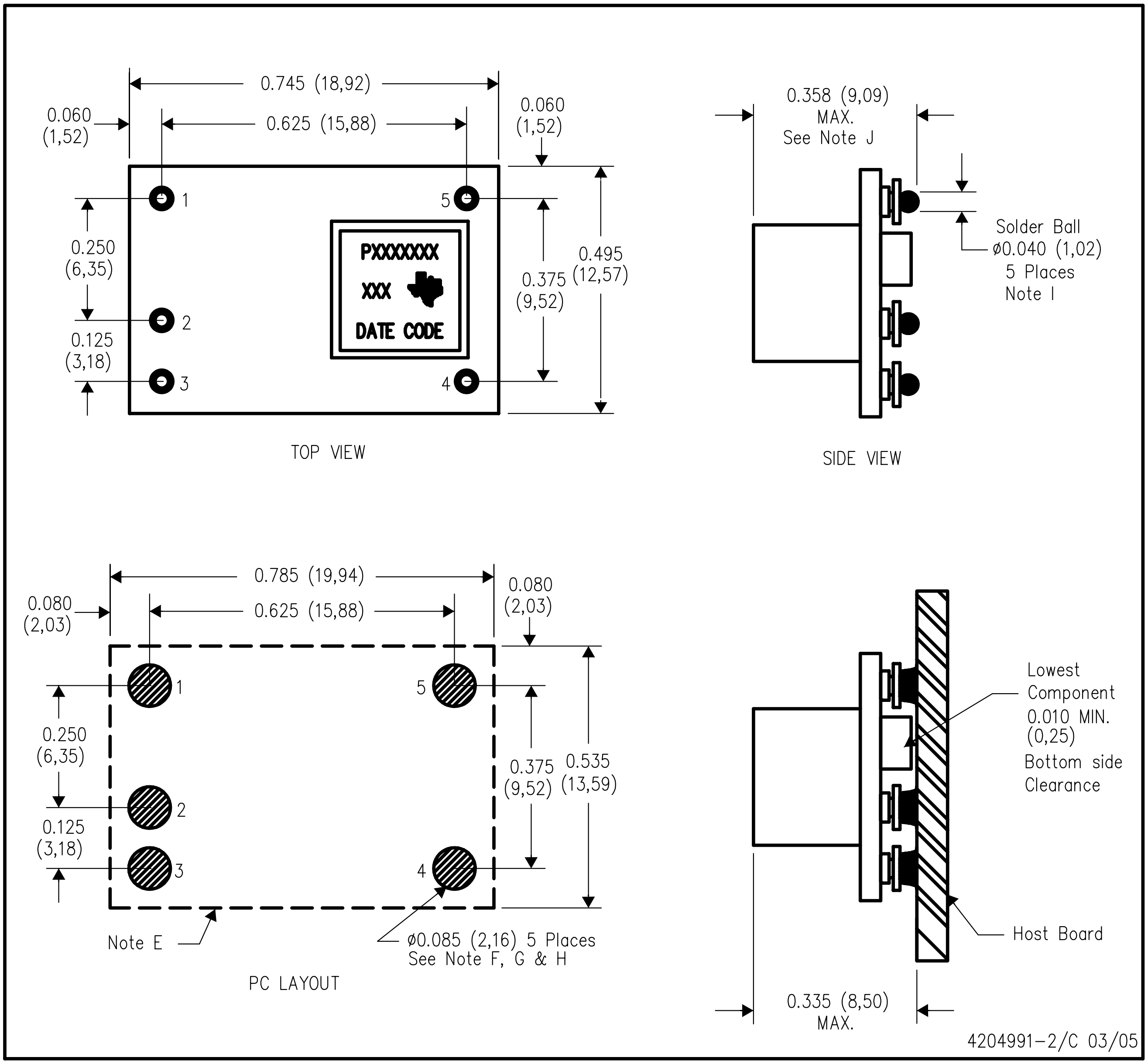
EUS (R–PDSS–T5) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EUT (R–PDSS–B5) DOUBLE SIDED MODULE



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.030 (±0,76mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended keep out area for user components.
- F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material – Copper Alloy
  Finish – Tin (100%) over Nickel plate
  Solder Ball – See product data sheet.
- J. Dimension prior to reflow solder.