FEATURES

- 2.5 GHz Bandwidth
- 4.0 kΩ Differential Transimpedance
- 10 pA/√Hz Typical Input Referred Noise
- 2 mA Maximum Input Current
- Offset Cancellation
- Received Signal Strength Indication
- Differential CML Data Outputs
- Single +3.3V Supply
- Bare-Die Option

APPLICATIONS

- SONET OC-48
- SDH STM-16
- APD Preamplifier-Receivers
- PIN Preamplifier-Receivers

DESCRIPTION

The ONET2511TA is a high-speed transimpedance amplifier used in SDH/SONET systems with data rates up to 2.5Gbps. It features a low input referred noise, 2.5GHz bandwidth, 4.0kΩ transimpedance, and a received signal strength indicator.

The ONET2511TA device is available in die form and requires a single +3.3V supply. It is very power efficient and dissipates less than 83 mW (typical). It is characterized for operations from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	DIE
–40°C to 85°C	ONET2511TAY

DETAILED DESCRIPTION

BLOCKDIAGRAM

The ONET2511TA is a high performance 2.5 Gbps transimpedance amplifier that can be segmented into the signal path, filter, and offset cancellation block.

The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and an output buffer.

The filter circuit provides a filtered VCC for the photodiode.

The offset correction circuit uses an internal low pass filter to cancel the DC on the input and it provides a signal to monitor the received signal strength.

A simplified block diagram of the ONET2511TA is shown in Figure 1.

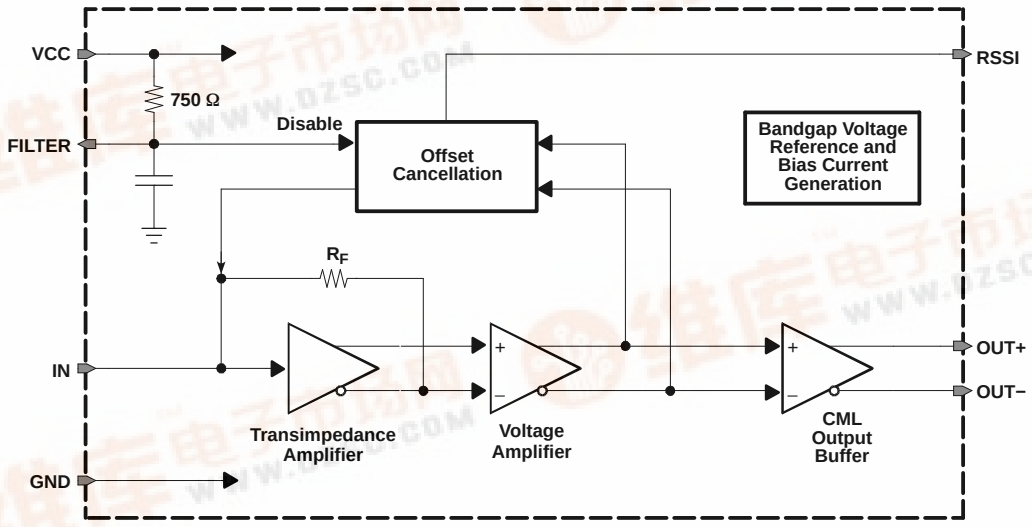

Figure 1. Simplified Block Diagram of the ONET2511TA

DETAILED DESCRIPTION (continued)

SIGNAL PATH

The first stage of the signal path is a transimpedance amplifier that takes the photodiode current and converts it to a voltage signal. The second stage is a voltage amplifier that provides additional gain. The output of the second stage feeds the output buffer and the offset cancellation circuitry. The third and final signal path stage of the ONET2511TA is the output buffer. The output buffer provides CML outputs with an on-chip 50Ω back-termination to VCC.

FILTER CIRCUITRY

The filter pin provides a filtered VCC for the photodiode bias. The on-chip low pass filter for the photodiode VCC is implemented using a filter resistor of 750Ω and an internal capacitor. If additional filtering is required for the application, an external capacitor should be connected to the FILTER pin.

OFFSET CANCELLATION AND RSSI

The offset cancellation circuitry performs low pass filtering of the output signal of the voltage amplifier. This senses the DC offset at the input of the ONET2511TA. The circuitry subtracts current from the input to effectively cancel the DC. The sensed current is mirrored and is used to generate the RSSI output through an external 10 kΩ resistor. To disable the offset correction loop, the FILTER pin should be tied to GND.

BOND PAD DESCRIPTION

The ONET2511TA is available as bare-die. The location of the bondpads is shown in Figure 2. The circuit is characterized for ambient temperatures between –40°C and 85°C. Table 1 shows the pad descriptions for the ONET2511TA.

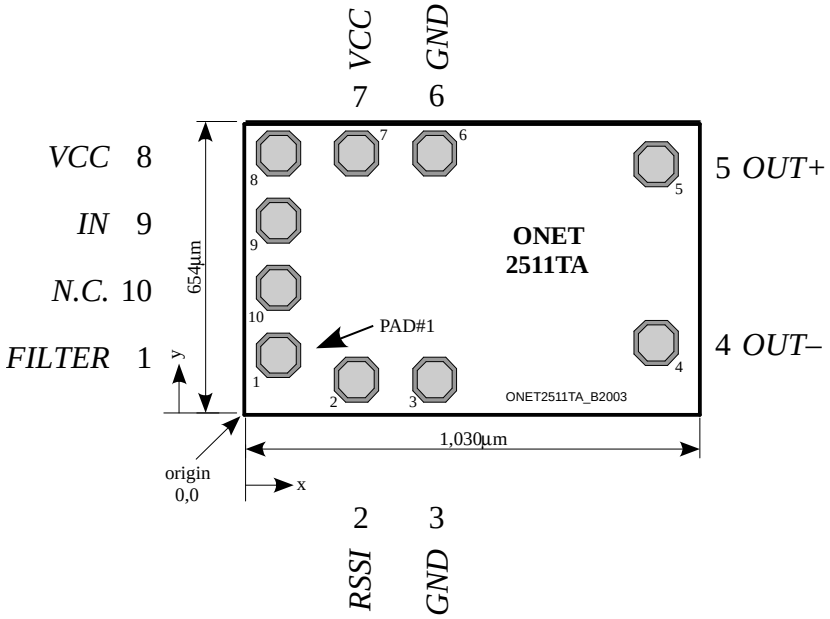

Figure 2. Bond Pad Assignment of ONET2511TA

Table 1. Pad Description of the ONET2511TA

PAD	SYMBOL	TYPE	DESCRIPTION
1	FILTER	Analog	Bias voltage for photodiode (connects to an internal 750-Ω resistor to V_{CC}). To disable offset correction loop connect FILTER to GND.
2	RSSI	Analog-Out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).
3, 6	GND	Supply	Circuit ground.

DETAILED DESCRIPTION (continued)

Table 1. Pad Description of the ONET2511TA (continued)

PAD	SYMBOL	TYPE	DESCRIPTION
4	OUT-	Analog-Out	Inverted data output. On-chip 50-Ω back-terminated to V_{CC}.
5	OUT+	Analog-Out	Non-inverted data output. On-chip 50-Ω back-terminated to V_{CC}.
7, 8	VCC	Supply	3.3-V ± 10% supply voltage
9	IN	Analog-In	Data input to TIA. Connect to anode of PIN or APD diode.
10	NC		Not connected

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage(2)	-0.3 to 4.0	V
V_{OUT+} V_{OUT-}	Voltage of OUT+ and Out-(2)	V_{CC}– 1.5 to V_{CC} +0.5	V
V_{FILTER} V_{RSSI}	Voltage of FILTER and RSSI(2)	-0.3 to 4.0	V
I_{IN}	Current into IN	-4 to 4	mA
I_{FILTER}	Current into FILTER	-8 to 8	mA
ESD	ESD rating at all pins except IN(3)	2	kV (HBM)
	ESD rating at IN(3)	1	kV (HBM)
T_{Jmax}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-65 to 85	°C
T_A	Operating free-air tempature	-40 to 85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) For optimum high-frequency performance, the input pin has reduced ESD protection.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
T_A	Operating free-air temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{CC}	Supply current			25	35	mA
V_{IB}	Input bias voltage		0.66	0.83	1.1	V
I_{IN-OVL}	DC input overload current		2			mA
R_{OUT}	Ouput resistance (OUT+, OUT-)	Single-ended to V_{CC}		50		Ω
R_{FILTER}	Photodiode filter resistance (FILTER)			750		Ω

AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN-OVL}	AC input overload current		2			mA_{p-p}
	Input linear range	0.95 < linearity < 1.05		40		μA_{p-p}
A_{RSSI}	RSSI gain	10-kΩ load		2000		V/A
Z_{21}	Small-signal transimpedance	Differential output	3000	4000	5000	Ω
f_{H-3dB}	Small-signal bandwidth	$C_{EXTERNAL}$ = 0.85 pF(1)		2.5		GHz
f_{L-3dB}	Low-frequency -3dB bandwidth	-3 dB, I_{IN} < 20 µA DC		7		kHz
$f_{H-3dB-RSSI}$	RSSI bandwidth			4		kHz
I_{N-IN}	Input refered RMS noise			470	640	nA_{RMS}
	Input refered noise density			10		pA/√Hz
DJ	Deterministic jitter	I_{IN} = 10 µA (K28.5 pattern)		21		ps_{p-p}
		I_{IN} = 100 µA (K28.5 pattern)		25		ps_{p-p}
		I_{IN} = 2 mA (K28.5 pattern)		16		ps_{p-p}
$V_{OD(MAX)}$	Differential output voltage, maximum	I_{IN} = 1 mA_{p-p}	200	320	400	mV_{p-p}
PSRR	Power supply rejection ratio	f < 2 MHz		55		dB

(1) $C_{EXTERNAL}$= is the total capacitance comprising of the photodiode capacitance, board capacitance, and pad capacitance at the IN bondpad.

APPLICATION INFORMATION

Basic Application Circuit

Figure 3 shows the ONET2511TA being used as a receiver in a typical fiber optic application. The ONET2511TA converts the electrical current generated by the PIN or APD photodiode into a differential voltage output. The FILTER input provides a DC bias voltage for the photodiode that is low pass filtered by the combination of the internal 750-Ω resistor and internal capacitor. For additional power supply filtering, use an external capacitor C_{FILTER}. The RSSI output is used to mirror the photodiode output current and must be connected via a 10-kΩ resistor to GND or left open. Within the ONET2511TA, the OUT+ and OUT- pins are back-terminated with 50 Ω to VCC.

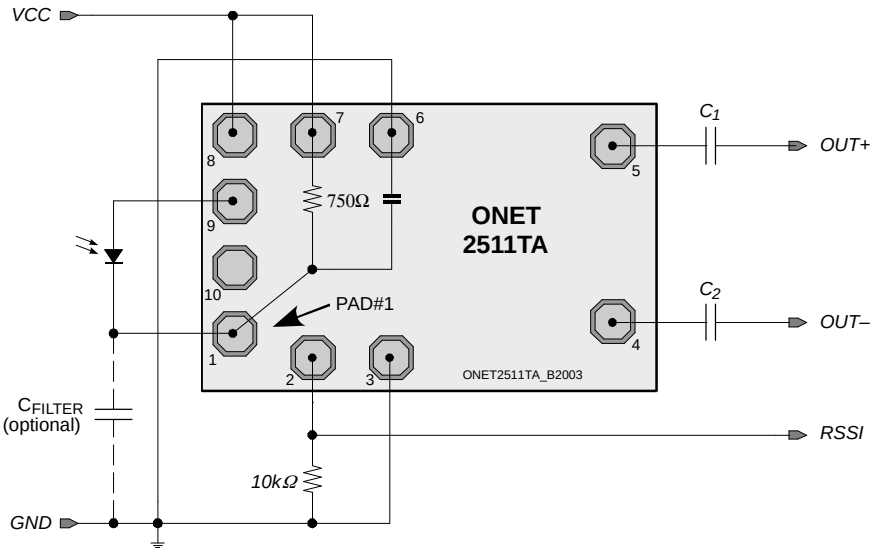

Figure 3. Basic Application Circuit

Board Layout

Careful attention to board layout parasitics and external components is necessary to achieve optimal performance with a high performance transimpedance amplifier like the ONET2511TA.

Recommendations that optimize performance include:

1. Minimize total capacitance on the IN pad by using a low capacitance photodiode and paying attention to stray capacitances. Place the photodiode close to the ONET2511TA die in order to minimize the bond wire length and thus the parasitic inductance.
2. The external filter capacitance C_{FILTER} may have an impact on the transfer function of the TIA and must be chosen with care based on the module implementation.
3. Use identical termination and symmetrical transmission lines at the differential output pins OUT+ and OUT-.
4. Use short bond wire connections for the supply terminals VCC and GND. Provide sufficient supply voltage filtering.

APPLICATION INFORMATION (continued)

CHIP DIMENSIONS AND PAD LOCATIONS

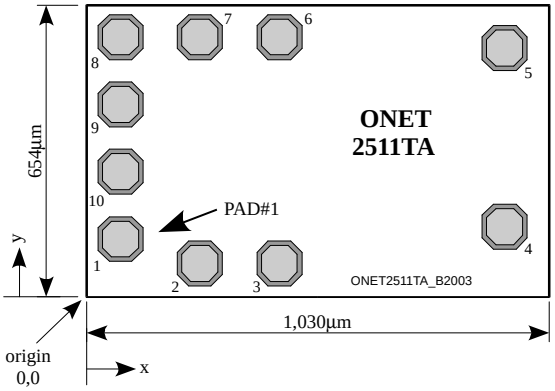

Figure 4. Chip Dimensions and Pad Locations

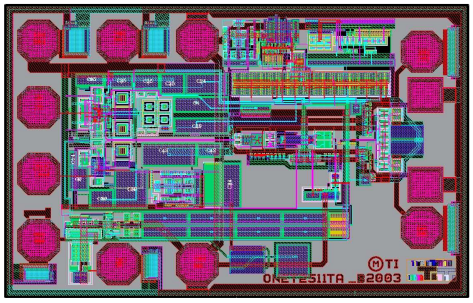

Figure 5. Chip Layout

Pad Locations and Description

PAD	LOWER LEFT COORDINATE		UPPER RIGHT COORDINATE		SYMBOL	TYPE	DESCRIPTION
	x [µm]	y [µm]	x [µm]	y [µm]			
1	30	84	115	169	FILTER	Analog	Bias voltage for photodiode
2	207	30	292	115	RSSI	Analog out	RSSI output voltage signal
3	384	30	469	115	GND	Supply	Circuit ground
4	886	112	971	197	OUT-	Analog out	Inverted data output
5	886	509	971	594	OUT+	Analog out	Non-inverted data output
6	384	534	469	619	GND	Supply	Circuit ground
7	207	534	292	619	VCC	Supply	+3.3 V ± 10% supply voltage
8	30	534	115	619	VCC	Supply	+3.3 V ± 10% supply voltage
9	30	384	115	469	IN	Analog in	Data input to TIA
10	30	234	115	319	NC		Not connected

TO46 Layout Example

An example for a suggested layout in a 5-pin TO46 ROSA is given in Figure 6 (top view).

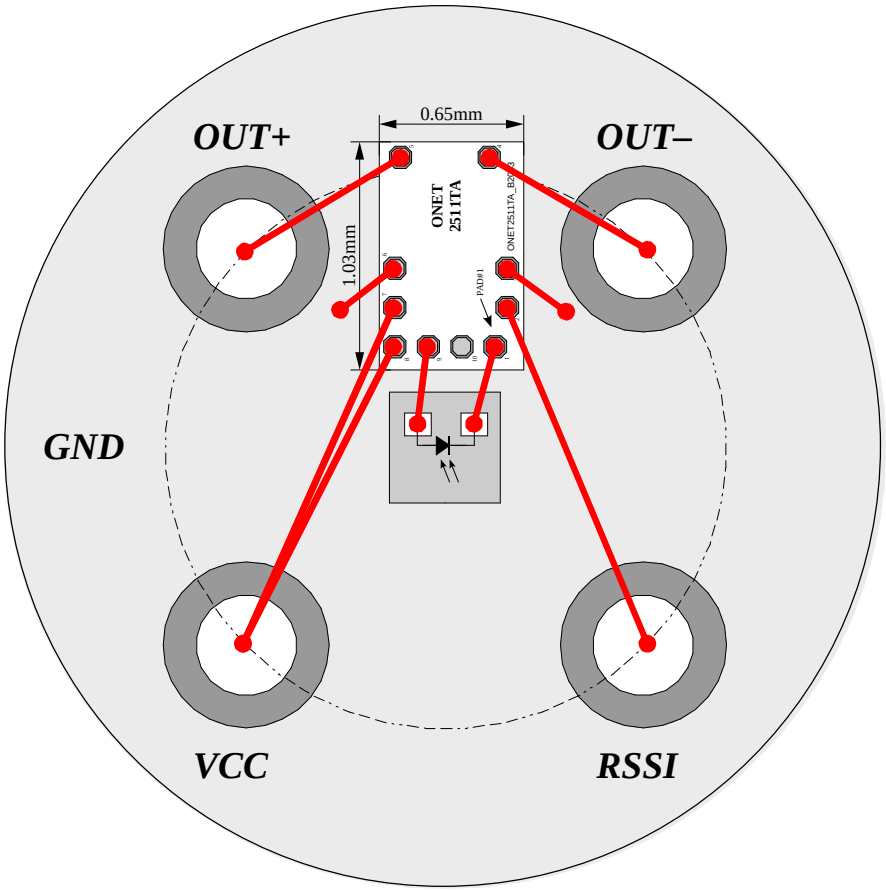

Figure 6. TO46 Layout Example Using the ONET2511TA

TYPICAL CHARACTERISTICS

V_{CC} = +3.3 V and T_A = +25°C (unless otherwise noted)

INPUT REFERRED NOISE vs AVERAGE INPUT CURRENT

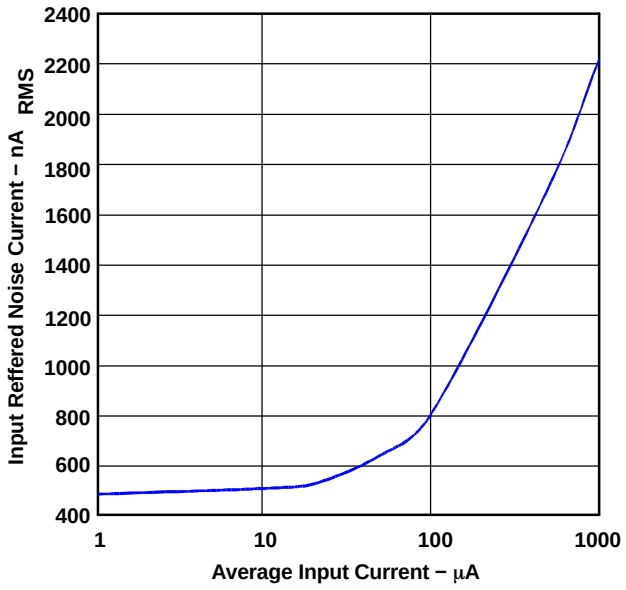

Figure 7.

INPUT REFERRED NOISE vs FREE-AIR TEMPERATURE

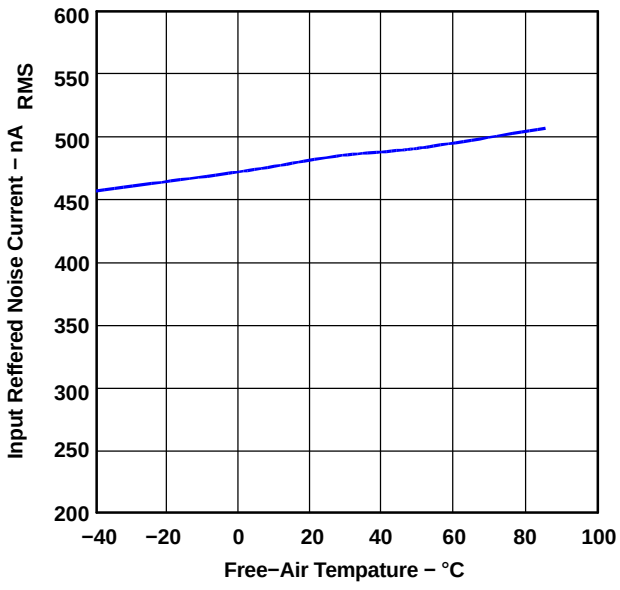

Figure 8.

DC TRANSFER CHARACTERISTIC (OFFSET CANCELLATION DISABLED)

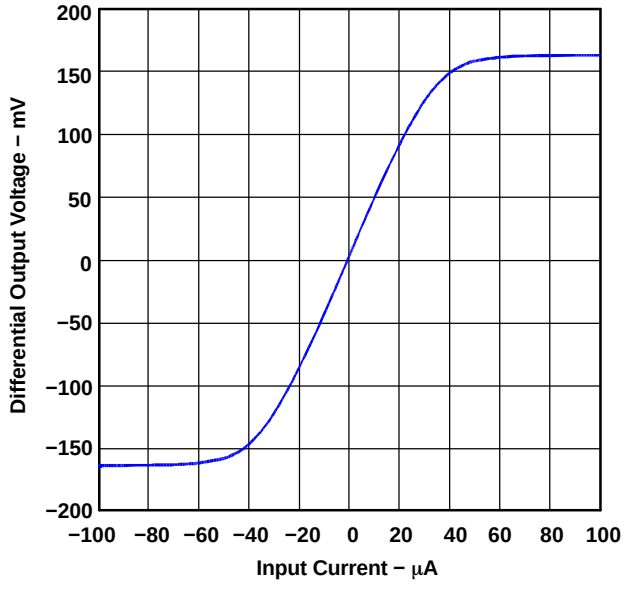

Figure 9.

TRANSIMPEDANCE vs FREE-AIR TEMPERATURE

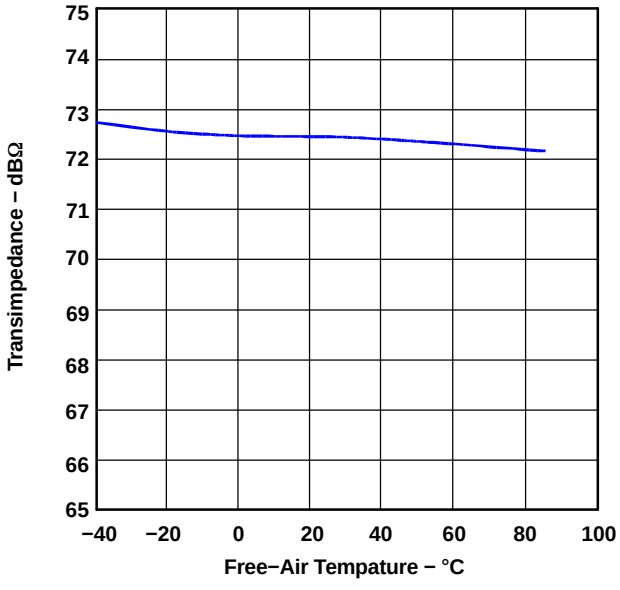

Figure 10.

TYPICAL CHARACTERISTICS (continued)

V_{CC} = +3.3 V and T_A = +25°C (unless otherwise noted)

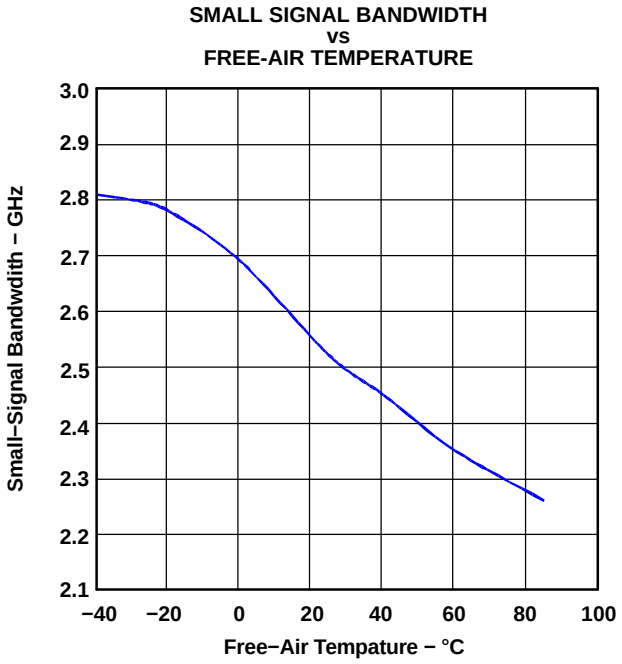

Figure 11.

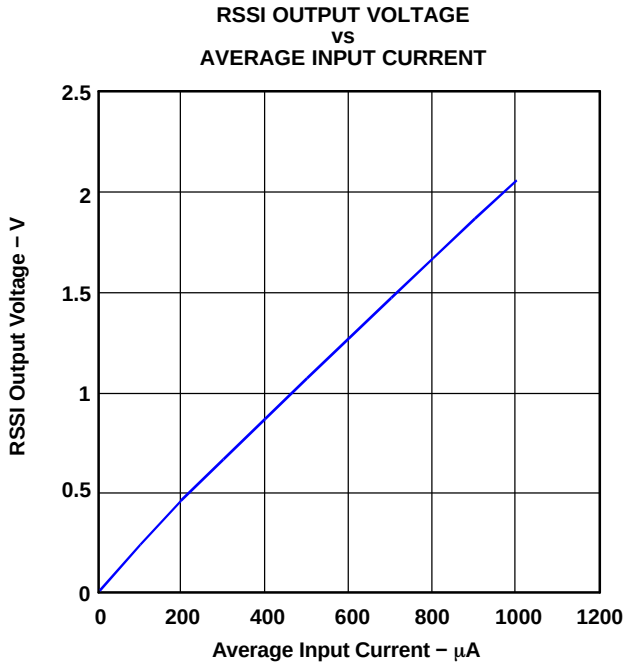

Figure 12.

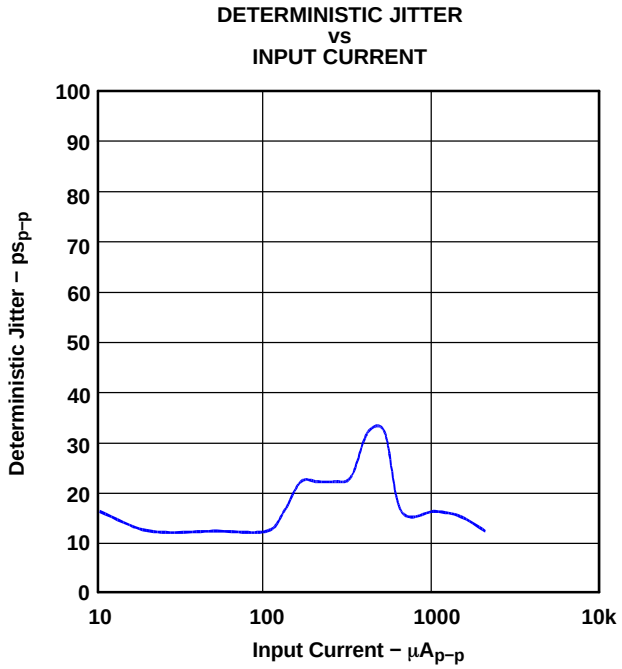

Figure 13.

TYPICAL CHARACTERISTICS (continued)

V_{CC} = +3.3 V and T_A = +25°C (unless otherwise noted)

OUTPUT EYE-DIAGRAM AT 2.5 GBPS and 20μA_{p-p} INPUT CURRENT USING A K28.5 PATTERN

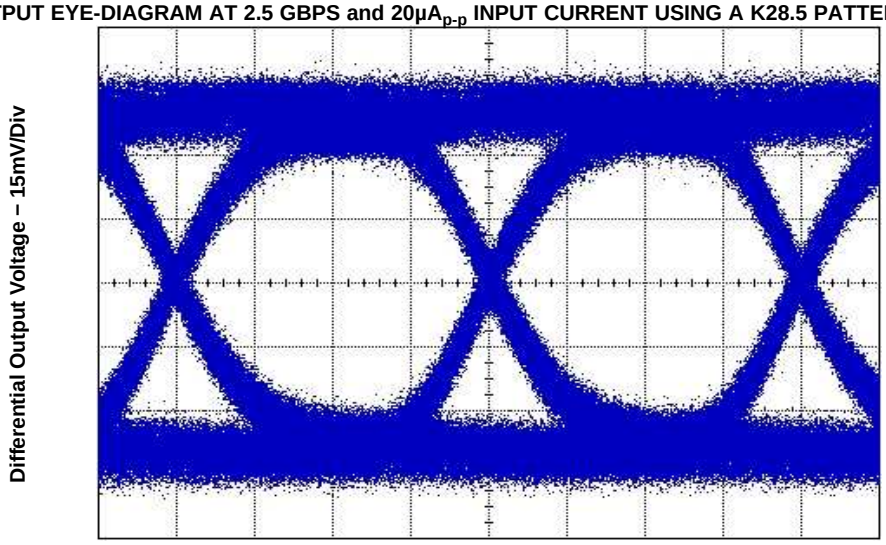

Figure 14.

OUTPUT EYE-DIAGRAM AT 2.5 GBPS and 2 mA_{p-p} INPUT CURRENT USING A K28.5 PATTERN

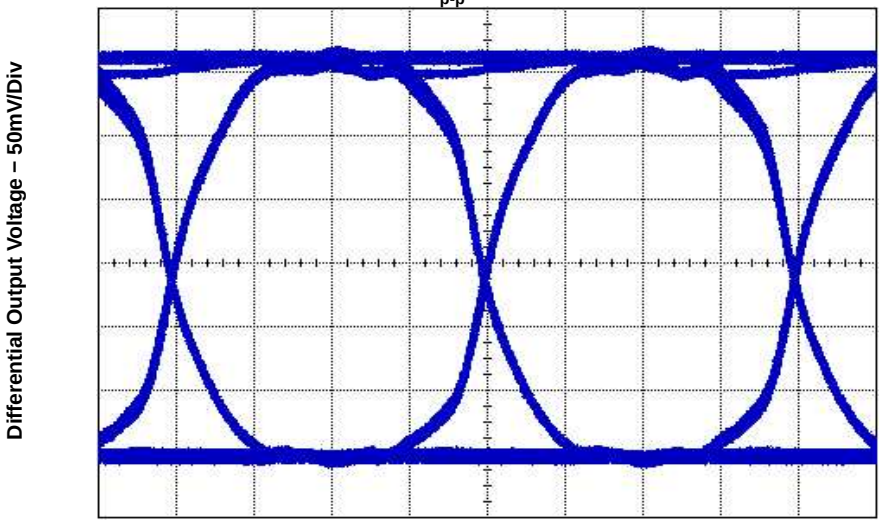

Figure 15.

PACKAGE OPTION ADDENDUM

12-Jan-2006

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ONET2511TAY	ACTIVE	XCEPT	Y	10	418	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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