Miniature, 2W, Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- Up To 89% Efficiency
- Thermal Protection
- Device-to-Device Synchronization
- SO-28 Power Density of 106W/in^3 (6.5W/cm^3)
- EN55022 Class B EMC Performance
- UL1950 Recognized Component
- JEDEC 14-Pin and SO-28 Packages

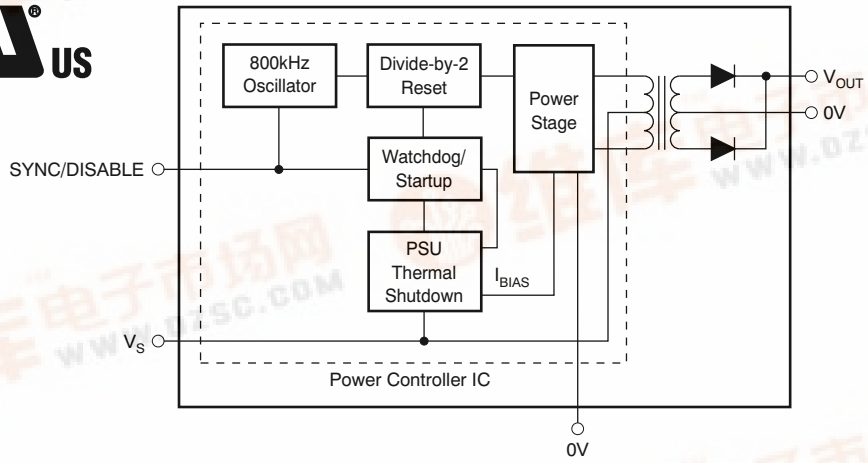
APPLICATIONS

- Point-of-Use Power Conversion
- Ground Loop Elimination
- Data Acquisition
- Industrial Control and Instrumentation
- Test Equipment

DESCRIPTION

The DCP02 series is a family of 2W, isolated, unregulated DC/DC converters. Requiring a minimum of external components and including on-chip device protection, the DCP02 series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly integrated package design results in highly reliable products with power densities of 79W/in^3 (4.8W/cm^3) for DIP-14, and 106W/in^3 (6.5W/cm^3) for SO-28. This combination of features and small size makes the DCP02 suitable for a wide range of applications.



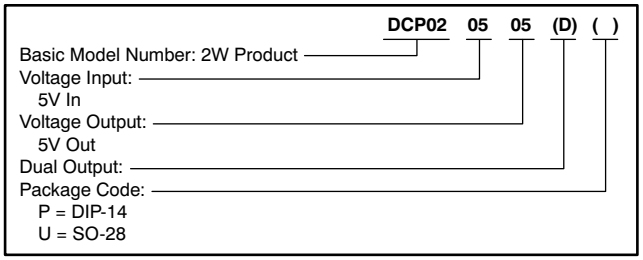
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

Supplemental Ordering Information



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		DCP02 Series	UNIT
Input Voltage	5V input models	7	V
	12V input models	15	V
	15V input models	18	V
	24V input models	29	V
Storage temperature range		–60 to +125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Power	100% full load		2		W
Ripple	O/P capacitor = 1µF, 50% load		20		mV_{PP}
INPUT					
Voltage range on V_S		–10		10	%
ISOLATION					
Voltage	1s Flash test	1			kVrms
	60s test, UL1950(1)	1			kVrms
LINE					
Regulation			1		%/1% of V_S
SWITCHING/SYNCHRONIZATION					
Oscillator frequency (f_{OSC})	Switching frequency = f_{OSC}/2		800		kHz
Sync input low		0		0.4	V
Sync input current	V_{SYNC} = +2V		75		µA
Disable time			2		µs
Capacitance loading on SYNC pin	External			10	pF
RELIABILITY					
Demonstrated	T_A = +55°C	75			FITS
THERMAL SHUTDOWN					
IC temperature at shutdown			+150		°C
Shutdown current			3		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C

(1) During UL1950 recognition tests only.

ELECTRICAL CHARACTERISTICS PER DEVICE

At T_A = +25°C, unless otherwise noted.

	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			LOAD REGULATION (%)		NO LOAD CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)
	V_S			V_{NOM}					I_Q		C_{ISO}
				75% LOAD(1)			10% TO 100% LOAD		0% LOAD	100% LOAD	V_{ISO} = 750Vrms
PRODUCT	MIN	TYP	MAX	MIN	TYP	MAX	TYP	MAX	TYP	TYP	TYP
DCP020503P, U	4.5	5	5.5	3.13	3.3	3.46	19	30	18	74	26
DCP020505P, U	4.5	5	5.5	4.75	5	5.25	14	20	18	80	22
DCP020507P, U	4.5	5	5.5	6.65	7	7.35	14	25	20	81	30
DCP020509P, U	4.5	5	5.5	8.55	9	9.45	12	20	23	82	31
DCP020515DP, U	4.5	5	5.5	±14.25	±15	±15.75	11	20	27	85	24
DCP021205P, U	10.8	12	13.2	4.75	5	5.25	7	15	14	83	33
DCP021212P, U	10.8	12	13.2	11.4	12	12.6	7	20	15	87	47
DCP021212DP, U	10.8	12	13.2	±11.4	±12	±12.6	6	20	16	88	35
DCP021215DP, U	10.8	12	13.2	±14.25	±15	±15.75	6	20	21	87	33
DCP021515P, U	13.5	15	16.5	14.25	15	15.75	6	20	15	88	42
DCP022405P	21.6	24	26.4	4.85	5	5.35	6	10	13	81	33
DCP022405U	21.6	24	26.4	4.75	5	5.25	10	15	13	81	33
DCP022405DP, U	21.6	24	26.4	±4.75	±5	+5.25	6	15	12	80	22
DCP022412DP, U	21.6	24	26.4	±11.4	±12	±12.6	4	16	19	83	29
DCP022415DP, U	21.6	24	26.4	±14.25	±15	±15.75	6	25	16	79	44
DCP022418DP, U	21.6	24	26.4	±17.1	±18	±18.9	9	25	20	84	32

(1) 100% load current = 2W/V_{NOM} typ.

DEVICE INFORMATION

NVA PACKAGE
DIP-14 (Single-DIP)
(Top View)

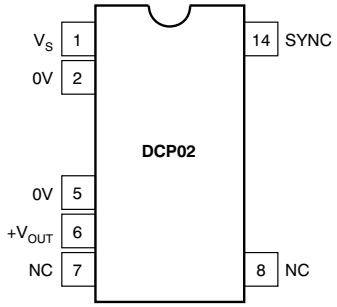


Table 1. Pin Description (Single-DIP)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
NC	7, 8	Not connected
SYNC	14	Synchronization pin

DVB PACKAGE
SO-28 (Single-SO)
(Top View)

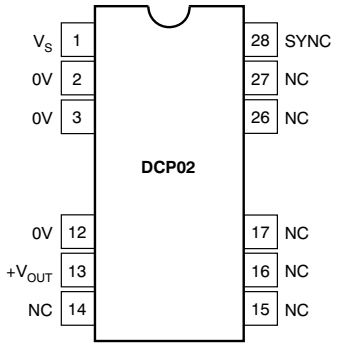


Table 2. TERMINAL FUNCTIONS (Single-SO)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	3	Input side common
0V	12	Output side common
$+V_{OUT}$	13	+Voltage out
NC	14, 15, 16, 17, 26, 27	Not connected
SYNC	28	Synchronization pin

NVA PACKAGE
DIP-14 (Dual-DIP)
(Top View)

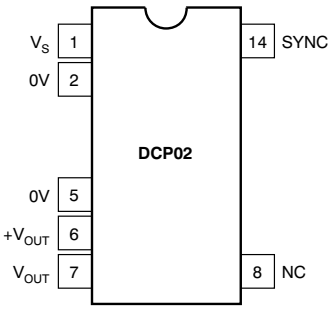


Table 3. TERMINAL FUNCTIONS (Dual-DIP)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
$-V_{OUT}$	7	–Voltage out
NC	8	Not connected
SYNC	14	Synchronization pin

DVB PACKAGE
SO-28 (Dual-SO)
(Top View)

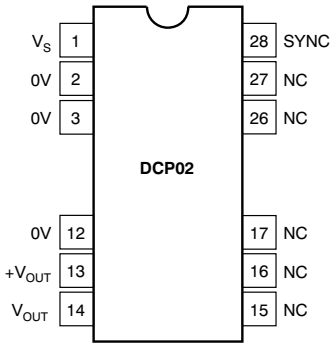


Table 4. TERMINAL FUNCTIONS (Dual-SO)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	3	Input side common
0V	12	Output side common
$+V_{OUT}$	13	+Voltage out
$-V_{OUT}$	14	–Voltage out
NC	15, 16, 17, 26, 27	Not connected
SYNC	28	Synchronization pin

TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

DCP020505P
CONDUCTED EMISSIONS (500mA Load)

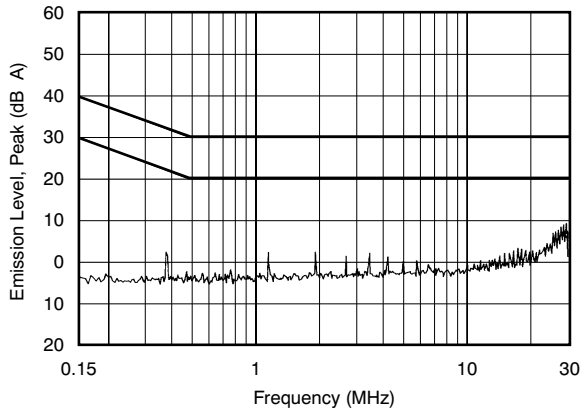


Figure 1.

DCP020505P
V_{OUT} vs TEMPERATURE (75% Load)

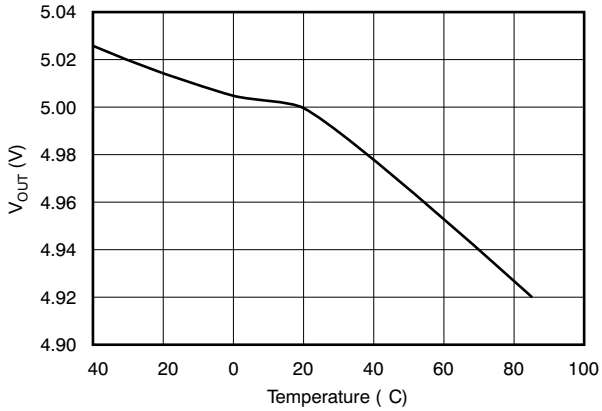


Figure 2.

DCP021205P
V_{OUT} vs LOAD

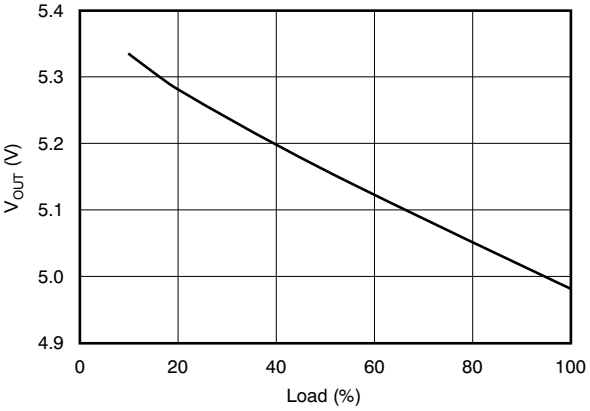


Figure 3.

DCP021205P
POWER OUT vs TEMPERATURE (400mA Load)

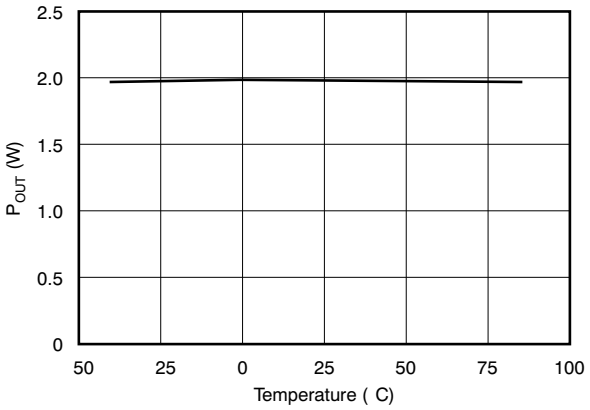


Figure 4.

DCP0212
EFFICIENCY vs LOAD

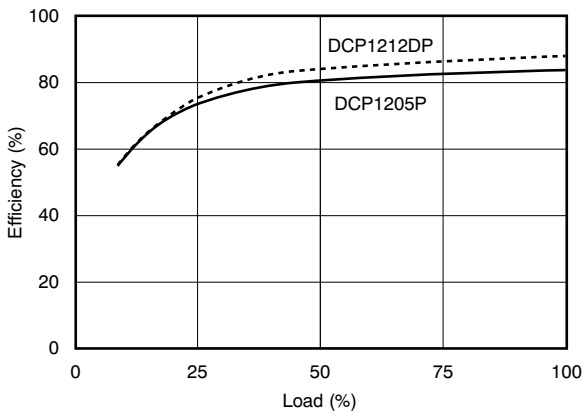


Figure 5.

DCP020505P
OUTPUT AC RIPPLE (20MHz Band)

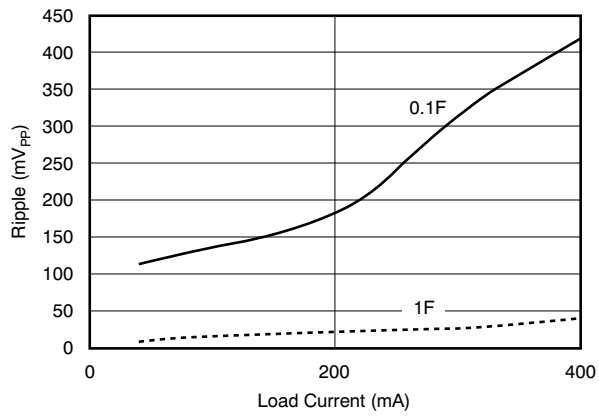


Figure 6.

FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP02 offers up to 2W of unregulated output power from a 5V, 12V, 15V, or 24V input source with a typical efficiency of up to 89%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design uses an advanced BiCMOS/DMOS process.

POWER STAGE

The DCP02 uses a push-pull, center-tapped topology switching at 400kHz (divide-by-2 from an 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP02 circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the SYNC pin low. The output pins will be tri-stated. This will occur in 2µs.

THERMAL SHUTDOWN

The DCP02 is protected by a thermal-shutdown circuit. If the on-chip temperature exceeds +150°C, the device will shut down. Once the temperature falls below +150°C, normal operation will resume.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This is due to the small variations in switching frequencies between the DC/DC converters.

The DCP02 overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, taking care to minimize the capacitance of tracking. Stray capacitance (> 10pF) will have the effect of reducing the switching frequency, or even stopping the oscillator circuit. It is also recommended that power and ground lines be star-connected.

It should be noted that if synchronized devices are used at start up, all devices will draw maximum current simultaneously. This can cause the input voltage to dip, and if it dips below the minimum input voltage (4.5V), the devices may not start up. A 2.2µF capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the SYNC pins be driven by an external device. Details are contained in Application Report SBAA035, *External Synchronization of the DCP01/02 Series of DC/DC Converters*, available for download from www.ti.com.

CONSTRUCTION

The basic construction of the DCP02 is the same as standard ICs. There is no substrate within the molded package. The DCP02 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Since there is no solder within the package, the DCP02 does not require any special printed circuit board (PCB) assembly processing. This results in an isolated DC/DC converter with inherently high reliability.

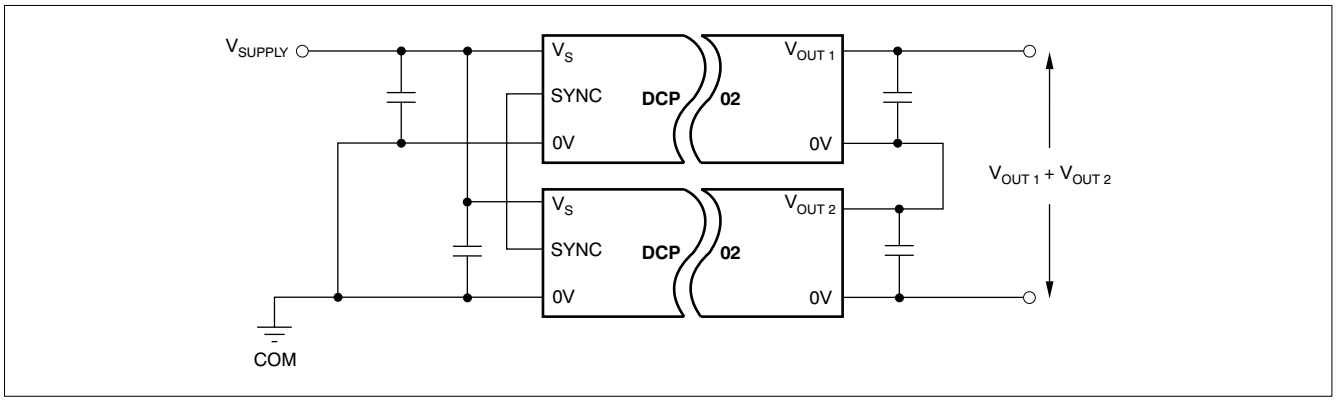


Figure 7. Connecting the DCP02 in Series

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP02 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCP02 will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2µs. Removal of the pull down will cause the DCP02 to be enabled.

Capacitive loading on the SYNC pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that a 1µF capacitor be used on V_{OUT}. Dual outputs should both be decoupled to pin 5. A 2.2µF capacitor on the input is recommended.

Connecting the DCP02 in Series

Multiple DCP02 isolated 2W DC/DC converters can be connected in series to provide nonstandard voltage rails. This is possible by using the floating outputs provided by the galvanic isolation of the DCP02.

Connect the positive V_{OUT} from one DCP02 to the negative V_{OUT} (0V) of another (see Figure 7). If the SYNC pins are tied together, the self-synchronization feature of the DCP02 will prevent beat frequencies on the voltage rails. The SYNC feature of the DCP02 allows easy series connection without external filtering, thus minimizing cost.

The outputs on the dual-output DCP02 versions can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 8. For example, a dual 15V DCP022415D could be connected to provide a 30V rail.

Connecting the DCP02 in Parallel

If the output power from one DCP02 is not sufficient, it is possible to parallel the outputs of multiple DCP02s, as shown in Figure 9. Again, the SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

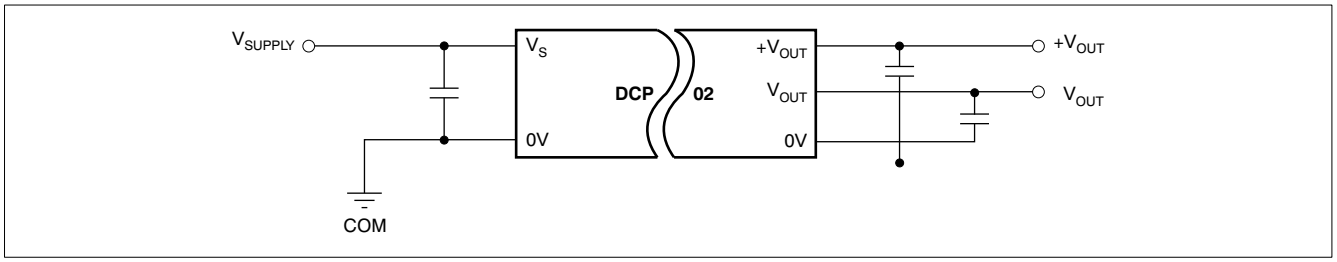


Figure 8. Connecting Dual Outputs in Series

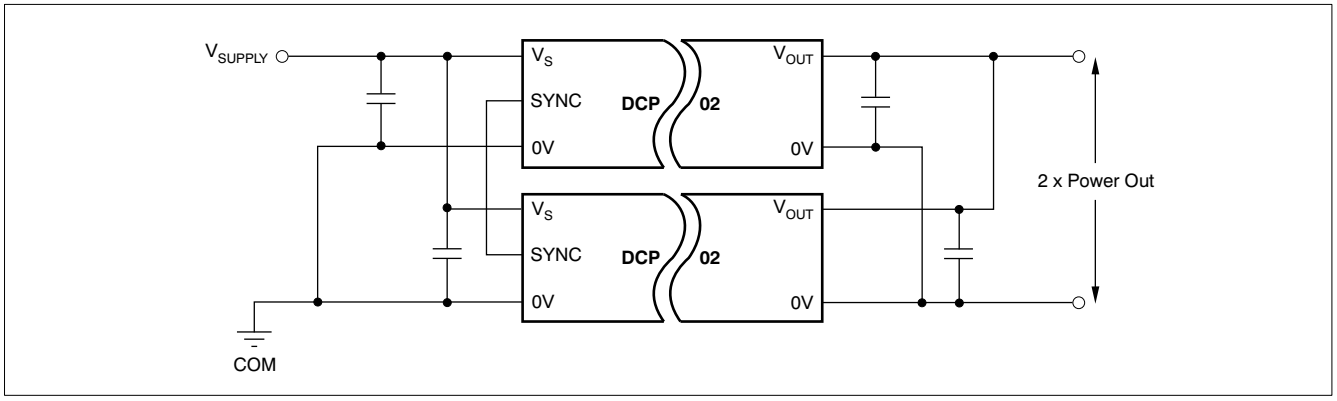


Figure 9. Connecting Multiple DCP02s in Parallel

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCP020503P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP020503U	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP020503U/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP020505P	ACTIVE	PDIP	NVA	7	25	TBD	CU SNPB	N / A for Pkg Type
DCP020505U	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP020505U/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP020507P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP020507U	ACTIVE	SOP	DVB	12	28	TBD	CU SNPB	Level-3-240C-168 HR
DCP020507U/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU SNPB	Level-3-240C-168 HR
DCP020509P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP020509U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP020515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP020515DU	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP020515DU/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP021205P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCP021205PE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCP021205U	ACTIVE	SOP	DVB	12	28	TBD	Call TI	Level-3-240C-168 HR
DCP021205U/1K	ACTIVE	SOP	DVB	12	1000	TBD	Call TI	Level-3-240C-168 HR
DCP021212DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP021212DU	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP021212DU/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP021212P	ACTIVE	PDIP	NVA	7	25	TBD	CU NIPDAU	N / A for Pkg Type
DCP021212U	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP021212U/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP021215DP	ACTIVE	PDIP	NVA	7	25	TBD	Call TI	Call TI
DCP021515P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCP021515PE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCP021515U	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP021515U/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP022405DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP022405DU	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP022405DU/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP022405P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAULATE	N / A for Pkg Type
DCP022405U	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCP022405U/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP022412DP	ACTIVE	PDIP	NVA	7	25	TBD	Call TI	Call TI
DCP022415DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP022415DU	ACTIVE	SOP	DVB	12	28	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP022415DU/1K	ACTIVE	SOP	DVB	12	1000	TBD	CU NIPDAU	Level-3-240C-168 HR
DCP022418DP	ACTIVE	PDIP	NVA	7	25	TBD	Call TI	Call TI

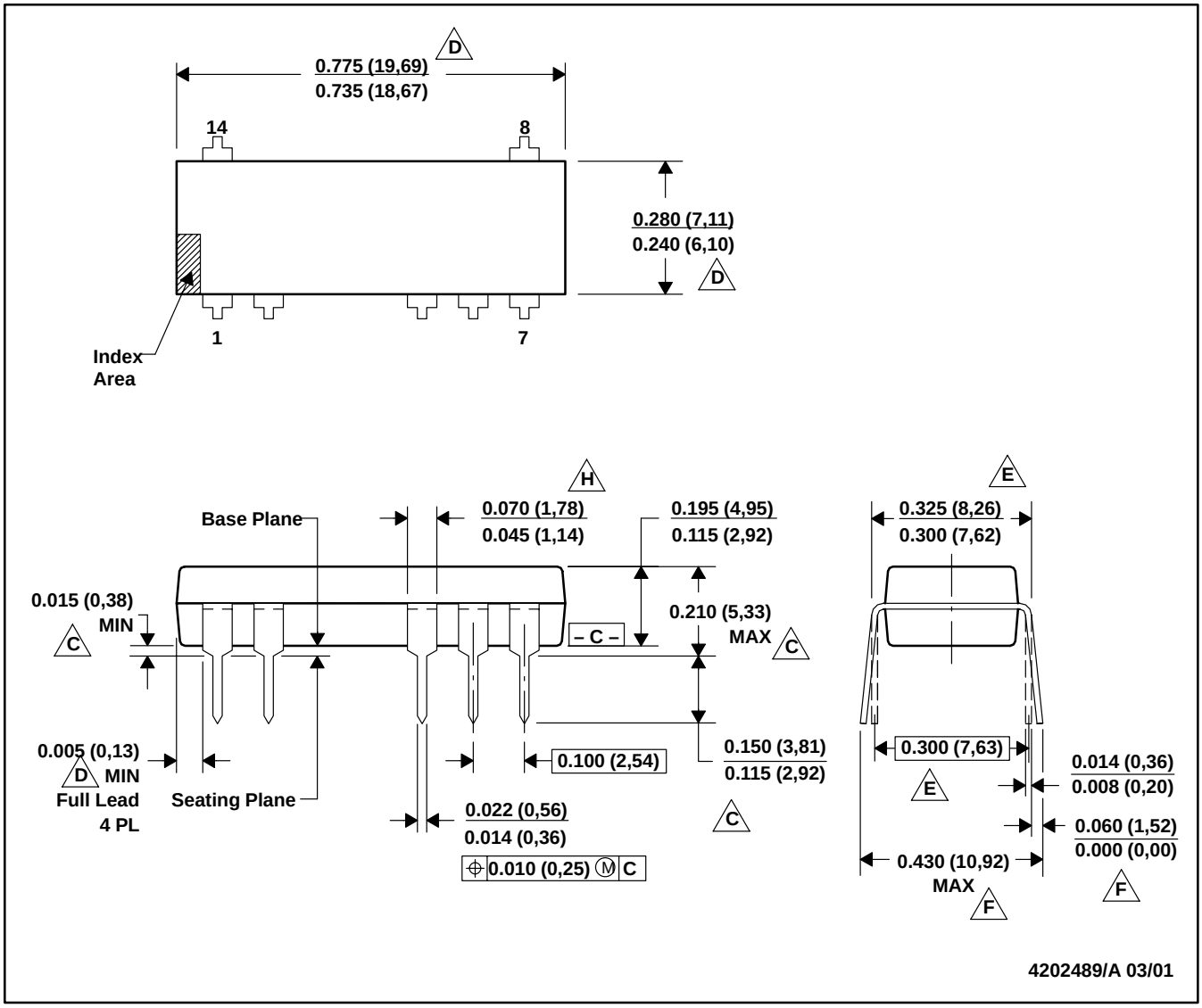
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPDI058 – APRIL 2001

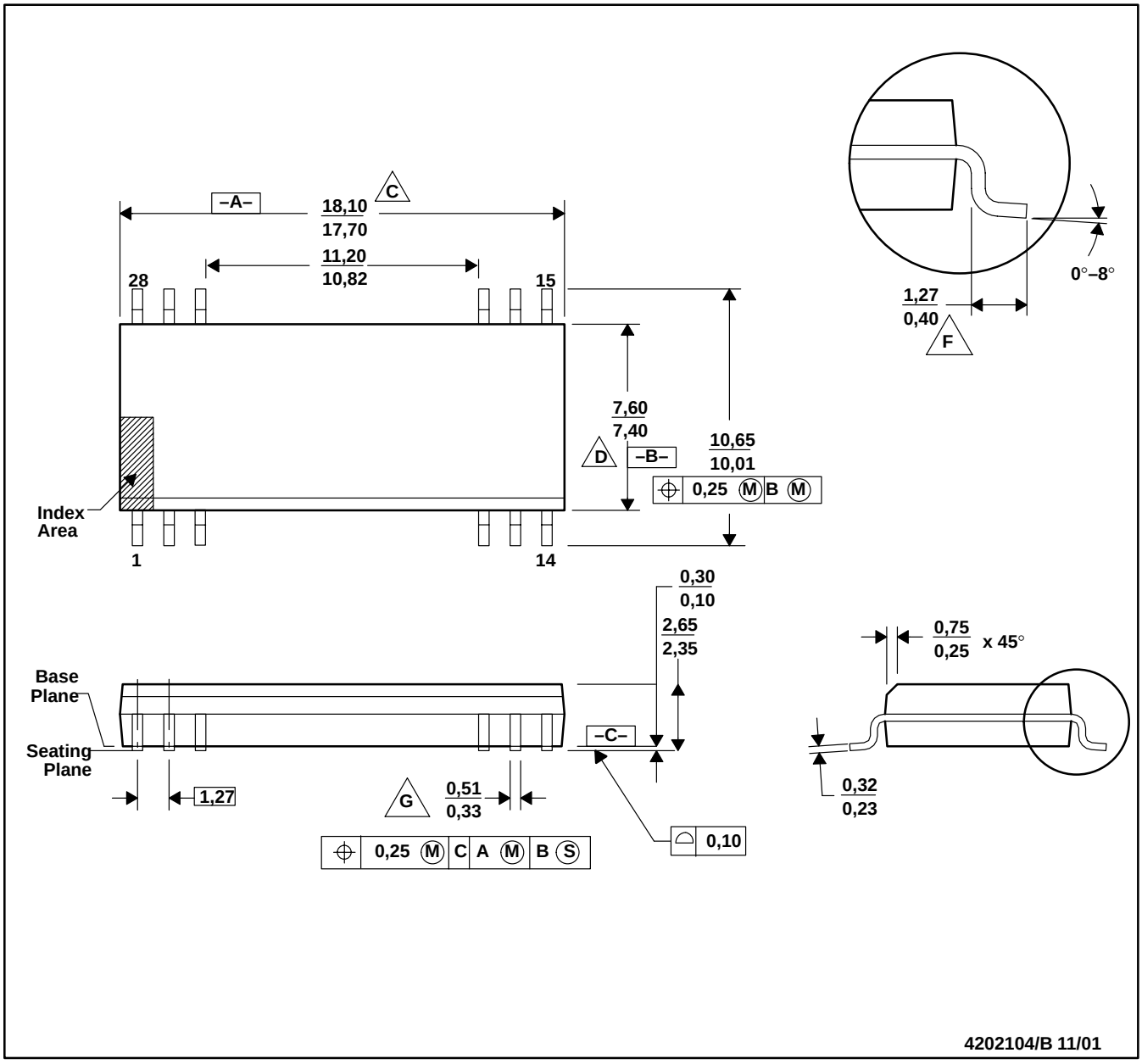
NVA (R-PDIP-T7/14) **PLASTIC DUAL-IN-LINE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. Pointed or rounded lead tips are preferred to ease insertion.
H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
I. Distance between leads including dambar protrusions to be 0.005 (0,13) minumum.
J. A visual index feature must be located within the cross–hatched area.
K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
L. Falls within JEDEC MS-001-AA.

MPDS106A – AUGUST 2001 – REVISED NOVEMBER 2001

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

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