16-Bit, Parallel Input Multiplying Digital-to-Analog Converter

FEATURES

- ±0.5 LSB DNL
- ±1 LSB INL
- 16-Bit Monotonic
- Low Noise: 12 nV/√Hz
- Low Power: IDD = 2 μA
- Analog Power Supply: +2.7 V to +5.5 V
- 2 mA Full-Scale Current: ±20%, with V_{REF} = 10 V
- Settling Time: 0.5 μs
- 4-Quadrant Multiplying Reference
- Reference Bandwidth: 10 MHz
- Reference Input: ±10 V
- Reference Dynamics: –105 THD
- SSOP-28 Package
- Industry-Standard Pin Configuration

APPLICATIONS

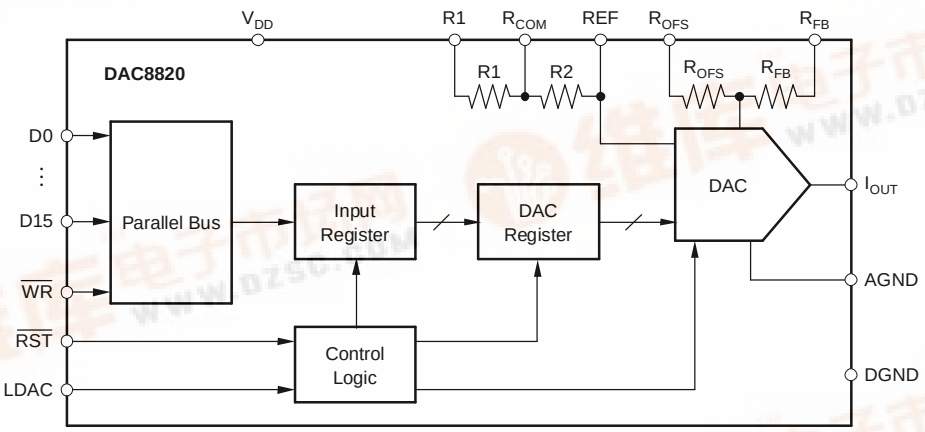
- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

DESCRIPTION

The DAC8820 multiplying digital-to-analog converter (DAC) is designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external, voltage-to-current (I/V) precision amplifier.

A parallel interface offers high-speed communications. The DAC8820 is packaged in a space-saving SSOP-28 package and has an industry-standard pinout.



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8820IB	±2	±1	DB-28 (SSOP)	–40°C to +85°C	TBD	DAC8820IBDB	Tubes, 50
					TBD	DAC8820IBDBR	Tape and Reel, 2500
DAC8820IC	±1	±1	DB-28 (SSOP)	–40°C to +85°C	TBD	DAC8820ICDB	Tubes, 50
					TBD	DAC8820ICDBR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		DAC8820	UNIT
V_{DD} to GND		–0.5 to +7	V
Digital input voltage to GND		–0.5 to +V_{DD} + 0.5	V
V (I_{OUT}) to GND		–0.5 to +V_{DD} + 0.5	V
Operating temperature range		–40 to +105	°C
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+125	°C
Power dissipation		(T_J max – T_A) / $R_{\theta JA}$	W
Thermal impedance, $R_{\theta JA}$		55	°C/W
Lead temperature, soldering	Vapor phase (60s)	215	°C
Lead temperature, soldering	Infrared (15s)	220	°C
ESD rating:			
Human Body Model (HBM)		2000	V
Charged Device Model (CDM)		1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85°C, V_{DD} = +2.7 V to +5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, and T_A = full operating temperature, unless otherwise noted.

PARAMETER		CONDITIONS	DAC8820 MIN	DAC8820 TYP	DAC8820 MAX	UNITS
STATIC PERFORMANCE(1)						
Resolution			16			Bits
Relative accuracy		DAC8820B			±2	LSB
Relative accuracy		DAC8820C			±1	LSB
Differential nonlinearity					±1	LSB
Output leakage current		Data = 0000h, T_A = +25°C			5	nA
Output leakage current		Data = 0000h, $T_A = T_{MAX}$			10	nA
Full-scale gain error		Unipolar, data = FFFFh		2	±16	LSB
		Bipolar, data = FFFFh		2	±16	LSB
Full-scale temperature coefficient				1	2	ppm/°C
PSRR		Power-supply rejection ratio; V_{DD} = 5V ± 10%		±0.2	±2.0	LSB/V
OUTPUT CHARACTERISTICS(2)						
Output current				2		mA
Output capacitance		Code dependent		50		pF
REFERENCE INPUT						
V_{REF} Range			–15		15	V
R_{REF}		Input resistance (unipolar)	4.5	6	10	kΩ
Input capacitance				5		pF
R1/R2		R1/R2 resistance (bipolar)	9	12	10	kΩ
R_{OFS}, R_{FB}		Feedback and offset resistance	9	12	20	kΩ
LOGIC INPUTS AND OUTPUT(2)						
Input low voltage	V_{IL}	V_{DD} = +2.7 V			0.6	V
	V_{IL}	V_{DD} = +5 V			0.8	V
Input high voltage	V_{IH}	V_{DD} = +2.7 V	2.1			V
	V_{IH}	V_{DD} = +5 V	2.4			V
Input leakage current	I_{IL}			0.001	1	µA
Input capacitance	C_{IL}				8	pF
INTERFACE TIMING						
	t_{DS}	Data to $\overline{WR}$ setup time	25			ns
	t_{DH}	Data to $\overline{WR}$ hold time	0			ns
	t_{WR}	$\overline{WR}$ pulse width	25			ns
	t_{LDAC}	LDAC pulse width	25			ns
Data setup time	t_{RST}	$\overline{RST}$ pulse width	25			ns
Data hold time	t_{LWD}	$\overline{WR}$ to LDAC delay time	0			ns
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
I_{DD} (normal operation)		Logic inputs = 0 V			5	µA
V_{DD} = +4.5 V to +5.5 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		3	5	µA
V_{DD} = +2.7 V to +3.6 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		1	2.5	µA

(1) Linearity calculated using a reduced code range of 48 to 4047; output unloaded.
(2) Specified by design and characterization; not production tested.

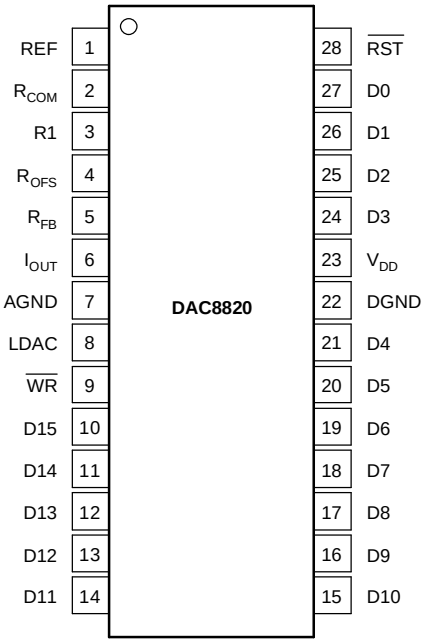
PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to +85°C, V_{DD} = +2.7 V to +5.5 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, and T_A = full operating temperature, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8820			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS					
Output current settling time			0.5		µs
Reference multiplying BW	V_{REF} = 5 V_{PP}, Data = FFFFh		10		MHz
DAC glitch impulse	V_{REF} = 0 V to 10 V, Data = 7FFFh to 8000h to 7FFFh		2		nV – s
Feedthrough error V_{OUT}/V_{REF}	Data = 0000h, V_{REF} = 100 kHz		–70		dB
Digital feedthrough			2		nV – s
Total harmonic distortion			–105		dB
Output spot noise voltage			12		nV/√Hz

PIN ASSIGNMENTS



PIN #	NAME	DESCRIPTION
2	R_{COM}	Center tap of two 4-quadrant resistors (R1 and R2).
3	R1	4-quadrant resistor (R1).
4	R_{OFS}	Bipolar offset resistor
5	R_{FB}	Internal matching feedback resistor
6	I_{OUT}	DAC current output
7	AGND	Analog ground
8	LDAC	Digital input load DAC control. When LDAC is high, data is loaded from input register into a DAC register, updating the DAC output.
9	$\overline{WR}$	Write control digital input. Active low. When $\overline{WR}$ is taken to logic low, data is loaded from the digital input pins (D0–D15) into a16-bit input register.
10–21	D15–D4	Digital input data bits. D15 is MSB.
22	DGND	Digital ground
23	V_{DD}	Positive power supply
24–27	D3–D0	Digital Input data bits. D0 is LSB.
28	$\overline{RST}$	Reset. Active low. When $\overline{RST}$ is taken to logic low, the DAC output and all internal registers are set to zero code for the DAC8820.

TERMINAL FUNCTIONS

PIN #	NAME	DESCRIPTION
1	REF	Reference input and 4-quadrant Resistor (R2).

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At T_A = +25°C and $+V_{DD}$ = +5 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 6.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C and $+V_{DD}$ = +5 V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

Figure 7.

REFERENCE MULTIPLYING BANDWIDTH

Figure 8.

DAC GLITCH

Figure 9.

DAC SETTLING TIME

Figure 10.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V

At T_A = +25°C and $+V_{DD}$ = +2.7 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 12.

LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 13.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 14.

LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 15.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Figure 16.

PRODUCT PREVIEW

THEORY OF OPERATION

The DAC8820 is a multiplying, single-channel current output, 16-bit DAC. The architecture, illustrated in Figure 17, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or to the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V_{REF}) that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 6 kΩ ± 25%. The external reference voltage can vary in a range of –15 V to +15 V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter op amp and the DAC8820 R_{FB} resistor, an output voltage range of $–V_{REF}$ to $+V_{REF}$ can be generated.

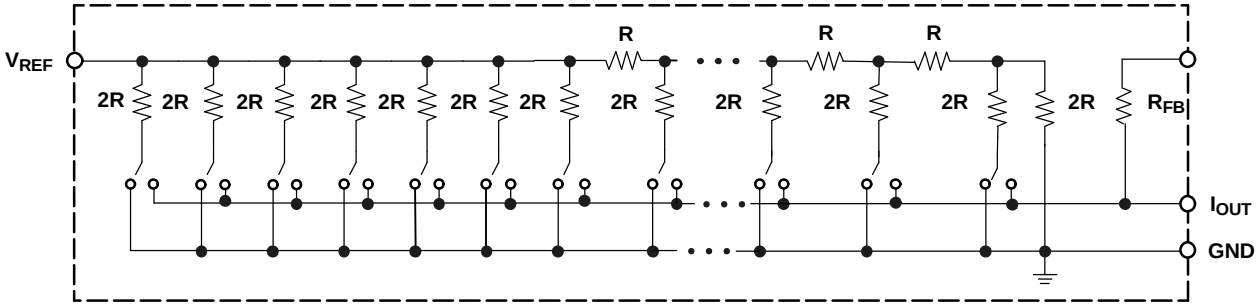


Figure 17. Equivalent R-2R DAC Circuit

When using an external I/V converter op amp and the DAC8820 R_{FB} resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{65536} \quad (1)$$

Each DAC code determines the 2R-leg switch position to either GND or I_{OUT}. The external I/V converter op amp noise gain will also change because the DAC output impedance (as seen looking into the I_{OUT} terminal) changes versus code. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8820 because of offset modulation versus DAC code. For best linearity performance of the DAC8820, an op amp (OPA277) is recommended, as shown in Figure 18. This circuit allows V_{REF} to swing from –15 V to +15 V.

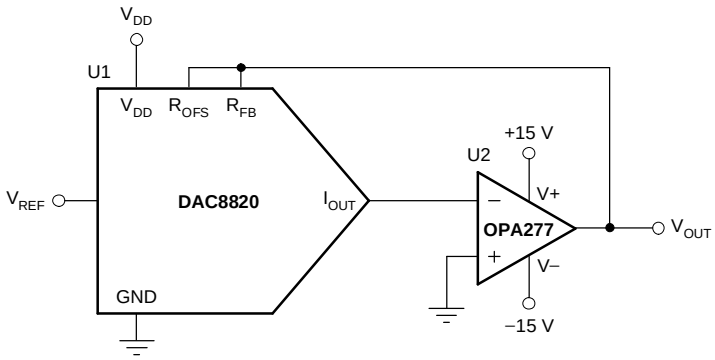


Figure 18. Voltage Output Configuration

PRODUCT PREVIEW

THEORY OF OPERATION (continued)

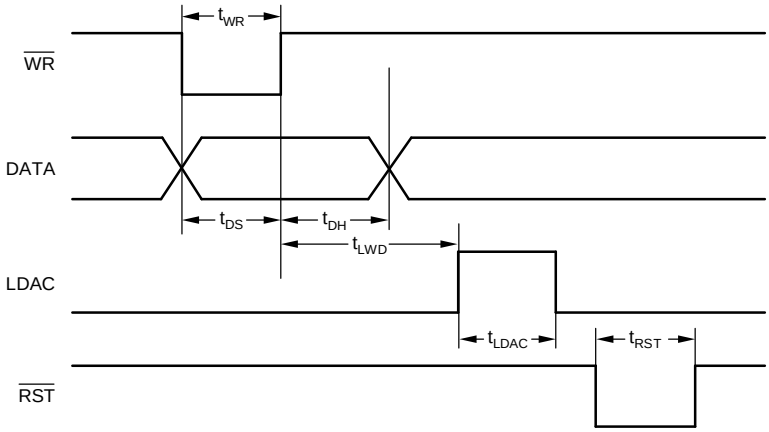


Figure 19. DAC8820 Timing Diagram

Table 1. Function of Control Inputs

CONTROL INPUTS			REGISTER OPERATION
$\overline{RST}$	$\overline{WR}$	LDAC	
0	X	X	Asynchronous operation. Reset the input and DAC register to a predetermined value. The DAC8820 is reset to all 0s.
1	0	0	Load the input register with all 16 data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC register are transparent.
1			LDAC and $\overline{WR}$ are tied together and programmed as a pulse. The 16 data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

PRODUCT PREVIEW

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage (V/I) design, as shown in Figure 20, the DAC8820 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and laid out according to correct printed circuit board (PCB) layout design. For each code change there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, a compensation capacitor C1 (4 pF to 20 pF, typ) can be added to the design for circuit stability, as shown in Figure 20.

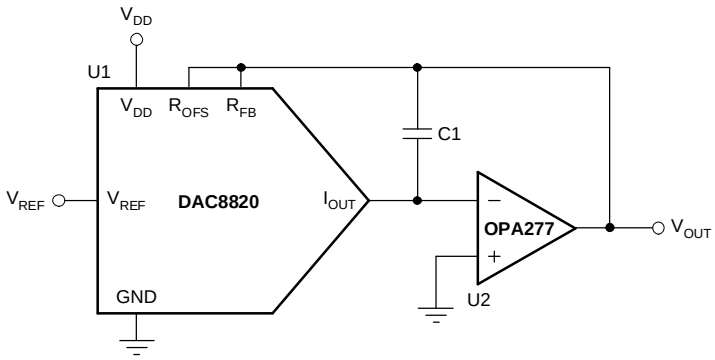


Figure 20. Gain Peaking Prevention Circuit With Compensation Capacitor

Bipolar Output Circuit

The DAC8820, as a 4-quadrant multiplying DAC, can be used to generate a bipolar output. The polarity of the full-scale output (I_{OUT}) is the inverse of the input reference voltage at V_{REF}.

Using a dual op amp, such as the OPA2277, full 4-quadrant operation can be achieved with minimal components. Figure 21 demonstrates a ±15 V_{OUT} circuit with a fixed +15 V reference.

$$V_{OUT} = \left(\frac{D}{32,768} - 1\right) \times V_{REF} \quad (2)$$

External resistance mismatching is the significant error in Figure 21.

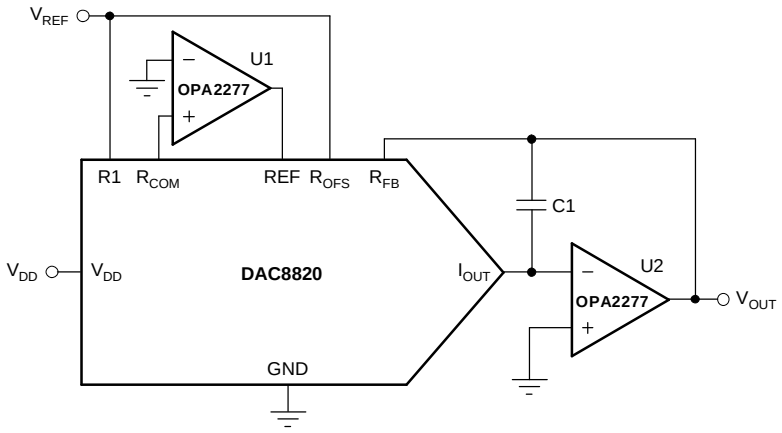


Figure 21. Bipolar Output Circuit

Programmable Current Source Circuit

A DAC8820 can be integrated into the circuit in Figure 22 to implement an improved Howland current pump for precise V/I conversions. Bidirectional current flow and high-voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L = \frac{(R2 + R3) \,/\, R1}{R3} \times V_{REF} \times D \quad (3)$$

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ±20 mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor (C1) in the circuit is not suggested as a result of the change in the output impedance (Z_O), according to Equation 4:

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (4)$$

As shown in Equation 4, Z_O with matched resistors is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

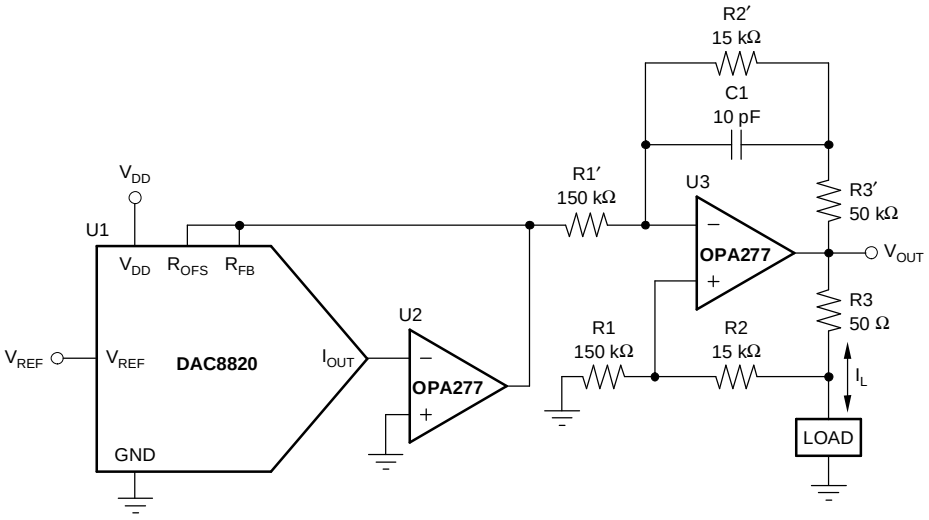


Figure 22. Programmable Bidirectional Current Source Circuit

Cross-Reference

The DAC8820 has an industry-standard pinout. Table 2 provides the cross-reference information.

Table 2. Cross-Reference

PRODUCT	BIT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8820BIDB	16	±2	±1	–40°C to +85°C	SSOP-28	SSOP-28	LTC1597BIG
DAC8820CIDB	16	±1	±1	–40°C to +85°C	SSOP-28	SSOP-28	LTC1597AIG

PRODUCT PREVIEW

PACKAGE OPTION ADDENDUM

5-Oct-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8820IBDB	PREVIEW	SSOP	DB	28	50	TBD	Call TI	Call TI
DAC8820IBDBR	PREVIEW	SSOP	DB	28	2000	TBD	Call TI	Call TI
DAC8820ICDB	PREVIEW	SSOP	DB	28	50	TBD	Call TI	Call TI
DAC8820ICDBR	PREVIEW	SSOP	DB	28	2000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

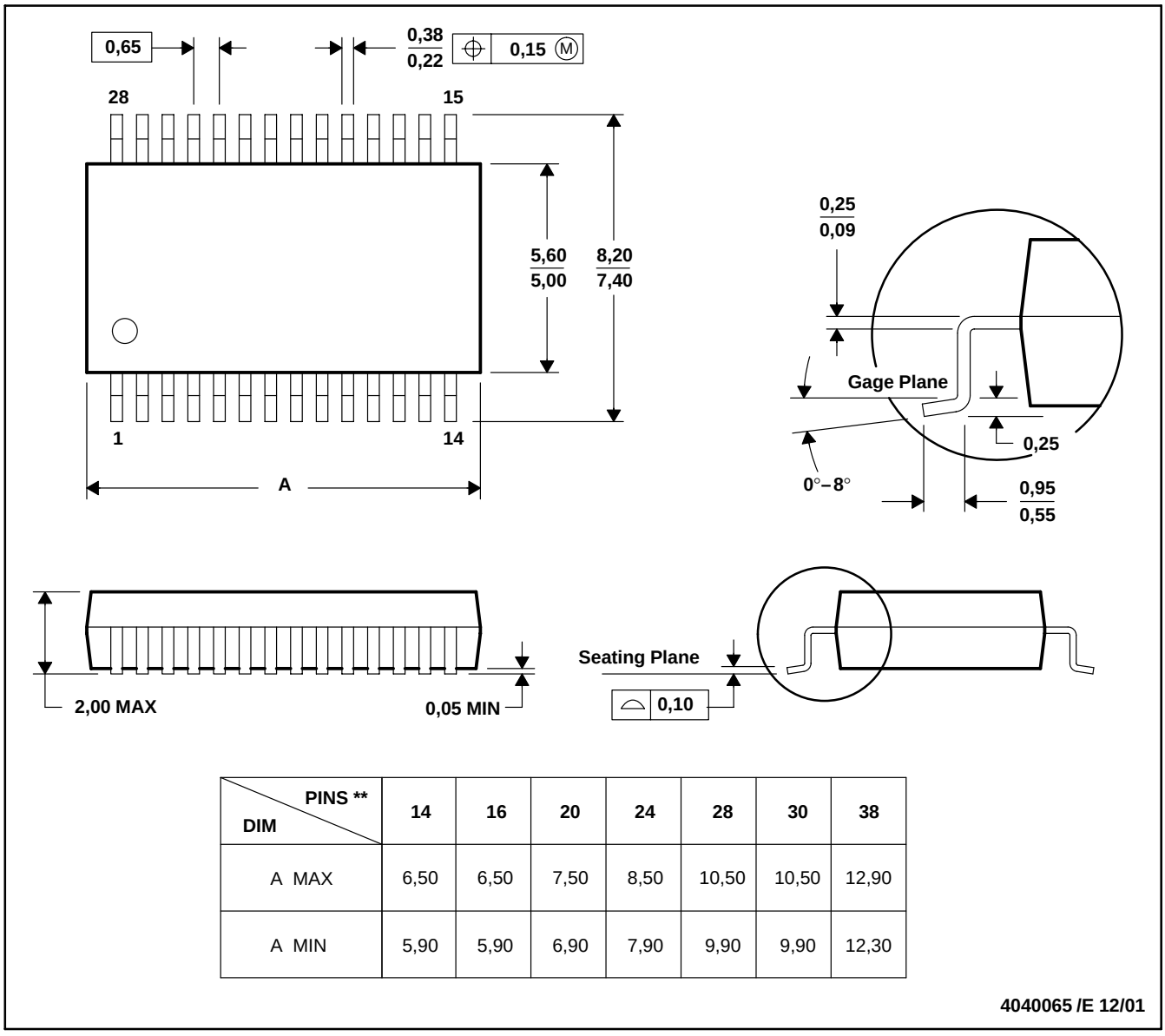
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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