捷多邦,专业PCB打**GY54F@T245T。GY**74FCT245T 8-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

SCCS018B - MAY 1994 - REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible
 With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT245T
 - 48-mA Output Sink Current
 12-mA Output Source Current
- CY74FCT245T
 - 64-mA Output Sink Current
 32-mA Output Source Current
- 3-State Outputs

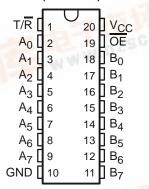
description

The 'FCT245T devices contain eight noninverting bidirectional buffers with 3-state outputs and are intended for bus-oriented applications.

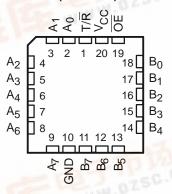
The transmit/receive (T/\overline{R}) input determines the direction of data flow through these bidirectional transceivers. Transmit (active high) enables data from A ports to B ports. The output enable (\overline{OE}) , when high, disables both the A and B ports by putting them in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT245T...D PACKAGE CY74FCT245T...P, Q, OR SO PACKAGE (TOP VIEW)



CY54FCT245T ... L PACKAGE (TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

TA	PAC	KAGE [†]	SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	QSOP - Q	Tape and reel	3.8	CY74FCT245DTQCT	FCT245D	
	QSOP - Q	Tape and reel	4.1	CY74FCT245CTQCT	FCT245C	
	SOIC - SO	Tube	4.1	CY74FCT245CTSOC	FCT245C	
	3010 - 30	Tape and reel	4.1	CY74FCT245CTSOCT	FC1245C	
	DIP – P	Tube	4.6	CY74FCT245ATPC	CY74FCT245ATPC	
–40°C to 85°C	QSOP - Q	Tape and reel	4.6	CY74FCT245ATQCT	FCT245A	
	SOIC - SO	Tube	4.6	CY74FCT245ATSOC	FCT245A	
	3010 - 30	Tape and reel	4.6	CY74FCT245ATSOCT	FC1245A	
	QSOP - Q	Tape and reel	7	CY74FCT245TQCT	FCT245	
	SOIC - SO	Tube	7	CY74FCT245TSOC	FCT245	
	3010 - 30	Tape and reel	7	CY74FCT245TSOCT	FC1245	
	CDIP - D	Tube	4.5	CY54FCT245CTDMB		
	LCC – L	Tube	4.5	CY54FCT245CTLMB		
EE°C +0 12E°C	CDIP - D	Tube	4.9	CY54FCT245ATDMB		
–55°C to 125°C	LCC – L	Tube	4.9	CY54FCT245ATLMB		
	CDIP – D	Tube	7.5	CY54FCT245TDMB		
	LCC – L	Tube	7.5	CY54FCT245TLMB		

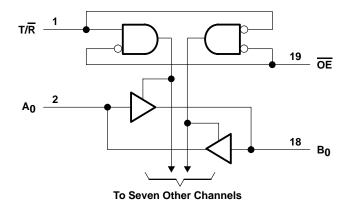
 $^{\ ^{\}dagger} \ Package \ drawings, standard \ packing \ quantities, thermal \ data, symbolization, and \ PCB \ design \ guidelines \ are \ available$ at www.ti.com/sc/package.

FUNCTION TABLE

INP	UTS	OPERATION
OE	T/R	OPERATION
L	L	B data to bus A
L	Н	A data to bus B
Н	Χ	Z

H = High logic level, L = Low logic level,X = Don't care, Z = High-impedance

logic diagram (positive logic)





CY54FCT245T, CY74FCT245T 8-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ _{JA} (see Note 1): P package	69°C/W
Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T _A	–65°C to 135°C
Storage temperature range, T _{Stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		CY54FCT245T		CY74FCT245T CY74FCT245AT CY74FCT245CT CY74FCT245DT			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
ІОН	High-level output current			-12			-32	mA
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	-40	•	85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

CY54FCT245T, CY74FCT245T 8-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TEST CONDITIONS					CY	74FCT24	15T	
PARAMETER	"	SI CONDITIONS	•	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT
Viia	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$			-0.7	-1.2				V
VIK	V _{CC} = 4.75 V,	$I_{IN} = -18 \text{ mA}$						-0.7	-1.2	V
	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA		2.4	3.3					
Voн	V _{CC} = 4.75 V	I _{OH} = -32 mA					2			V
	VCC = 4.75 V	I _{OH} = -15 mA					2.4	3.3		
Vol	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 48 \text{ mA}$			0.3	0.55				V
VOL	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 64 \text{ mA}$						0.3	0.55	V
V_{hys}	All inputs				0.2			0.2		V
	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$				5				μА
ΙΙ	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = V_{CC}$							5	μΑ
1	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 2.7 V$				±1				μΑ
ΊΗ	$V_{CC} = 5.25 \text{ V},$	$V_{IN} = 2.7 V$							±1	μΑ
1	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 0.5 V$				±1			μΑ	
ΊL	V _{CC} = 5.25 V, V _{IN} = 0.5 V								±1	μΑ
lozu	$V_{CC} = 5.5 \text{ V},$	V _{OUT} = 2.7 V				10				μΑ
lozh	$V_{CC} = 5.25 \text{ V},$	V _{OUT} = 2.7 V							10	μΑ
lozi	$V_{CC} = 5.5 \text{ V},$	$V_{OUT} = 0.5 V$				-10				μΑ
lozL	$V_{CC} = 5.25 \text{ V},$	V _{OUT} = 0.5 V							-10	μΑ
los‡	$V_{CC} = 5.5 \text{ V},$	V _{OUT} = 0 V		-60	-120	-225				mA
108+	$V_{CC} = 5.25 \text{ V},$	V _{OUT} = 0 V					-60	-120	-225	ША
l _{off}	$V_{CC} = 0 V$	V _{OUT} = 4.5 V				±1			±1	μΑ
laa			$V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.1	0.2				mA
Icc	$V_{CC} = 5.25 \text{ V},$	$V_{IN} \le 0.2 V$,	$V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.1	0.2	IIIA
	$V_{CC} = 5.5 \text{ V}, V_{IN} = 3.4$	4 V\$, f ₁ = 0, Outp	uts open		0.5	2				
ΔlCC	V _{CC} = 5.25 V, V _{IN} = 3					0.5	2	mA		
loos¶	$V_{CC} = 5.5 \text{ V}, One inpute Outputs open, T/R or VIN \leq 0.2 \text{ V} or V_{IN} \geq 0.2 \text{ V}$		0.06	0.12				mA/		
ICCD [¶]	$V_{CC} = 5.25 \text{ V}$, One inpose open, T/R or $V_{IN} \le 0.2 \text{ V}$ or $V_{IN} \ge 0.2 \text{ V}$	OE = GND and	0% duty cycle,					0.06	0.12	MHz

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



^{*} Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, IOS tests should be performed last.

 $[\]S$ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

This parameter is derived for use in total power-supply calculations.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

DADAMETED		TEST CONDITION	ie.	CY	54FCT2	45T	CY74FCT245T			LINIT
PARAMETER	TEST CONDITIONS				TYP	MAX	MIN	TYP†	MAX	UNIT
		One bit switching at f ₁ = 10 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.7	1.4				
	V _{CC} = 5.5 V, O <u>utputs open,</u>	pen,	V _{IN} = 3.4 V or GND		1.2	3.4				
	T/R or OE = GND		$V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2 V$		1.3	2.6				
IC#	lo#	at 50% duty cycle	V _{IN} = 3.4 V or GND		3.3	10.6				mA
10"		One bit switching at f ₁ = 10 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.7	1.4	IIIA
	V _{CC} = 5.25 V,	at 50% duty cycle	V _{IN} = 3.4 V or GND					1.2	3.4	
	Outputs open, T/R or OE = GND Eight bits switching at f ₁ = 2.5 MHz	switching	$V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2 V$					1.3	2.6	
		at 50% duty cycle	V _{IN} = 3.4 V or GND					3.3	10.6	
Ci					5	10		5	10	pF
Co					9	12		9	12	pF

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

 I_{CC} = Total supply current I_{CC} = Power-supply current with CMOS input levels

 ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

 D_H = Duty cycle for TTL inputs high N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

= Clock frequency for registered devices, otherwise zero

= Input signal frequency

= Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

 \parallel Values for these conditions are examples of the ICC formula.

 $^{^{\#}}$ IC = ICC + \triangle ICC \times DH \times NT + ICCD (f₀/2 + f₁ \times N₁)

CY54FCT245T, CY74FCT245T 8-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS SCCS018B – MAY 1994 – REVISED NOVEMBER 2001

switching characteristics over operating free-air temperature range (see Figure 1)

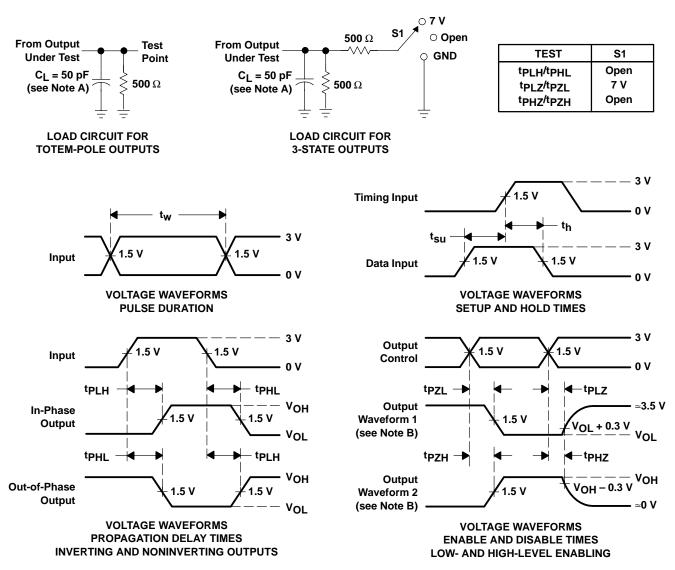
PARAMETER	FROM	то	CY54FC	T245T	CY54FC1	245AT	CY54FC1	7245CT	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	ONIT	
t _{PLH}	A or B	B or A	1.5	7.5	1.5	4.9	1.5	4.5	nc	
^t PHL	AOIB	BUIA	1.5	7.5	1.5	4.9	1.5	4.5	ns	
^t PZH	OE or T/R	A or B	1.5	10	1.5	6.5	1.5	6.2	20	
t _{PZL}	OE 01 1/K	AUID	1.5	10	1.5	6.5	1.5	6.2	ns	
t _{PHZ}	OE or T/R	A or B	1.5	10	1.5	6	1.5	5.2		
t _{PLZ}	OE OF 1/R	AUID	1.5	10	1.5	6	1.5	5.2	ns	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	CY74FCT245T		CY74FCT245AT		CY74FCT245CT		CY74FCT245DT		UNIT
PARAMETER (II	(INPUT)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNII
^t PLH	A or B	A or B B or A		7	1.5	4.6	1.5	4.1	1.5	3.8	no
t _{PHL}	AUB	BUIA	1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	ns
^t PZH	OE or T/R	A or B	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5	no
t _{PZL}	OE OF 1/R	AUIB	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5	ns
t _{PHZ}	OE or T/R	A or B	1.5	7.5	1.5	5	1.5	4.8	1.5	4.3	no
^t PLZ	OE 01 1/K	AOIB	1.5	7.5	1.5	5	1.5	4.8	1.5	4.3	ns

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







6-Feb-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9221401M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
5962-9221401MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
5962-9221403M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
5962-9221403MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
5962-9221405M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
5962-9221405MRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
CY54FCT245ATDMB	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
CY54FCT245CTLMB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
CY54FCT245TLMB	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
CY74FCT245ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT245ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245CTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245DTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245DTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245TQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
CY74FCT245TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM



PACKAGE OPTION ADDENDUM

6-Feb-2006

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing		ckage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
CY74FCT245TSOCT	ACTIVE	SOIC	DW	20 2	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT245TSOCTE4	ACTIVE	SOIC	DW	20 2	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

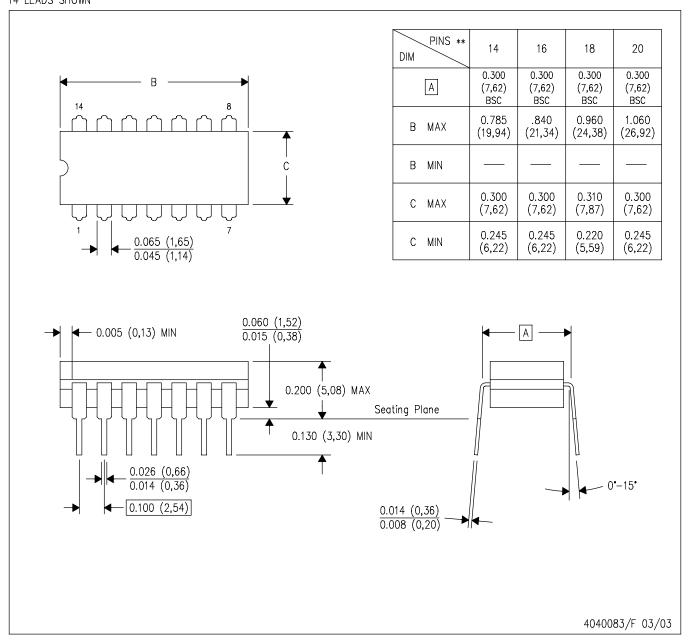
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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14 LEADS SHOWN

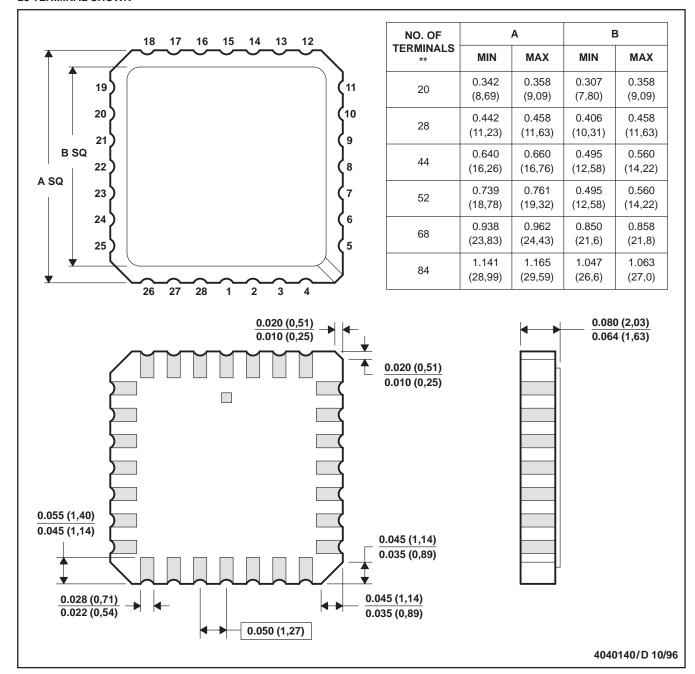


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



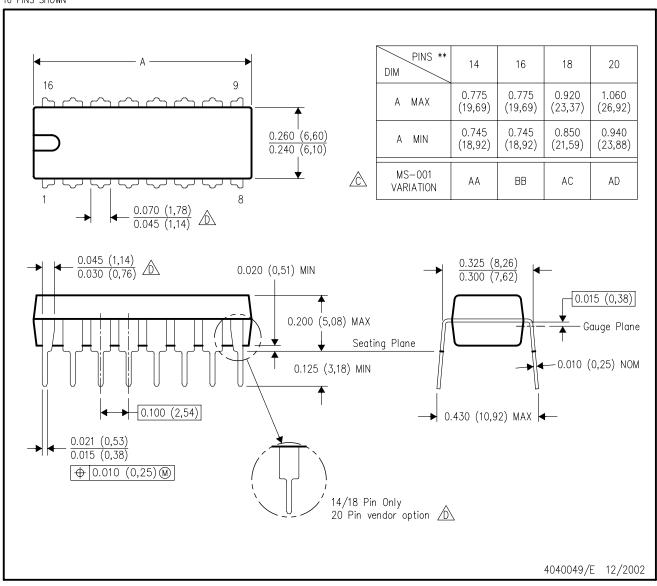
- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

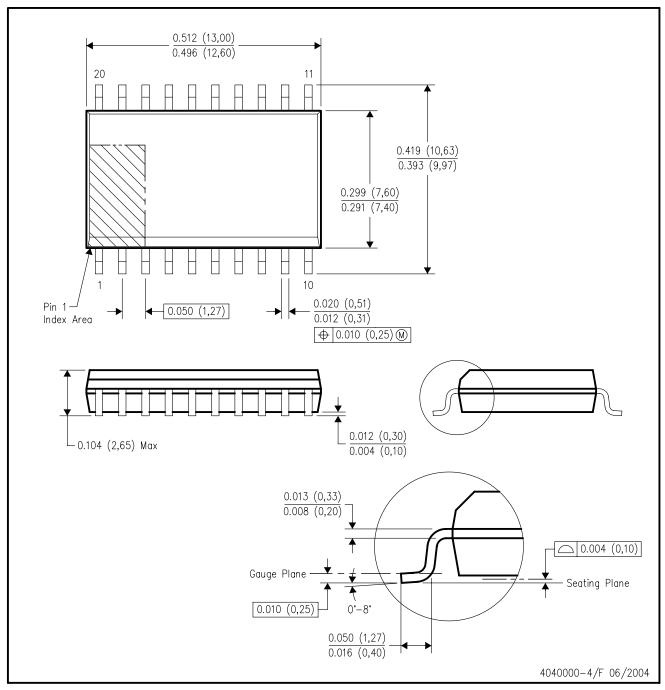
16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

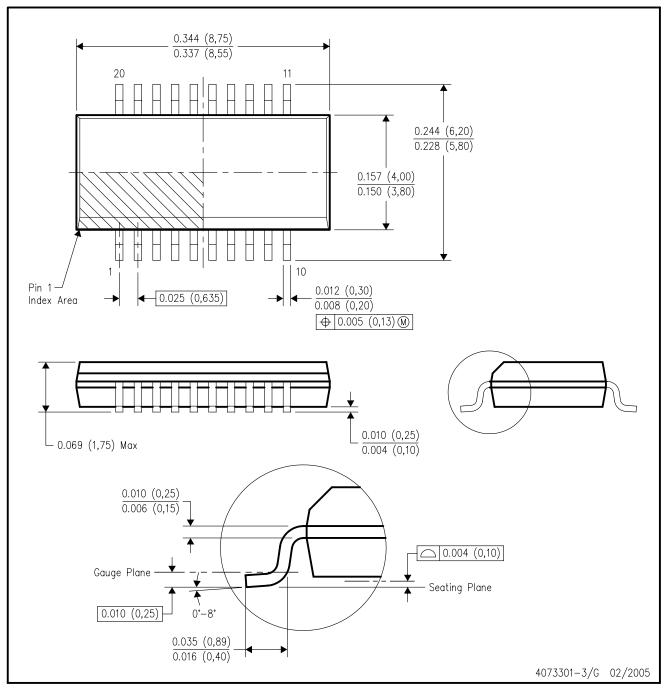


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AD.



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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265