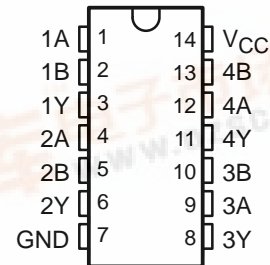


- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Buffered Inputs
- Typical Propagation Delay 7 ns at $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
 - Standard Outputs . . . 10 LSTTL Loads
 - Bus Driver Outputs . . . 15 LSTTL Loads
- Extended Temperature Performance of -40°C to 125°C

† Contact factory for details. Q100 qualification data available on request.

- Balanced Propagation Delay and Transition Times
- Significant Power Reduction, Compared to LSTTL Logic ICs
- 2-V to 6-V V_{CC} Operation
- High Noise Immunity N_{IL} or $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5\text{ V}$
- CMOS Input Compatibility, $I_I \leq 1\text{ }\mu\text{A}$ at V_{OL} , V_{OH}

M PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC08 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. The device can drive 10 LSTTL loads.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – M	Tape and reel	CD74HC08QM96Q1	HC08Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CD74HC08-Q1

QUADRUPLE 2-INPUT POSITIVE-AND GATES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2)	180°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
T_A	Operating free-air temperature	–40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

CD74HC08-Q1 QUADRUPLE 2-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I _O (mA)	V _{CC}	T _A = 25°C			CD74HC08-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	CMOS loads	−0.02	2 V	1.9			1.9		V
			−0.02	4.5 V	4.4			4.4		
			−0.02	6 V	5.9			5.9		
		TTL loads	−4	4.5 V	3.98			3.7		
			−5.2	6 V	5.48			5.2		
V _{OL}	V _I = V _{IH} or V _{IL}	CMOS loads	0.02	2 V	0.1			0.1		V
			0.02	4.5 V	0.1			0.1		
			0.02	6 V	0.1			0.1		
		TTL loads	4	4.5 V	0.26			0.4		
			5.2	6 V	0.26			0.4		
I _I	V _I = V _{CC} or GND			6 V	±0.1			±1		μA
I _{CC}	V _I = V _{CC} or GND		0	6 V	2			40		μA
C _i					10			10		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			CD74HC08-Q1		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	$C_L = 50\text{ pF}$	2 V			90		135	ns
				4.5 V			18		27	
				6 V			15		23	
			$C_L = 15\text{ pF}$	5 V		7				
t_t		Y	$C_L = 50\text{ pF}$	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	

operating characteristics, $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate (see Note 4)	No load	37	pF

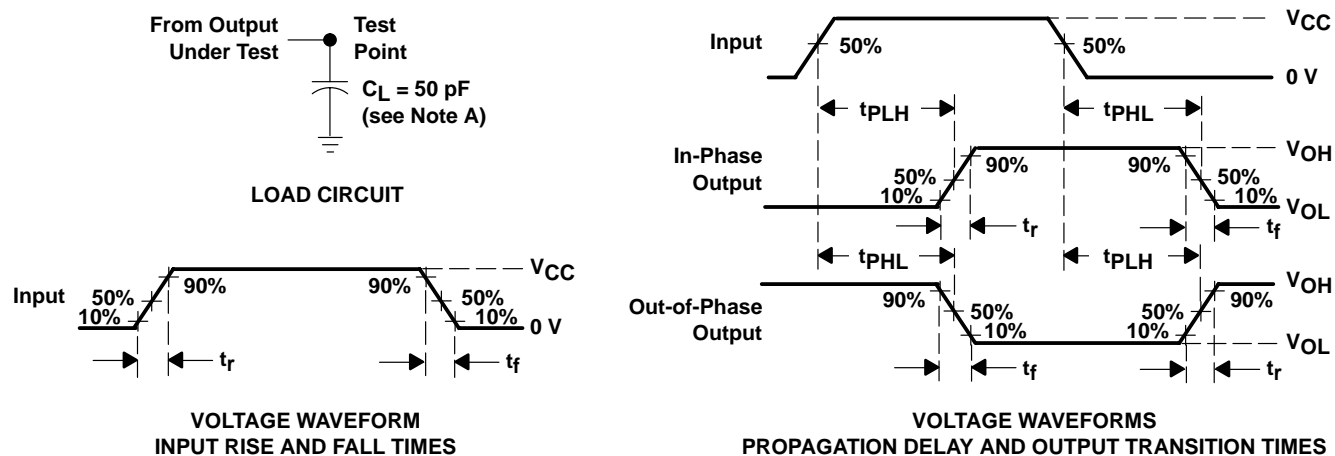
NOTE 4: C_{pd} is used to determine the dynamic power consumption, per gate.
 $P_D = V_{CC}^2 f_I (C_{pd} + C_L)$
 f_I = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

CD74HC08-Q1

QUADRUPL 2-INPUT POSITIVE-AND GATES

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HC08QM96Q1	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

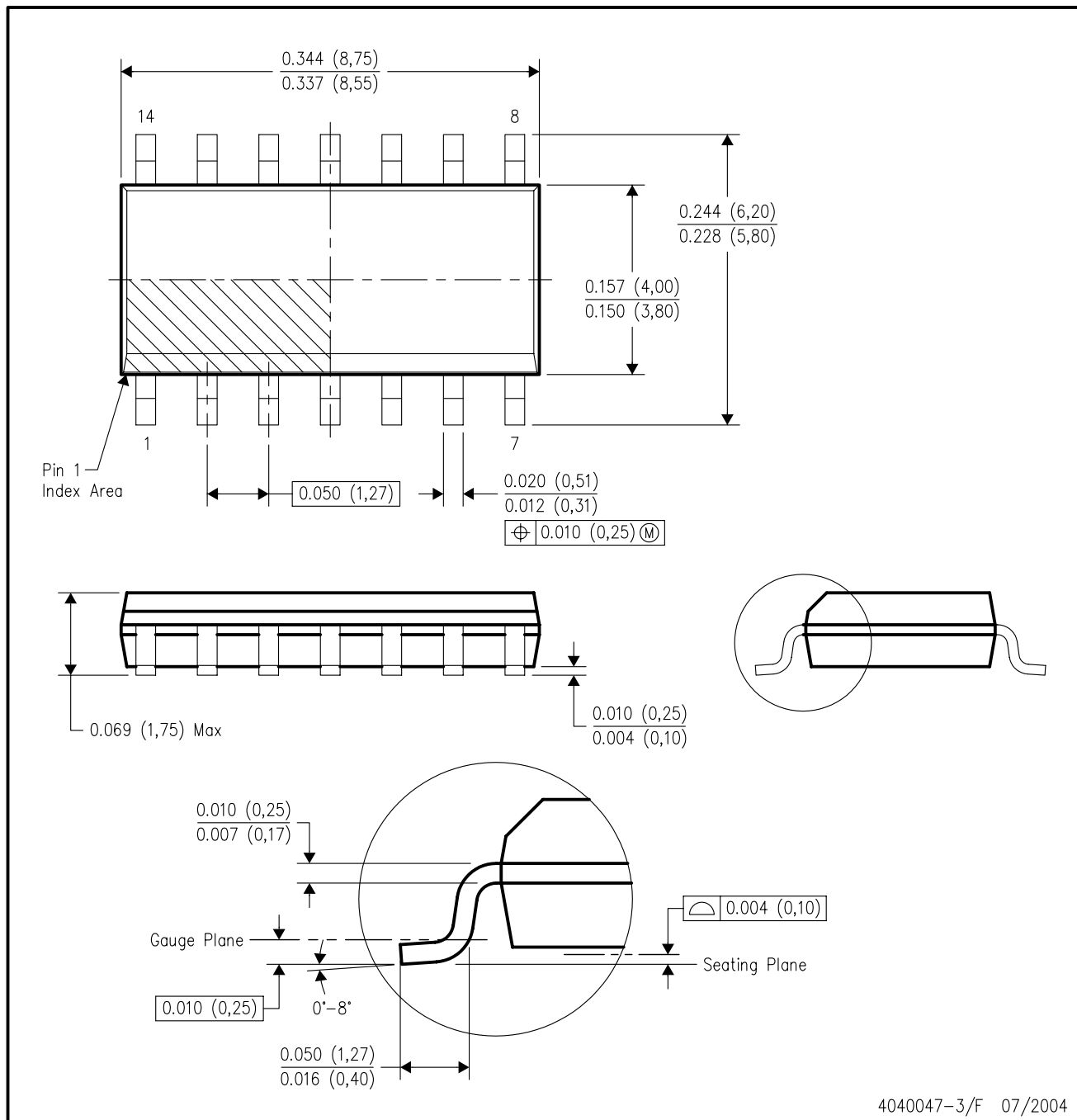
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MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/F 07/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

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