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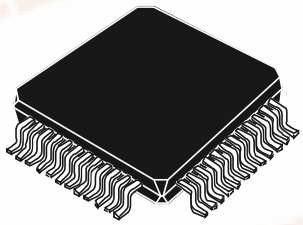
ST72681

USB 2.0 HIGH-SPEED FLASH DRIVE CONTROLLER

- **USB 2.0 Interface compatible with Mass Storage Device Class**
  - Integrated USB 2.0 PHY
  - Supports USB High Speed and Full Speed
  - Suspend and Resume operations
- **Mass Storage Controller Interface (MSCI)**
  - Supports all type of NAND Flash devices including ST, Hynix, Samsung, Toshiba, Micron.
  - Reed-Solomon Encoder/Decoder for MLC NAND Flash support: on-the-fly correction (4 bytes of a 512-byte block)
  - Flash identification support
  - up to 11MB/s for read and 7MB/s for write operations in single channel
- **Embedded ST7 8-bit MCU**
- **Supply Management**
  - 3.3V operation
  - Integrated 3.3V-1.8V voltage regulator
- **USB 2.0 low-power device compliant**
  - Less than 100mA during write operation with two NAND Flash devices
  - Less than 500µA in suspend mode
- **Clock Management**
  - Integrated PLL for generating core and USB 2.0 clock sources using an external 12 MHz crystal
- **Data Protection**
  - Write protect switch control
  - Public/Private partitions support
- **Bootability support (HDD mode)**



TQFP48

- **Production tool device configurability:**
  - USB Vendor ID/Product ID (VID/PID), Serial Number and USB strings with foreign language support
  - SCSI strings
  - One or two LED outputs
  - Adjustable NAND Flash bus frequency to reach highest performance
- **TQFP48 7x7 lead-free package**
- **Development Support**
  - Complete reference design including schematics, BOM and gerber files
- **Supports Windows XP, Windows 2K, Windows ME, Linux and MacOS. Drivers available for Windows 98 SE**

Features	ST72681
USB interface	USB 2.0 High Speed
# of NAND devices supported	up to 4
R/W speed	11MBps/7MBps
Operating Supply	3.0V to 3.6V
Operating Temperature	0°C to +70°C
Packages	TQFP48 7x7 / Die form

Rev. 2

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Table of Contents

1 INTRODUCTION

The ST72681 is a USB 2.0 high-speed Flash Drive controller. The USB 2.0 high-speed interface including PHY and function supports USB 2.0 Mass Storage Device Class.

The Mass Storage Controller Interface combined with the Reed-Solomon Encoder/Decoder on-the-fly correction (4-byte on 512-byte data blocks) provides a flexible, high transfer rate solution for interfacing a wide of range NAND Flash memory device types.

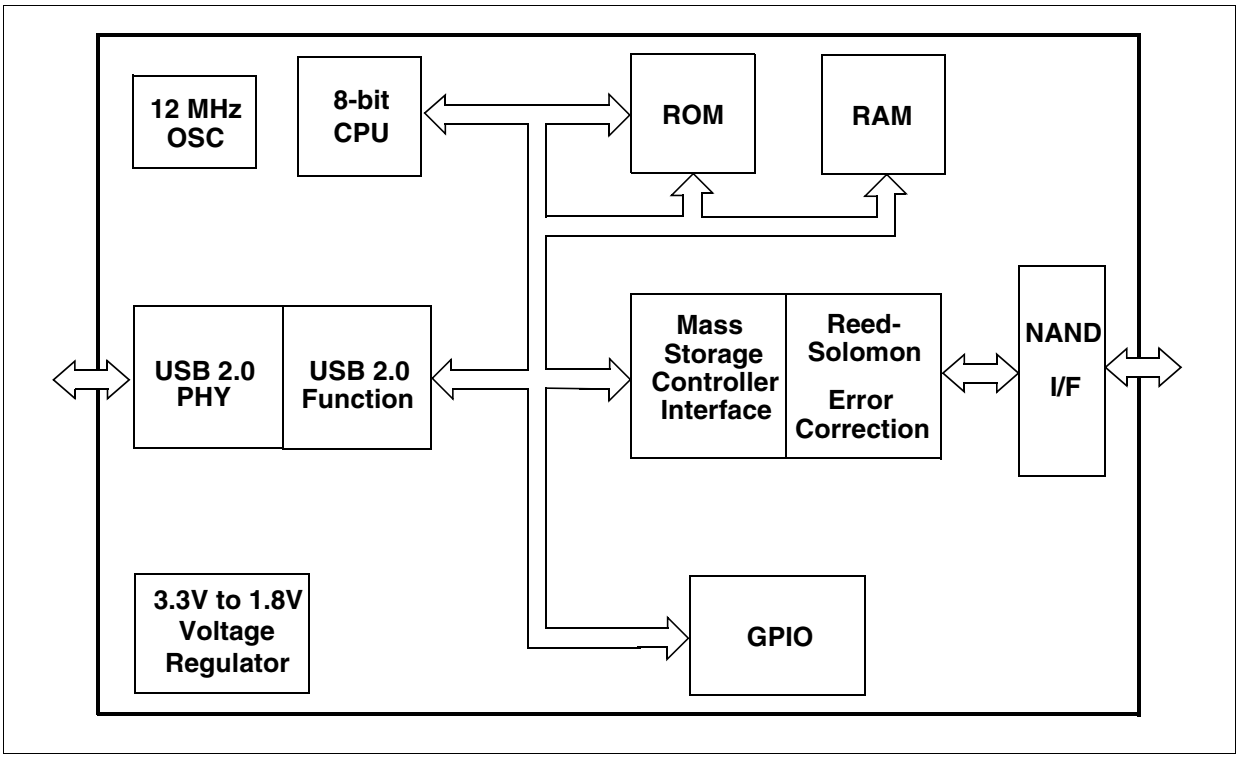
The internal 60 MHz PLL driven by the 12MHz oscillator is used to generate the 480MHz frequency for the USB 2.0 PHY.

The ST7 8-bit CPU runs the application program from the internal ROM and RAM. USB data and patch code are stored in internal RAM.

I/O ports provide functions for EEPROM connection, LEDs and write protect switch control.

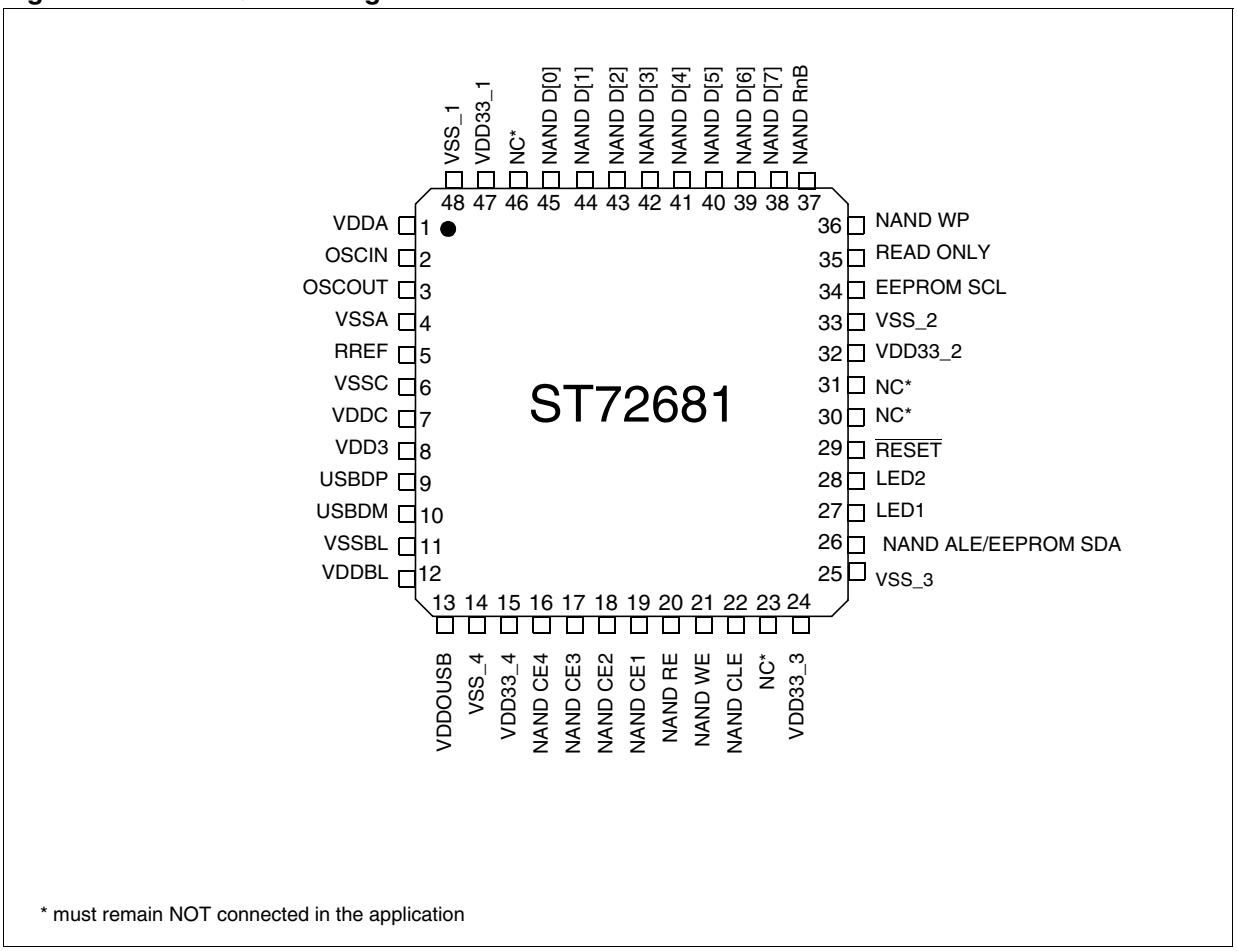
The internal 3.3V to 1.8V voltage regulator provides the 1.8V supply voltage to the digital part of the circuit.

Figure 1. Device Block Diagram



2 PIN DESCRIPTION

Figure 2. 48-Pin TQFP Package Pinout



* must remain NOT connected in the application

PIN DESCRIPTION (Cont'd)

Legend / Abbreviations for tables:

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

T_T= TTL 0.8V / 2V with Schmitt trigger

Output level: D8 = 8mA drive

D4 = 4mA drive

D2 = 2mA drive

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, wpd = weak pull-down, int = interrupt

– Output: OD = pseudo open drain, PP = push-pull

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Power Supply

Pin	Pin Name	Type	Description
48	VSS_1	S	Ground
47	VDD33_1	S	IOs and Regulator supply voltage
33	VSS_2	S	Ground
32	VDD33_2	S	IOs and Regulator supply voltage
25	VSS_3	S	Ground
24	VDD33_3	S	IOs and Regulator supply voltage
14	VSS_4	S	Ground
15	VDD33_4	S	IOs and Regulator supply voltage
13	VDDOUSB	O	USB2 PHY, OSC and PLL power supply output (1.8V)

Table 2. Control & System

Pin	Pin Name	Type	Power	Level		Description
TQFP48				Input	Output	
29	$\overline{\text{RESET}}$	I/O	3.3	C_T		Reset input with filter with internal pull-up

PIN DESCRIPTION (Cont'd)

Table 3. USB 2.0 Interface

Pin TQFP48	Pin Name	Type	Description
12	VDDBL	S	Supply voltage for buffers and deserialisation flip flops (1.8V)
11	VSSBL	S	Ground for buffers and deserialisation flip flops (1.8V)
10	USBDM	I/O	USB2 DATA -
9	USBDP	I/O	USB2 DATA +
8	VDD3	S	Supply voltage for the FS compliance (3.3V)
7	VDDC	S	Supply voltage for DLL & xor tree (1.8V)
6	VSSC	S	Ground for DLL & XOR tree (1.8V)
5	RREF	I/O	Ref. resistor for integrated impedance process adaptation (11.3 kOhms 1% Pull Down)

Table 4. USB 2.0 and core Clock System

Pin TQFP48	Pin Name	Type	Description
4	VSSA	S	Ground for osc & PLL (1.8V)
3	OSCOUT	O	12MHz oscillator output
2	OSCIN	I	12MHz oscillator input
1	VDDA	S	Supply voltage for osc & PLL (1.8V)

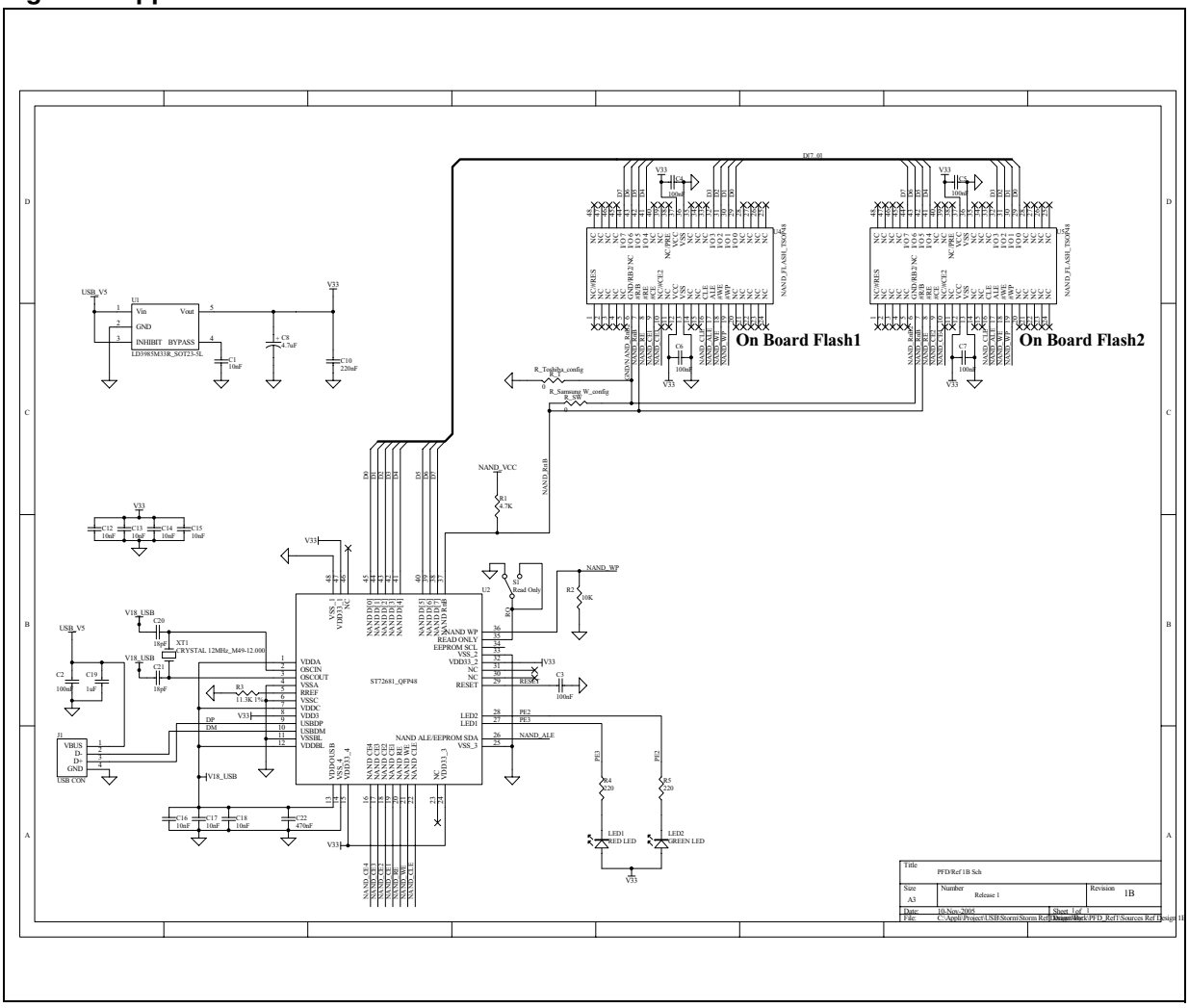
PIN DESCRIPTION (Cont'd)

Table 5. General Purpose IO Ports / Mass Storage IOs

Pin	Pin Name	Type	Level		Main function (after reset)	Alternate function
TQFP48			Input	Outputs		
45	NAND D[0]	I/O	T_T	D4	NAND DATA [0]	
44	NAND D[1]	I/O	T_T	D4	NAND DATA [1]	
43	NAND D[2]	I/O	T_T	D4	NAND DATA [2]	
42	NAND D[3]	I/O	T_T	D4	NAND DATA [3]	
41	NAND D[4]	I/O	T_T	D4	NAND DATA [4]	
40	NAND D[5]	I/O	T_T	D4	NAND DATA [5]	
39	NAND D[6]	I/O	T_T	D4	NAND DATA [6]	
38	NAND D[7]	I/O	T_T	D4	NAND DATA [7]	
26	NAND ALE / EEPROM SDA	I/O	T_T	D8	NAND ADDRESS LATCH ENABLE	EEPROM SERIAL DATA
22	NAND CLE	O	T_T	D8	NAND COMMAND LATCH ENABLE	
21	NAND WE	O	T_T	D8	NAND WRITE ENABLE	
20	NAND RE	O	T_T	D8	NAND READ ENABLE	
19	NAND CE1	O	T_T	D4	NAND ENABLE 1	
18	NAND CE2	O	T_T	D4	NAND ENABLE 2	
17	NAND CE3	O	T_T	D4	NAND ENABLE 3	
16	NAND CE4	O	T_T	D4	NAND ENABLE 4	
37	NAND RnB	I	T_T	D2	NAND READY/$\overline{\text{BUSY}}$	
36	NAND WP	O	T_T	D2	NAND WRITE PROTECT	
35	READ ONLY	I	T_T	D2	READ ONLY SWITCH	
34	EEPROM SCL	O	T_T	D2	EEPROM SERIAL CLOCK	
28	LED2	O	T_T	D8	GREEN LED (USB ACCESS)	
27	LED1	O	T_T	D8	RED LED (NAND ACCESS)	

3 APPLICATION SCHEMATICS

Figure 3. Application Schematic Sheet 1



4 ELECTRICAL CHARACTERISTICS

4.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the Devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, VDD33=3.3V. They are given only as design guidelines and are not tested.

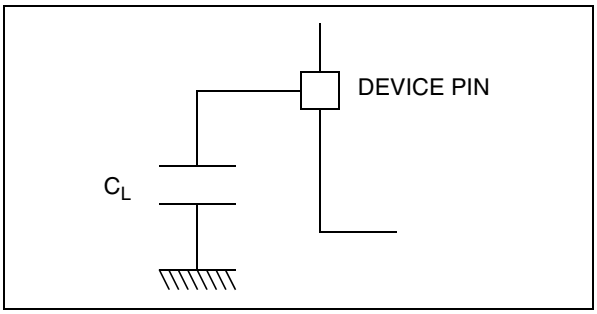
4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 4.

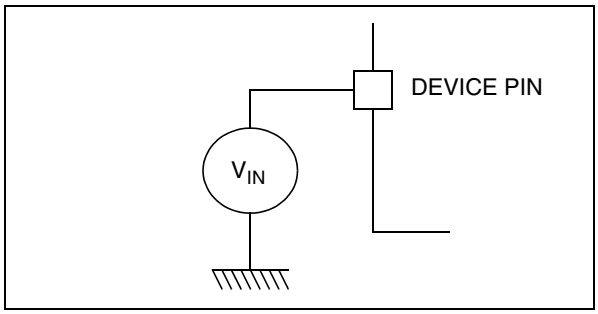
Figure 4. Pin loading conditions



4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 5.

Figure 5. Pin input voltage



4.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the Device. This is a stress rating only and functional operation of the Device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.2.1 Voltage Characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD33} - V_{SS}	Supply voltage	4.0	V
V_{IN} [1) & 2)]	Input voltage on any other pin	V_{SS}-0.3 to V_{DD33}+0.3	V
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see section 4.6.3 on page 14	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		

4.2.2 Current Characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD33}	Total current into V_{DD33} power lines (source) [3)]	200	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) [3)]	200	
I_{IO} [(4)]	Output current sunk by any I/O D2 type	25	
	Output current sunk by any I/O D4 type	35	
	Output current sunk by any I/O D8 type	50	
	Output current source by any I/Os and control pin	-25	

4.2.3 Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_{JMAX}	Maximum junction temperature	120	°C

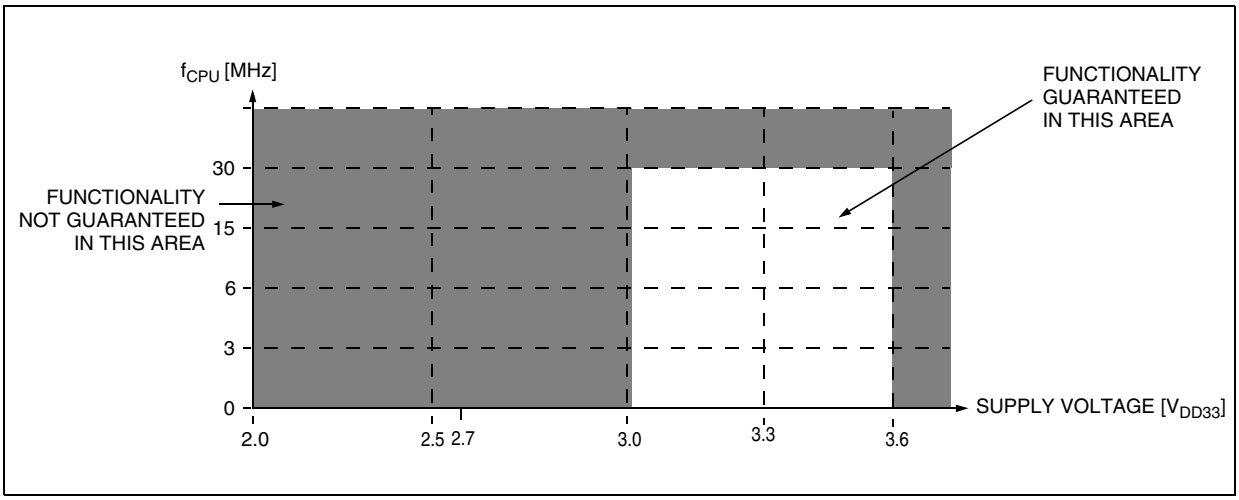
Notes:

1. Directly connecting the $\overline{\text{RESET}}$ and I/O pins to V_{DD33} or V_{SS} could damage the Device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for $\overline{\text{RESET}}$, 10kΩ for I/Os). For the same reason, unused I/O pins must not be directly tied to V_{DD33} or V_{SS}.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD33}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. All power supply (V_{DD33}) and ground (V_{SS}) lines must always be connected to the external supply.
4. Refer to Table 5 on page 7, to know the output drive capability of each of the I/Os

4.3 OPERATING CONDITIONS

4.3.1 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD33}	Power Supply		3.0	3.6	V
T_A	Ambient temperature range		0	70	°C



4.4 SUPPLY CURRENT CHARACTERISTICS

4.4.1 RUN and SUSPEND Modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current in RUN mode	f_{OSC}=12MHz	15	25	35	mA
	Supply current in SUSPEND mode	V_{DD33}=3.3V, T_A=+25°C	60	90	190	µA

4.4.2 Supply and Clock Managers

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
$I_{DD(CK)}$	Supply current of crystal oscillator [3]		1000	2000	µA

Notes:

1. Typical data are based on T_A=25°C and f_{CPU}=12MHz.
2. Data based on characterization results, not tested in production.
3. Data based on characterization results done with the external components specified in Section 4.5.1, not tested in production.

4.5 CLOCK AND TIMING CHARACTERISTICS

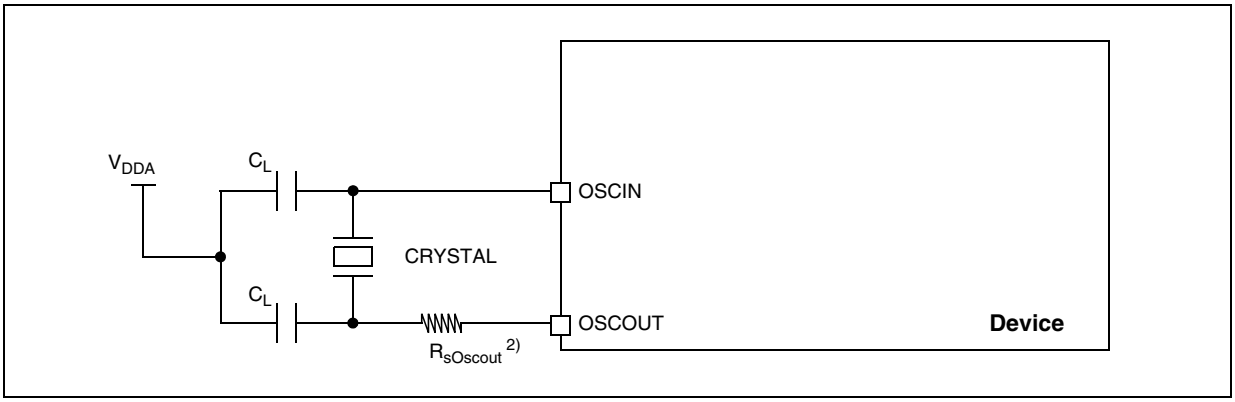
Subject to general operating conditions for V_{DD33}, f_{OSC}, and T_A.

4.5.1 Crystal Oscillator

The Device internal clock is supplied from a crystal oscillator. All the information given in this paragraph are based on characterization results with specified typical external components. In the application the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal manufacturer for more details (frequency, package, accuracy...).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency			12		MHz
CK_{ACC}	Total crystal oscillator accuracy	abs. value + temp + aging			+/-60	ppm
α_{OSC}	Crystal oscillator duty cycle [1]		45	50	55	%

Figure 6. Typical Application with a Crystal



Notes:

1. The crystal oscillator duty cycle has to be adjusted through the two C_L capacitors. Refer to the crystal manufacturer for more details.

2. Depending on the crystal power dissipation, a serial resistor $R_{sOscout}$ may be added. Refer to the crystal manufacturer for more details.

Table 6. Typical C_L and R_S Values by Crystal

Supplier	Typical Crystal	C_L (pF)	$R_{sOscout}$ (Ω)
NDK	AT51 or AT41	16	560

4.6 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

4.6.1 Functional EMS (Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD33} and V_{SS33} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

4.6.1.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

– Corrupted program counter

– Unexpected reset

– Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD33}=3.3V, T_A=+25°C, f_{OSC}=12MHz conforms to IEC 1000-4-2	4B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD33} and V_{SS33} pins to induce a functional disturbance	V_{DD33}=3.3V, T_A=+25°C, f_{OSC}=12MHz conforms to IEC 1000-4-4	4A

4.6.2 Electro Magnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}@12MHz]	Unit
S_{EMI}	Peak level	V_{DD33}=3.3V, T_A=+25°C, conforming to SAE J 1752/3 **Note:** Refer to Application Note AN1709 for data on other package types.	0.1MHz to 30MHz	20	dBµV
			30MHz to 130MHz	25	
			130MHz to 1GHz	25	
			SAE EMI Level	4	-

EMC CHARACTERISTICS (Cont'd)

4.6.3 Absolute Maximum Ratings (Electrical Sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

4.6.3.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V

Notes:

1. Data based on characterization results, not tested in production.

4.6.3.2 Static and Dynamic Latch-Up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical Sensitivities

Symbol	Parameter	Conditions	Class [1]
LU	Static latch-up class	T_A=+25°C	A
DLU	Dynamic latch-up class	V_{DD33}=3.3V, f_{OSC}=12MHz, T_A=+25°C	A

Notes:

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

4.7 I/O PORT PIN CHARACTERISTICS

4.7.1 General Characteristics

Subject to general operating conditions for VDD33, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports				$0.16xV_{DD33}$	V
V_{IH}	Input high level voltage			$0.85xV_{DD33}$			
V_{hys}	Schmitt trigger voltage hysteresis [1]			400			mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD33}$, standard I/Os				1	µA
R_{PU}	Weak pull-up equivalent resistor [2]	$V_{IN}=V_{SS}$	V_{DD33}=3.3V	32	50	75	kΩ

Notes:

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, tested in production at V_{DD33} max.

Figure 7. Typical V_{IL} and V_{IH} standard I/Os

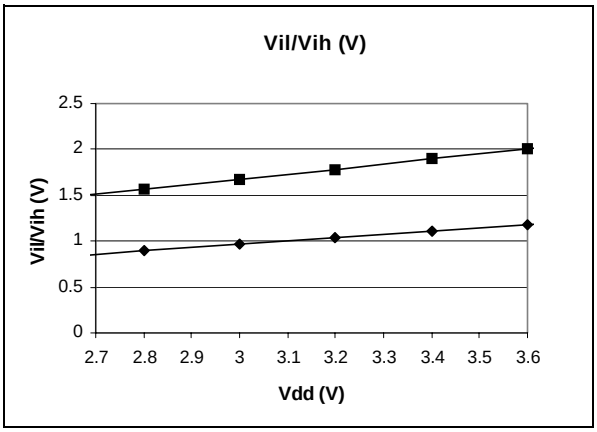


Figure 8. Typical R_{PU} vs. V_{DD33} with $V_{IN}=V_{SS}$

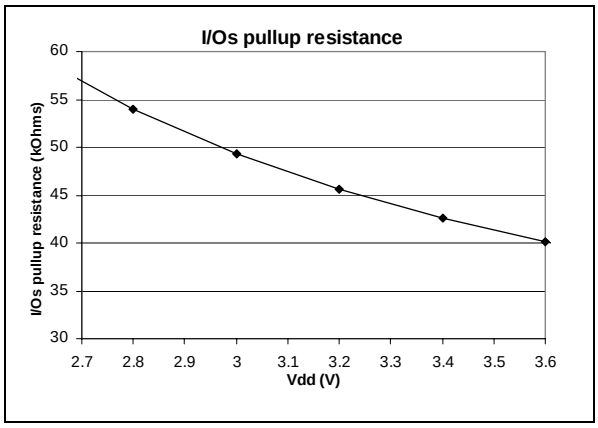
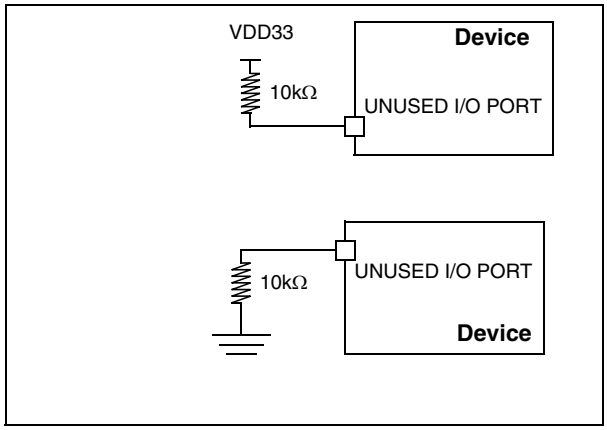


Figure 9. Two typical Applications with unused I/O Pin



I/O PORT PIN CHARACTERISTICS (Cont'd)

4.7.2 Output Driving Current

Subject to general operating conditions for V_{DD33}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} 1)	Output low level voltage for a D2 I/O pin when 8 pins are sunk at same time (see Figure 10)	V_{DD33}=3.3V	I_{IO}=2mA		300	mV
	Output low level voltage for a D4 I/O pin when 8 pins are sunk at same time (see Figure 11)		I_{IO}=4mA		400	
	Output low level voltage for a D8 I/O pin when 8 pins are sunk at same time (see Figure 12)		I_{IO}=8mA		500	
V_{DD33}-V_{OH} 2)	Output high level voltage for a D2 I/O pin when 8 pins are sourced at same time (see and Figure 13)		I_{IO}=2mA		600	mV
	Output high level voltage for a D4 I/O pin when 8 pins are sourced at same time (see Figure 14)		I_{IO}=4mA		600	
	Output high level voltage for a D8 I/O pin when 8 pins are sourced at same time (see Figure 15)		I_{IO}=8mA		600	

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 4.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

2. The I_{IO} current sourced must always respect the absolute maximum rating specified in Section 4.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD33}. True open drain I/O pins does not have V_{OH}.

Figure 10. Typical V_{OL} at V_{DD33}=3.3V (I/O D2)

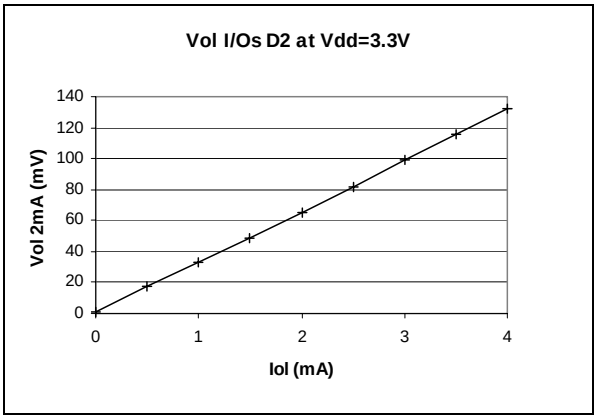


Figure 11. Typical V_{OL} at V_{DD33}=3.3V (I/O D4)

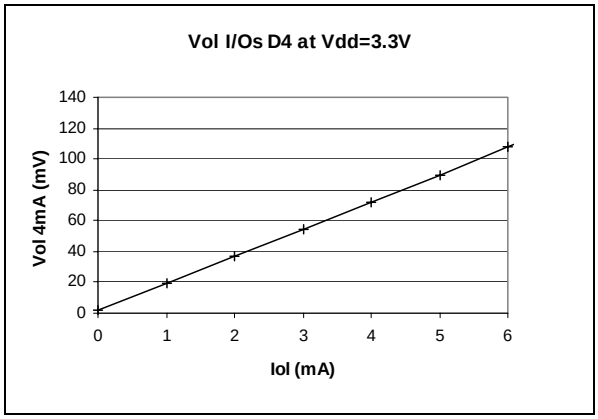


Figure 12. Typical V_{OL} at V_{DD33}=3.3V (I/O D8)

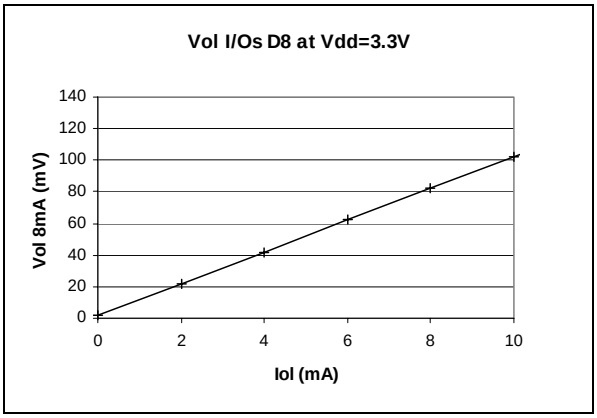


Figure 13. Typical V_{DD33}-V_{OH} vs. V_{DD33} (IO D2)

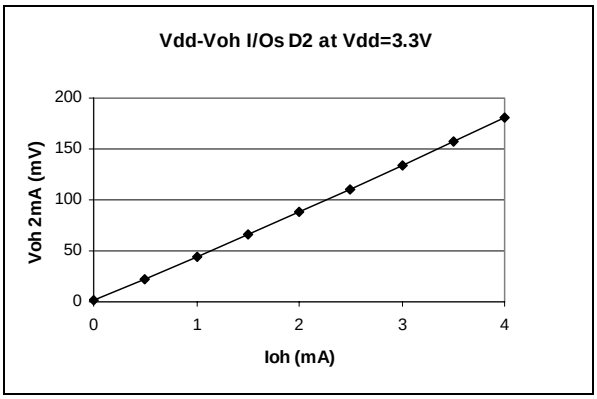


Figure 14. Typical V_{DD33}-V_{OH} vs. V_{DD33} (IO D4)

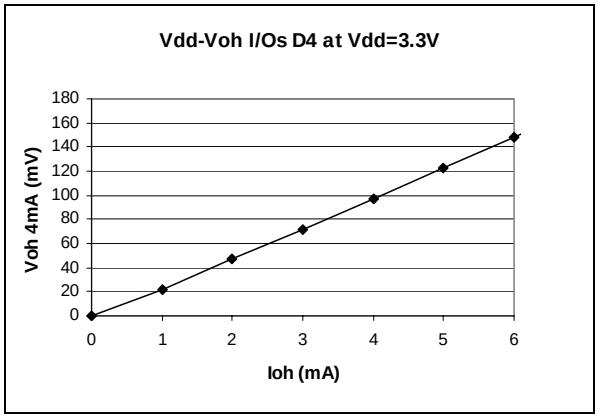
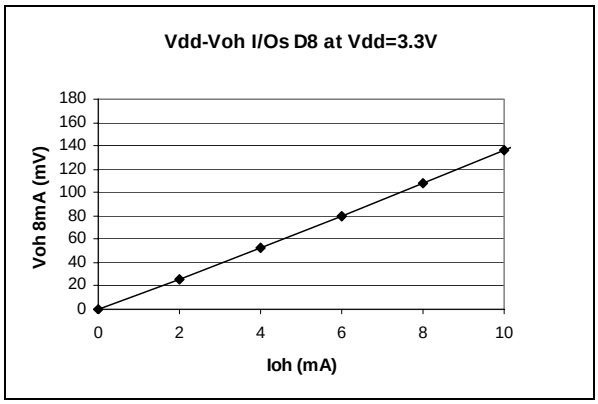


Figure 15. Typical V_{DD33}-V_{OH} vs. V_{DD33} (IO D8)



4.8 CONTROL PIN CHARACTERISTICS

4.8.1 Asynchronous $\overline{\text{RESET}}$ Pin

T_A = 0 to +55°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]				$0.16xV_{DD33}$	V
V_{IH}	Input high level voltage		$0.85xV_{DD33}$			
V_{hys}	Schmitt trigger voltage hysteresis[1]			450		mV
R_{ON}	Pull-up equivalent resistor	V_{DD33}=3.3V	20	40	80	kΩ
		V_{DD33}=2V		100		
$t_{eh(RSTL)}$	External reset pulse hold time [2]		2.5			µs
$t_{g(RSTL)}$	Filtered glitch duration [3]			200		ns
$t_{ew(RSTL)}$	External reset pulse duration [4]		500			µs
$t_{iw(RSTL)}$	Internal reset pulse duration			2		Tcpu

Notes:

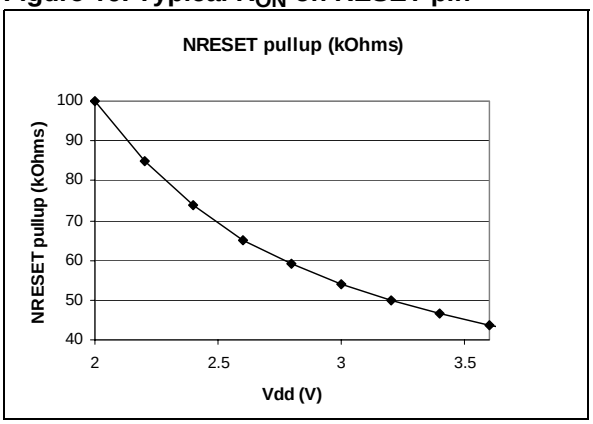
1. The user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in Section 4.8.1. Otherwise the reset will not be taken into account internally.

2. To guarantee the reset of the Device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{eh(RSTL)}$ can be ignored. Not tested in production, guaranted by design.

3. The reset network protects the device against parasitic resets.

4. The user must ensure that external reset duration respect this timing to guarantee a correct start-up of the internal regulator at power-up. Not tested in production, guaranted by design.

Figure 16. Typical R_{ON} on $\overline{\text{RESET}}$ pin



4.9 OTHER COMMUNICATION INTERFACE CHARACTERISTICS

4.9.1 MSCI Parallel Interface

Figure 17. Timing diagrams for input mode (with max load on CTRL signal=50pf)

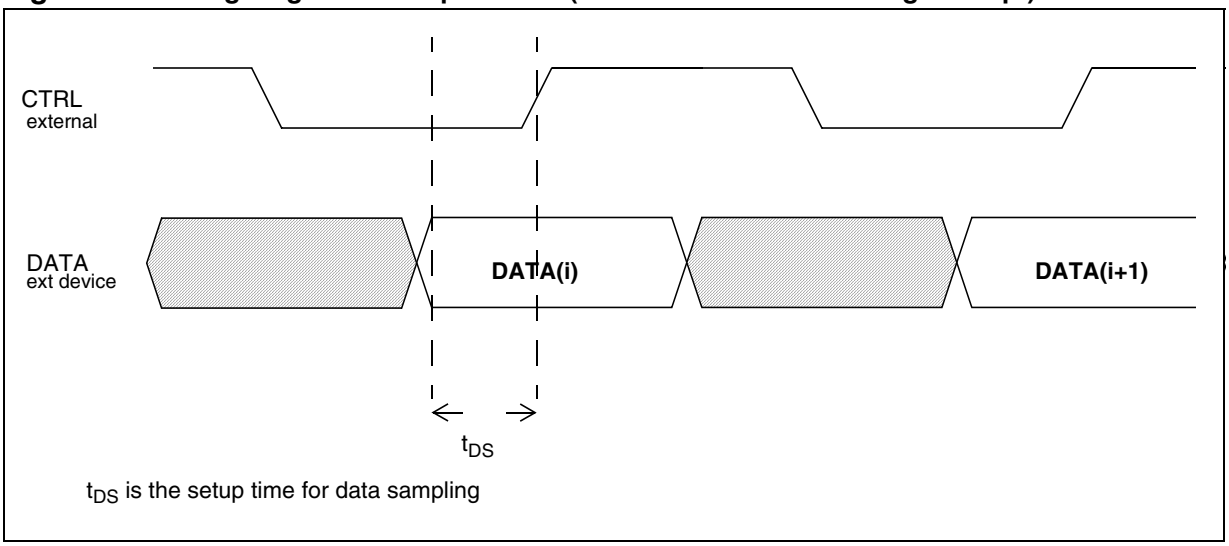


Figure 18. Timing diagrams for output mode (with max CTRL signal=50pf, DATA)

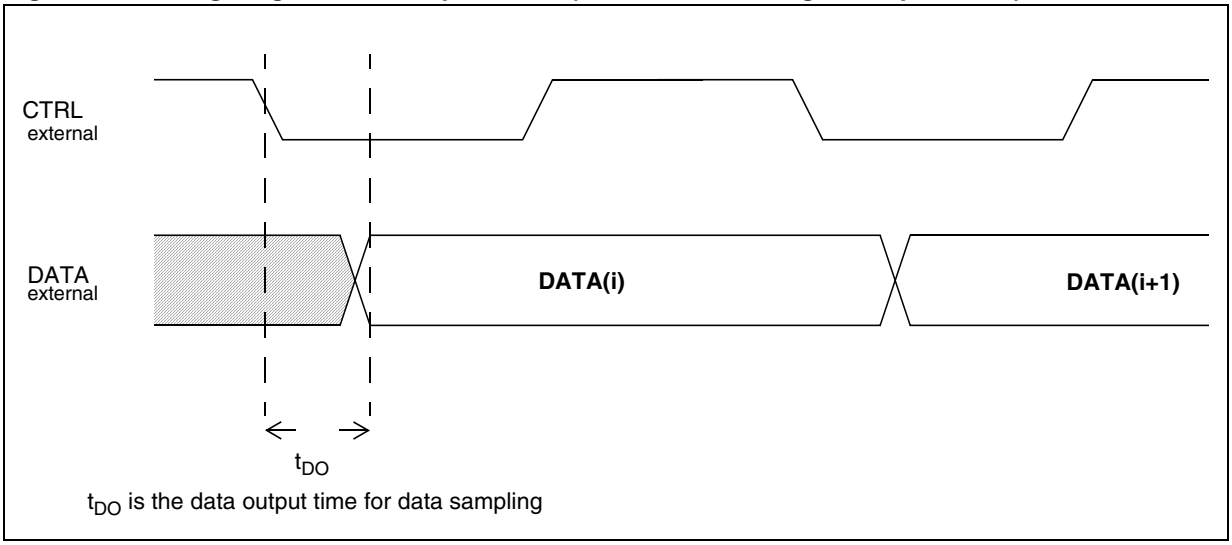


Table 7. MSCI Parallel Interface: DC Characteristics

MSCI DC Electrical Characteristics						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ [1)]**	**Max.**	**Unit**
Data Setup Time	t_{DS}			11		ns
Data Output time	t_{DO}			6		ns
CTRL line capacitance	Cctrl			50		pF
Data line capacitance	Cdata			50		pF

Notes:
1. Data based on design simulation and not tested in production.

4.9.2 USB (Universal Bus Interface)

Table 8. USB Interface: DC Characteristics

USB DC Electrical Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$I_{DDsuspend}$	Suspend current	V_{DD33}=3.3V, regulator and PHY ON	0.5 [1)]	1.5	6 [1)]	mA
		V_{DD33}=3.3V, Powerdown mode, 25°C [2)]	60	90	190	uA
R_{PU}	Pull-up resistor [1)]			1.5		kΩ
Full Speed Mode						
V_{TERM}	Termination Voltage		0.8		2.0	V
VOH	High Level Output Voltage		2.8		3.6	V
VOL	Low Level Output Voltage				0.8	V
V_{CRS}	Crossover Voltage		1.3		2.0	V
High Speed Mode						
V_{HSOH}	HS Data Signalling High			400		mV
V_{HSOL}	HS Data Signalling Low			5		mV

Notes:
1. Not tested in production, guaranteed by characterization.
2. In order to reach this value, the software must force the regulator into powerdown mode and the IOs compensation cell off.

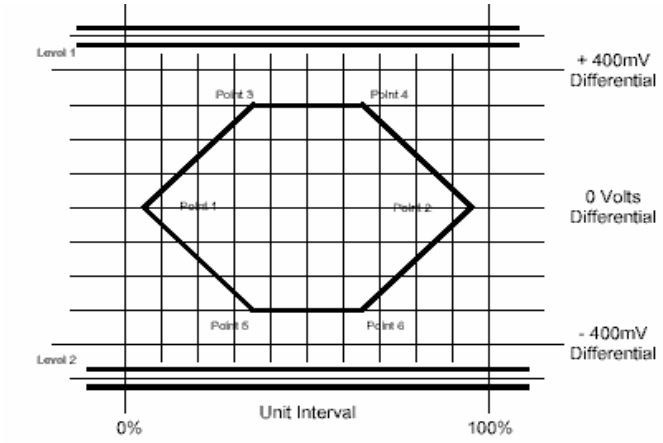
Table 9. USB Interface: Timing

USB DC Electrical Characteristics					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Unit**
Full Speed Mode					
T_{FR}	Rise Time	C_L=50pF	4	20	ns
T_{FF}	Fall Time	C_L=50pF	4	20	ns
High Speed Mode					
T_{HSR}	Rise Time			500 [1)]	ps
T_{HSF}	Fall Time			500 [1)]	ps
T_{HSDRAT}	HS Data Rate		479.76	480.24	Mb/s

Notes:
1. Not tested in production, guaranteed by characterization.

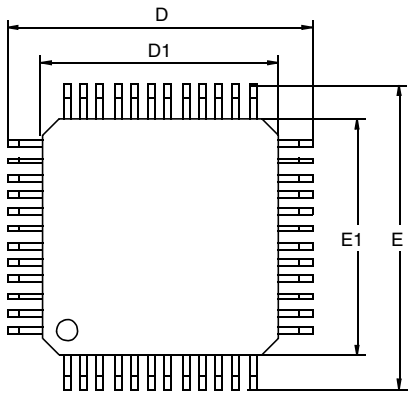
Table 10. USB High Speed Transmit Waveform requirements

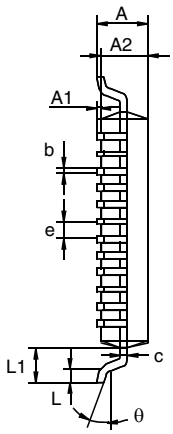
	Voltage Level (DP - DN)	**Time**
Unit Interval (UI)	-	2.082 to 2.084 ns
Level 1	475 mV	-
Level 2	-475 mV	-
Point 1	0V	5% UI
Point 2	0V	95% UI
Point 3	300 mV	35% UI
Point 4	300 mV	65% UI
Point 5	-300 mV	35% UI
Point 6	-300 mV	65% UI



5 PACKAGE MECHANICAL DATA

Figure 19. 48-Pin Thin Quad Flat Package





Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
E		9.00			0.354	
E1		7.00			0.276	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	48					

6 DEVICE ORDERING INFORMATION

Table 11. Ordering Information

Part number	Package	Operating voltage	Temperature range
ST72681/S13	TQFP48 7x7mm	3.0V to 3.6V	0°C to +70°C

7 REVISION HISTORY

Table 12. Revision History

Date	Revision	Description of Changes
17-May-2005	1	Changed status of the document Changed description on 1st page Removed unconnected pins in Table 5 on page 7 Changed Table 4, “USB 2.0 and core Clock System,” on page 6 Changed pin 5 description in Table 3, “USB 2.0 Interface,” on page 6 Changed section 3 on page 8 Changed Figure 3 and Figure 4
18-Nov-2005	2	Electrical Characteristics section added, section 4 on page 9 Additional features listed on front page Status of document changed to Datasheet Application schematics modified, Figure 4 removed Section 4.6 (Memory Characteristics) removed VDDOUSB marked as O (output) in Table 1, “Power Supply,” on page 5

Notes:

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