LM2902W

Low Power Quad Operational Amplifier

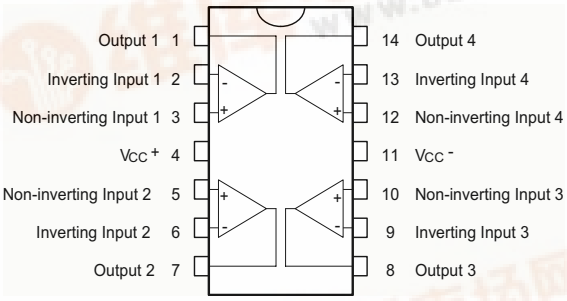
- Wide gain bandwidth: 1.3MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100dB
- Very low supply current per amp: 375µA
- Low input bias current: 20nA
- Low input offset current: 2nA
- ESD internal protection: 700V
- Wide power supply range:
  - Single supply: +3V to +30V
  - Dual supplies: ±1.5V to ±15V

N
DIP14
(Plastic Package)

D
SO-14
(Plastic Micropackage)

P
TSSOP14
(Thin Shrink Small Outline Package)

Pin connections (top view)



Description

This circuit consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed especially for automotive and industrial control systems.

It operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

All the pins are protected against electrostatic discharges up to 700V.

Order Codes

Part Number	Temperature Range	Package	Packing	Marking
LM2902WN	-40°C, +125°C	DIP14	Tube	2902W
LM2902WD/DT		SO-14	Tube or Tape & Reel	
LM2902WPT		TSSOP14 (Thin Shrink Outline Package)	Tape & Reel	

1 Absolute Maximum Ratings

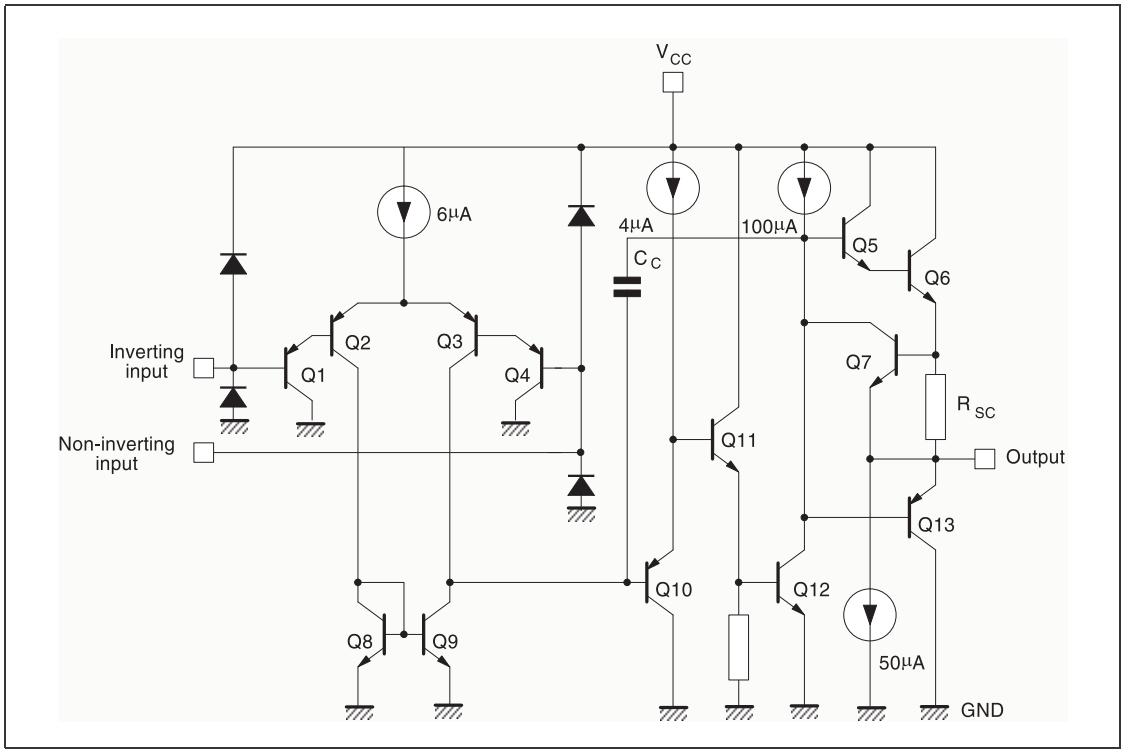
Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±16 to 32	V
V_{ID}	Differential Input Voltage	+32	V
V_I	Input Voltage	-0.3 to Vcc + 0.3	V
	Output Short-circuit to Ground (1)	Infinite	
I_{in}	Input Current (2)	50	mA
T_{oper}	Operating Free-Air Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
R_{thja}	Thermal Resistance Junction to Ambient SO-14 TSSOP14 DIP14	 100 103 66	°C/W
ESD	HBM: Human Body Model(3)	700	V
	MM: Machine Model(4)	150	V
	CDM: Charged Device Model	1500	V

1. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA, independent of the magnitude of V_{CC}^+
2. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than -0.3V.
3. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
4. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

2 Circuit Schematics

Figure 1. Schematic diagram (1/4 LM2902)



3 Electrical Characteristics

Table 2. V_{CC}^+ = 5V, V_{CC}^- = Ground, Vo = 1.4V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (1)	T_{amb} = +25°C		2	7	mV
		$T_{min} \le T_{amb} \le T_{max.}$			9	
I_{IO}	Input Offset Current	T_{amb} = +25°C		2	30	nA
		$T_{min} \le T_{amb} \le T_{max.}$			40	
I_{IB}	Input Bias Current(2)	T_{amb} = +25°C		20	150	nA
		$T_{min} \le T_{amb} \le T_{max.}$			300	
A_{VD}	Large Signal Voltage Gain	V_{CC}^+ = +15V, R_L = 2kΩ, V_o = 1.4V to 11.4V, T_{amb} = + 25°C	50	100		V/mV
		V_{CC}^+ = +15V, R_L = 2kΩ, V_o = 1.4V to 11.4V, $T_{min} \le T_{amb} \le T_{max.}$	25			
SVR	Supply Voltage Rejection Ratio	R_S ≤10kΩ, T_{amb} =+ 25°C	65	110		dB
		R_S ≤10kΩ, $T_{min} \le T_{amb} \le T_{max.}$	65			
I_{CC}	Supply Current (all op-amps, no load)	T_{amb} = +25°C, V_{CC} = +5V		0.7	1.2	mA
		T_{amb} = +25°C, V_{CC} = +30V		1.5	3	
		$T_{min} \le T_{amb} \le T_{max.}$, V_{CC} = +5V		0.9	1.2	
		$T_{min} \le T_{amb} \le T_{max.}$, V_{CC} = +30V		1.5	3	
V_{ICM}	Input Common Mode Voltage Range(3)	V_{CC}= 30V T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max.}$	 0 0		 V_{CC} -1.5 V_{CC} - 2	V
CMR	Common-mode Rejection Ratio	R_S ≤10kΩ, T_{amb} = +25°C	70	80		dB
		R_S ≤10kΩ, $T_{min} \le T_{amb} \le T_{max.}$	60			
I_O	Output Short-circuit Current	V_{id} = +1V, V_{CC} = +15V, V_o = +2V	20	40	70	mA
I_{SINK}	Output Sink Current	V_{id} = -1V, V_{CC} = +15V, V_o = +2V	10	20		mA
		V_{id} = -1V, V_{CC} = +15V, V_o = +0.2V	12	50		µA
V_{OH}	High Level Output Voltage	V_{CC} + 30V, R_L = 2kΩ: T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max.}$	 26 26	27		V
		V_{CC} + 30V, R_L = 10kΩ: T_{amb} = +25°C, $T_{min} \le T_{amb} \le T_{max.}$	 27 27	28		
		V_{CC} + 5V, R_L = 2kΩ: $T_{min} \le T_{amb} \le T_{max.}$ T_{amb} = +25°C	 3.5 3			

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	R_L = 10kΩ, T_{amb} = +25°C		5	20	mV
		R_L = 10kΩ, $T_{min} \leq T_{amb} \leq T_{max}$			20	
SR	Slew Rate	V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain		0.4		V/µs
GBP	Gain Bandwidth Product	V_{CC} = 30V, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF		1.3		MHz
THD	Total Harmonic Distortion	f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = 2Vpp, C_L = 100pF, V_{CC} = 30V		0.015		%
e_n	Equivalent Input Noise Voltage	f = 1kHz, R_S = 100Ω, V_{CC} = 30V		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift			7	30	µV/°C
DI_{io}	Input Offset Current Drift			10	200	pA/°C
V_{O1}/V_{O2}	Channel Seperation (4)	1kHz ≤ f ≤ 20kHz		120		dB

1. V_O = 1.4V, R_S = 0Ω, 5V < V_{CC}^+ < 30V, 0V < V_{ic} < V_{CC}^+ - 1.5V.
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so no loading charge change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ –1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Figure 2. Input bias current vs. T_{amb}

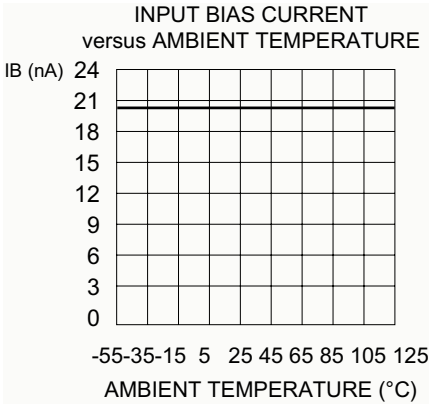


Figure 3. Input voltage range

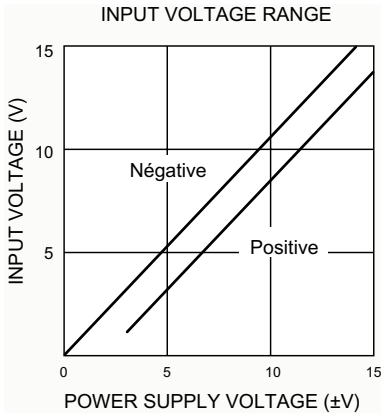


Figure 4. Current limiting

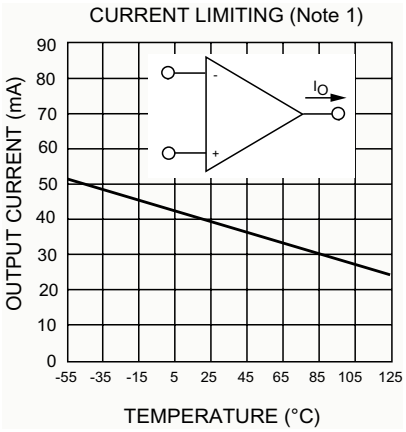


Figure 5. Supply current

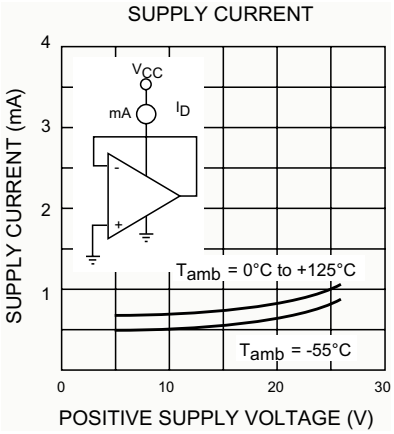


Figure 6. Gain bandwidth product

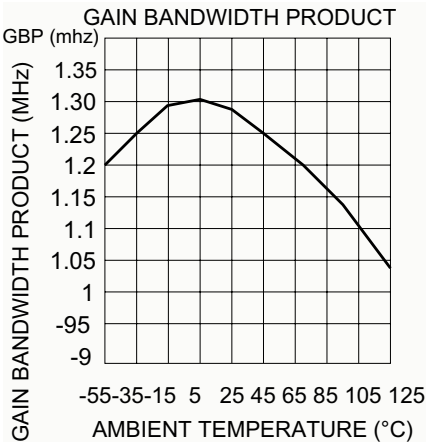


Figure 7. Voltage follower pulse response

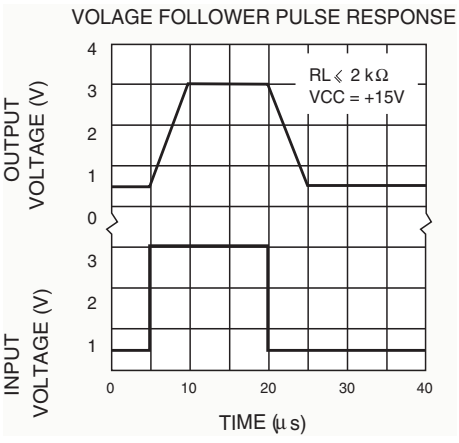


Figure 8. Common mode rejection ratio

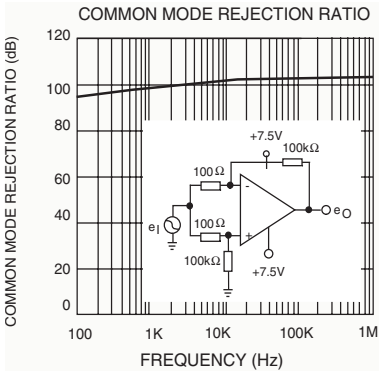


Figure 9. Output characteristics

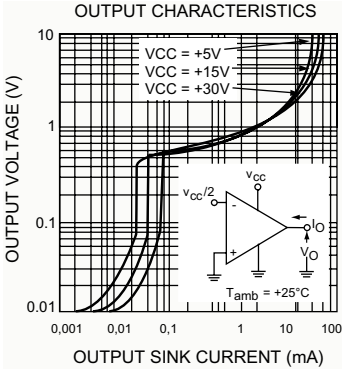


Figure 10. Open loop frequency response

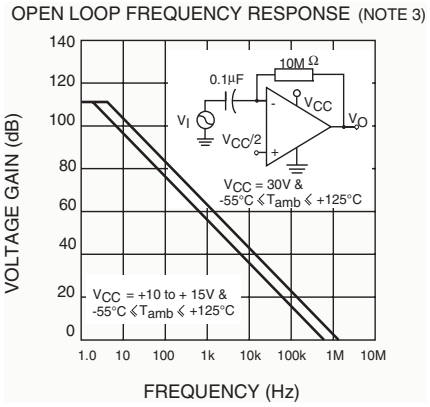


Figure 11. Voltage follower pulse response

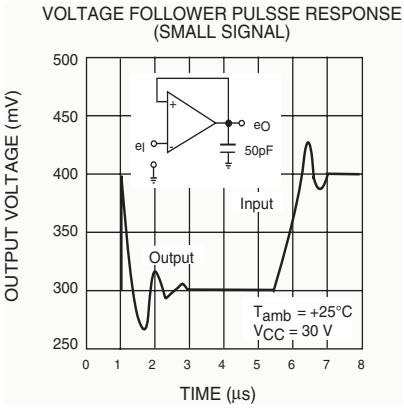


Figure 12. Large signal frequency response

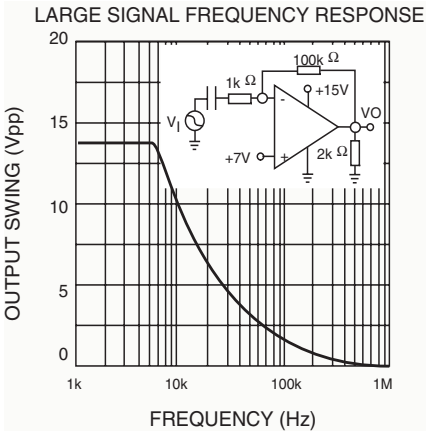


Figure 13. Output characteristics

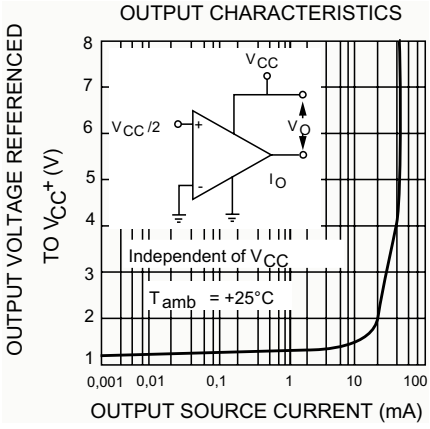


Figure 14. Positive supply voltage

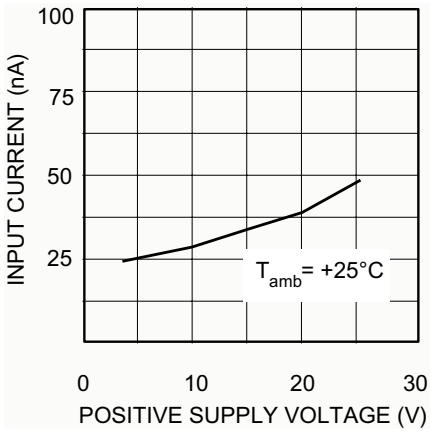


Figure 15. Positive supply voltage

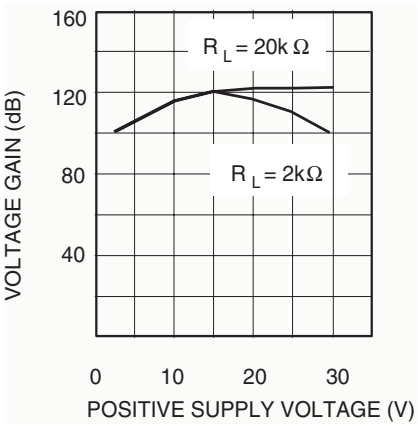


Figure 16. Power supply & common mode rejection ratio

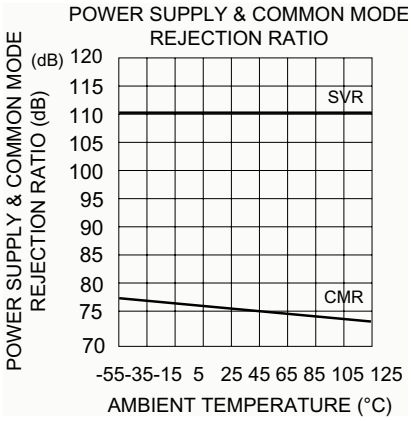
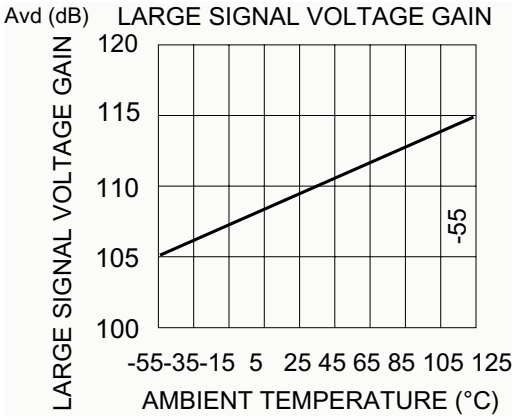


Figure 17. Large signal voltage gain



4 Typical Single-Supply Applications

Figure 18. AC coupled inverting amplifier

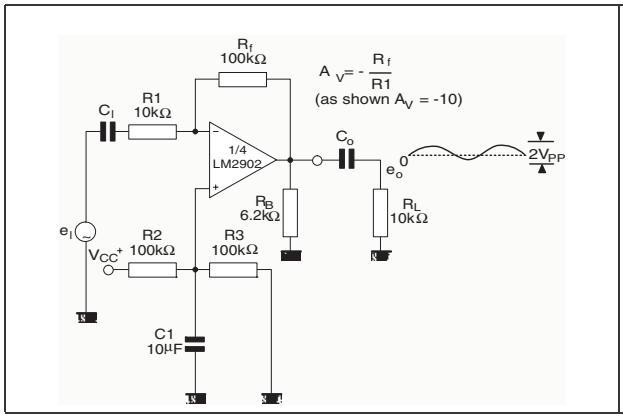


Figure 19. AC coupled non-inverting amplifier

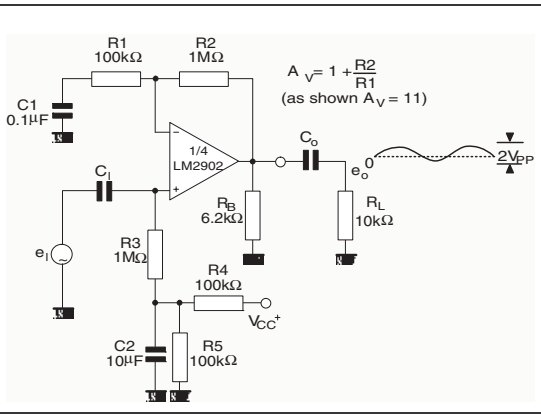


Figure 20. Non-inverting DC gain

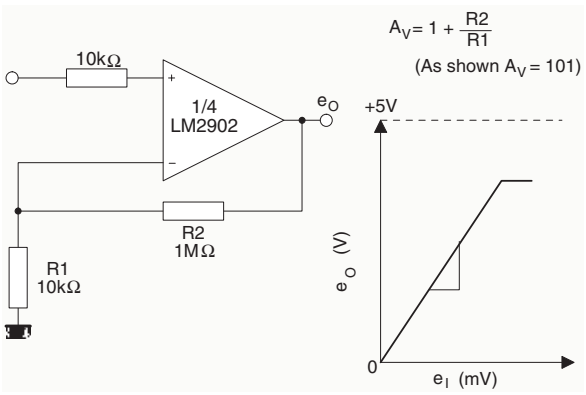


Figure 21. DC summing amplifier

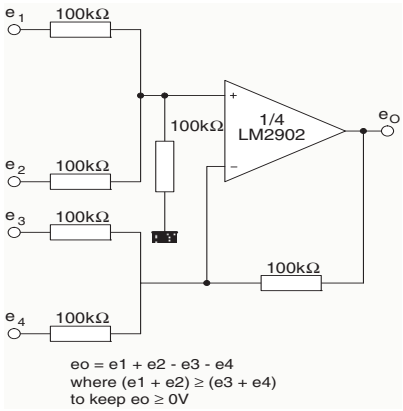


Figure 22. Active bandpass filter

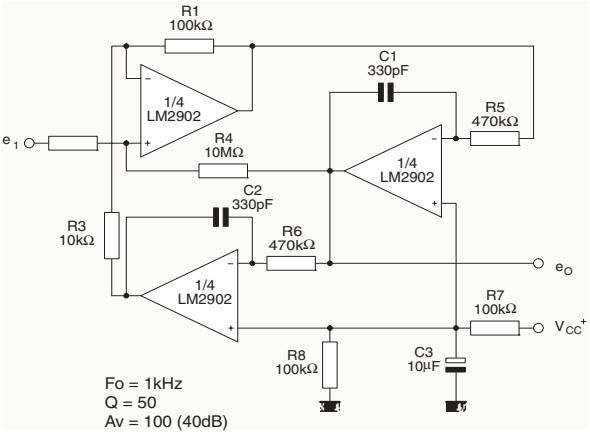


Figure 23. High input Z adjustable gain DC instrumentation amplifier

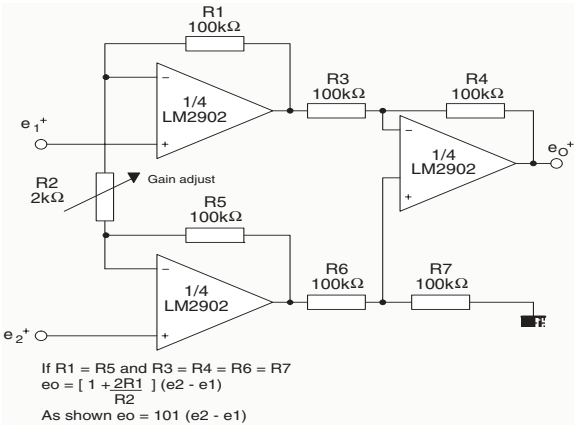


Figure 24. High input Z, DC differential amplifier

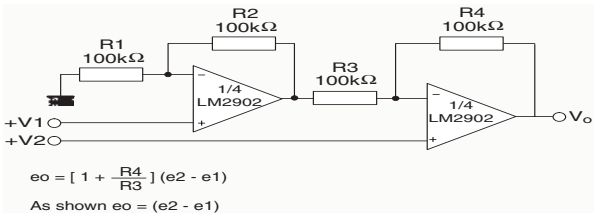


Figure 25. Low drift peak detector

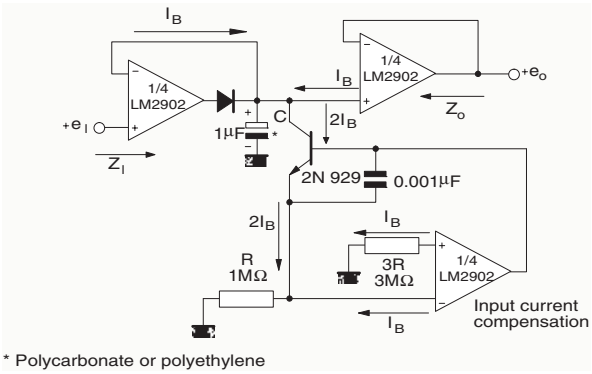
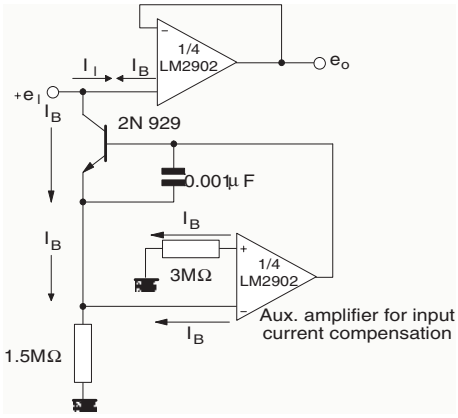


Figure 26. Using symmetrical amplifiers to reduce input current (general concept)



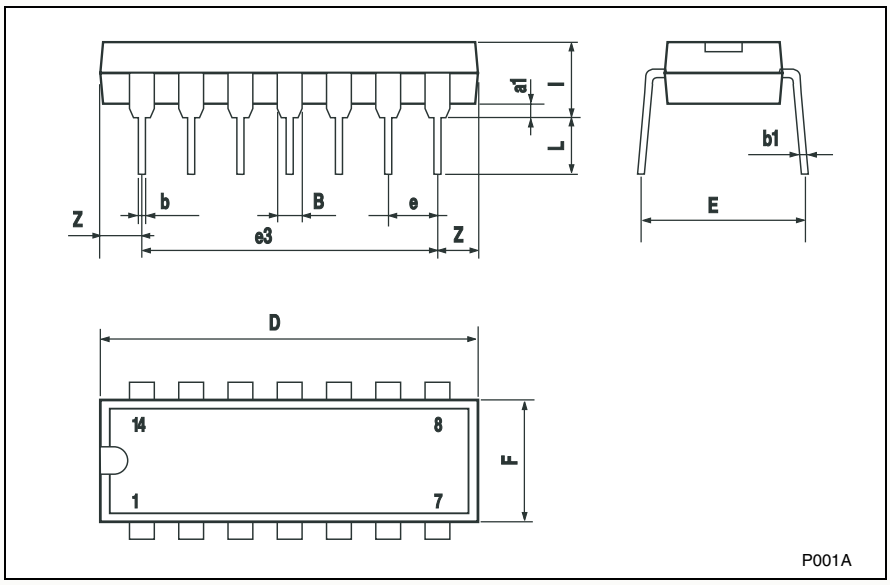
5 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.1 DIP14 package

Plastic DIP-14 MECHANICAL DATA

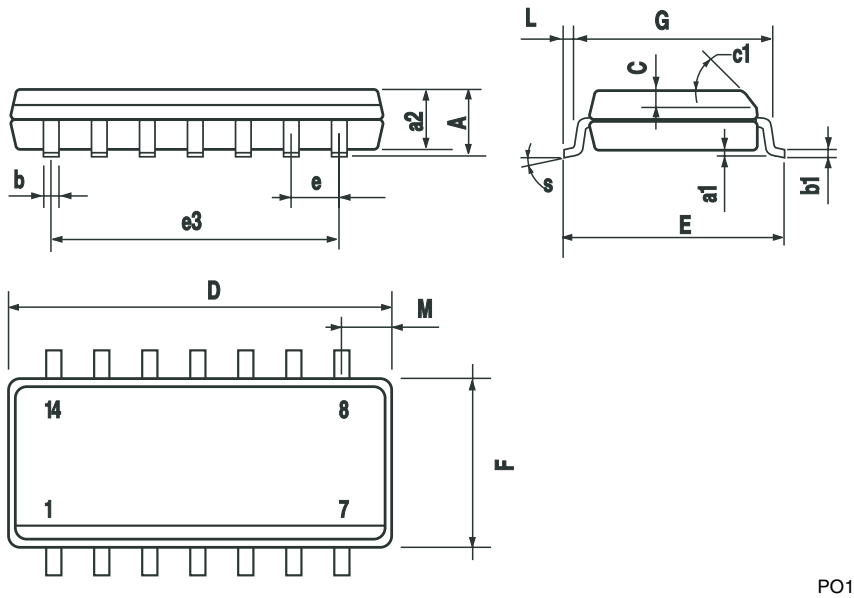
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



5.2 SO-14 package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45˚ (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8˚ (max.)					

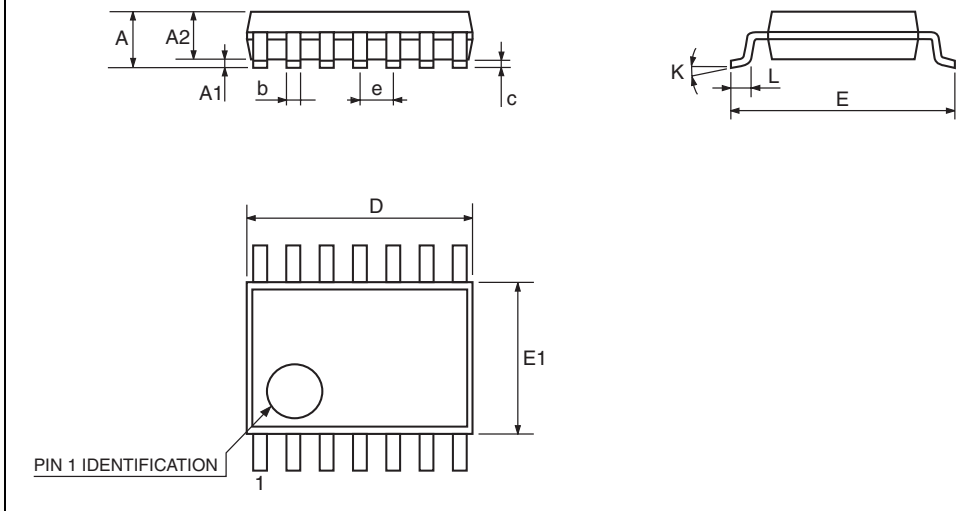


PO13G

5.3 TSSOP14 package

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



6 Revision History

Date	Revision	Changes
Sept. 2003	1	Initial release.
Nov. 2005	2	The following changes were made in this revision: – Table data reformatted for easier use in *Electrical Characteristics*. – Minor grammatical and formatting changes throughout.