L6316

4-CHANNEL LOW POWER PREAMPLIFIER

DATA BRIEF

1 FEATURES

- Dual Power Supplies of +5V, 10% and -3v, 6%
- Low Power consumption; 980 mW @ 800Mb/s (Single Head 100% Write mode duty cycle, Random pattern, Iw = 40mA, Max Ovs).
- Flip Chip package.L6316
- Differential Voltage Bias / Voltage Sense architecture. Current Bias available
- Programmable read input differential impedance.
- Selectable read path bandwidth from 200 to >600 MHz (Rmr=40Ω). (Parameter dependent on interconnect)
- Selectable LF corner (1, 2.5, 3.5 or 5.5 MHz with RMR=40Ω).
- Noise Figure of merit; 2.2 dB (Rmr=40Ω)
- MR bias voltage programmable from 70 to 225 mV nom. (5 bits) (7.2mA max).
- MR bias current programmable from 0.65 to 7.2 mA nom. (5 bits) (225mV max).
- Read input stage optimized for MR resistance from 20 to 70 Ohm.
- Programmable read voltage gain of 37, 40, 43, 46 dB Rmr = 40Ω, Rload = 100Ω
- Fully Differential write driver: Programmable overshoot amplitude (3bits) and duration (2bits).
- Write current rise/fall time with custom head and interconnect model 140 pS at 40 mA (10% to 90%) (Steady state to steady state)
- Write current amplitude programmable (5 bits) 0 to 62 mA (0-pk).
- Bi-directional 16-bit serial interface 2.5V and 3.3V CMOS compatible.
- 2-pin (RXW and TFI), 2 bits mode selection (WAKE, ENTFI).
- All control signals are 2.5 & 3.3V CMOS compatible.
- Analog buffered head voltage ABHV (gain of 5)
- Automatic digital MR resistance measurement (7 bits).
- Read head open detection, Read head shorted detection.
- Write head open or shorted to ground, Writer to Reader short, write data frequency too low detection.
- SAFEDETECT method for write fault detection.

Figure 1. Package

Flip Chip

Table 1. Order Codes

Part Number	Package
L6316	Flip Chip

- Low VCC or VEE supply & die over temperature detect, Analog Temperature Measurement.
- Fast write-to-read recovery 150nS (max) (same head).
- Head-to-head switch in read mode 1.5us (nom).
- Zero MR bias, very low power (43mW) idle mode with fast recovery to read mode 1.5us (nom).
- MR bias switching without overshoot for head protection.
- Read-to-Write switching 50nS (max) (same head).
- ESD diodes for MR head protection

2 DESCRIPTION

The L6316 is a BICMOS Silicon Germanium integrated circuit differential preamplifier. It is designed for use with four-terminal MR read and inductive write heads. In read mode, the device consists of a fully differential amplifier, offering; voltage or current bias, voltage-sense input, programmable input impedance, low noise and high bandwidth. In write mode, it includes fast current switching differential write drivers, which support data rates up to 1200 Mb/s.

This preamplifier provides programmable read voltage or current bias and write current (5 bit DACs for the read bias and for the write current), fault detection circuitry and servo track writing features. Read amplifier gain, low corner frequency, and write current wave shape are adjustable. The amplitude and duration of the overshoot are separately programmable through a 16-bit bi-directional serial interface (SEN, SDATA, and SCLK). The device operates from +5V and -3V supplies.

Figure 2. Preamplifier Block Diagram

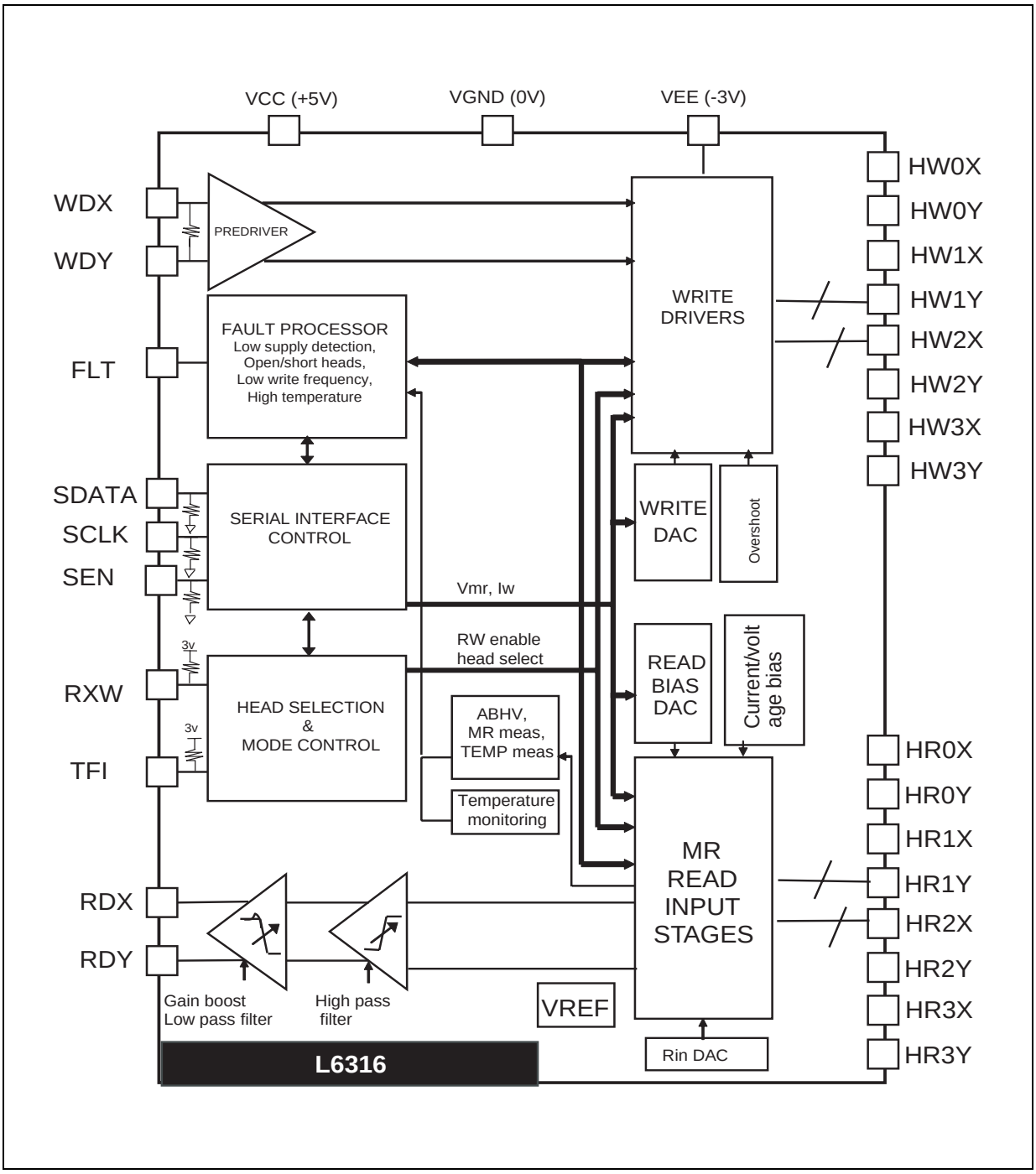
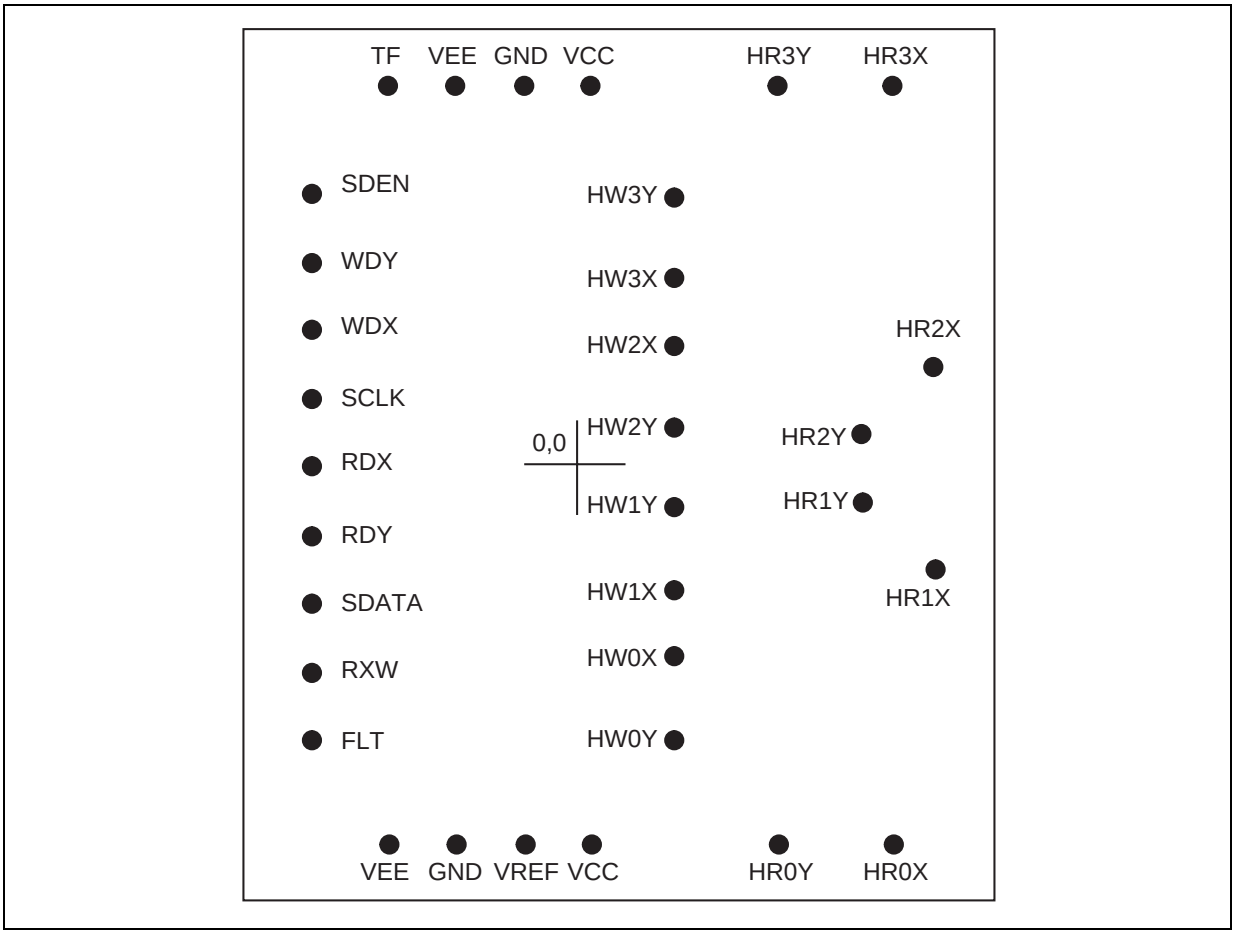


Figure 3. Flip Chip Pinout Diagram - BUMPS DOWN

Note: Minimum pad pitch = 204 um and pad opening (octagonal) = 70 um

Bump Sequence (see next table for coordinates)



Die dimensions:	X = 2192 ±20 um Y = 2686 ±20 um
Minimum distance between pads opening center to center:	204um
Wafer thickness:	500 ±20 um
Bump height:	90 ±15 um
Bump diameter:	120 ±15 um
Die center misalignment w.r.t original die center after cut:	38 um
Bump material if eutectic:	63% Tin, 37% Lead
Bump material if lead free:	96% Tin, 3.5% Silver, 0.5% Copper

Note: VREF PAD can be left floating or grounded. DO NOT CONNECT IT ANYWHERE ELSE.

Table 2. Bump Coordinates (bumps down, from center of die, dimensions in microns).

Pin name	X-coord (um)	Y-coord (um)	Pin name	X-coord (um)	Y-coord (um)
HR3Y	471	1140	VREF	-278	-1140
HR3X	775	1140	GND	-482	-1140
HW3Y	141.1	813.7	VEE	-686	-1140
HW3X	141.1	566.7	FLT	-890	-816
HW2X	141.1	362.7	RXW	-890	-612
HW2Y	141.1	115.7	SDATA	-890	-408
HR2Y	686	102	RDY	-890	-204
HR2X	890	252	RDX	-890	0
HR1X	890	-252	SCLK	-890	204
HR1Y	686	-102	WDX	-890	408
HW1Y	141.1	-115.7	WDY	-890	612
HW1X	141.1	-362.7	SDEN	-890	816
HW0X	141.1	-566.7	TFI	-686	1140
HW0Y	141.1	-813.7	VEE	-482	1140
HR0X	775	-1140	GND	-278	1140
HR0Y	471	-1140	VCC	-74	1140
VCC	-74	-1140	-	-	-

Note: VREF PAD can be left floating or grounded. DO NOT CONNECT IT ANYWHERE ELSE.

Table 3. Revision History

Date	Revision	Description of Changes
September 2004	1	First Issue in EDOCS dms.