FlashFlex51 MCU

SST89E52RC / SST89E54RC
SST89V52RC / SST89V54RC

Preliminary Specifications

FEATURES:

- **8-bit 8051-Compatible Microcontroller (MCU) with Embedded SuperFlash Memory**
  - Fully Software Compatible
  - Development Toolset Compatible
  - Pin-for-Pin Package Compatible
- **SST89E5xRC Operation**
  - 0 to 33MHz at 5V
- **SST89V5xRC Operation**
  - 0 to 25MHz at 3V
- **Total 512 Byte Internal RAM (256 Byte by default + 256 Byte enabled by software)**
- **Single Block SuperFlash EEPROM**
  - SST89E/V54RC: 16 KByte primary partition + 1 KByte secondary partition
  - SST89E/V52RC: 8 KByte primary partition + 1 KByte secondary partition
  - Primary Partition is divided into Four Pages
  - Secondary Partition has One Page
  - Individual Page Security Lock
  - In-System Programming (ISP)
  - In-Application Programming (IAP)
  - Small-Sector Architecture: 128-Byte Sector Size
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **Three High-Current Port 1 pins (16 mA each)**
- **Three 16-bit Timers/Counters**
- **Full-Duplex, Enhanced UART**
  - Framing error detection
  - Automatic address recognition
- **Eight Interrupt Sources at 4 Priority Levels**
- **Programmable Watchdog Timer (WDT)**
- **Four 8-bit I/O Ports (32 I/O Pins)**
- **Second DPTR register**
- **Low EMI Mode (Inhibit ALE)**
- **Standard 12 Clocks per cycle, the device has an option to double the speed to 6 clocks per cycle.**
- **TTL- and CMOS-Compatible Logic Levels**
- **Low Power Modes**
  - Power-down Mode with External Interrupt Wake-up
  - Idle Mode
- **Selectable Operation Clock**
  - Divide down to 1/4, 1/16, 1/256, or 1/1024th
- **Temperature Ranges:**
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)
- **Packages Available**
  - 40-pin PDIP
  - 44-lead PLCC
  - 44-lead TQFP
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST89E/V54RC and SST89E/V52RC are members of the FlashFlex51 family of 8-bit microcontroller products designed and manufactured with SST's patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for our customers.The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The device comes with 17/9 KByte of on-chip flash EEPROM program memory which is divided into 2 independent program memory partitions. The primary partition occupies 16/8 KByte of internal program memory space and the secondary partition occupies 1 KByte of internal program memory space.

The flash memory can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and firmware for SST's devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-system programming (ISP) operation. The devices are designed to be programmed in-system on the printed circuit board for maximum flexibility. The device is pre-programmed with an example of the bootstrap loader (BSL) in memory, demonstrating initial user program code loading or subsequent user code updating via an ISP operation. The sample BSL is for the user's reference only; SST does not guarantee its functionality. Chip-Erase operations will erase the pre-programmed sample code.

In addition to 17/9 KByte of SuperFlash EEPROM program memory on-chip, the device can address up to 64 KByte of external program memory. In addition to 512 x8 bits of on-chip RAM, up to 64 KByte of external RAM can be addressed.

SST's highly reliable, patented SuperFlash technology and memory cell architecture have a number of important advantages for designing and manufacturing flash EEPROMs. These advantages translate into significant cost and reliability benefits for our customers.

Preliminary Specifications

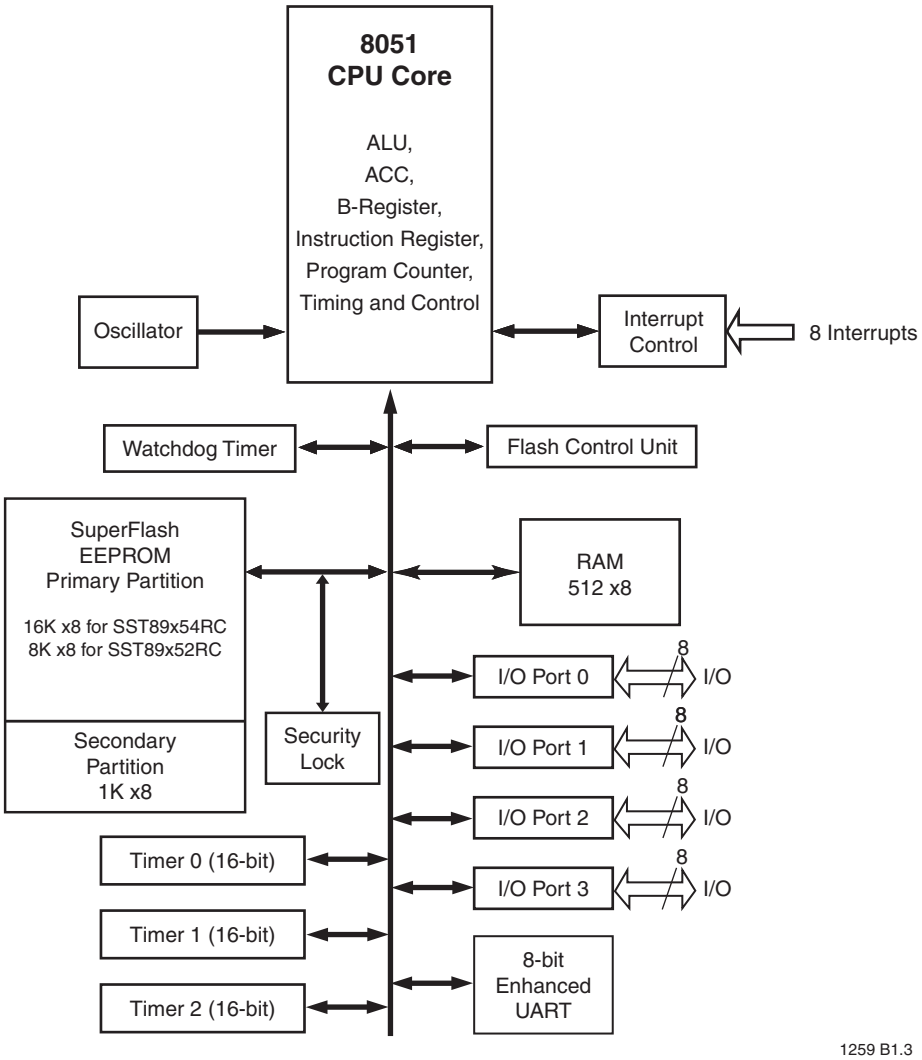
TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



1259 B1.3

2.0 PIN ASSIGNMENTS

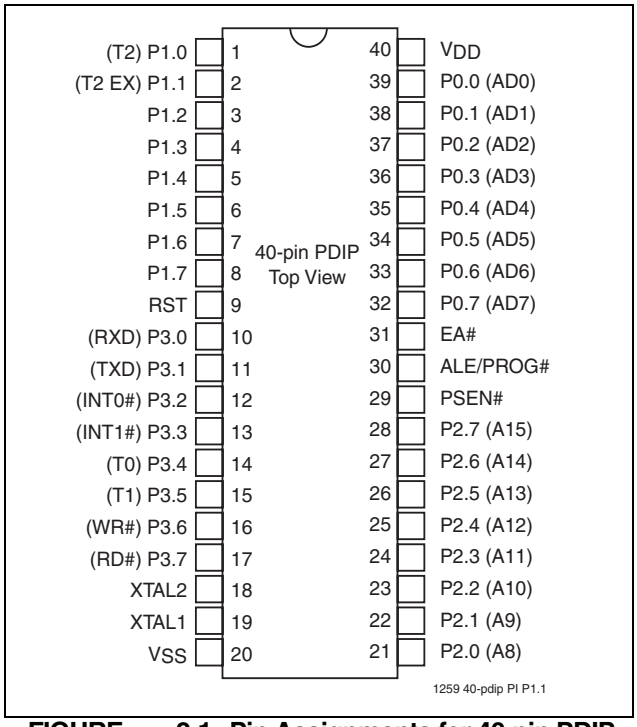


FIGURE 2-1: Pin Assignments for 40-pin PDIP

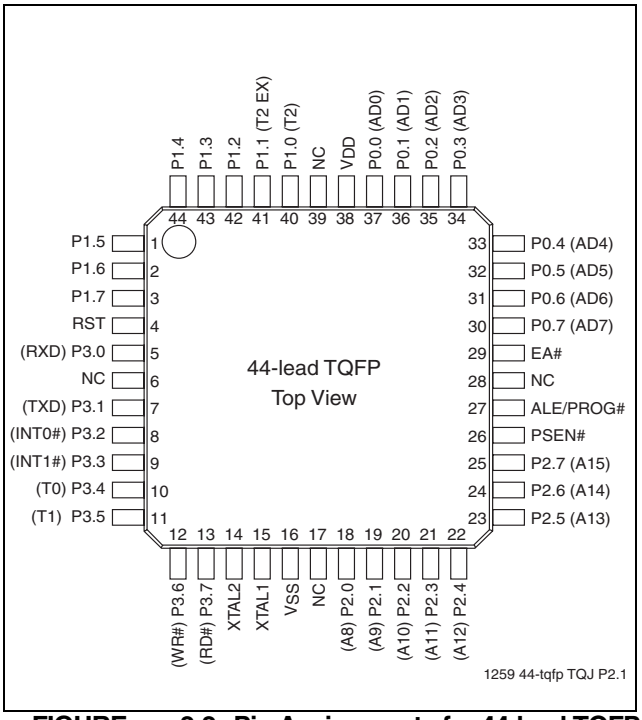


FIGURE 2-2: Pin Assignments for 44-lead TQFP

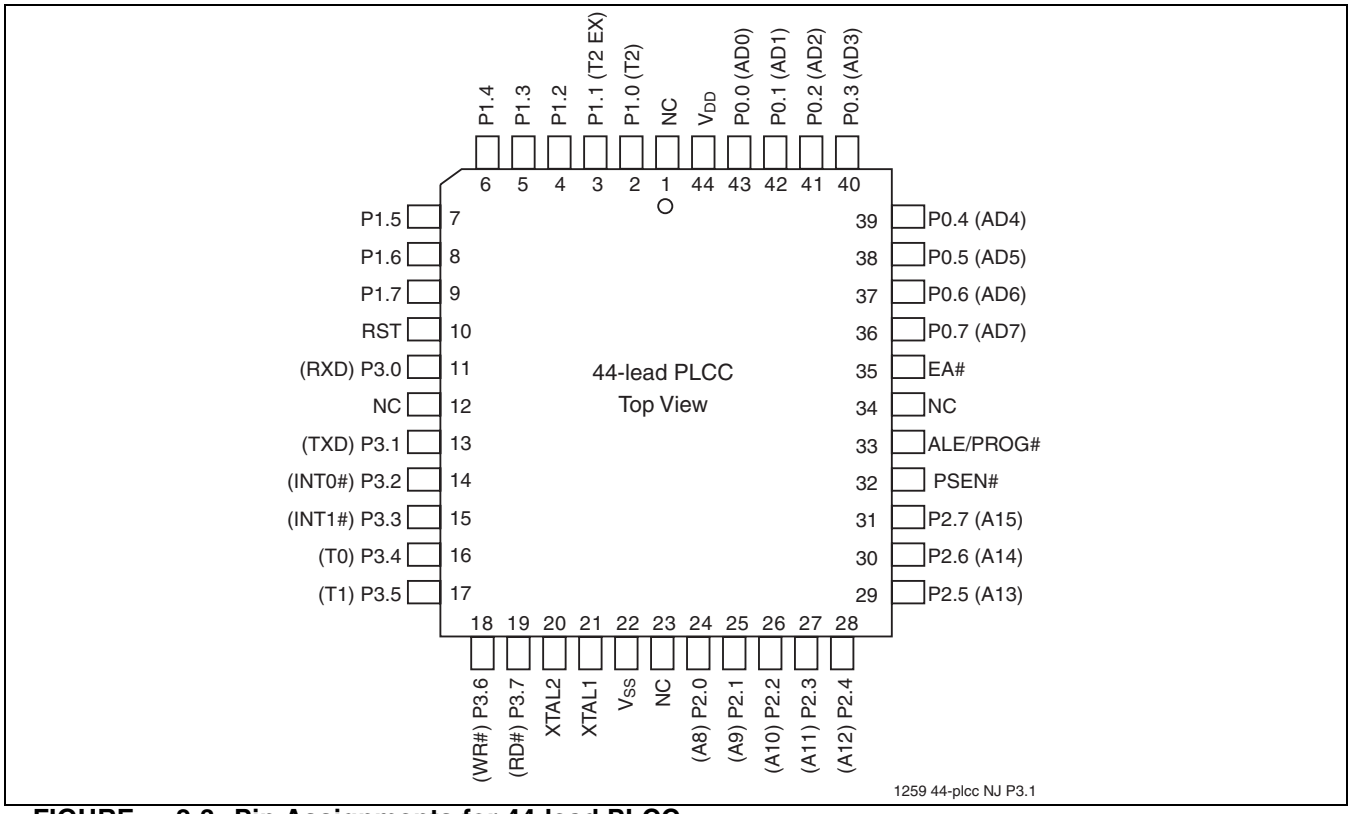


FIGURE 2-3: Pin Assignments for 44-lead PLCC

2.1 Pin Descriptions

TABLE 2-1: Pin Descriptions (1 of 2)

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P1[7:0]	I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, see Tables 12-6 and 12-7) because of the internal pull-ups. P1[5, 6, 7] have high current drive of 16 mA. Port 1 also receives the low-order address byte during the external host mode programming and verification.
P1[0]	I/O	**T2:** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]	I	**T2EX:** Timer/Counter 2 capture/reload trigger and direction control
P1[2]	I/O	**GPIO**
P1[3]	I/O	**GPIO**
P1[4]	I/O	**GPIO**
P1[5]	I/O	**GPIO**
P1[6]	I/O	**GPIO**
P1[7]	I/O	**GPIO**
P2[7:0]	I/O with internal pull-up	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, see Tables 12-6 and 12-7) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to '1's. Port 2 also receives the high-order address byte during the external host mode programming and verification.
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, see Tables 12-6 and 12-7) because of the internal pull-ups. Port 3 also receives the high-order address byte during the external host mode programming and verification.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0
P3[5]	I	**T1:** External count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe

TABLE 2-1: Pin Descriptions (Continued) (2 of 2)

Symbol	Type[1]	Name and Functions
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to external program. When the device is executing from internal program memory, PSEN# is inactive (High). When the device is executing code from external program memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to external data memory. A forced high-to-low input transition on the PSEN# pin while the RST input is continually held high for more than 10 machine cycles will cause the device to enter external host mode programming.
RST	I	**Reset:** While the oscillator is running, a "high" logic state on this pin for two machine cycles will reset the device. If the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held "high," the device will enter the external host mode, otherwise the device will enter the normal operation mode.
EA#	I	**External Access Enable:** EA# must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. EA# must be strapped to V_{DD} for internal program execution. However, Disable-Extern-Boot (See Section 8.0, "Security Lock") will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[2] of 12V. (See Section 12.0, "Electrical Specification")
ALE/PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[3] is emitted at a constant rate of 1/6 the crystal frequency[4] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled. (See "Auxiliary Register (AUXR)" in Section 3.5, "Special Function Registers")
NC	I/O	**No Connect**
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

T2-1.0 1259

1. I = Input; O = Output
2. It is not necessary to receive a 12V programming supply voltage during flash programming.
3. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
4. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.

3.0 MEMORY ORGANIZATION

The device has separate address spaces for program and data memory.

3.1 Program Flash Memory

There are two internal flash memory partitions in the device. The primary flash memory partition (Partition 0) has 16/8 KByte. The secondary flash memory partition (Partition 1) has 1 KByte. The total flash memory space of both partitions can be used as a contiguous code storage.

The 16K/8K x8 primary flash partition is organized as 128/64 sectors, each sector consists of 128 Bytes. The primary partition is divided into four logical pages as shown in Figure 3-2

The 1K x8 secondary flash partition is organized as 8 sectors, each sector consists also of 128 Bytes.

For both partitions, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the partition.

3.2 Data RAM Memory

The data RAM has 512 Bytes of internal memory. The first 256 Bytes are available by default. The second 256 Bytes are enabled by clearing the EXTRAM bit in the AUXR register. The RAM can be addressed up to 64 KByte for external data memory.

3.3 Expanded Data RAM Addressing

The SST89E/V5xRC have the capability of 512 Bytes of RAM. See Figure 3-1.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 256 Bytes (00H to FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section 3.5, “Special Function Registers”)

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

```
MOV     @R0, #data      ; R0 contains 90H
```

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

```
MOV     90H, #data      ; write data to P1
```

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 256 Bytes of memory is physically located on the chip and logically occupies the first 256 bytes of external memory (addresses 000H to FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

```
MOVX    @DPTR, A        ; DPTR contains 0A0H
```

DPTR points to 0A0H and data in “A” is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than FFH using the MOVX instruction will access external memory (0100H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up the 64K. Port 2 provides the high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary

read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 3-1 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

TABLE 3-1: External Data Memory RD#, WR# with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
AUXR	**ADDR < 0100H**	**ADDR >= 0100H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

T3-1.0 1259

1. Access limited to ERAM address within 0 to 0FFH.

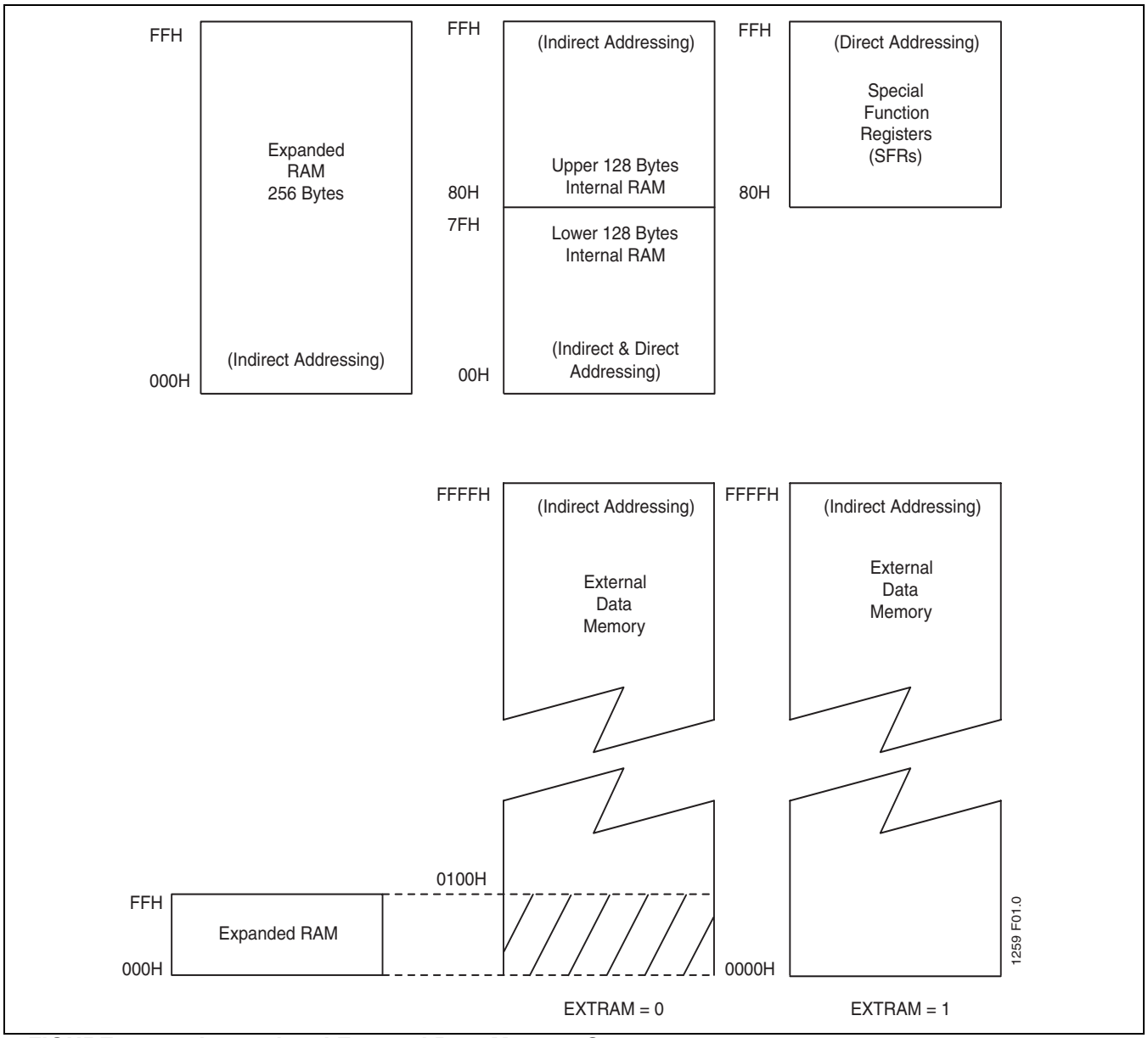


FIGURE 3-1: Internal and External Data Memory Structure

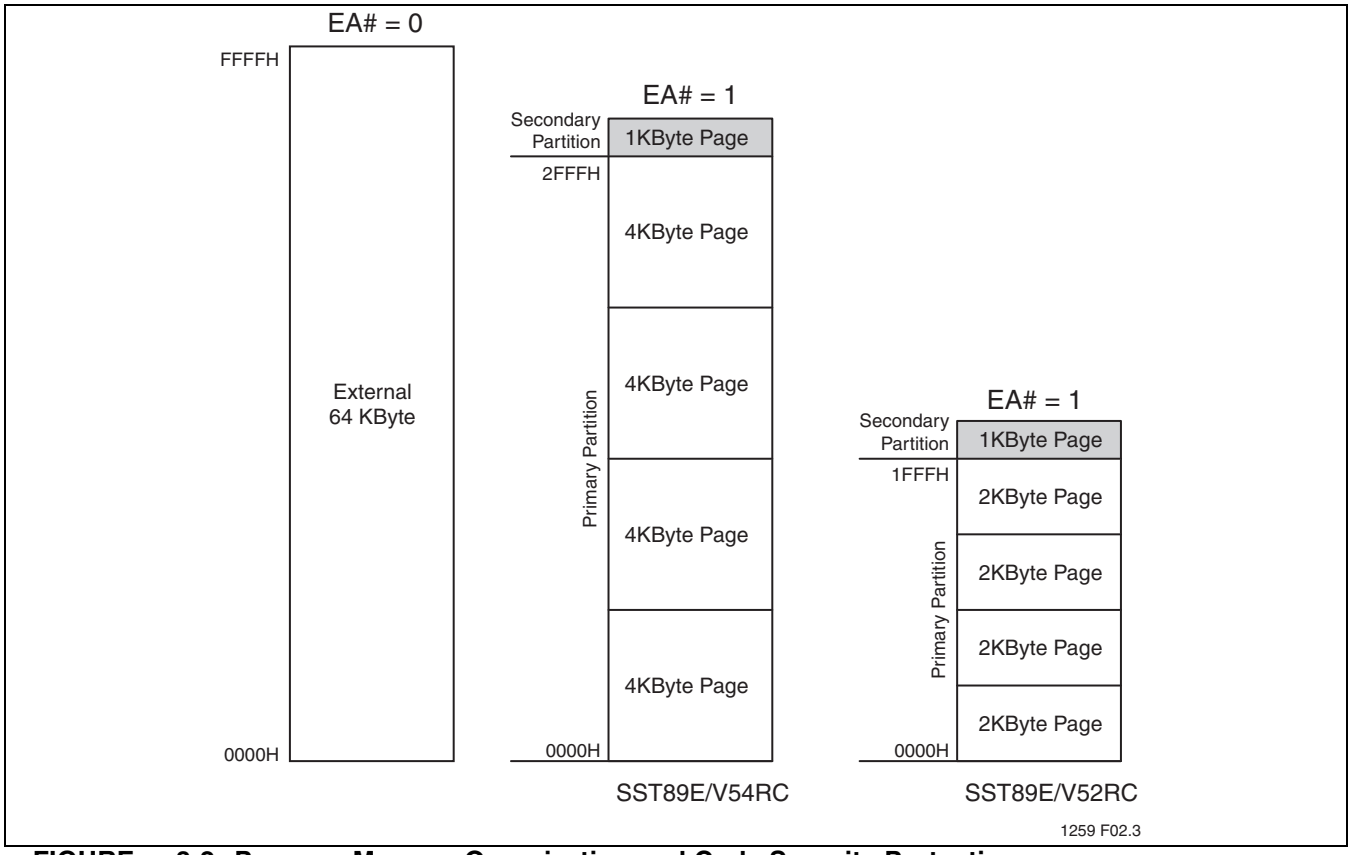


FIGURE 3-2: Program Memory Organization and Code Security Protection

3.4 Dual Data Pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS=0, DPTR0 is selected; when DPS=1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1. (See Figure 3-3)

3.5 Special Function Registers

Most of the unique features of the FlashFlex51 microcontroller family are controlled by bits in special function registers (SFRs) located in the SFR memory map shown in Table 3-2. Individual descriptions of each SFR are provided and reset values indicated in Tables 3-3 to 3-8.

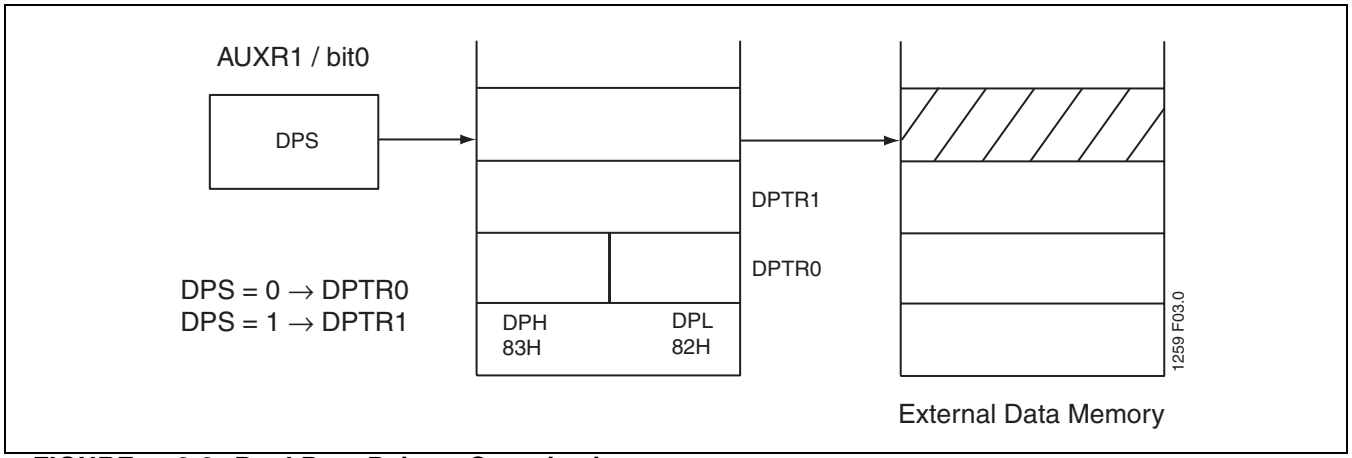


FIGURE 3-3: Dual Data Pointer Organization

TABLE 3-2: FlashFlex51 SFR Memory Map

	8 BYTES								
F8H	IPA[1]								FFH
F0H	B[1]							IPAH	F7H
E8H	IEA[1]								EFH
E0H	ACC[1]								E7H
D8H									DFH
D0H	PSW[1]					SPCR			D7H
C8H	T2CON[1]	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	WDTC[1]				SFIS1				C7H
B8H	IP[1]	SADEN						COSR	BFH
B0H	P3[1]	SFCF	SFCM	SFAL	SFAH	SFDT	SFST	IPH	B7H
A8H	IE[1]	SADDR							AFH
A0H	P2[1]	PMC	AUXR1						A7H
98H	SCON[1]	SBUF							9FH
90H	P1[1]							SFIS0	97H
88H	TCON[1]	TMOD	TL0	TL1	TH0	TH1	AUXR		8FH
80H	P0[1]	SP	DPL	DPH		WDTD		PCON	87H

T3-2.1 1259

1. Bit addressable SFRs

TABLE 3-3: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE[1]	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IEA[1]	Interrupt Enable A	E8H	-	EWD	-	-	-	-	-	-	x0xxxxxxb
IP[1]	Interrupt Priority Reg	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	x0000000b
IPH	Interrupt Priority Reg High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000b
IPA[1]	Interrupt Priority Reg A	F8H	-	PWD	-	-	-	-	-	-	x0xxxxxxb
IPAH	Interrupt Priority Reg A High	F7H	-	PWDH	-	-	-	-	-	-	x0xxxxxxb
PCON	Power Control	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00x10000b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx00b
AUXR1	Auxiliary Reg 1	A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0b
PMC	Power Management Control Register	A1H	-	-	WDU	TCT	TCT2	PB2	PB1	UART	xx000000b

T3-3.1 1259

1. Bit Addressable SFRs

TABLE 3-4: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configuration	B1H	CMD_Status	IAPEN	-	HWIAP	-	SFST_SEL			01x0x000b
SFCM	SuperFlash Command	B2H	-	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H SFST_SEL= 0H	Manufacturer's ID								BFH
		SFST_SEL= 1H	Device ID0 (F7H indicates Device ID1 is real ID)								
		SFST_SEL= 2H	Device ID1								
		SFST_SEL= 3H	Boot Vector								
		SFST_SEL= 4H	-	-	-	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0	xxx11111b
		SFST_SEL= 5H	X	Boot From Zero	Boot-From-User-Vector	Enable Clock-Double	Disable-Extern-Host-Cmd	Disable-Extern-MOVC	Disable-Extern-Boot	Disable-Extern-IAP	x1111111b

T3-4.0 1259

TABLE 3-5: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC[1]	Watchdog Timer Control	C0H	-	WDTON	WDFE	-	WDRE	WDTS	WDT	SWDT	x0000000b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

T3-5.0 1259

1. Bit Addressable SFRs

TABLE 3-6: Feed Sequence SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	Reset Value
SFIS0	Sequence Reg 0	97H	(Write only)	00H
SFIS1	Sequence Reg 1	C4H	(Write only)	00H

T3-6.0 1259

TABLE 3-7: Timer/Counters SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer / Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
T2MOD#	Timer2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

T3-7.0 1259

1. Bit Addressable SFRs

TABLE 3-8: Interface SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
SBUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
SCON[1]	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SADDR	Slave Address	A9H	SADDR[7:0]								00H
SADEN	Slave Address Mask	B9H	SADEN[7:0]								00H
P0[1]	Port 0	80H	P0[7:0]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
P2[1]	Port 2	A0H	P2[7:0]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH

T3-8.1 1259

1. Bit Addressable SFRs

TABLE 3-9: Clock Option SFR

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB						LSB	Reset Value
COSR	Clock Option Register	BFH	-	-	-	-	COEN	CO_REL	CO_IN	0x00000b

SuperFlash Configuration Register (SFCF)

Location	7	6	5	4	3	2	1	0	Reset Value
B1H	CMD_ Status	IAPEN	-	HWIAP	-	SFST_SEL			01x0x000b

Symbol	Function
CMD_Status	IAP Command Completion Status 0: IAP command is ignored 1: IAP command is completed fully
IAPEN	IAP Enable Bit 0: Disable all IAP commands (Commands will be ignored) 1: Enable all IAP commands
HWIAP	Boot Status Flag 0: System boots up without special pin configuration setup 1:System boots up with both P1[0] and P1[1] pins in logic low state curing reset. (See Figure 9-3.)
SFST_SEL	Provide index to read back information when read to SFST register is executed. (See , “SuperFlash Status Register (SFST) (Read Only Register)” on page 18 for detailed settings.)

SuperFlash Command Register (SFCM)

Location	7	6	5	4	3	2	1	0	Reset Value
B2H	-	FCM6	FCM5	FCM4	FCM3	FCM2	FCM1	FCM0	00H

Symbol	Function
-	Reserved
FCM[6:0]	Flash operation command

000_0001b Chip-Erase
000_1011b Sector-Erase
000_1101b Partition0-Erase
000_1100b Byte-Verify[1]
000_1110b Byte-Program
000_0011b Secure-Page
Page-Level Security Commands
SFAH=90H; Secure-Page0
SFAH=91H; Secure-Page1
SFAH=92H; Secure-Page2
SFAH=93H; Secure-Page3
SFAH=94H; Secure-Page4
000-0101b Secure-Chip
Chip-Level Security Commands
SFAH=B0H; Disable-Extern-IAP
SFAH=B1H; Disable-Extern-Boot
SFAH=B2H; Disable-Extern-MOVC
SFAH=B3H; Disable-Extern-Host-Cmd
000-1000b Boot Options
Boot Option Setting Commands
SFAH=E0H; Enable-Clock-Double
SFAH=E1H; Boot-From-User-Vector
SFAH=E2H; Boot-From-Zero
000-1001b Set-User-Boot-Vector
All other combinations are not implemented, and reserved for future use.

1. Byte-Verify has a single machine cycle latency and will not generate any INT1# interrupt regardless of FIE.

SuperFlash Address Registers (SFAL)

Location	7	6	5	4	3	2	1	0	Reset Value
B3H	SuperFlash Low Order Byte Address Register								00H

Symbol	Function
SFAL	Mailbox register for interfacing with flash memory block. (Low order address register).

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register).

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SuperFlash Status Register								xxxxx0xxb

Symbol	Function
SFST	This is a read-only register. The read-back value is indexed by SFST_SEL in the SuperFlash Configuration Register (SFCF). SFST_SEL=0H: Manufacturer's ID 1H: Device ID0 = F7H 2H: Device ID1 = Device ID (Refer to Table 4-1 on page 27) 3H: Boot Vector 4H: Page-Security bit setting 5H: Chip-Level Security bit setting and Boot Options

Interrupt Enable (IE)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00H

Symbol	Function
EA	Global Interrupt Enable. 0 = Disable 1 = Enable
ET2	Timer 2 Interrupt Enable.
ES	Serial Interrupt Enable.
ET1	Timer 1 Interrupt Enable.
EX1	External 1 Interrupt Enable.
ET0	Timer 0 Interrupt Enable.
EX0	External 0 Interrupt Enable.

Interrupt Enable A (IEA)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	EWD	-	-	-	-	-	-	x0xxxxxxb

Symbol	Function
EWD	Watchdog Interrupt Enable. 1 = Enable the interrupt 0 = Disable the interrupt

Preliminary Specifications

Interrupt Priority (IP)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	x0000000b

Symbol	Function
PT2	Timer 2 interrupt priority bit.
PS	Serial Port interrupt priority bit.
PT1	Timer 1 interrupt priority bit.
PX1	External interrupt 1 priority bit.
PT0	Timer 0 interrupt priority bit.
PX0	External interrupt 0 priority bit.

Interrupt Priority High (IPH)

Location	7	6	5	4	3	2	1	0	Reset Value
B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000b

Symbol	Function
PT2H	Timer 2 interrupt priority bit high.
PSH	Serial Port interrupt priority bit high.
PT1H	Timer 1 interrupt priority bit high.
PX1H	External interrupt 1 priority bit high.
PT0H	Timer 0 interrupt priority bit high.
PX0H	External interrupt 0 priority bit high.

Interrupt Priority A (IPA)

Location	7	6	5	4	3	2	1	0	Reset Value
F8H	-	PWD	-	-	-	-	-	-	x0xxxxxxb

Symbol	Function
PWD	Watchdog interrupt priority bit.

Interrupt Priority A High (IPAH)

Location	7	6	5	4	3	2	1	0	Reset Value
F7H	-	PWDH	-	-	-	-	-	-	x0xxxxxxb

Symbol	Function
PWDH	Watchdog interrupt priority bit high.

Auxiliary Register (AUXR)

Location	7	6	5	4	3	2	1	0	Reset Value
8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx10b

Symbol	Function
EXTRAM	Internal/External RAM access 0: Internal Expanded RAM access within range of 00H to FFH using MOVX @Ri / @DPTR. Beyond 100H, the MCU always accesses external data memory. For details, refer to Section 3.3, “Expanded Data RAM Addressing” . 1: External data memory access.
AO	Disable/Enable ALE 0: ALE is emitted at a constant rate of 1/3 the oscillator frequency in 6 clock mode, 1/6 f_{OSC} in 12 clock mode. 1: ALE is active only during a MOVX or MOVC instruction.

Auxiliary Register 1 (AUXR1)

Location	7	6	5	4	3	2	1	0	Reset Value
A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0b

Symbol	Function
GF2	General purpose user-defined flag
DPS	DPTR registers select bit 0: DPTR0 is selected. 1: DPTR1 is selected.

Sequence Register 0 (SFIS0)

Location	7	6	5	4	3	2	1	0	Reset Value
97H	(Write only)								N/A

Symbol	Function
SFIS0	Register used with SFIS1 to provide a feed sequence to validate writing to WDTC and SFCM. Without a proper feed sequence, writing to SFCM will be ignored and writing to WDTC in Watchdog mode will cause an immediate Watchdog reset.

Sequence Register 1 (SFIS1)

Location	7	6	5	4	3	2	1	0	Reset Value
C4H	(Write only)								N/A

Symbol	Function
SFIS1	Register used with SFIS0 to provide a feed sequence to validate writing to WDTC and SFCM.

Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	-	WDTON	WDFE	-	WDRE	WDTS	WDT	SWDT	x0000000b

Symbol	Function
WDTON	Watchdog timer start control bit (Used in Watchdog mode) 0: Watchdog timer can be started or stopped freely during Watchdog mode. 1: Start Watchdog timer; bit cannot be cleared by software.
WDFE	Watchdog feed sequence error flag 0: Watchdog feed sequence error has not occurred. 1: Due to an incorrect feed sequence before writing to WDTC in Watchdog mode, the hardware entered Watchdog reset and set this flag to “1.” This is for software to detect whether the Watchdog reset was caused by timer expiration or an incorrect feed sequence.
WDRE	Watchdog timer reset enable. 0: Disable Watchdog timer reset. 1: Enable Watchdog timer reset.
WDTS	Watchdog timer reset flag. 0: External hardware reset or power-on reset clears the flag. Flag can also be cleared by writing a 1. Flag survives if chip reset happened because of Watchdog timer overflow. 1: Hardware sets the flag on watchdog overflow.
WDT	Watchdog timer refresh. 0: Hardware resets the bit when refresh is done. 1: Software sets the bit to force a Watchdog timer refresh.
SWDT	Start Watchdog timer. 0: Stop WDT. 1: Start WDT.

Clock Option Register (COSR)

Location	7	6	5	4	3	2	1	0	Reset Value
BFH	-	-	-	-	COEN	CO_SEL		CO_IN	00H

Symbol	Function
COEN	Clock Divider Enable 0: Disable Clock Divider 1: Enable Clock Divider
CO_SEL	Clock Divider Selection 00b: 1/4 clock source 01b: 1/16 clock source 10b: 1/256 clock source 11b: 1/1024 clock source
CO_IN	Clock Source Selection 0b: Select clock from 1x clock 1b: Select clock from 2x clock The default value of this bit is set during Power-on reset by copying from Enable_Clock_Double_i non-volatile bit setting. CO_IN can be changed during normal operation to select the double clock option. If the clock source is a 1x clock, the clock divider exports 1/4, 1/16, 1/256, or 1/1024 of the input clock. If the clock source is a 2x clock, the clock divider exports 1/2, 1/8, 1/128, or 1/512 of the input clock.

Power Management Control Register (PMC)

Location	7	6	5	4	3	2	1	0	Reset Value
A1H	-	-	WDU	TCT	TCT2	PB2	PB1	UART	xx000000b

Symbol	Function
WDU	Watchdog Timer Clock Control 0:The clock for the Watchdog timer is running 1:The clock for the Watchdog timer is stopped
TCT	Timer 0/1 Clock Control 0:The Timer 0/1 logic is running 1:The Timer 0/1 logic is stopped
TCT2	Timer 2 Clock Control 0:The Timer 2 logic is running 1:The Timer 2 logic is stopped
PB2	Further Power Control 2 0:The PB2 logic is running 1:The PB2 logic is stopped
PB1	Further Power Control 1 0:The PB1 logic is running 1:The PB1 logic is stopped Power consumption can be decreased by setting both PB2 and PB1 to 1.
UART	UART Clock Control 0:The UART logic is running 1:The UART logic is stopped

Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
85H	Watchdog Timer Data/Reload								00H

Power Control Register (PCON)

Location	7	6	5	4	3	2	1	0	Reset Value
87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00x10000b

Symbol	Function
SMOD1	Double Baud rate bit. If SMOD1 = 1, Timer 1 is used to generate the baud rate, and the serial port is used in modes 1, 2, and 3.
SMOD0	FE/SM0 Selection bit. 0: SCON[7] = SM0 1: SCON[7] = FE,
POF	Power-on reset status bit, this bit will not be affected by any other reset. POF should be cleared by software. 0: No Power-on reset. 1: Power-on reset occurred
GF1	General-purpose flag bit.
GF0	General-purpose flag bit.
PD	Power-down bit, this bit is cleared by hardware after exiting from power-down mode. 0: Power-down mode is not activated. 1: Activates Power-down mode.
IDL	Idle mode bit, this bit is cleared by hardware after exiting from idle mode. 0: Idle mode is not activated. 1: Activates idle mode.

Serial Port Control Register (SCON)

Location	7	6	5	4	3	2	1	0	Reset Value
98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b

Symbol	Function
FE	Set SMOD0 = 1 to access FE bit. 0: No framing error 1: Framing Error. Set by receiver when an invalid stop bit is detected. This bit needs to be cleared by software.
SM0	SMOD0 = 0 to access SM0 bit. Serial Port Mode Bit 0
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate[1]
0	0	0	Shift Register	f_{OSC}/6 (6 clock mode) or f_{OSC}/12 (12 clock mode)
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	f_{OSC}/32 or f_{OSC}/16 (6 clock mode) or f_{OSC}/64 or f_{OSC}/32 (12 clock mode)
1	1	3	9-bit UART	Variable

1. f_{OSC} = oscillator frequency

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a given or broadcast address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be 0.
REN	Enables serial reception. 0: to disable reception. 1: to enable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission, Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

4.0 FLASH MEMORY PROGRAMMING

The device internal flash memory can be programmed or erased using In-Application Programming (IAP).

4.1 Product Identification

The Read-ID command accesses the Signature Bytes that identify the device and the manufacturer as SST. External programmers primarily use these Signature Bytes in the selection of programming algorithms.

TABLE 4-1: Product Identification

	Address	Data
Manufacturer's ID	30H	BFH
Device ID	31H	F7H
Device ID (extended)		
SST89E54RC	32H	43H
SST89V54RC	32H	4BH
SST89E52RC	32H	42H
SST89V52RC	32H	4AH

T4-1.1 1259

4.2 In-Application Programming

The device offers 17/9/5 KByte of in-application programmable flash memory. During In-Application Programming (IAP), the CPU of the microcontroller enters STOP mode. Upon completion of IAP, the CPU will be released to resume program execution. The mailbox registers (SFST, SFCM, SFAL, SFAH, SFDT and SFCF) located in the special function register (SFR), control and monitor the device's Erase and Program processes.

Table 4-3 outlines the commands and their associated mailbox register settings.

4.2.1 IAP Mode Clock Source

During IAP mode, both the CPU core and the flash controller unit are driven off the external clock. However, an internal oscillator will provide timing references for Program and Erase operations. The internal oscillator is only turned on when required, and is turned off as soon as the flash operation is completed.

4.2.2 IAP Enable Bit

The IAP enable bit, SFCF[6], enables In-Application programming mode. Until this bit is set, all flash programming IAP commands will be ignored.

4.2.3 IAP Mode Commands

In order to protect the flash memory against inadvertent writes during unstable power conditions, all IAP commands need the following feed sequence to validate the execution of commands.

Feed Sequence

1. Write A2H to SFIS0 (097H)
2. Write DFH to SFIS1 (0C4H)
3. Then write IAP command to SFCM (0B2H)

Note: Above commands should be executed in sequence without interference from other instructions.

All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the SFCM register will initiate all of the operations. A feed sequence is required prior to issuing commands through SFCM. Without the feed sequence all IAP commands are ignored. Sector-Erase, Byte-Program, and Byte-Verify commands will not be carried out on a specific memory page if the security locks are enabled on the memory page.

The Byte-Program command is to update a byte of flash memory. If the original flash byte is not FFH, it should first be erased with an appropriate Erase command. **Warning: Do not attempt to write (Program or Erase) to a sector that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.**

4.2.3.1 Chip-Erase

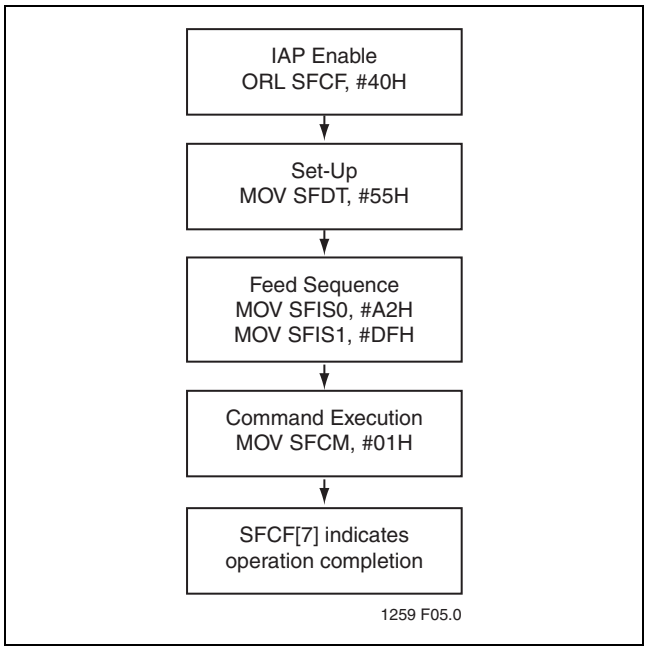
The Chip-Erase command erases all bytes in both memory partitions. This command is only allowed when EA#=0 (external memory execution).

Chip-Erase ignores the Security setting status and will erase all settings on all pages and the different chip-level security restrictions, returning the device to its Unlocked state. The Chip-Erase command will also erase the boot vector setting. Upon completion of Chip-Erase command, the chip will boot from the default setting. See Table 4-2 for the default boot vector setting.

TABLE 4-2: Default Boot Vector Settings

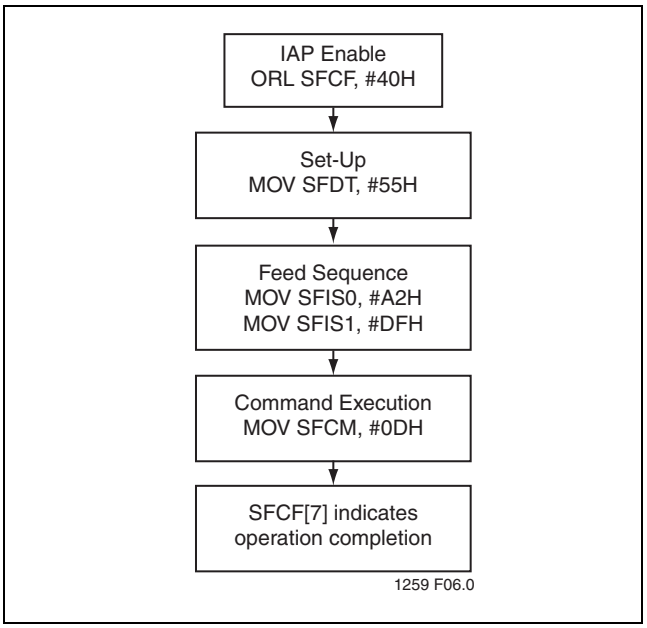
Device	Address
SST89E54RC	4000H
SST89V54RC	4000H
SST89E52RC	2000H
SST89V52RC	2000H

T4-2.1 1259



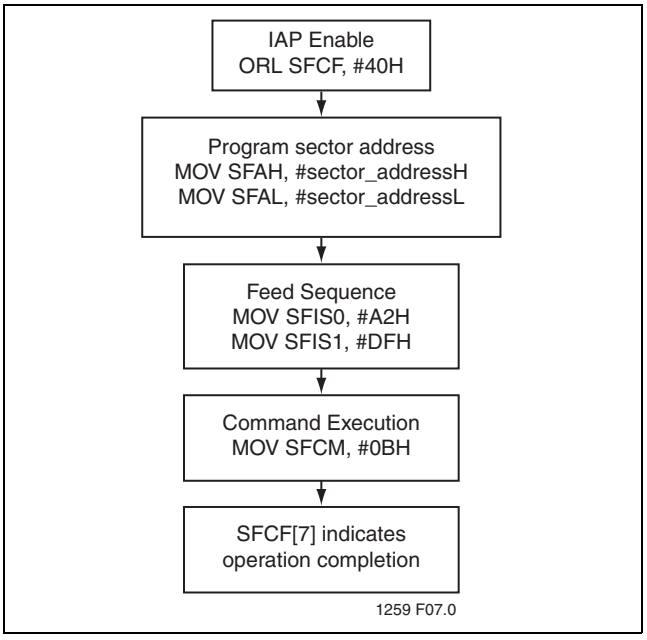
4.2.3.2 Partition0-Erase

The Partition0-Erase command erases all bytes in memory partition 0. All security bits associated with Page0-3 are also reset.



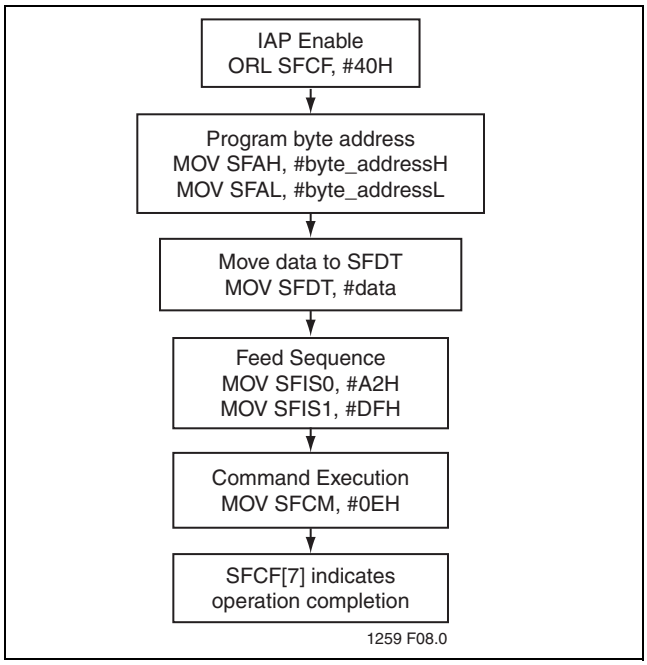
4.2.3.3 Sector-Erase

The Sector-Erase command erases all of the bytes in a sector. The sector size for the flash memory blocks is 128 Bytes. The selection of the sector to be erased is determined by the contents of SFAH and SFAL.



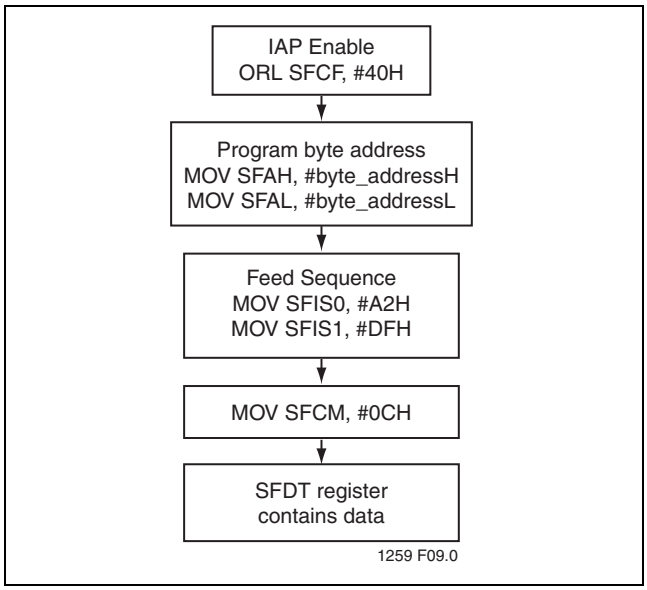
4.2.3.4 Byte-Program

The Byte-Program command programs data into a single byte. The address is determined by the contents of SFAH and SFAL. The data byte is in SFDT.



4.2.3.5 Byte-Verify

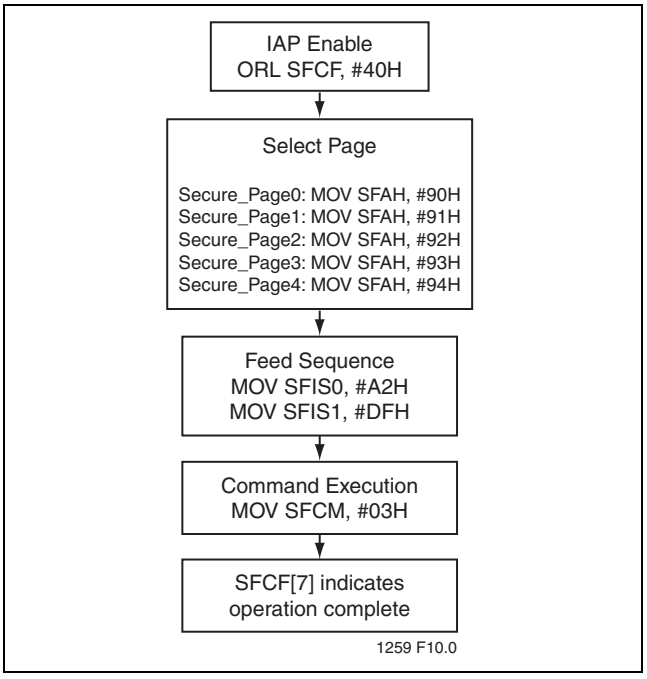
The Byte-Verify command allows the user to verify that the device has correctly performed an Erase or Program command. Byte-Verify command returns the data byte in SFDT if the command is successful. The previous flash operation has to be fully completed before a Byte-Verify command can be issued.



4.2.3.6 Secure-Page0, Secure-Page1, Secure-Page2, Secure-Page3, and Secure-Page4

Secure-Page0, Secure-Page1, Secure-Page2, Secure-Page3, and Secure-Page4 commands are used to program the page security bits. Upon completion of any of these commands, the page security options will be updated immediately.

Page security bits previously in un-programmed state can be programmed by these commands. The factory setting for these bits is all “1”s which indicates the pages are not security locked.



4.2.3.7 Enable-Clock-Double

Enable-Clock-Double command is used to make the MCU run at 6 clocks per machine cycle. The standard (default) is 12 clocks per machine cycle (i.e. clock double command disabled).

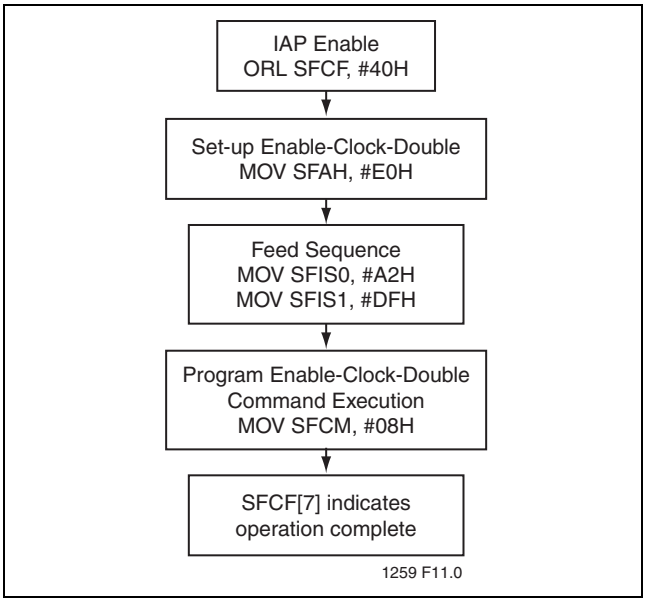


TABLE 4-3: IAP COMMANDS

Operation	SFCM [6:0]	SFDT [7:0]	SFAH [7:0]	SFAL [7:0]
Chip-Erase	01H	55H	X	X
Partition0-Erase	0DH	55H	X	X
Sector-Erase	0BH	X	AH	AL
Byte-Program	0EH	DI	AH	AL
Byte-Verify (Read)	0CH	DO	AH	AL
Secure-Page0	03H	X	90H	X
Secure-Page1	03H	X	91H	X
Secure-Page2	03H	X	92H	X
Secure-Page3	03H	X	93H	X
Secure-Page4	03H	X	94H	X
Disable-Extern-IAP	05H	X	B0H	X
Disable-Extern-Boot	05H	X	B1H	X
Disable-Extern-MOVC	05H	X	B2H	X
Disable-Extern-Host-Cmd	05H	X	B3H	X
Enable-Clock-Double	08H	X	E0H	X
Boot-From-User-Vector	08H	X	E1H	X
Boot-From-Zero	08H	X	E2H	X
Set-User-Boot-Vector	09H	DI	F0H	X

T4-3.0 1259

Note: V_{IL} = Input Low Voltage; V_{IH} = Input High Voltage; V_{IH1} = Input High Voltage (XTAL, RST); X = Don't care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output.

4.3 In-System Programming

SST provides an example In-System Programming (ISP) solution for this device series. The example bootstrap loader is to be pre-programmed into Partition1, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation.

Users can either use the SST ISP solution or develop a customized ISP solution. Customized ISP firmware can be pre-programmed into a user-defined boot vector. See Section "Boot Sequence" on page 40 for details.

5.0 TIMERS/COUNTERS

5.1 Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

5.2 Timer Set-up

Refer to Table 3-7 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

TABLE 5-1: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

T5-1.0 1259

1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

TABLE 5-2: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

T5-2.0 1259

1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

TABLE 5-3: Timer/Counter 2

	Mode	T2CON	
		Internal Control[1]	External Control[2]
Used as Timer	16-bit Auto-Reload	00H	08H
	16-bit Capture	01H	09H
	Baud rate generator receive and transmit same baud rate	34H	36H
	Receive only	24H	26H
	Transmit only	14H	16H
Used as Counter	16-bit Auto-Reload	02H	0AH
	16-bit Capture	03H	0BH

T5-3.0 1259

1. Capture/Reload occurs only on timer/counter overflow.
2. Capture/Reload occurs on timer/counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

5.3 Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure Timer/Counter 2 as a clock generator, bit C/#T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

n = 2 (in 6 clock mode)
4 (in 12 clock mode)

Where (RCAP2H, RCAP2L) = the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will not be the same.

6.0 SERIAL I/O

6.1 Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

6.1.1 Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 6-1). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 6-2 and Figure 6-3).

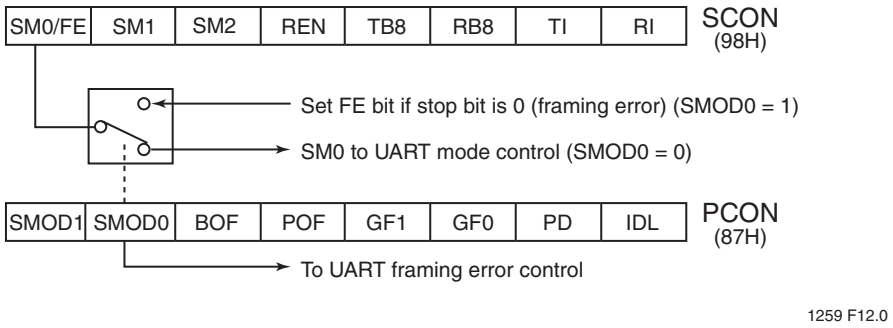


FIGURE 6-1: Framing Error Block Diagram

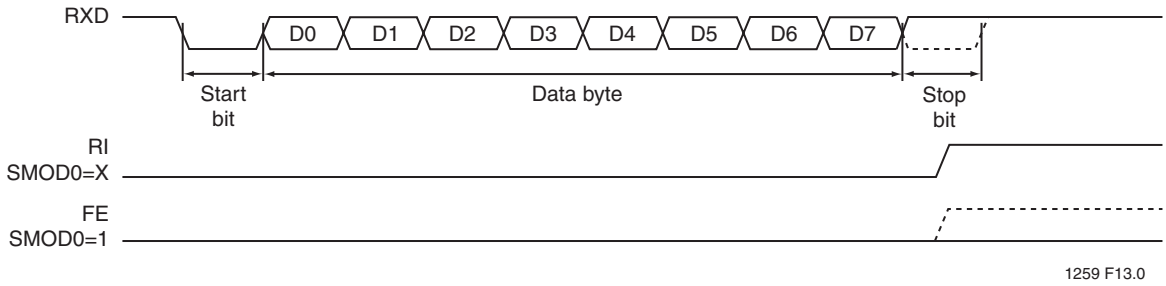


FIGURE 6-2: UART Timings in Mode 1

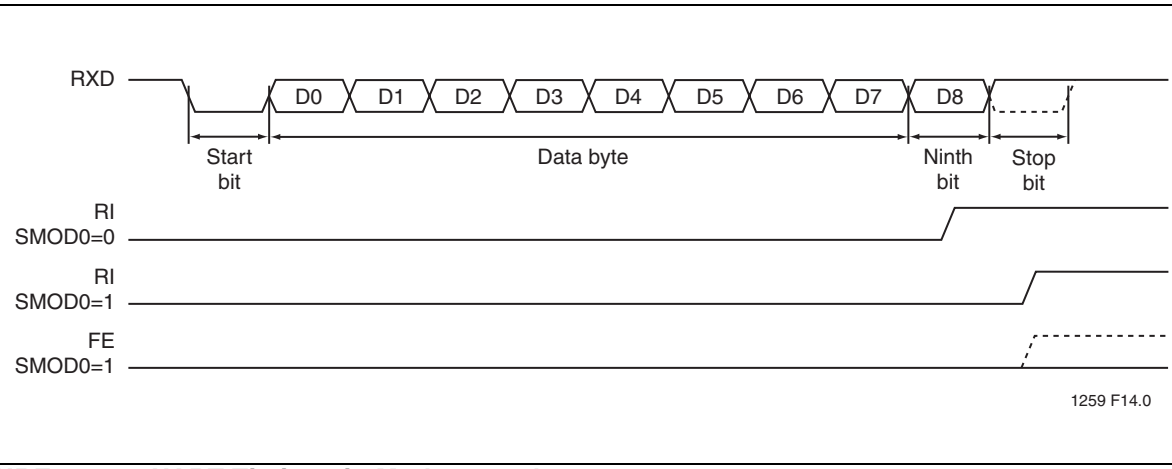


FIGURE 6-3: UART Timings in Modes 2 and 3

6.1.2 Automatic Address Recognition

Automatic Address Recognition helps to reduce the MCU time and power required to talk to multiple serial devices. Each device is hooked together sharing the same serial link with its own address. In this configuration, a device is only interrupted when it receives its own address, thus eliminating the software overhead to compare addresses.

This same feature helps to save power because it can be used in conjunction with idle mode to reduce the system's overall power consumption. Since there may be multiple slaves hooked up serial to one master, only one slave would have to be interrupted from idle mode to respond to the master's transmission. Automatic Address Recognition (AAR) allows the other slaves to remain in idle mode while only one is interrupted. By limiting the number of interruptions, the total current draw on the system is reduced.

There are two ways to communicate with slaves: a group of them at once, or all of them at once. To communicate with a group of slaves, the master sends out an address called the given address. To communicate with all the slaves, the master sends out an address called the "broadcast" address.

AAR can be configured as mode 2 or 3 (9-bit modes) and setting the SM2 bit in SCON. Each slave has its own SM2 bit set waiting for an address byte (9th bit = 1). The Receive Interrupt (RI) flag will only be set when the received byte matches either the given address or the broadcast address. Next, the slave then clears its SM2 bit to enable reception of the data bytes (9th bit = 0) from the master. When the 9th bit = 1, the master is sending an address. When the 9th bit = 0, the master is sending actual data.

If mode 1 is used, the stop bit takes the place of the 9th bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. Note that mode 0 cannot be used. Setting SM2 bit in the SCON register in mode 0 will have no effect.

Each slave's individual address is specified by SFR SADDR. SFR SADEN is a mask byte that defines "don't care" bits to form the given address when combined with SADDR. See the example below:

Slave 1

SADDR = 1111 0001
SADEN = 1111 1010
GIVEN = 1111 0X0X

Slave 2

SADDR = 1111 0011
SADEN = 1111 1001
GIVEN = 1111 0XX1

6.1.2.1 Using the Given Address to Select Slaves

Any bits masked off by a 0 from SADEN become a "don't care" bit for the given address. Any bit masked off by a 1, becomes ANDED with SADDR. The "don't cares" provide flexibility in the user-defined addresses to address more slaves when using the given address.

Shown in the example above, Slave 1 has been given an address of 1111 0001 (SADDR). The SADEN byte has been used to mask off bits to a given address to allow more combinations of selecting Slave 1 and Slave 2. In this case for the given addresses, the last bit (LSB) of Slave 1 is a "don't care" and the last bit of Slave 2 is a 1. To communicate with Slave 1 and Slave 2, the master would need to send an address with the last bit equal to 1 (e.g. 1111 0001) since Slave 1's last bit is a don't care and Slave 2's last bit has to be a 1. To communicate with Slave 1 alone, the master would send an address with the last bit equal to 0 (e.g. 1111 0000), since Slave 2's last bit is a 1. See the table below for other possible combinations.

Select Slave 1 Only		
Slave 1	**Given Address**	**Possible Addresses**
	1111 0X0X	1111 0000 1111 0100

Select Slave 2 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 0XX1	1111 0111 1111 0011

Select Slaves 1 and 2	
Slaves 1 and 2	**Possible Addresses**
	1111 0001 1111 0101

If the user added a third slave such as the example below:

Slave 3

SADDR = 1111 1001
SADEN = 1111 0101
GIVEN = 1111 X0X1

Select Slave 3 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 X0X1	1111 1011 1111 1001

The user could use the possible addresses above to select slave 3 only. Another combination could be to select slave 2 and 3 only as shown below.

Select Slaves 2 and 3 Only	
Slaves 2 and 3	**Possible Addresses**
	1111 0011

More than one slave may have the same SADDR address as well, and a given address could be used to modify the address so that it is unique.

6.1.2.2 Using the Broadcast Address to Select Slaves

Using the broadcast address, the master can communicate with all the slaves at once. It is formed by performing a logical OR of SADDR and SADEN with 0s in the result treated as “don’t cares”.

Slave 1

1111 0001	=	SADDR
+1111 1010	=	SADEN
1111 1X11	=	Broadcast

“Don’t cares” allow for a wider range in defining the broadcast address, but in most cases, the broadcast address will be FFH.

On reset, SADDR and SADEN are “0”. This produces an given address of all “don’t cares” as well as a broadcast address of all “don’t cares.” This effectively disables Automatic Addressing mode and allows the microcontroller to function as a standard 8051, which does not make use of this feature.

7.0 WATCHDOG TIMER

The programmable Watchdog Timer (WDT) is for fail safe protection against software deadlock and for automatic recovery.

The Watchdog timer can be utilized as a watchdog or a timer. To use the Watchdog timer as a watchdog, WDRE (WDTC[3]) should be set to "1." To use the Watchdog timer as a timer only, WDRE should be set to "0" so that an interrupt will be generated upon timer overflow, and the EWD (IEA[6]) should be set to "1" in order to enable the interrupt.

7.1 Watchdog Timer Mode

To protect the system against software deadlock, WDT (WDTC[1]) should be refreshed within a user-defined time period. Without a periodic refresh, an internal hardware reset will be initiated when WDRE (WDTC[3]) = 1). The WDRE bit can only be cleared by a power-on reset.

Any Write to WDTC must be preceded by a correct feed sequence. If WDTON (WDTC[6])=0, SWDT (WDTC[0]) controls the start or stop of the watchdog. If WDTON = 1, the watchdog starts regardless of SWDT and cannot be stopped.

The upper 8 bits of the time base register (WDTD) is used as the reload register of the counter. When WDT (WDTC[1]) is set to "1," the content of WDTD is loaded into the watchdog counter and the prescaler is also cleared.

If a watchdog reset occurs, the internal reset is active for at least one watchdog clock cycle. The code execution will begin immediately after the reset cycle.

The WDTS flag bit is set by Watchdog timer overflow and can only be cleared by power-on reset. Users can also clear the WDTS bit by writing "1" to it following a correct feed sequence.

7.2 Pure Timer Mode

In Timer mode, the WDTC and WDTD can be written at any time without a feed sequence. Setting or clearing the SWDT bit will start or stop the counter. A timer overflow will set the WDTS bit. Writing "1" to this bit clears the bit. When an overflow occurs, the content of WDTD is reloaded into the counter and the Watchdog timer immediately begins to count again. If the interrupt is enabled, an interrupt will occur when the timer overflows. The vector address is 053H and it has a second level priority by default. A feed sequence is not required in this mode.

7.3 Clock Source

The WDT in the device uses the system clock (XTAL1) as its time base. So strictly speaking, it is a watchdog counter rather than a Watchdog timer. The WDT register will increment every 344,064 crystal clocks. The upper 8-bits of the time base register (WDTD) are used as the reload register of the WDT.

Figure 7-1 provides a block diagram of the WDT. Two SFRs (WDTC and WDTD) control Watchdog timer operation.

The time-out period of the WDT is calculated as follows:

$$\text{Period} = (255 - \text{WDTD}) * 344064 * 1/f_{CLK\ (XTAL1)}$$

where WDTD is the value loaded into the WDTD register and f_{OSC} is the oscillator frequency.

7.4 Feed Sequence

In Watchdog mode (WDRE=1), a feed sequence is needed to write into the WDTC register.

The correct feed sequence is:

1. write FDH to SFIS1,
2. write 2AH to SFIS0, then
3. write to the WDTC register

An incorrect feed sequence will cause an immediate reset in Watchdog mode.

In Timer mode, the WDTC and WDTD can be written at any time. A feed sequence is not required.

7.5 Power Saving Considerations for Using the Watchdog Timer

During Idle mode, the Watchdog timer will remain active. The device should be awakened and the Watchdog timer refreshed periodically before expiration. During Power-down mode, the Watchdog timer is stopped. When the Watchdog timer is used as a pure timer, users can turn off the clock to save power. See "Power Management Control Register (PMC)" on page 23.

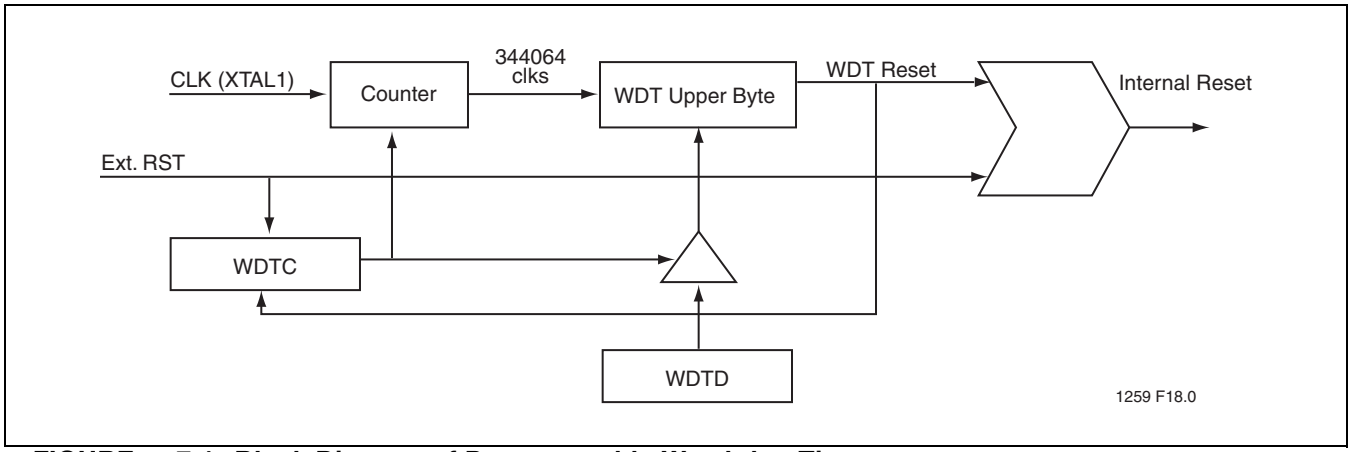


FIGURE 7-1: Block Diagram of Programmable Watchdog Timer

8.0 SECURITY LOCK

The security lock protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory. There are two different types of security locks in the device security lock system: Chip-Level Security Lock and Page-Level Security Lock.

8.1 Chip-Level Security Lock

There are four types of chip-level security locks.

1. Disable External MOVC instruction
2. Disable External Host Mode (Except Read Chip ID and Chip-Erase commands)
3. Disable Boot from External Memory
4. Disable External IAP commands (Except Chip-Erase commands)

Users can turn on these security locks in any combination to achieve the security protection scheme. To unlock security locks, the Chip-Erase command must be used.

8.1.1 Disable External MOVC instruction

When Disable-Extern-MOVC command is executed either by External Host Mode command or IAP Mode Command, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory.

8.1.2 Disable External Host Mode

When Disable-Extern-Host-Cmd command is executed either by External Host Mode Command or IAP Mode Command, all external host mode commands are disabled except Chip-Erase command and Read-ID command.

Upon activation of this option, the device can not be accessed through external host mode. User can not verify and copy the contents of the internal flash

8.1.3 Disable Boot From External Memory

When Disable-Extern-Boot command is executed either by External Host Mode Command or IAP Mode Command, the EA pin value will be ignored during chip Reset and always boot from the internal memory.

8.1.4 Disable External IAP Commands

When Disable-Extern-IAP command is executed either by External Host Mode Command or IAP Mode Command, all IAP commands executed from external memory are disabled except Chip-Erase command. All IAP commands executed from internal memory are allowed if the Page Lock is not set.

8.2 Page-Level Security Lock

When any of Secure-Page0, Secure-Page1, Secure-Page2, Secure-Page3, or Secure-Page4 command is executed, the individual page (Page0, Page1, Page2, Page3, or Page4) will enter secured mode. No part of the page can be verified by either External Host mode commands or IAP commands. MOVC instructions are also unable to read any data from the page.

To unlock the security locks on Page0-3 of the primary partition (Partition0), the Partition0-Erase command must be used. To unlock the security lock on Page4, the Chip-Erase command must be used.

8.3 Read Operation Under Lock Condition

The following three cases can be used to indicate the Read operation is targeting a locked, secured memory area:

1. External host mode: Read-back = 00H (locked)
2. IAP command: Read-back = previous SFDT data
3. MOVC: Read-back = FFH (blank)

9.0 RESET

A system reset initializes the MCU and begins program execution at program memory location 0000H or the boot vector address. The reset input for the device is the RST pin. In order to reset the device, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE and PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a proper reset. This level must not be affected by external element. A system reset will not affect the 512 Bytes of on-chip RAM while the device is running, however, the contents of the on-chip RAM during power up are indeterminate. Following reset, all Special Function Registers (SFR) return to their reset values outlined in Tables 3-3 to 3-8.

9.1 Power-on Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high.

When power is applied to the device, the RST pin must be held high long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2KΩ resistor as shown in Figure 9-1. Note that if an RC circuit is being used, provisions should be made to ensure the V_{DD} rise time does not exceed 1 millisecond and the oscillator start-up time does not exceed 10 milliseconds.

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software. Please refer to Section 3.5, PCON register definition, for detailed information.

For more information on system level design techniques, please review the *Design Considerations for the SST FlashFlex51 Family Microcontroller* application note.

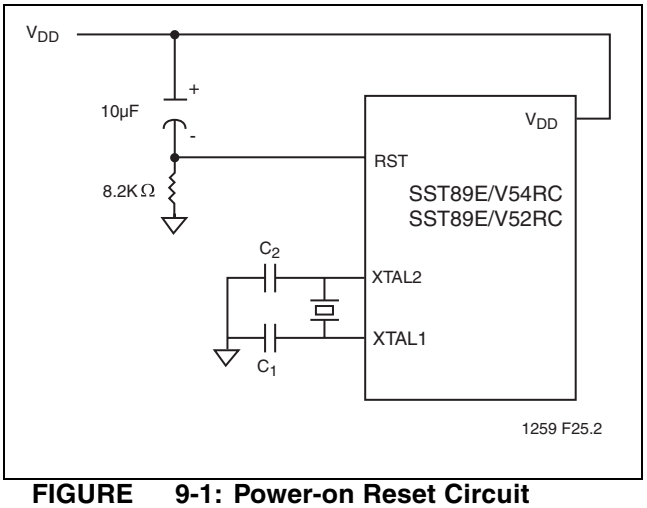


FIGURE 9-1: Power-on Reset Circuit

9.2 Boot Sequence

After Power On Reset, the device can boot from one of three locations: zero, default boot vector (see Table 4-2), or a user-defined boot vector. The checking sequence follows the flowchart in Figure 9-2. If the device uses external code memory (EA#=0), the boot-start address is always zero. The next sequence is to detect any external hardware pin setup.

The device should check P1[0] and P1[1] at the falling edge of reset. (See Figure 9-3 for the timing diagram.) If both pins are low, the device is forced to boot from either the default boot vector or the user-defined boot vector depending on the setting of Boot_From_User_Vector_i. The Boot_Status_Flag bit (HWIAP) in the SFCF register indicates whether or not the system booted with P1[0] and P1[1] set to low during reset. (See Section 3.5, “Special Function Registers” on page 11 for details.)

Programming the control bits (Boot_From_User_Vector_i and Boot_From_Zero_i) can be done through IAP mode commands or External Host Mode commands. The factory default setting for these two bits is “1” and will lead the system to boot from the default boot vector per Table 4-2.

When the device is configured to boot from a user-defined vector, users should use the Set_User_Boot_Vector command to program the Boot Vector[7:0]. The final boot vector address is calculated in Table 9-1.

TABLE 9-1: Boot Vector Address

	Bit Number															
Device	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SST89E/V54RC	0	0	Boot Vector[7:0]								0	0	0	0	0	0
SST89E/V52RC	0	0	0	Boot Vector[7:0]								0	0	0	0	0

T9-1.1 1259

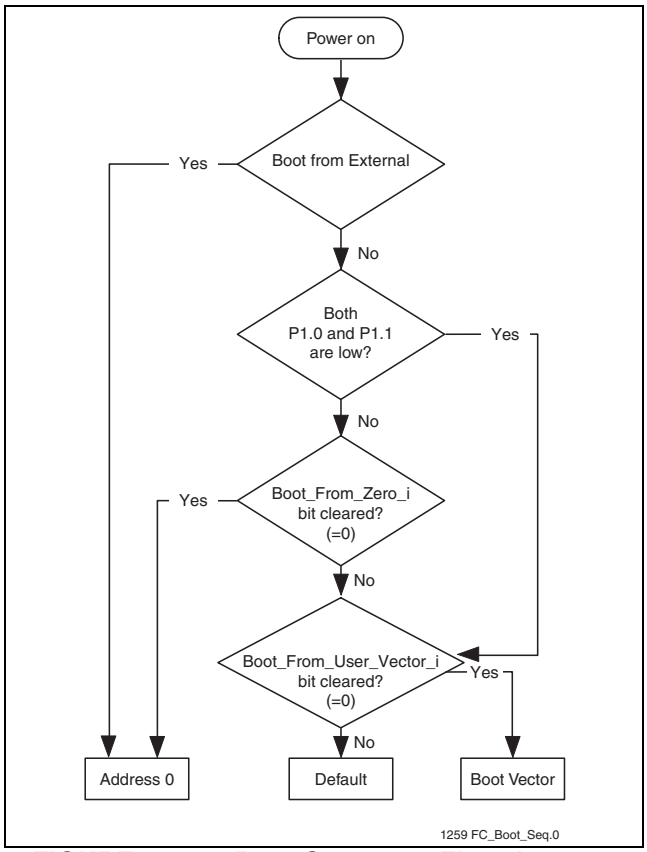


FIGURE 9-2: Boot Sequence Flowchart

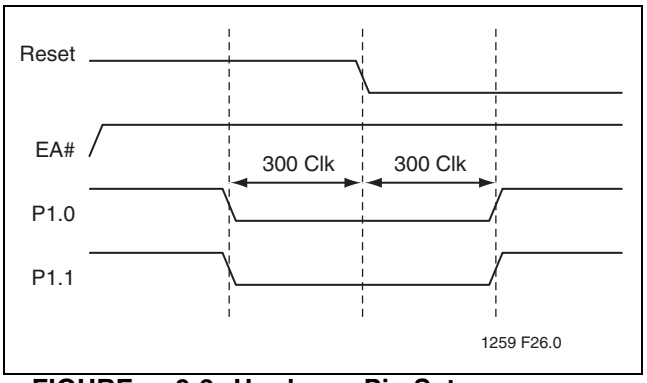


FIGURE 9-3: Hardware Pin Setup

9.3 Interrupt Priority and Polling Sequence

The device supports seven interrupt sources under a four level priority scheme. Table 9-2 and Figure 9-4 summarize the polling sequence of the supported interrupts.

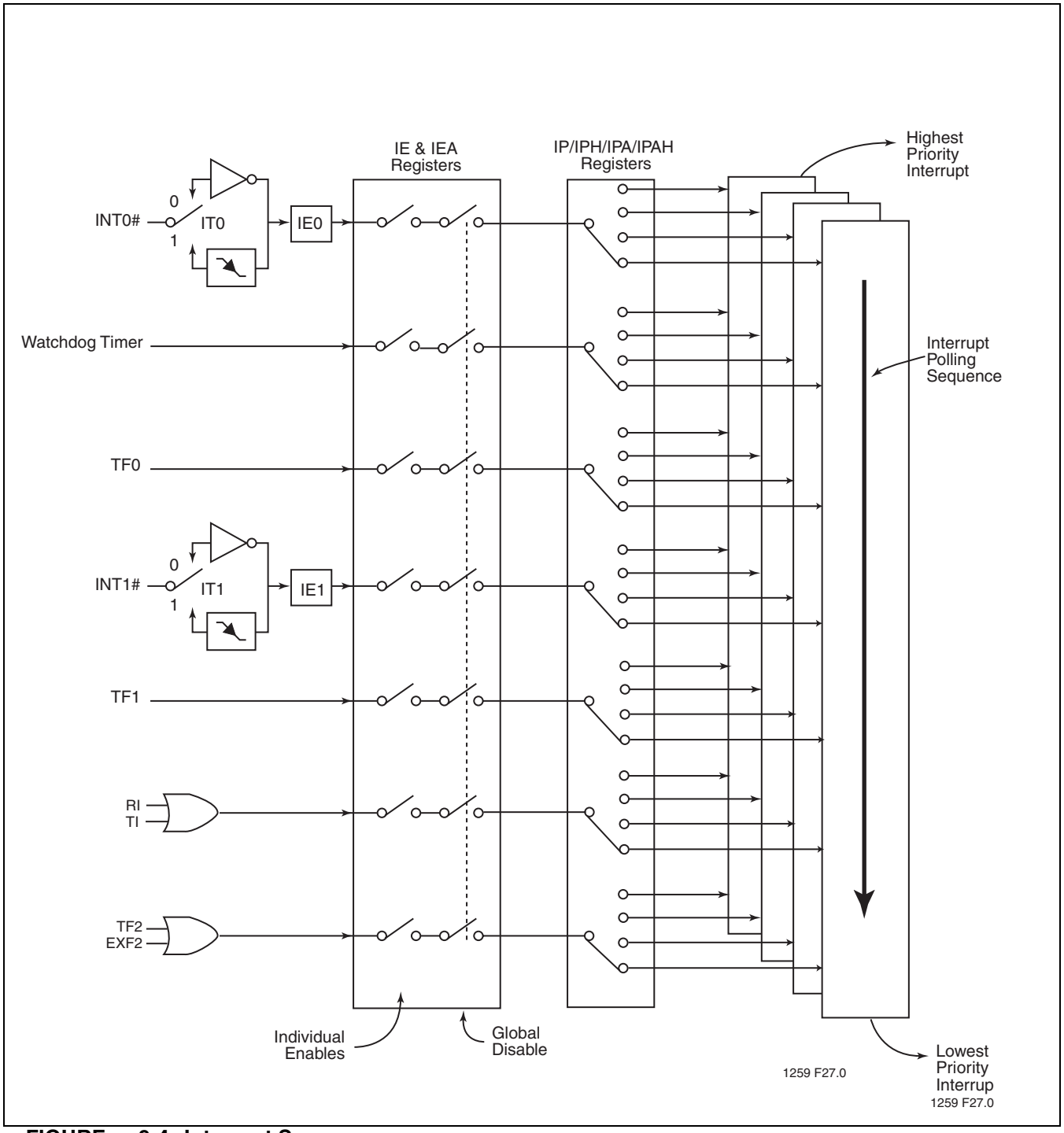


FIGURE 9-4: Interrupt Sequence

TABLE 9-2: Interrupt Polling Sequence

Description	Interrupt Flag	Vector Address	Interrupt Enable	Interrupt Priority	Service Priority	Wake-Up Power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1(highest)	yes
Watchdog	-	0053H	EWD	PWD/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
UART	TI/RI	0023H	ES	PS/H	6	no
T2	TF2, EXF2	002BH	ET2	PT2/H	7	no

T9-2.0 1259

10.0 POWER-SAVING MODES

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 10-1.

In addition to these two power saving modes, users can choose to set the device to run at one of four slower clock rates to reduce power consumption. See Section 11.3, "Clock Divider Option".

Another option is to turn off the clocks by individual functional blocks, please refer to Section 3.5, the PMC register definition, for detailed information.

10.1 Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

10.2 Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 2.0V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal restored to logic $V_{IH,}$ the interrupt service routine program execution resumes beginning at the instruction immediately following the instruction which invoked power-down mode. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

TABLE 10-1: Power Saving Modes

Mode	Initiated by	State of MCU	Exited by
Idle	Software (Set IDL bit in PCON) MOV PCON, #01H;	• CLK is running. • Interrupts, serial port and timers/counters are active. • Program Counter is stopped. • ALE and PSEN# signals at a HIGH level during Idle. • All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked idle mode. A user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down	Software (Set PD bit in PCON) MOV PCON, #02H;	• CLK is stopped. • On-chip SRAM and SFR data is maintained. • ALE and PSEN# signals at a LOW level during power -down. • External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.

Preliminary Specifications

11.0 SYSTEM CLOCK AND CLOCK OPTIONS

11.1 Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 11-1 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 11-1, shows the typical values for C1 and C2 vs. crystal type for various frequencies

TABLE 11-1:Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

T11-1.1 1259

More specific information about on-chip oscillator design can be found in the *FlashFlex51 Oscillator Circuit Design Considerations* application note.

11.2 Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 11-2 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 4-3 for the IAP mode enabling command (When set, the Enable-Clock-Double_i bit in the SFST register will indicate 6-clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

11.3 Clock Divider Option

The device has an option to run at scaled-down clock rates of 1/4, 1/16, 1/256, and 1/1024. The COEN bit in the COSR register must be set to enable this option. The CO_SEL bits are set to select the clock rate. See the COSR register for more information.

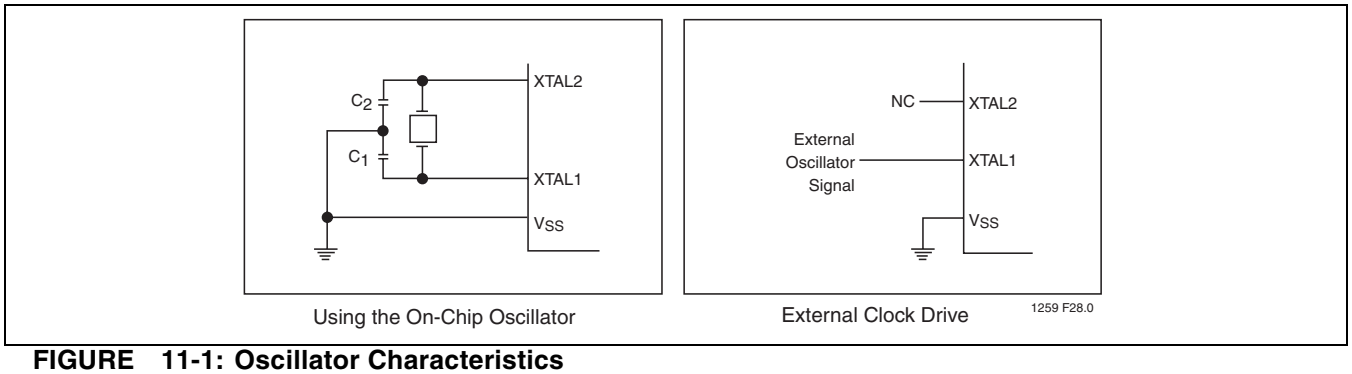


FIGURE 11-1: Oscillator Characteristics

TABLE 11-2: Clock Doubling Features

Device	Standard Mode (x1)		Clock Double Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89E5xRC	12	33	6	16
SST89V5xRC	12	25	6	12

T11-2.0 1259

12.0 ELECTRICAL SPECIFICATION

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on EA# Pin to V_{SS} . . . . . -0.5V to +14.0V
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to V_{DD}+1.0V
Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 . . . . . 20mA
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time. (Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production. The specifications are subject to change without notice.

TABLE 12-1: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage			
	SST89E5xRC	4.5	5.5	V
	SST89V5xRC	2.7	3.6	V
f_{OSC}	Oscillator Frequency			
	SST89E5xRC	0	33	MHz
	SST89V5xRC	0	25	MHz
	Oscillator Frequency for In-Application programming			
	SST89E5xRC	.25	33	MHz
	SST89V5xRC	.25	25	MHz

T12-1.1 1259

TABLE 12-2: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T12-2.0 1259

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12-3: AC Conditions of Test

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . C_L = 100 pF
See Figures 12-6 and 12-8

T12-3.0 1259

TABLE 12-4: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T12-4.2 1259

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 12-5: Pin Impedance (VDD=3.3V, TA=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

T12-5.4 1259

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

12.1 DC Electrical Characteristics

TABLE 12-6: DC Characteristics for SST89E5xRC: T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage	4.5 < V_{DD} < 5.5	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current				
	Active Mode @ 33 MHz			32	mA
	Idle Mode@ 33 MHz			26	mA
	Power-down Mode (min V_{DD} = 2V)	T_A = 0°C to 70°C T_A = -40°C to +85°C		50	µA

T12-6.1 1259

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs:71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE and PSEN#= 100pF, load capacitance for all other outputs = 80 pF.
4. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

TABLE 12-7: DC Characteristics for SST89V5xRC: T_A = -40°C to +85°C; V_{DD} = 2.7-3.6V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	2.7 < V_{DD} < 3.6	-0.5	0.7	V
V_{IH}	Input High Voltage	2.7 < V_{DD} < 3.6	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.7 < V_{DD} < 3.6	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 2.7V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 2.7V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 2.7V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 2.7V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 2.7V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pull-down Resistor			225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current				
	Active Mode @ 25 MHz			27	mA
	Idle Mode @ 25 MHz			21	mA
	Power-down Mode (min V_{DD} = 2V)	T_A = 0°C to 70°C T_A = -40°C to +85°C		40	µA

T12-7.7 1259

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE and PSEN#= 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

12.2 AC Electrical Characteristics

AC Characteristics: (Over Operating Conditions: Load Capacitance for Port 0, ALE#, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

TABLE 12-8: AC Electrical Characteristics (1 of 2)
T_A = -40°C to +85°C, V_{DD} = 2.7-3.6V@25MHz, 4.5-5.5V@33MHz, V_{SS} = 0V

		Oscillator						
		25 MHz (x1 Mode) 12 MHz (x2 Mode)[1]		33 MHz (x1 Mode) 16 MHz (x2 Mode)[1]		Variable		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	25	0	33	0		MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	12	0	16	0		MHz
T_{LHLL}	ALE Pulse Width	65		46		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low	15				T_{CLCL} - 25 (3V)		ns
				15		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low	15				T_{CLCL} - 25 (3V)		ns
				15		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		95				$4T_{CLCL}$ - 65 (3V)	ns
					66		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	15				T_{CLCL} - 25 (3V)		ns
				15		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	95				$3T_{CLCL}$ - 25 (3V)		ns
				76		$3T_{CLCL}$ - 15 (5V)		
T_{PLIV}	PSEN# Low to Valid Instr In		65				$3T_{CLCL}$ - 55 (3V)	ns
					41		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#					0		ns
T_{PXIZ}	Input Instr Float After PSEN#		35				T_{CLCL} - 5 (3V)	ns
					15		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	32		22		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In		120				$5T_{CLCL}$ - 80 (3V)	ns
					92		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T_{RLRH}	RD# Pulse Width	200				$6T_{CLCL}$ - 40 (3V)		ns
				152		$6T_{CLCL}$ - 30 (5V)		
T_{WLWH}	Write Pulse Width (WE#)	200				$6T_{CLCL}$ - 40 (3V)		ns
				152		$6T_{CLCL}$ - 30 (5V)		
T_{RLDV}	RD# Low to Valid Data In		110				$5T_{CLCL}$ - 90 (3V)	ns
					102		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		0		ns
T_{RHDZ}	Data Float After RD#		65				$2T_{CLCL}$ - 25 (3V)	ns
					49		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In		230				$8T_{CLCL}$ - 90 (3V)	ns
					192		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In		270				$9T_{CLCL}$ - 90 (3V)	ns
					198		$9T_{CLCL}$ - 75 (5V)	ns
T_{LLWL}	ALE Low to RD# or WR# Low	95	145			$3T_{CLCL}$ - 25 (3V)	$3T_{CLCL}$ + 25 (3V)	ns
				76	106	$3T_{CLCL}$ - 15 (5V)	$3T_{CLCL}$ + 15 (5V)	
T_{AVWL}	Address to RD# or WR# Low	85				$4T_{CLCL}$ - 75 (3V)		ns
				91		$4T_{CLCL}$ - 30 (5V)		ns

TABLE 12-8: AC Electrical Characteristics (Continued) (2 of 2)
T_A = -40°C to +85°C, V_{DD} = 2.7-3.6V@25MHz, 4.5-5.5V@33MHz, V_{SS} = 0V

		Oscillator						
		25 MHz (x1 Mode) 12 MHz (x2 Mode)[1]		33 MHz (x1 Mode) 16 MHz (x2 Mode)[1]		Variable		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
T_{QVWX}	Data Valid to WR# High to Low Transition		20		10	T_{CLCL} - 20		ns
T_{WHQX}	Data Hold After WR#	13				T_{CLCL} - 27 (3V)		ns
				10		T_{CLCL} - 20 (5V)		ns
T_{QVWH}	Data Valid to WR# High	210				$7T_{CLCL}$ - 70 (3V)		ns
				162		$7T_{CLCL}$ - 50 (5V)		ns
T_{RLAZ}	RD# Low to Address Float		0		0		0	ns
T_{WHLH}	RD# to WR# High to ALE High	15	65			T_{CLCL} - 25 (3V)	T_{CLCL} + 25 (3V)	ns
				15	45	T_{CLCL} - 15 (5V)	T_{CLCL} + 15 (5V)	ns

T12-8.0 1259

1. Calculated values are for x1 Mode only

Explanation of Symbols Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW or ALE
P: PSEN#
Q: Output data
R: RD# signal
T: Time
V: Valid
W: WR# signal
X: No longer a valid logic level
Z: High Impedance (Float)

For example:

T_{AVLL} = Time from Address Valid to ALE Low
T_{LLPL} = Time from ALE Low to PSEN# Low

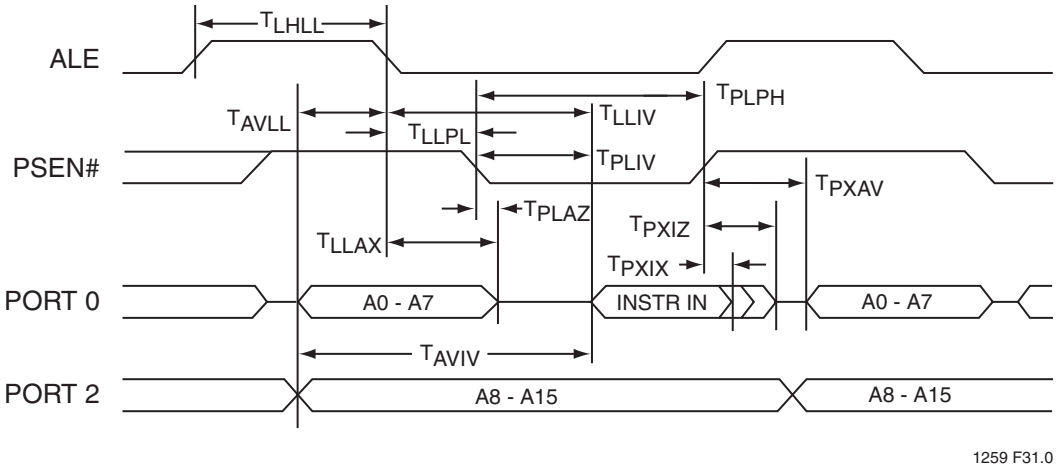


FIGURE 12-1: External Program Memory Read Cycle

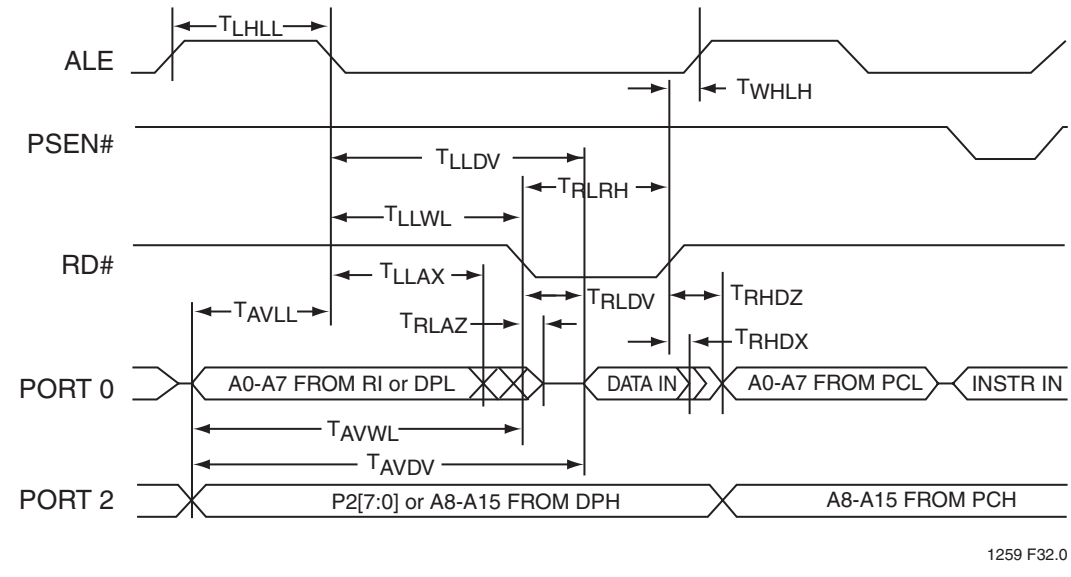


FIGURE 12-2: External Data Memory Read Cycle

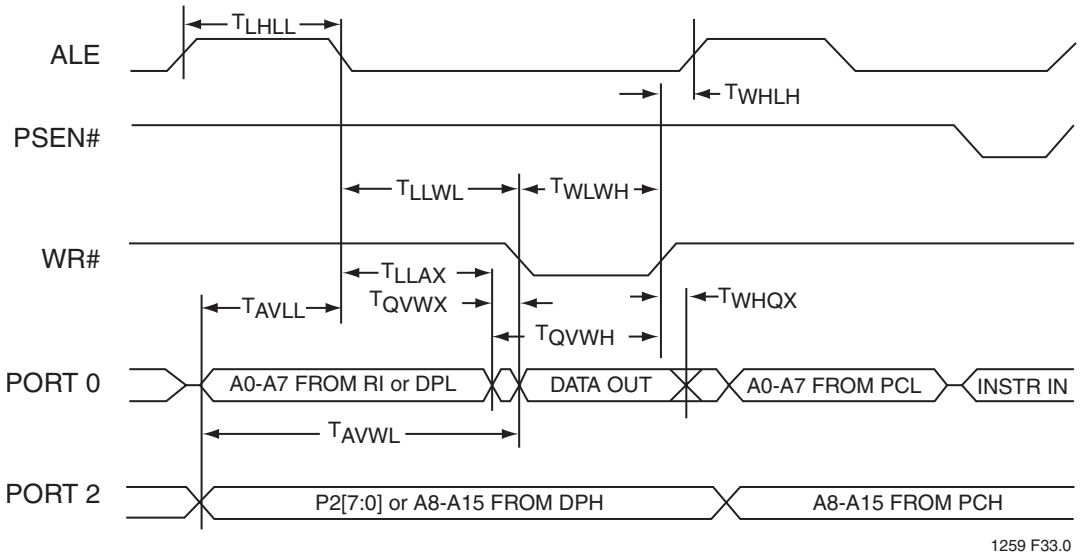


FIGURE 12-3: External Data Memory Write Cycle

TABLE 12-9: External Clock Drive

Symbol	Parameter	Oscillator						Units
		12MHz		33MHz		Variable		
		Min	Max	Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency					0	40	MHz
T_{CLCL}		83		30.3				ns
T_{CHCX}	High Time			10.6		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time			10.6		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		20		10			ns
T_{CHCL}	Fall Time		20		10			ns

T12-9.2 1259

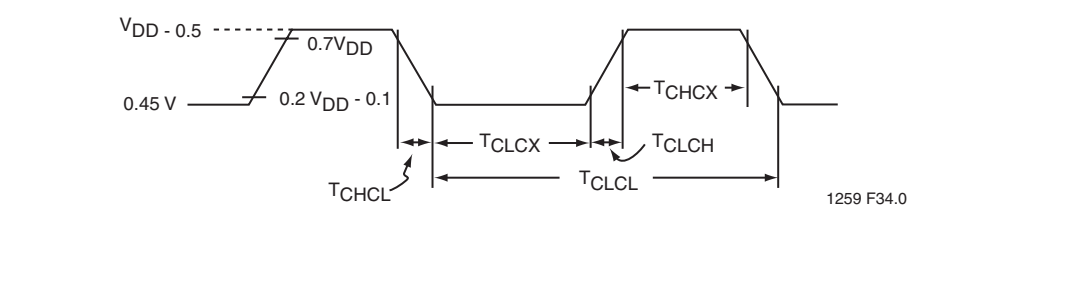


FIGURE 12-4: External Clock Drive Waveform

TABLE 12-10: Serial Port Timing

Symbol	Parameter	Oscillator						Units
		12MHz		33MHz		Variable		
		Min	Max	Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		0.364		$12T_{CLCL}$		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		170		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50				$2T_{CLCL}$ - 117		ns
				11		$2T_{CLCL}$ - 50		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		170		$10T_{CLCL}$ - 133	ns

T12-10.2 1259

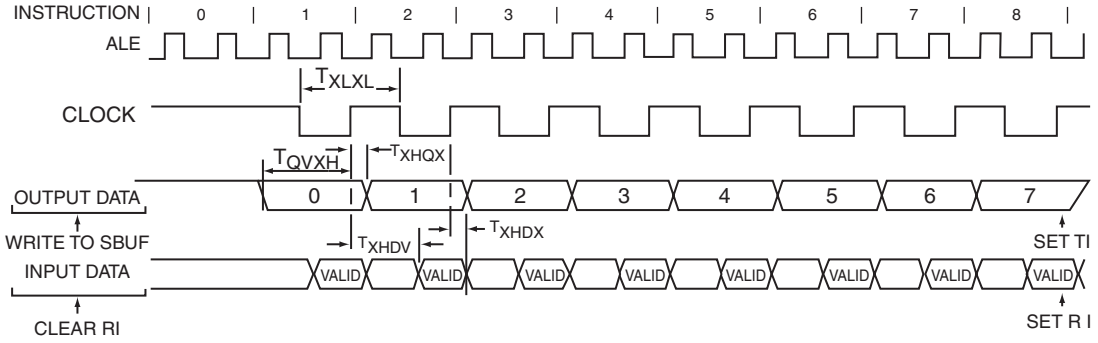
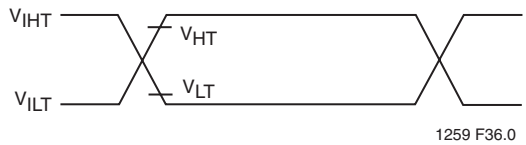


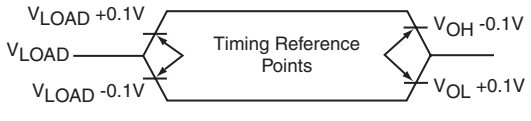
FIGURE 12-5: Shift Register Mode Timing Waveforms



AC Inputs during testing are driven at V_{IHT} (V_{DD} -0.5V) for Logic "1" and V_{ILT} (0.45V) for a Logic "0". Measurement reference points for inputs and outputs are at V_{HT} ($0.2V_{DD}$ + 0.9) and V_{LT} ($0.2V_{DD}$ - 0.1)

Note: V_{HT}- V_{HIGH} Test
V_{LT}- V_{LOW} Test
V_{IHT}-V_{INPUT} HIGH Test
V_{ILT}- V_{INPUT} LOW Test

FIGURE 12-6: AC Testing Input/Output Test Waveform



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ± 20mA.

FIGURE 12-7: Float Waveform

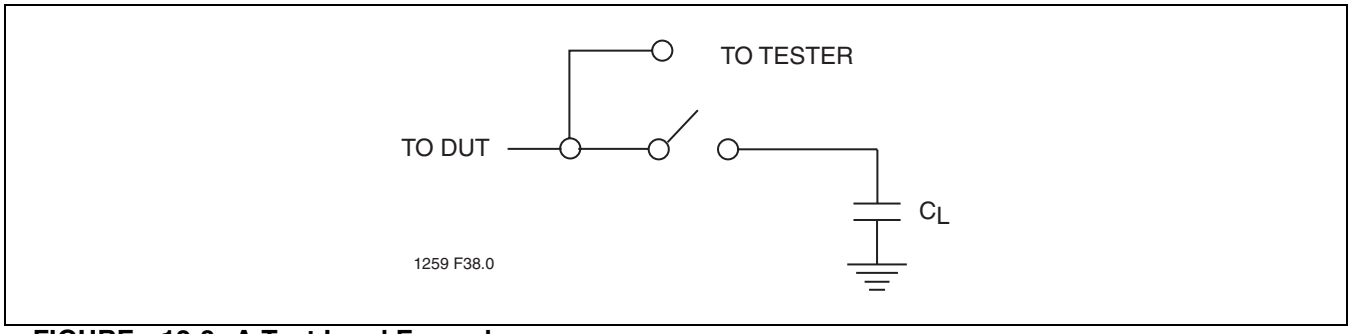


FIGURE 12-8: A Test Load Example

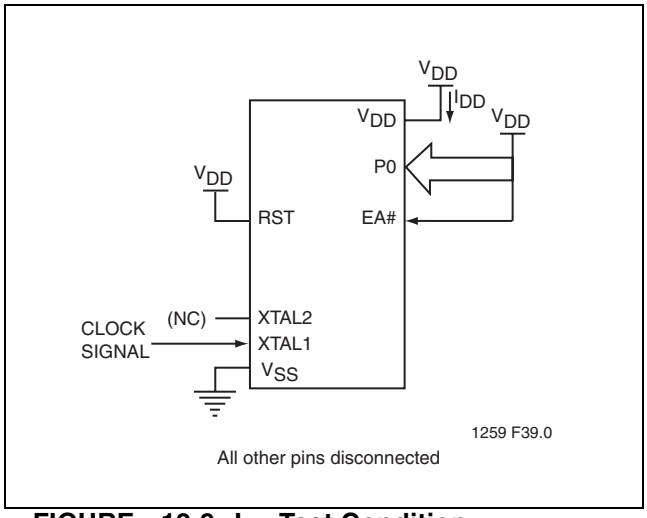


FIGURE 12-9: I_{DD} Test Condition, Active Mode

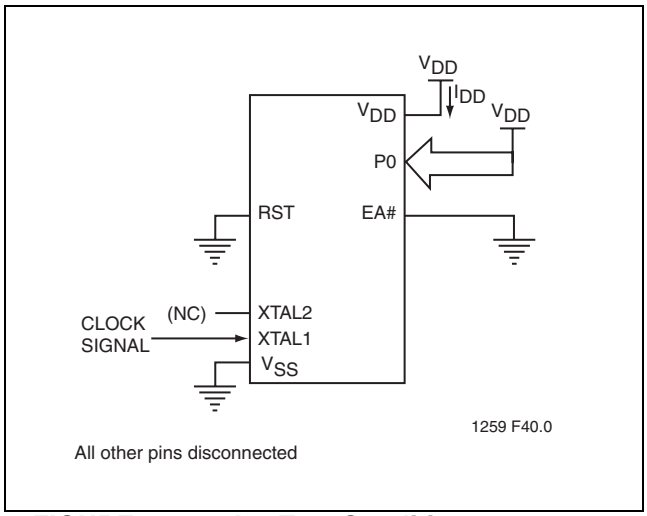


FIGURE 12-10: I_{DD} Test Condition, Idle Mode

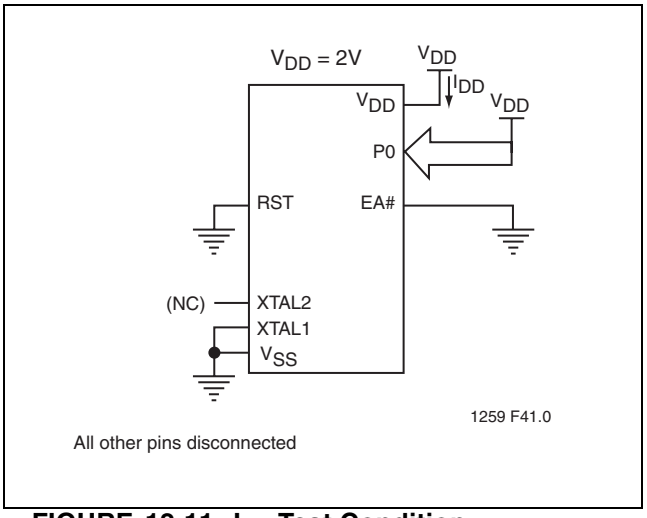


FIGURE 12-11: I_{DD} Test Condition, Power-down Mode

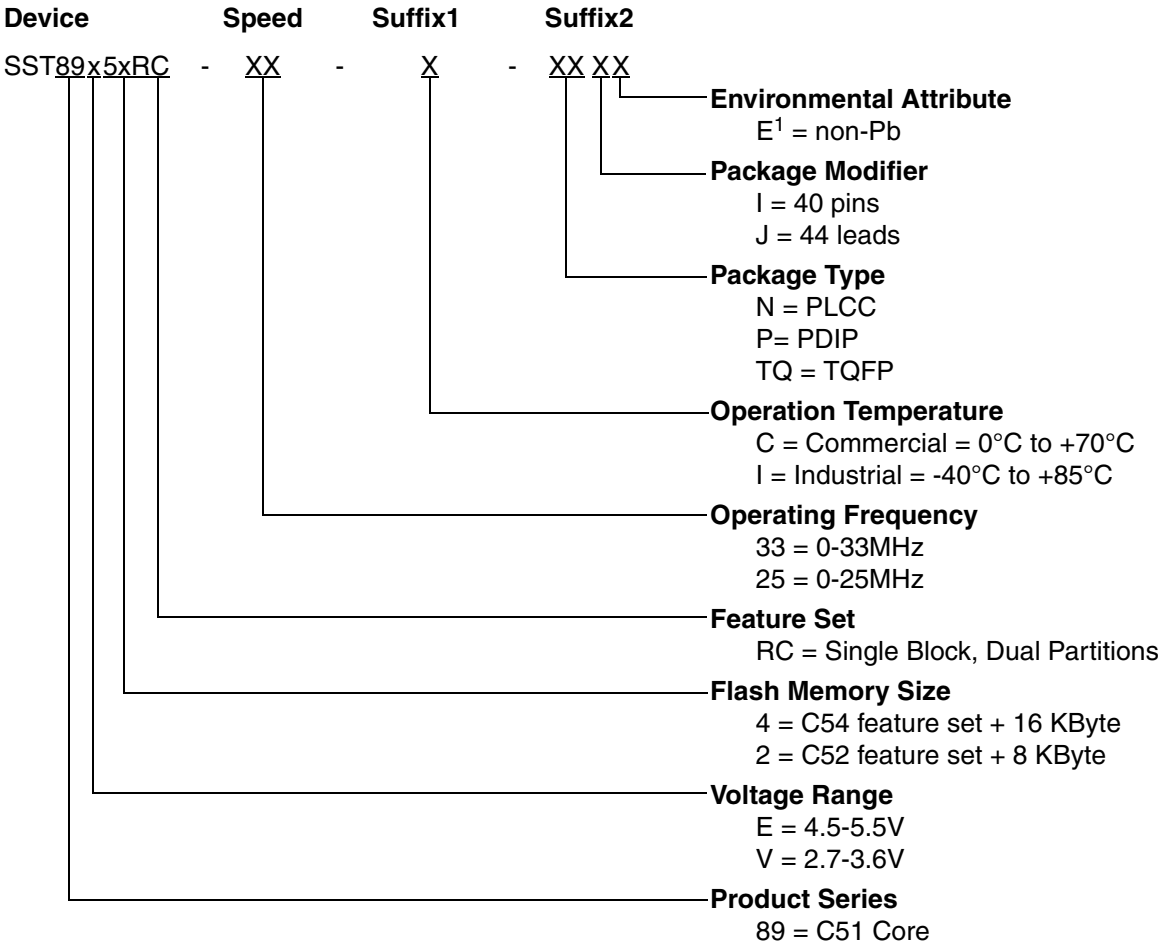
TABLE 12-11: Flash Memory Programming/ Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	350	ms
Block-Erase Time	300	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	100	µs
Re-map or Security bit Program Time	100	µs

T12-11.0 1259

1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

13.0 PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

13.1 Valid Combinations

Valid combinations for SST89E52RC

SST89E52RC-33-C-NJE	SST89E52RC-33-C-TQJE	SST89E52RC-33-C-PIE
SST89E52RC-33-I-NJE	SST89E52RC-33-I-TQJE	

Valid combinations for SST89V52RC

SST89V52RC-25-C-NJE	SST89V52RC-25-C-TQJE	SST89V52RC-25-C-PIE
SST89V52RC-25-I-NJE	SST89V52RC-25-I-TQJE	

Valid combinations for SST89E54RC

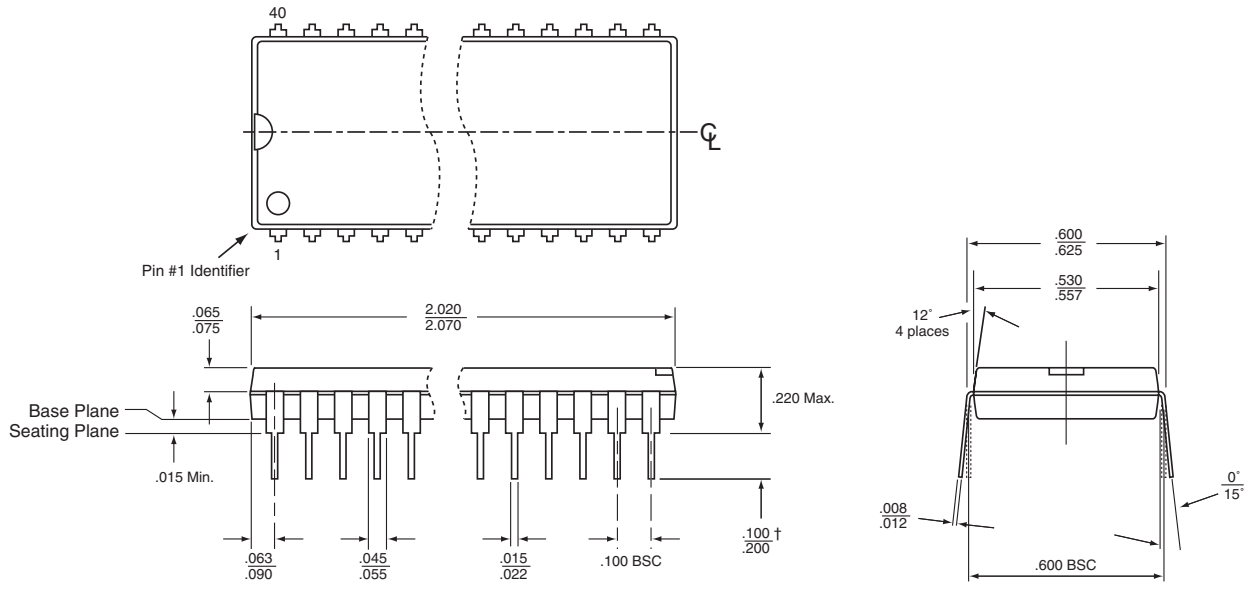
SST89E54RC-33-C-NJE	SST89E54RC-33-C-TQJE	SST89E54RC-33-C-PIE
SST89E54RC-33-I-NJE	SST89E54RC-33-I-TQJE	

Valid combinations for SST89V54RC

SST89V54RC-25-C-NJE	SST89V54RC-25-C-TQJE	SST89V54RC-25-C-PIE
SST89V54RC-25-I-NJE	SST89V54RC-25-I-TQJE	

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

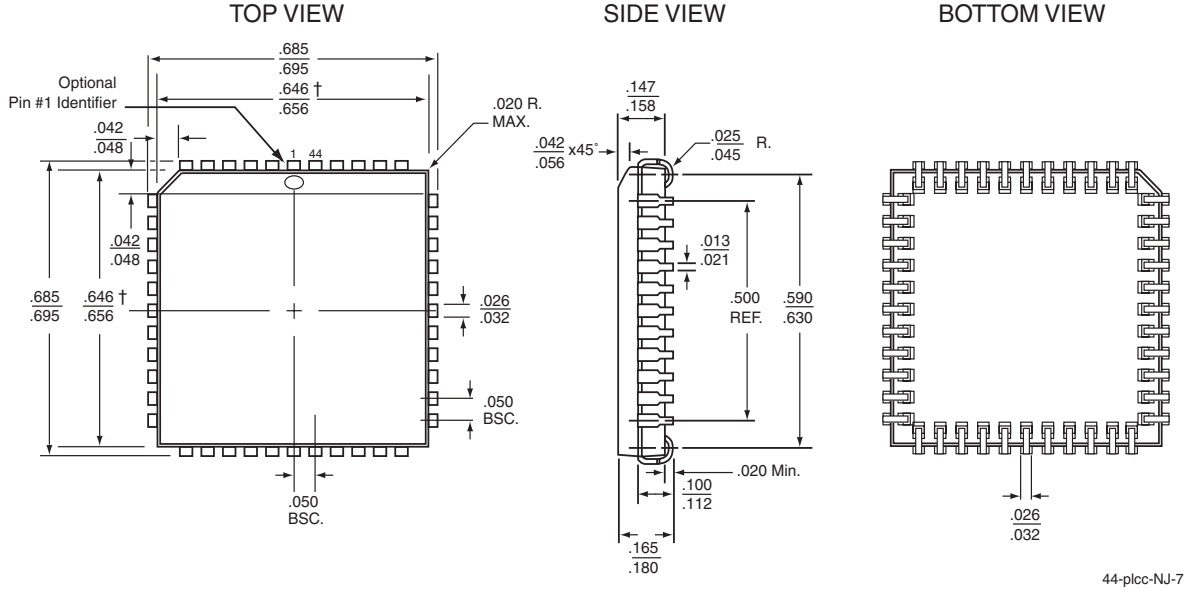
14.0 PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-011 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .115; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

40-pdip-PI-7

FIGURE 14-1: 40-pin Plastic Dual In-line Pins (PDIP)
SST Package Code: PI



44-plcc-NJ-7

Note: 1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .650; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

FIGURE 14-2: 44-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ

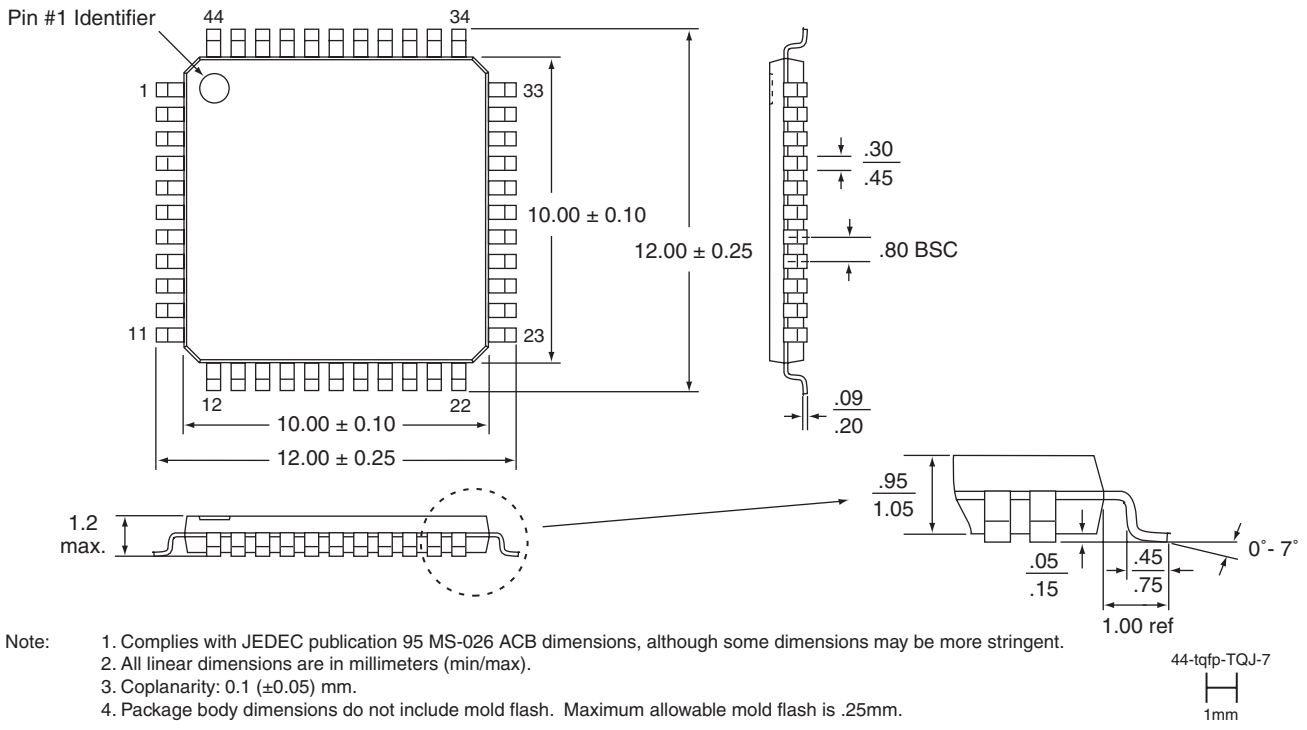


FIGURE 14-3: 44-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQJ

TABLE 14-1: Revision History

Number	Description	Date
00	• Initial Release of Fact Sheet	Feb 2005
01	• Added 40-PDIP devices and associated MPNs • Revised Function Block and Pin Assignment diagrams • Revised Valid Combinations product numbers • Removed 4KByte product from the fact sheet (SST89x51RC) • Initial Release of Data Sheet	Feb 2006