# MC100EPT25

## -3.3V / -5V Differential ECL to +3.3V LVTTL Translator

The MC100EPT25 is a Differential ECL to LVTTL translator. This device requires +3.3 V, −3.3 V to −5.2 V, and ground. The small outline 8−lead package and the single gate of the EPT25 make it ideal for applications which require the translation of a clock or data signal.

The $V_{BB}$ output allows the EPT25 to also be used in a single−ended input mode. In this mode the $V_{BB}$ output is tied to the D input for a inverting buffer or the $\overline{D}$ input for a non−inverting buffer. If used, the $V_{BB}$ pin should be bypassed to ground with at least a 0.01 μF capacitor.

- 1.1 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- Operating Range: $V_{CC}$ = 3.0 V to 3.6 V; $V_{EE}$ = −5.5 V to −3.0 V; GND = 0 V
- 24 mA TTL Outputs
- Q Output Will Default LOW with Inputs Open or at $V_{EE}$
- $V_{BB}$ Output
- Open Input Default State
- Safety Clamp on Inputs
- Pb−Free Packages are Available

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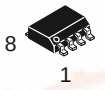
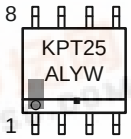
**MARKING DIAGRAMS***

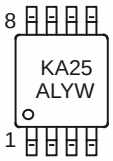



**SO−8**
**D SUFFIX**
**CASE 751**





**TSSOP−8**
**DT SUFFIX**
**CASE 948R**



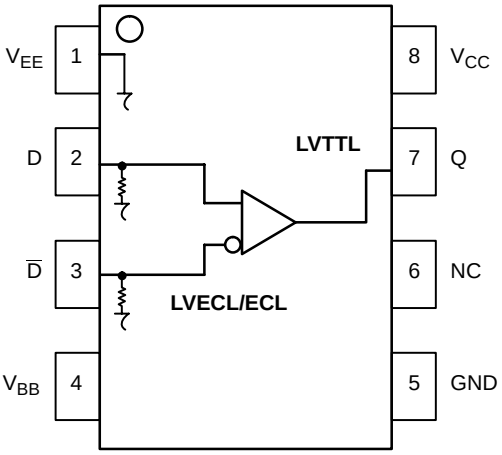

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC100EPT25D | SO−8 | 98 Units/Rail |
| MC100EPT25DG | SO−8 (Pb−Free) | 98 Units/Rail |
| MC100EPT25DR2 | SO−8 | 2500 Tape & Reel |
| MC100EPT25DT | TSSOP−8 | 100 Units/Rail |
| MC100EPT25DTG | TSSOP−8 (Pb−Free) | 100 Units/Rail |
| MC100EPT25DTR2 | TSSOP−8 | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.




**PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| Q | LVTTL Output |
| D*, $\overline{D}$* | Differential ECL Input Pair |
| $V_{CC}$ | Positive Supply |
| $V_{BB}$ | Output Reference Voltage |
| GND | Ground |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

* Pins will default LOW when left open.

**Figure 1. 8−Lead Pinout** (Top View) **and Logic Diagram**

**ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ |
| Internal Input Pullup Resistor | | N/A |
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL−94 V−0 @ 0.125 in |
| Transistor Count | | 111 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, see Application Note AND8003/D.

**MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | GND = 0 V | $V_{EE}$ = −5.0 V | 3.8 | V |
| $V_{EE}$ | Negative Power Supply | GND = 0 V | $V_{CC}$ = +3.3 V | −6 | V |
| $V_{IN}$ | Input Voltage | GND = 0 V | | 0 to $V_{EE}$ | V |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 LFPM<br>500 LFPM | 8 SOIC<br>8 SOIC | 190<br>130 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | std bd | 8 SOIC | 41 to 44 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 LFPM<br>500 LFPM | 8 TSSOP<br>8 TSSOP | 185<br>140 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | std bd | 8 TSSOP | 41 to 44 | °C/W |
| $T_{sol}$ | Wave Solder | < 2 to 3 sec @ 248°C | | 265 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

**NECL DC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = −5.5 V to −3.0 V; GND = 0.0 V (Note 2)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| IEE | Power Supply Current | 8.0 | 16 | 25 | 8.0 | 16 | 25 | 8.0 | 16 | 25 | mA |
| $V_{IH}$ | Input HIGH Voltage Single−Ended | −1225 | | −880 | −1225 | | −880 | −1225 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage Single−Ended | −1945 | | −1625 | −1945 | | −1625 | −1945 | | −1625 | mV |
| $V_{BB}$ | Output Voltage Reference | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Note 3) | $V_{EE}$ + 2.0 | | 0.0 | $V_{EE}$ + 2.0 | | 0.0 | $V_{EE}$ + 2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2. Input parameters vary 1:1 with GND.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**TTL OUTPUT DC CHARACTERISTICS** $V_{CC}$ = 3.3 V; $V_{EE}$ = −5.5 V to −3.0 V; GND = 0.0 V; $T_A$ = −40°C to 85°C

| Symbol | Characteristic | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −3.0 mA | 2.2 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA | | | 0.5 | V |
| $I_{CCH}$ | Power Supply Current | | 6 | 10 | 14 | mA |
| $I_{CCL}$ | Power Supply Current | | 7 | 12 | 17 | mA |

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

**AC CHARACTERISTICS** $V_{CC}$ = 3.0 V to 3.6 V; $V_{EE}$ = −5.5 V to −3.0 V; GND = 0.0 V (Note 4)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Frequency (See Figure 2 $F_{max}$/JITTER) | 275 | | | 275 | | | 275 | | | MHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential (Cross−Point to 1.5 V) | 800 | 1200 | 1800 | 800 | 1100 | 1600 | 800 | 1100 | 1600 | ps |
| $t_{SKPP}$ | Device−to−Device Skew (Note 5) | | | 500 | | | 500 | | | 500 | ps |
| $t_{JITTER}$ | Random Clock Jitter (RMS) (See Figure 2 $F_{max}$/JITTER) | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps |
| $V_{PP}$ | Input Voltage Swing (Differential) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times Q, $\overline{Q}$<br>(0.8 V − 2.0 V) | 450<br>900 | 600<br>1160 | 750<br>1400 | 450<br>900 | 600<br>1100 | 750<br>1400 | 450<br>900 | 600<br>1100 | 750<br>1400 | ps |

4. Measured with a 750 mV 50% duty−cycle clock source. $R_L$ = 500 Ω to GND and $C_L$ = 20 pF to GND. Refer to Figure 3.
5. Skews are measured between outputs under identical conditions.

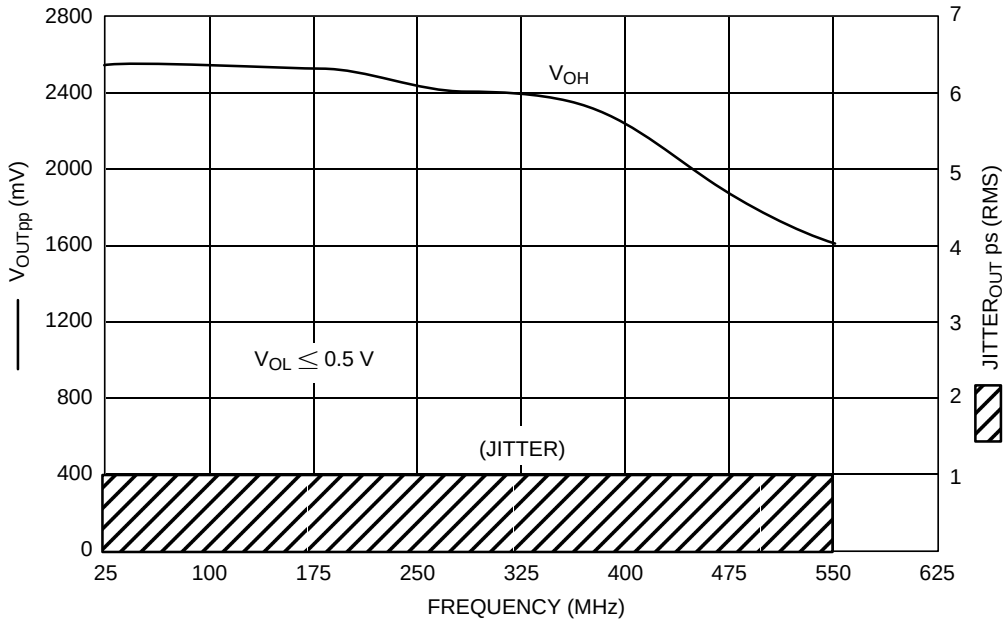



**Figure 2. $F_{max}$/Jitter**

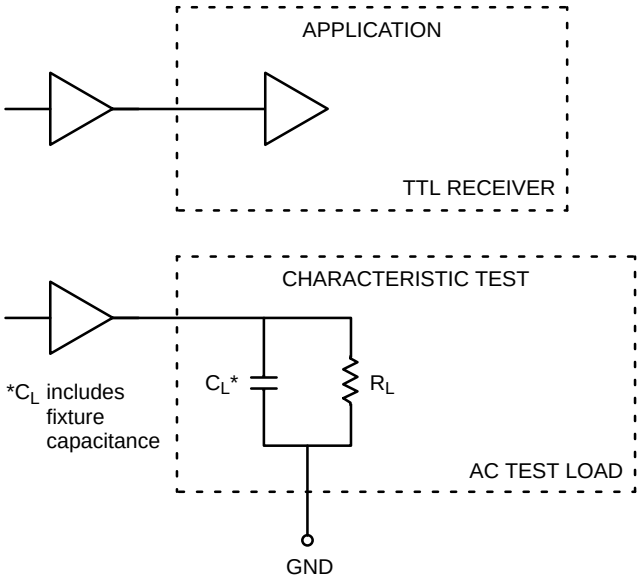



**Figure 3. TTL Output Loading Used for Device Evaluation**

## Resource Reference of Application Notes

**AN1404** − ECLinPS Circuit Performance at Non−Standard $V_{IH}$ Levels

**AN1405** − ECL Clock Distribution Techniques

**AN1406** − Designing with PECL (ECL at +5.0 V)

**AN1504** − Metastability and the ECLinPS Family

**AN1568** − Interfacing Between LVDS and ECL

**AN1650** − Using Wire−OR Ties in ECLinPS Designs

**AN1672** − The ECL Translator Guide

**AND8001** − Odd Number Counters Design

**AND8002** − Marking and Date Codes

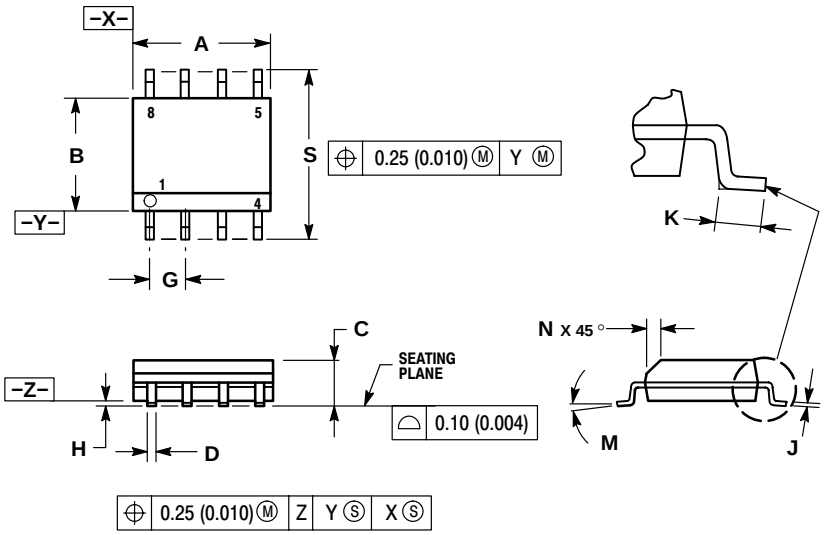
**AND8009** − ECLinPS Plus Spice I/O Model Kit

**AND8020** − Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

## PACKAGE DIMENSIONS

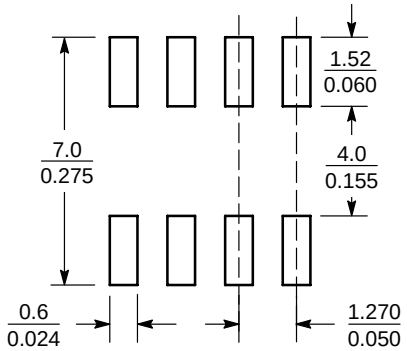
**SOIC−8**
**D SUFFIX**
CASE 751−07
ISSUE AD




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

### SOLDERING FOOTPRINT*

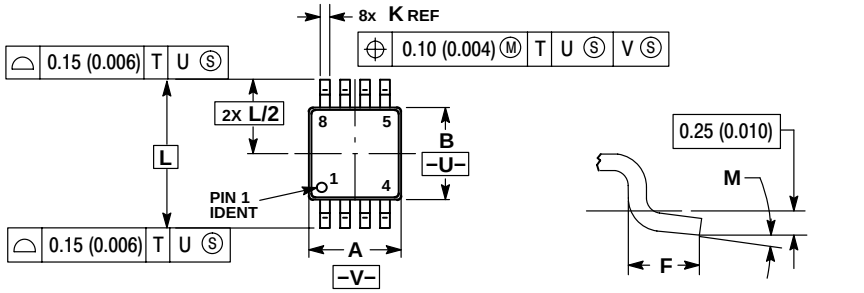



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

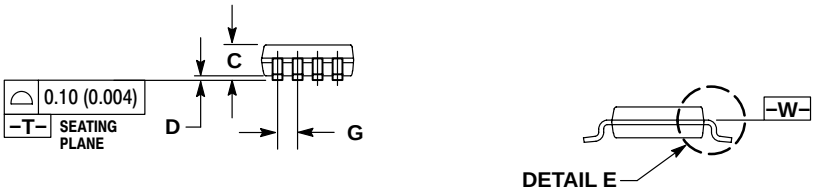
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**TSSOP−8**
**DT SUFFIX**
PLASTIC TSSOP PACKAGE
CASE 948R−02
ISSUE A



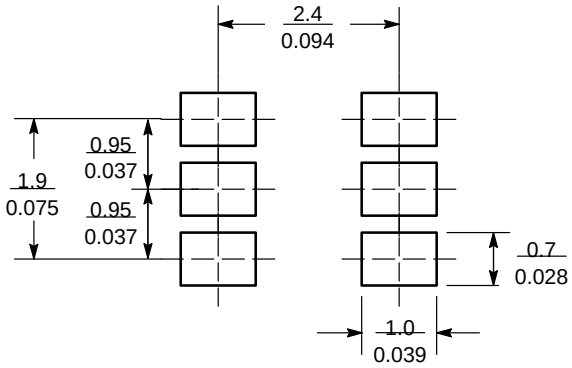

**DETAIL E**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

## SOLDERING FOOTPRINT*




SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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