DL111/D
Rev. 9, Oct-2004

ON Semiconductor®

Bipolar Power Transistor Data

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DL111/D
Rev. 9, Oct−2004

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Selector Guide

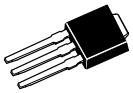
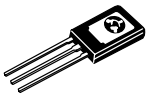
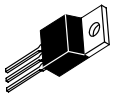
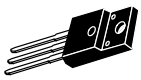
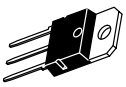
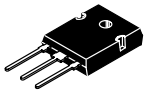
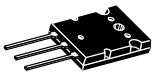
Bipolar Power Transistors

In Brief . . .

ON Semiconductor's broad line of Bipolar Power Transistors includes discrete and Darlington transistors in a variety of packages from the popular surface mount DPAK at 1.75 watts to the 250 watt TO-3. We also have transistors in the smaller SO−8 (Dual Transistors) and SOT−223 packages. We have a broad line of Electronic Lamp Ballast Transistors, in the BUL Series and MJD18002D2T4, MJE18002, and MJE18004D24. New products include the high gain, low $V_{CE(sat)}$ NJD2873 surface mount DPAK and a number of new audio transistors. The MJL4302A/MJL4281A reach higher voltages than previously available in an audio output transistor while the MJL31193/MJL31194 provide leading safe operating area performance. We also have a broad line of high performance audio output transistors in TO−3, TO−264 and the TO−247 package. These have excellent high voltage FBSOA performance. ON Semiconductor has a commitment to quality and total customer satisfaction.

BIPOLAR POWER TRANSISTORS SELECTOR GUIDE

SELECTION BY PACKAGE

Package		I_C Range (Amps)	V_{CE} Range (Volts)	P_D (Watts)
	**SO−8**	3.0	30	2.0 (Note 2)
	**SOT−223**	0.5−3.0	30	2.0 (Note 1)
	**DPAK**	0.5-10	40-450	12.5-25
	**D^2PAK**	5.0−15	80−450	50−75
	**DPAK**	0.5-10	40-450	12.5-25
	**TO-225AA (TO-126)**	0.3-5.0	25-400	12.5-50
	**TO-220AB**	0.5-15	32-400	30-150
	**Isolated TO-220**	1.0-12	60-450	28-45
	**TO−218**	10−25	60−350	80−150
	**TO−247**	8.0−30	150−250	100−200
	**TO-264**	15-20	200-350	200−250
	**TO-204AA (TO-3)**	4.0-30	40-250	115-250
	**TO-204AE (TO−3)**	30−60	60-250	150-300

1. Tested on 1″ sq. FR4 Board.
2. Tested on 1″ sq., 2 oz. copper.

SO−8 (Dual Transistors)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
3.0	30	MMDJ3N03BJTR2	MMDJ3P03BJTR2	50	1.0				30	2.0

SOT−223

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
0.5	30		MMJT350T1	30/240	0.05					0.8
3.0	30	MMJT9410T1	MMJT9435T1	50	1.0					0.8

DPAK

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
0.5	300	MJD340T4	MJD350T4	30/240	0.05					15
1.0	250	MJD47T4		30/150	0.3	2.0	0.2	0.3	10	15
	350		MJD5731T4	10 min	1.0				10	15
	400	MJD50T4		30/150	0.3	2.0	0.2	0.3	10	15
2.0	45		MJD148T4	50 min	2.0				3.0	20
	50	NJD2873T4		40 min	2.0				30	12.5
	100	MJD112T4 (Note 3)	MJD117T4 (Note 3)	1000 min	2.0	1.7	1.3	2.0	25	20
	450	MJD18002D2T4		6.0 min	2.0	1.0 typ	0.15 typ	1.0	13 typ	25
3.0	40	MJD31T4	MJD32T4	10 min	1.0	0.6	0.3	1.0	3.0	15
	100	MJD31CT4	MJD32CT4	10 min	1.0	0.6	0.3	1.0	3.0	15
4.0	80	MJD6039T4 (Note 3)		1k/2k	2.0	1.7	1.2	2.0	25	20
		TIP131 (Note 3)		1k/15k	4.0					70
	100	MJD243T4	MJD253T4	40/180	0.2	0.16	0.04	1.0	40	12.5
		TIP132 (Note 3)	TIP137 (Note 3)	1k/15k	4.0					70
5.0	25	MJD200T4	MJD210T4	45/180	2.0	0.15	0.04	2.0	65	12.5
6.0	100	MJD41CT4	MJD42CT4	15/75	3.0	0.4	0.15	3.0	3.0	20
8.0	80	MJD44H11T4	MJD45H11T4	40 min	4.0	0.5	0.14	5.0	50 typ	20
	100	MJD122T4 (Note 3)	MJD127T4 (Note 3)	1k/2k	4.0	1.5	2.0	4.0	4	20
	120		MJD128T4 (Note 3)	1k/2k	4.0				4	20
10	60	MJD3055T4	MJD2955T4	20/100	4.0	1.5	1.5	3.0	2.0	20
	80	MJD44E3T4 (Note 3)		1k min	5.0	2.0	0.5	10		20

3. Darlington.
4. Switching test performed with special application circuit.

D^2PAK

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
6.0	100	MJB41CT4	MJB42CT4	15/75	3.0				3.0	65
8.0	80	MJB44H11T4	MJB45H11T4	40/100	4.0	0.5 typ	0.14	5.0	40	50
10	350	BUB323Z		500/3400	5.0	(Note 5)			2.0	75
15	80	MJB6488	MJB6491	20/150	5.0				5.0	75

TO−225AA (TO−126)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
0.3	350	MJE3439		40/160	0.02				15	15
0.5	200	MJE344		30/300	0.05				15	20.8
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
	300	MJE340	MJE350	30/240	0.05					20.8
	350	2N5657		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD159		30/240	0.05					20
1.0	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30
	80	2N4923	2N4920	20/100	0.5	0.6 typ	0.3 typ	0.5	3.0	30
1.5	45	BD135	BD136	40/250	0.15					12.5
	60	BD137	BD138	40/250	0.15					12.5
	80	BD139	BD140	40/250	0.15					12.5
	400	MJE13003 (Note 7)		5/25	1.0	4.0	0.7	1.0	5.0	40
2.0	45		BD234	25 min	1.0				3.0	25
	80	BD237	BD238	25 min	1.0				3.0	25
	100	MJE270 (Notes 6 & 7)	MJE271 (Notes 6 & 7)	1.5k min	0.12				6.0	15
3.0	40	MJE180	MJE170	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	80	BD179	BD180	40/250	0.15					25
		MJE182	MJE172	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	500	BUH51 (Note 7)		8.0 min	1.0					50

5. Switching test performed with special application circuit.
6. Darlington.
7. Style 3.

TO−225AA (TO−126) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
4.0	32	BD435	BD436	50 min	2.0				3.0	36
	40	MJE521	MJE371	40 min	1.0					40
			2N6034 (Note 9)	25 min	1.5				2.0	40
		2N5190		25 min	1.5				2.0	40
	45	BD437	BD438	40 min	2.0				3.0	36
		BD675 (Note 9)	BD676 (Note 9)	750	1.5				3.0	40
		BD675A (Note 9)	BD676A (Note 9)	750	2.0				3.0	40
	60	BD439	BD440	25 min	2.0				3.0	36
		BD677 (Note 9)	BD678 (Note 9)	750 min	1.5					40
		BD677A (Note 9)	BD678A (Note 9)	750 min	2.0					40
		BD787	BD788	20 min	2.0				50	15
		2N5191	2N5194	25/100	1.5	0.4 typ	0.4 typ	1.5	2.0	40
		MJE800 (Note 9)	MJE700 (Note 9)	750 min	1.5				1.0	40
		2N6038 (Note 9)	2N6035 (Note 9)	750/18k	2.0	1.7 typ	1.2 typ	2.0	25	40
	80	2N5192	2N5195	25/100	1.5	0.4 typ	0.4 typ	1.5	2.0	40
		BD441	BD442	15 min	2.0				3.0	36
		BD679 (Note 9)	BD680 (Note 9)	750 min	1.5					40
		BD679A (Note 9)	BD680A (Note 9)	750 min	2.0					40
		MJE802 (Note 9)	MJE702 (Note 9)	750 min	1.5				1.0	40
		MJE803 (Note 9)	MJE703 (Note 9)	750 min	2.0				1.0	40
		2N6039 (Note 9)	2N6036 (Note 9)	750/18k	2.0	1.7 typ	1.2 typ	2.0	25	40
	100	BD681 (Note 9)	BD682 (Note 9)	750 min	1.5					40
		MJE243	MJE253	40/120	0.2	0.15 typ	0.07 typ	2.0	40	15
5.0	25	MJE200	MJE210	45/180	2	0.13 typ	0.035 typ	2.0	65	15

8. Switching test performed with special application circuit.
9. Darlington.
10. Style 3.

TO−220AB

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 14)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
1.0	40	TIP29	TIP30	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30
	60	TIP29A	TIP30A	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30
	80	TIP29B	TIP30B	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30
	100	TIP29C	TIP30C	15/75	1.0	0.6 typ	0.3 typ	1.0	3.0	30
	250	TIP47		30/150	0.3	2.0 typ	0.18 typ	0.3	10	40
	300	TIP48	MJE5730	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40
	350		MJE5731	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40
	400	TIP50	MJE5731A (Note 13)	30/150	0.3	2.0 typ	0.18 typ	0.3	10	40
2.0	60	TIP110 (Note 11)	TIP115 (Note 11)	500 min	2.0	1.7 typ	1.3 typ	2.0	25	50
	80	TIP111 (Note 11)	TIP116 (Note 11)	500 min	2.0	1.7 typ	1.3 typ	2.0	25	50
	100	TIP112 (Note 11)	TIP117 (Note 11)	500 min	2.0	1.7 typ	1.3 typ	2.0	25	50
	400/700	BUL44		14/36	0.4	2.75 (Note 12)	0.175 (Note 12)	1.0	13 typ	50
	450/1000	BUX85		30	0.1	3.5	1.4	1.0	4.0	50
		MJE18002		14/34	0.2	3.0 (Note 12)	0.17 (Note 12)	1.0	12 typ	40
3.0	40	TIP31	TIP32	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40
	60	TIP31A	TIP32A	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40
	80		BD242B	25 min	1.0				3.0	40
		TIP31B	TIP32B	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40
	100	BD241C	BD242C	25 min	1.0				3.0	40
		TIP31C	TIP32C	25 min	1.0	0.6 typ	0.3 typ	1.0	3.0	40
	440/825	BUL642D2		16 min	0.5	0.5 typ	0.4 typ	0.5	13 typ	75
4.0	80	D44C12	D45C12	40/120	0.2			1.0	40 typ	30
	350	MJE15034	MJE15035	10 min	2.0				30	50
	400/700	MJE13005		6/30	3.0	3.0	0.7	3.0	4.0	60
		BUL42D		10	2.0		0.8	2.5	20 typ	75
	500/800	BUH50		10 typ	2.0	1.2	0.15	2.0	4.0	50
5.0	60	TIP120 (Note 11)	TIP125 (Note 11)	1k min	3.0	1.5 typ	1.5 typ	3.0	4.0	65
	80	TIP121 (Note 11)	TIP126 (Note 11)	1k min	3.0	1.5 typ	1.5 typ	3.0	4.0	65
	100	TIP122 (Note 11)	TIP127 (Note 11)	1k min	3.0	1.5 typ	1.5 typ	4.0	4.0	75

11. Darlington.
12. Switching tests performed with special application simulator circuit. See data sheet for details.
13. V_{CEO} = 375 V.
14. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

TO−220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 17)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
5.0	250	2N6497		10/75	2.5	1.8	0.8	2.5	5.0	80
	400/700	BUL45		14/34	0.3	1.7 (Note 16)	0.15 (Note 16)	1.0	12 typ	75
		BUL45D2		22 min	0.8			1.0	13 typ	75
	450/1000	MJE18004		14/34	0.3	1.7	0.15	1.0	13	75
		MJE18004D2*								
6.0	40	TIP41	TIP42	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65
	60	TIP41A	TIP42A	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65
	80	TIP41B	TIP42B	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65
		BD243B	BD244B	15 min	3.0	0.4 typ	0.15 typ	3.0	3.0	65
	100	BD243C	BD244C	15 min	3.0	0.4 typ	0.15 typ	3.0	3.0	65
		TIP41C	TIP42C	15/75	3.0	0.4 typ	0.15 typ	3.0	3.0	65
	400/700	BUL146		14/34	0.5	1.75 (Note 16)	0.15 (Note 16)	3.0	14 typ	100
	450/1000	MJE18006		14/34	0.5	3.2 (Note 16)	0.13 (Note 16)	3.0	14 typ	100
7.0	30	2N6288	2N6111	30/150	3.0	0.4 typ	0.15 typ	3.0	4.0	40
	50		2N6109	30/150	2.5	0.4 typ	0.15 typ	3.0	4.0	40
	70	2N6292	2N6107	30/150	2.0	0.4 typ	0.15 typ	3.0	4.0	40
	150	BU407		30 min	1.5		0.75	5.0	10	60
	200	BU406		30 min	1.5		0.75	5.0	10	60
8.0	60	2N6043 (Note 15)	2N6040 (Note 15)	1k/10k	4.0	1.5 typ	1.5 typ	3.0	4.0	75
		TIP100 (Note 15)	TIP105 (Note 15)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0	80
	80	BDX53B (Note 15)	BDX54B (Note 15)	750 min	3.0				4.0	60
		TIP101 (Note 15)	TIP106 (Note 15)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0	80
	100	2N6045 (Note 15)	2N6042 (Note 15)	1k/10k	3.0	1.5 typ	1.5 typ	3.0	4.0	75
		BDX53C (Note 15)	BDX54C (Note 15)	750 min	3.0					
		TIP102 (Note 15)	TIP107 (Note 15)	1k/20k	3.0	1.5 typ	1.5 typ	3.0	4.0	80
	120	MJE15028	MJE15029	20 min	4.0				30	50
	150	MJE15030	MJE15031	20 min	4.0				30	50

15. Darlington.
16. Switching tests performed with special application simulator circuit. See data sheet for details.
17. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

*D2 suffix indicates transistor with built in C−E freewheeling diode and antisaturation network.

TO−220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 20)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
8.0	250	MJE15032	MJE15033	10 min	2.0				30	50
	300/600	MJE5740 (Note 18)		200 min	4.0	8.0 typ	2.0 typ	6.0	4.0	80
	300		MJE5850	15 min	2.0	2.0	0.5	4.0		80
	350		MJE5851	15 min	2.0	2.0	0.5	4.0		80
	400	MJE5742 (Note 18)		200 min	4.0	8.0 typ	2.0 typ	6.0		80
		MJE13007		5/30	5.0	3.0	0.7	5.0		80
			MJE5852	15 min	2.0	2.0	0.5	4.0		80
	400/700	BUL147		14/34	1.0	2.5 (Note 19)	0.18 (Note 19)	2.0	14 typ	125
	450/1000	MJE18008		16/34	1.0	2.75 (Note 19)	0.18 (Note 19)	2.0	13 typ	125
10	60	D44H8	D45H8	40 min	4.0					50
		MJE3055T	MJE2955T	20/70	4.0					75
		2N6387 (Note 18)	2N6667 (Note 18)	1k/20k	5.0				20	65
	80	BDX33B (Note 18)	BDX34B (Note 18)	750 min	3.0				3.0	70
		BD809	BD810	15 min	4.0				1.5	90
		2N6388 (Note 18)	2N6668 (Note 18)	1k/20k	5.0				20	65
		D44H11	D45H11	40 min	4.0	0.5 typ	0.14 typ	5.0	50 typ	50
	100	BDX33C (Note 18)	BDX34C (Note 18)	750 min	3.0				3.0	70
	400/700	BUH100		6.0 min	10	2.5 typ	0.15 typ	1.0	23 typ	100
12	90	BUV26		12 min	12	1.0	0.15	12	30 typ	85
	120	BUV27		12 min	8.0	0.5 typ	0.12 typ	8.0	30 typ	70
	400/700	MJE13009		6/30	8.0	3.0	0.7	8.0	4.0	100
15	60	2N6487	2N6490	20/150	5.0	0.6 typ	0.3 typ	5.0	5.0	75
	80	2N6488	2N6491	20/150	5.0	0.6 typ	0.3 typ	5.0	5.0	75
			BDW46 (Note 18)	1k min	5.0				4.0	85
		D44VH10	D45VH10	20 min	4.0	0.5	0.09	8.0	50 typ	83
	100	BDW42 (Note 18)	BDW47 (Note 18)	1k min	5.0	1.0 typ	1.5 typ	5.0	4.0	85
	400/700	BUH150		4.0 min	20	5.0 typ	0.11 typ	2.0	23 typ	150

18. Darlington
19. Switching tests performed with special application simulator circuit. See data sheet for details.
20. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Isolated TO-220

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
			NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
1.0	250		MJF47		30/150	0.3	2.0 typ	0.17 typ	0.3	10	28
3.0	100		MJF31C	MJF32C	10 min	1.0	0.6	0.3	1.0	3.0	28
5.0	100		MJF122 (Note 21)	MJF127 (Note 21)	2000 min	3.0	1.5 typ	1.5 typ	3.0	4.0	28
	450	1000	MJF18004		14/34	0.3	1.7 (Note 22)	0.15 (Note 22)	1.0	13 typ	35
6.0	400	700	BUL146F		14/34	0.5	2.5 (Note 22)	0.15 (Note 22)	3.0	14 typ	40
8.0	150		MJF15030	MJF15031	40 min	3.0	1.0 typ	0.15 typ	3.0	30	35
	450	1000	MJF18008		16/34	1.0	2.75 (Note 22)	0.18 (Note 22)	2.0	13 typ	45
10	60		MJF3055	MJF2955	20/100	4.0				2.0	40
	80		MJF44H11	MJF45H11	40/100	4.0	0.5 typ	0.14 typ	5.0	40	35
	100		MJF6388 (Note 21)	MJF6668 (Note 21)	3k/20k	3.0	1.5 typ	1.5 typ		20	40

TO−218

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 23)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
10	60	TIP33A		20/100	3.0				3.0	80
		TIP140 (Note 21)	TIP145 (Note 21)	500 min	10	2.5 typ	2.5 typ	5.0	4.0	125
		TIP141 (Note 21)	TIP146 (Note 21)	500 min	10	2.5 typ	2.5 typ	5.0	4.0	125
	100	BDV65B (Note 21)	BDV64B (Note 21)	1k min	5.0					125
		TIP33C		20/100	3.0				3.0	80
		TIP142 (Note 21)	TIP147 (Note 21)	500 min	10	2.5 typ	2.5 typ	5.0	4.0	125
	350	BU323Z (Note 21)		500/3400	5.0			6.0		150
15	60	TIP3055	TIP2955	5 min	10				2.5	80
	150	MJH11018 (Note 21)	MJH11017 (Note 21)	400/15k	10				3.0	150
	200	MJH11020 (Note 21)	MJH11019 (Note 21)	400/15k	10				3.0	150
	250	MJH11022 (Note 21)	MJH11021 (Note 21)	400/15k	10				3.0	150
16	160	MJE4343	MJE4353	15 min	8.0	1.2 typ	1.2 typ	8.0	1.0	125
20	100	MJH6284 (Note 21)	MJH6287 (Note 21)	750/18k	10				4.0	125
25	60	TIP35A	TIP36A	15/75	15	0.6 typ	0.3 typ	10	3.0	125
	100	BD249C		15/75	15				3.0	125
		TIP35C	TIP36C	15/75	15	0.6 typ	0.3 typ	10	3.0	125

21. Darlington.
22. Switching tests performed with special application simulator circuit. See data sheet for details.
23. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

TO−247

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
8.0	150	MJW21192	MJW21191	15 min	8.0				4.0	100
15	230	MJW0281A	MJW0302A	60/180	5.0				30	150
		MJW3281A	MJW1302A	60/175	5.0				30	200
16	250	MJW21194	MJW21193	20/60	8.0				4.0	200
		MJW21196	MJW21195	20/60	8.0				4.0	200
30	450/1000	MJW18020		9.0 typ	20	4.75 typ	0.38 typ	10	13 typ	250

TO-264

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
15	200	MJL3281A	MJL1302A	60/175	5.0				30 typ	200
	350	MJL4281A	MJL4302A	80/250	5.0				35	230
16	250	MJL21194	MJL21193	25/75	8.0				4.0	200
		MJL21196	MJL21195	25/75	8.0				4.0	200
20	250	MJL31194	MJL31193	25/75	10				4.0	250

TO−204AA (TO−3)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 25)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
4.0	250	MJ15020	MJ15021	30 min	1.0				20	150
10	140	2N3442		20/70	4.0					117
	250	MJ15011	MJ15012	20/100	2.0					200
12	100		2N6052 (Note 24)	750/18k	6.0	1.6 typ	1.5 typ	6.0	4.0	150
15	60	2N3055	MJ2955	20/70	4.0	0.7 typ	0.3 typ	4.0	2.5	115
		2N3055A		20/70	4.0				0.8	115
	120	MJ15015	MJ15016	20/70	4.0	0.7 typ	0.3 typ	4.0	1.0	180
	140	MJ15001	MJ15002	25/150	4.0				2.0	200
	250	MJ11022 (Note 24)	MJ11021 (Note 24)	100 min	15				3.0	175
16	140	2N3773	2N6609	15/60	8.0	1.1 typ	1.5 typ	8.0	4.0	150
		2N5631	2N6031	15/60	8.0	1.2 typ	1.2 typ	8.0	1.0	200
	200	MJ15022	MJ15023	15/60	8.0				5.0	250
	250	MJ15024	MJ15025	15/60	8.0				5.0	250
		MJ21194	MJ21193	25/75	8.0				4.0	250
		MJ21196	MJ21195	25/75	8.0				4.0	250

24. Darlington.
25. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

TO−204AA (TO−3) (continued)

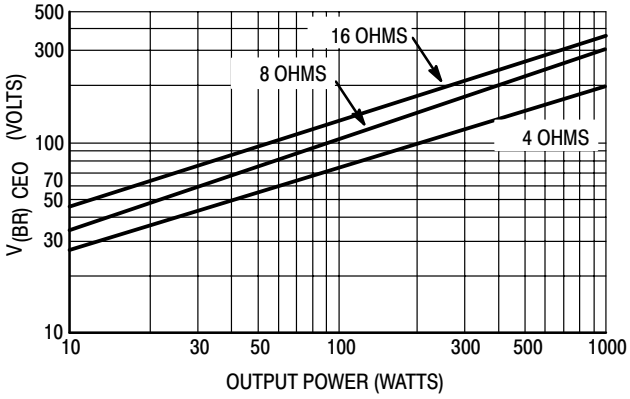
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min (Note 27)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
20	60	2N3772		15/60	10				2.0	150
		2N6282 (Note 26)		750/18k	10				4.0	160
	80		2N6286 (Note 26)	750/18k	10				4.0	160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	2N6284 (Note 26)	2N6287 (Note 26)	750/18k	10	2.5 typ	2.5 typ	10	4.0	160
	140	MJ15003	MJ15004	25/150	5.0				2.0	250
	250	MJ31194	MJ31193	25/75	10				4.0	300
25	60	2N5885	2N5883	20/100	10	1.0	0.8	10	4.0	200
	80	2N5886	2N5884	20/100	10	1.0	0.8	10	4.0	200
	100	2N6338		30/120	10	1.0	0.25	10	40	200
	150	2N6341		30/120	10	1.0	0.25	10	40	200
30	40	2N3771		15/60	15				2.0	150
	60	2N5302		15/60	15	2.0	1.0	10	2.0	200
		MJ11012 (Note 26)		1k min	20				4.0	200
	100	MJ802	MJ4502	25/100	7.5				2.0	200
	120	MJ11016 (Note 26)	MJ11015 (Note 26)	1k min	20				4.0	200
	250	MJ11022 (Note 26)	MJ11021 (Note 26)	400/15k	10				3.0	200
40	200	BUV21 (Note 28)		10 min	25	1.8	0.4	25	8.0	150
	250	BUV22 (Note 28)		10 min	20	1.1	0.35	20	8.0	250
50	60	MJ11028 (Notes 26 & 28)	MJ11029 (Notes 26 & 28)	400 min	50					300
	80	2N5686 (Note 28)	2N5684 (Note 28)	15/60	25	0.5 typ	0.3 typ	25	2.0	300
	90	MJ11030 (Notes 26 & 28)		400 min	50					300
	120	MJ11032 (Notes 26 & 28)	MJ11033 (Notes 26 & 28)	400 min	50					300
60	60		MJ14001 (Note 28)	15/100	50					300
	80	MJ14002 (Note 28)	MJ14003 (Note 28)	15/100	50					300

26. Darlington.
27. When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
28. Case 197A (TO−204AE).

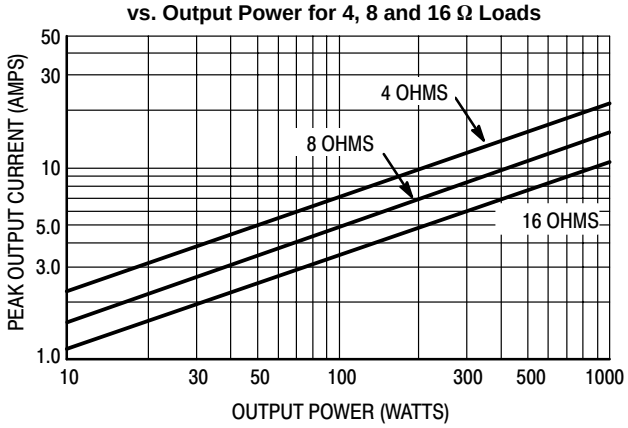
Audio

GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES

$V_{(BR)CEO}$ Required on Output and Driver Transistor vs. Output Power for 4, 8 and 18 Ω Loads



Output Transistor Peak Collector Current vs. Output Power for 4, 8 and 16 Ω Loads



Another important parameter that must be considered before selecting the output transistors is the safe−operating area these devices must withstand. For a complete discussion see Application Note AN485.

Recommended Power Transistors for Audio/Servo Loads

RMS Power Output	NPN	PNP	Package	P_D Watts @ 25°C	V_{CEO}	h_{FE} @ Min/Max	I_C Amps	f_T MHz Typ	ISB Volts/Amps
To 25 W	MJE15030	MJE15031	TO−220	50	150	20 min	4.0	30	14/3.6
	MJE15032	MJE15033	TO−220	50	250	50 min	1.0	30	50/1.0
25 to 50 W	MJE15034	MJE15035	TO−220	50	350	50 min	1.0	30	
	2N3055A	MJ2955A	TO−204	120	120	20/70	4.0	3.0	60/2.0
	MJ15001	MJ15002	TO−204	200	140	25/150	4.0	3.0	40/5.0
50 to 100 W	MJ15003	MJ15004	TO−204	150	140	25/150	5.0	3.0	100/1.0
	MJ15015	MJ15016	TO−204	180	120	20/70	4.0	3.0	60/3.0
	MJ15020	MJ15021	TO−204	250	250	30 min	1.0	30	50/3.0
Over 100 W	MJW21192	MJW21191	TO−247	100	150	15 min	4.0	4.0	50/3.0
	MJW0281A	MJW0302A	TO−247	150	230	60/180	5.0	30	
	MJL21194	MJL21193	TO−264	200	200	25/75	8.0	4.0	100/2.0
	MJL21196	MJL21195	TO−264	200	200	25/75	8.0	4.0	100/2.0
	MJW21194	MJW21193	TO−247	200	250	20/60	8.0	4.0	50/4.0
	MJW21196	MJW21195	TO−247	200	250	25/60	8.0	4.0	50/4.0
	MJL3281A	MJL1302A	TO−264	200	200	60/175	7.0	30	40/4.0
	MJW3281A	MJW1302A	TO−247	200	200	60/175	5.0	30	50/4.0
	MJL4281A	MJL4302A	TO−264	200	350	80/200	5.0	35	50/5.0
	MJL31194	MJL31193	TO−264	230	250	25/75	10	4.0	
	MJ15024	MJ15025	TO−204	250	250	15/60	8.0	4.0	80/2.2
	MJ21194	MJ21193	TO−204	250	250	25/75	8.0	4.0	100/2.0
	MJ31194	MJ31193	TO−204	300	250	25/75	10	4.0	

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe−operating area required and the mounting and heat sinking configuration used.

Bipolar Power Transistors for Electronic Lamp Ballasts

TO−220AB

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{Si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2.0	400	700	BUL44	0.8	10	2.6 / 3.8	50
	450	1000	MJE18002	1.0	6.0	/ 2.75	50
3.0	440	825	BUL642D2	0.5	16		75
4.0	500	800	BUH50	2.0	8.0 typ	/ 2.5	50
5.0	400	700	BUL45	2.0	7.0	2.6 / 3.8	75
		700	BUL45D2*	2.0	10	1.95 / 2.25	75
	450	1000	MJE18004	2.0	6.0	/ 2.5	75
		1000	MJE18004D2*	2.0	6.0	2.1 / 2.4	75
6.0	400	700	BUL146	3.0	8.0	2.6 / 3.8	100
	450	1000	MJE18006	3.0	6.0	/ 3.2	100
8.0	400	700	BUL147	4.5	8.0	2.6 / 3.8	125
	450	1000	MJE18008	4.5	6.0	/ 3.2	125
10	400	700	BUH100	5.0	10 typ	/ 3.0	100
15	400	700	BUH150	10	8.0 typ	/ 2.75	150

BUH−Series are specified for Halogen applications.
*D2 suffix indicates transistor with built in C−E freewheeling diode and antisaturation network.

Bipolar Power Transistors for Electronic Lamp Ballasts

The isolated TO−220 is UL RECOGNIZED for its isolation feature and has been evaluated to 3500 volts RMS. Actual isolation rating depends on specific mounting position and maintaining required strike and creepage distances.

Isolated TO-220

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
5.0	450	1000	MJF18004	2.0	6.0	/ 2.5	35
6.0	400	700	BUL146F	3.0	8.0	2.6 / 3.8	40
8.0	450	1000	MJF18008	4.5	6.0	/ 3.2	45

DPAK

I_C Cont Amps Max	$V_{CEO(sus)}$ /V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Inductive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
2.0	450/1000	MJD18002D2T4		6.0	1.0	1.2	0.150	1.0 A	13 typ	25

TO−225AA (TO−126)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1.0 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
1.5	400	700	MJE13003 (Note 29)	1.0	6.0 typ	/ 3.0	40
3.0	500	800	BUH51 (Note 29)	1.0	8.0	/ 3.75	50

29. Style 3.
BUH−Series are specified for Halogen applications.
*D2 suffix indicates transistor with built in C−E freewheeling diode and antisaturation network.

CHAPTER 2
Data Sheets

Complementary Silicon High-Power Transistors

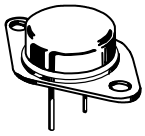
. . . PowerBase™ complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc−to−dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055.

- Current−Gain — Bandwidth−Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) − NPN
  = 2.2 MHz (Min) − PNP
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

NPN
2N3055A
MJ15015 *
PNP
MJ15016 *

***ON Semiconductor Preferred Device**

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 120 VOLTS
115, 180 WATTS



CASE 1−07
TO−204AA
(TO−3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3055A	MJ15015 MJ15016	Unit
Collector−Emitter Voltage	V_{CEO}	60	120	Vdc
Collector−Base Voltage	V_{CBO}	100	200	Vdc
Collector−Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter−Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	0.98	°C/W

*Indicates JEDEC Registered Data. (2N3055A)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 − Rev. 4
Publication Order Number:
2N3055A/D

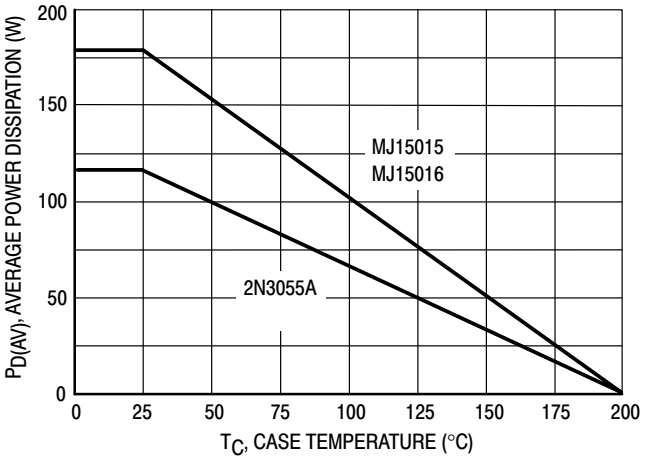


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector−Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	— —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	 2N3055A MJ15015, MJ15016	I_{CEO}	 — —	 0.7 0.1	mAdc
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A MJ15015, MJ15016	I_{CEV}	— —	5.0 1.0	mAdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N3055A MJ15015, MJ15016	I_{CEV}	 — —	 30 6.0	mAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A MJ15015, MJ15016	I_{EBO}	— —	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased (t = 0.5 s non−repetitive) (V_{CE} = 60 Vdc)	 2N3055A MJ15015, MJ15016	$I_{S/b}$	 1.95 3.0	 — —	Adc
***ON CHARACTERISTICS (1)**					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 10 20 5.0	 70 70 —	—
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc) (I_C = 15 Adc, I_B = 7.0 Adc)		$V_{CE(sat)}$	 — — —	 1.1 3.0 5.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current−Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
***SWITCHING CHARACTERISTICS (2N3055A only)**					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	—	0.5	μs
Rise Time		t_r	—	4.0	μs
Storage Time		t_s	—	3.0	μs
Fall Time		t_f	—	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data. (2N3055A)

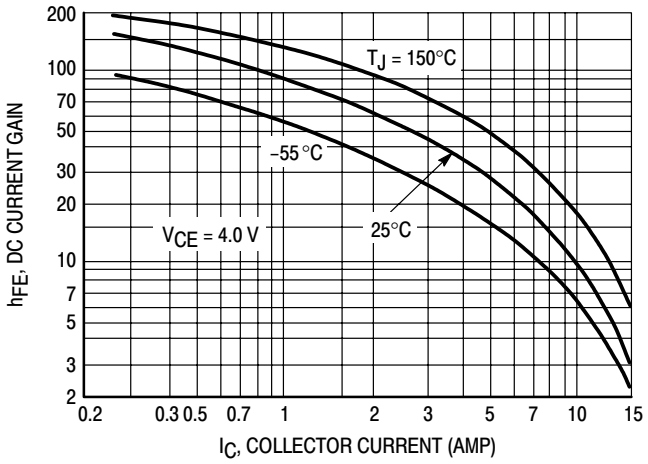


Figure 2. DC Current Gain

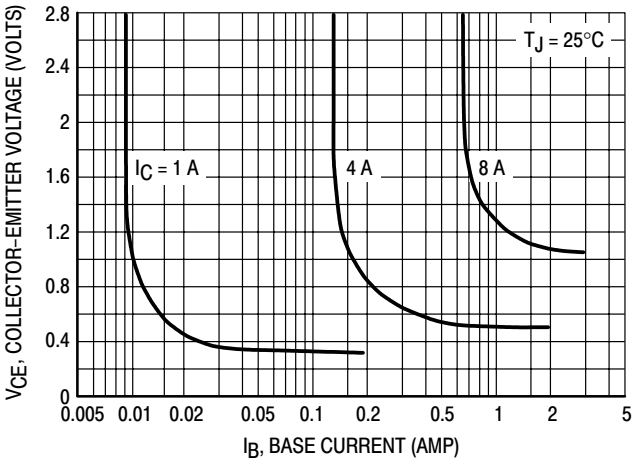


Figure 3. Collector Saturation Region

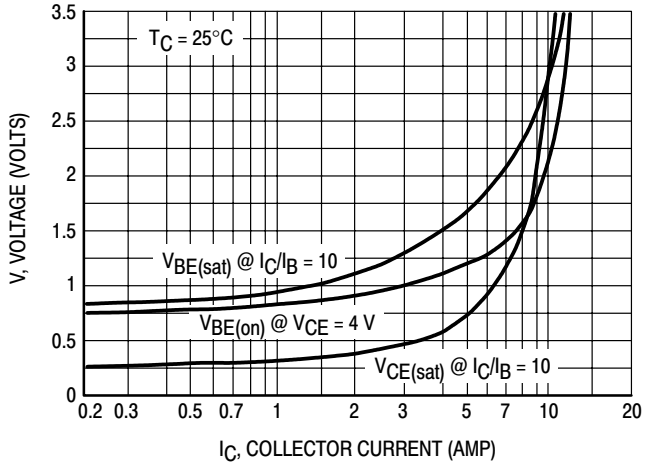


Figure 4. “On” Voltages

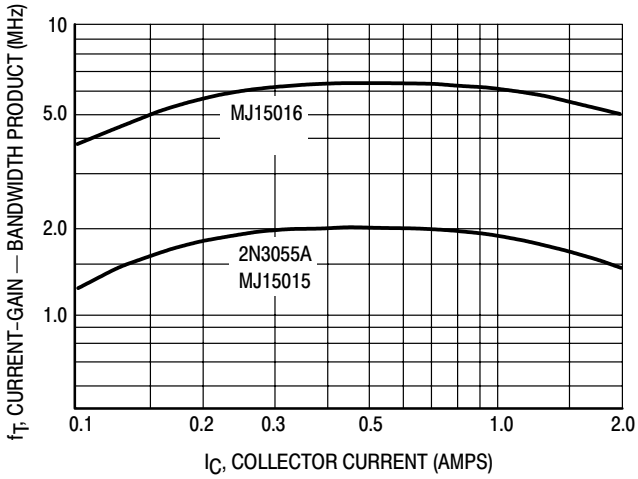


Figure 5. Current−Gain — Bandwidth Product

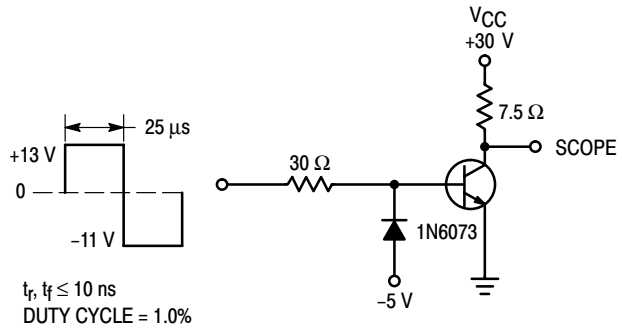


Figure 6. Switching Times Test Circuit (Circuit shown is for NPN)

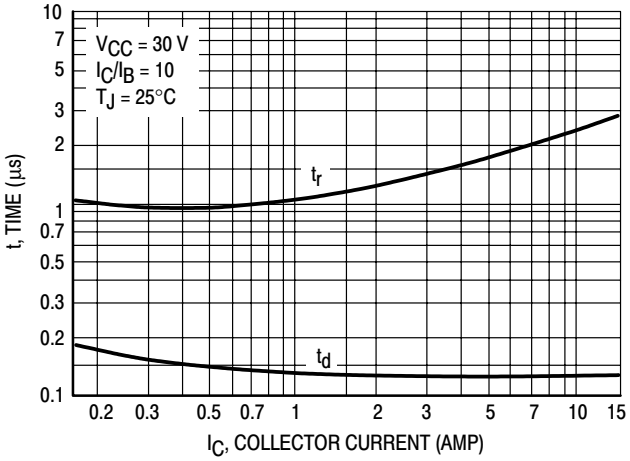


Figure 7. Turn−On Time

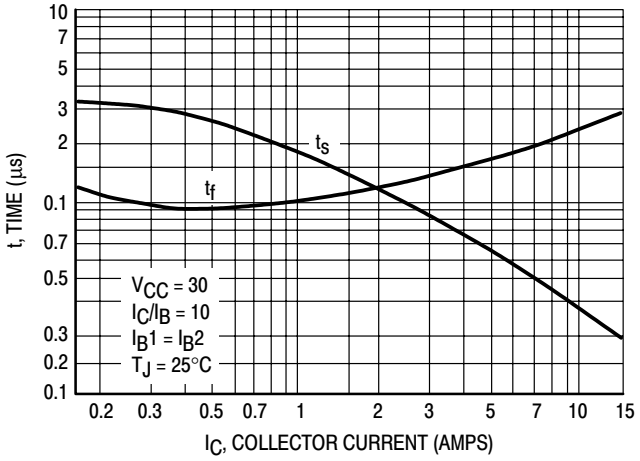


Figure 8. Turn−Off Times

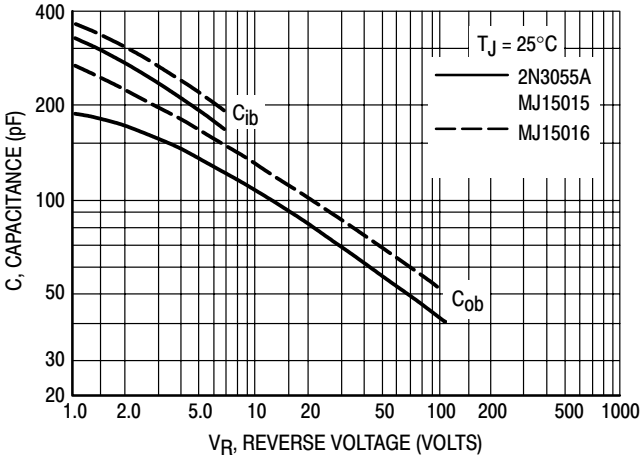


Figure 9. Capacitances

COLLECTOR CUT−OFF REGION

NPN

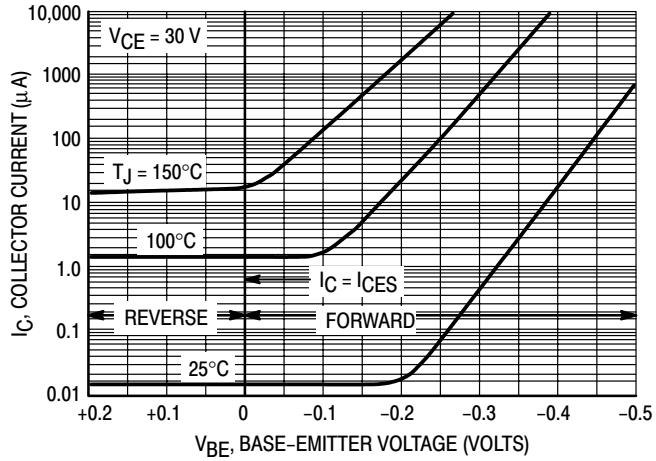


Figure 10. 2N3055A, MJ15015

PNP

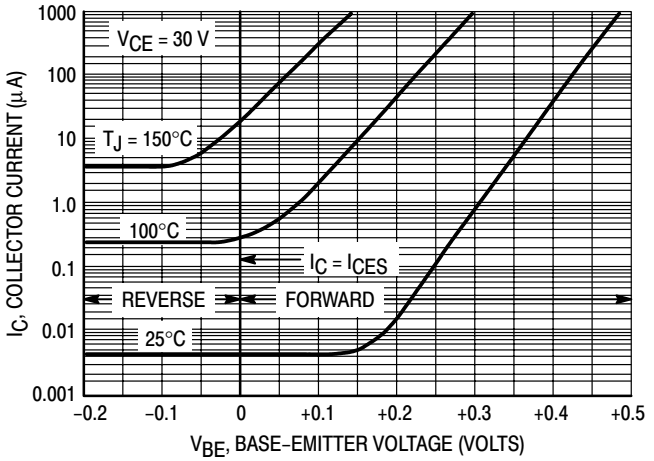


Figure 11. MJ15016

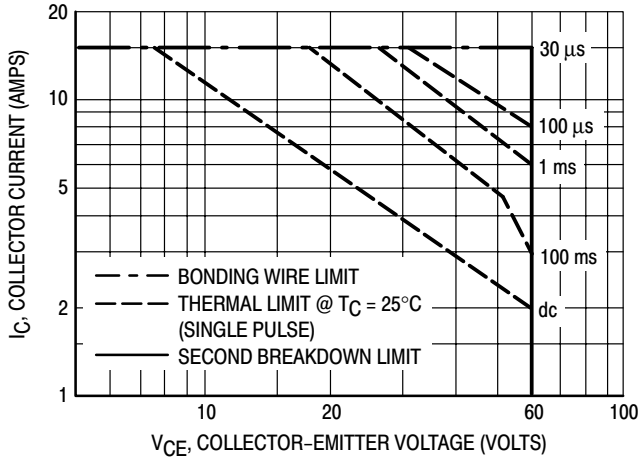


Figure 12. Forward Bias Safe Operating Area 2N3055A

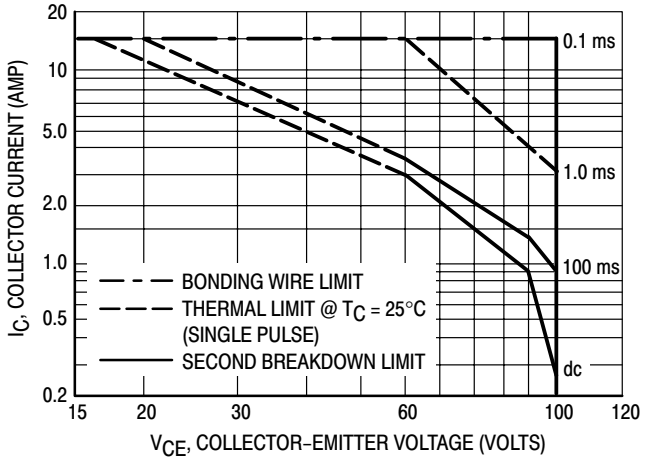


Figure 13. Forward Bias Safe Operating Area MJ15015, MJ15016

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

2N3055, MJ2955

Preferred Device

Complementary Silicon Power Transistors

. . . designed for general−purpose switching and amplifier applications.

- DC Current Gain − h_{FE} = 20−70 @ I_C = 4 Adc
- Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area
- Pb−Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Emitter Voltage	V_{CER}	70	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	7	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.52	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

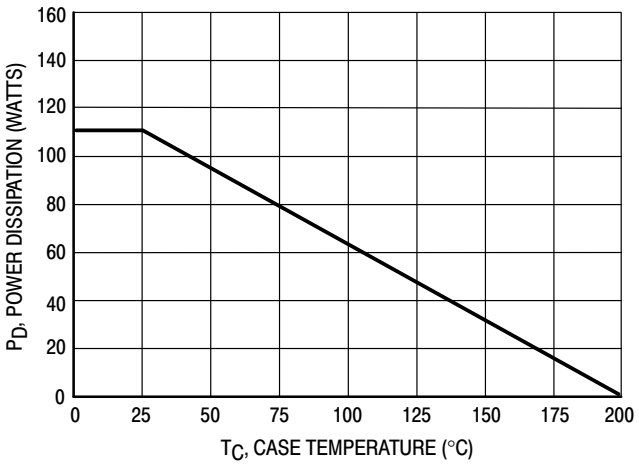
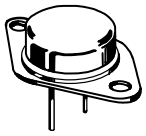


Figure 1. Power Derating

ON Semiconductor®

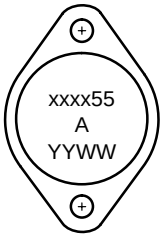
http://onsemi.com

15 A
POWER TRANSISTORS
COMPLEMENTARY SILICON
60 V
115 W



TO−204AA (TO−3)
CASE 1−07

MARKING DIAGRAM



xxxx55 = Device Code
xxxx= 2N3055 or MJ2955
A = Assembly Location
YY = Year
WW = Work Week
x = 1, 2, or 3

ORDERING INFORMATION

Device	Package	Shipping†
2N3055	TO−204AA	100 Units / Tray
2N3055G	TO−204AA (Pb−Free)	1 Units / Tubes
2N3055H	TO−204AA	100 Units / Tray
MJ2955	TO−204AA	100 Units / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	−	Vdc
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	70	−	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	−	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 − −	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	mAdc
***ON CHARACTERISTICS** (Note 1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 −	−
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	−	 1.1 3.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, Nonrepetitive)	$I_{s/b}$	2.87	−	Adc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	−	MHz
*Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	−
*Small−Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	−	kHz

*Indicates Within JEDEC Registration. (2N3055)

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

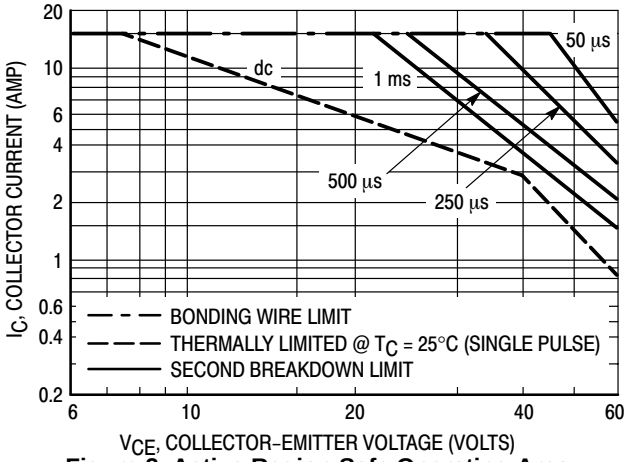


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

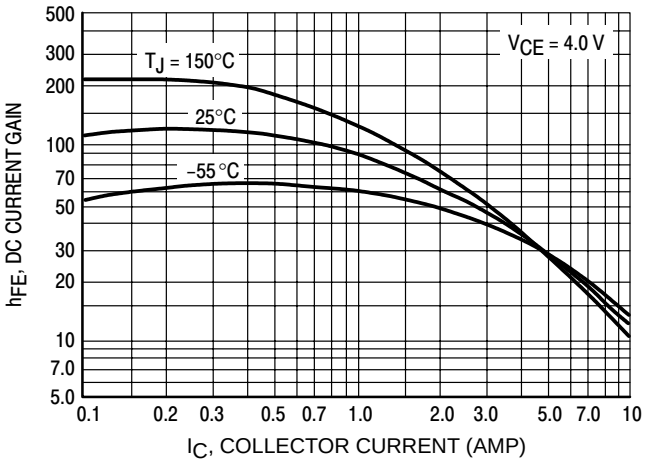


Figure 3. DC Current Gain, 2N3055 (NPN)

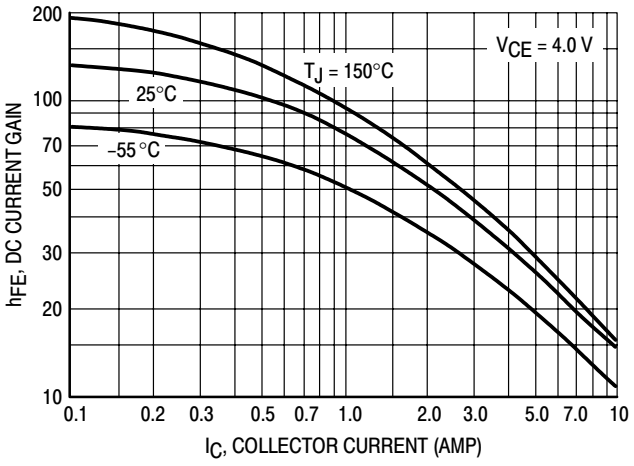


Figure 4. DC Current Gain, MJ2955 (PNP)

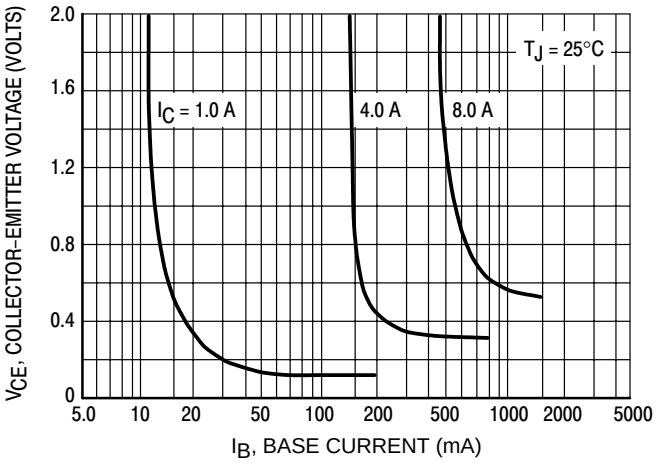


Figure 5. Collector Saturation Region, 2N3055 (NPN)

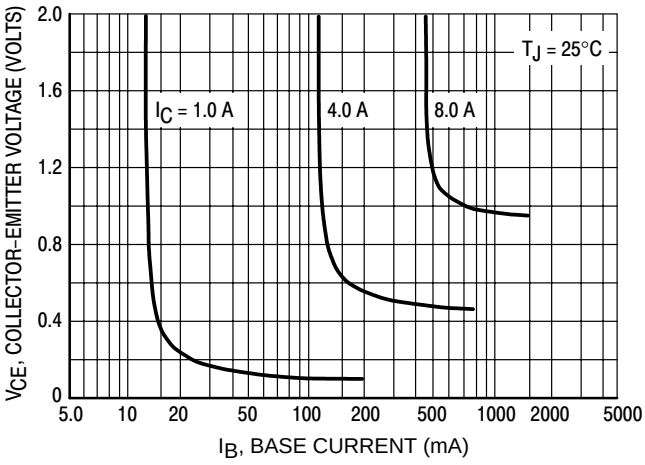


Figure 6. Collector Saturation Region, MJ2955 (PNP)

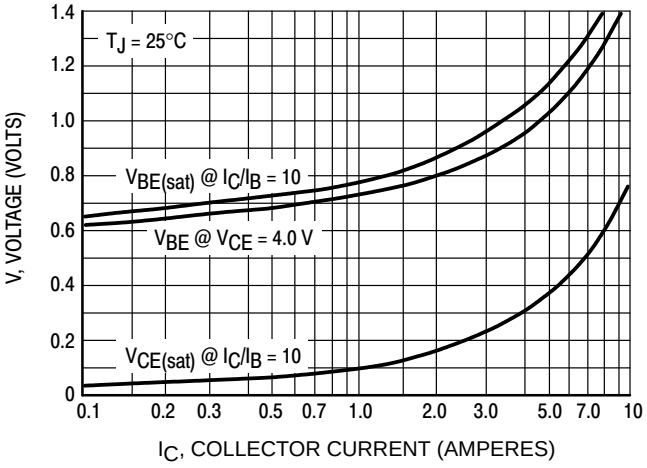


Figure 7. “On” Voltages, 2N3055 (NPN)

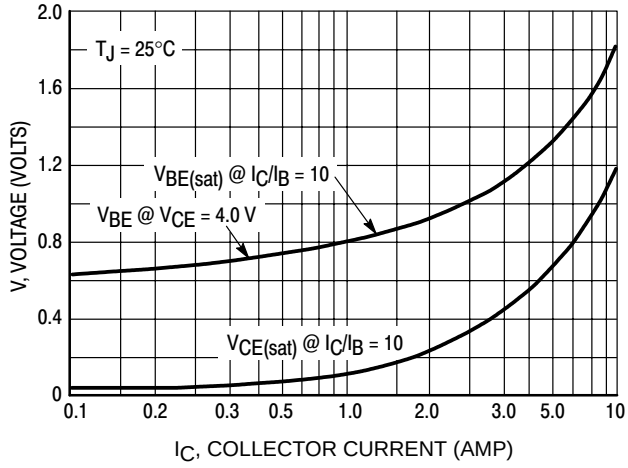


Figure 8. “On” Voltages, MJ2955 (PNP)

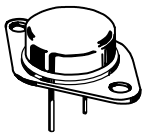
2N3442

High-Power Industrial Transistors

NPN silicon power transistor designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

- Collector −Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 140 Vdc (Min)
- Excellent Second Breakdown Capability

10 AMPERE
POWER TRANSISTOR
NPN SILICON
140 VOLTS
117 WATTS



CASE 1−07
TO−204AA
(TO−3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CB}	160	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	10 15**	Adc
Base Current — Continuous Peak	I_B	7.0 —	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

* Indicates JEDEC Registered Data.
** This data guaranteed in addition to JEDEC registered data.

March, 2001 − Rev. 10
Publication Order Number:
2N3442/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	200	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	5.0 30	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 7.5	70 —	—
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	—	5.0	Vdc
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	5.7	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (2) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	f_T	80	—	kHz
Small−Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	12	72	—

*Indicates JEDEC Registered Data.

NOTES:

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$

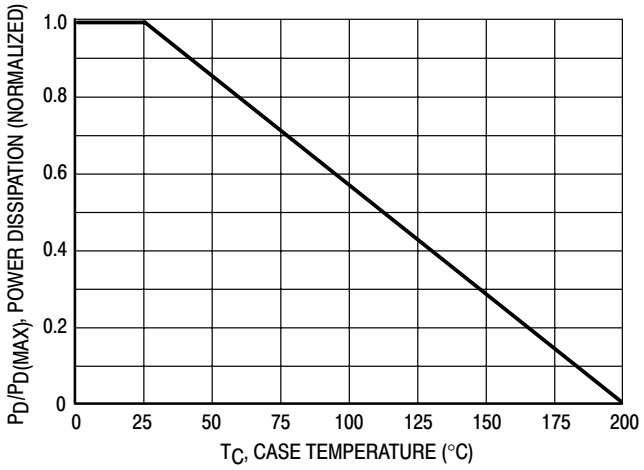


Figure 1. Power Derating

ACTIVE REGION SAFE OPERATING AREA INFORMATION

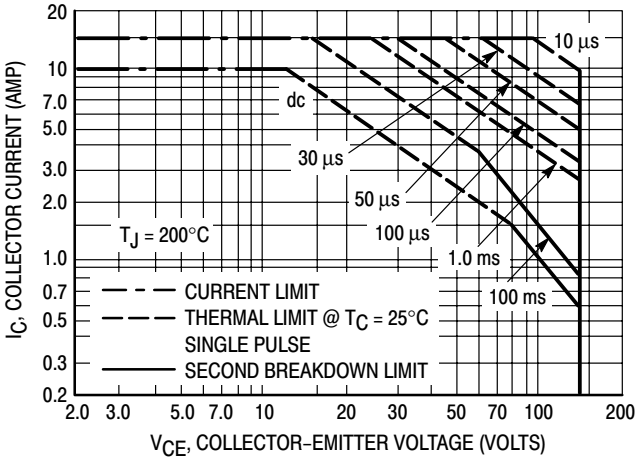


Figure 2. 2N3442

There are two limitations on the power−handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

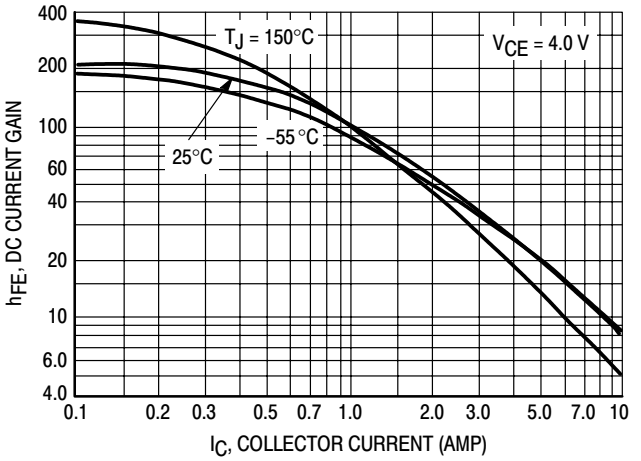


Figure 3. DC Current Gain

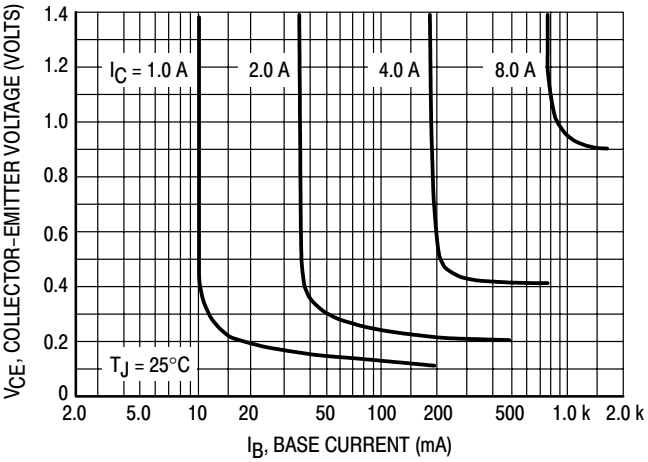


Figure 4. Collector−Saturation Region

High Power NPN Silicon Power Transistors

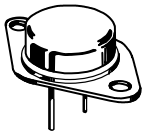
2N3771*
2N3772

*ON Semiconductor Preferred Device

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc — 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc — 2N3772

20 and 30 AMPERE POWER TRANSISTORS NPN SILICON 40 and 60 VOLTS 150 WATTS



CASE 1−07
TO−204AA
(TO−3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector−Emitter Voltage	V_{CEO}	40	60	Vdc
Collector−Emitter Voltage	V_{CEX}	50	80	Vdc
Collector−Base Voltage	V_{CB}	50	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current — Continuous Peak	I_C	30 30	20 30	Adc
Base Current — Continuous Peak	I_B	7.5 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

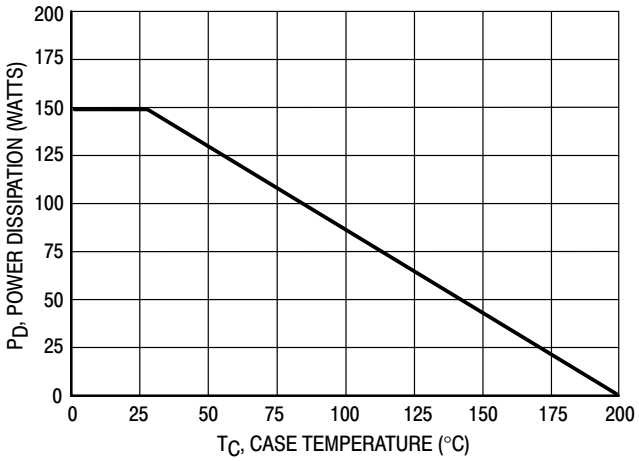


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 − Rev. 9
Publication Order Number:
2N3771/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector−Emitter Sustaining Voltage (1) (I_C = 0.2 Adc, I_B = 0)	2N3771 2N3772	$V_{CEO(sus)}$	40 60	— —	Vdc
Collector−Emitter Sustaining Voltage (I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CEX(sus)}$	50 80	— —	Vdc
Collector−Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CER(sus)}$	45 70	— —	Vdc
*Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 25 Vdc, I_B = 0)	 2N3771 2N3772	I_{CEO}	 — —	 10 10	mAdc
*Collector Cutoff Current (V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N3771 2N3772 2N6257 2N3771 2N3772	I_{CEV}	 — — — — —	 2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 2N3771 2N3772	I_{CBO}	 — —	 2.0 5.0	mAdc
*Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0) (V_{BE} = 7.0 Vdc, I_C = 0)	 2N3771 2N3772	I_{EBO}	 — —	 5.0 5.0	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (1) (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc) (I_C = 20 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772 2N3771 2N3772	h_{FE}	 15 15 5.0 5.0	 60 60 — —	—
Collector−Emitter Saturation Voltage (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 30 Adc, I_B = 6.0 Adc) (I_C = 20 Adc, I_B = 4.0 Adc)	 2N3771 2N3772 2N3771 2N3772	$V_{CE(sat)}$	 — — — —	 2.0 1.4 4.0 4.0	Vdc
Base−Emitter On Voltage (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772	$V_{BE(on)}$	 — —	 2.7 2.2	Vdc
***DYNAMIC CHARACTERISTICS**					
Current−Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	—	MHz
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non−repetitive) (V_{CE} = 40 Vdc) (V_{CE} = 60 Vdc)	 2N3771 2N3772	$I_{S/b}$	 3.75 2.5	 — —	Adc

*Indicates JEDEC Registered Data.
(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

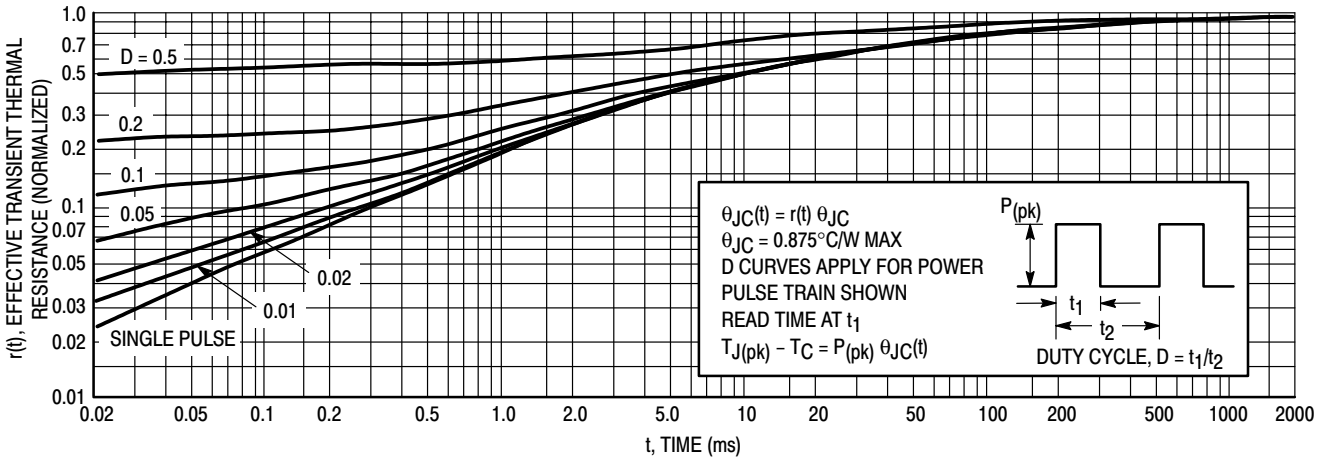


Figure 2. Thermal Response — 2N3771, 2N3772

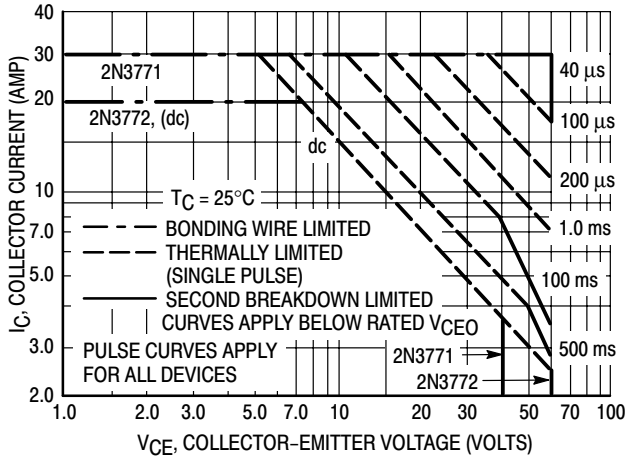


Figure 3. Active−Region Safe Operating Area — 2N3771, 2N3772

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

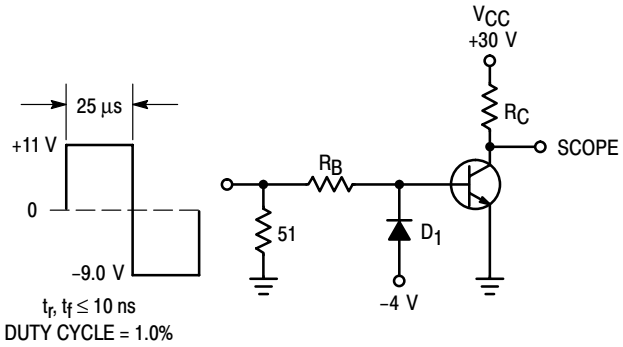


Figure 4. Switching Time Test Circuit

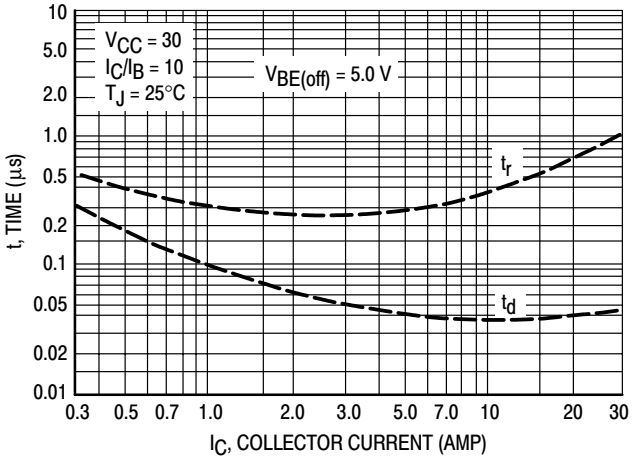


Figure 5. Turn−On Time

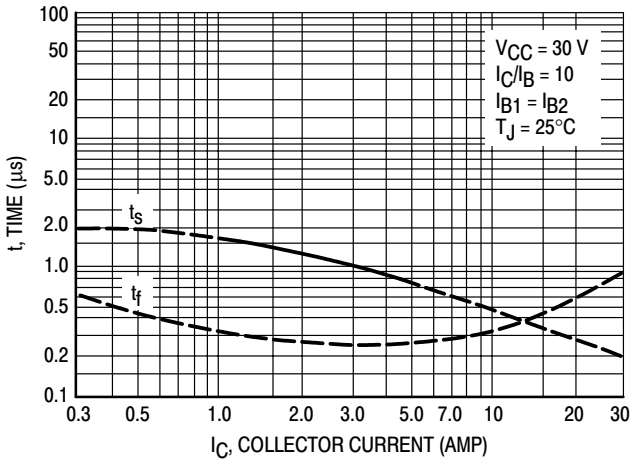


Figure 6. Turn−Off Time

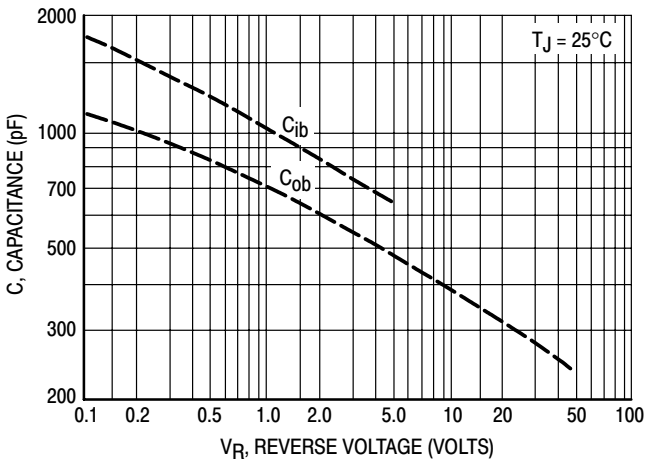


Figure 7. Capacitance

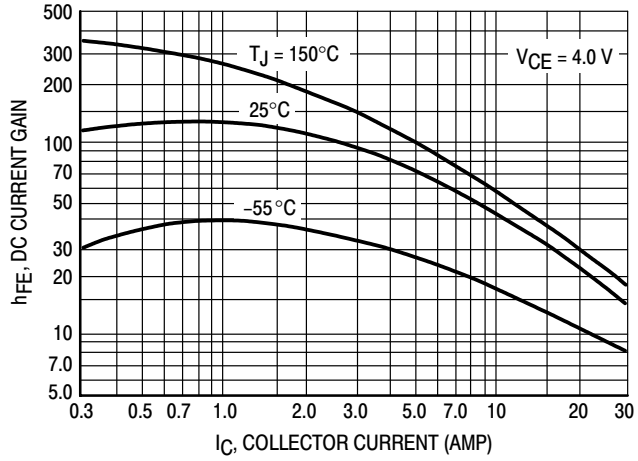


Figure 8. DC Current Gain

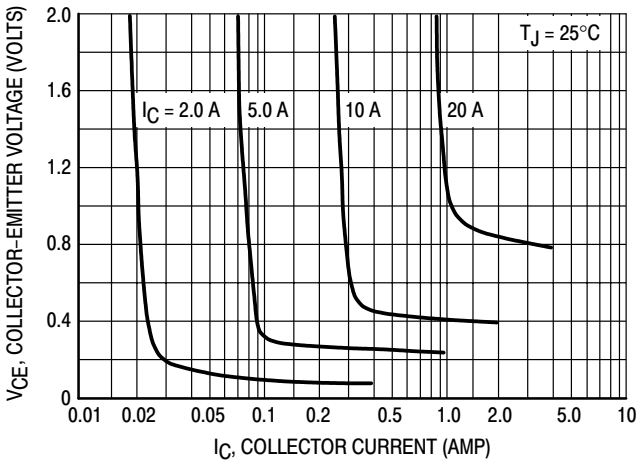


Figure 9. Collector Saturation Region

NPN 2N3773*, PNP 2N6609

Preferred Device

Complementary Silicon Power Transistors

The 2N3773 and 2N6609 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, DC−DC converters or inverters.

Features

- Pb−Free Packages are Available**
- High Safe Operating Area (100% Tested) 150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 15 (Min) @ 8.0 A, 4.0 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8.0 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	140	Vdc
Collector − Emitter Voltage	V_{CEX}	160	Vdc
Collector − Base Voltage	V_{CBO}	160	Vdc
Emitter − Base Voltage	V_{EBO}	7	Vdc
Collector Current − Continuous − Peak (Note 2)	I_C	 16 30	Adc
Base Current − Continuous − Peak (Note 2)	I_B	 4 15	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 0.855	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.
2. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

THERMAL CHARACTERISTICS

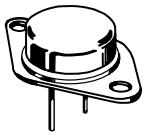
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.17	°C/W

**For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

16 A COMPLEMENTARY POWER TRANSISTORS 140 V, 150 W



TO−204
CASE 1−07

MARKING DIAGRAM

xxxx = 3773 or 6609
A = Assembly Location
YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 46 of this data sheet.

***Preferred** devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (Note 3)				
Collector−Emitter Breakdown Voltage (Note 4) (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	−	Vdc
Collector−Emitter Sustaining Voltage (Note 4) (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	−	Vdc
Collector−Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	−	Vdc
Collector Cutoff Current (Note 4) (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	−	10	mAdc
Collector Cutoff Current (Note 4) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 − −	 2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	−	2	mAdc
Emitter Cutoff Current (Note 4) (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	−	5	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (Note 4) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60 −	−
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 800 mAdc) (Note 4) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 − −	 1.4 4	Vdc
Base−Emitter On Voltage (Note 4) (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common−Emitter Small−Signal, Short−Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	−	−
Small−Signal Current Gain (Note 4) (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	−	−
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non−repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	−	Adc

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
4. Indicates JEDEC Registered Data.

ORDERING INFORMATION

Device	Package	Shipping†
2N3773	TO−204	100 Unit / Tray
2N3773G	TO−204 (Pb−Free)	100 Unit / Tray
2N6609	TO−204	100 Unit / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NPN

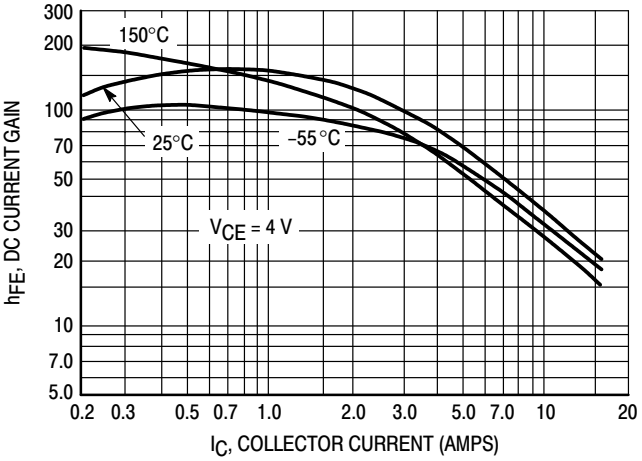


Figure 10. DC Current Gain

PNP

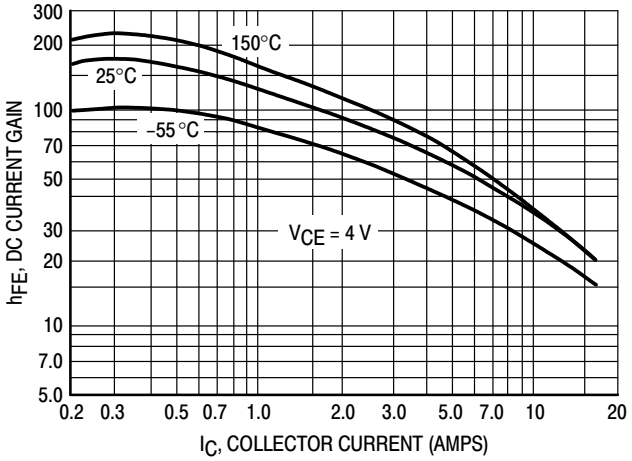


Figure 11. DC Current Gain

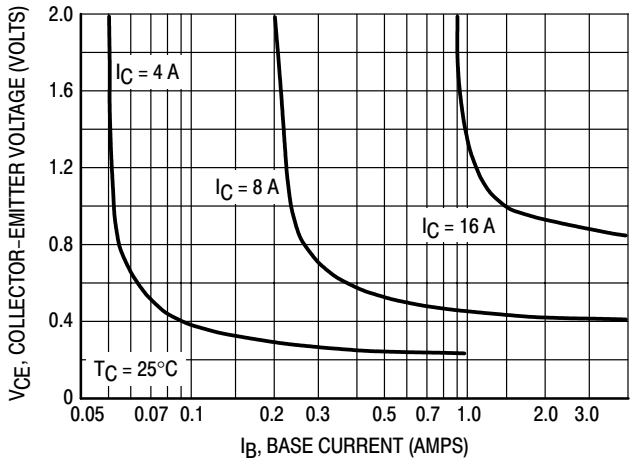


Figure 12. Collector Saturation Region

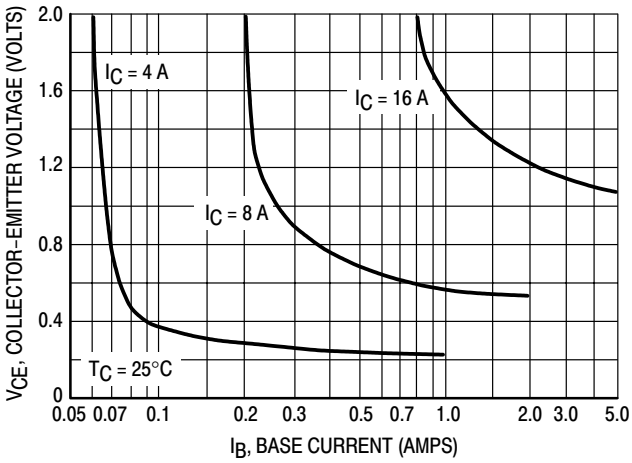


Figure 13. Collector Saturation Region

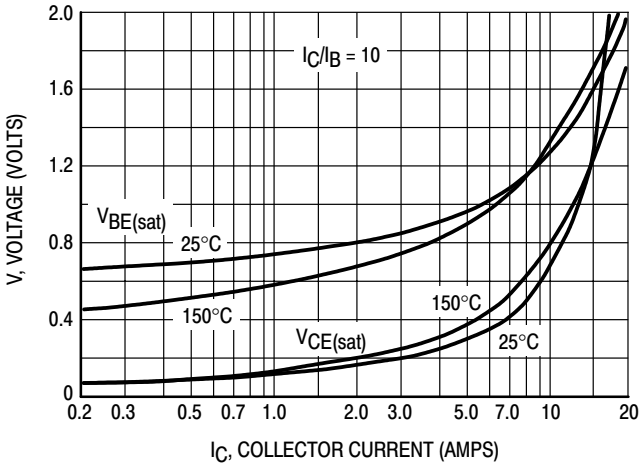


Figure 14. “On” Voltage

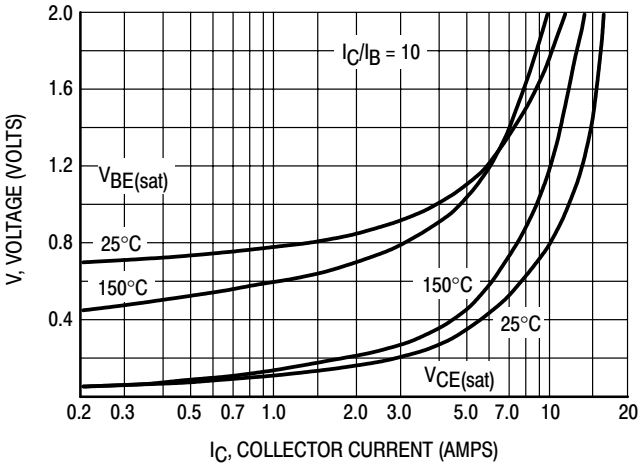


Figure 15. “On” Voltage

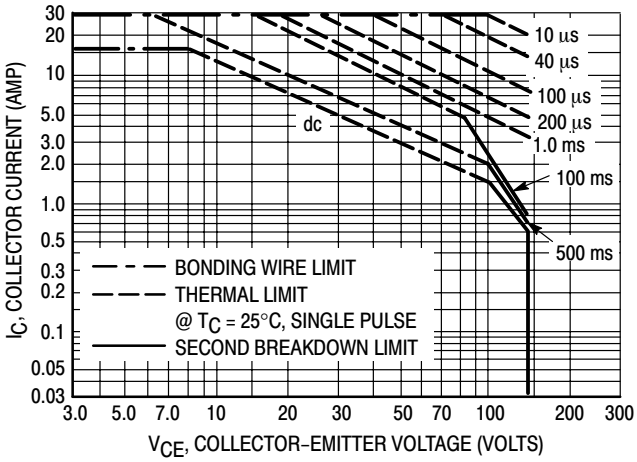


Figure 16. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

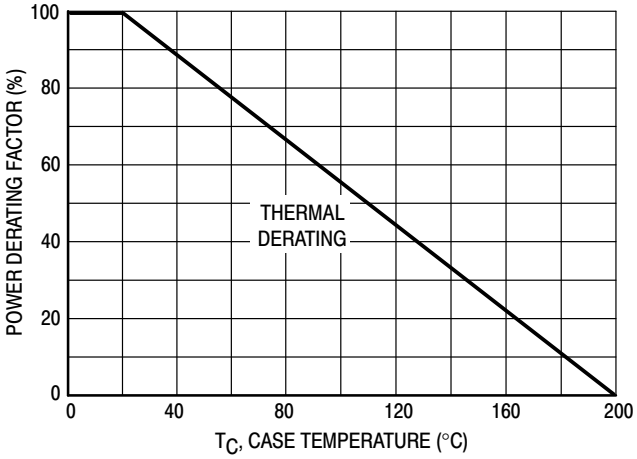


Figure 17. Power Derating

2N4918 - 2N4920* Series

Preferred Device

Medium-Power Plastic PNP Silicon Transistors

These medium−power, high−performance plastic devices are designed for driver circuits, switching, and amplifier applications.

Features

- Pb−Free Package is Available**
- Low Saturation Voltage − $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 A
- Excellent Power Dissipation Due to Thermopad Construction, P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 A
- Complement to NPN 2N4921, 2N4922, 2N4923

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage 2N4918 2N4919 2N4920	V_{CEO}	 40 60 80	Vdc
Collector − Base Voltage 2N4918 2N4919 2N4920	V_{CBO}	 40 60 80	Vdc
Emitter − Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous (Note 5)	I_C (Note 6)	1.0 3.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	30 0.24	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

5. The 1.0 A max I_C value is based upon JEDEC current gain requirements. The 3.0 A max value is based upon actual current−handling capability of the device (See Figure 5).
6. Indicates JEDEC Registered Data for 2N4918 Series.

THERMAL CHARACTERISTICS (Note 7)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θJC	4.16	°C/W

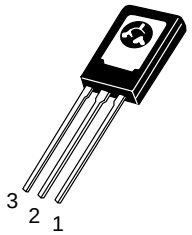
7. Recommend use of thermal compound for lowest thermal resistance.

**For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

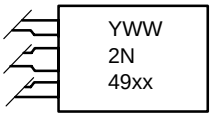
http://onsemi.com

3.0 A, 40−80 V, 30 W
GENERAL PURPOSE
POWER TRANSISTORS



TO−225
CASE 077
STYLE 1

MARKING DIAGRAM



xx = 18, 19, 20
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 50 of this data sheet.

***Preferred** devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 8) (I_C = 0.1 Adc, I_B = 0)	2N4918 2N4919 2N4920	$V_{CEO(sus)}$	 40 60 80	 − − −	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N4918 2N4919 2N4920	I_{CEO}	 − − −	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C		I_{CEX}	 − −	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	−	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 8) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30 10	 − 150 −	−
Collector−Emitter Saturation Voltage (Note 8) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	−	0.6	Vdc
Base−Emitter Saturation Voltage (Note 8) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	−	1.3	Vdc
Base−Emitter On Voltage (Note 8) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	−	1.3	Vdc
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	−	100	pF
Small−Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	−	−

8. Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

ORDERING INFORMATION

Device	Package	Shipping†
2N4918	TO−225	500 Unit / Bulk
2N4919	TO−225	500 Unit / Bulk
2N4920	TO−225	500 Unit / Bulk
2N4920G	TO−225 (Pb−Free)	500 Unit / Bulk

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

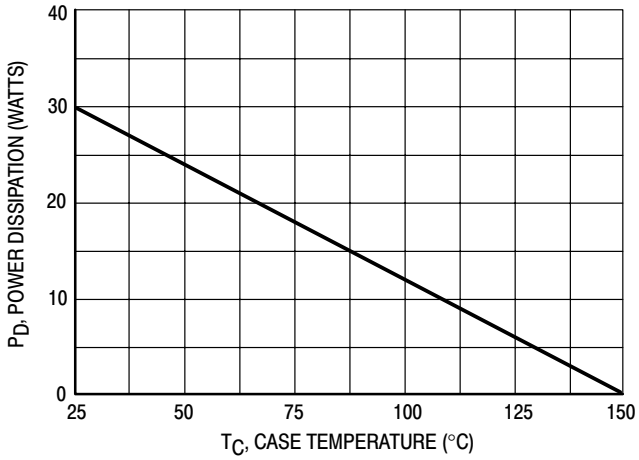


Figure 1. Power Derating

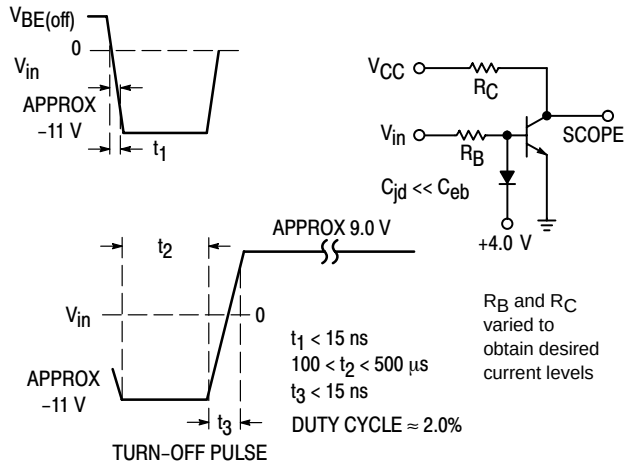


Figure 2. Switching Time Equivalent Test Circuit

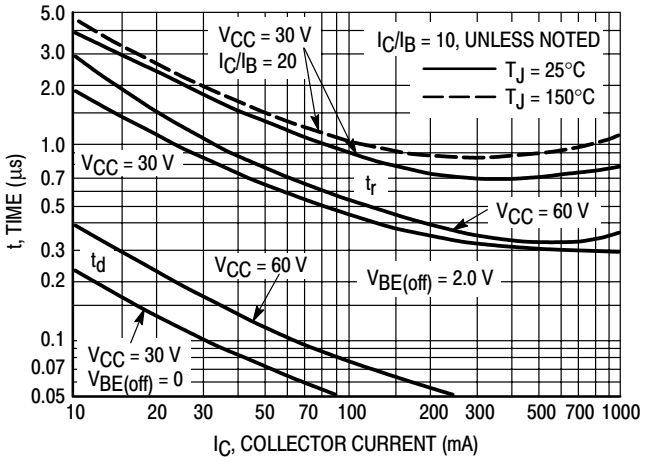


Figure 3. Turn−On Time

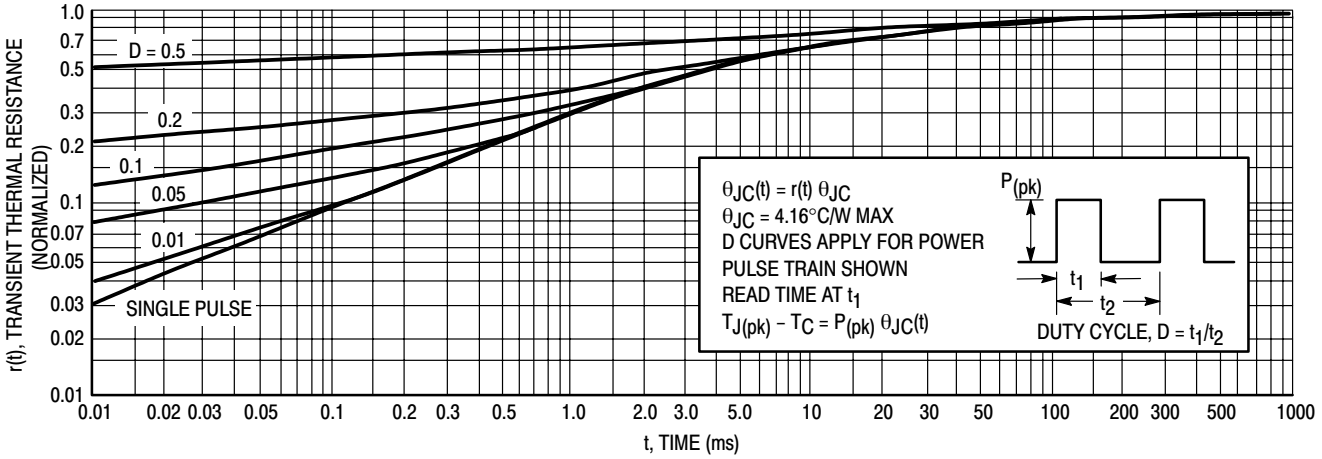


Figure 4. Thermal Response

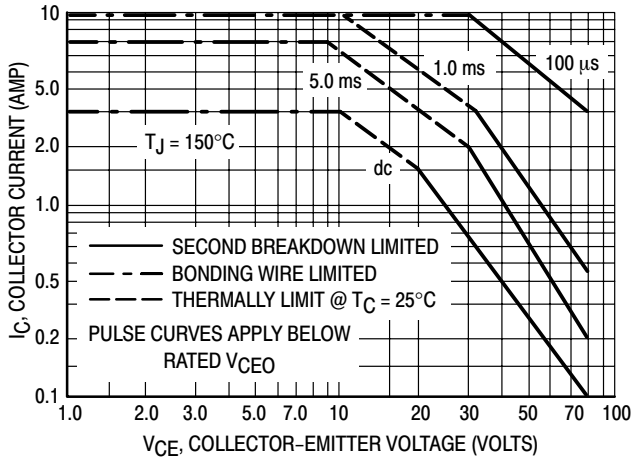


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

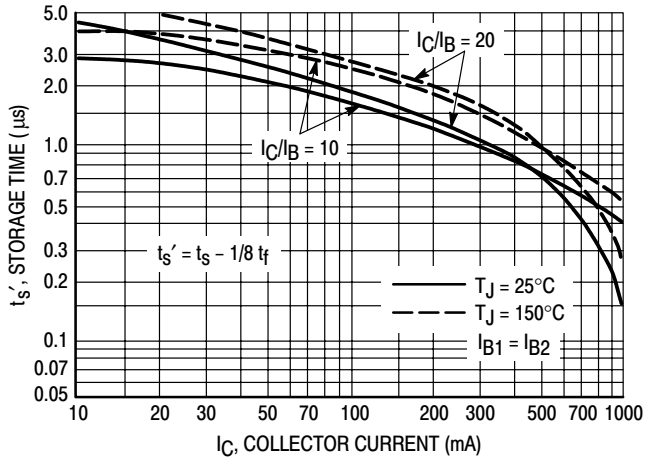


Figure 6. Storage Time

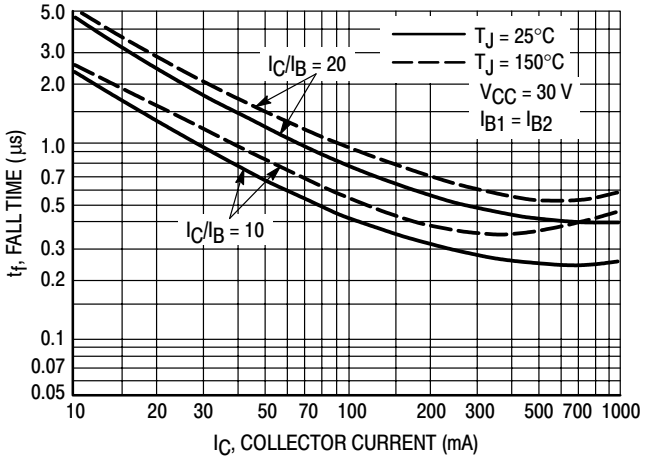


Figure 7. Fall Time

TYPICAL DC CHARACTERISTICS

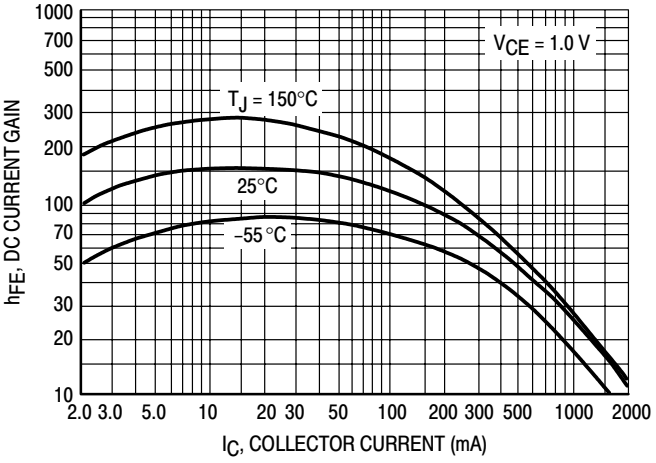


Figure 8. Current Gain

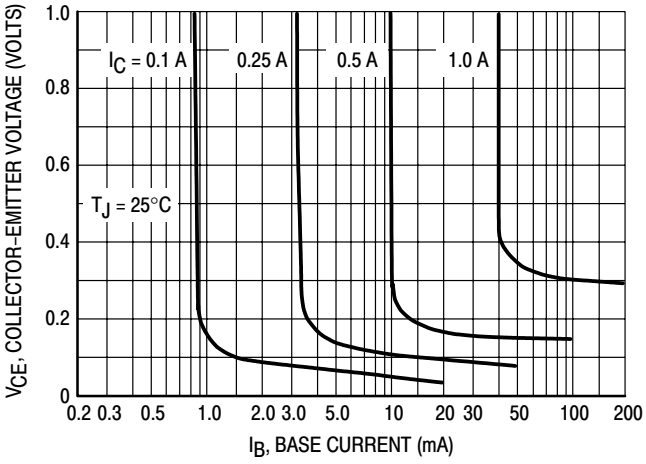


Figure 9. Collector Saturation Region

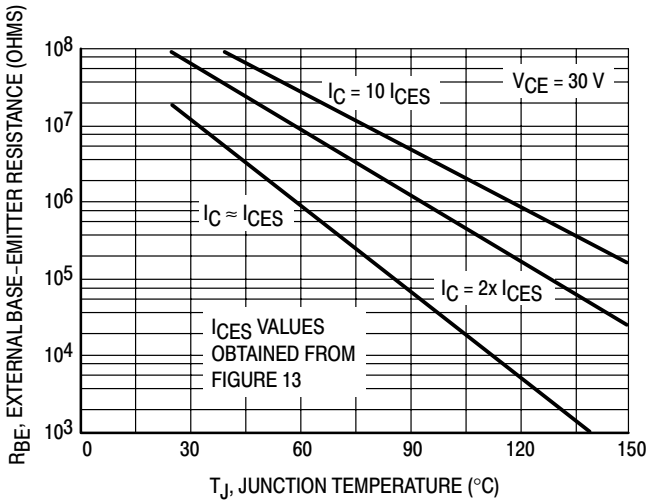


Figure 10. Effects of Base−Emitter Resistance

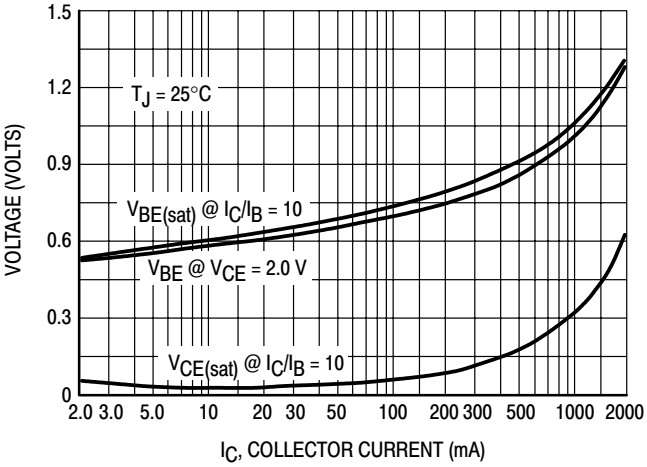


Figure 11. "On" Voltage

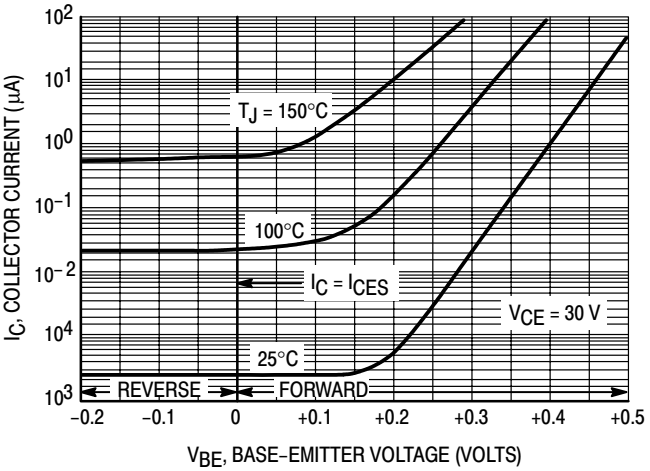


Figure 12. Collector Cut−Off Region

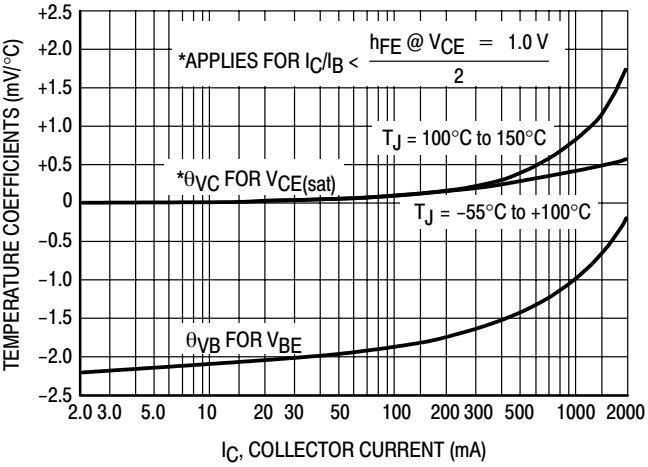


Figure 13. Temperature Coefficients

Medium-Power Plastic NPN Silicon Transistors

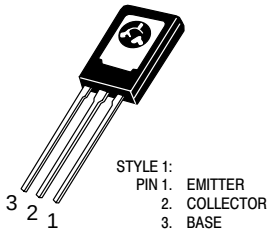
2N4921 thru 2N4923 *

*ON Semiconductor Preferred Device

. . . designed for driver circuits, switching, and amplifier applications. These high−performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920

1 AMPERE GENERAL−PURPOSE POWER TRANSISTORS 40−80 VOLTS 30 WATTS



CASE 77−09 TO−225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector−Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector−Base Voltage	V_{CB}	40	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous (1)	I_C	1.0 3.0			Adc
Base Current — Continuous	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current handling capability of the device (see Figures 5 and 6).

(2) Recommend use of thermal compound for lowest thermal resistance.

*Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 10
Publication Order Number:
2N4921/D

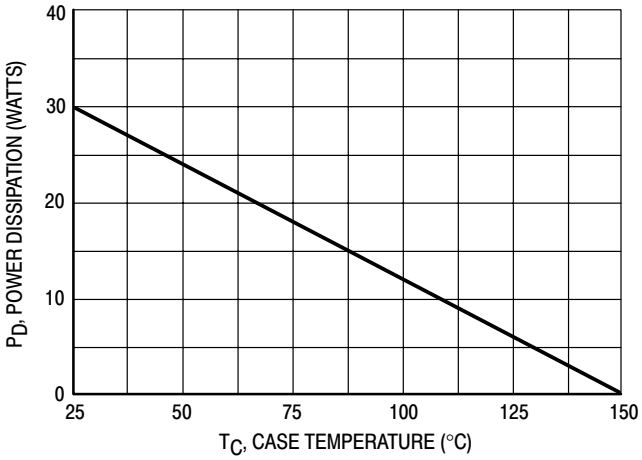


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (3) (I_C = 0.1 Adc, I_B = 0)	2N4921 2N4922 2N4923	$V_{CEO(sus)}$	 40 60 80	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N4921 2N4922 2N4923	I_{CEO}	 — — —	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C		I_{CEX}	 — —	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (3) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30 10	 — 150 —	—
Collector−Emitter Saturation Voltage (3) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.6	Vdc
Base−Emitter Saturation Voltage (3) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	—	1.3	Vdc
Base−Emitter On Voltage (3) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	100	pF
Small−Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(3) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.
*Indicates JEDEC Registered Data.

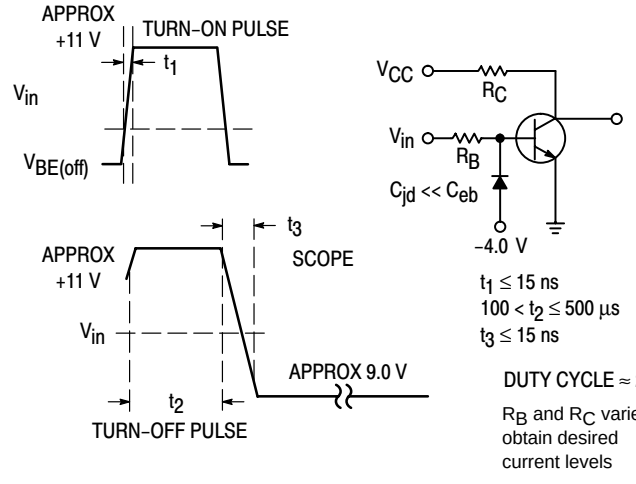


Figure 2. Switching Time Equivalent Circuit

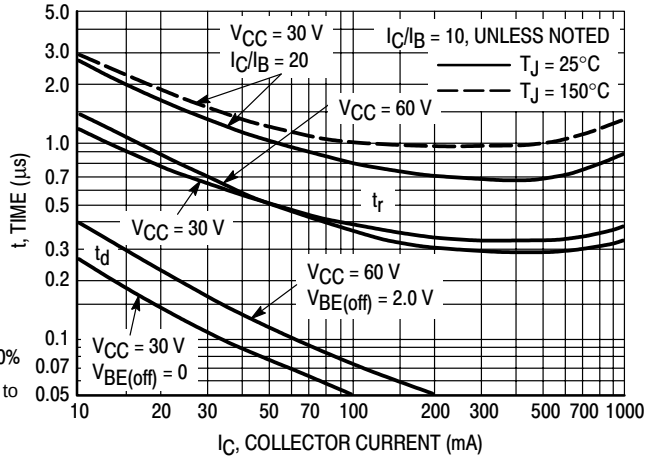


Figure 3. Turn−On Time

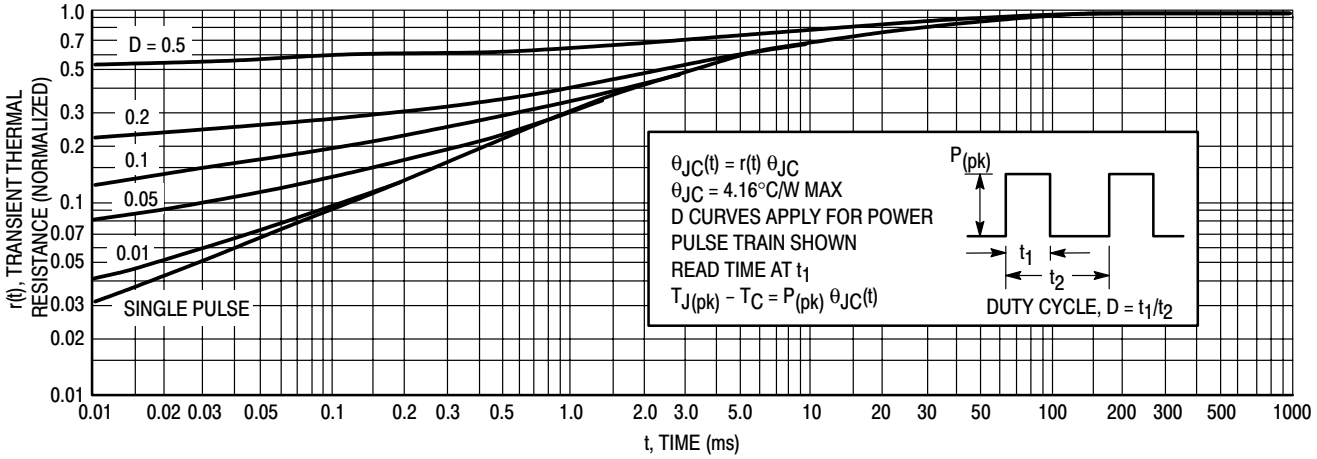


Figure 4. Thermal Response

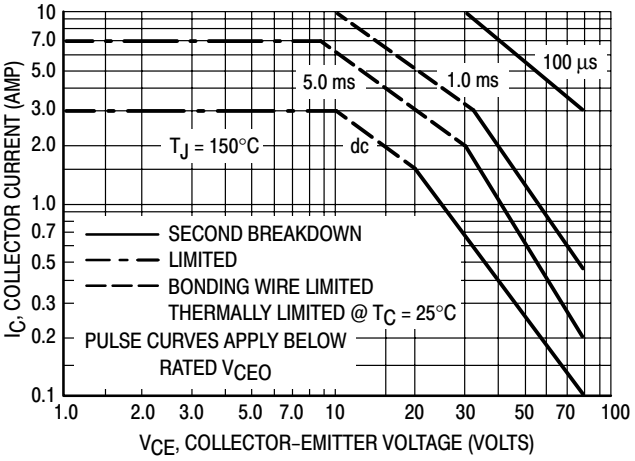


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

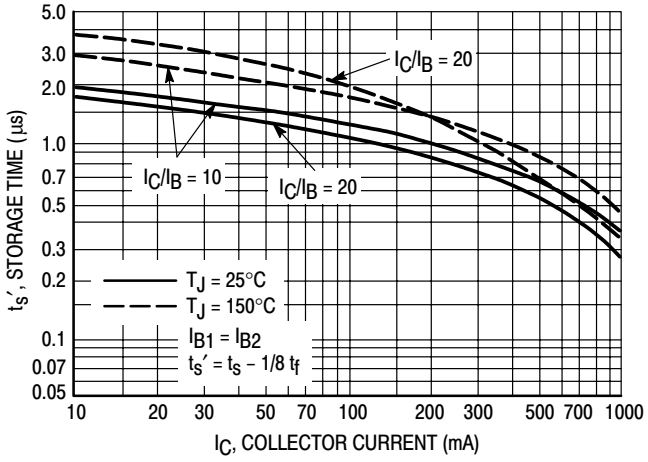


Figure 6. Storage Time

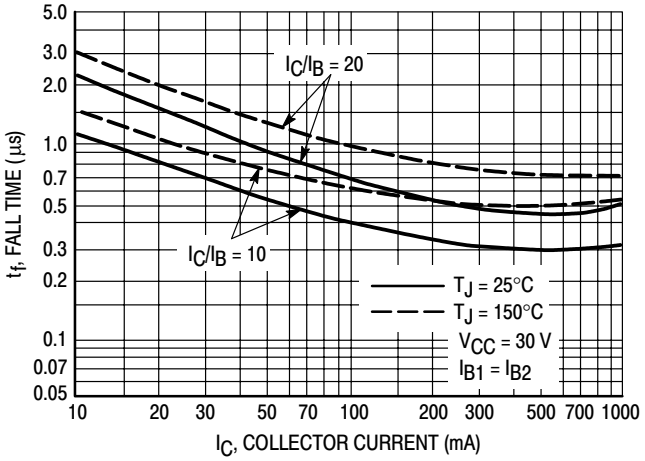


Figure 7. Fall Time

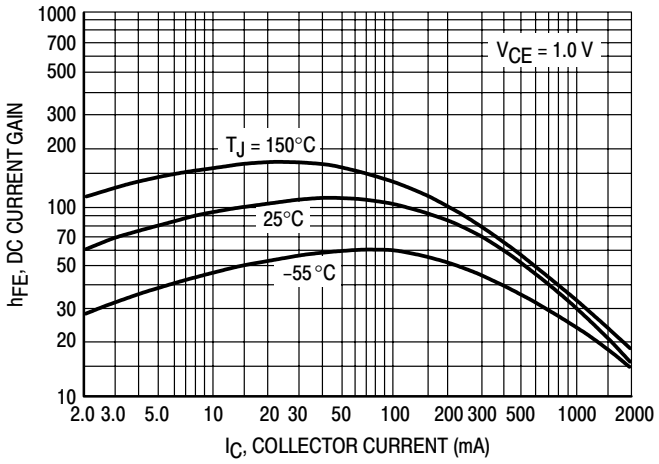


Figure 8. Current Gain

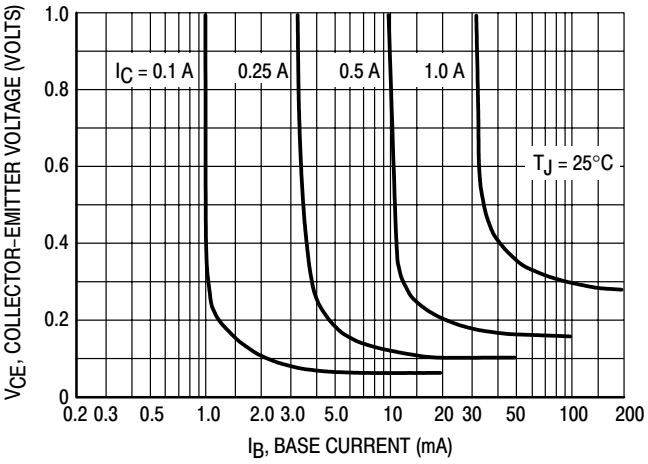


Figure 9. Collector Saturation Region

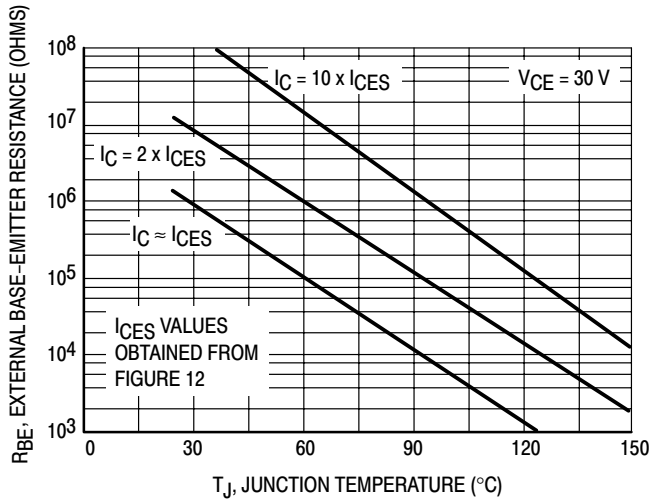


Figure 10. Effects of Base−Emitter Resistance

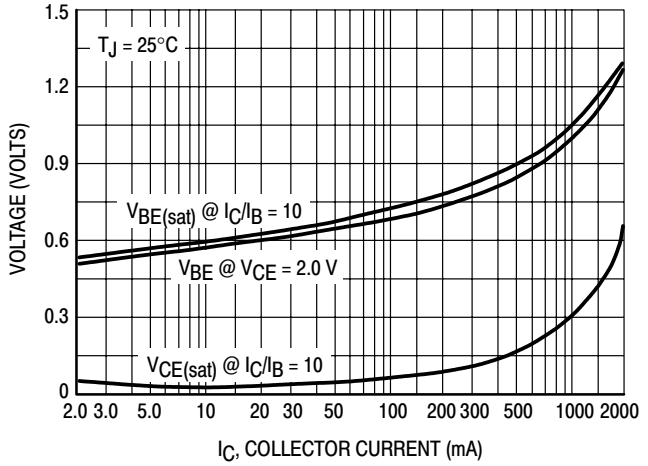


Figure 11. “On” Voltage

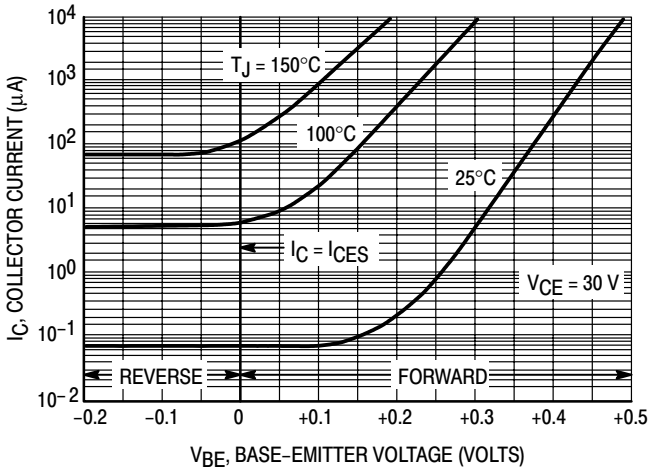


Figure 12. Collector Cut−Off Region

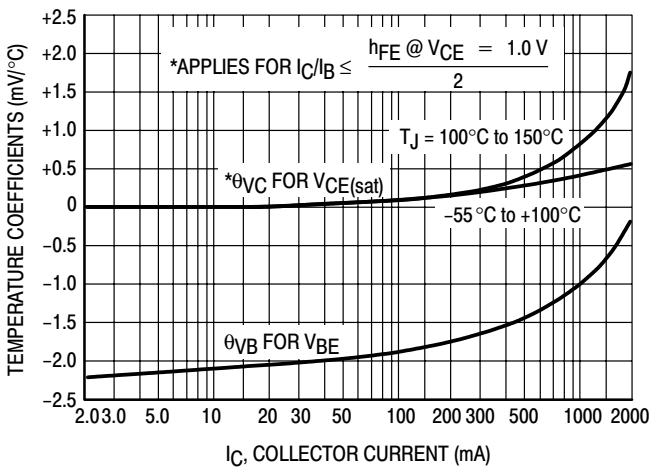


Figure 13. Temperature Coefficients

2N5190, 2N5191, 2N5192

Silicon NPN Power Transistors

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5194, 2N5195.

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V−0 @ 1/8”
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	2N5190 2N5191 2N5192	V_{CEO}	40 60 80	Vdc
Collector−Base Voltage	2N5190 2N5191 2N5192	V_{CBO}	40 60 80	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

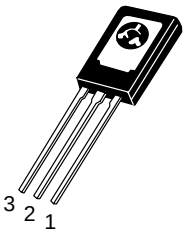
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.12	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

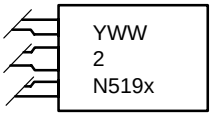
http://onsemi.com

4.0 A
NPN SILICON
POWER TRANSISTORS
40, 60, 80 V, 40 W



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



x = 0, 1, 2
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
2N5190	TO−225AA	500 Units/Box
2N5191	TO−225AA	500 Units/Box
2N5191G	TO−225AA (Pb−Free)	500 Units/Box
2N5192	TO−225AA	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N5190		40	−	
	2N5191		60	−	
	2N5192		80	−	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5190		−	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5191		−	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5192		−	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5190		−	0.1	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5191		−	0.1	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5192		−	0.1	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5190		−	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5191		−	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5192		−	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5190		−	0.1	
(V_{CB} = 60 Vdc, I_E = 0)	2N5191		−	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N5192		−	0.1	
Emitter Cutoff Current		I_{EBO}	−	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (Note 1)					
DC Current Gain		h_{FE}			−
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5190/2N5191		25	100	
	2N5192		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5190/2N5191		10	−	
	2N5192		7.0	−	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			−	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			−	1.4	
Base−Emitter On Voltage		$V_{BE(on)}$	−	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product		f_T	2.0	−	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					

*Indicates JEDEC Registered Data.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

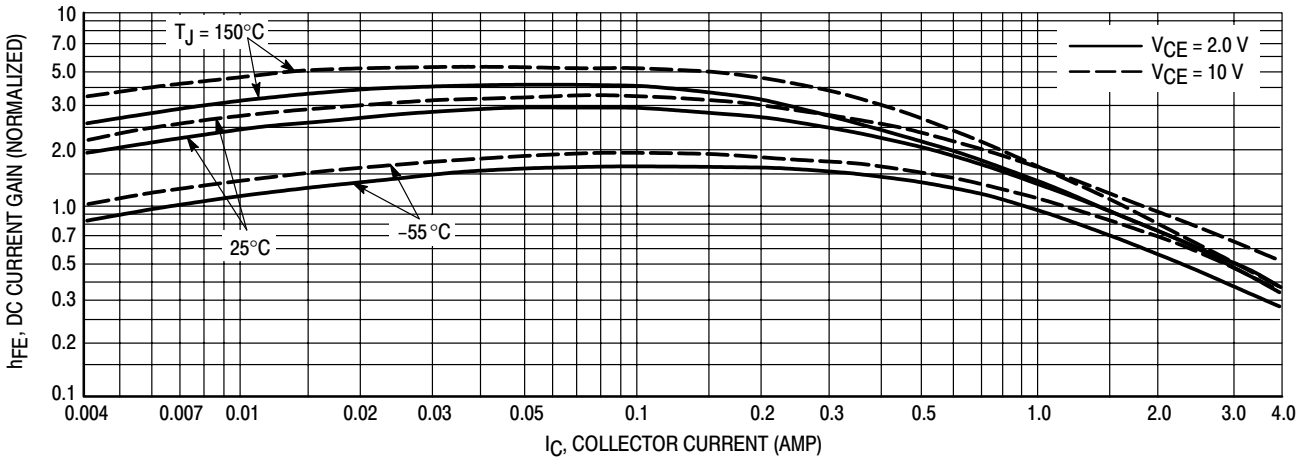


Figure 1. DC Current Gain

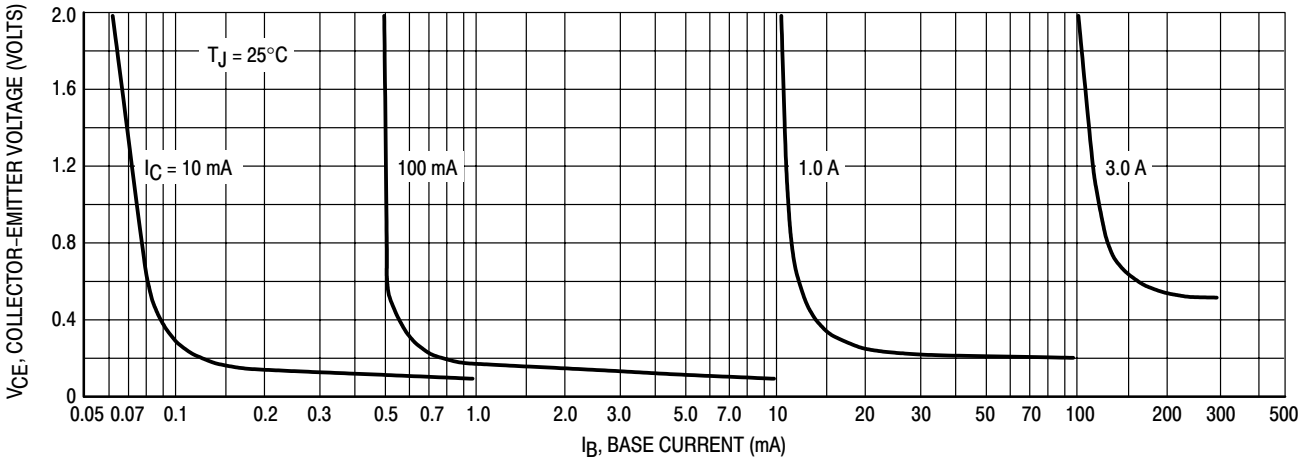


Figure 2. Collector Saturation Region

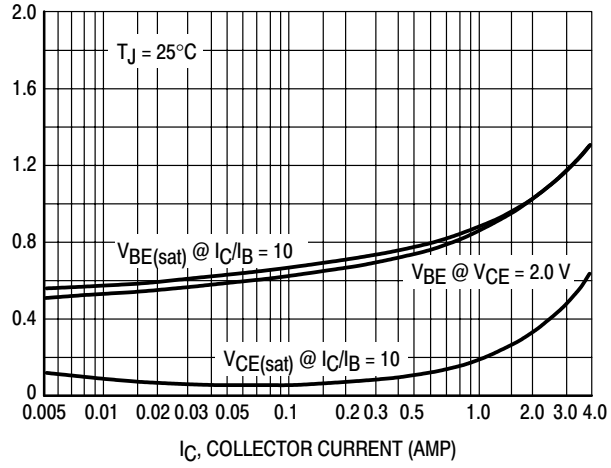


Figure 3. “On” Voltages

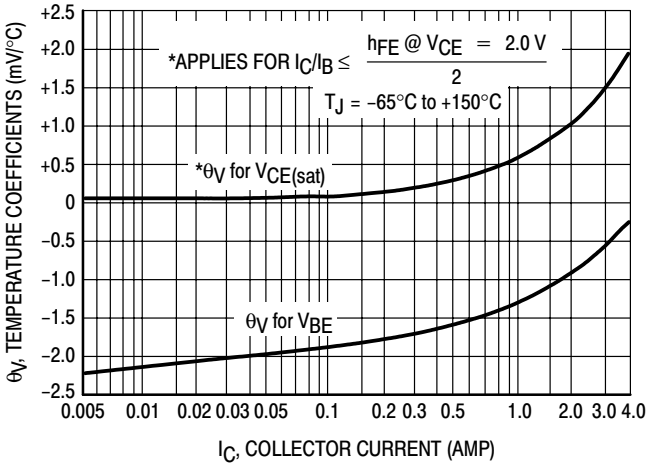


Figure 4. Temperature Coefficients

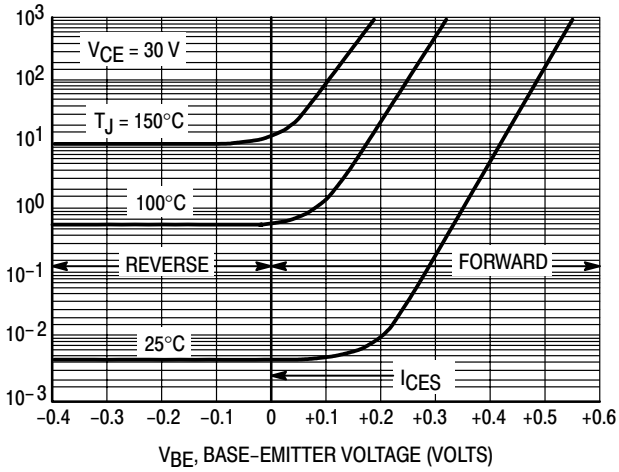


Figure 5. Collector Cut−Off Region

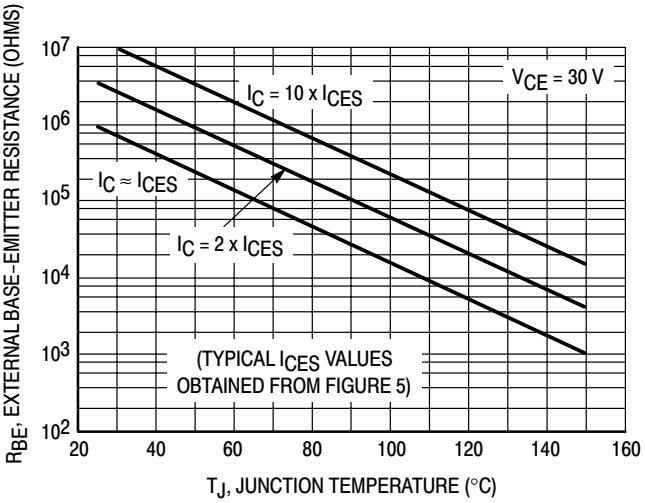


Figure 6. Effects of Base−Emitter Resistance

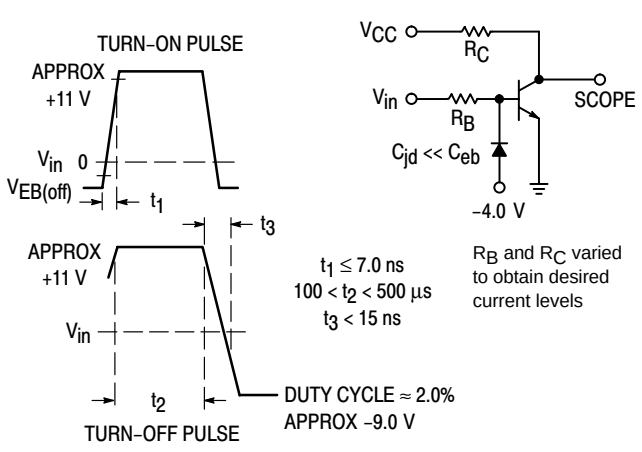


Figure 7. Switching Time Equivalent Test Circuit

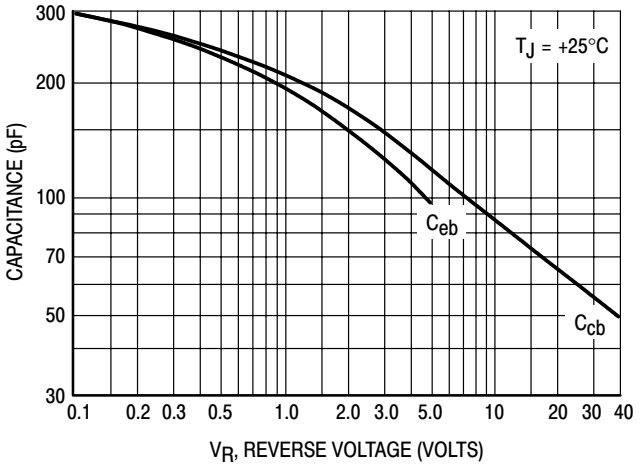


Figure 8. Capacitance

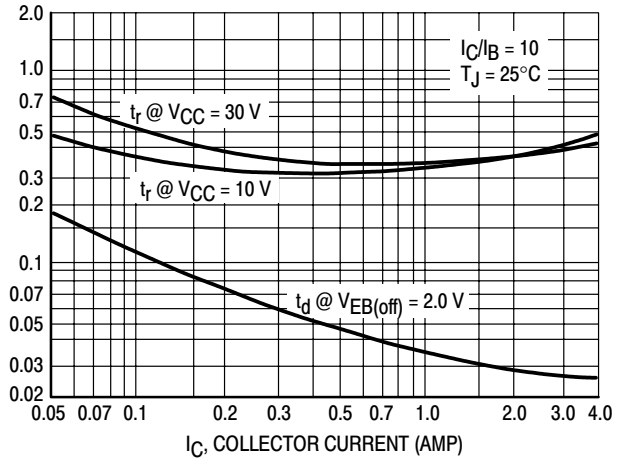


Figure 9. Turn−On Time

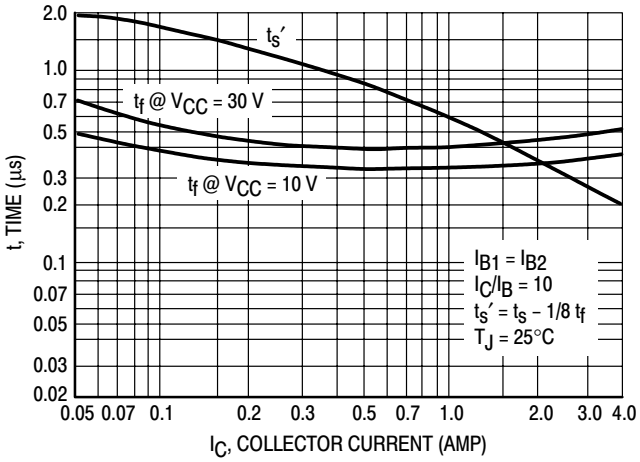


Figure 10. Turn−Off Time

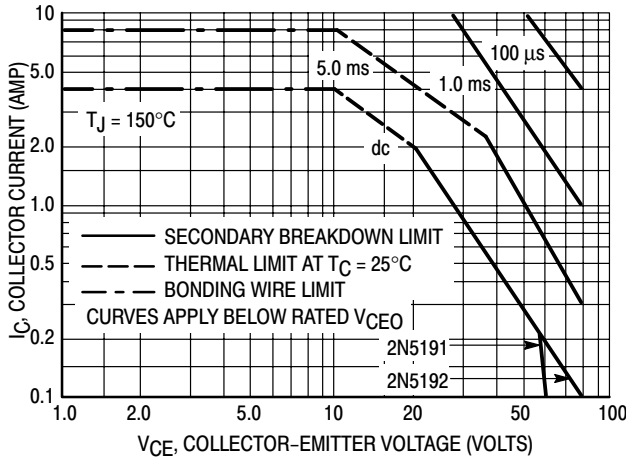


Figure 11. Rating and Thermal Data
Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

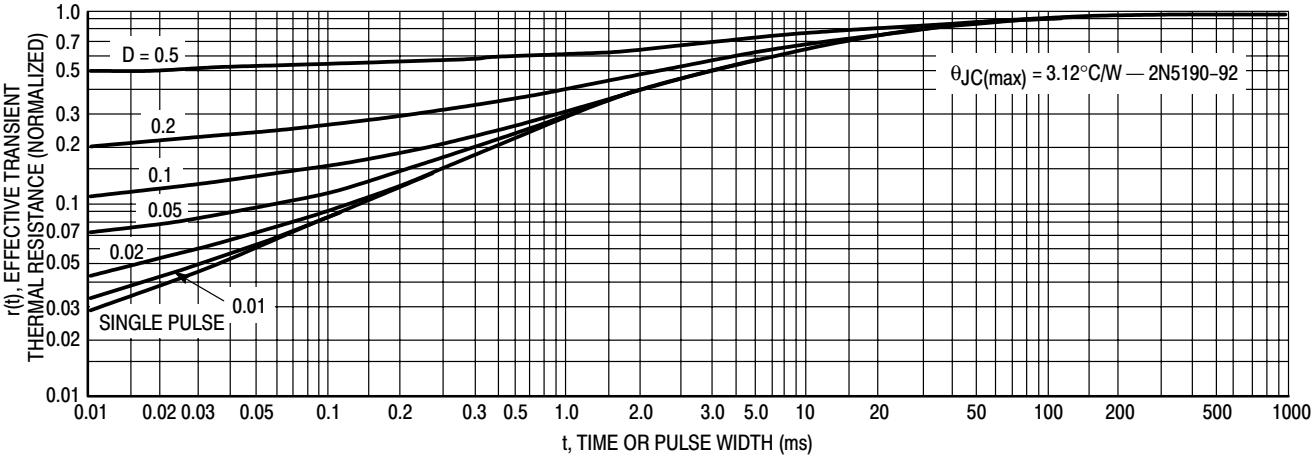
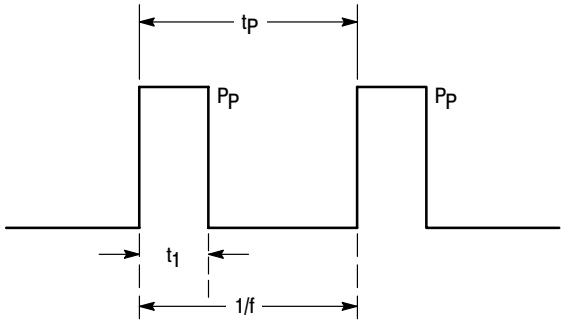


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE, $D = t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

Figure A

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in function temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^{\circ}C$$

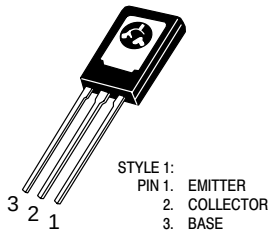
Silicon PNP Power Transistors

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5191, 2N5192

2N5194
2N5195*

*ON Semiconductor Preferred Device

4 AMPERE
POWER TRANSISTORS
SILICON PNP
60−80 VOLTS



CASE 77−09
TO−225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N5194	2N5195	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N5194 2N5195	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N5194 2N5195	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N5194 2N5195 2N5194 2N5195	I_{CEX}	 — — — —	 0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5194 2N5195	I_{CBO}	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 10
Publication Order Number:
2N5194/D

***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (2)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5194		25	100	
	2N5195		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5194		10	—	
	2N5195		7.0	—	
Collector−Emitter Saturation Voltage (2)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			—	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			—	1.4	
Base−Emitter On Voltage (2)		$V_{BE(on)}$	—	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product		f_T	2.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					

*Indicates JEDEC Registered Data.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

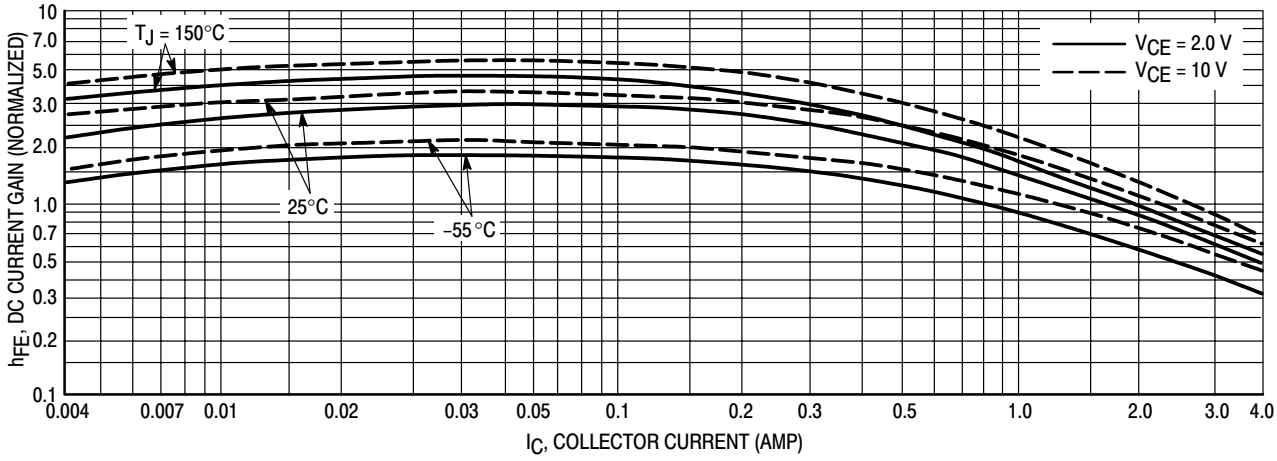


Figure 1. DC Current Gain

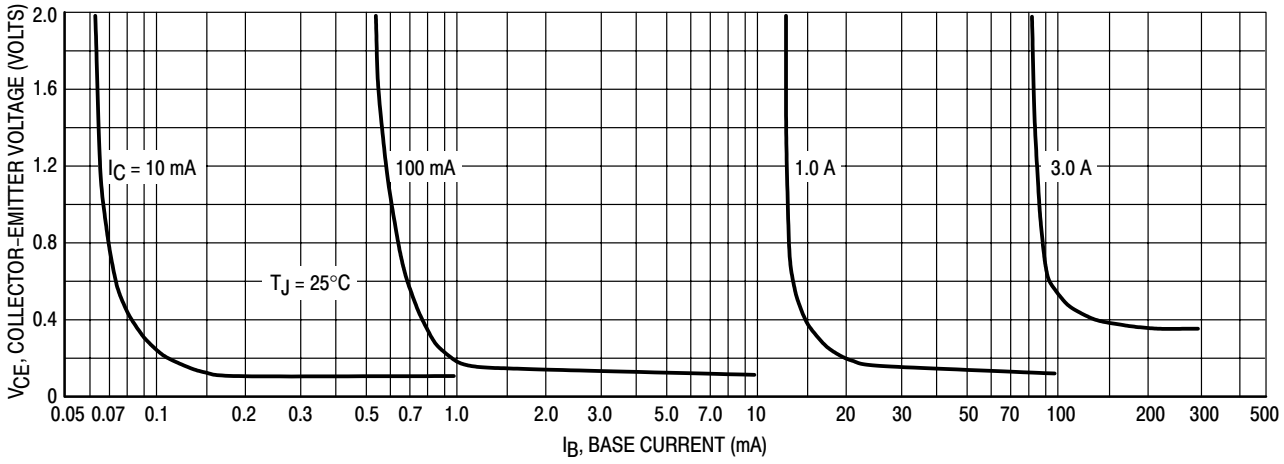


Figure 2. Collector Saturation Region

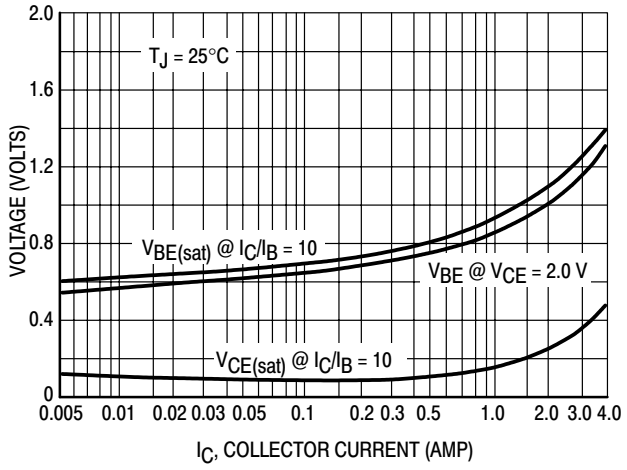


Figure 3. "On" Voltage

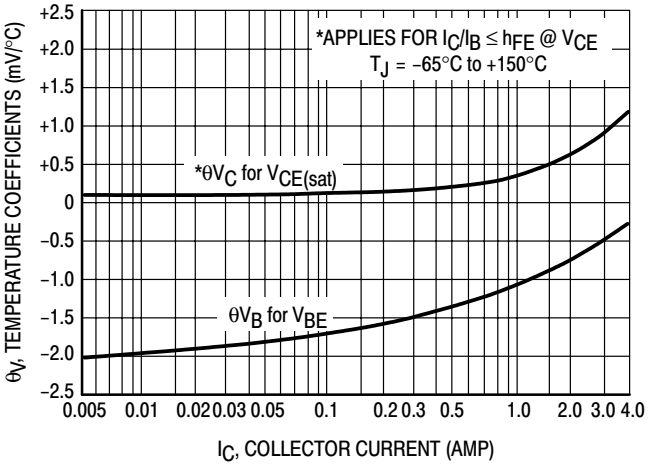


Figure 4. Temperature Coefficients

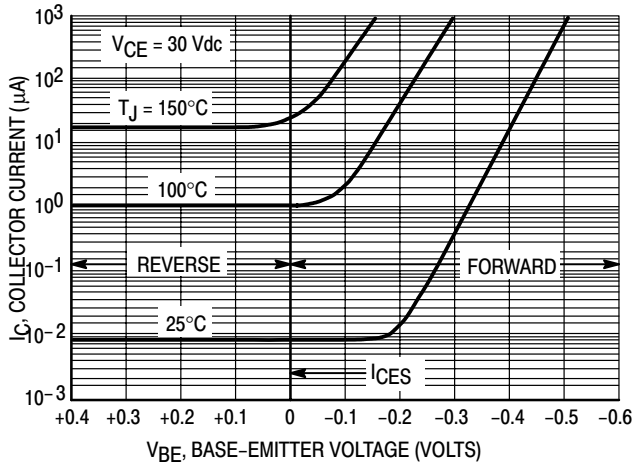


Figure 5. Collector Cut−Off Region

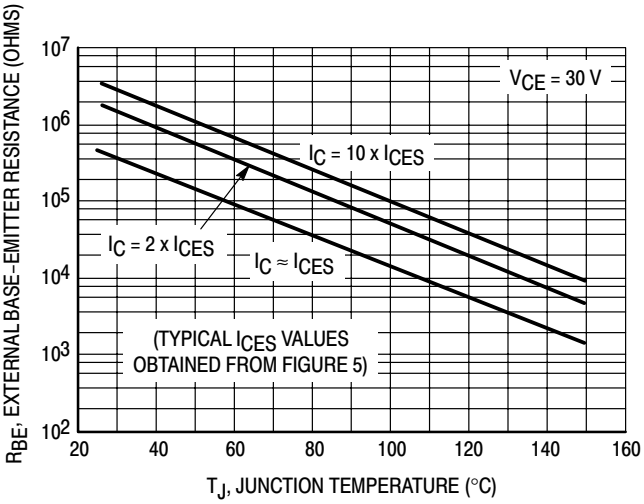


Figure 6. Effects of Base−Emitter Resistance

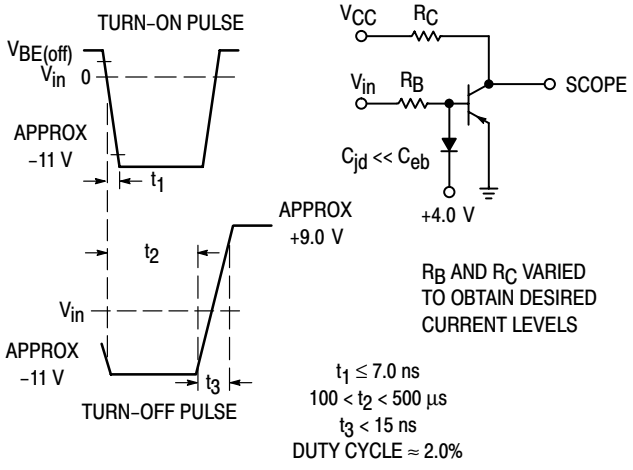


Figure 7. Switching Time Equivalent Test Circuit

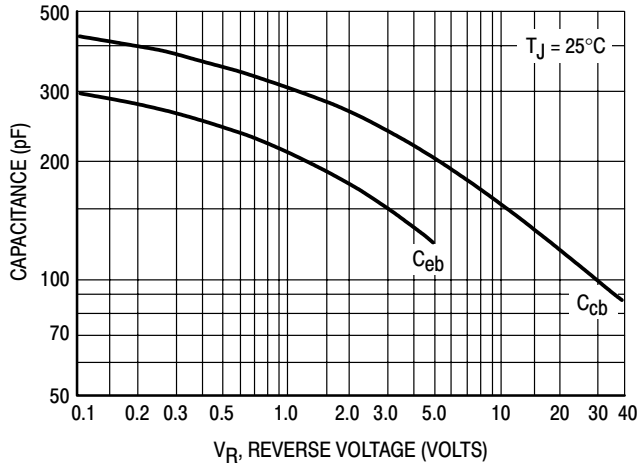


Figure 8. Capacitance

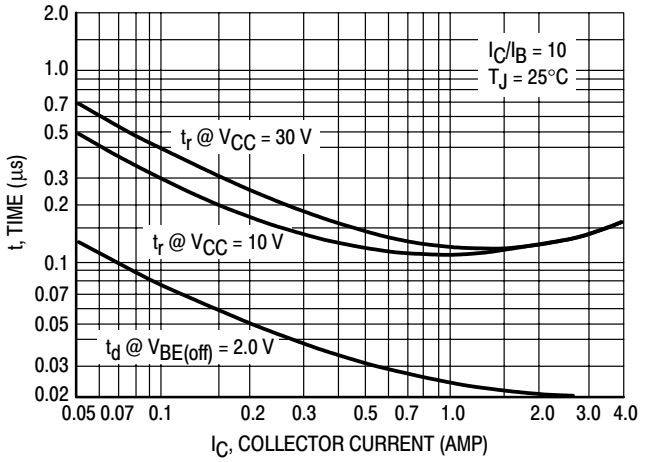


Figure 9. Turn−On Time

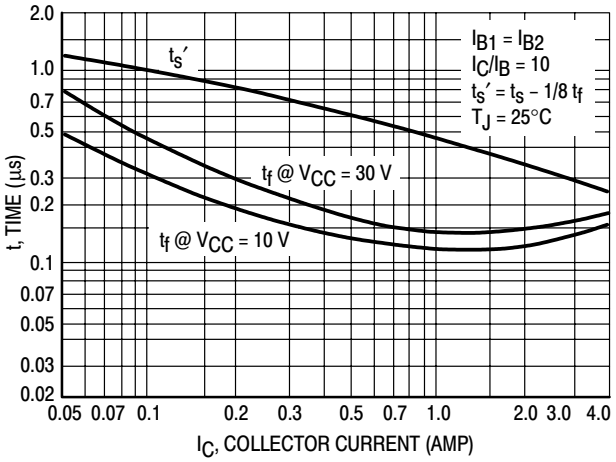


Figure 10. Turn−Off Time

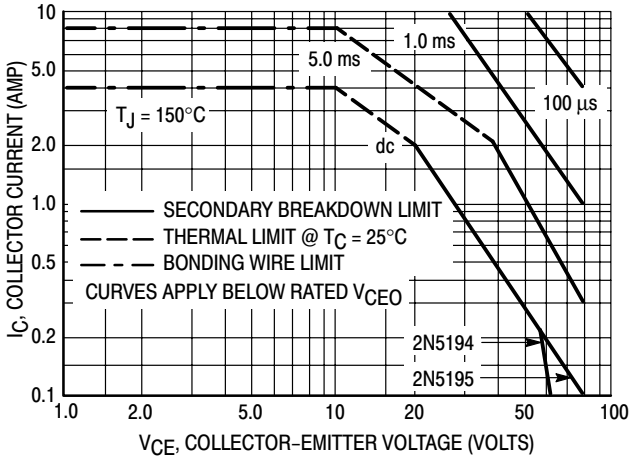


Figure 11. Rating and Thermal Data
Active−Region Safe Operating Area

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high−case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

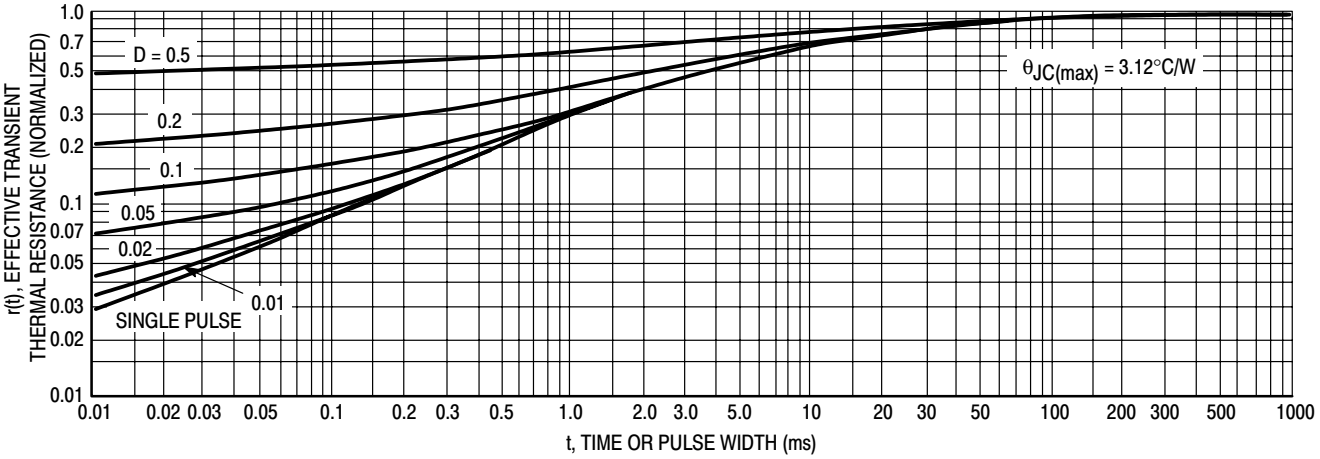


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

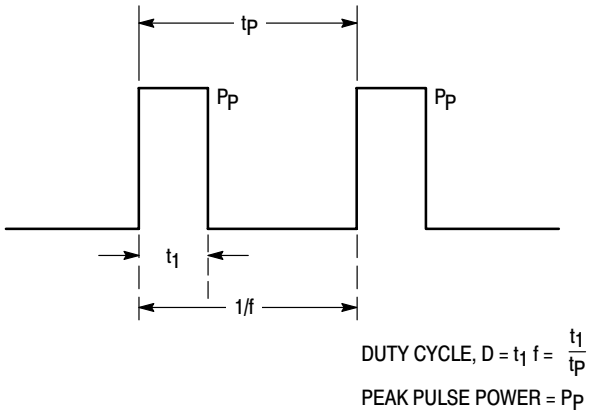


Figure 13.

A train of periodical power pulses can be represented by the model shown in Figure 13. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r(t_1, D) is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

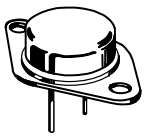
High-Power NPN Silicon Transistor

2N5302

. . . for use in power amplifier and switching circuits applications.

- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc

30 AMPERE
POWER TRANSISTOR
NPN SILICON
60 VOLTS
200 WATTS



CASE 1−07
TO−204AA
(TO−3)

***MAXIMUM RATINGS**

Rating	Symbol	2N5302	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CB}	60	Vdc
Collector Current − Continuous	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

*Indicates JEDEC Registered Data.

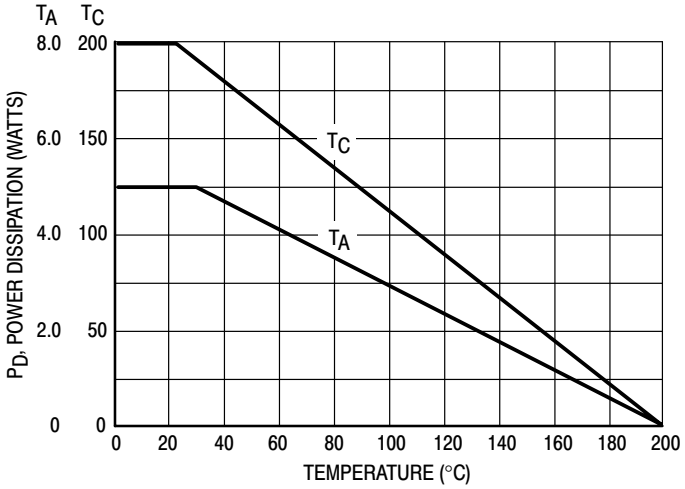


Figure 1. Power Temperature Derating Curve

Publication Order Number:
2N5302/D
May, 2001 − Rev. 0

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	−	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	−	5.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	−	1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	−	10	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	−	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 1) *(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc) *(I_C = 15 Adc, V_{CE} = 2.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 40 15 5.0	 − 60 −	−
*Collector−Emitter Saturation Voltage (Note 1) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 20 Adc, I_B = 2.0 Adc)2 (I_C = 30 Adc, I_B = 6.0 Adc)	$V_{CE(sat)}$	 − − −	 0.75 2.0 3.0	Vdc
*Base Emitter Saturation Voltage (Note 1) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 20 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 − − −	 1.7 1.8 2.5	Vdc
*Base−Emitter On Voltage (Note 1) (I_C = 15 Adc, V_{CE} = 2.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	 − −	 1.7 3.0	Vdc
***DYNAMIC CHARACTERISTICS**				
Current−Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	−	MHz
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	40	−	−
***SWITCHING CHARACTERISTICS**				
Rise Time	t_r	−	1.0	μs
Storage Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_s	−	2.0	μs
Fall Time	t_f	−	1.0	μs

*Indicates JEDEC Registered Data.

Note 1: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

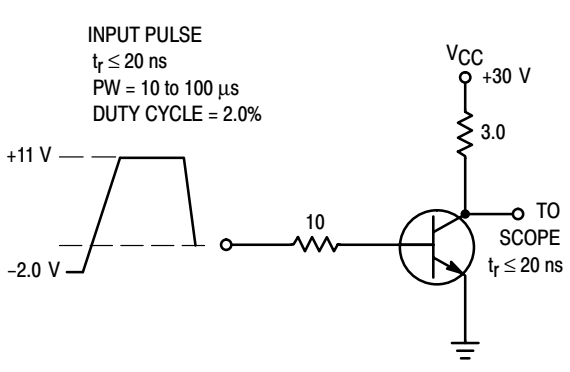


Figure 2. Turn−On time

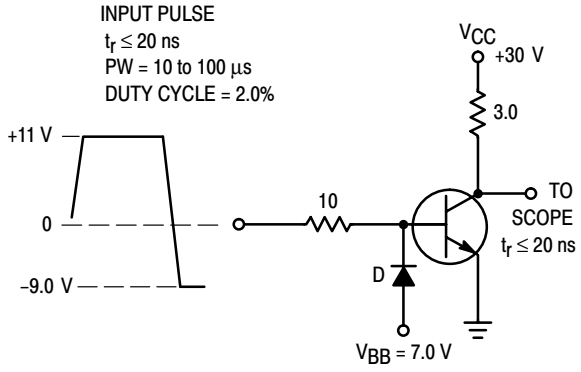


Figure 3. Turn−Off time

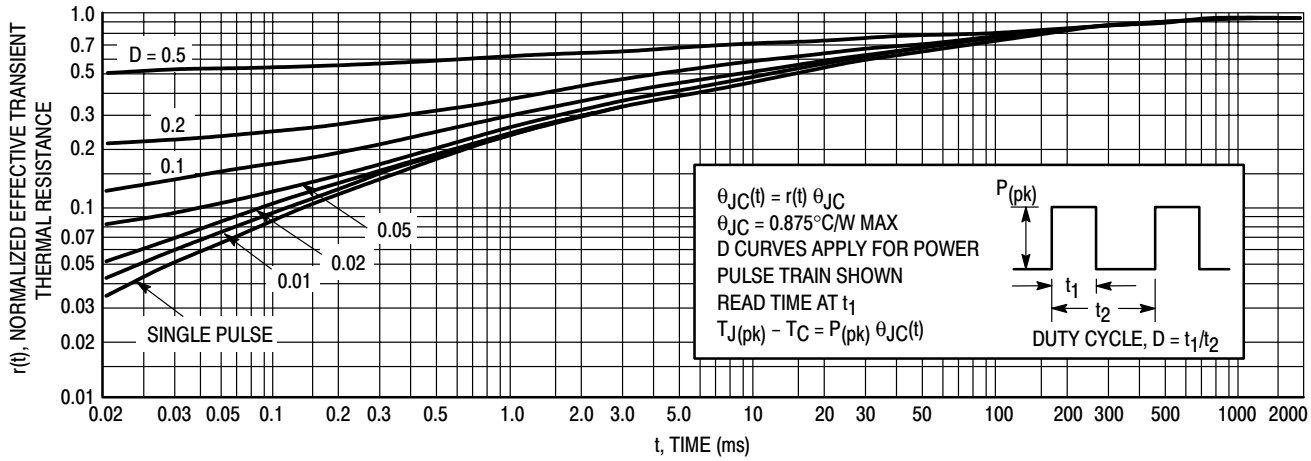


Figure 4. Thermal Response

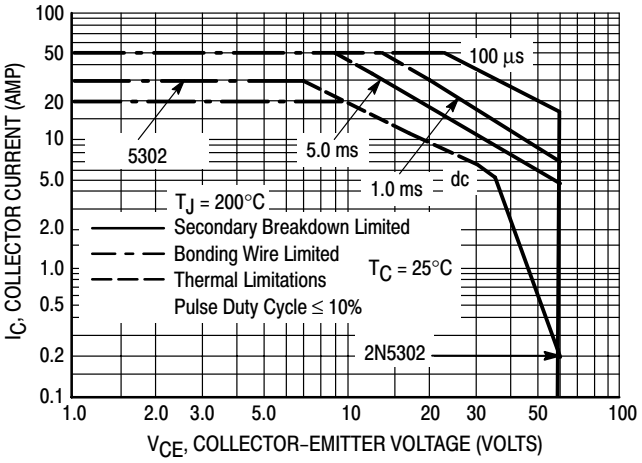


Figure 5. Active−Region Safe Operating Area

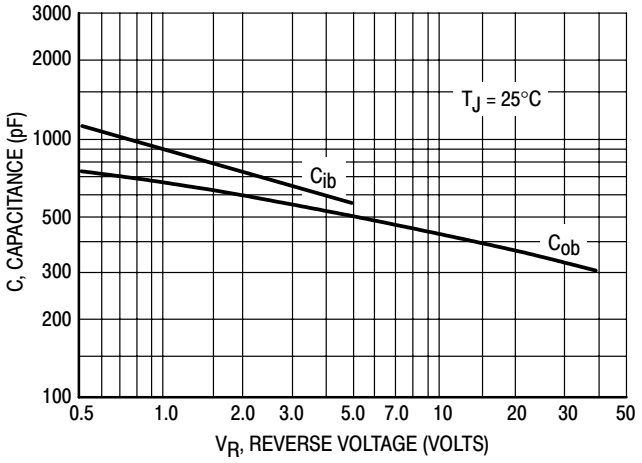


Figure 6. Capacitance versus Voltage

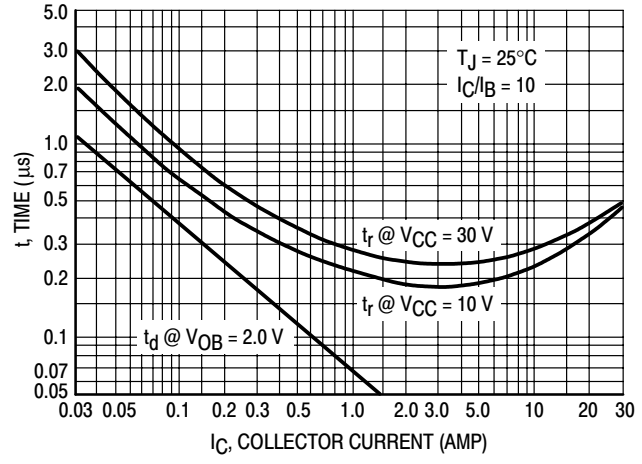


Figure 7. Turn−On Time

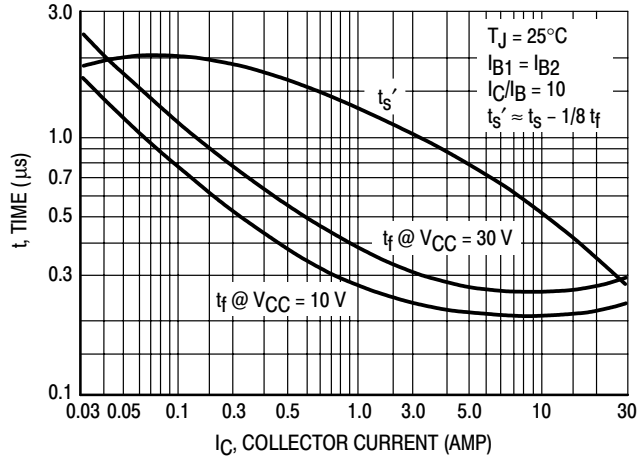


Figure 8. Turn−Off Time

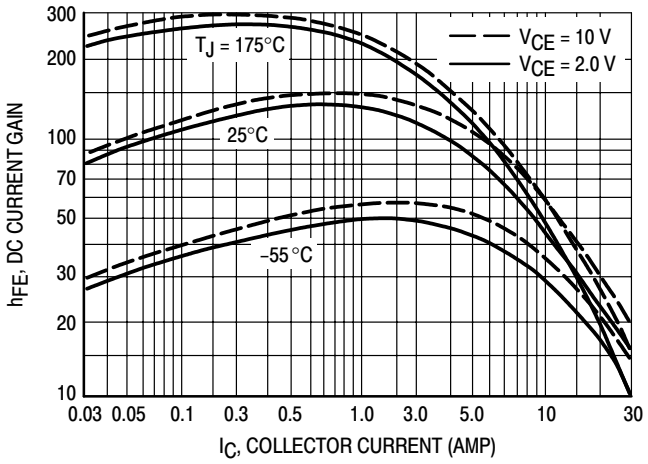


Figure 9. DC Current Gain

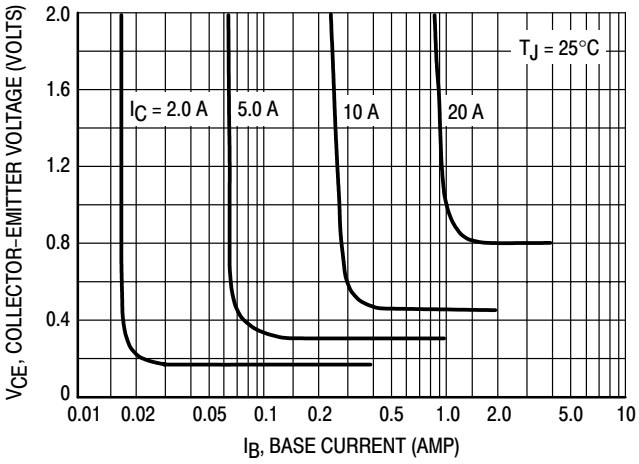


Figure 10. Collector Saturation Region

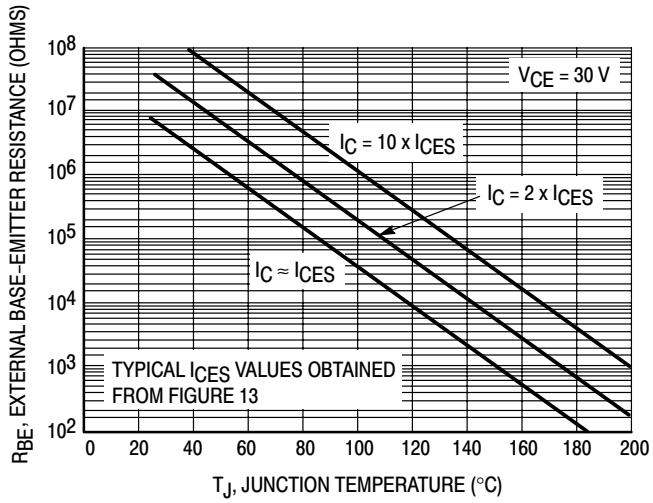


Figure 11. Effects of Base−Emitter Resistance

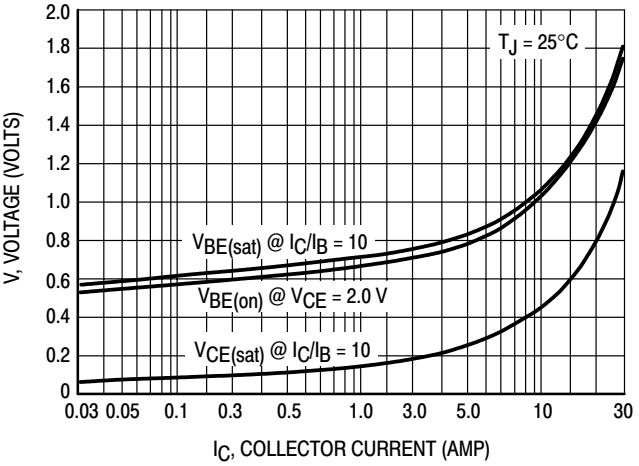


Figure 12. “On” Voltages

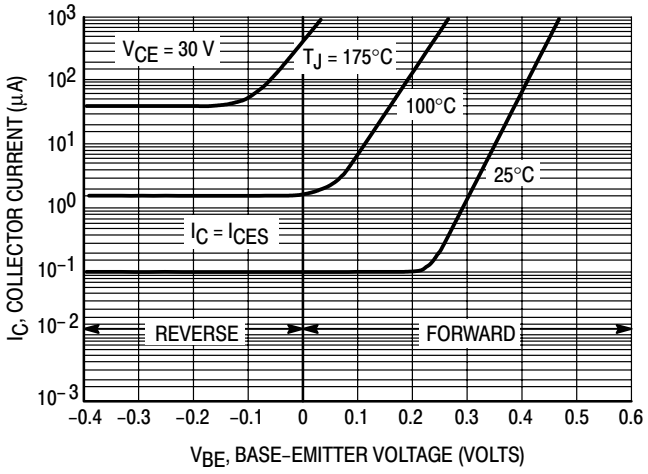


Figure 13. Collector Cut−Off Region

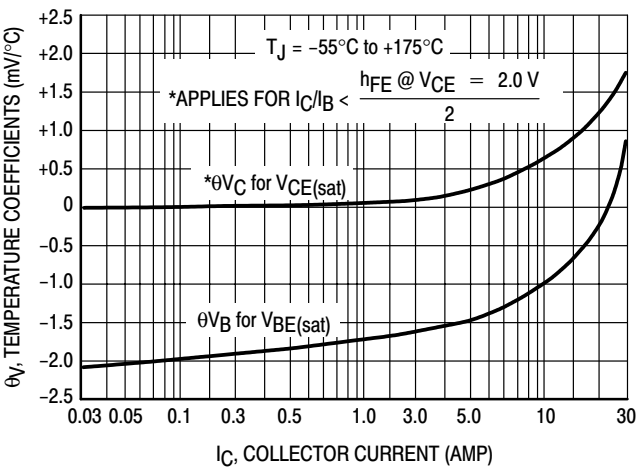


Figure 14. Temperature Coefficients

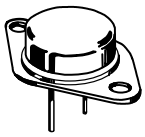
High-Voltage - High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 140 Vdc
- High DC Current Gain − @ I_C = 8.0 Adc
  h_{FE} = 15 (Min)
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc

NPN
2N5631
PNP
2N6031

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
200 WATTS



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CB}	140	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current − Continuous Peak	I_C	16 20	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

(1) Indicates JEDEC Registered Data.

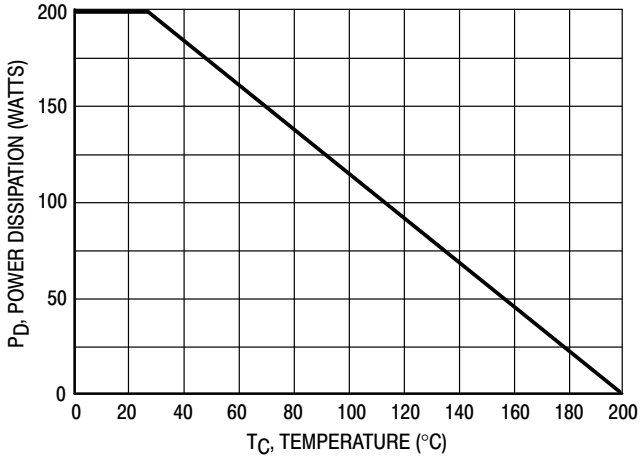


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

May, 2001 − Rev. 0
Publication Order Number:
2N5631/D

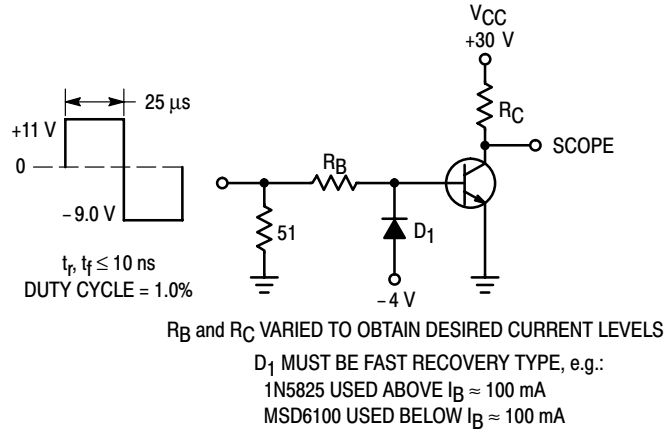
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)		$V_{CEO(sus)}$	140	–	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 70 Vdc, I_B = 0)		I_{CEO}	–	2.0	mAdc
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	2.0 7.0	mAdc
Collector−Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	2.0	mAdc
Emitter−Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 8 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	15 4.0	60 –	–
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 16 Adc, I_B = 4.0 Adc)		$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	1.8	Vdc
Base−Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (3) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5631 2N6031	C_{ob}	– –	500 1000	pF
Small−Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Times Test Circuit

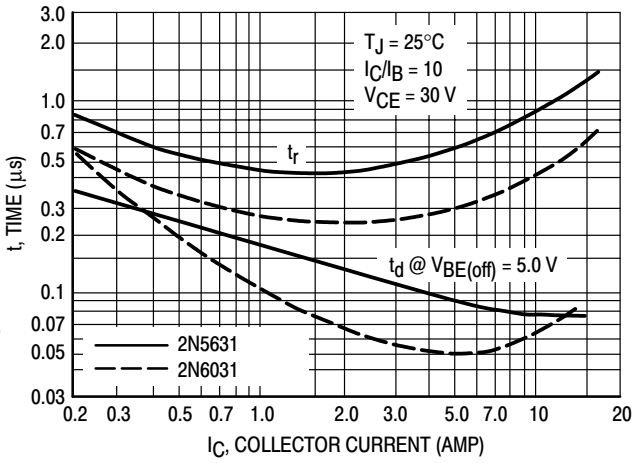


Figure 3. Turn−On Time

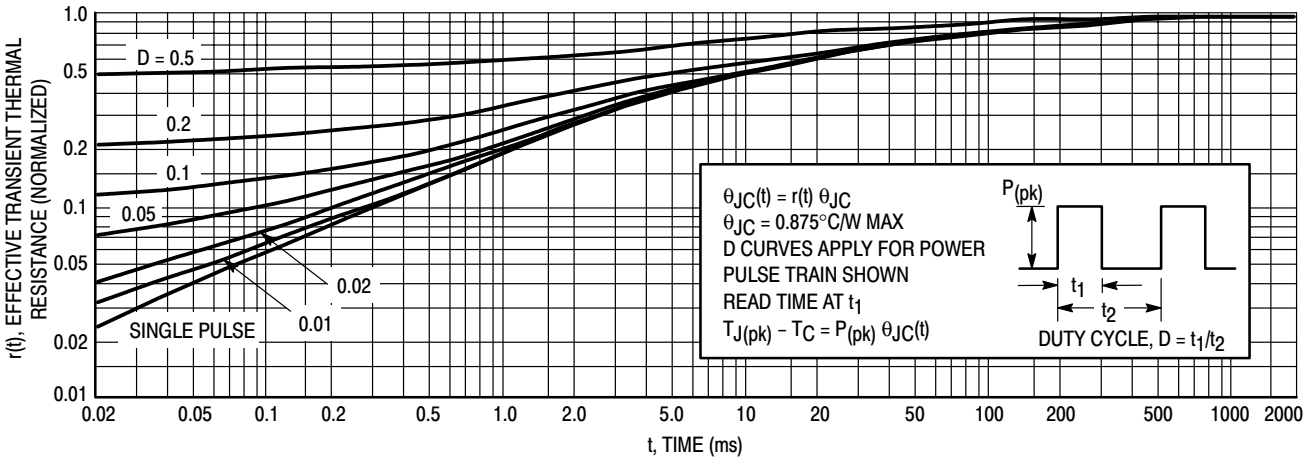


Figure 4. Thermal Response

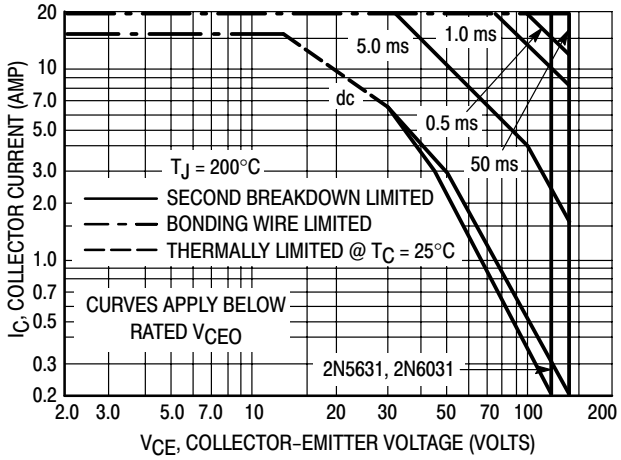
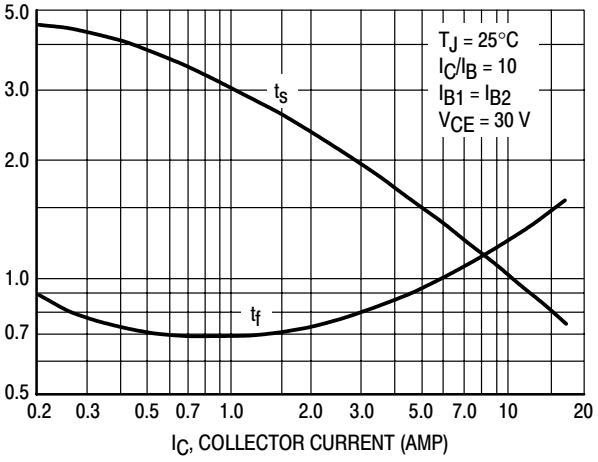


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5631



PNP
2N6031

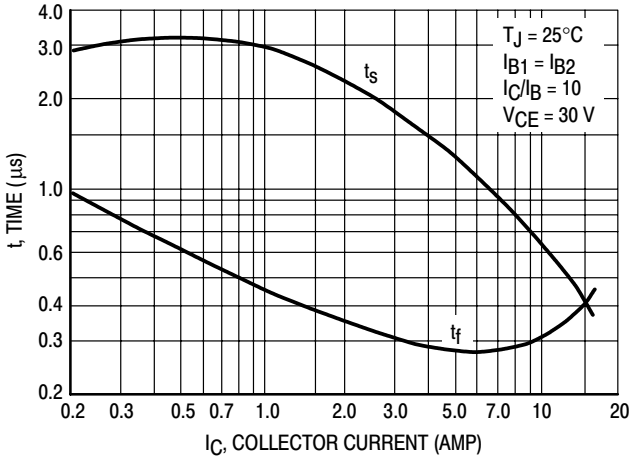
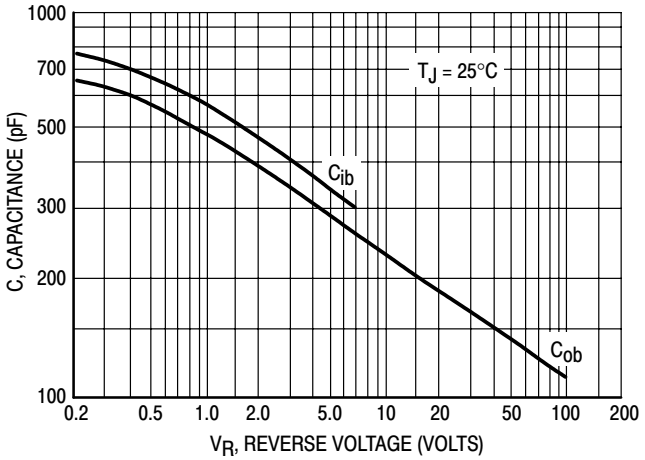


Figure 6. Turn−Off Time

NPN
2N5631



PNP
2N6031

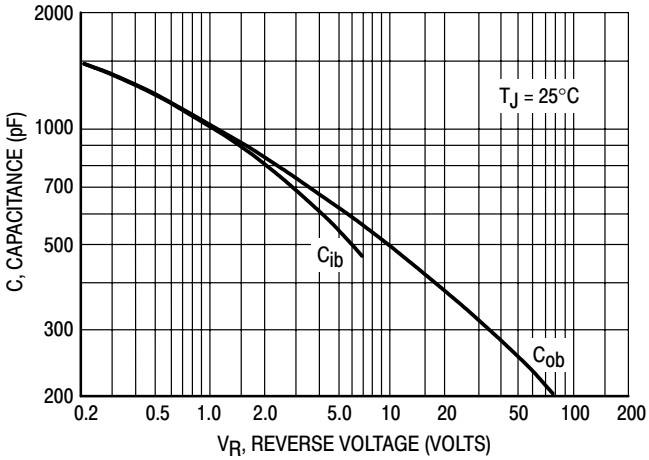
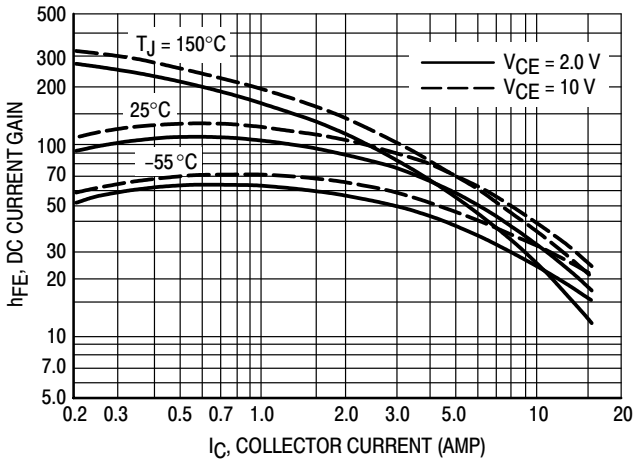


Figure 7. Capacitance



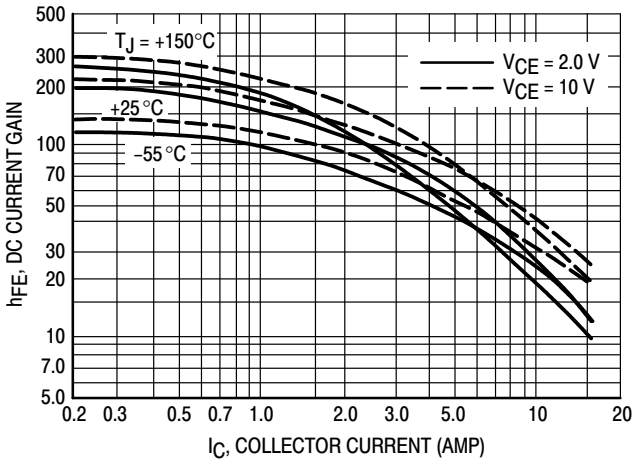
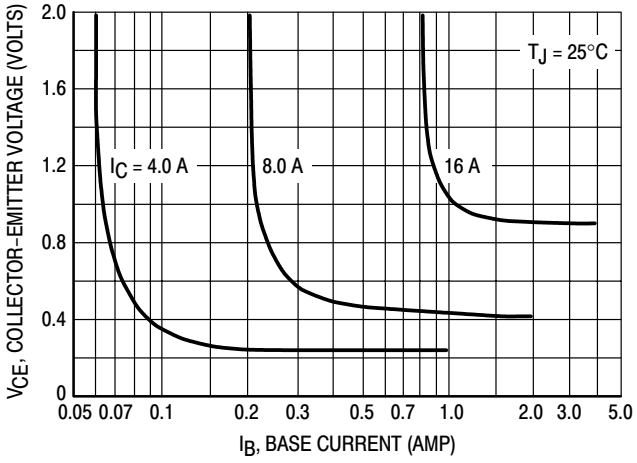


Figure 8. DC Current Gain



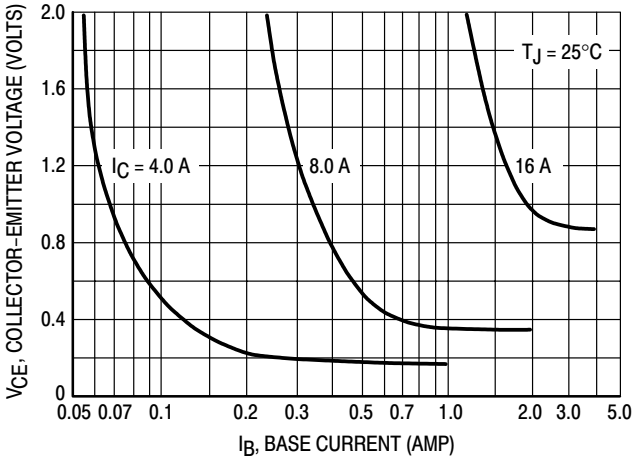


Figure 9. Collector Saturation Region

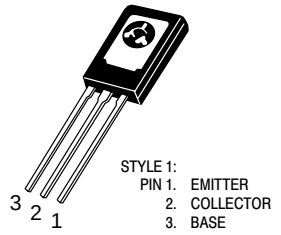
Plastic NPN Silicon High-Voltage Power Transistor

2N5655
2N5657

. . . designed for use in line−operated equipment such as audio output amplifiers; low−current, high−voltage converters; and AC line relays.

- Excellent DC Current Gain −
  h_{FE} = 30−250 @ I_C = 100 mAdc
- Current−Gain − Bandwidth Product −
  f_T = 10 MHz (Min) @ I_C = 50 mAdc

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 −350 VOLTS
20 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS (1)

Rating	Symbol	2N5655	2N5657	Unit
Collector−Emitter Voltage	V_{CEO}	250	350	Vdc
Collector−Base Voltage	V_{CB}	275	375	Vdc
Emitter−Base Voltage	V_{EB}	6.0		Vdc
Collector Current − Continuous Peak	I_C	0.5 1.0		Adc
Base Current	I_B	0.25		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

(1) Indicates JEDEC Registered Data.

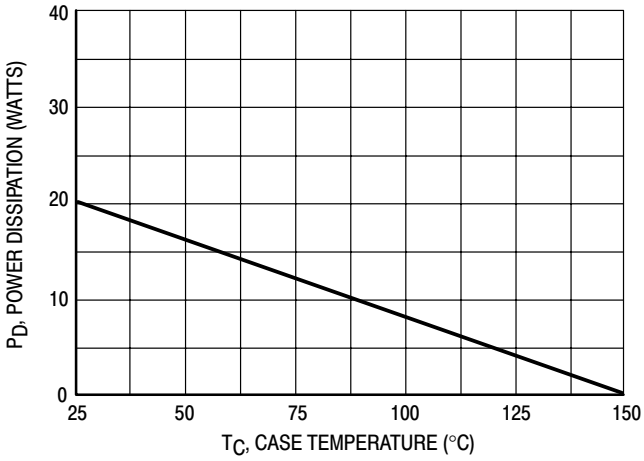


Figure 1. Power Derating

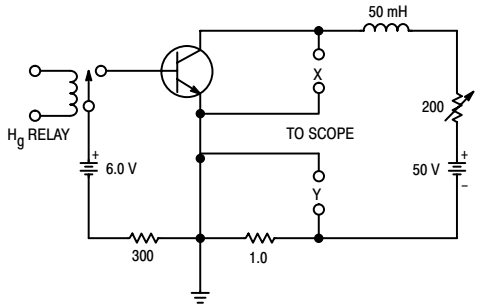


Figure 2. Sustaining Voltage Test Circuit

Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

April, 2002 − Rev. 7
Publication Order Number:
2N5655/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655 2N5657	$V_{CEO(sus)}$	250 350	− −	Vdc
Collector−Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655 2N5657	$V_{(BR)CEO}$	250 350	− −	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N5655		−	0.1	
(V_{CE} = 250 Vdc, I_B = 0)	2N5657		−	0.1	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5655		−	0.1	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5657		−	0.1	
(V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655		−	1.0	
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5657		−	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 275 Vdc, I_E = 0)	2N5655		−	10	
(V_{CB} = 375 Vdc, I_E = 0)	2N5657		−	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	−	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			−
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			25	−	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			30	250	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			15	−	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)			5.0	−	
Collector−Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)			−	1.0	
(I_C = 250 mAdc, I_B = 25 mAdc)			−	2.5	
(I_C = 500 mAdc, I_B = 100 mAdc)			−	10	
Base−Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	−	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	−	25	pF
Small−Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	−	−

*Indicates JEDEC Registered Data for 2N5655 Series.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

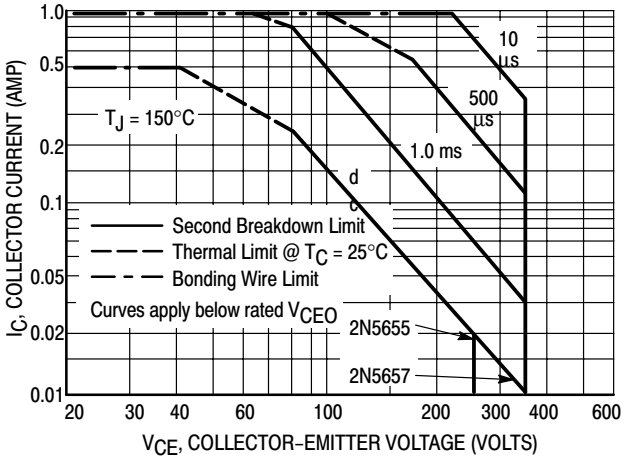


Figure 3. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

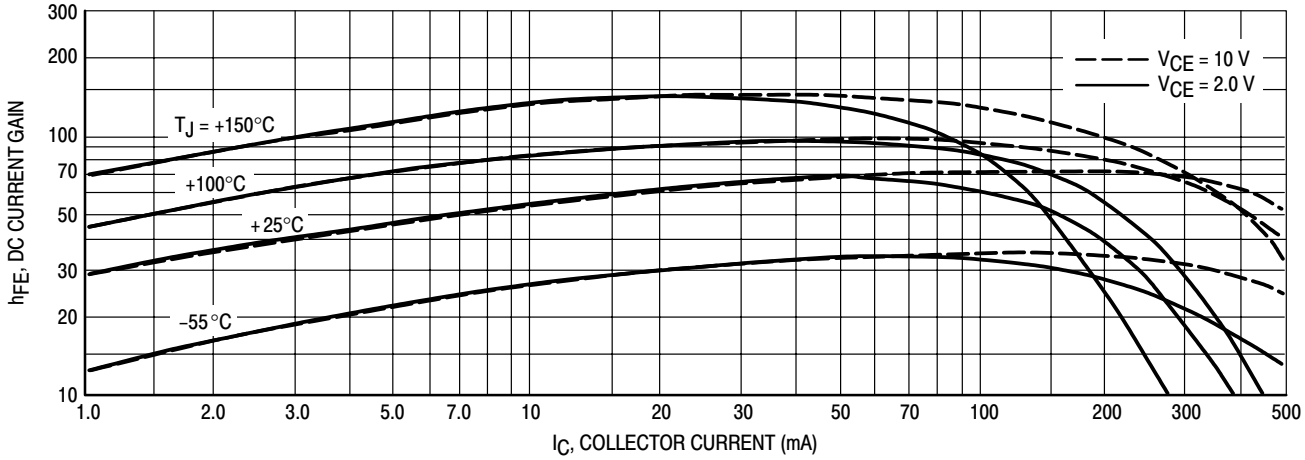


Figure 4. Current Gain

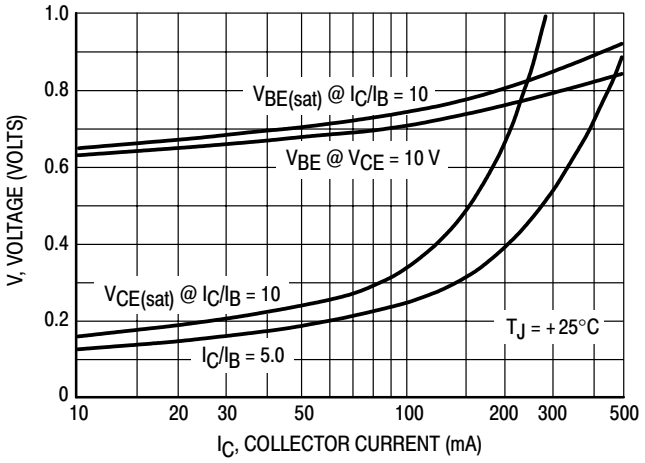


Figure 5. “On” Voltages

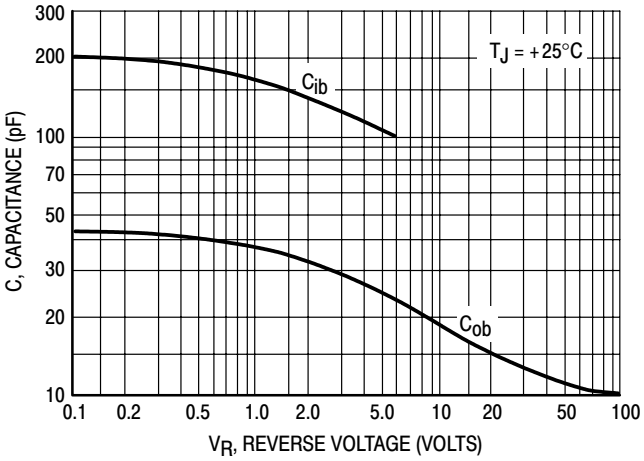


Figure 6. Capacitance

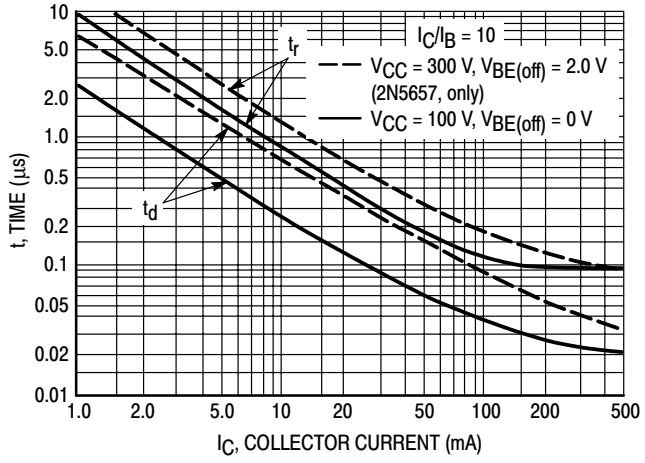


Figure 7. Turn−On Time

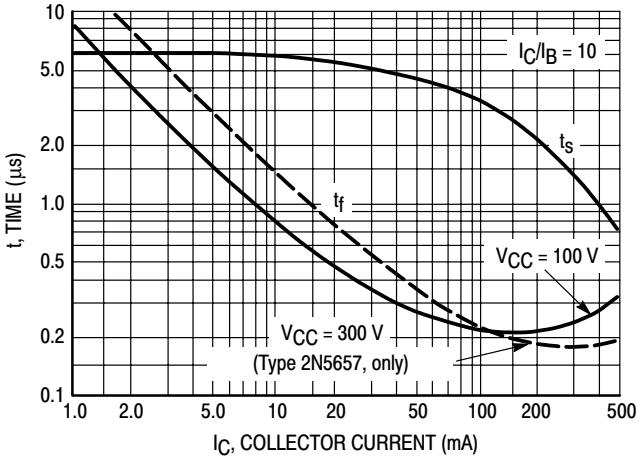


Figure 8. Turn−Off Time

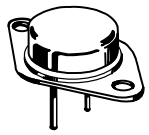
High-Current Complementary Silicon Power Transistors

. . . designed for use in high−power amplifier and switching circuit applications.

- High Current Capability − I_C Continuous = 50 Amperes.
- DC Current Gain − h_{FE} = 15−60 @ I_C = 25 Adc
- Low Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

PNP
2N5684
NPN
2N5686

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60−80 VOLTS 300 WATTS



CASE 197A−05 TO−204AE

MAXIMUM RATINGS (1)

Rating	Symbol	2N5684 2N5686	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CB}	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	50	Adc
Base Current	I_B	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	°C/W

(1) Indicates JEDEC Registered Data.

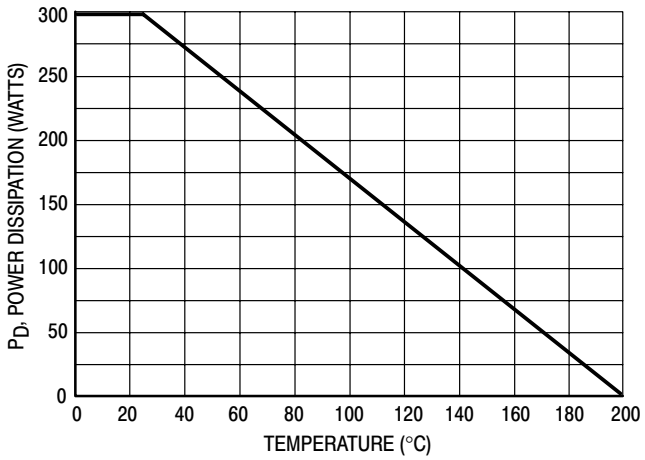


Figure 1. Power Derating

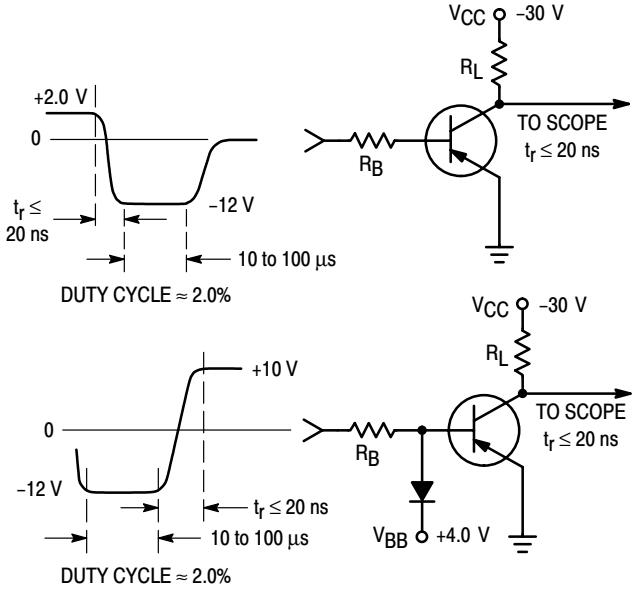
Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	80	−	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	−	1.0	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	− −	2.0 10	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	−	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 2) (I_C = 25 Adc, V_{CE} = 2.0 Vdc) (I_C = 50 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	15 5.0	60 −	−
Collector−Emitter Saturation Voltage (Note 2) (I_C = 25 Adc, I_B = 2.5 Adc) (I_C = 50 Adc, I_B = 10 Adc)	$V_{CE(sat)}$	− −	1.0 5.0	Vdc
Base−Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc)	$V_{BE(sat)}$	−	2.0	Vdc
Base−Emitter On Voltage (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	−	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	−	MHz
Output Capacitance 2N5684 (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) 2N5686	C_{ob}	− −	2000 1200	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	15	−	

*Indicates JEDEC Registered Data.

Note 2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

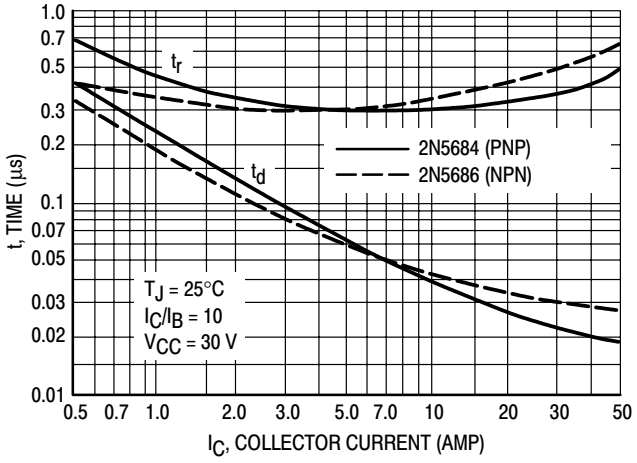


Figure 3. Turn−On Time

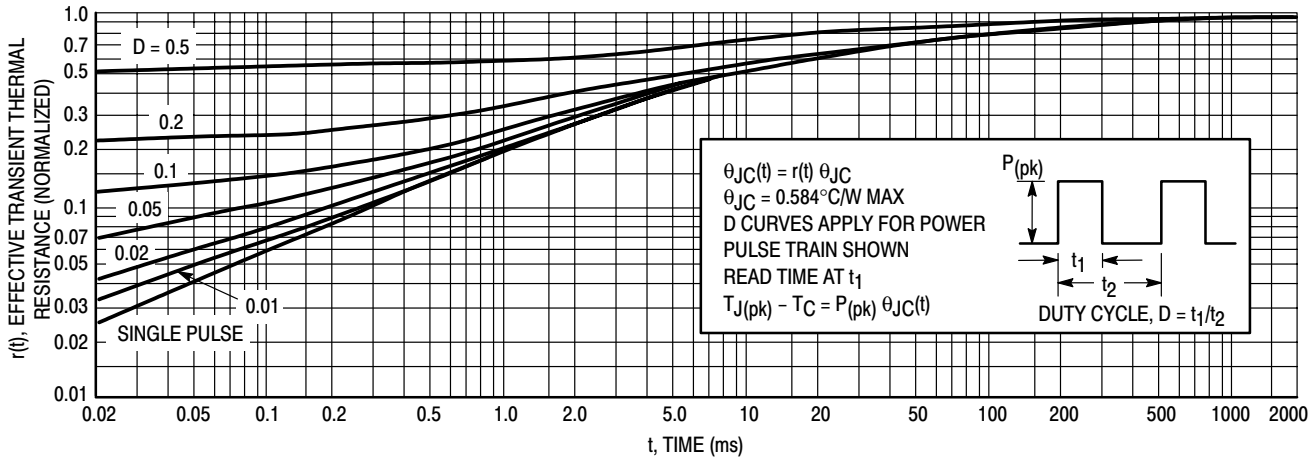


Figure 4. Thermal Response

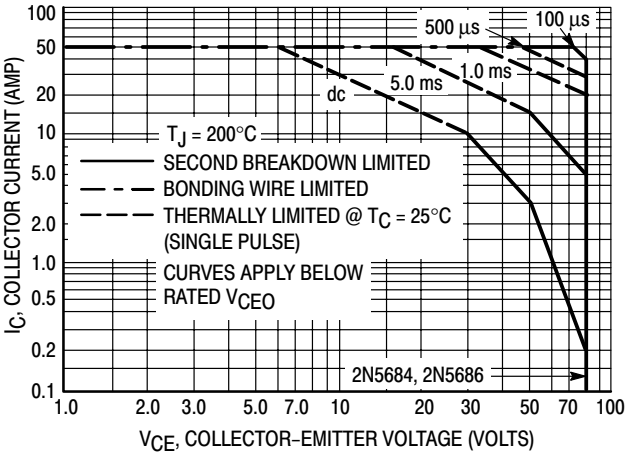


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

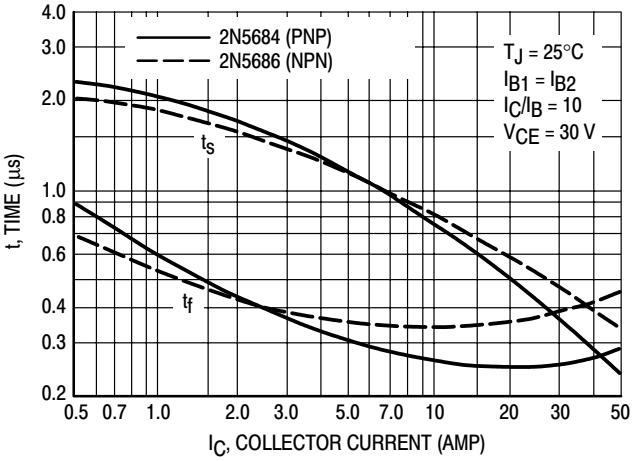


Figure 6. Turn−Off Time

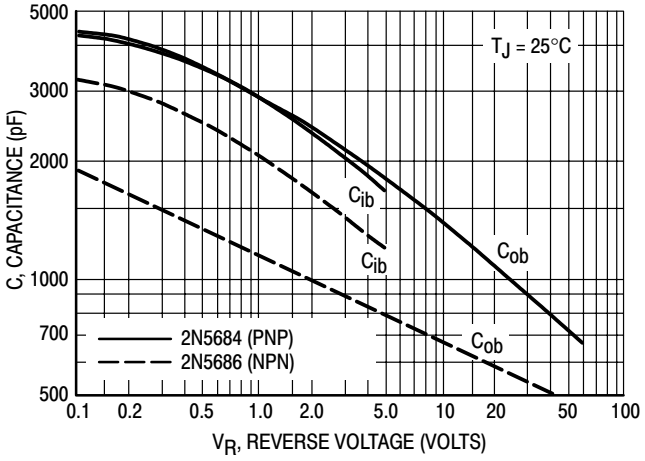
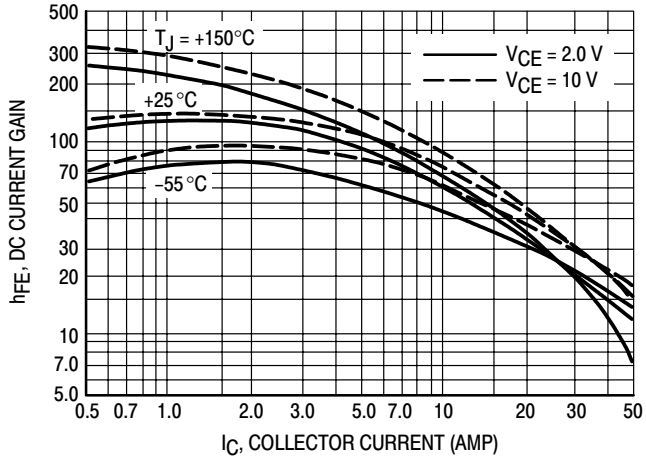


Figure 7. Capacitance

PNP
2N5684



NPN
2N5686

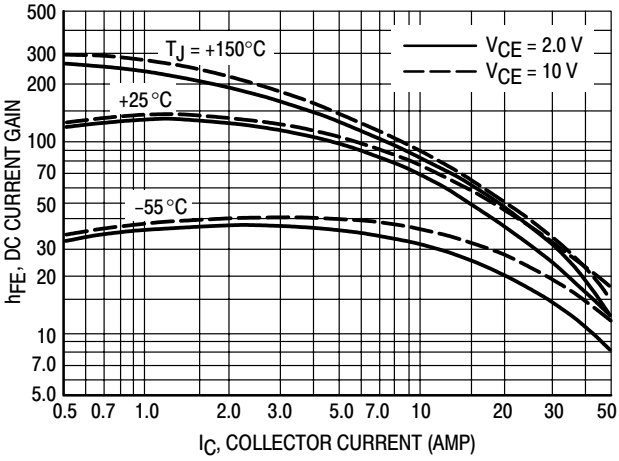
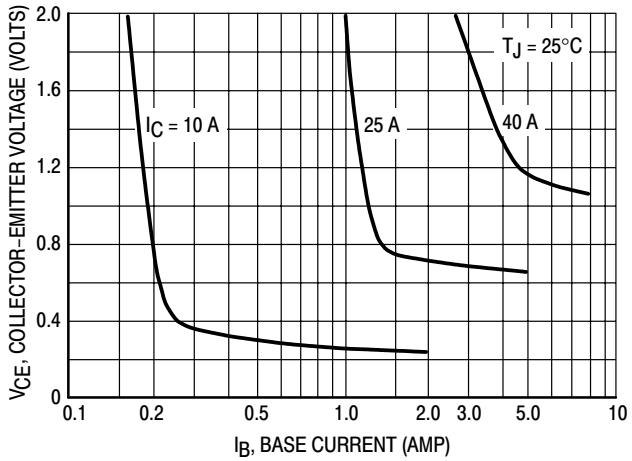


Figure 8. DC Current Gain



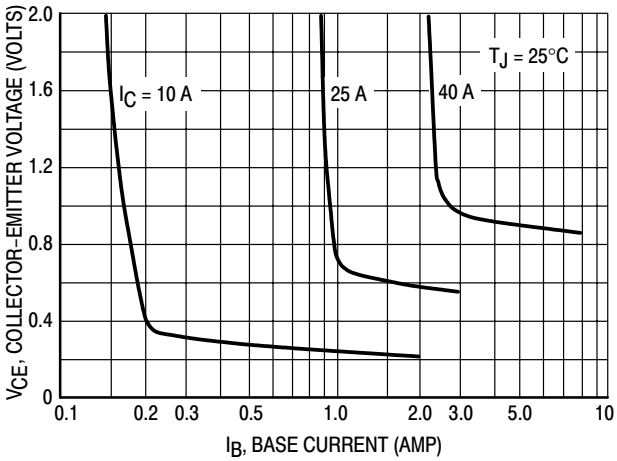
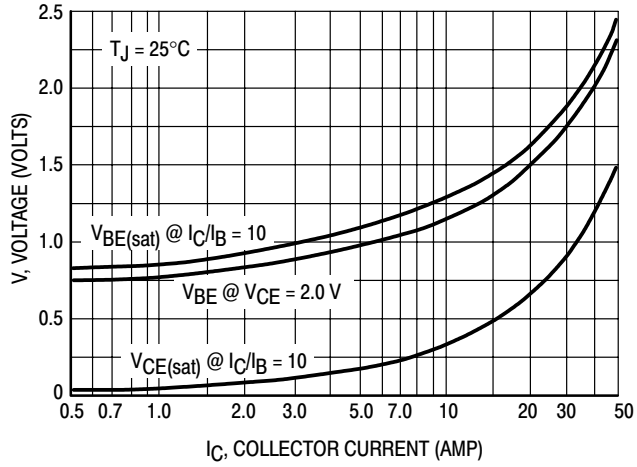


Figure 9. Collector Saturation Region



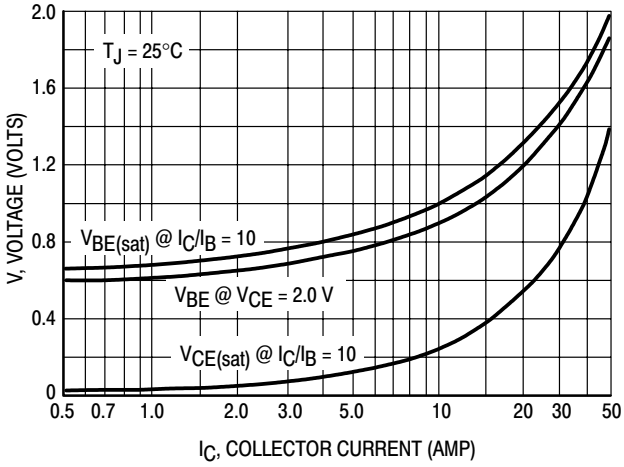


Figure 10. “On” Voltages

PNP 2N5883, 2N5884*, NPN 2N5885, 2N5886*

Preferred Device

Complementary Silicon High-Power Transistors

. . . designed for general−purpose power amplifier and switching applications.

- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current
  I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain −
  h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product −
  f_τ = 4.0 MHz (min) at I_C = 1.0 Adc

MAXIMUM RATINGS (No

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current − Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

1. Indicates JEDEC registered data. Units and conditions differ on some parameters and re−registration reflecting these changes has been requested. All above values most or exceed present JEDEC registered data.

ON Semiconductor®

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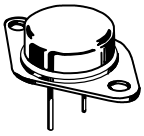
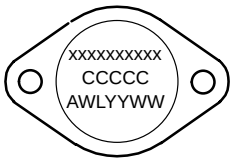
25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60 − 80 V 200 W

MARKING DIAGRAM





CASE 1−07
TO−204AA
(TO−3)

xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
CCCCC = Non USA Country Code

Preferred devices are recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	60 80	− −	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5883, 2N5885 2N5984, 2N5886	I_{CEO}	− −	2.0 2.0	mAdc
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5883, 2N5885		−	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5884, 2N5886		−	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5883, 2N5885			10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5884, 2N5886		−	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5883, 2N5885		−	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5884, 2N5886		−	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (Note 2)	(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 25 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	35 20 4.0	− 100	−
Collector−Emitter Saturation Voltage (Note 2)	(I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 25 Adc, I_B = 6.25 Adc)	$V_{CE(sat)}$	− −	1.0 4.0	Vdc
Base−Emitter Saturation Voltage (Note 2)	(I_C = 25 Adc, I_B = 6.25 Adc)	$V_{BE(sat)}$	−	2.5	Vdc
Base−Emitter On Voltage (Note 2)	(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current−Gain − Bandwidth Product (Note 3)	(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884 2N5885, 2N5886	C_{ob}	− −	1000 500	pF
Small−Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)		h_{fe}	20	−	−

SWITCHING CHARACTERISTICS

Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	−	0.7	μs
Storage Time		t_s	−	1.0	μs
Fall Time		t_f	−	0.8	μs

*Indicates JEDEC Registered Data.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. $f_T = |h_{fe}| \bullet f_{test}$.

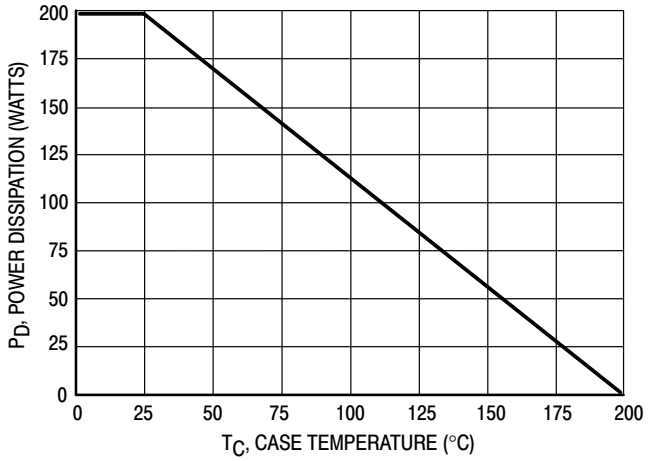
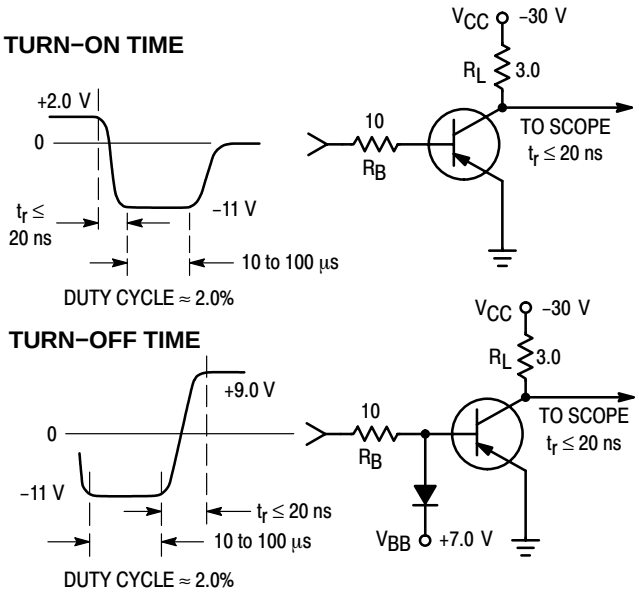


Figure 1. Power Derating



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

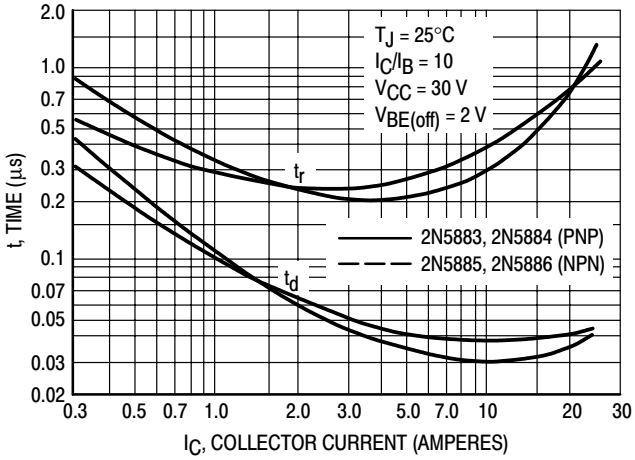


Figure 3. Turn−On Time

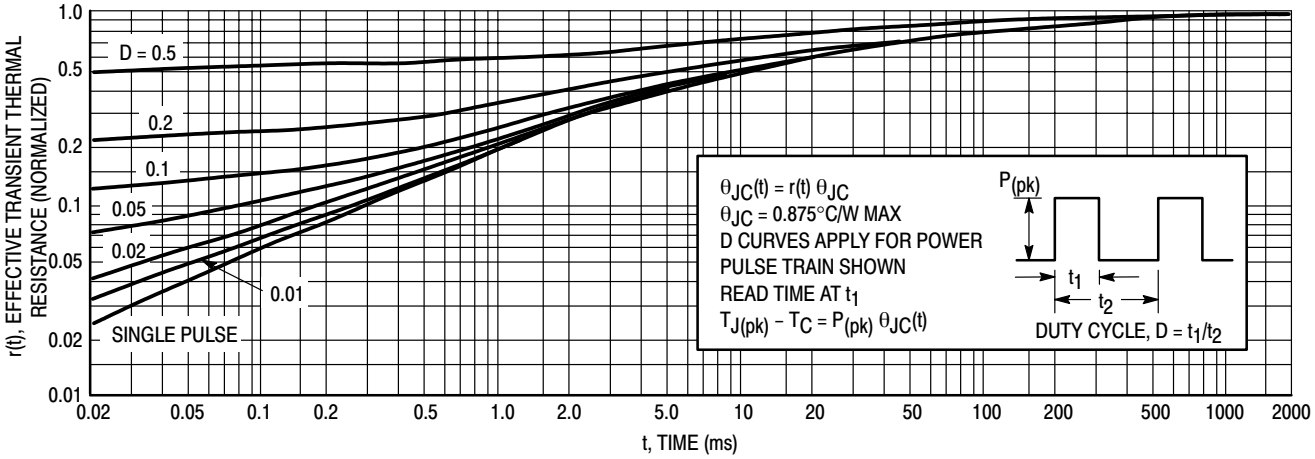


Figure 4. Thermal Response

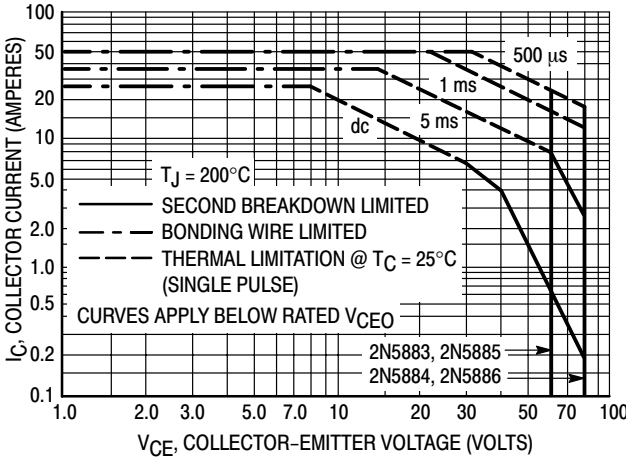


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

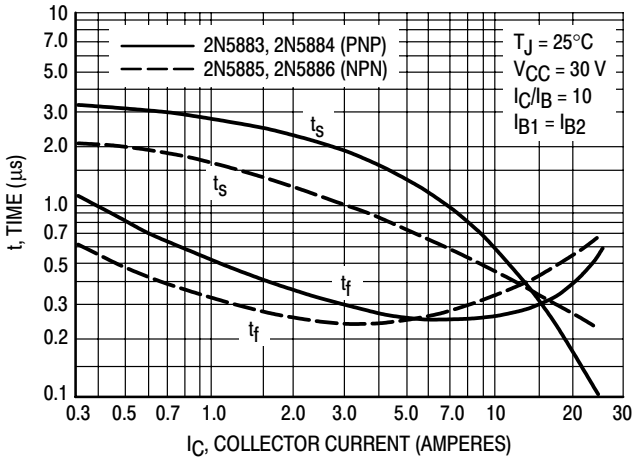


Figure 6. Turn−Off Time

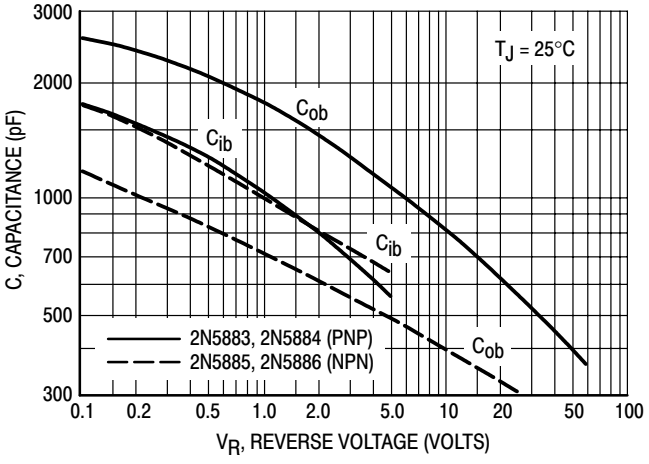


Figure 7. Capacitance

PNP DEVICES
2N5883 and 2N5884

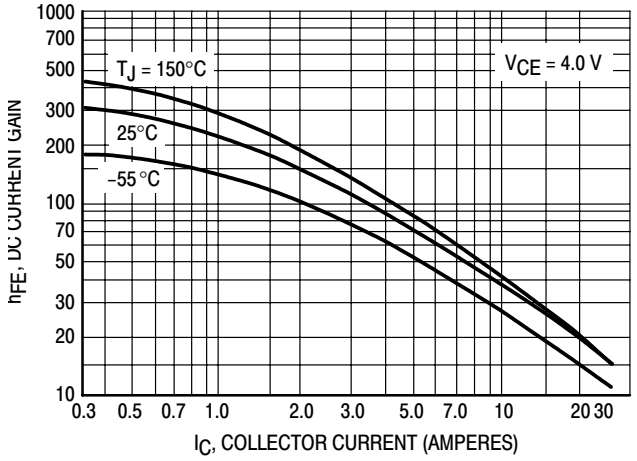


Figure 8. DC Current Gain

NPN DEVICES
2N5885 and 2N5886

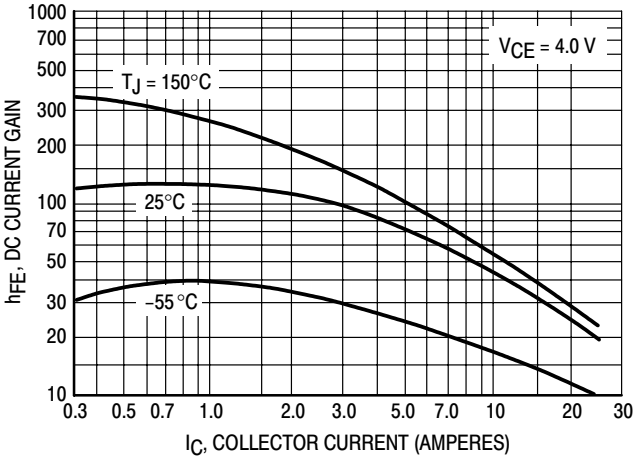


Figure 9. DC Current Gain

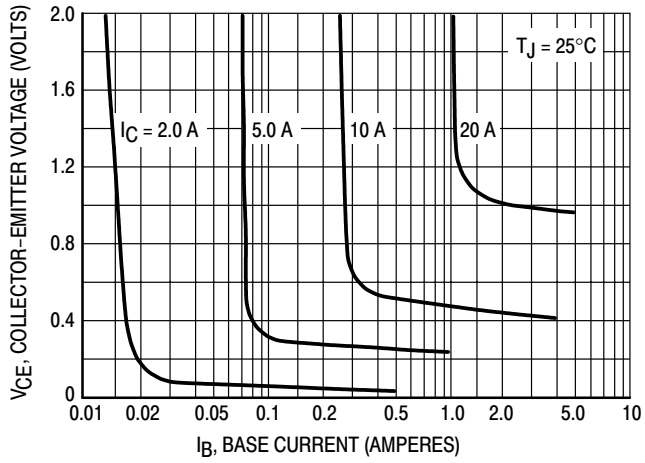


Figure 10. Collector Saturation Region

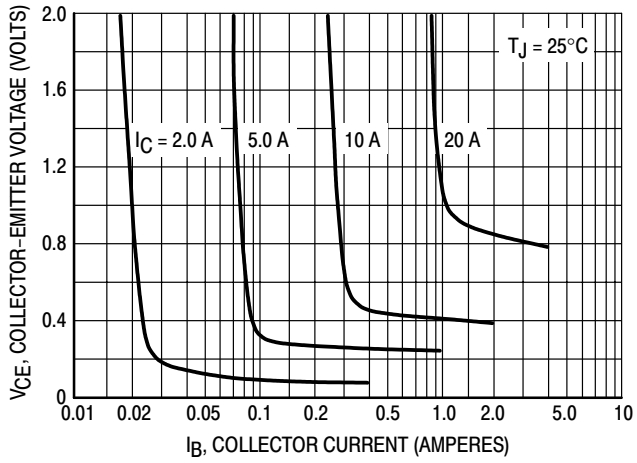


Figure 11. Collector Saturation Region

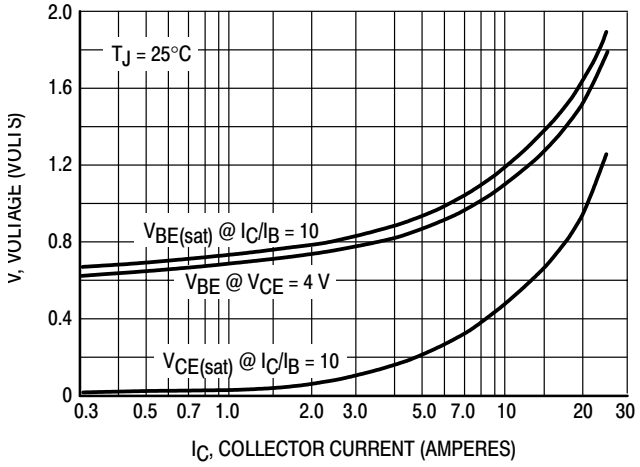


Figure 12. “On” Voltages

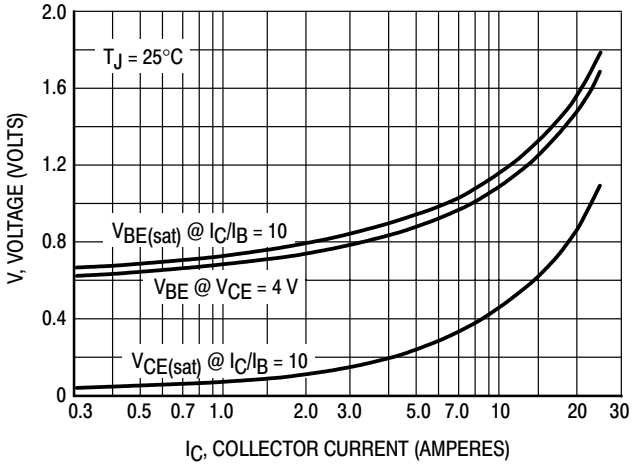


Figure 13. “On” Voltages

(PNP) 2N6034, 2N6035, 2N6036 (NPN) 2N6038, 2N6039

Plastic Darlington Complementary Silicon Power Transistors

. . . designed for general−purpose amplifier and low−speed switching applications.

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V−0 @ 1/8”

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N6034 2N6035, 2N6038 2N6036, 2N6039	V_{CEO}	40 60 80	Vdc
Collector−Base Voltage 2N6034 2N6035, 2N6038 2N6036, 2N6039	V_{CBO}	40 60 80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous Peak	I_C	4.0 8.0	Adc Apk
Base Current	I_B	100	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

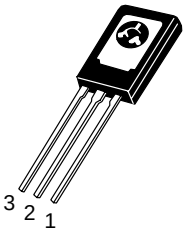
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	83.3	°C/W

ON Semiconductor®

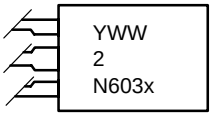
http://onsemi.com

4.0 A DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 40, 60, 80 V, 40 W



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



x = 4, 5, 6, 8, 9
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6034	TO−225AA	500 Units/Box
2N6035	TO−225AA	500 Units/Box
2N6036	TO−225AA	500 Units/Box
2N6038	TO−225AA	500 Units/Box
2N6039	TO−225AA	500 Units/Box

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6034	$V_{CEO(sus)}$	40	—	Vdc
	2N6035, 2N6038		60	—	
	2N6036, 2N6039		80	—	
Collector−Cutoff Current		I_{CEO}			μA
(V_{CE} = 40 Vdc, I_B = 0)	2N6034		—	100	
(V_{CE} = 60 Vdc, I_B = 0)	2N6035, 2N6038		—	100	
(V_{CE} = 80 Vdc, I_B = 0)	2N6036, 2N6039		—	100	
Collector−Cutoff Current		I_{CEX}			μA
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6034		—	100	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6035, 2N6038		—	100	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6036, 2N6039		—	100	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6034		—	500	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6035, 2N6038		—	500	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6036, 2N6039		—	500	
Collector−Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6034		—	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N6035, 2N6038		—	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N6036, 2N6039		—	0.5	
Emitter−Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			500	—	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	15,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			—	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			—	3.0	
Base−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base−Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current−Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	—	—
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6034, 2N6035, 2N6036		—	200	
	2N6038, 2N6039		—	100	

*Indicates JEDEC Registered Data.

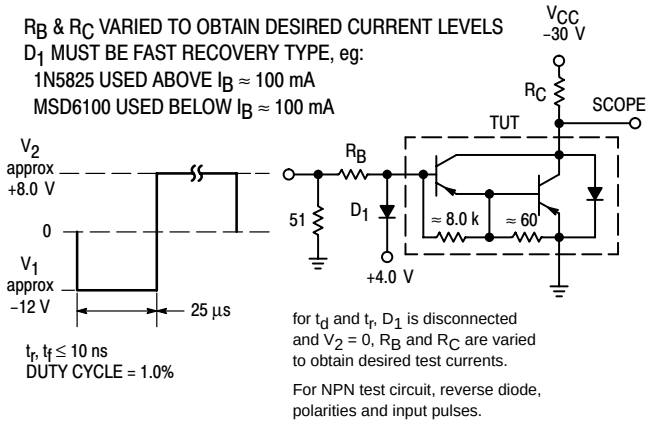


Figure 14. Switching Times Test Circuit

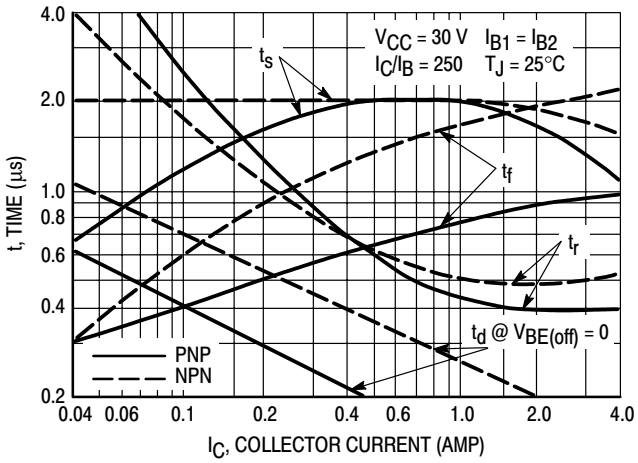


Figure 15. Switching Times

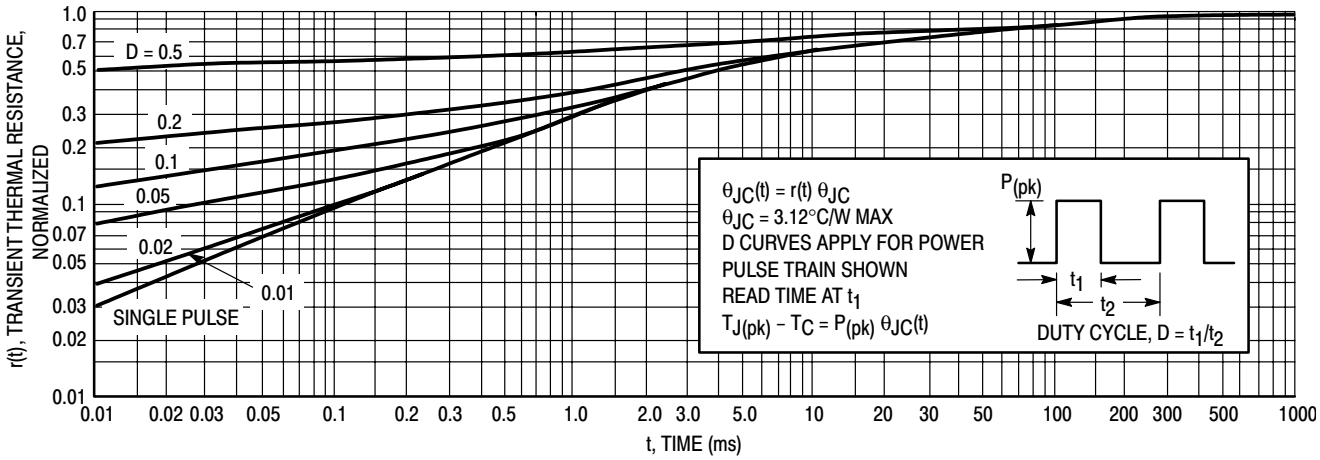


Figure 16. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

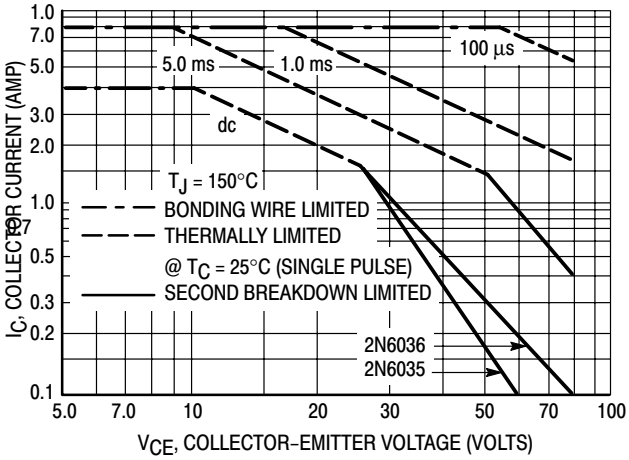


Figure 17. 2N6035, 2N6036

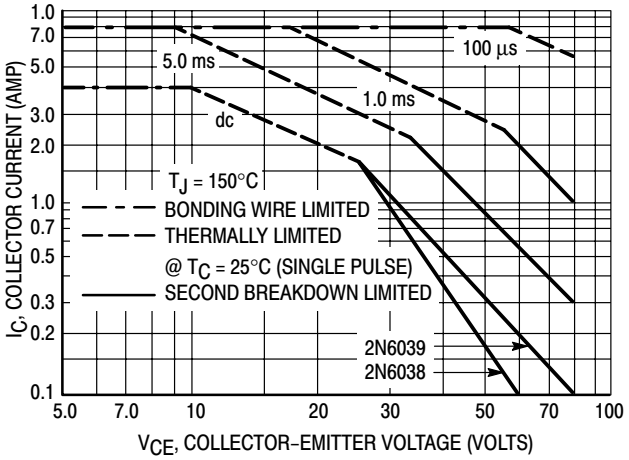


Figure 18. 2N6038, 2N6039

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 17 and 18 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

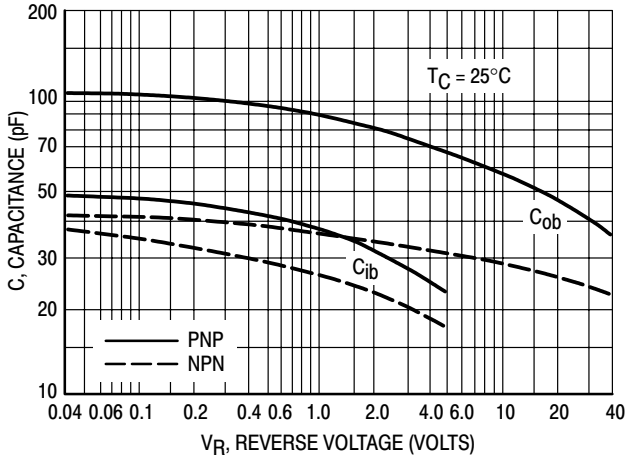
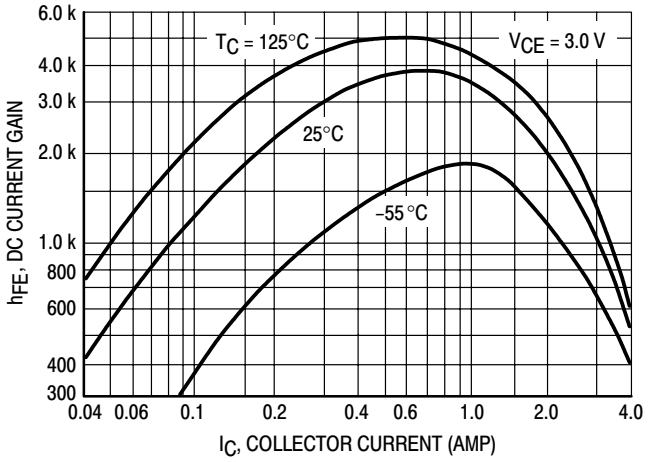


Figure 19. Capacitance

PNP
2N6034, 2N6035, 2N6036



NPN
2N6038, 2N6039

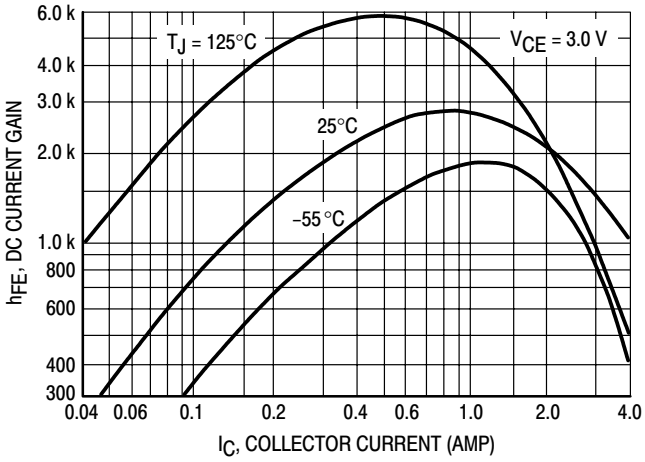
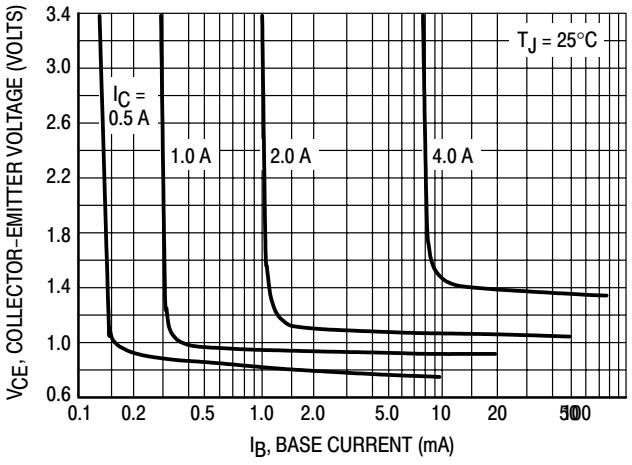


Figure 20. DC Current Gain



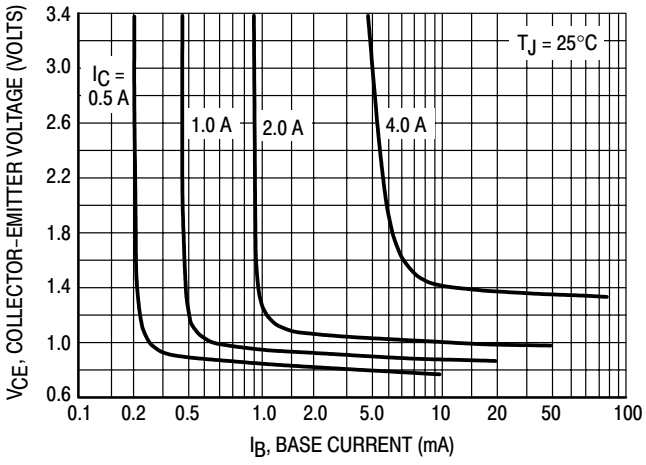
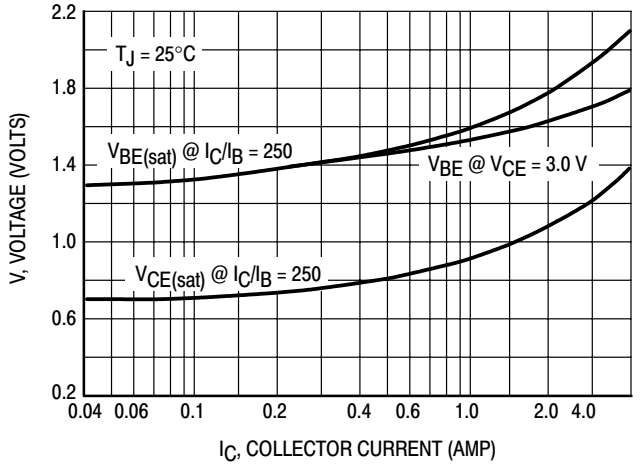


Figure 21. Collector Saturation Region



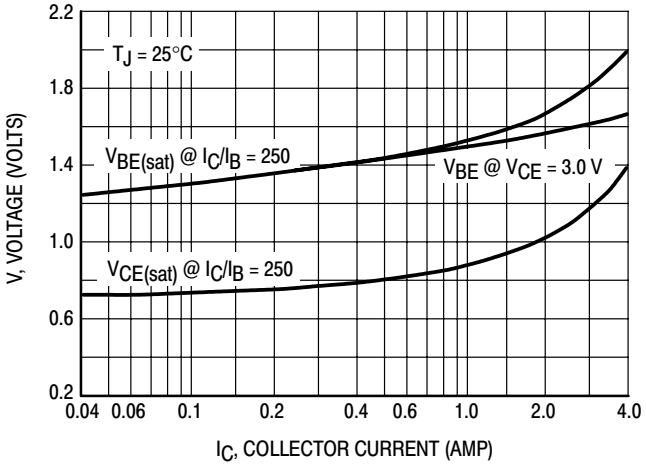


Figure 22. “On” Voltages

(PNP) 2N6040, 2N6042, (NPN) 2N6043*, 2N6045*

*Preferred Device

Plastic Medium-Power Complementary Silicon Transistors

. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 100 mAdc −
  $V_{CEO(sus)}$ = 60 Vdc (Min) − 2N6040, 2N6043
  = 100 Vdc (Min) − 2N6042, 2N6045
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc − 2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc − 2N6042, 2N6045
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- EPOXY MEETS UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS (Note 4)

Rating	Symbol	2N6040 2N6043	2N6042 2N6045	Unit
Collector−Emitter Voltage	V_{CEO}	60	100	Vdc
Collector−Base Voltage	V_{CB}	60	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current− Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	120		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60		W W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

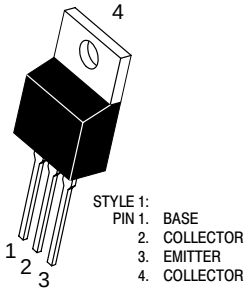
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

4. Indicates JEDEC Registered Data.

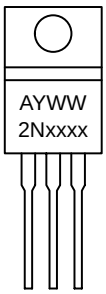
ON Semiconductor®

http://onsemi.com

DARLINGTON, 8 A COMPLEMENTARY SILICON POWER TRANSISTORS 60 V − 100 V, 75 W



MARKING DIAGRAM



TO−220AB
CASE 221A−09
Style 1

xxxx = Specific Device Code:
6040, 6042, 6043, 6045
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6040	TO−220AB	50 Units / Rail
2N6042	TO−220AB	50 Units / Rail
2N6043	TO−220AB	50 Units / Rail
2N6045	TO−220AB	50 Units / Rail

***Preferred** devices are recommended choices for future use and best overall value.

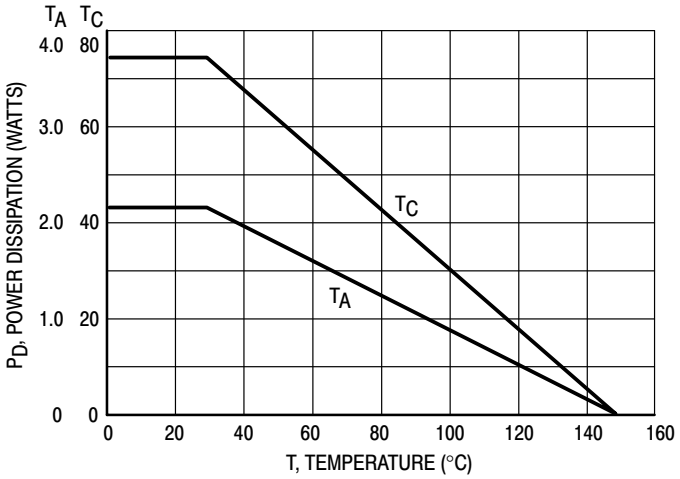


Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043	$V_{CEO(sus)}$	60	–	Vdc
	2N6042, 2N6045		100	–	
Collector Cutoff Current		I_{CEO}			μA
(V_{CE} = 60 Vdc, I_B = 0)	2N6040, 2N6043		–	20	
(V_{CE} = 100 Vdc, I_B = 0)	2N6042, 2N6045		–	20	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6040, 2N6043		–	20	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6042, 2N6045		–	20	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6041, 2N6044		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6042, 2N6045		–	200	
Collector Cutoff Current		I_{CBO}			μA
(V_{CB} = 60 Vdc, I_E = 0)	2N6040, 2N6043		–	20	
(V_{CB} = 100 Vdc, I_E = 0)	2N6042, 2N6045		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	2N6040, 2N6043,		1000	20.000	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6042, 2N6045		1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	All Types		100	–	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)	2N6040, 2N6043,		–	2.0	
(I_C = 3.0 Adc, I_B = 12 mAdc)	2N6042, 2N6045		–	2.0	
(I_C = 8.0 Adc, I_B = 80 Adc)	All Types		–	4.0	
Base−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.5	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	
Output Capacitance	2N6040/2N6042	C_{ob}	–	300	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6043/2N6045		–	200	
Small−Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data.

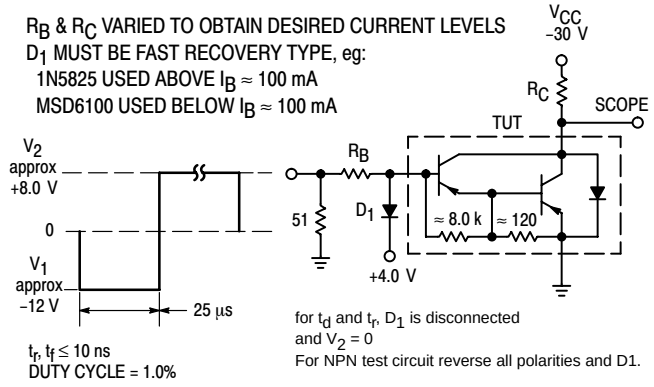


Figure 2. Switching Times Equivalent Circuit

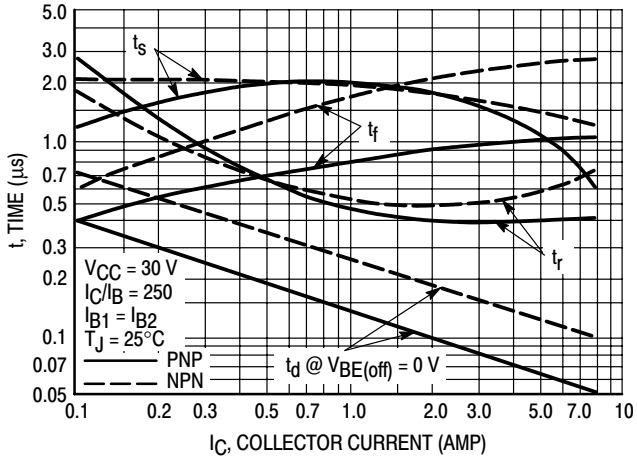


Figure 3. Switching Times

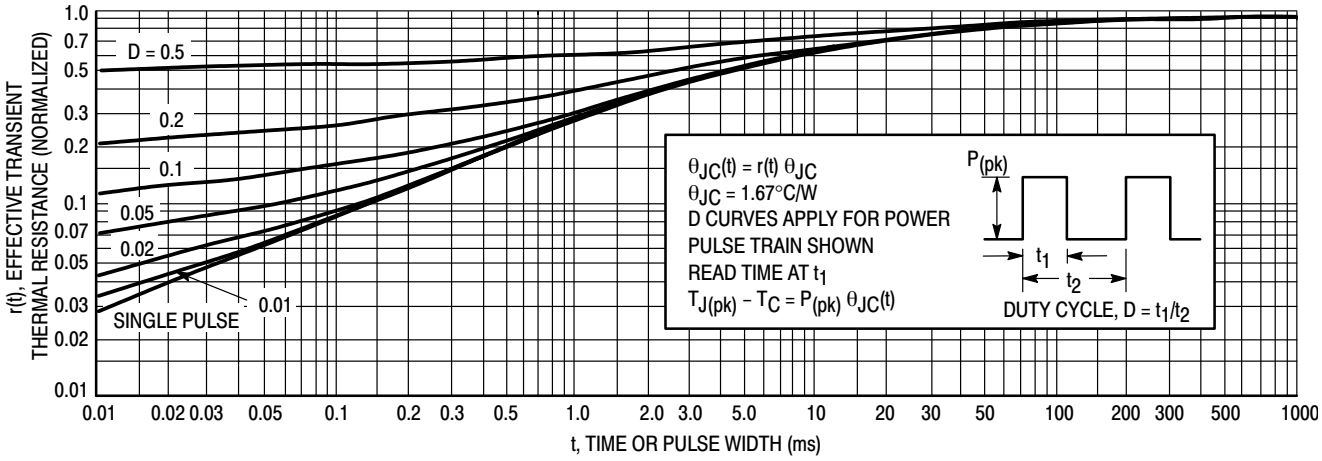


Figure 4. Thermal Response

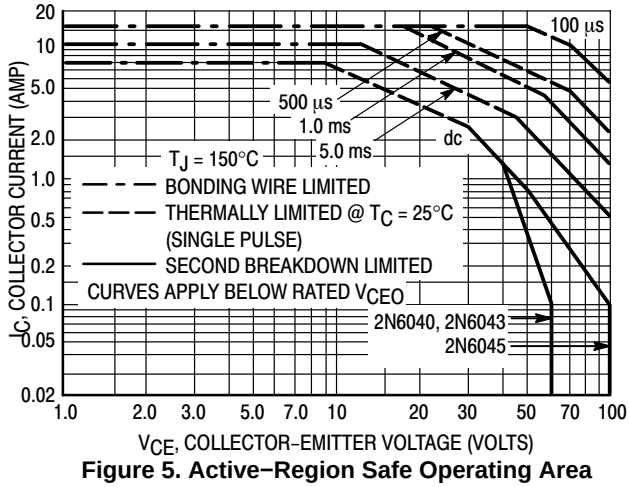


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

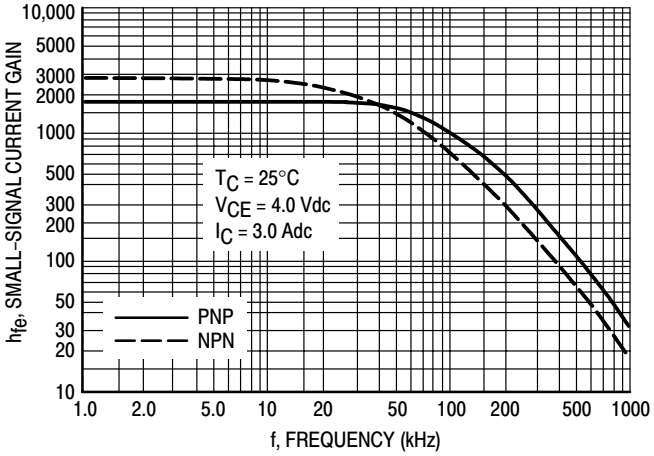


Figure 6. Small−Signal Current Gain

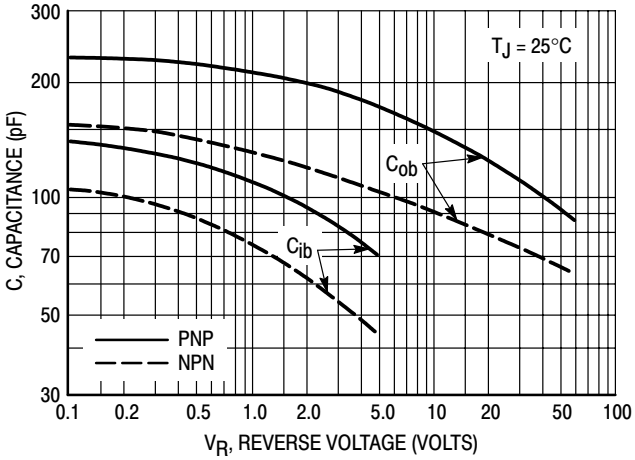
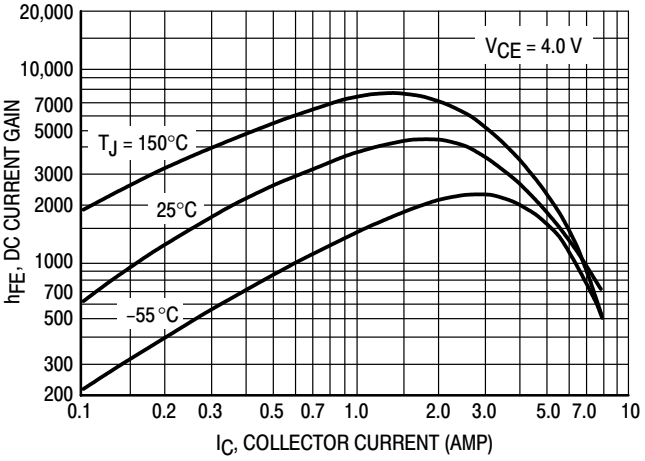


Figure 7. Capacitance

PNP
2N6040, 2N6042



NPN
2N6043, 2N6045

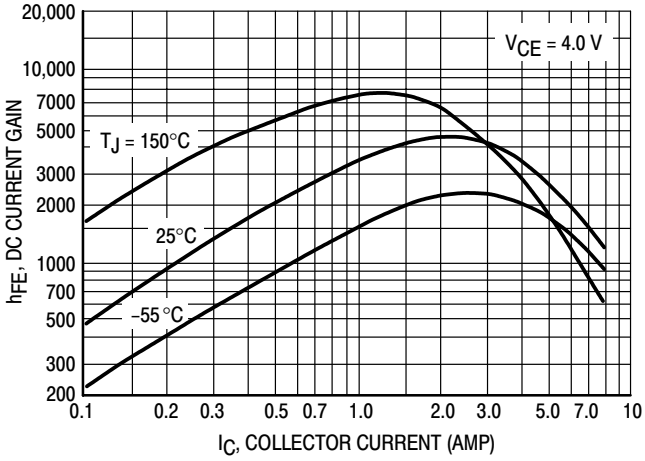
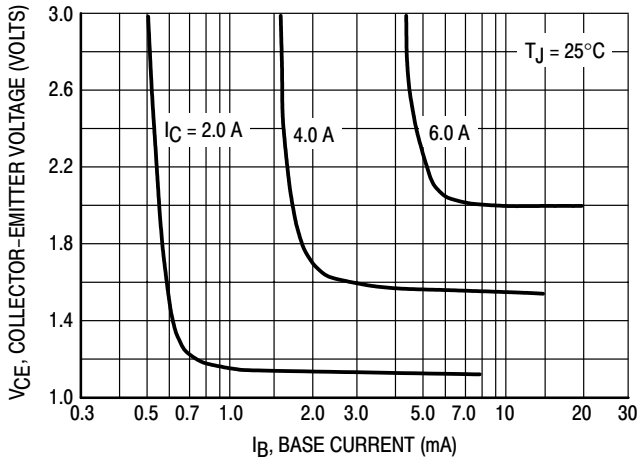


Figure 8. DC Current Gain



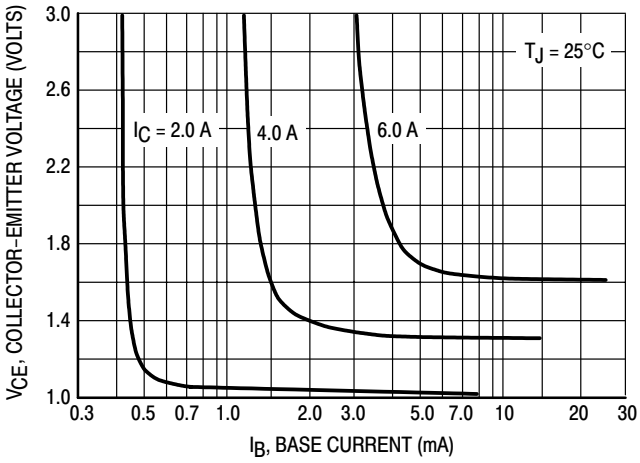
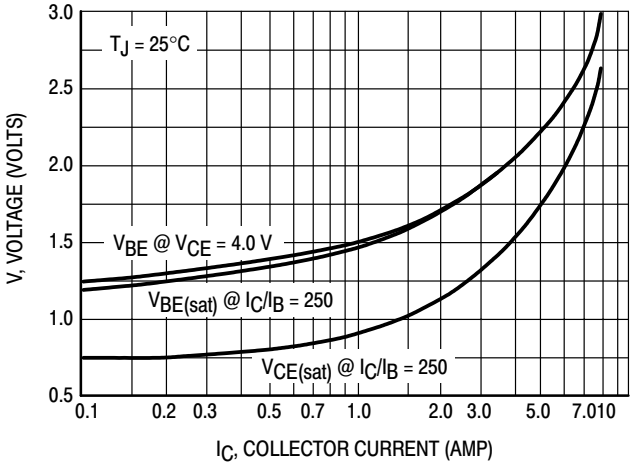


Figure 9. Collector Saturation Region



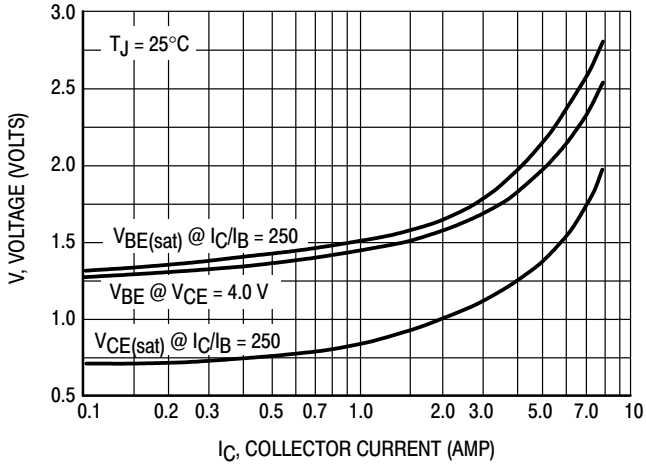


Figure 10. “On” Voltages

Darlington Complementary Silicon Power Transistors

. . . designed for general−purpose amplifier and low frequency switching applications.

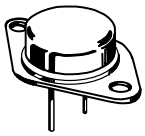
- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector−Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors

PNP
2N6052*

NPN
2N6058
2N6059*

***ON Semiconductor Preferred Device**

DARLINGTON
12 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80−100 VOLTS
150 WATTS



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6058	2N6052 2N6059	Unit
Collector−Emitter Voltage	V_{CEO}	80	100	Vdc
Collector−Base Voltage	V_{CB}	80	100	Vdc
Emitter−Base voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	12 20		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200°C		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

(1) Indicates JEDEC Registered Data.

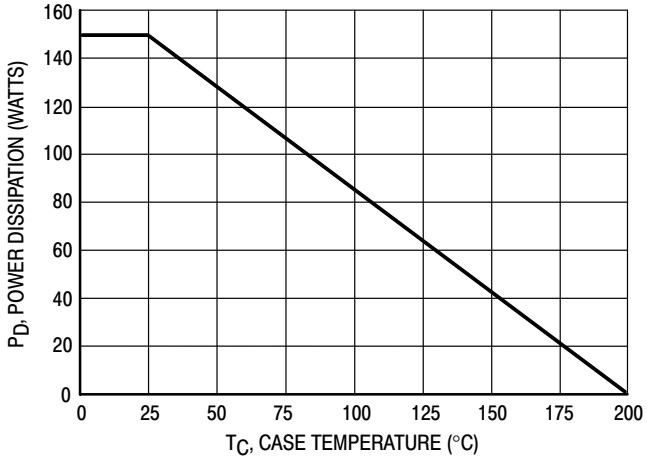


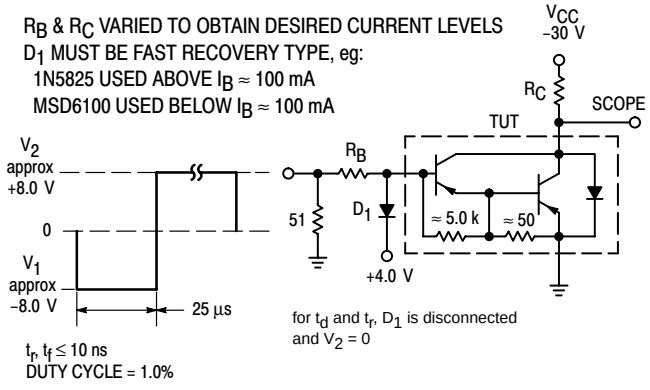
Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (2) (I_C = 100 mAdc, I_B = 0)	2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 2N6058 2N6052, 2N6059	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 —	—
Collector−Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base−Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base−Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small−Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6052 2N6058/2N6059	C_{ob}	— —	500 300	pF
Small−Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

*Indicates JEDEC Registered Data.
(2) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

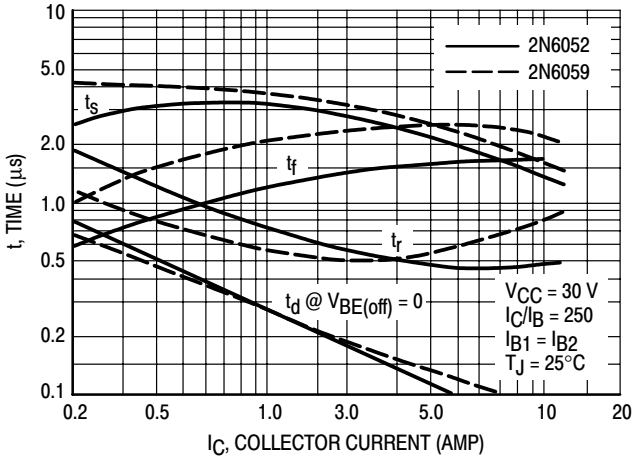


Figure 3. Switching Times

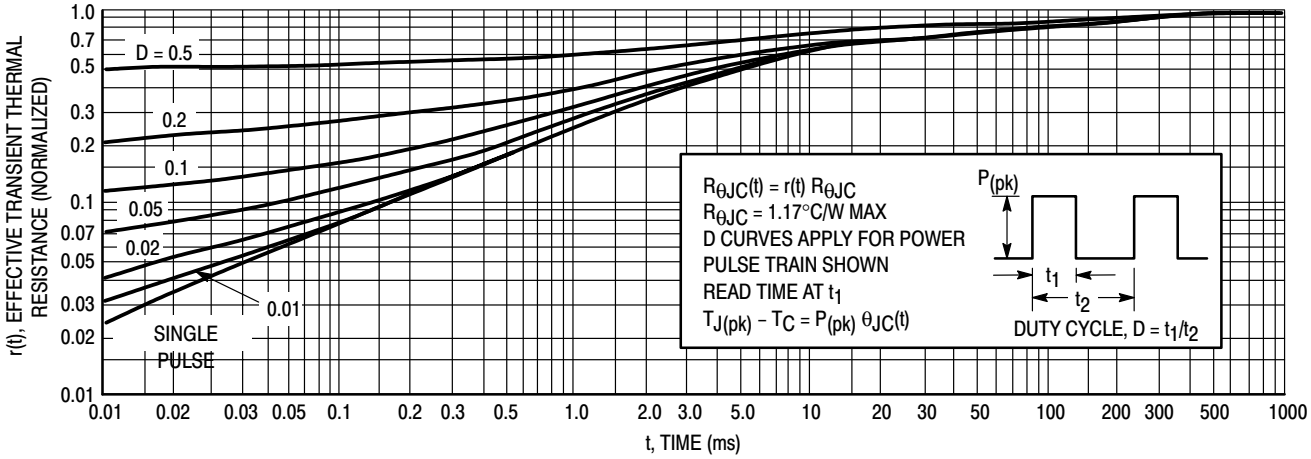


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

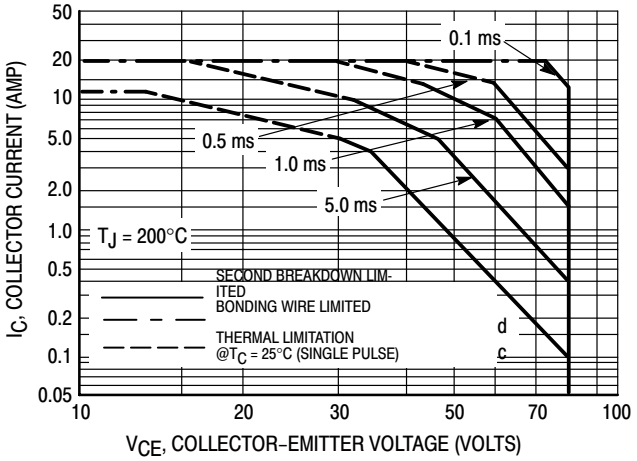


Figure 5. 2N6058

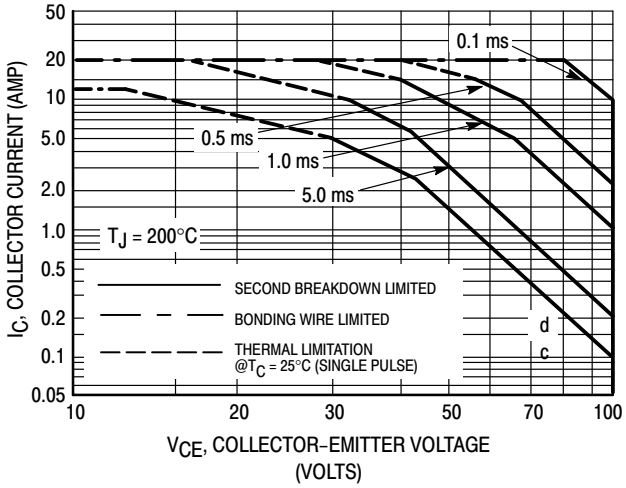


Figure 6. 2N6052, 2N6059

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6, and 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$; $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

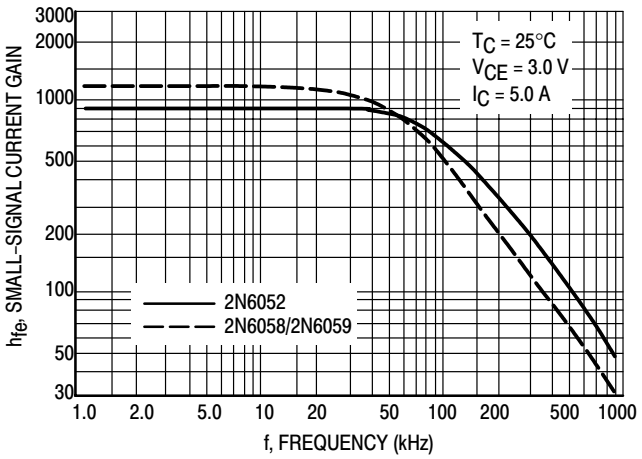


Figure 7. Small−Signal Current Gain

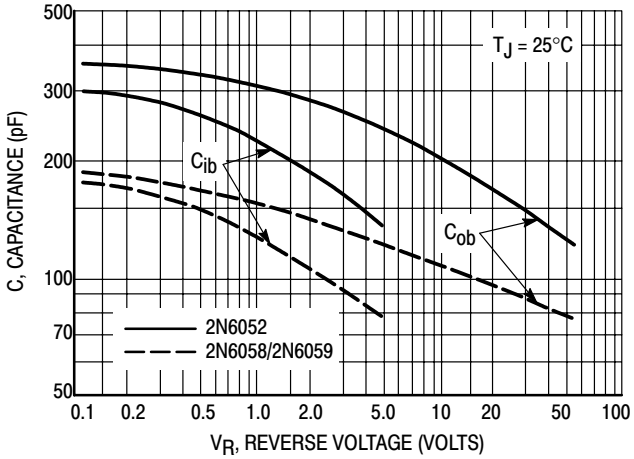


Figure 8. Capacitance

PNP
2N6052

NPN
2N6058, 2N6059

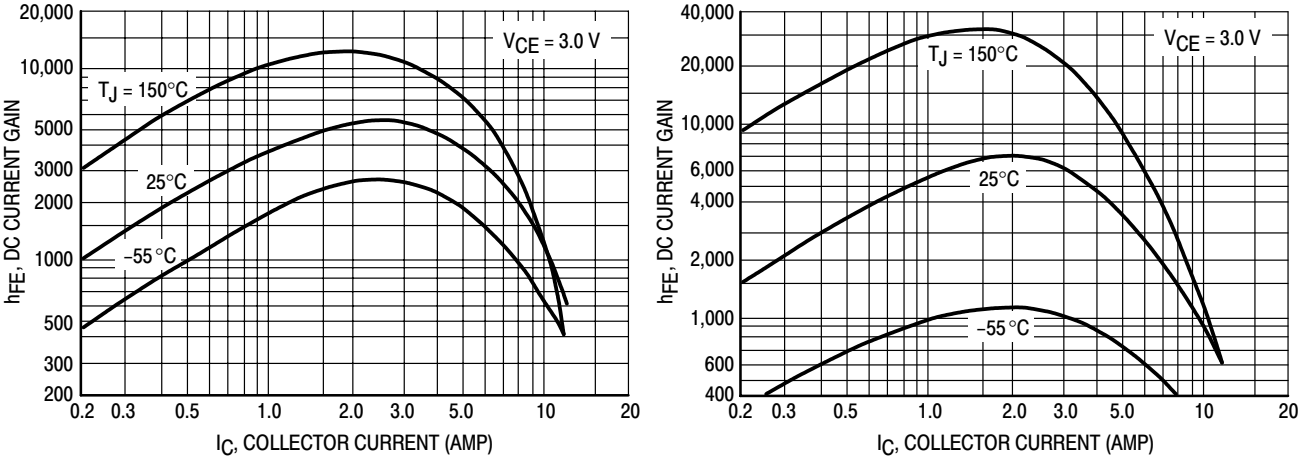


Figure 9. DC Current Gain

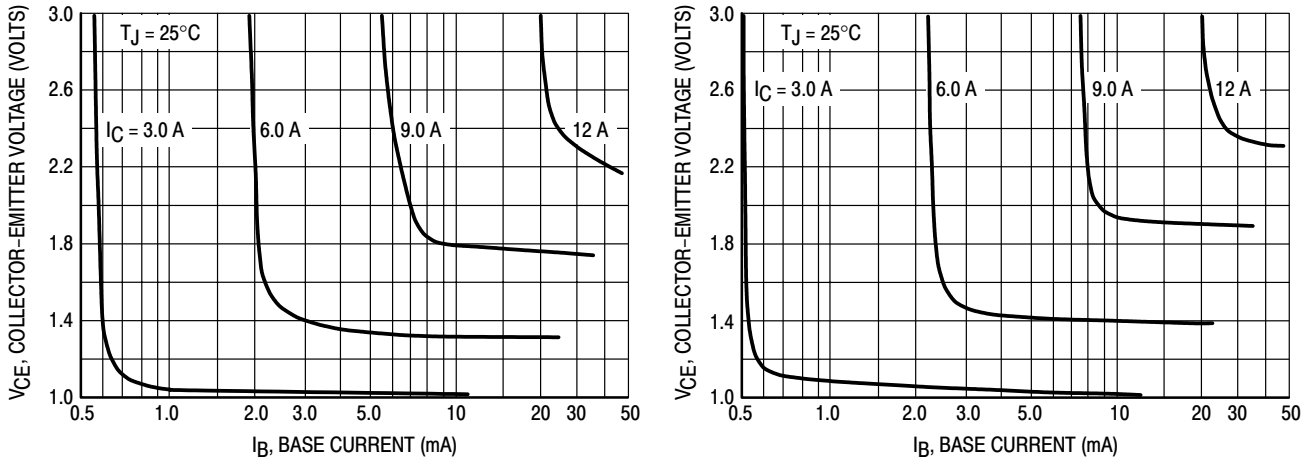


Figure 10. Collector Saturation Region

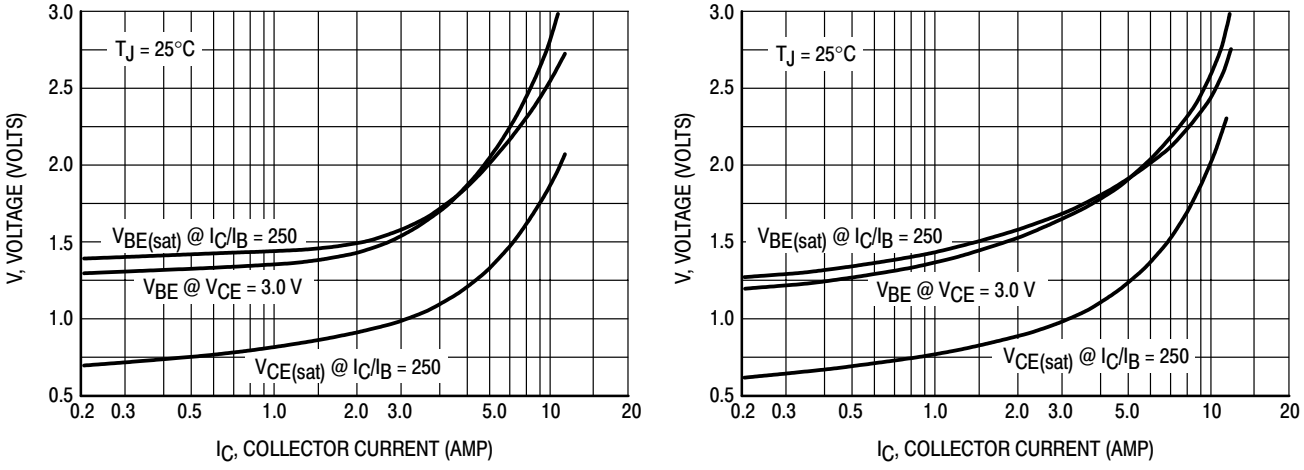


Figure 11. “On” Voltages

Complementary Silicon Plastic Power Transistors

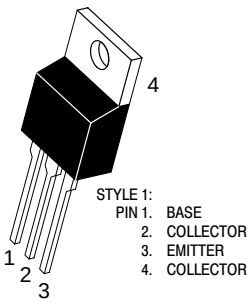
. . . designed for use in general−purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
  h_{FE} = 30−150 @ I_C
  = 3.0 Adc — 2N6111, 2N6288
  = 2.3 (Min) @ I_C = 7.0 Adc — All Devices
- Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) — 2N6111, 2N6288
  = 50 Vdc (Min) — 2N6109
  = 70 Vdc (Min) — 2N6107, 2N6292
- High Current Gain — Bandwidth Product
  f_T = 4.0 MHz (Min) @ I_C = 500 mAdc — 2N6288, 90, 92
  = 10 MHz (Min) @ I_C = 500 mAdc — 2N6107, 09, 11
- TO−220AB Compact Package

PNP
2N6107
2N6109*
2N6111
NPN
2N6288
2N6292*

***ON Semiconductor Preferred Device**

7 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
30−50−70 VOLTS
40 WATTS



CASE 221A−09
TO−220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector−Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector−Base Voltage	V_{CB}	40	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	7.0 10			Adc
Base Current	I_B	3.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

*Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 5
Publication Order Number:
2N6107/D

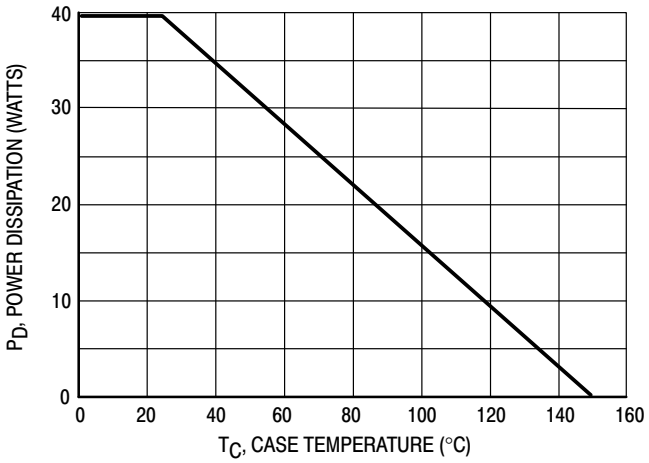


Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6111, 2N6288		30	—	
	2N6109		50	—	
	2N6107, 2N6292		70	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6111, 2N6288		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6109		—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6107, 2N6292		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6111, 2N6288		—	100	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6109		—	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6107, 2N6292		—	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6111, 2N6288		—	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6109		—	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6107, 2N6292		—	2.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N6107, 2N6292		30	150	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)	2N6109		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)	All Devices		2.3	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$	—	3.5	Vdc
(I_C = 7.0 Adc, I_B = 3.0 Adc)					
Base−Emitter On Voltage		$V_{BE(on)}$	—	3.0	Vdc
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)	2N6288, 92		4.0	—	
	2N6107, 09, 11		10	—	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	250	pF
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)		h_{fe}	20	—	—

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

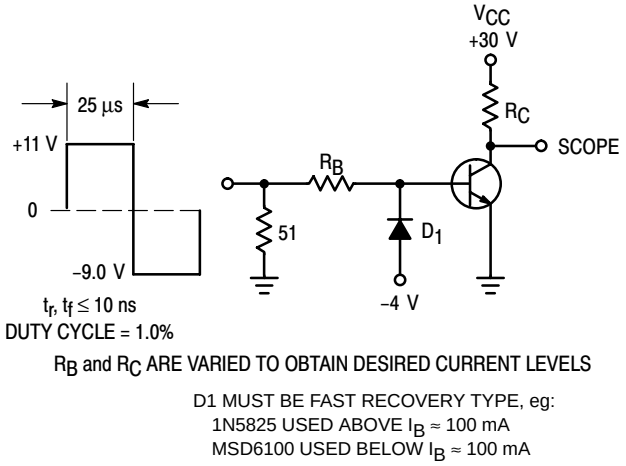


Figure 2. Switching Time Test Circuit

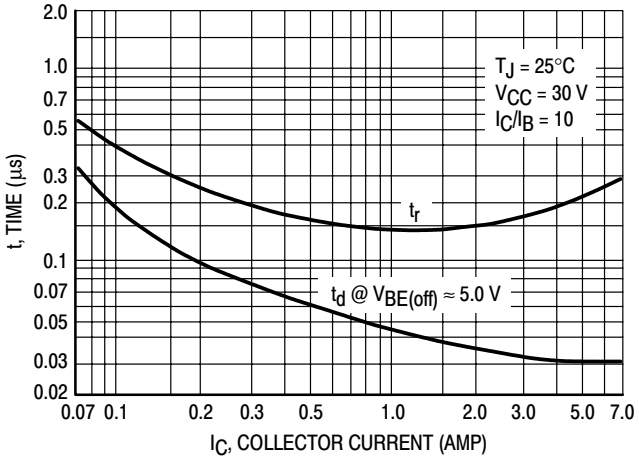


Figure 3. Turn−On Time

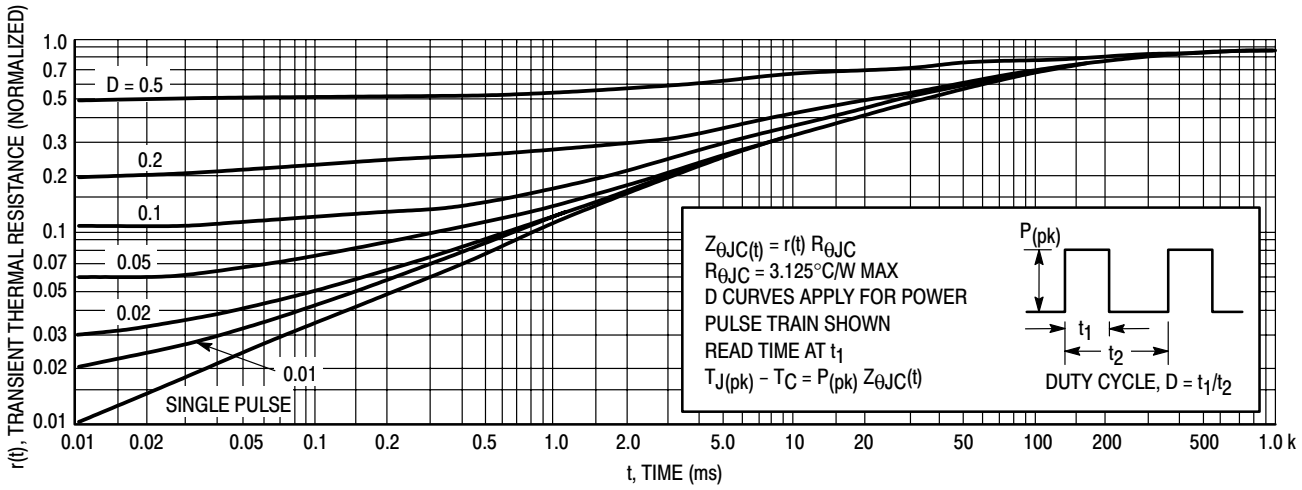


Figure 4. Thermal Response

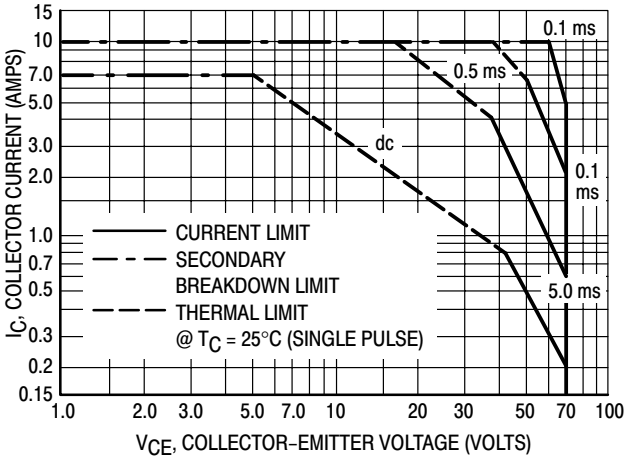


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

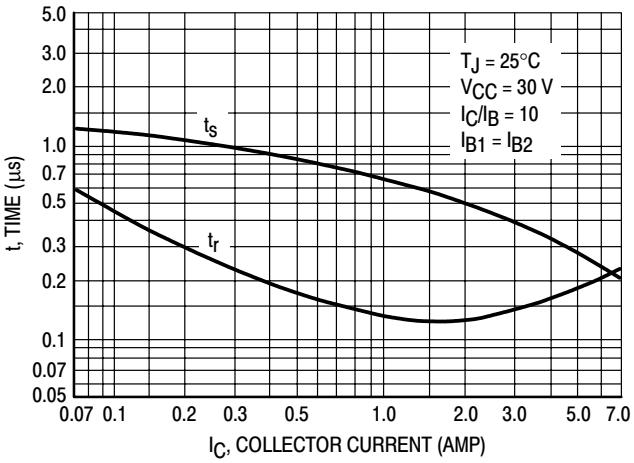


Figure 6. Turn−Off Time

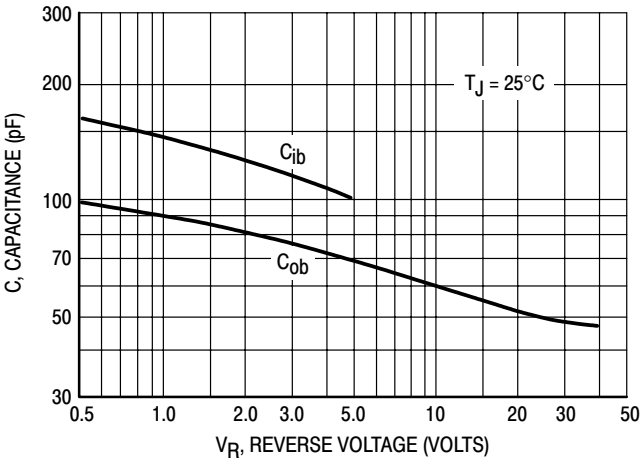


Figure 7. Capacitance

Darlington Complementary Silicon Power Transistors

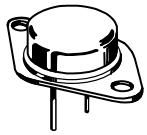
. . . designed for general−purpose amplifier and low−frequency switching applications.

- High DC Current Gain @ I_C = 10 Adc —
  h_{FE} = 2400 (Typ) — 2N6282, 2N6283, 2N6284
  = 4000 (Typ) — 2N6285, 2N6286, 2N6287
- Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6282, 2N6285
  = 80 Vdc (Min) — 2N6283, 2N6286
  = 100 Vdc (Min) — 2N6284, 2N6287
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors

NPN
2N6282
thru
2N6284*
PNP
2N6285
thru
2N6287*

***ON Semiconductor Preferred Device**

DARLINGTON
20 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 80, 100 VOLTS
160 WATTS



CASE 1−07
TO−204AA
(TO−3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +200			°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	°C/W

*Indicates JEDEC Registered Data.

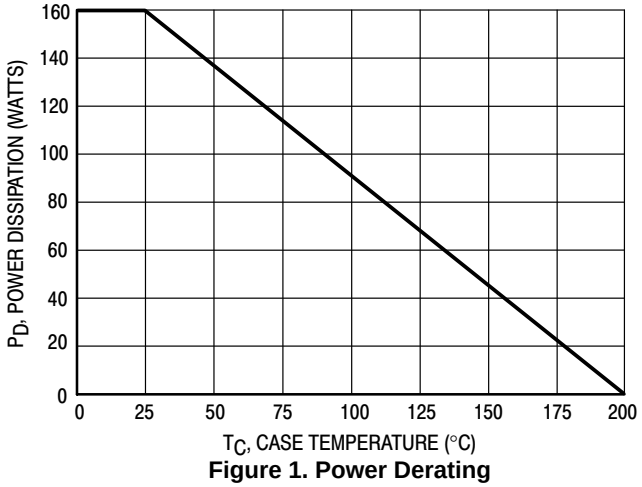


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 − Rev. 2
Publication Order Number:
2N6282/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	2N6282, 2N6285 2N6283, 2N6286 2N6284, 2N6287	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 2N6282, 2N6285 2N6283, 2N6286 2N6284, 2N6287	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 —	—
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base−Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small−Signal Short−Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 2N6282,83,84 2N6285,86,87	C_{ob}	 — —	 400 600	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

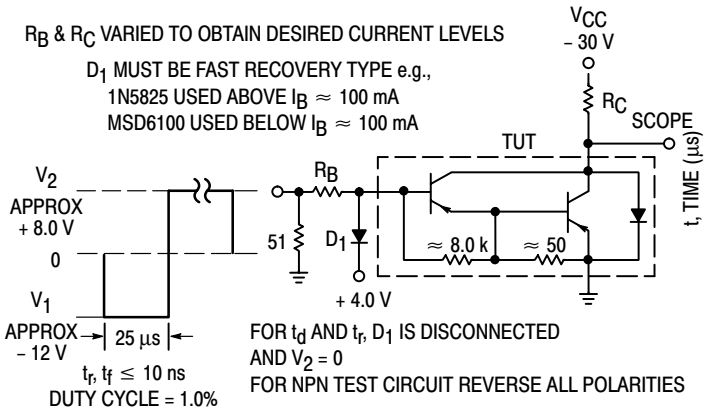


Figure 2. Switching Times Test Circuit

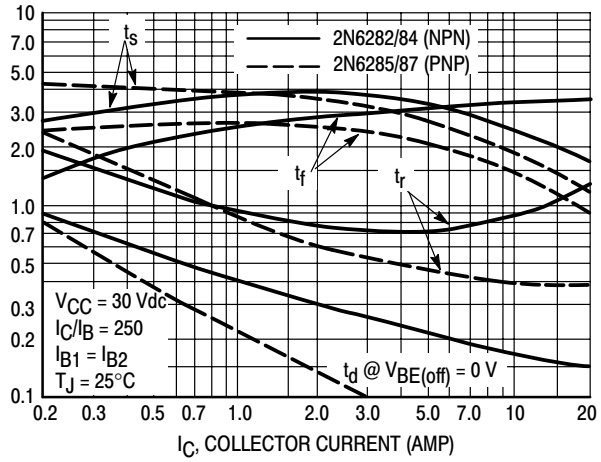


Figure 3. Switching Times

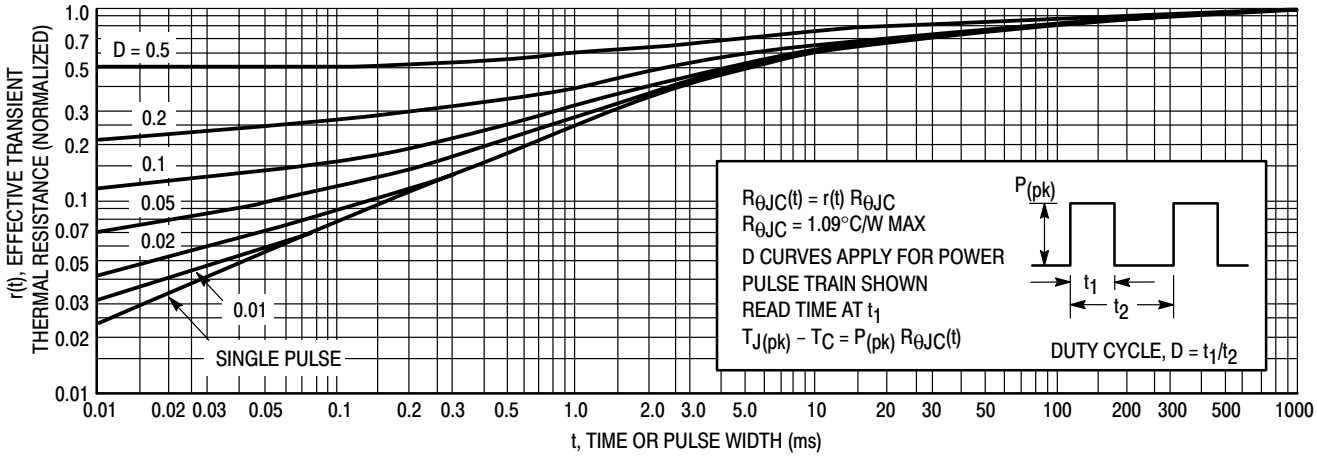


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

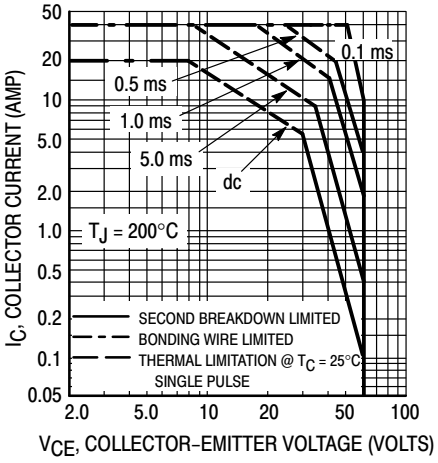


Figure 5. 2N6282, 2N6285

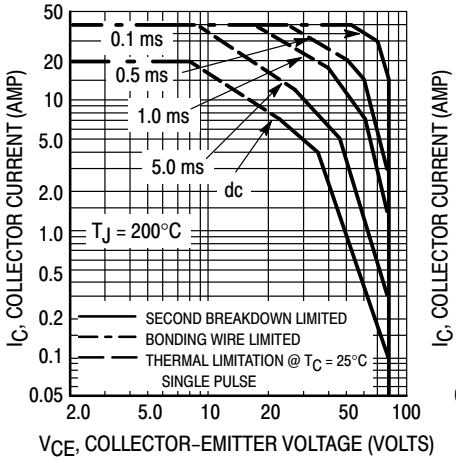


Figure 6. 2N6283, 2N6286

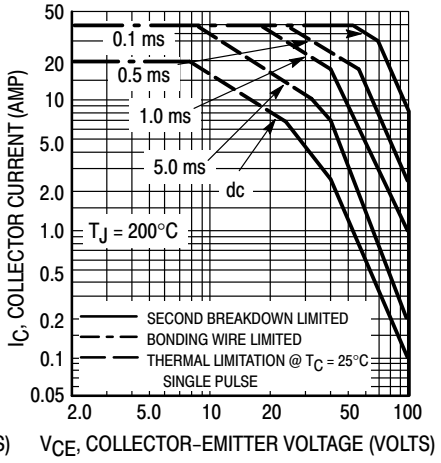


Figure 7. 2N6284, 2N6287

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6, and 7 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

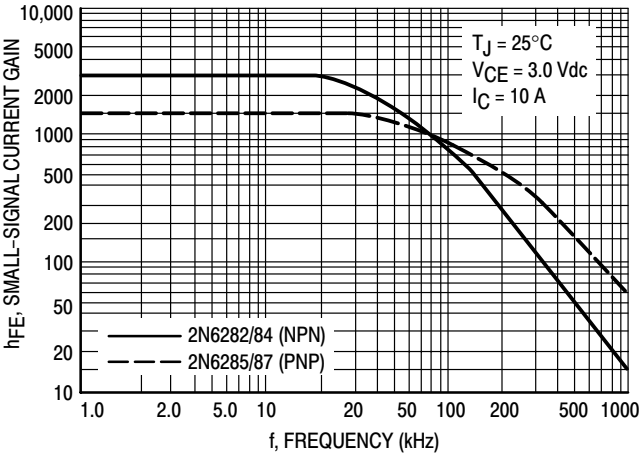


Figure 8. Small−Signal Current Gain

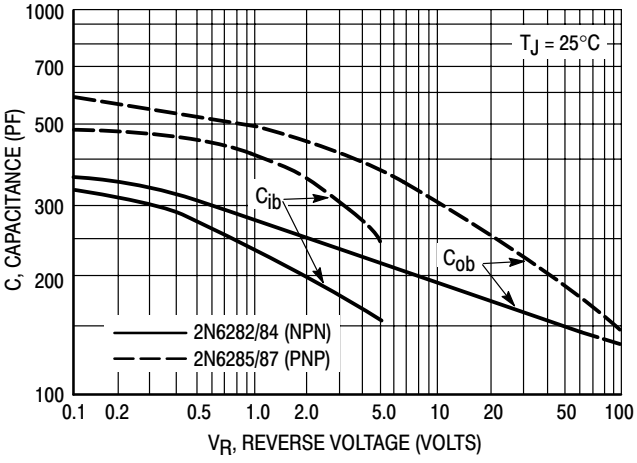


Figure 9. Capacitance

NPN
2N6282, 2N6283, 2N6284

PNP
2N6285, 2N6286, 2N6287

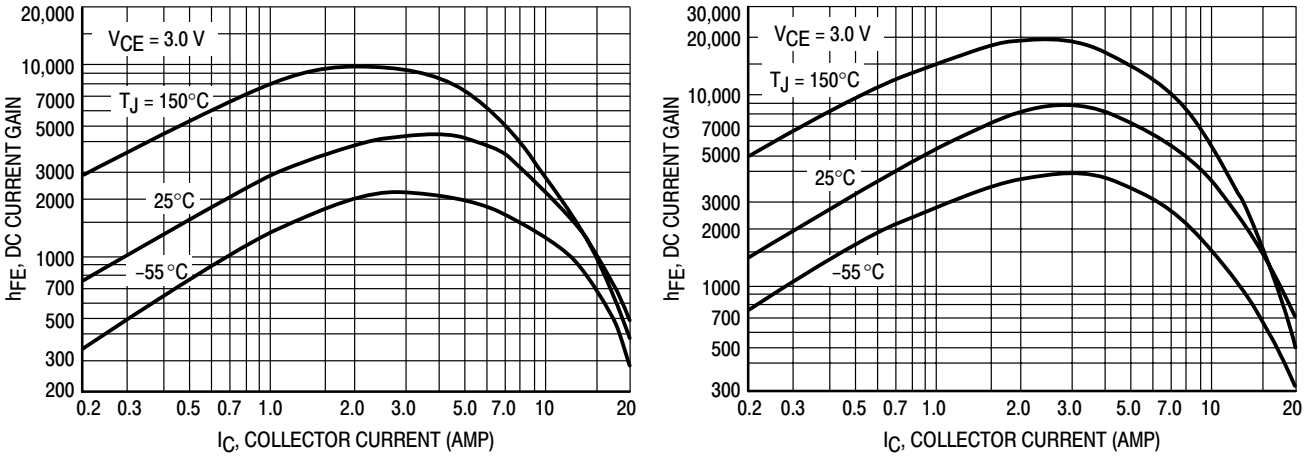


Figure 10. DC Current Gain

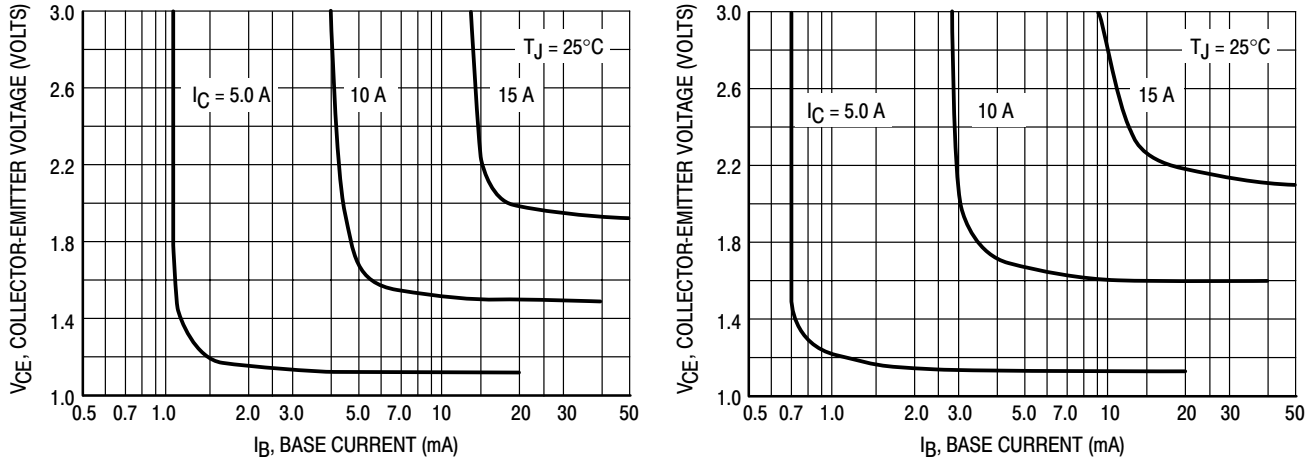


Figure 11. Collector Saturation Region

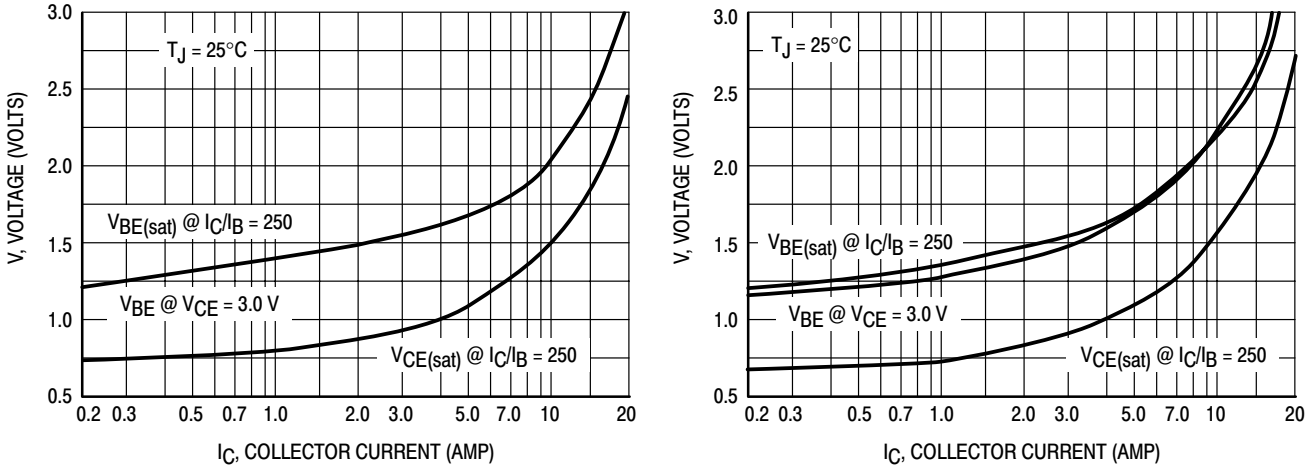
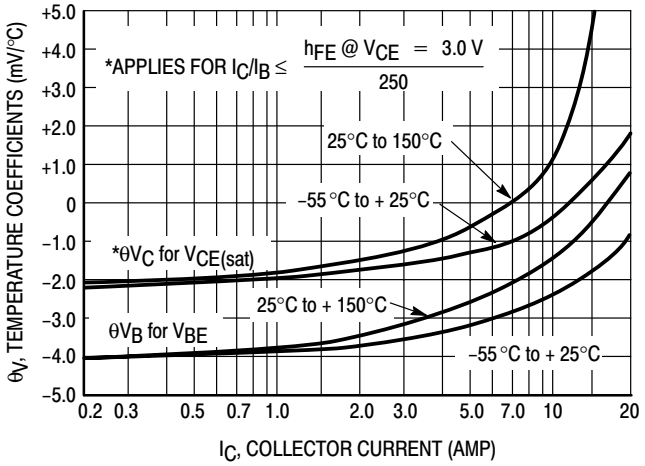


Figure 12. “On” Voltages

NPN
2N6282, 2N6283, 2N6284



PNP
2N6285, 2N6286, 2N6287

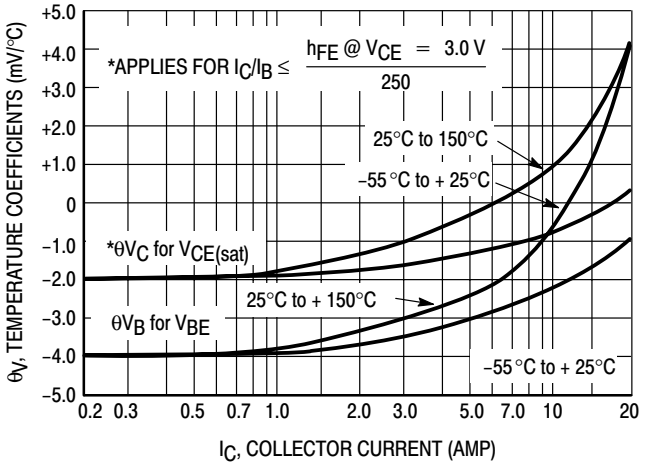
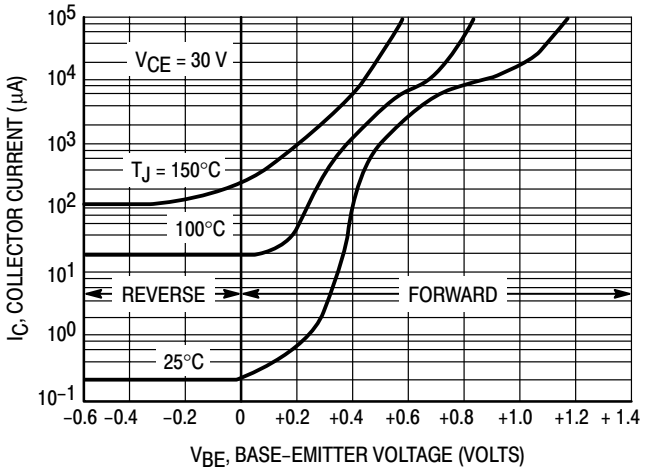


Figure 13. Temperature Coefficients



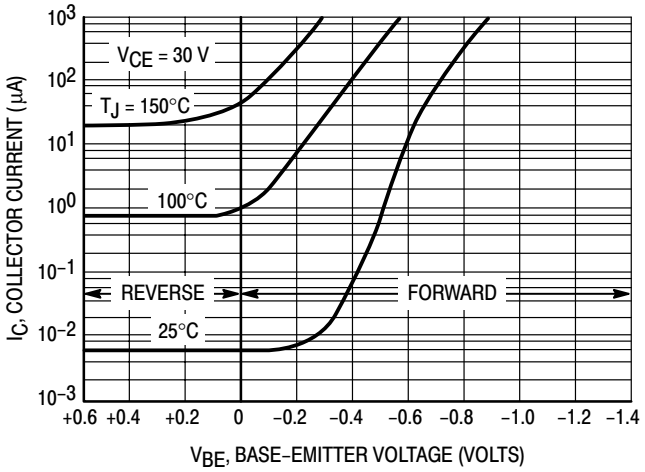


Figure 14. Collector Cut−Off Region

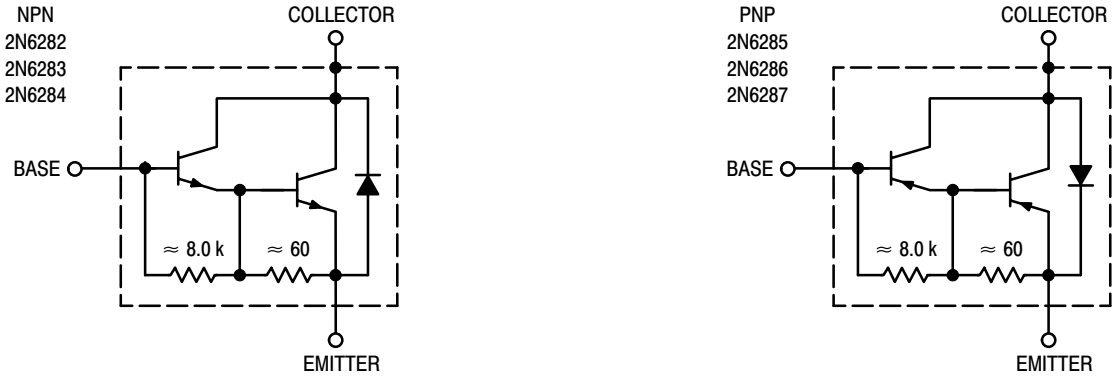


Figure 15. Darlington Schematic

High-Power NPN Silicon Transistors

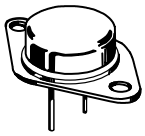
. . . designed for use in industrial−military power amplifier and switching circuit applications.

- High Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 100 Vdc (Min) − 2N6338
  = 150 Vdc (Min) − 2N6341
- High DC Current Gain −
  h_{FE} = 30 − 120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 ms (Max)
  t_s = 1.0 ms (Max)
  t_f = 0.25 ms (Max)

2N6338
2N6341*

*ON Semiconductor Preferred Device

25 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
200 WATTS



CASE 1−07
TO−204AA
(TO−3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6338	2N6341	Unit
Collector−Base Voltage	V_{CB}	120	180	Vdc
Collector−Emitter Voltage	V_{CEO}	100	150	Vdc
Emitter−Base Voltage	V_{EB}	6.0		Vdc
Collector Current Continuous Peak	I_C	 25 50		Adc
Base Current	I_B	10		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 200 1.14		 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

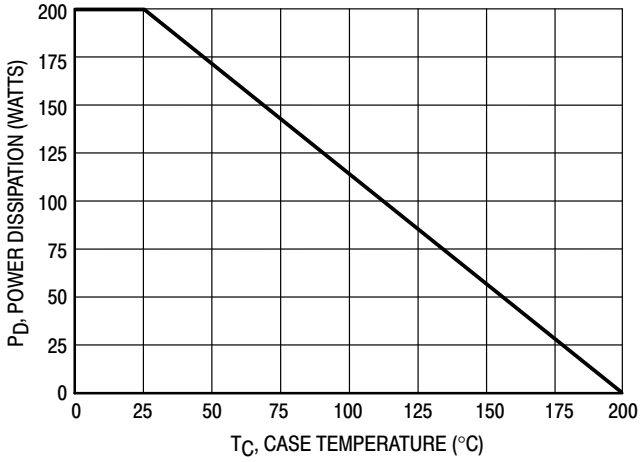


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 − Rev. 10
Publication Order Number:
2N6338/D

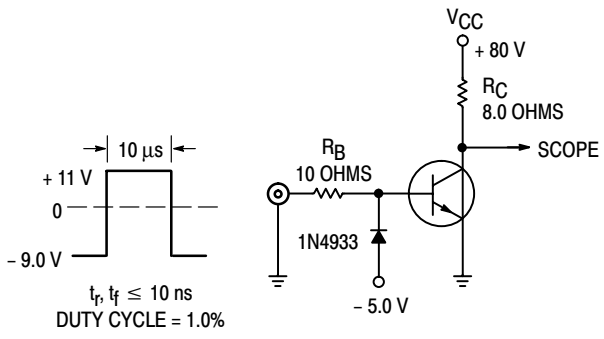
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6338 2N6341	$V_{CEO(sus)}$	100 150	− −	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 75 Vdc, I_B = 0)	 2N6338 2N6341	I_{CEO}	 − −	 50 50	µAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 − −	 10 1.0	 µAdc mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	−	10	µAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	−	100	µAdc
ON CHARACTERISTICS (1)					
DC Current Gain) (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 50 30 12	 − 120 −	−
Collector Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{CE(sat)}$	 − −	 1.0 1.8	Vdc
Base−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	 − −	 1.8 2.5	Vdc
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	−	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	−	300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r	−	0.3	µs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	−	1.0	µs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	−	0.25	µs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.



NOTE: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

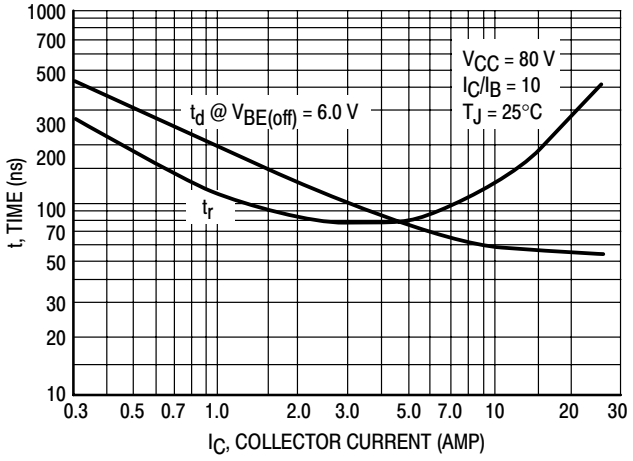


Figure 3. Turn−On Time

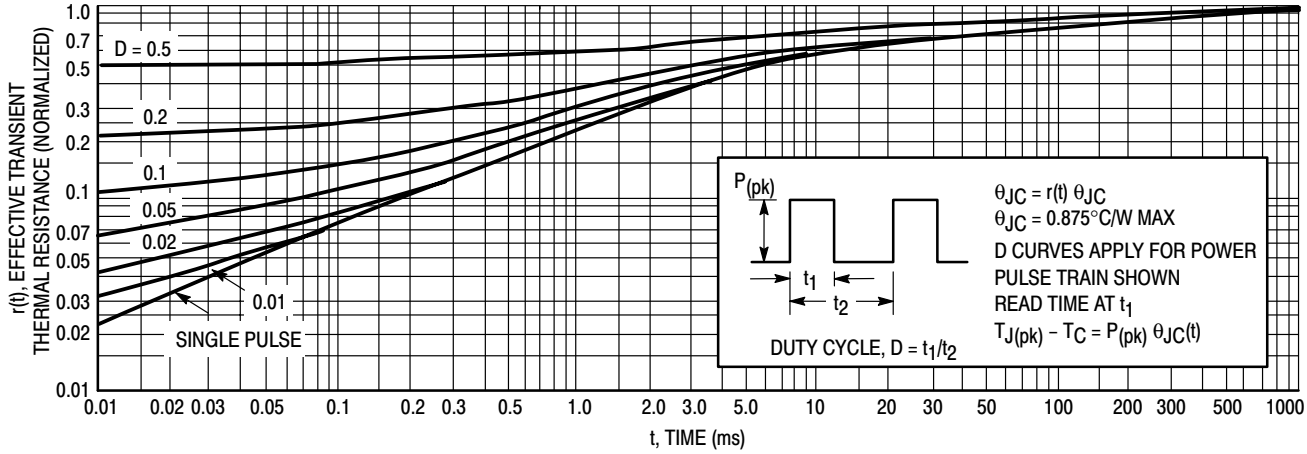


Figure 4. Thermal Response

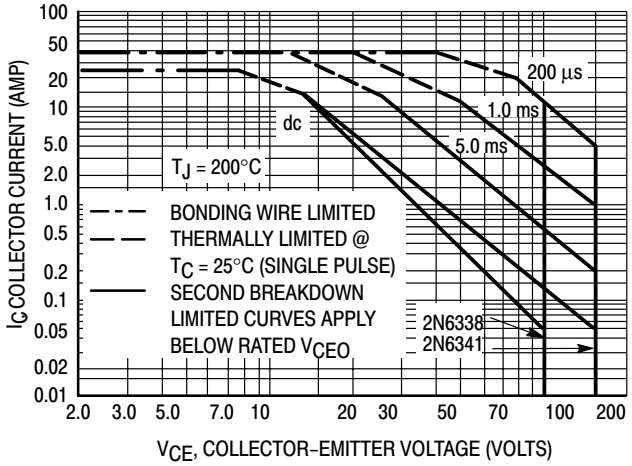


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

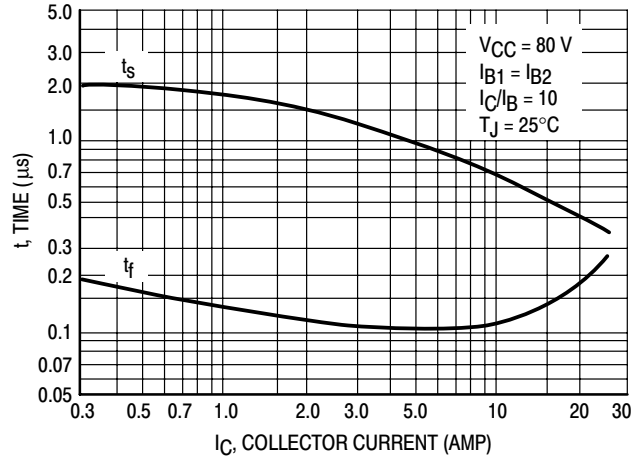


Figure 6. Turn−Off Time

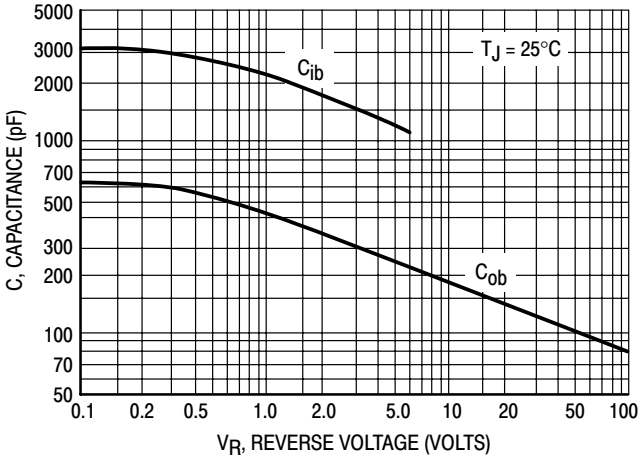


Figure 7. Capacitance

Plastic Medium-Power Silicon Transistors

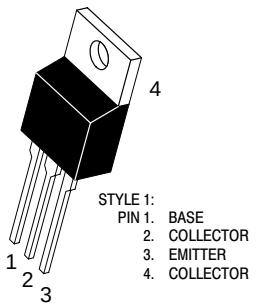
2N6387
2N6388*

*ON Semiconductor Preferred Device

. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6387
  = 80 Vdc (Min) — 2N6388
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 5.0 Adc — 2N6387, 2N6388
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package

DARLINGTON
8 AND 10 AMPERE
NPN SILICON
POWER TRANSISTORS
60−80 VOLTS
65 WATTS



CASE 221A−09
TO−220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6387	2N6388	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15	10 15	Adc
Base Current	I_B	250		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52		 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016		 Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

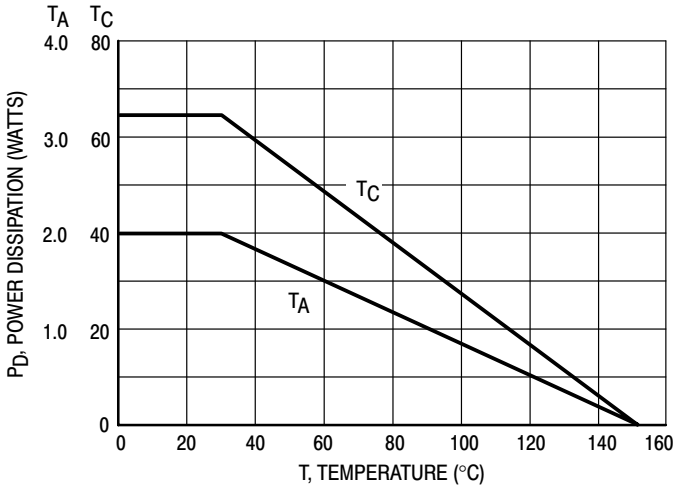


Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6387		60	—	
	2N6388		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N6387		—	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6388		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6387		—	300	
(V_{CE} − 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6388		—	300	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6387		—	3.0	mAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6388		—	3.0	
Emitter Cutoff Current		I_{EBO}	—	5.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		1000	20,000	
(I_C = 1 0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		100	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6387, 2N6388		—	2.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6387, 2N6388		—	3.0	
Base−Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	2.8	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	4.5	
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain		$\|h_{fe}\|$	20	—	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	—	200	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)					
Small−Signal Current Gain		h_{fe}	1000	—	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

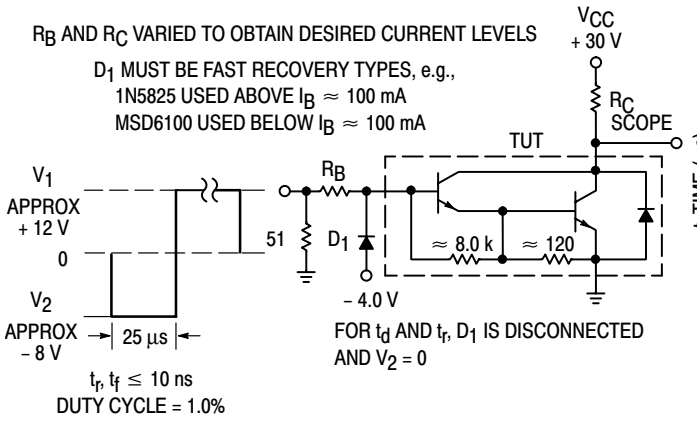


Figure 2. Switching Times Test Circuit

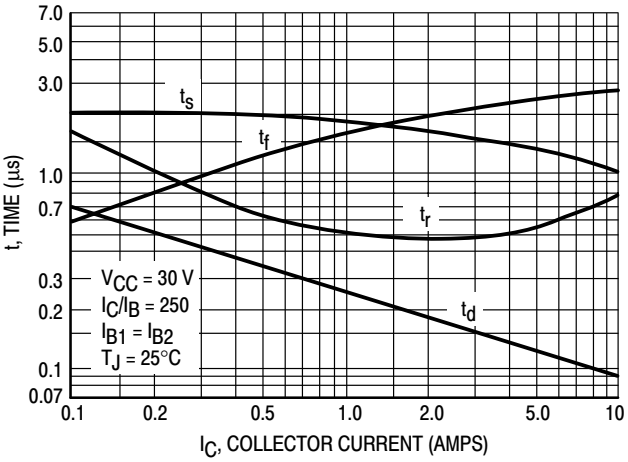


Figure 3. Switching Times

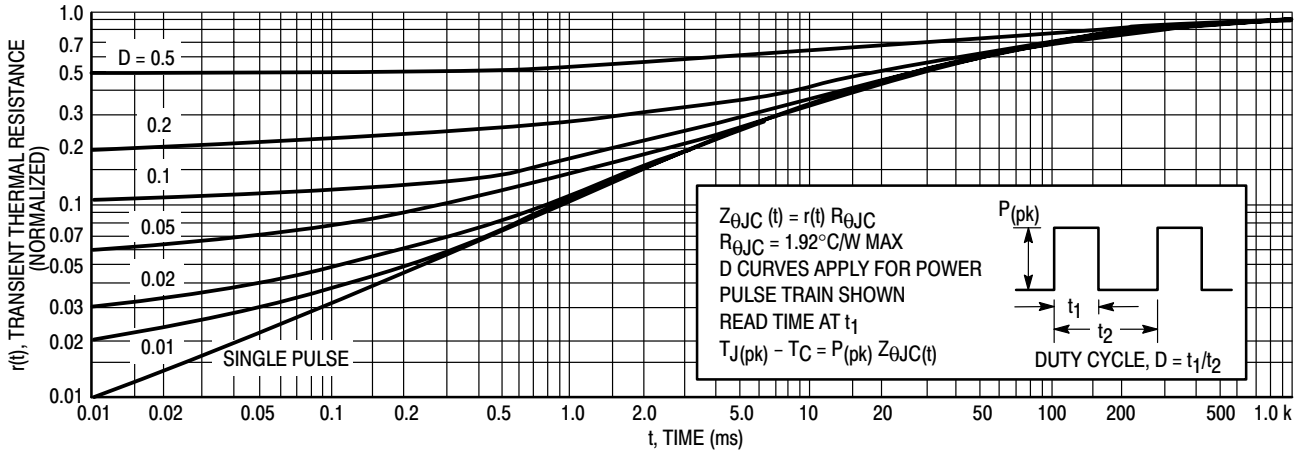


Figure 4. Thermal Response

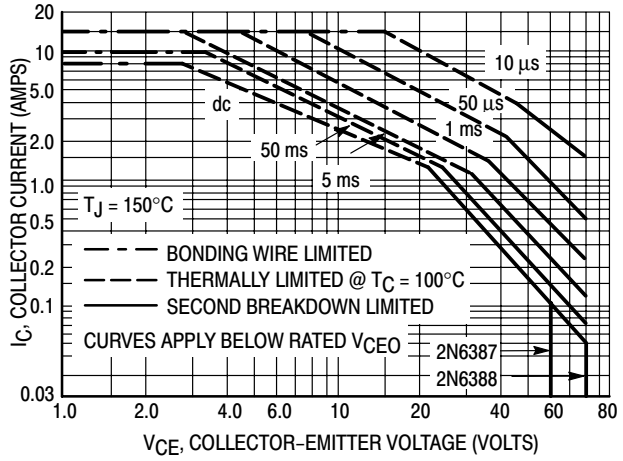


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

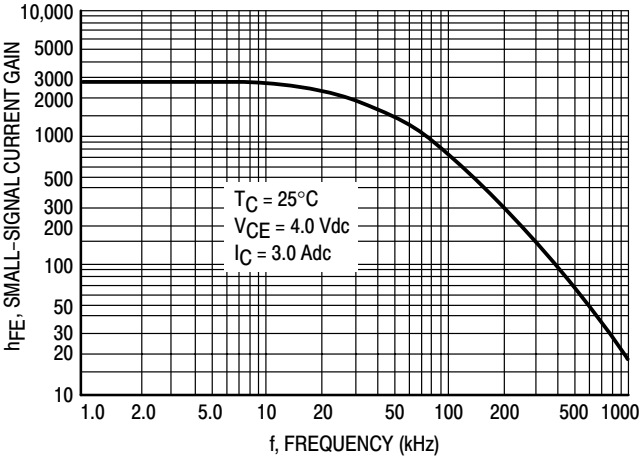


Figure 6. Small−Signal Current Gain

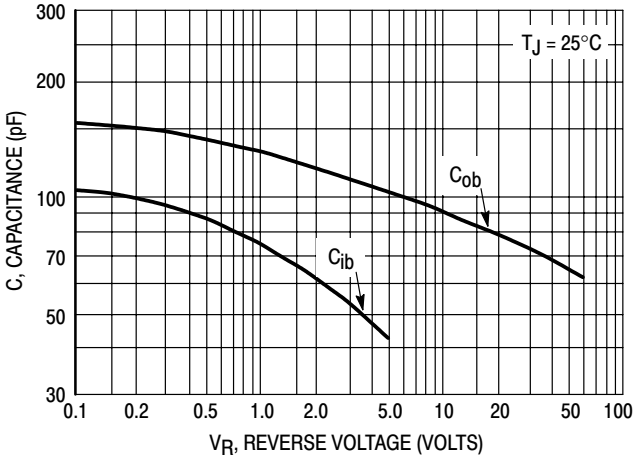


Figure 7. Capacitance

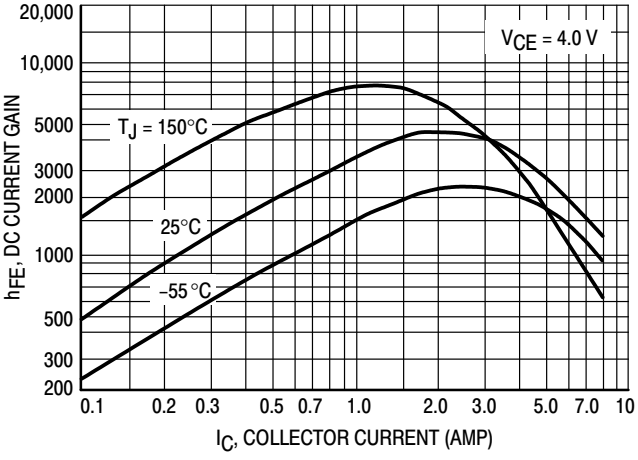


Figure 8. DC Current Gain

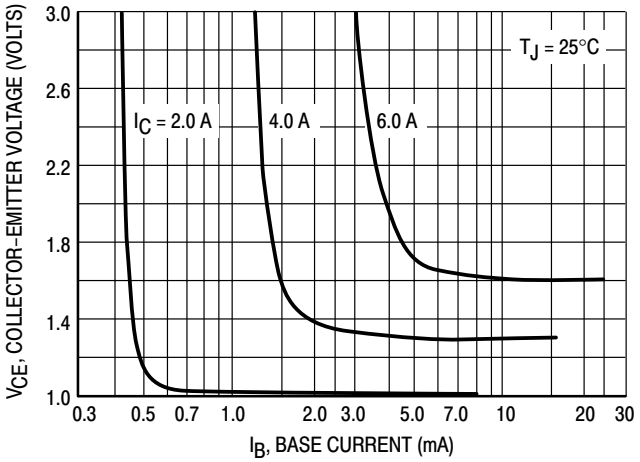


Figure 9. Collector Saturation Region

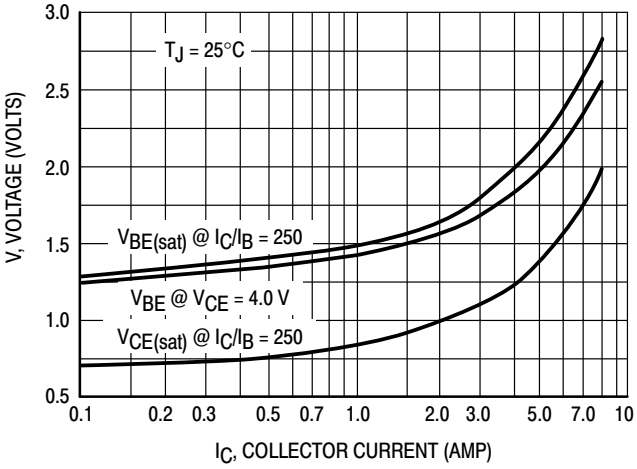


Figure 10. “On” Voltages

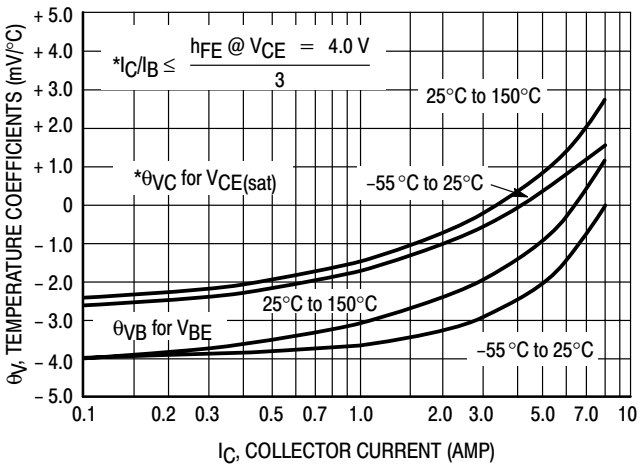


Figure 11. Temperature Coefficients

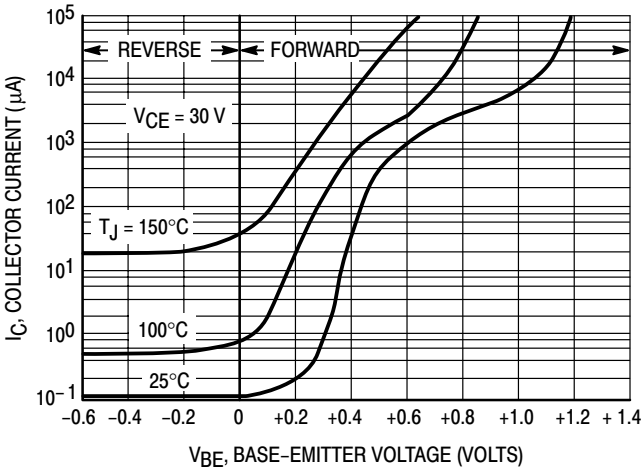


Figure 12. Collector Cut−Off Region

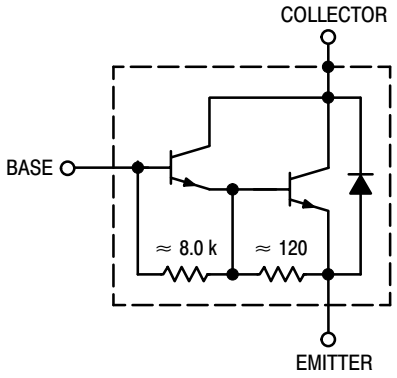


Figure 13. Darlington Schematic

Complementary Silicon Plastic Power Transistors

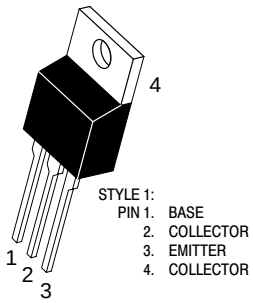
. . . designed for use in general−purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes —
  h_{FE} = 20−150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) − 2N6487, 2N6490
  = 80 Vdc (Min) − 2N6488, 2N6491
- High Current Gain — Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO−220AB Compact Package

NPN
2N6487
2N6488*
PNP
2N6490
2N6491*

***ON Semiconductor Preferred Device**

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60−80 VOLTS
75 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6487 2N6490	2N6488 2N6491	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	70	90	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	5.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.8 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

(1) Indicates JEDEC Registered Data.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 10
Publication Order Number:
2N6487/D

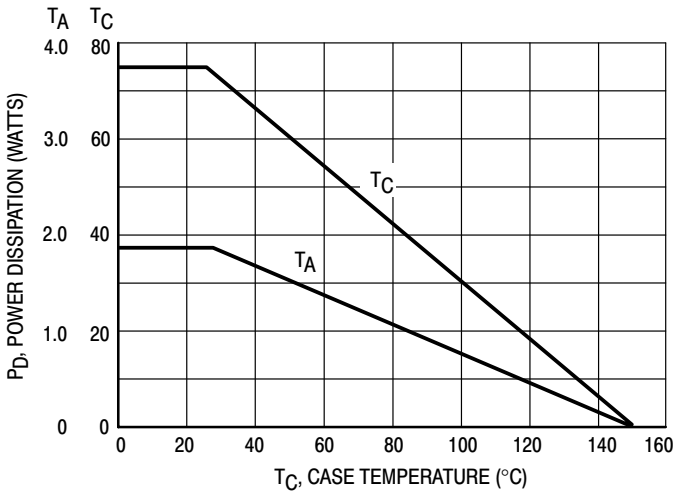


Figure 1. Power Derating

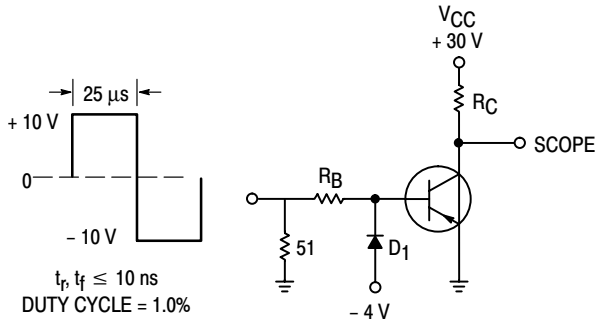
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6487, 2N6490		60	—	
	2N6488, 2N6491		80		
Collector−Emitter Sustaining Voltage (1)		VCEX			Vdc
(I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	2N6487, 2N6490		70	—	
	2N6488, 2N6491		90	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6487, 2N6490		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6488, 2N6491		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6487, 2N6490		—	500	
(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6488, 2N6491		—	500	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6487, 2N6490		—	5.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6488, 2N6491		—	5.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			20	150	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			5.0	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			—	1.3	
(I_C = 15 Adc, I_B = 5.0 Adc)			—	3.5	
Base−Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			—	1.3	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			—	3.5	
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (2)		f_T	5.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)					
Small−Signal Current Gain		h_{fe}	25	—	—
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.
FOR PNP, REVERSE ALL POLARITIES.

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Figure 2. Switching Time Test Circuit

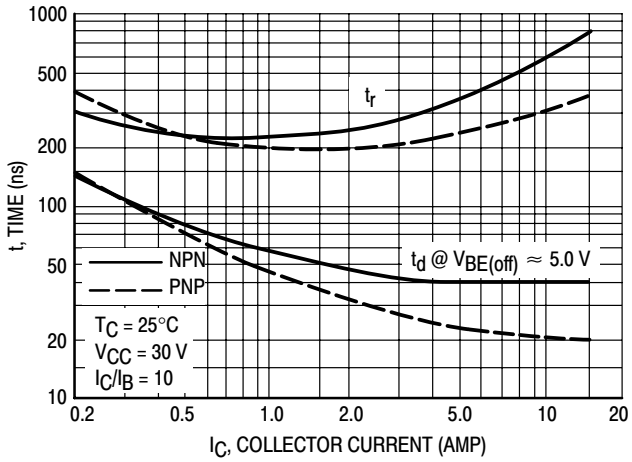


Figure 3. Turn−On Time

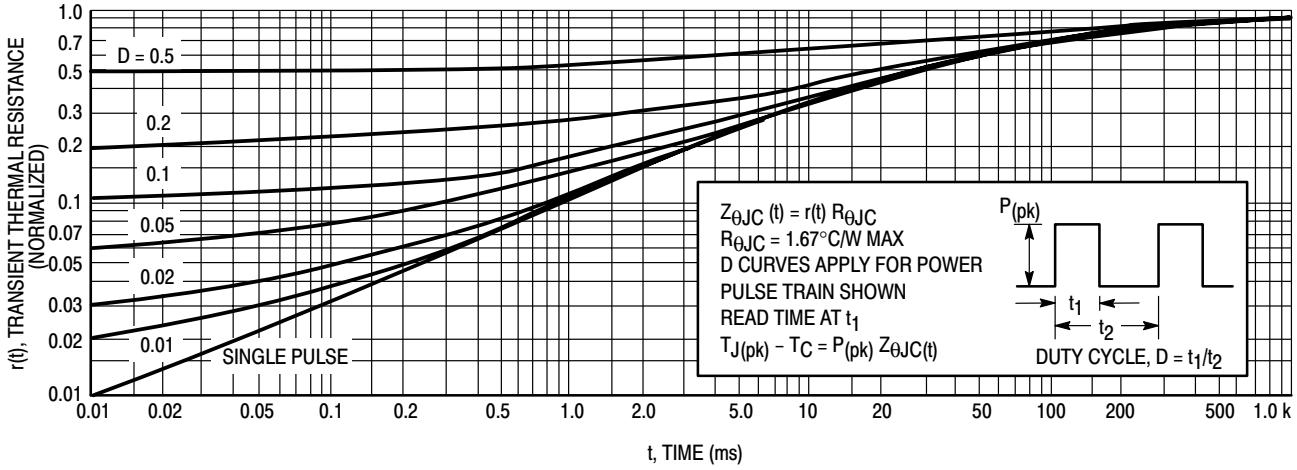


Figure 4. Thermal Response

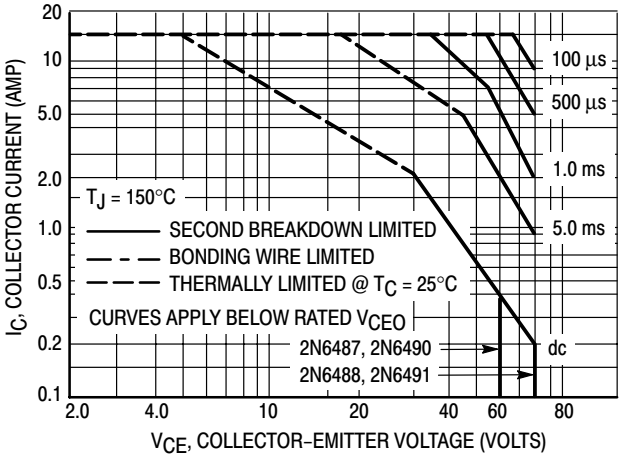


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

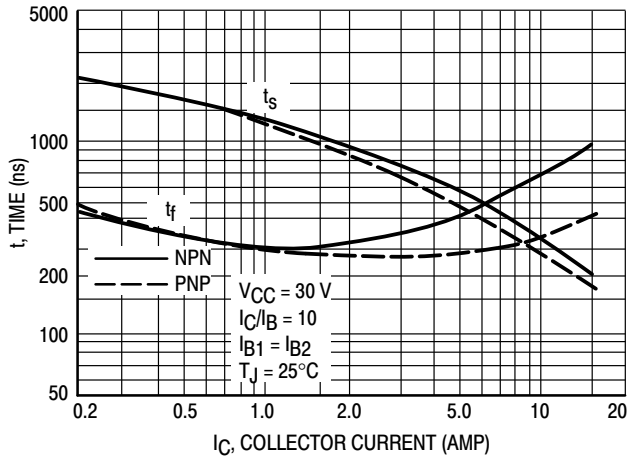


Figure 6. Turn−Off Time

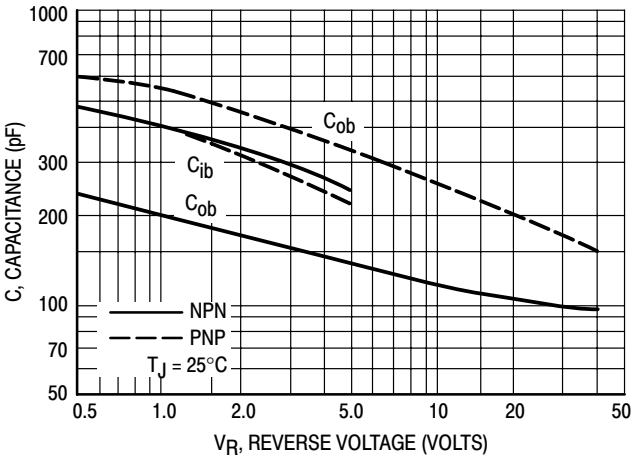
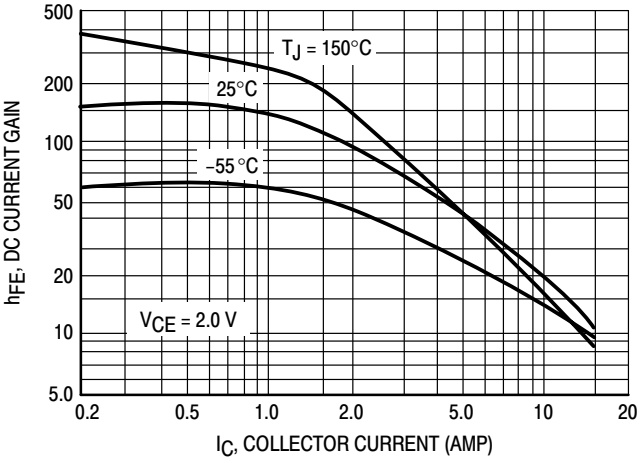


Figure 7. Capacitances

NPN
2N6487, 2N6488



PNP
2N6490, 2N6491

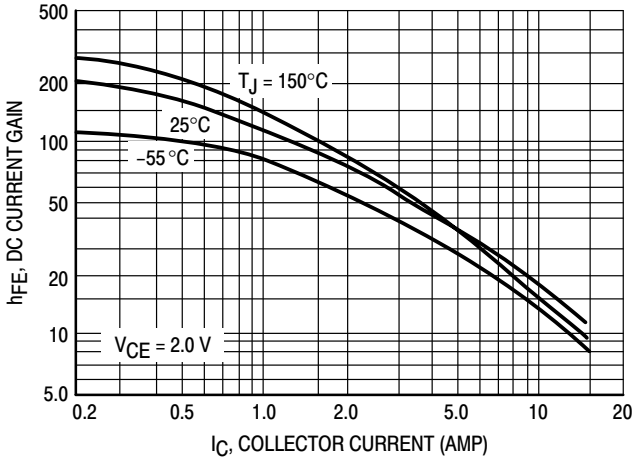
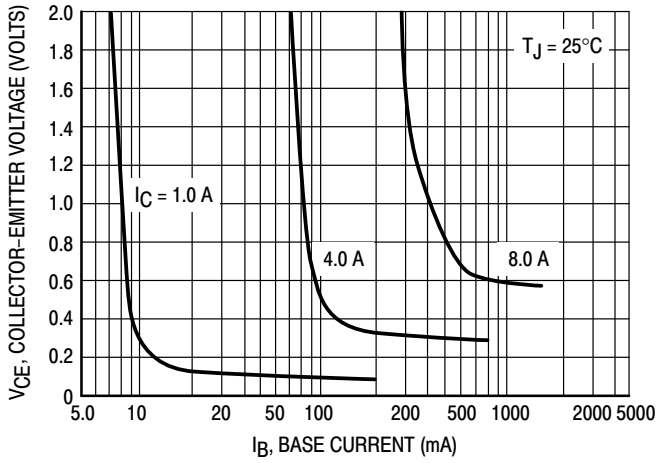


Figure 8. DC Current Gain



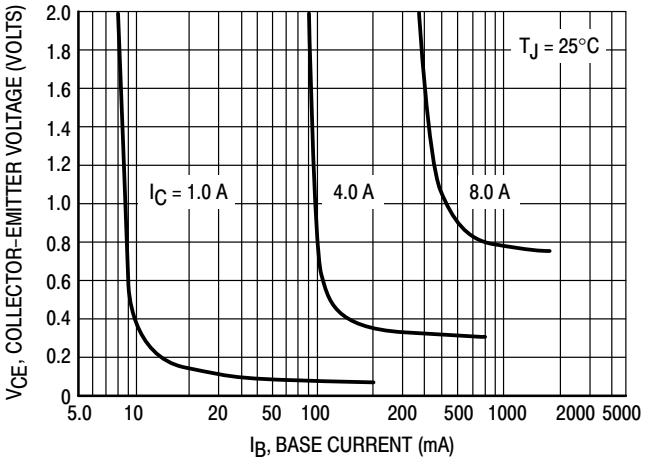
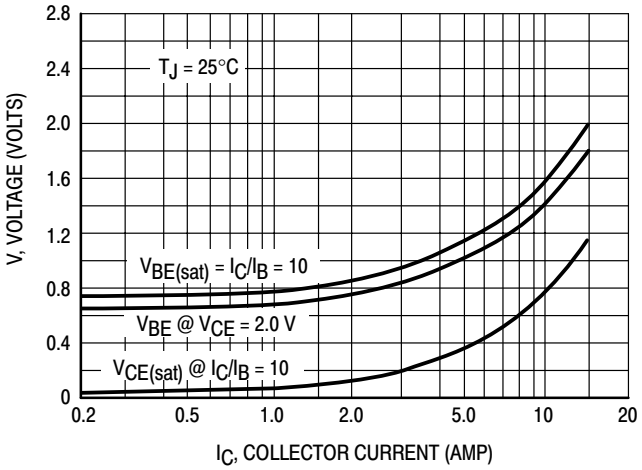


Figure 9. Collector Saturation Region



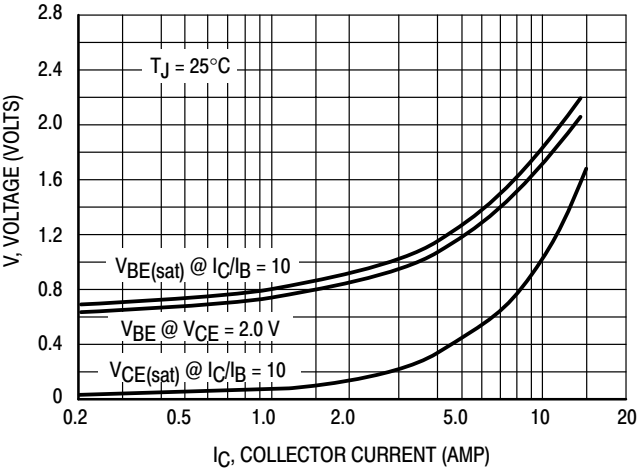


Figure 10. “On” Voltages

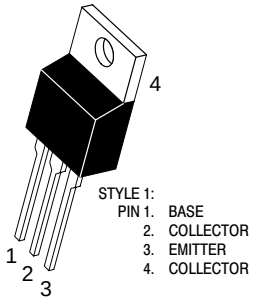
High Voltage NPN Silicon Power Transistors

2N6497

. . . designed for high voltage inverters, switching regulators and line−operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 250 Vdc (Min)
- Excellent DC Current Gain
  h_{FE} = 10−75 @ I_C = 2.5 Adc
- Low Collector−Emitter Saturation Voltage @ I_C = 2.5 Adc −
  $V_{CE(sat)}$ = 1.0 Vdc (Max)

5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 VOLT
80 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CB}	350	Vdc
Emitter−Base Voltage	V_{EB}	6.0	Vdc
Collector Current − Continuous − Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

(1) Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 25 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current (V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEX}	– –	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 10 Vdc) (I_C = 5.0 Adc, V_{CE} = 10 Vdc)	h_{FE}	10 3.0	– –	75 –	–
Collector−Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) (I_C = 5.0 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	– –	– –	1.0 5.0	Vdc
Base−Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) (I_C = 5.0 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	– –	– –	1.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	5.0	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)	t_r	–	0.4	1.0	μs
Storage Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)	t_s	–	1.4	2.5	μs
Fall Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	t_f	–	0.45	1.0	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

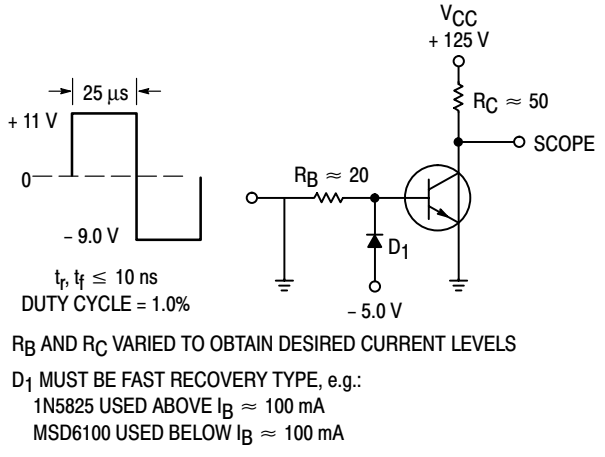


Figure 11. Switching Time Test Circuit

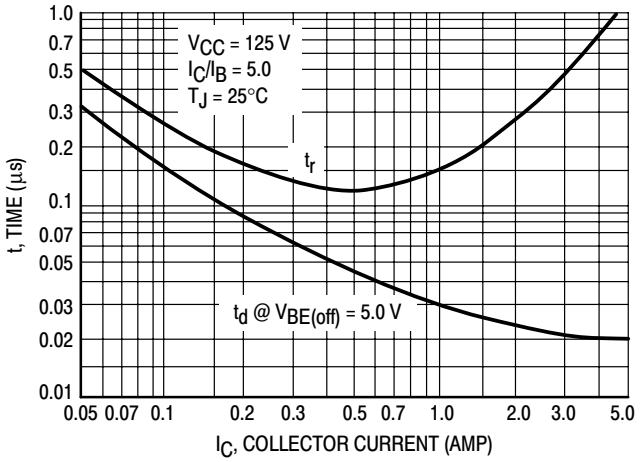


Figure 12. Turn−On Time

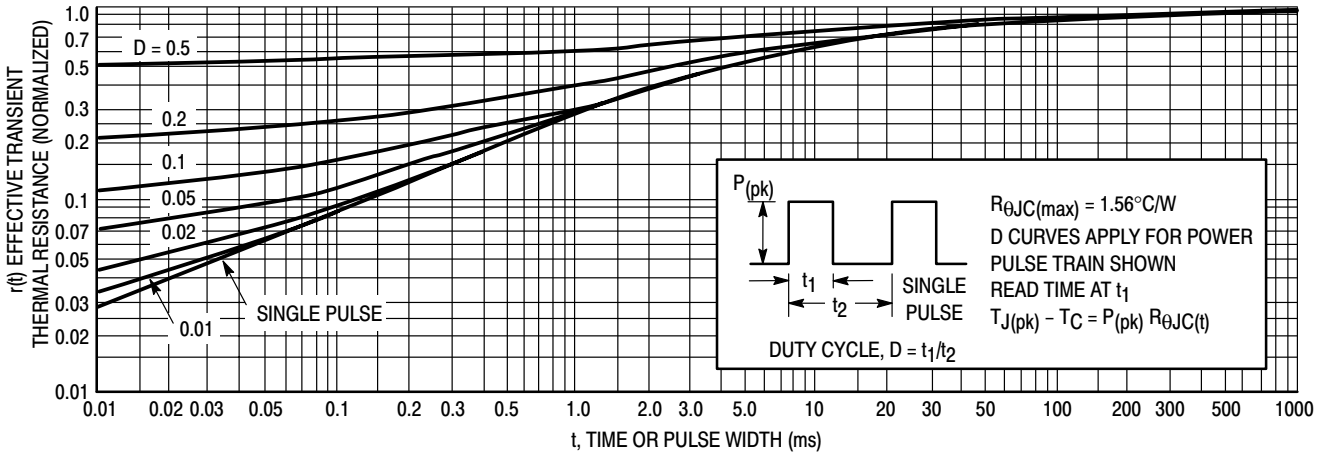


Figure 13. Thermal Response

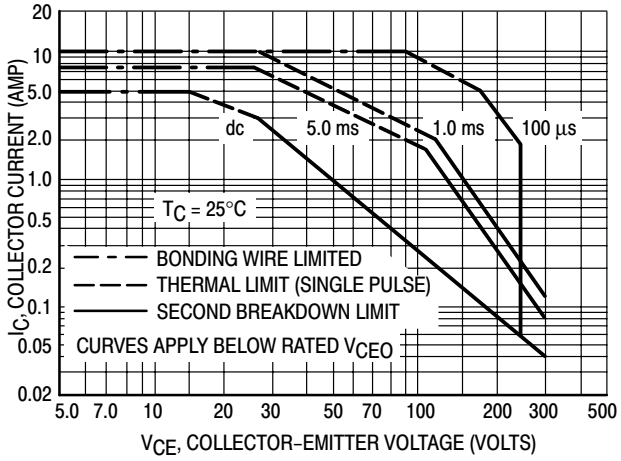


Figure 14. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

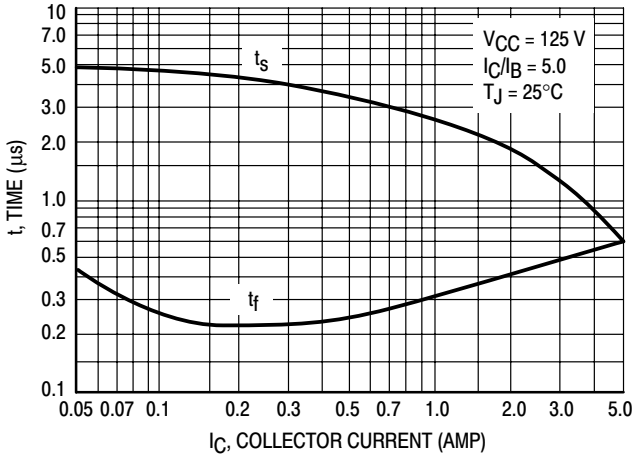


Figure 15. Turn−Off Time

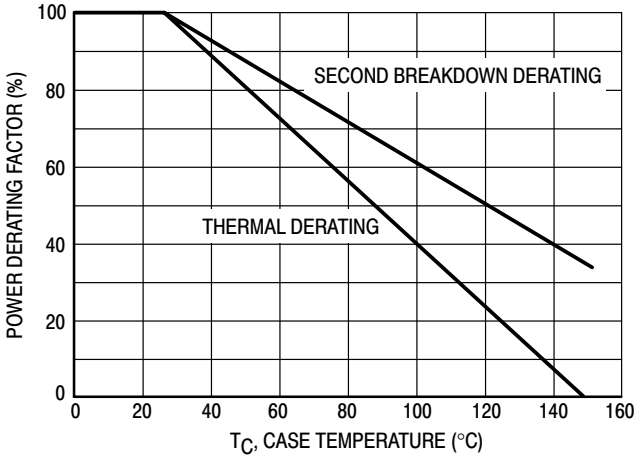


Figure 16. Power Derating

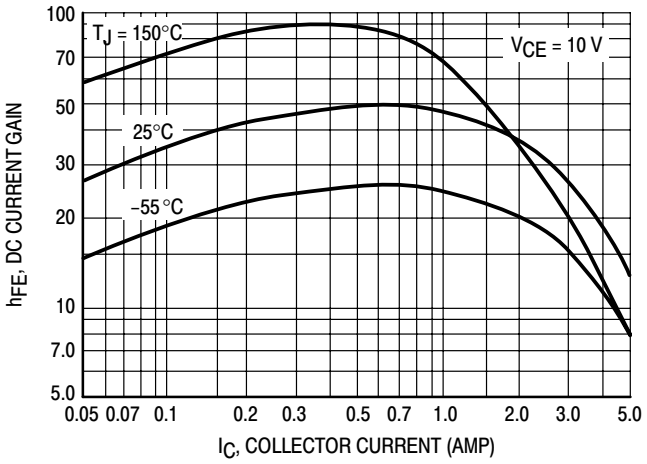


Figure 17. DC Current Gain

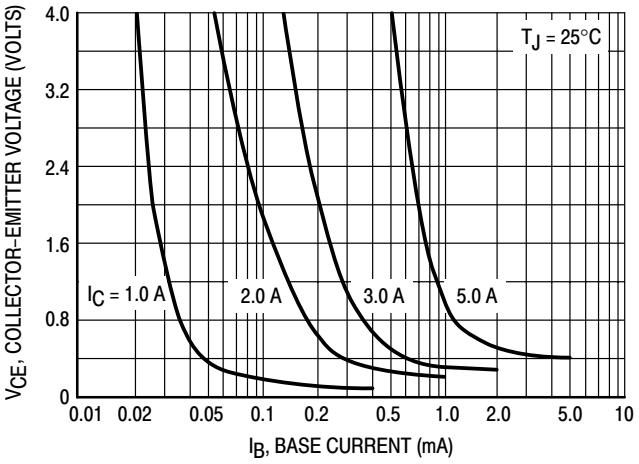


Figure 18. Collector Saturation Region

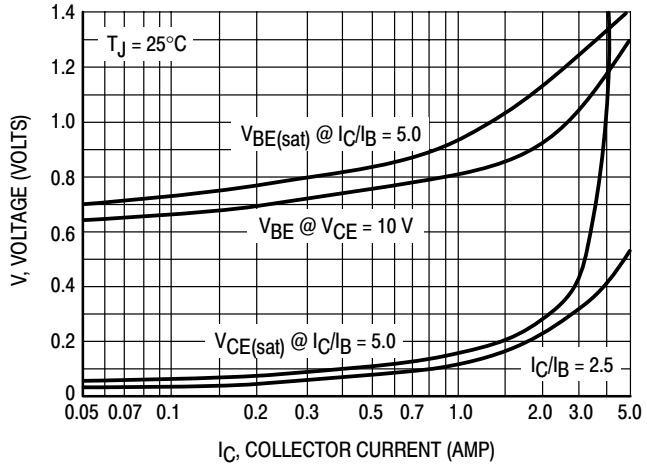


Figure 19. “On” Voltages

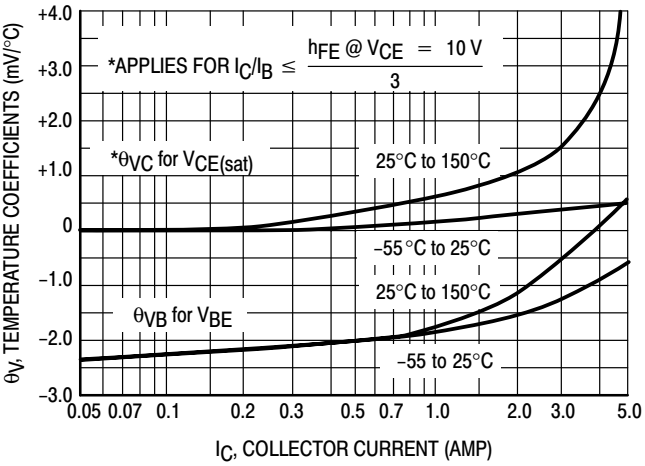


Figure 20. Temperature Coefficients

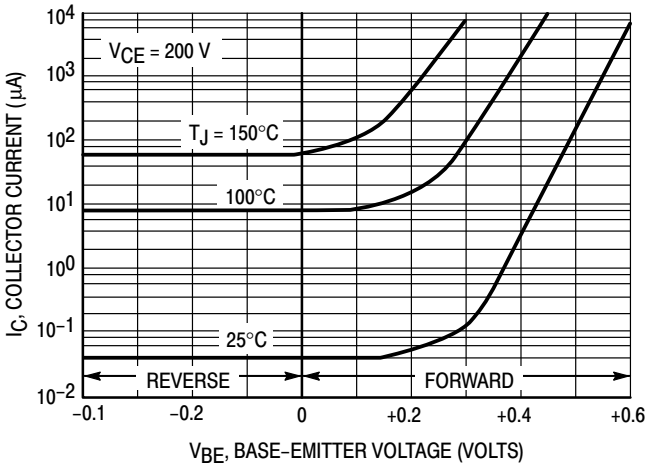


Figure 21. Collector Cutoff Region

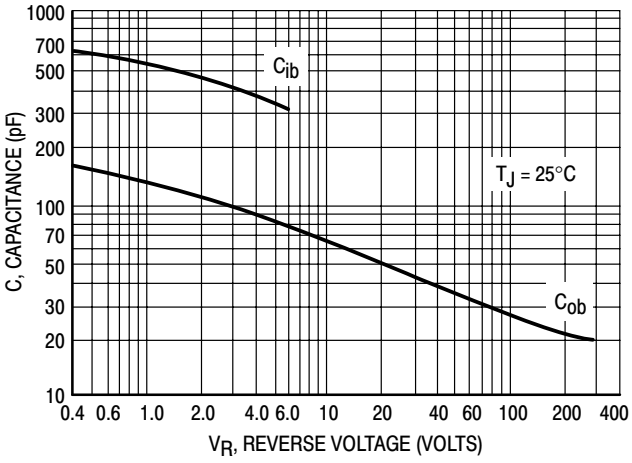


Figure 22. Capacitance

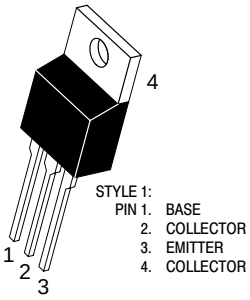
Darlington Silicon Power Transistors

2N6667
2N6668

PNP SILICON
DARLINGTON
POWER TRANSISTORS
10 AMPERES
60−80 VOLTS
65 WATTS

. . . designed for general−purpose amplifier and low speed switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 4 Adc
- Collector−Emitter Sustaining Voltage — @ 200 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6667
  = 80 Vdc (Min) — 2N6668
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2 Vdc (Max)@ I_C = 5 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package
- Complementary to 2N6387, 2N6388



CASE 221A−09
TO−220AB

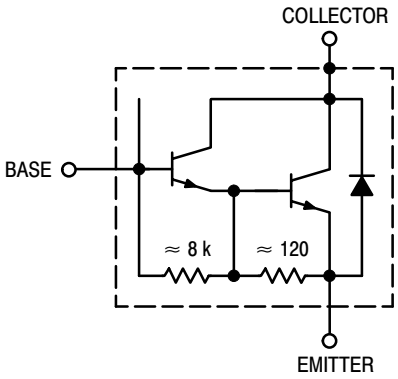


Figure 1. Darlington Schematic

MAXIMUM RATINGS (1)

Rating	Symbol	2N6667	2N6668	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous — Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52		watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

(1) Indicates JEDEC Registered Data.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)	2N6667 2N6668	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N6667 2N6668	I_{CEO}	— —	1 1	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6667 2N6668 2N6667 2N6668	I_{CEX}	 — — — —	 300 300 3 3	 μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 3 Vdc) (I_C = 10 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 100	20000 —	—
Collector−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	— —	2 3	Vdc
Base−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	— —	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	200	pF
Small−Signal Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc, f = 1 kHz)		h_{fe}	1000	—	—

*Indicates JEDEC Registered Data

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1, MUST BE FAST RECOVERY TYPES e.g.,
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FOR t_d AND t_r, D_1 IS DISCONNECTED AND V_2 = 0

t_r, $t_f \leq$ 10 ns
DUTY CYCLE = 1.0%

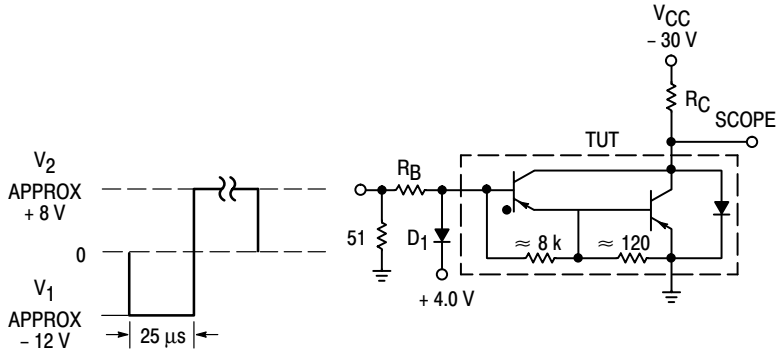


Figure 2. Switching Times Test Circuit

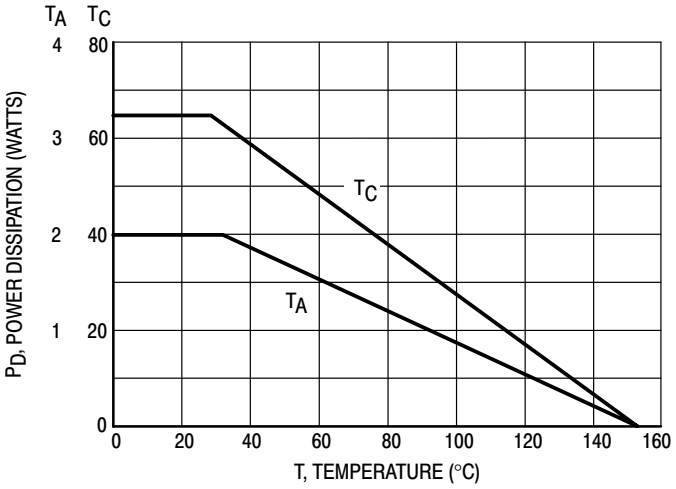


Figure 3. Power Derating

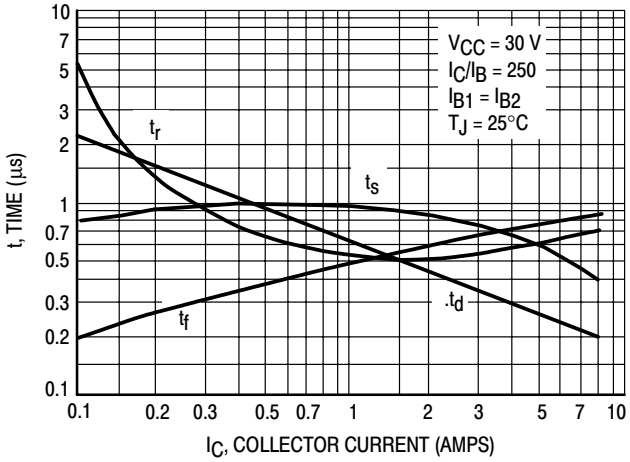


Figure 4. Typical Switching Times

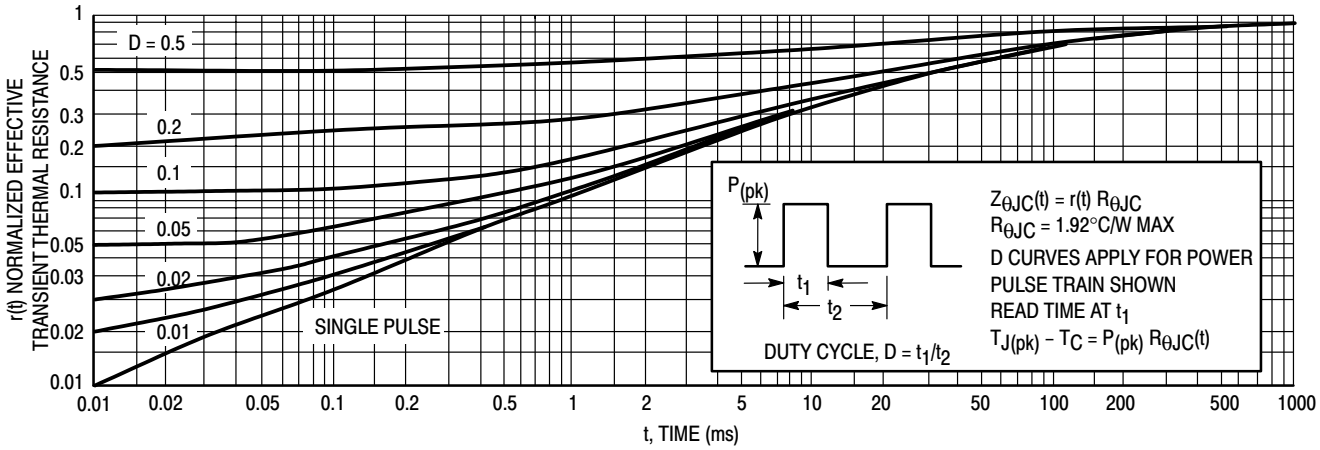


Figure 5. Thermal Response

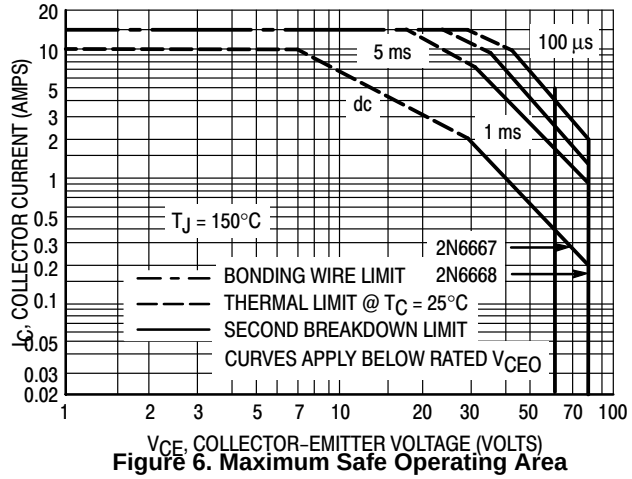


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

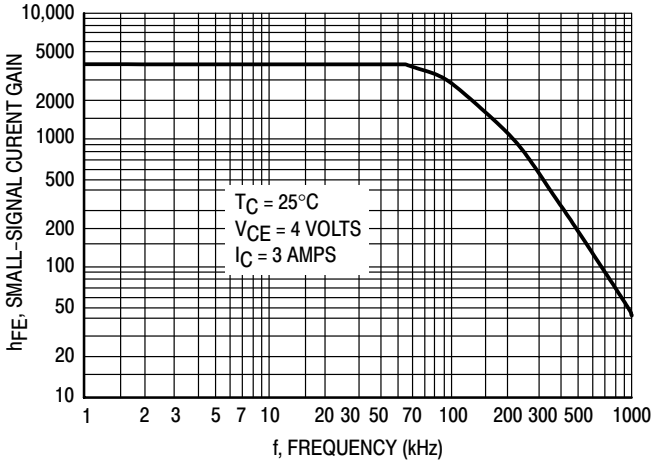


Figure 7. Typical Small−Signal Current Gain

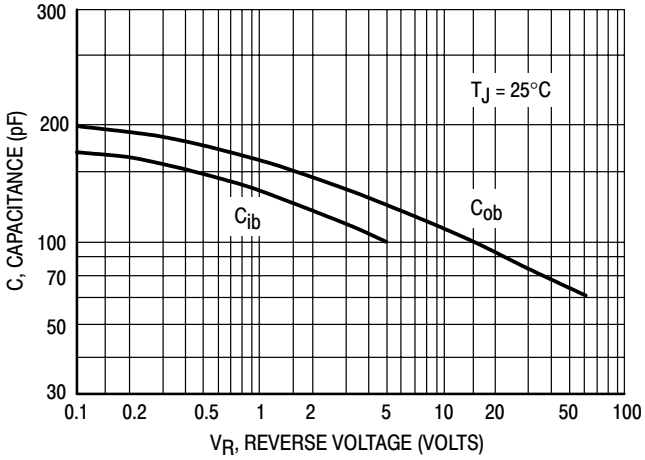


Figure 8. Typical Capacitance

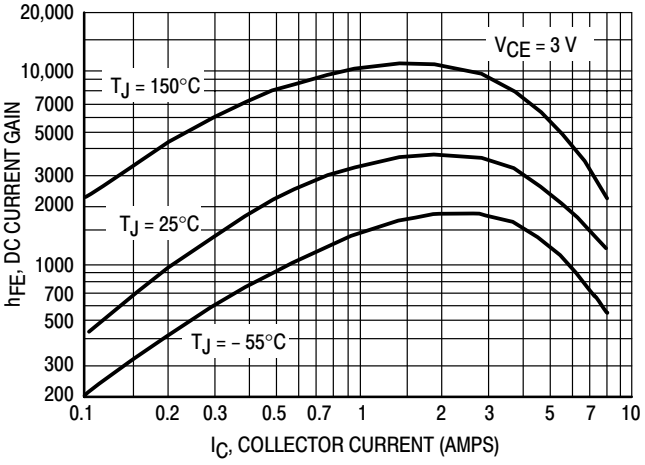


Figure 9. Typical DC Current Gain

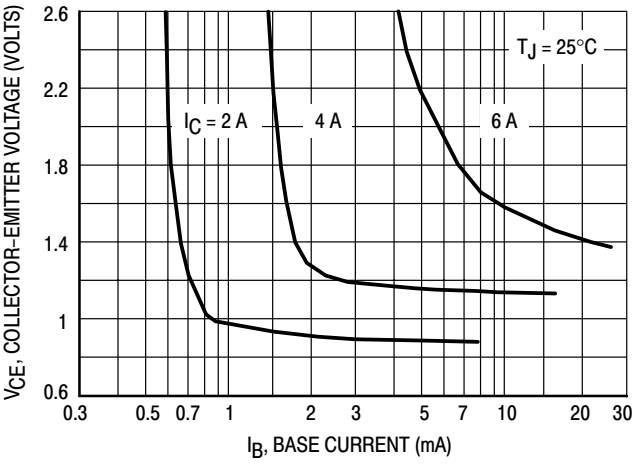


Figure 10. Typical Collector Saturation Region

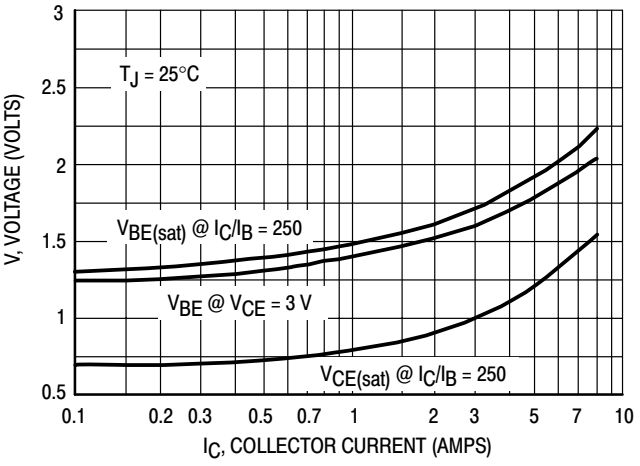


Figure 11. Typical “On” Voltages

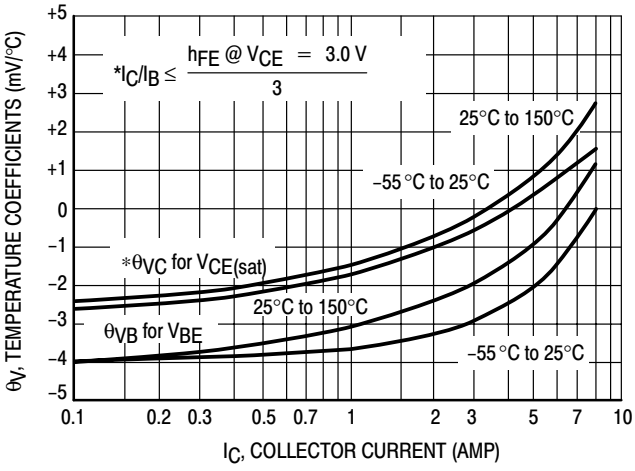


Figure 12. Typical Temperature Coefficients

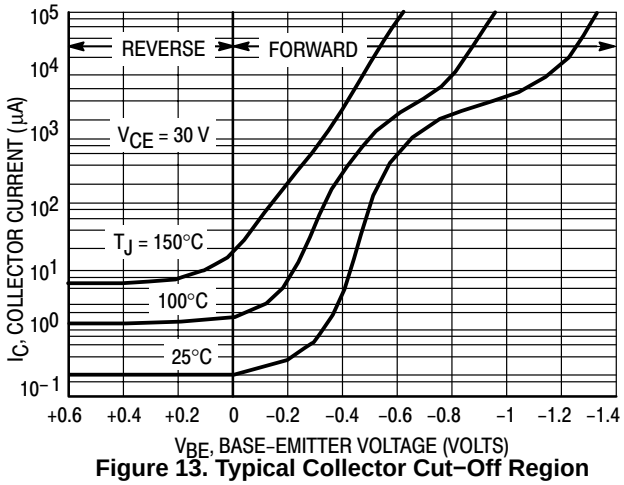


Figure 13. Typical Collector Cut−Off Region

BD135, BD137, BD139

Plastic Medium Power Silicon NPN Transistor

This series of plastic, medium−power silicon NPN transistors are designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

Features

- Pb−Free Package is Available*
- DC Current Gain − h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	BD135 BD137 BD139	V_{CEO}	45 60 80	Vdc
Collector−Base Voltage	BD135 BD137 BD139	V_{CBO}	45 60 100	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	1.5	Adc
Base Current		I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	12.5 100	Watts mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

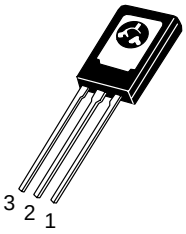
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction−to−Ambient	θ_{JA}	100	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

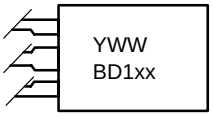
http://onsemi.com

1.5 A POWER TRANSISTORS
NPN SILICON
45, 60, 80 V, 10 W



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



xx = 35, 37, 39
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
BD135	TO−225AA	500 Units/Box
BD137	TO−225AA	500 Units/Box
BD139	TO−225AA	500 Units/Box
BD139G	TO−225AA (Pb−Free)	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	– – –	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}		– –	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		–	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A V_{CE} = 2 V)	h_{FE}*		25 40 25	– 250 –	–
Collector−Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		–	0.5	Vdc
Base−Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		–	1	Vdc

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

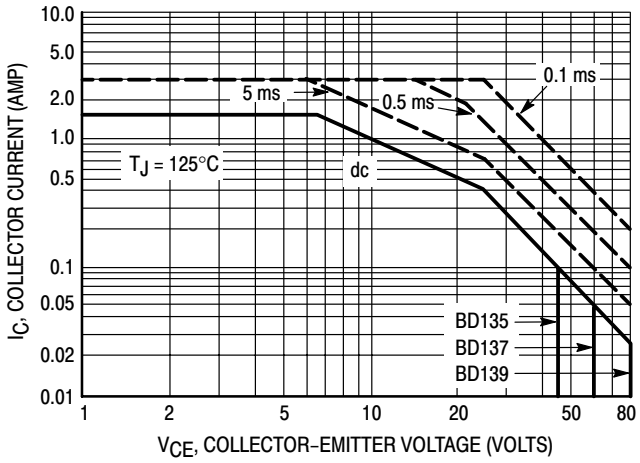


Figure 1. Active−Region Safe Operating Area

BD136, BD138, BD140

Plastic Medium Power Silicon PNP Transistor

This series of plastic, medium−power silicon PNP transistors are designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

Features

- Pb−Free Package is Available*
- DC Current Gain − h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	BD136 BD138 BD140	V_{CEO}	45 60 80	Vdc
Collector−Base Voltage	BD136 BD138 BD140	V_{CBO}	45 60 100	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	1.5	Adc
Base Current		I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	12.5 100	Watts mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

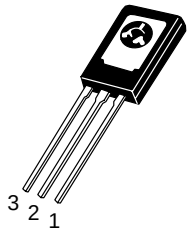
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction−to−Ambient	θ_{JA}	100	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

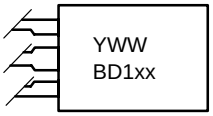
http://onsemi.com

1.5 A POWER TRANSISTORS
PNP SILICON
45, 60, 80 V, 10 W



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



xx = 36, 38, 40
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
BD136	TO−225AA	500 Units/Box
BD136G	TO−225AA (Pb−Free)	500 Units/Box
BD138	TO−225AA	500 Units/Box
BD140	TO−225AA	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Type	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)		BV_{CEO}	BD 136 BD 138 BD 140	45 60 80	– – –	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125 °C)		I_{CBO}		– –	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		–	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	 ALL ALL	h_{FE}*		 25 40 25	 – 250 –	–
Collector−Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)		$V_{CE(sat)}$*		–	0.5	Vdc
Base−Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$*		–	1	Vdc

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

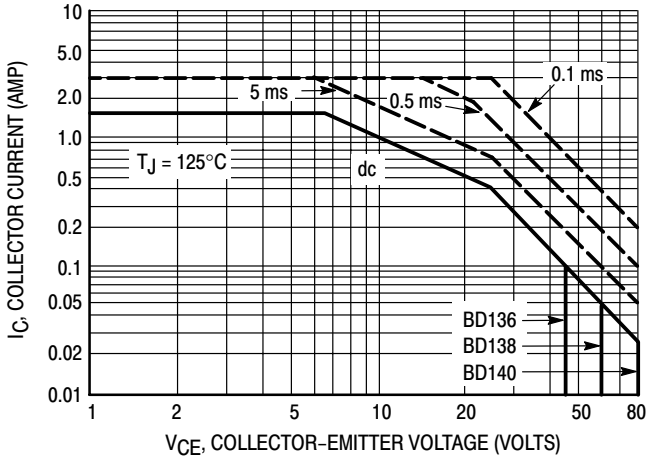


Figure 1. Active−Region Safe Operating Area

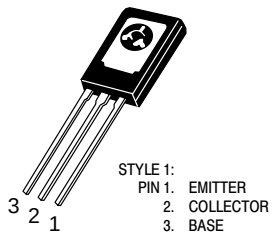
Plastic Medium Power NPN Silicon Transistor

BD159

. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line−Operated Equipment
- Thermopad™ Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
20 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	350	Vdc
Collector−Base Voltage	V_{CB}	375	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	0.5 1.0	Adc
Base Current	I_B	0.25	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	350	—	Vdc
Collector Cutoff Current (At rated voltage)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

April, 2002 − Rev. 3
Publication Order Number:
BD159/D

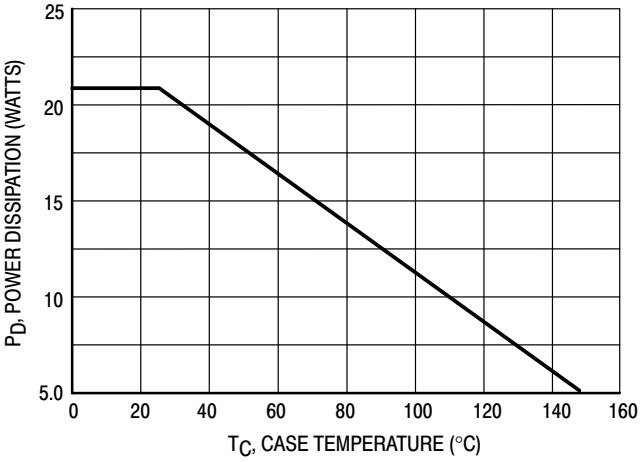


Figure 2. Power−Temperature Derating Curve

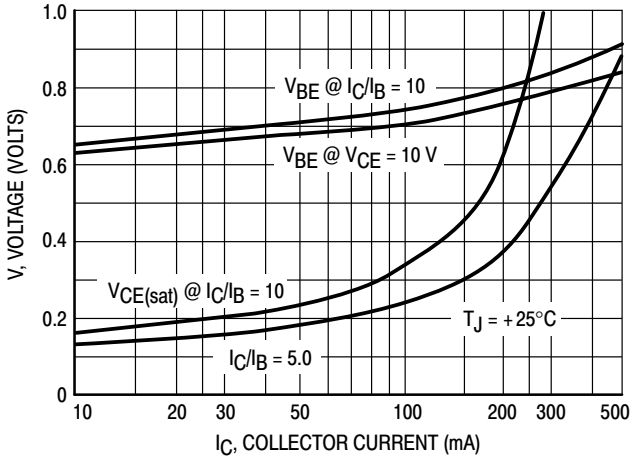


Figure 3. "On" Voltages

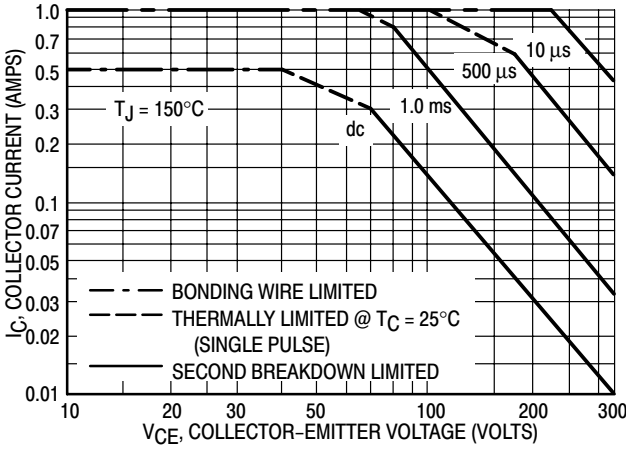


Figure 4. DC Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below, the maximum T_J, power−temperature derating must be observed for both steady state and pulse power conditions.

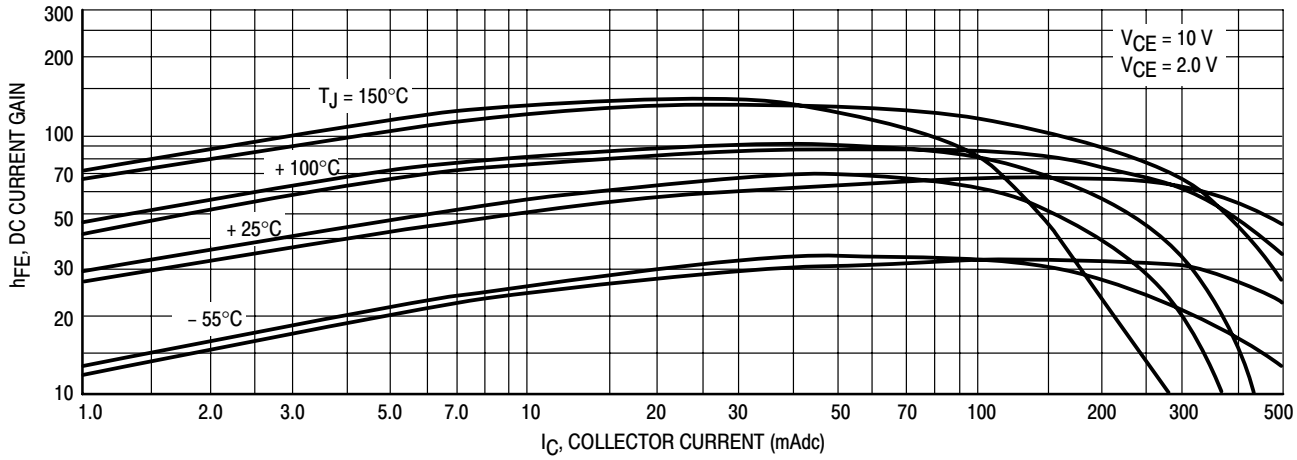


Figure 5. Current Gain

Plastic Medium Power Silicon NPN Transistor

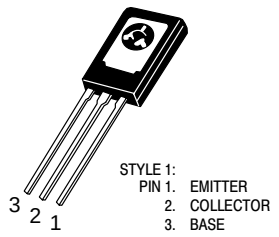
BD179
BD179-10

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD179 is complementary with BD180

3.0 AMPERES
POWER TRANSISTORS
NPN SILICON
80 VOLTS
30 WATTS

*ON Semiconductor Preferred Device



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 240	Watts mw/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) BD179−10 (I_C = 1.0 A, V_{CE} = 2.0 V) ALL	h_{FE}	 63 15	 160 —	
Collector−Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base−Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current−Gain − Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

*Pulse Test: Pulse Width ≦ 300 As, Duty Cycle ≦ 2.0%.

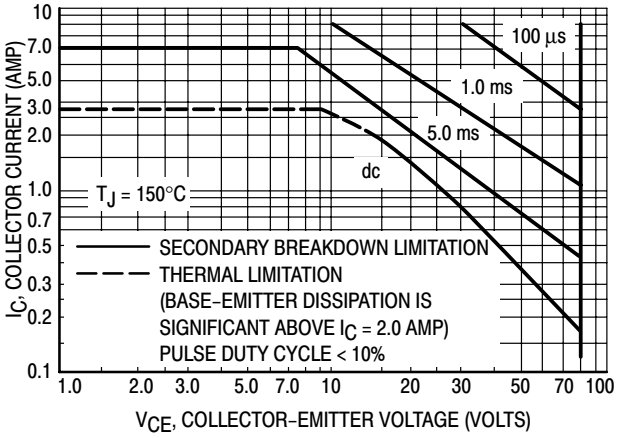


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power−temperature derating must be observed for both steady state and pulse power conditions.

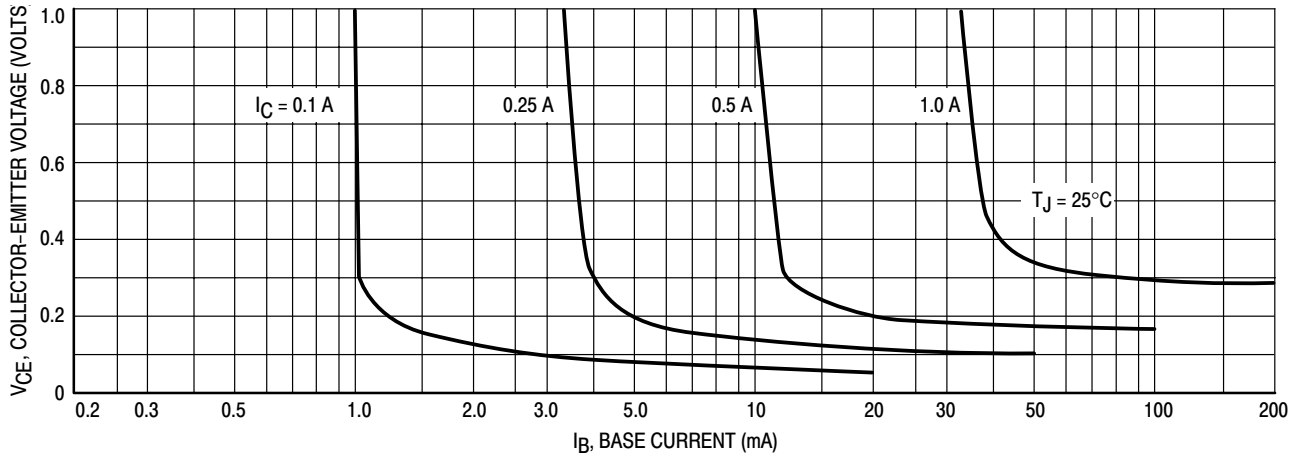


Figure 2. Collector Saturation Region

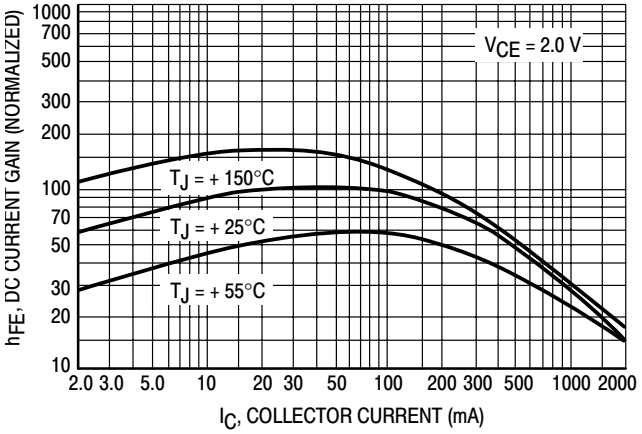


Figure 3. Current Gain

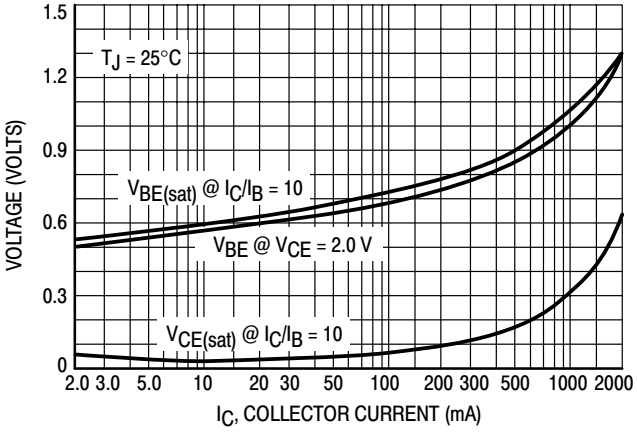


Figure 4. “On” Voltages

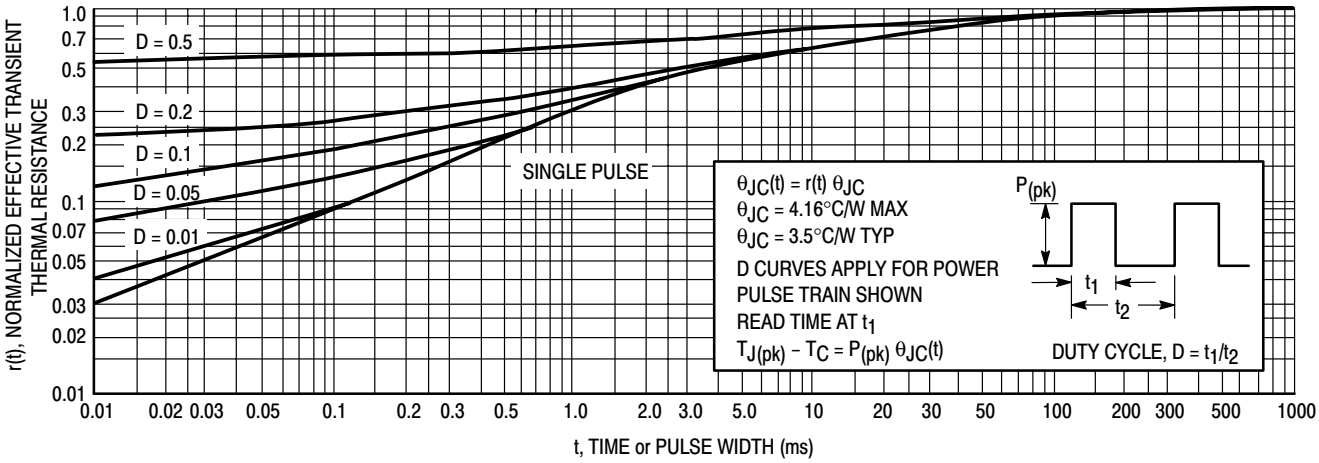


Figure 5. Thermal Response

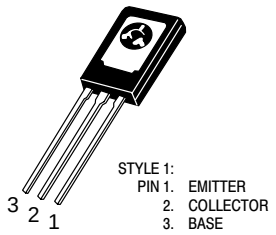
BD180

Plastic Medium Power Silicon PNP Transistor

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD180 is complementary with BD179

3.0 AMPERES
POWER TRANSISTOR
PNP SILICON
80 VOLTS
30 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) BD180	I_{CBO}	 —	 —	mAdc
		—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V)	h_{FE}	 40 15	 250 —	—
Collector−Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base−Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current−Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

April, 2002 − Rev. 10
Publication Order Number:
BD180/D

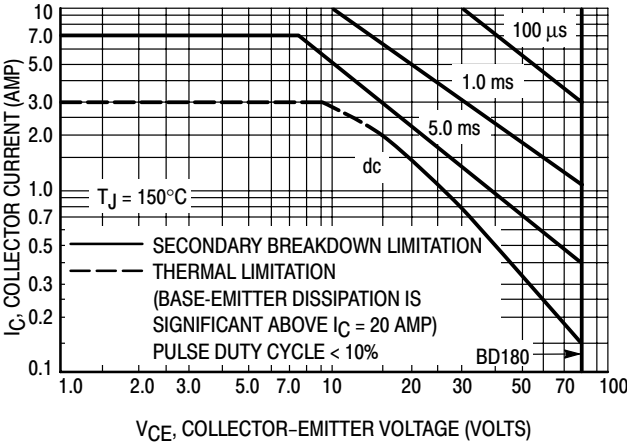


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power−temperature derating must be observed for both steady state and pulse power conditions.

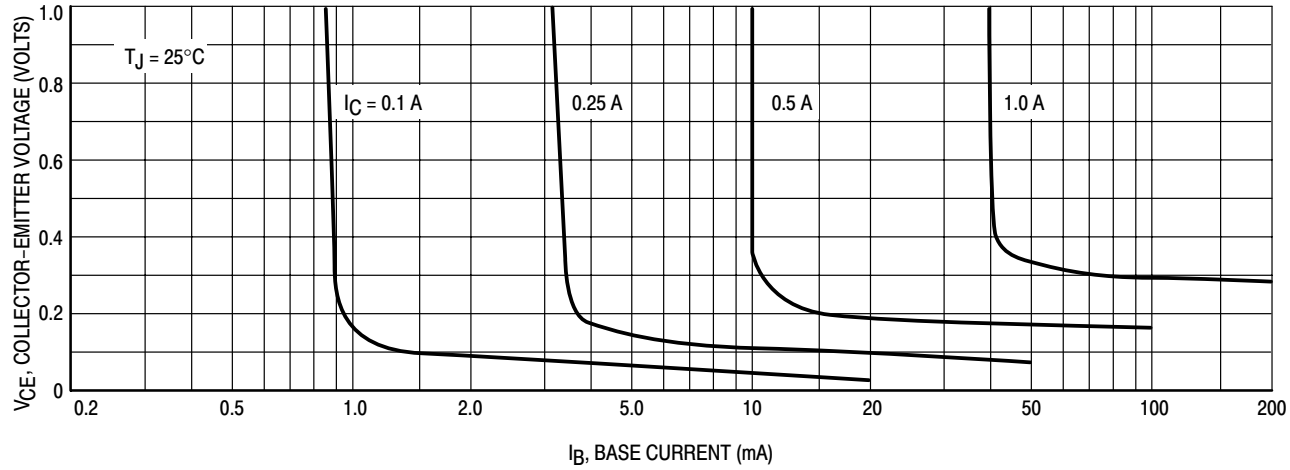


Figure 2. Collector Saturation Region

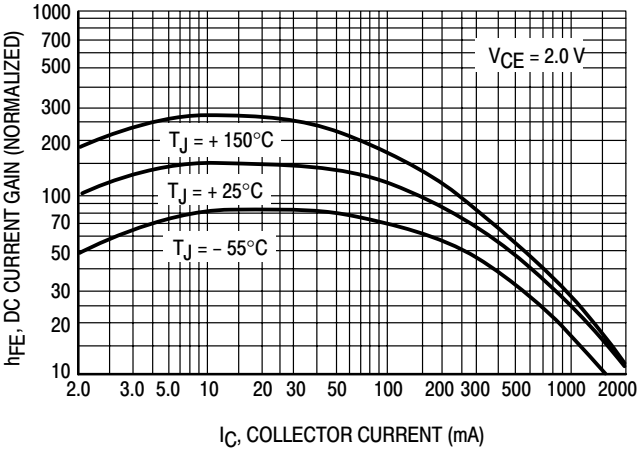


Figure 3. Current Gain

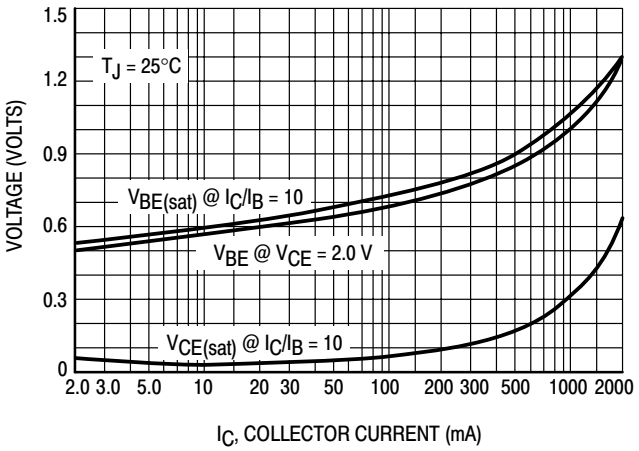


Figure 4. "On" Voltages

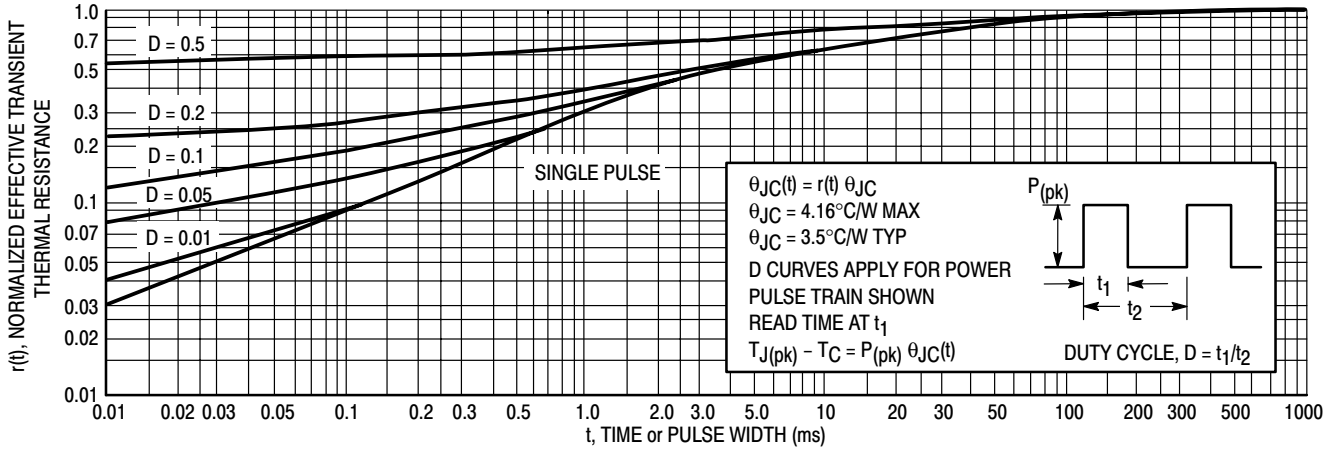


Figure 5. Thermal Response

BD237 (NPN), BD238 (PNP)

Preferred Devices

Plastic Medium Power Silicon NPN Transistor

Designed for use in 5.0 to 10 W audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain −
  h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- Epoxy Meets UL94, VO @ 1/8″
- ESD Ratings: Human Body Model, 3B; >8000 V
  Machine Model, C; >400 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CBO}	100	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	2.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

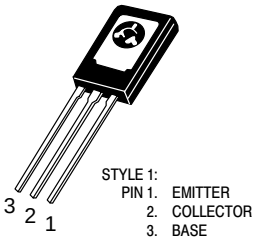
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	5.0	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ON Semiconductor®

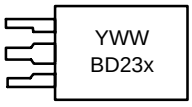
http://onsemi.com

2.0 AMPERES
POWER TRANSISTORS
NPN SILICON
80 VOLTS
25 WATTS



CASE 77−09
TO−225

MARKING DIAGRAM



x = 7 or 8
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BD237	TO−225	500 Units/Box
BD238	TO−225	500 Units/Box

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	−	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	−	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V)	h_{FE1} h_{FE2}	40 25	− −	−
Collector−Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	−	0.6	Vdc
Base−Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	−	1.3	Vdc
Current−Gain − Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	−	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

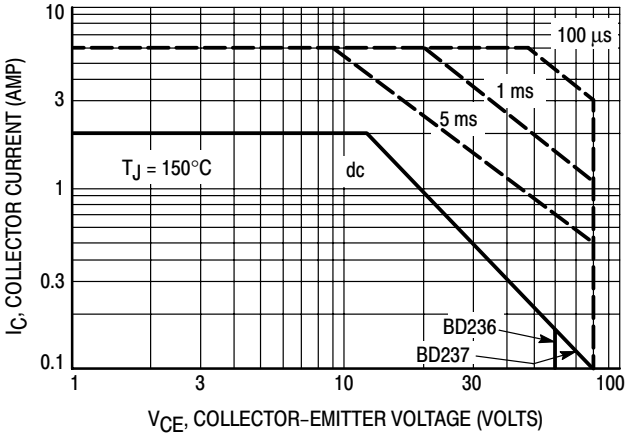


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power−temperature derating must be observed for both steady state and pulse power conditions.

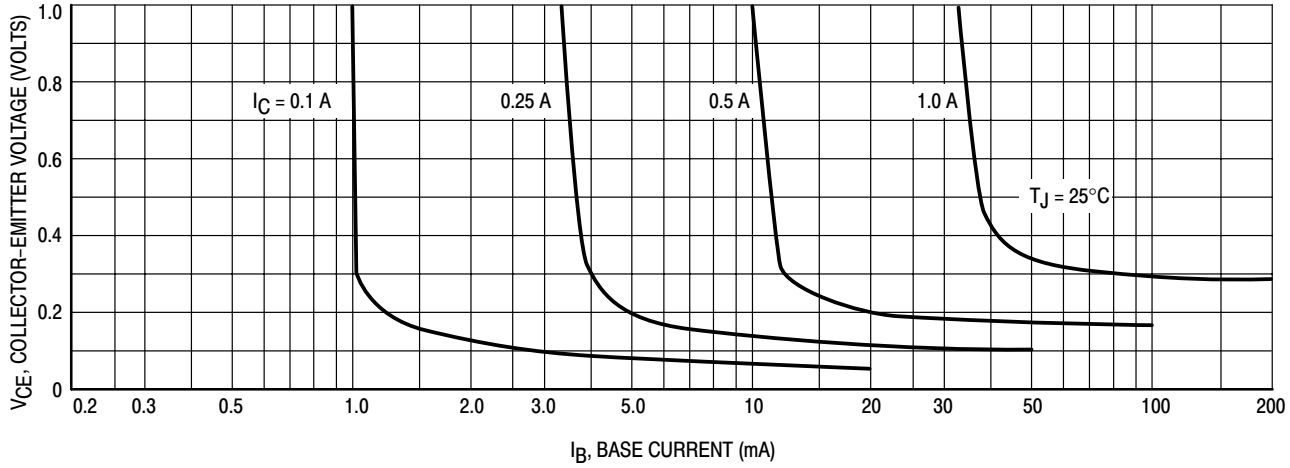


Figure 2. Collector Saturation Region

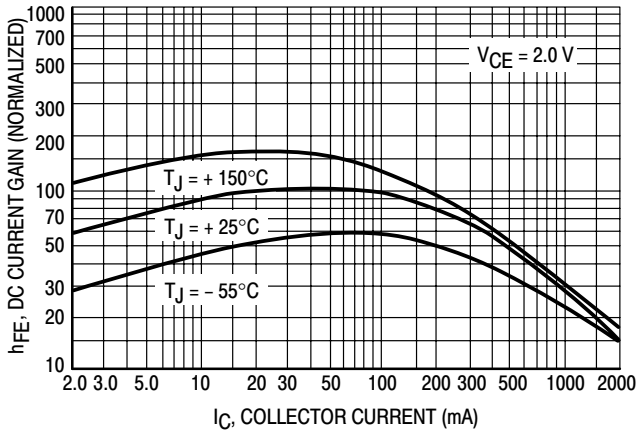


Figure 3. Current Gain

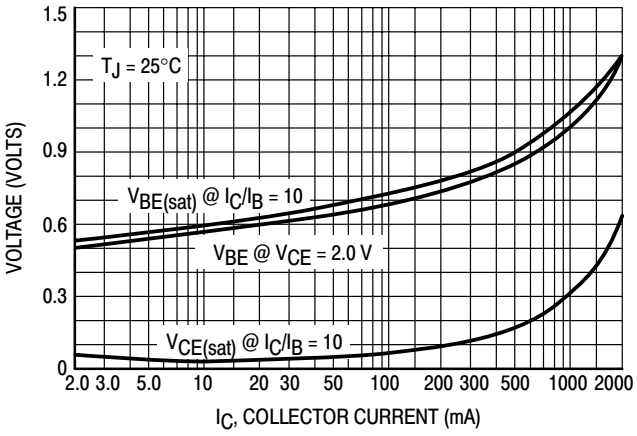


Figure 4. “On” Voltages

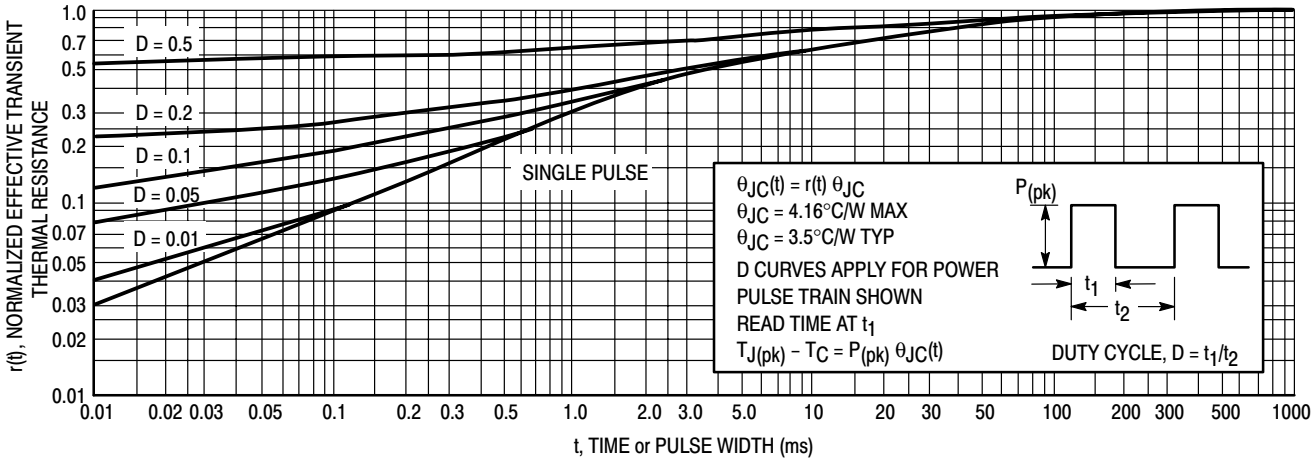


Figure 5. Thermal Response

BD241C* (NPN), BD242B (PNP), BD242C* (PNP)

***Preferred Devices**

Complementary Silicon Plastic Power Transistors

Designed for use in general purpose amplifier and switching applications.

- Collector−Emitter Saturation Voltage −
  V_{CE} = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 100 Vdc (Min) BD241C, BD242C
- High Current Gain − Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO−220 AB Package
- Epoxy Meets UL94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	BD242B	BD241C BD242C	Unit
Collector−Emitter Voltage	V_{CEO}	80	100	Vdc
Collector−Emitter Voltage	V_{CES}	90	115	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current Continuous Peak	I_C	 3.0 5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

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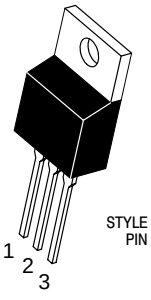
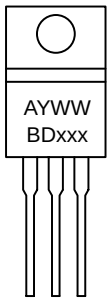
POWER TRANSISTORS
COMPLEMENTARY
SILICON
3 AMPERES
80, 100 VOLTS
40 WATTS



TO−220AB
CASE 221A
STYLE 1

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

MARKING DIAGRAM



xxx = Specific Device Code:
241C, 242B, 242C
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BD241C	TO−220AB	50 Units/Rail
BD242B	TO−220AB	50 Units/Rail
BD242C	TO−220AB	50 Units/Rail

Publication Order Number:

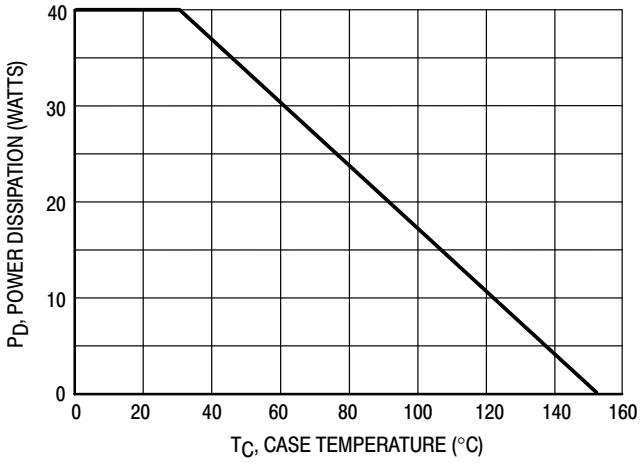


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 5) (I_C = 30 mAdc, I_B = 0)	BD242B BD241C, BD242C	V_{CEO}	 80 100		Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	 BD242B BD241C, BD242C	I_{CEO}		0.3	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	 BD242B BD241C, BD242C	I_{CES}		200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		1.0	mAdc
ON CHARACTERISTICS (Note 5)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 25 10		
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc)		$V_{CE(sat)}$		1.2	Vdc
Base−Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain − Bandwidth Product (Note 6) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0		MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20		

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
6. $f_T = |h_{fe}| \bullet f_{test}$.

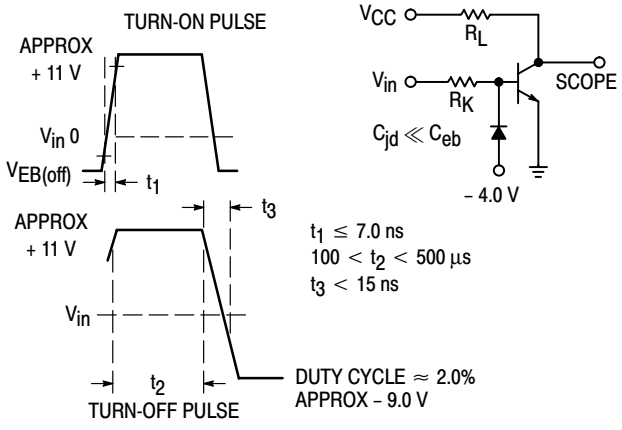


Figure 2. Switching Time Equivalent Circuit

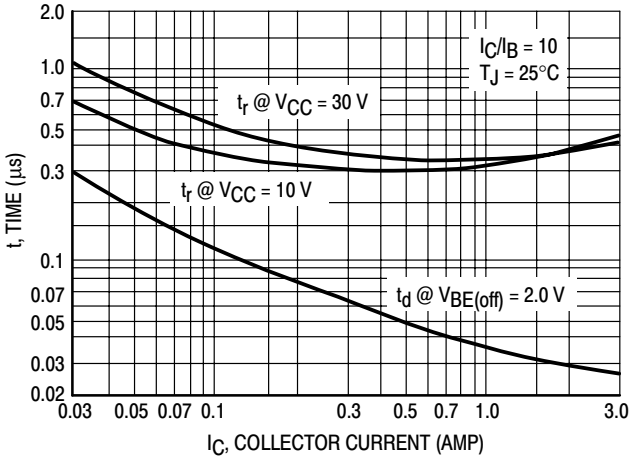


Figure 3. Turn−On Time

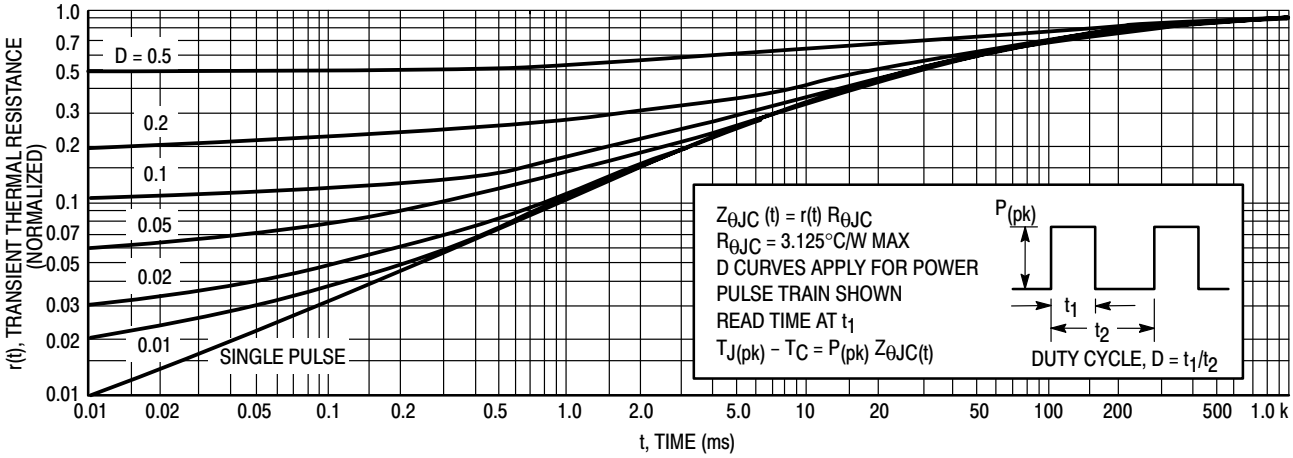


Figure 4. Thermal Response

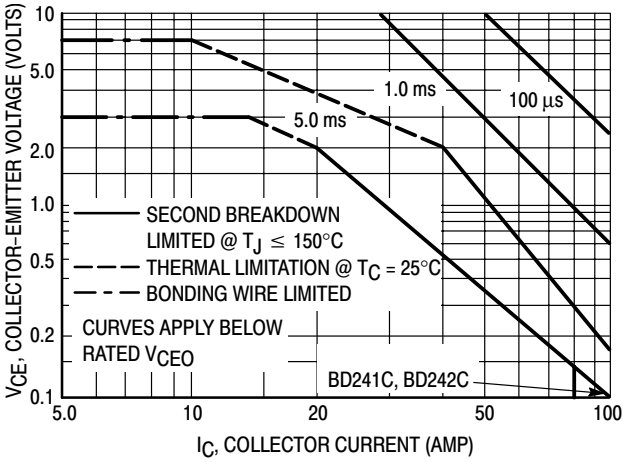


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

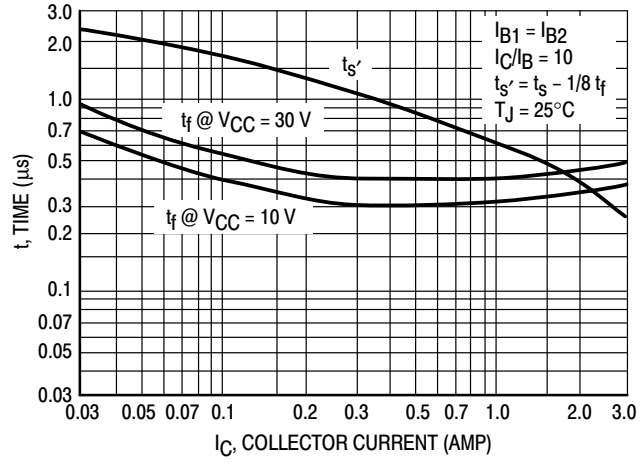


Figure 6. Turn−Off Time

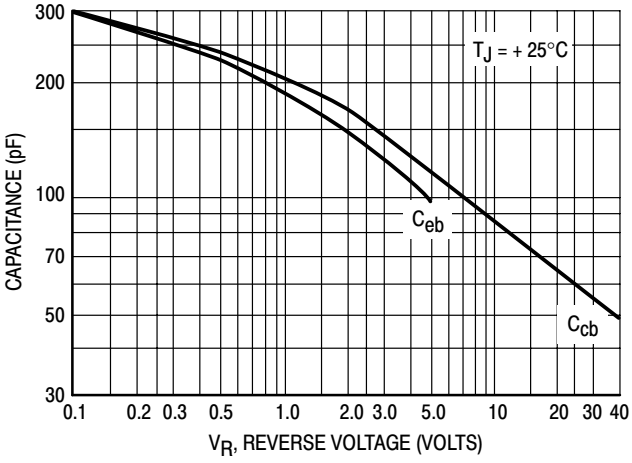


Figure 7. Capacitance

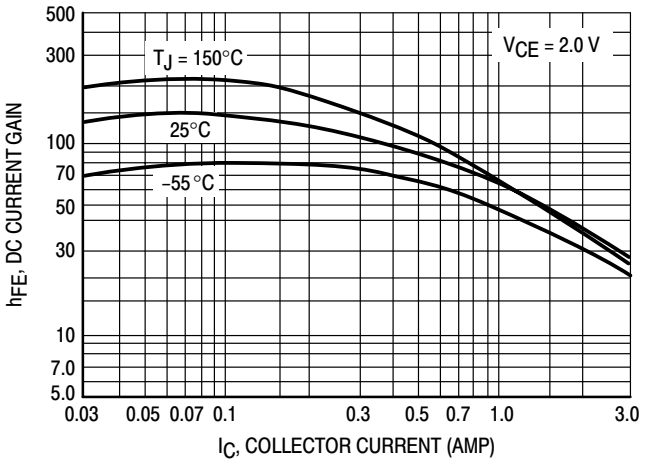


Figure 8. DC Current Gain

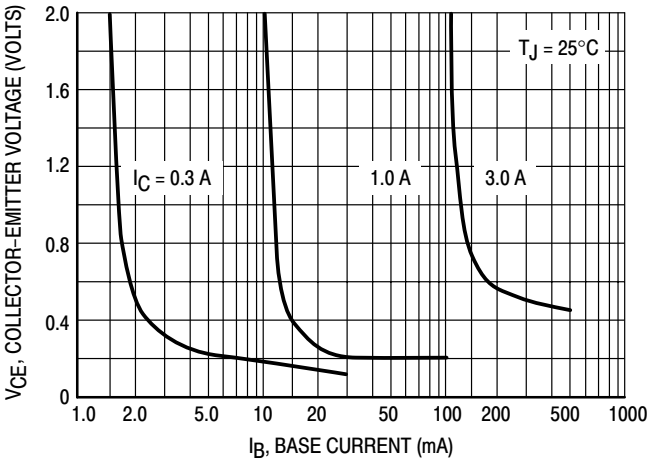


Figure 9. Collector Saturation Region

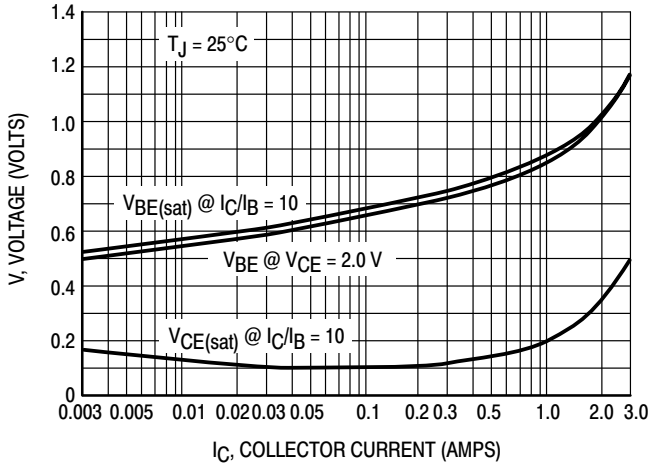


Figure 10. “On” Voltages

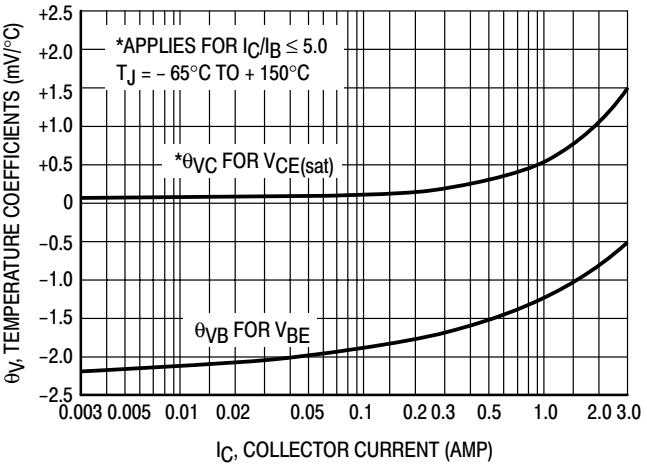


Figure 11. Temperature Coefficients

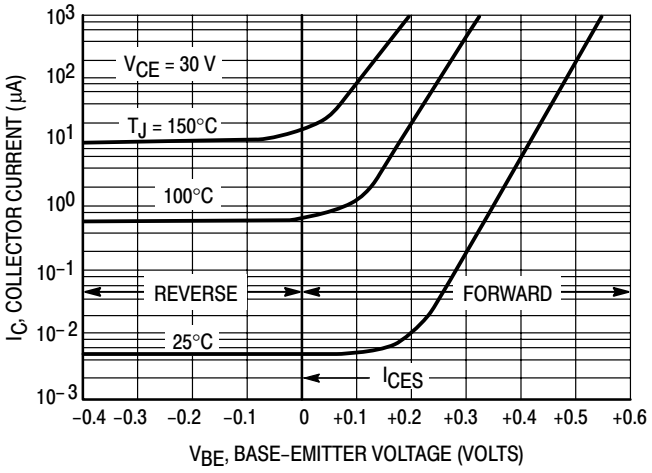


Figure 12. Collector Cut−Off Region

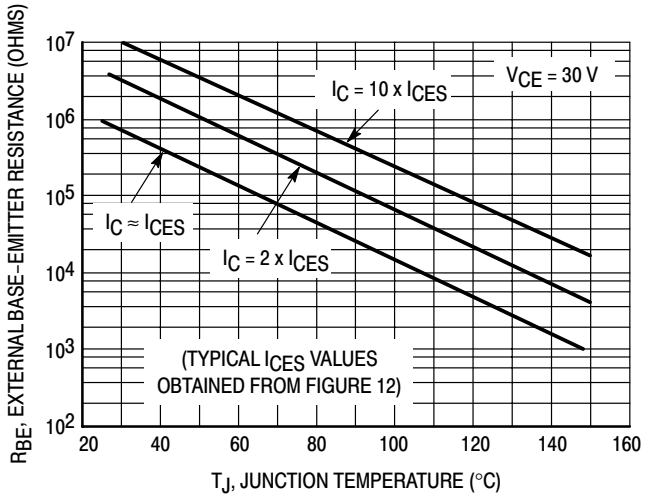


Figure 13. Effects of Base−Emitter Resistance

Complementary Silicon Plastic Power Transistors

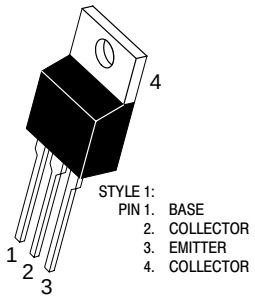
. . . designed for use in general purpose amplifier and switching applications.

- Collector − Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BD243B, BD244B
  = 100 Vdc (Min) — BD243C, BD244C
- High Current Gain Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO−220 AB Package

NPN
BD243B
BD243C*
PNP
BD244B
BD244C*

*ON Semiconductor Preferred Device

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80−100 VOLTS
65 WATTS



CASE 221A−06
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	BD243B BD244B	BD243C BD244C	Unit
Collector−Emitter Voltage	V_{CEO}	80	100	Vdc
Collector−Base Voltage	V_{CB}	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	6 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

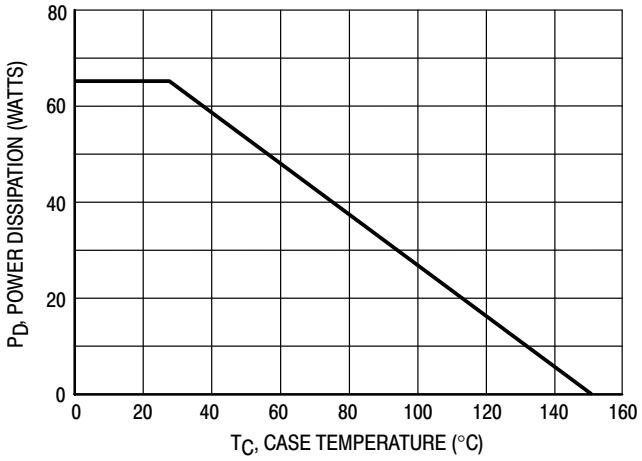


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD243B, BD244B BD243C, BD244C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	BD243B, BD243C, BD244B, BD244C	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	BD243B, BD244B BD243C, BD244C	I_{CES}	— —	400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	— —	—
Collector−Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	—	1.5	Vdc
Base−Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = h_{fe} \bullet f_{test}$

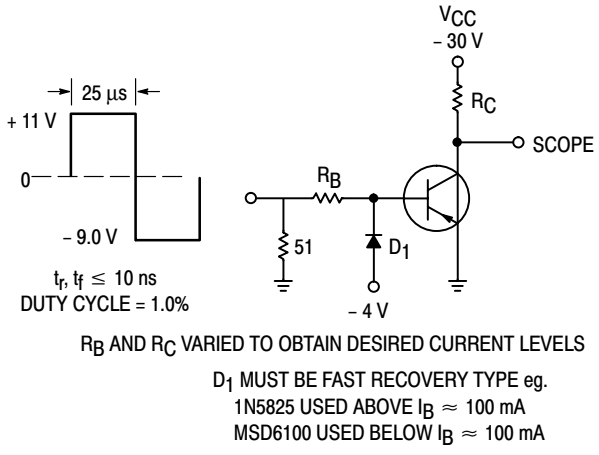


Figure 2. Switching Time Test Circuit

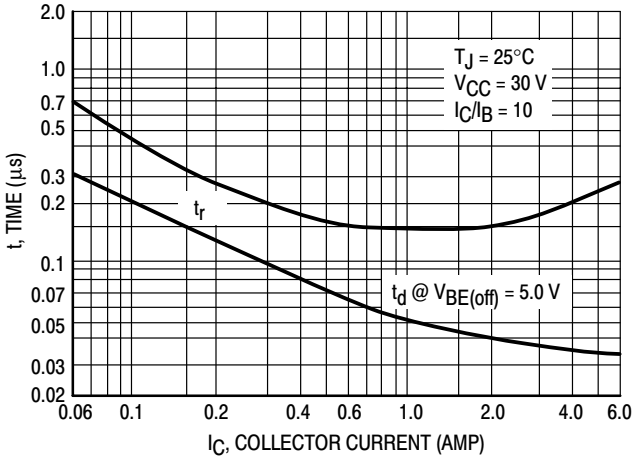


Figure 3. Turn−On Time

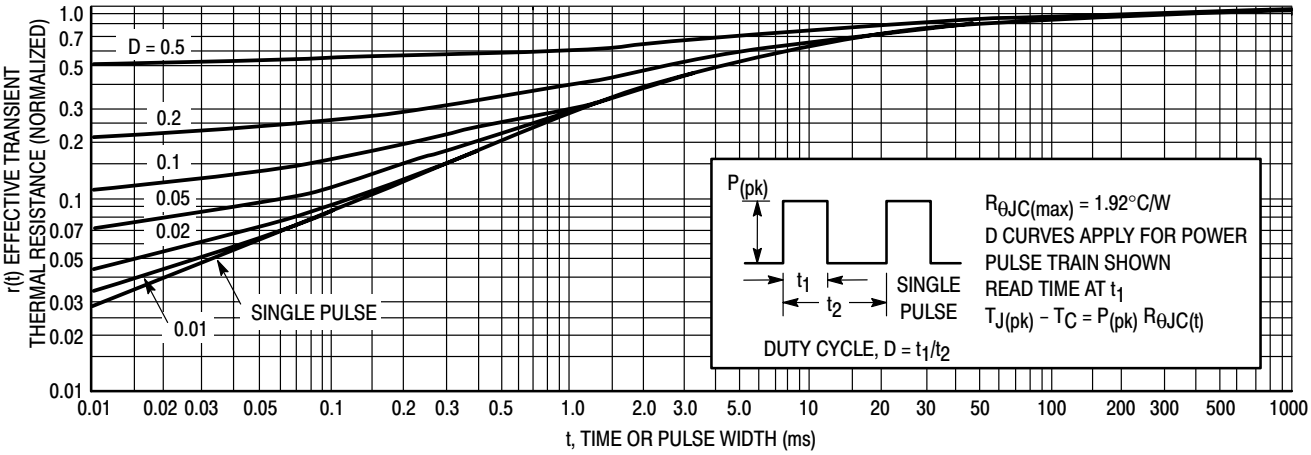


Figure 4. Thermal Response

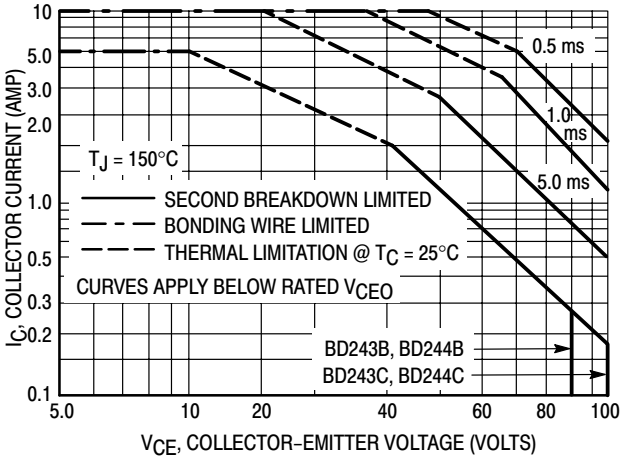


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

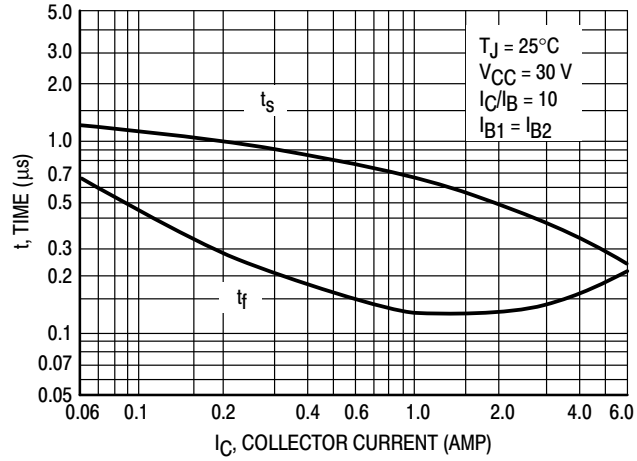


Figure 6. Turn-Off Time

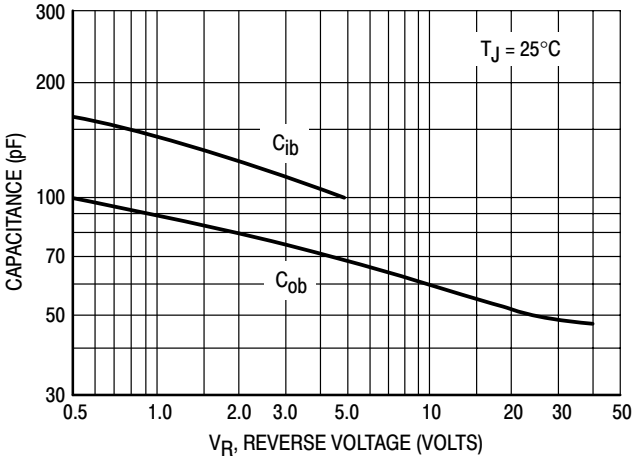


Figure 7. Capacitance

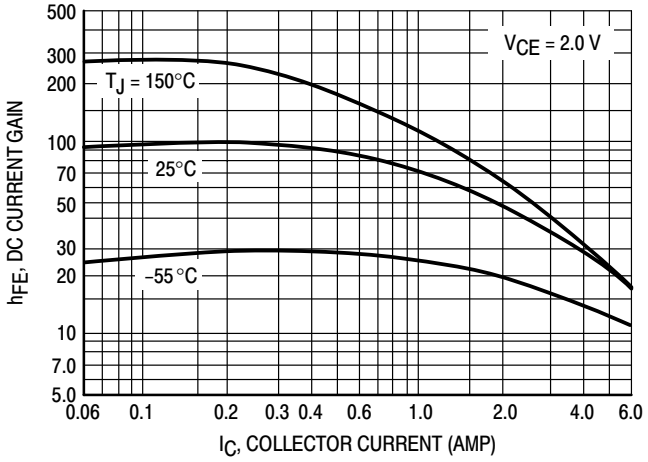


Figure 8. DC Current Gain

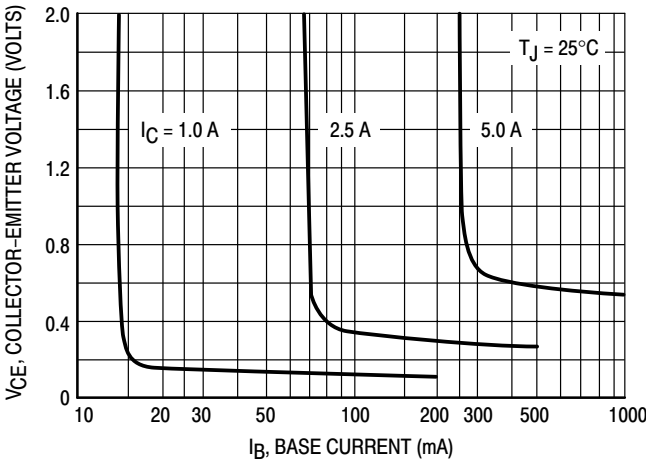


Figure 9. Collector Saturation Region

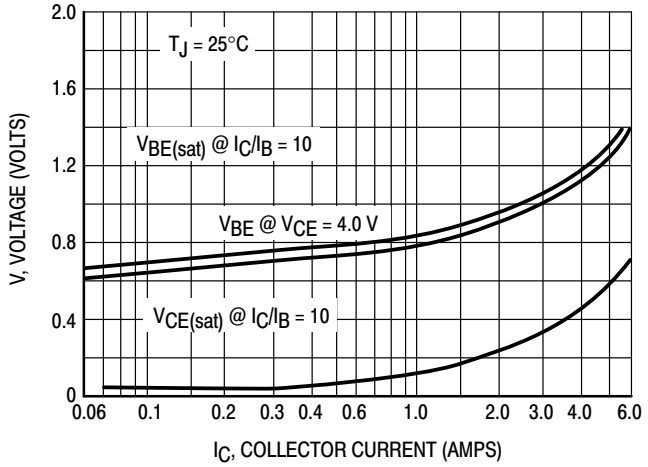


Figure 10. “On” Voltages

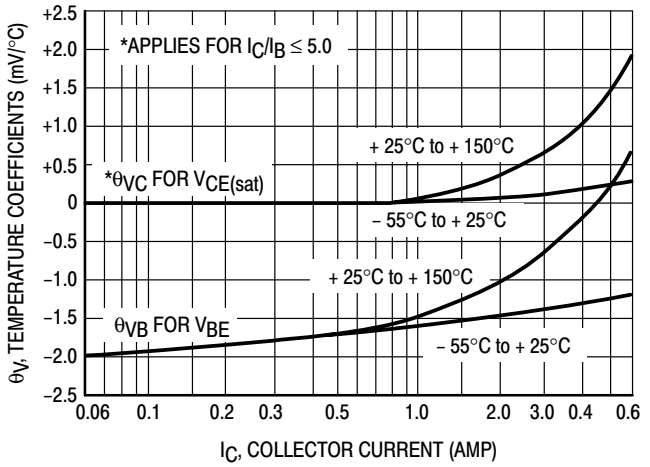


Figure 11. Temperature Coefficients

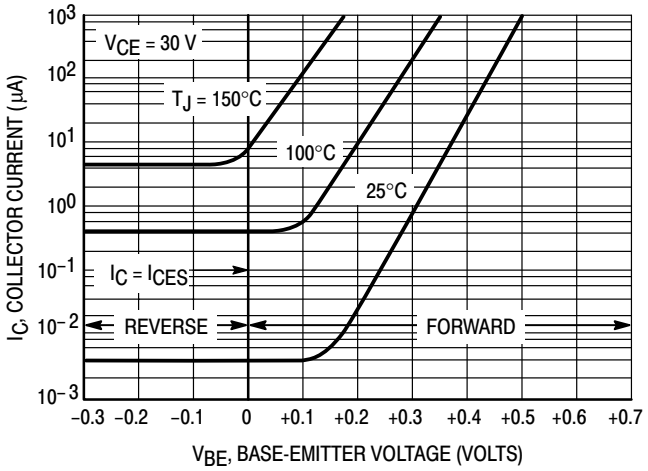


Figure 12. Collector Cut-Off Region

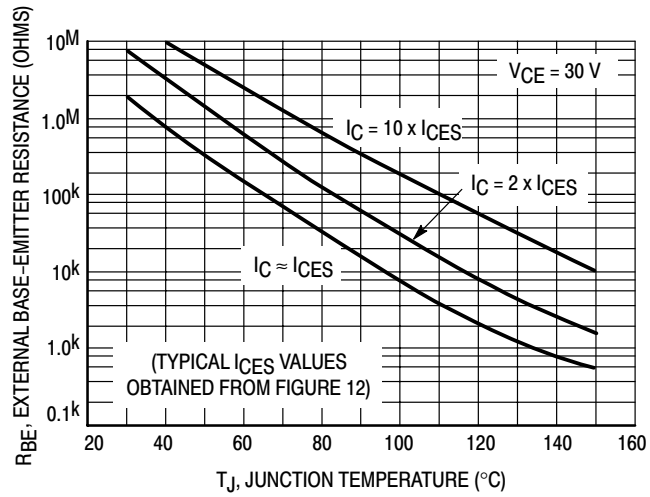


Figure 13. Effects of Base−Emitter Resistance

BD249C

NPN High-Power Transistor

. . . for general−purpose power amplifier and switching applications.

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V−0 @ 1/8”

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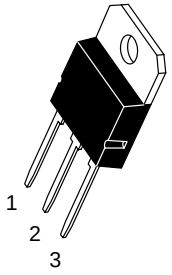
25 A, 100 V, 125 W
NPN SILICON
POWER TRANSISTOR



TO−218
CASE 340D
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CBO}	100	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous Peak (Note 1)	I_C	25 40	Adc Apk
Base Current − Continuous	I_B	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
Unclamped Inductive Load	E_{SB}	90	mJ

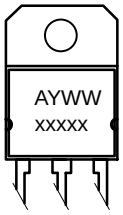
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35.7	°C/W

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

ORDERING INFORMATION

Device	Package	Shipping
BD249C	TO−218	30 Units / Rail

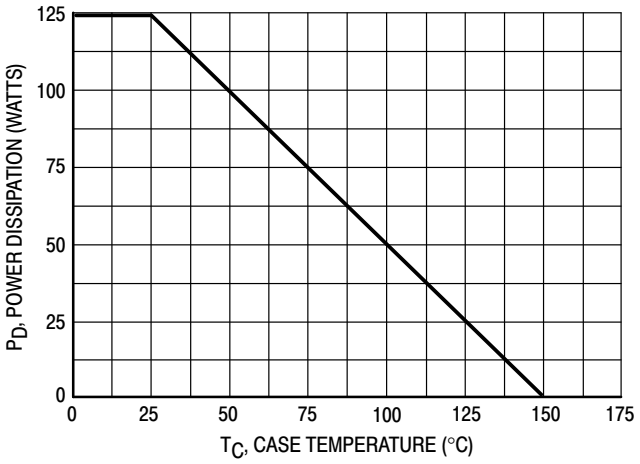


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mA, I_B = 0)	$V_{CEO(sus)}$	100	−	V
Collector−Emitter Cutoff Current (V_{CE} = 60 V, I_B = 0)	I_{CEO}	−	1.0	mA
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	−	0.7	mA
Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	−	1.0	mA
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 1.5 A, V_{CE} = 4.0 V) (I_C = 15 A, V_{CE} = 4.0 V) (I_C = 25 A, V_{CE} = 4.0 V)	h_{FE}	 25 10 5.0	 − − −	−
Collector−Emitter Saturation Voltage (I_C = 15 A, I_B = 1.5 A) (I_C = 25 A, I_B = 5.0 A)	$V_{CE(sat)}$	 − −	 1.8 4.0	V
Base−Emitter On Voltage (I_C = 15 A, V_{CE} = 4.0 V) (I_C = 25 A, V_{CE} = 4.0 V)	$V_{BE(on)}$	 − −	 2.0 4.0	V
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	25	−	−
Current−Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	−	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

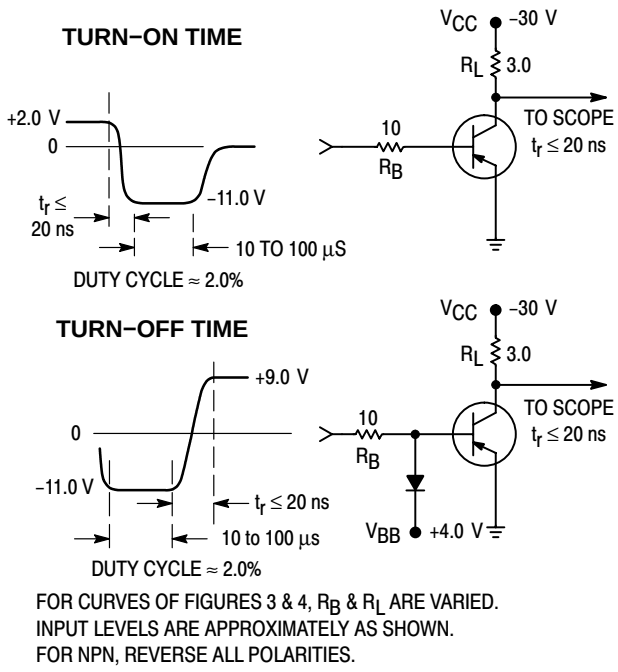


Figure 2. Switching Time Equivalent Test Circuits

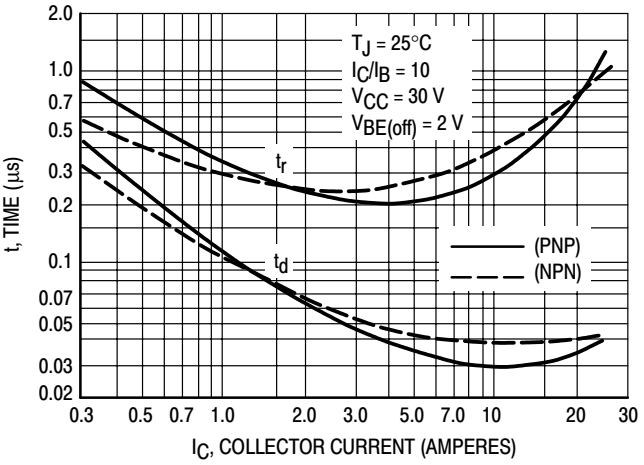


Figure 3. Turn−On Time

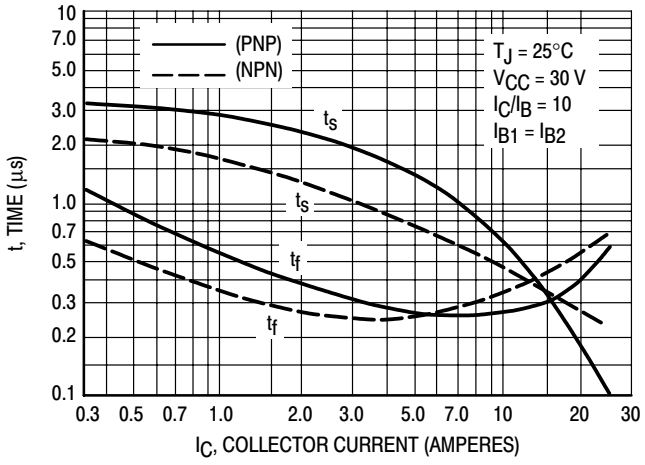


Figure 4. Turn−Off Time

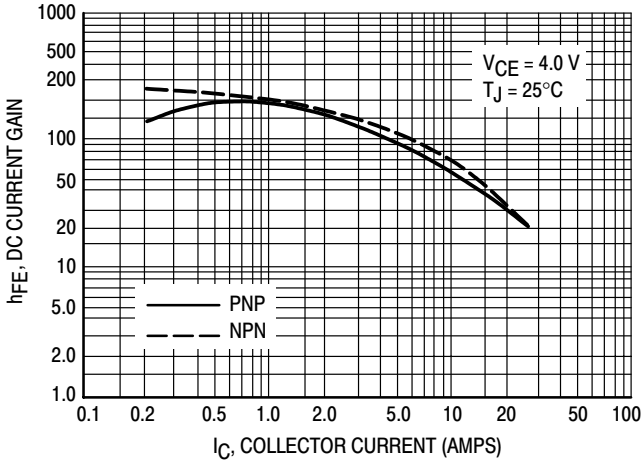


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

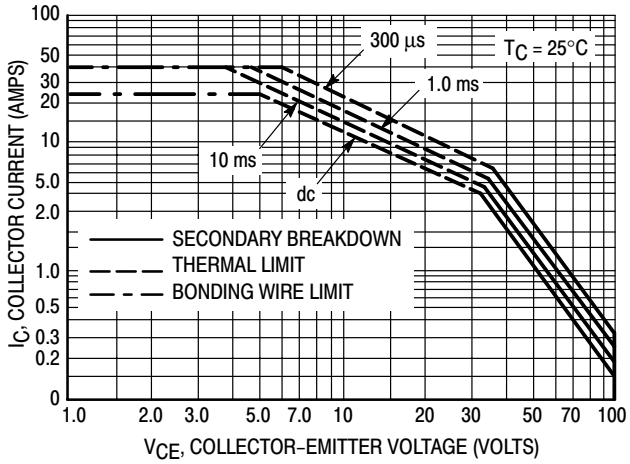


Figure 6. Maximum Rated Forward Bias Safe Operating Area

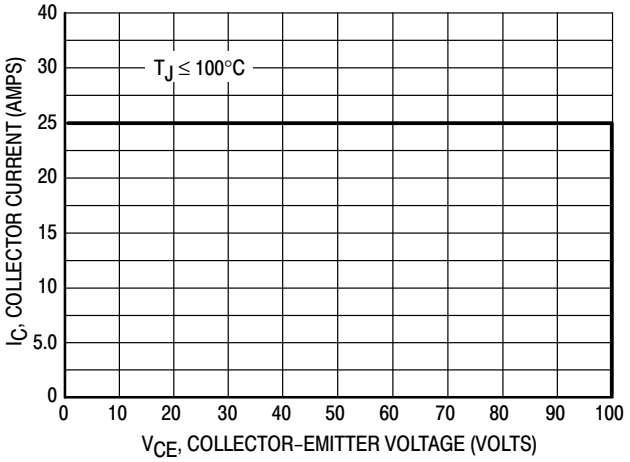
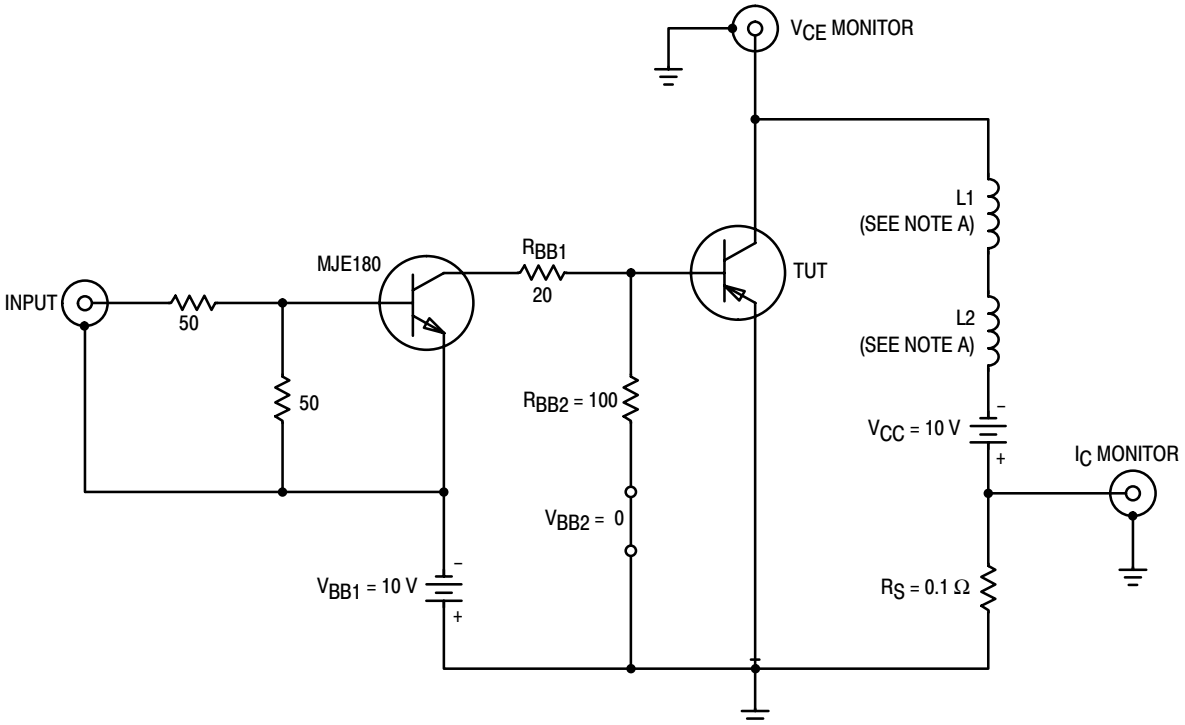
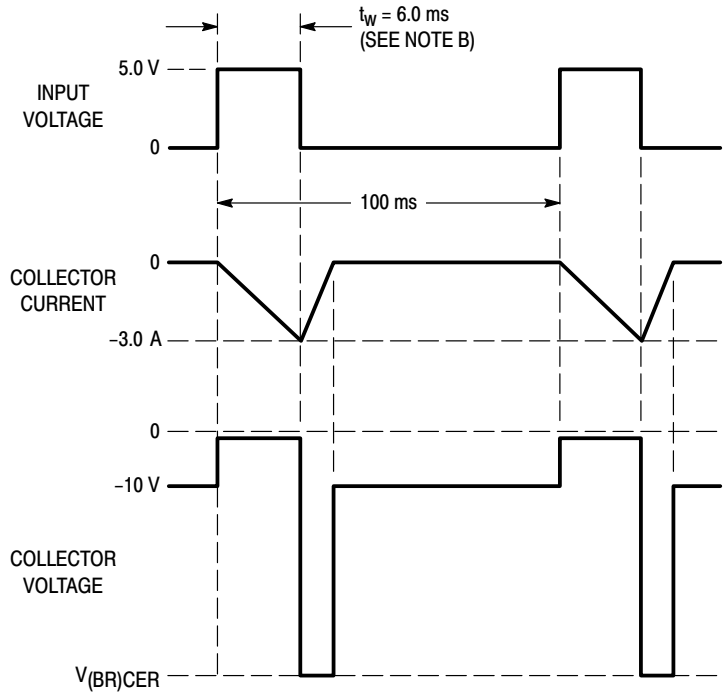


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C−2688, or equivalent.
B. Input pulse width is increased until I_{CM} = −3.0 A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

BD435, BD437, BD439, BD441

Plastic Medium Power Silicon NPN Transistor

This series of plastic, medium−power silicon NPN transistors can be used for amplifier and switching applications. Complementary types are BD438 and BD442.

Features

- Pb−Free Package is Available*

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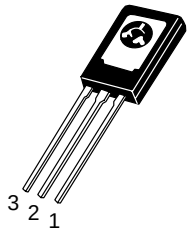
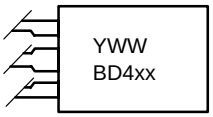
4.0 AMPERES
POWER TRANSISTORS
NPN SILICON



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



xx = 35, 37, 39, 41
Y = Year
WW = Work Week

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	BD435 BD437 BD439 BD441	V_{CEO}	32 45 60 80	Vdc
Collector−Base Voltage	BD435 BD437 BD439 BD441	V_{CBO}	32 45 60 80	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	36 288	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	3.5	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
BD435	TO−225AA	500 Units/Box
BD437	TO−225AA	500 Units/Box
BD437G	TO−225AA (Pb−Free)	500 Units/Box
BD437T	TO−225AA	500 Units/Rail
BD439	TO−225AA	500 Units/Box
BD441	TO−225AA	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector−Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD435 BD437 BD439 BD441	$V_{(BR)CEO}$	32 45 60 80	− − − −	− − − −	Vdc
Collector−Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD435 BD437 BD439 BD441	$V_{(BR)CBO}$	32 45 60 80	− − − −	− − −	Vdc
Emitter−Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		$V_{(BR)EBO}$	5.0	−	−	Vdc
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 32 V, I_E = 0)	BD435		−	−	0.1	
(V_{CB} = 45 V, I_E = 0)	BD437		−	−	0.1	
(V_{CB} = 60 V, I_E = 0)	BD439		−	−	0.1	
(V_{CB} = 80 V, I_E = 0)	BD441		−	−	0.1	
Emitter Cutoff Current (V_{EB} = 5.0 V)		I_{EBO}	−	−	1.0	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5.0 V)	BD435 BD437 BD439 BD441	h_{FE}	40 30 20 15	− − − −	− − − −	
DC Current Gain (I_C = 500 mA, V_{CE} = 1.0 V)	BD435 BD437 BD439, BD441	h_{FE}	85 85 40	− − −	475 375 475	
DC Current Gain (I_C = 2.0 A, V_{CE} = 1.0 V)	BD435 BD437 BD439 BD441	h_{FE}	50 40 25 15	− − − −	− − − −	
Collector Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.0 A, I_B = 0.2 V)	BD435		−	−	0.5	
(I_C = 3.0 A, I_B = 0.3 A)	BD437, BD439, BD441		−	−	0.8	
Base−Emitter On Voltage (I_C = 2.0 A, V_{CE} = 1.0 V)		$V_{BE(on)}$	−	−	1.1	Vdc
Current−Gain − Bandwidth Product (V_{CE} = 1.0 V, I_C = 250 mA, f = 1.0 MHz)		f_T	3.0	−	−	MHz

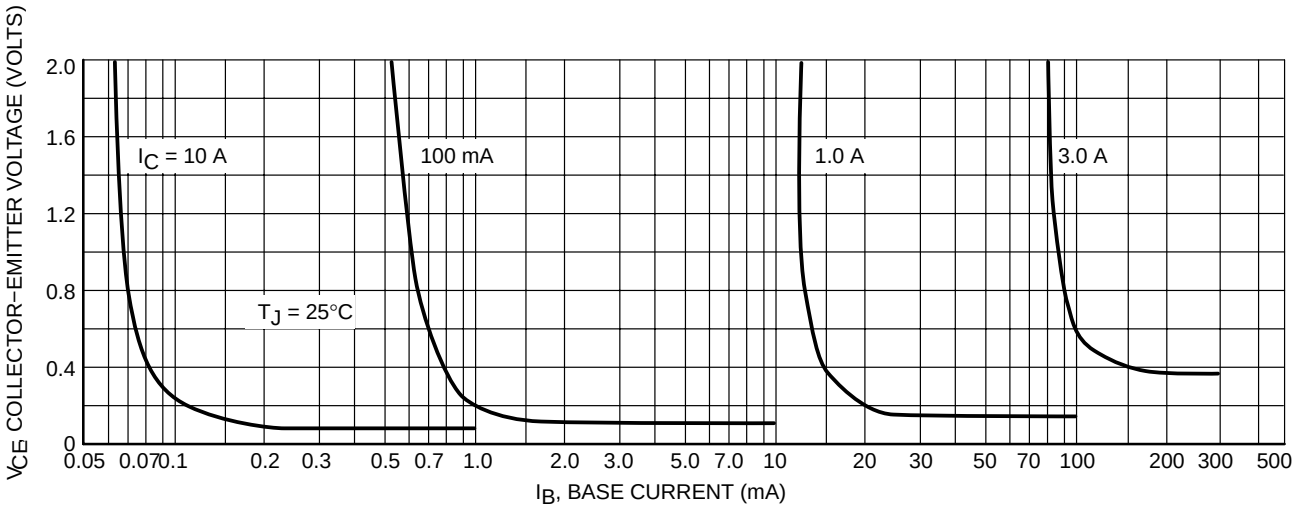


Figure 1. Collector Saturation Region

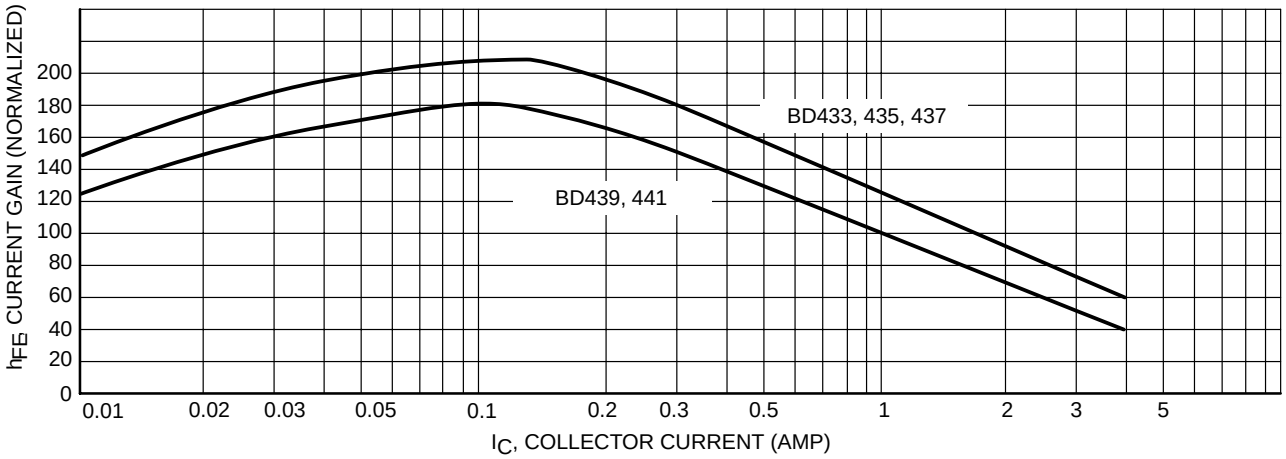


Figure 2. Current Gain

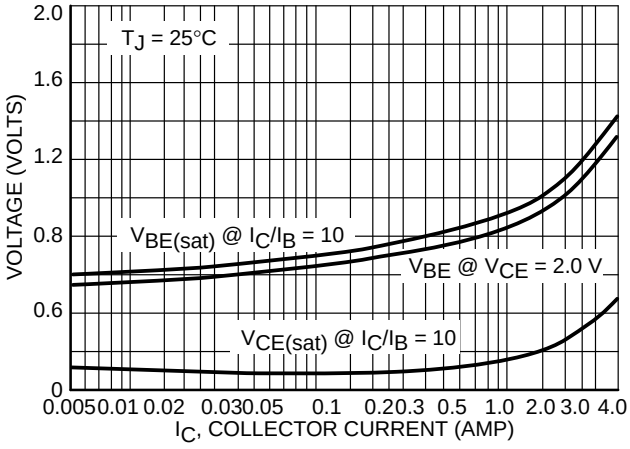


Figure 3. “On” Voltage

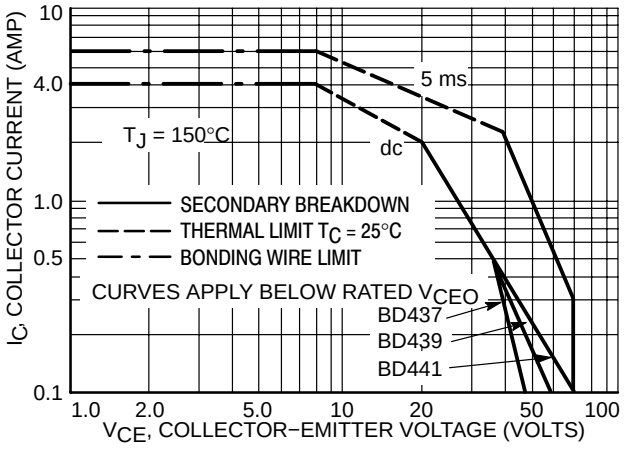


Figure 4. Active Region Safe Operating Area

BD436, BD438, BD440, BD442

Plastic Medium Power Silicon PNP Transistor

This series of plastic, medium−power silicon PNP transistors can be used for for amplifier and switching applications. Complementary types are BD437 and BD441.

Features

- Pb−Free Package is Available

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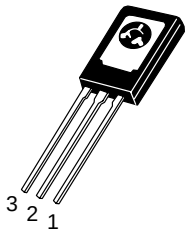
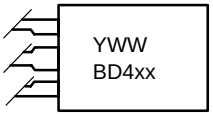
4.0 A POWER TRANSISTORS PNP SILICON



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



xx = 36, 38, 40, 42
Y = Year
WW = Work Week

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	BD436 BD438 BD440 BD442	V_{CEO}	32 45 60 80	Vdc
Collector−Base Voltage	BD436 BD438 BD440 BD442	V_{CBO}	32 45 60 80	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	36 288	W W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	3.5	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
BD436	TO−225AA	500 Units/Box
BD438	TO−225AA	500 Units/Box
BD436TG	TO−225AA (Pb−Free)	500 Units/Box
BD436T	TO−225AA	500 Units/Rail
BD440	TO−225AA	500 Units/Box
BD442	TO−225AA	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector−Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD436 BD438 BD440 BD442	$V_{(BR)CEO}$	32 45 60 80	− − − −	− − − −	Vdc
Collector−Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD436 BD438 BD440 BD442	$V_{(BR)CBO}$	32 45 60 80	− − − −	− − − −	Vdc
Emitter−Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		$V_{(BR)EBO}$	5.0	−	−	Vdc
Collector Cutoff Current (V_{CB} = 32 V, I_E = 0) (V_{CB} = 45 V, I_E = 0) (V_{CB} = 60 V, I_E = 0) (V_{CB} = 80 V, I_E = 0)	 BD436 BD438 BD440 BD442	I_{CBO}	 − − − −	 − − − −	 0.1 0.1 0.1 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 V)		I_{EBO}	−	−	1.0	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5.0 V)	BD436 BD438 BD440 BD442	h_{FE}	40 30 20 15	− − − −	− − − −	
DC Current Gain (I_C = 500 mA, V_{CE} = 1.0 V)	BD436 BD438 BD440 BD442	h_{FE}	85 85 40 40	− − − −	475 375 475 475	
DC Current Gain (I_C = 2.0 A, V_{CE} = 1.0 V)	BD436 BD438 BD440 BD442	h_{FE}	50 40 25 15	− − − −	− − − −	
Collector Saturation Voltage (I_C = 2.0 A, I_B = 0.2 A) (I_C = 3.0 A, I_B = 0.3 A)	 BD436 BD438 BD440 BD442	$V_{CE(sat)}$	 − − − −	 − − − −	 0.5 0.7 0.8 0.8	Vdc
Base−Emitter On Voltage (I_C = 2.0 A, V_{CE} = 1.0 V)	BD436/BD438 BD440/BD442	$V_{BE(ON)}$	− −	− −	1.1 1.5	Vdc
Current−Gain − Bandwidth Product (V_{CE} = 1.0 V, I_C = 250 mA, f = 1.0 MHz)		f_T	3.0	−	−	MHz

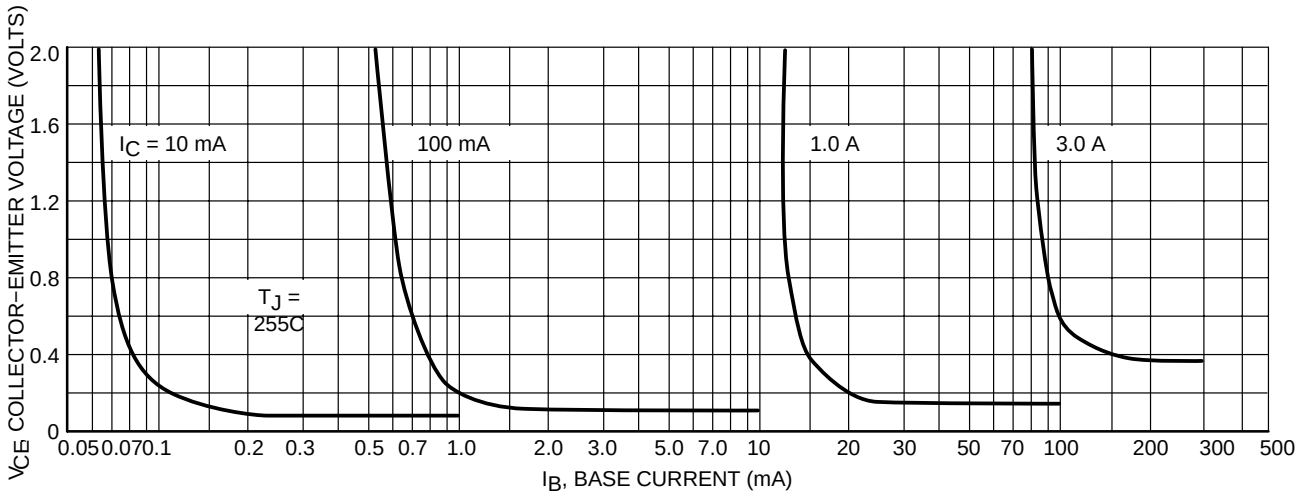


Figure 1. Collector Saturation Region

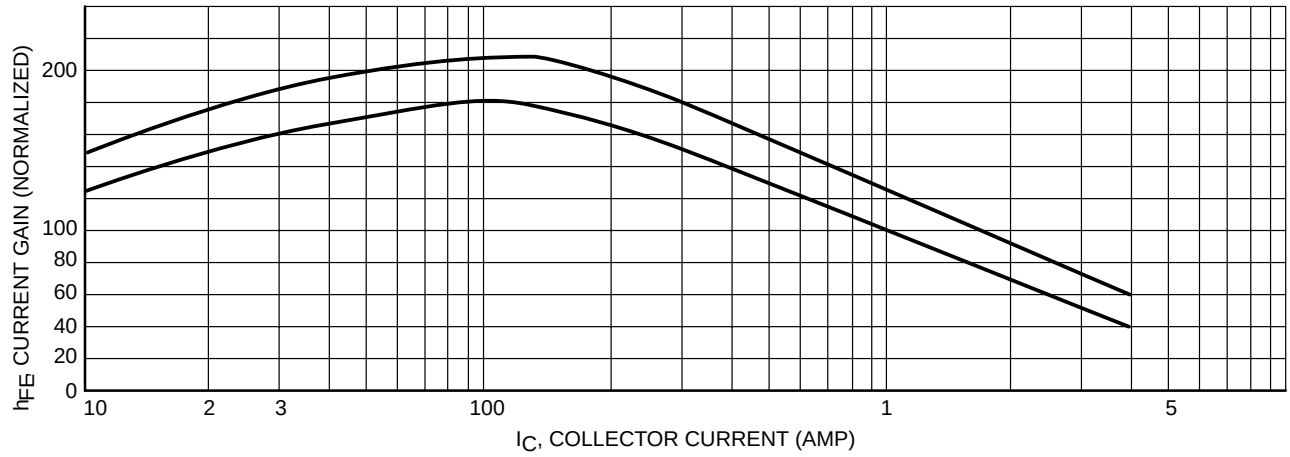


Figure 2. Current Gain

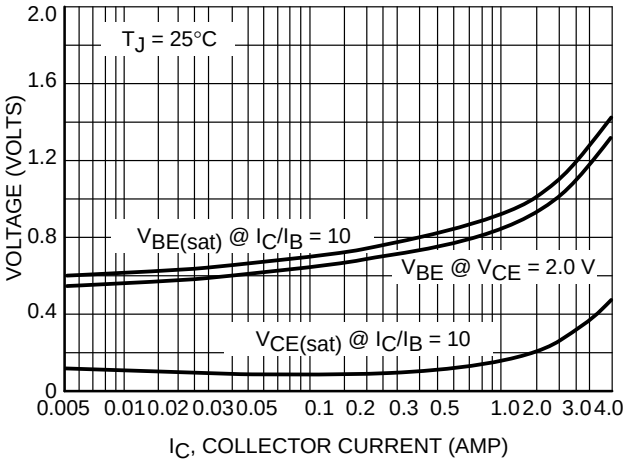


Figure 3. “On” Voltage

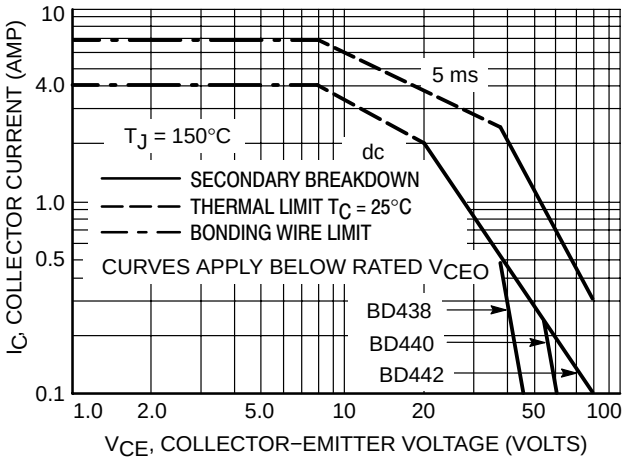


Figure 4. Active Region Safe Operating Area

BD675, BD675A, BD677, BD677, BD679A, BD681*

Preferred Device

Plastic Medium-Power Silicon NPN Darlingtons

This series of plastic, medium−power silicon NPN Darlington transistors can be used as output devices in complementary general−purpose amplifier applications.

Features

- Pb−Free Package is Available*
- High DC Current Gain:
  h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	BD675, A BD677, A BD679, A BD681	V_{CEO}	45 60 80 100	Vdc
Collector−Base Voltage	BD675, A BD677, A BD679, A BD681	V_{CBO}	45 60 80 100	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	40 0.32	W W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	3.13	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

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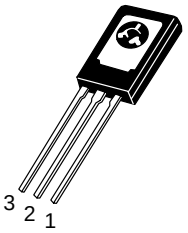
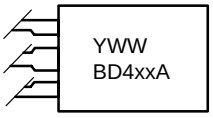
4.0 AMPERES
POWER TRANSISTORS
NPN SILICON
60, 80, 100 VOLTS
40 WATTS



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



xx = 75, 77, 79, 81
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
BD675	TO−225AA	500 Units/Box
BD675A	TO−225AA	500 Units/Box
BD677	TO−225AA	500 Units/Rail
BD677A	TO−225AA	500 Units/Box
BD679	TO−225AA	500 Units/Box
BD679A	TO−225AA	500 Units/Box
BD679AG	TO−225AA (Pb−Free)	500 Units/Box
BD681	TO−225AA	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

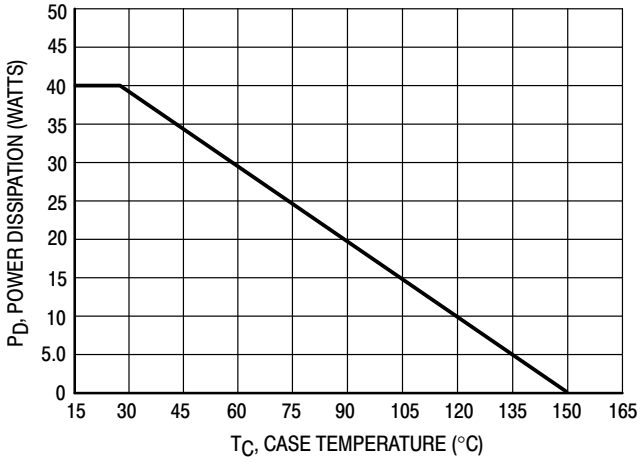


Figure 1. Power Temperature Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage, (Note 2) (I_C = 50 mAdc, I_B = 0)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	− − − −	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	−	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100'C)		I_{CBO}	 − −	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Currert Gain, (Note 2) (I_C = 1.5 Adc,V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD675, 677, 679, 681 BD675A, 677A, 679A	h_{FE}	 750 750	 − −	−
Collector−Emitter Saturation Voltage, (Note 2) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD677, 679, 681 BD675A, 677A, 679A	$V_{CE(sat)}$	 − −	 2.5 2.8	Vdc
Base−Emitter On Voltage, (Note 2) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3 0 Vdc)	 BD677, 679, 681 BD675A, 677A, 679A	$V_{BE(on)}$	 − −	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	−	−

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

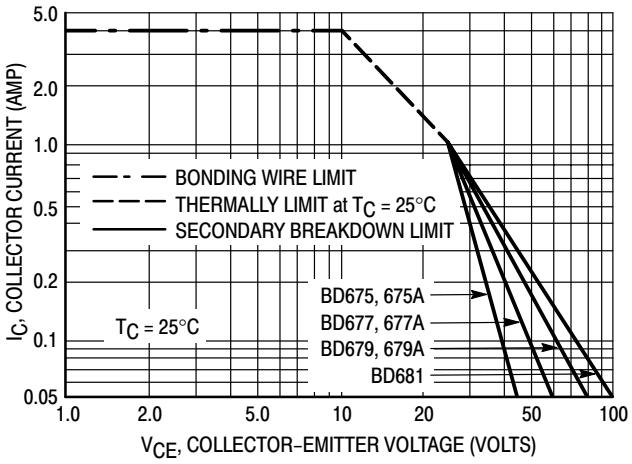


Figure 2. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

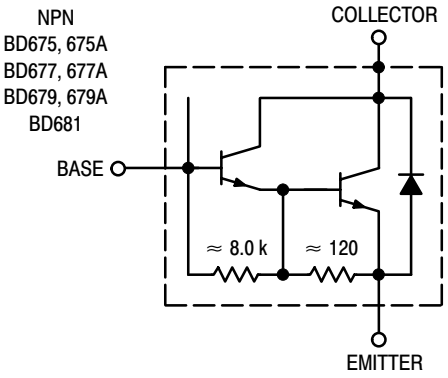


Figure 3. Darlington Circuit Schematic

BD676, BD676A, BD678, BD678A, BD680, BD680A, BD682

Plastic Medium-Power Silicon PNP Darlingtons

This series of plastic, medium−power silicon PNP Darlington transistors can be used as output devices in complementary general−purpose amplifier applications.

Features

- Pb−Free Package is Available*
- High DC Current Gain − h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BD676, BD676A BD678, BD678A BD680, BD680A BD682	V_{CEO}	 45 60 80 100	Vdc
Collector-Base Voltage BD676, BD676A BD678, BD678A BD680, BD680A BD682	V_{CB}	 45 60 80 100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	4.0	Adc
Base Current	I_B	0.1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 0.32	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.13	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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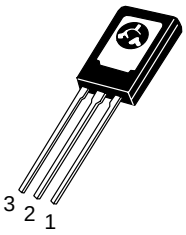
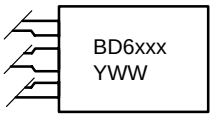
4.0 A DARLINGTON POWER TRANSISTORS PNP SILICON 45, 60, 80, 100 V, 40 W



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



xxx = 76, 76A, 78, 78A, 80, 80A or 82
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 180 of this data sheet.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (Note 1) (I_C = 50 mAdc, I_B = 0)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	− − − −	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	−	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	 − −	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD676, 678, 680, 682 BD676A, 678A, 680A	h_{FE}	 750 750	 − −	
Collector−Emitter Saturation Voltage (Note 1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD678, 680, 682 BD676A, 678A, 680A	$V_{CE(sat)}$	 − −	 2.5 2.8	Vdc
Base−Emitter On Voltage (Note 1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD678, 680, 682 BD676A, 678A, 680A	$V_{BE(on)}$	 − −	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	−	−

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

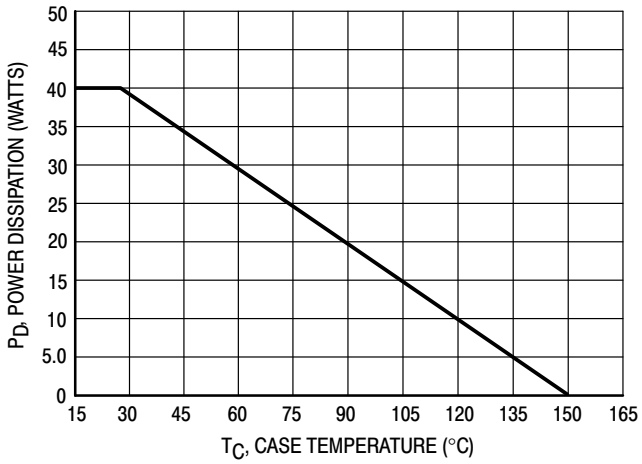


Figure 1. Power Temperature Derating

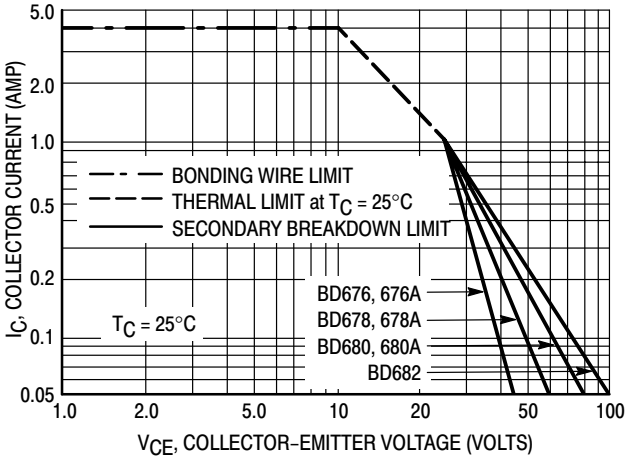


Figure 2. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

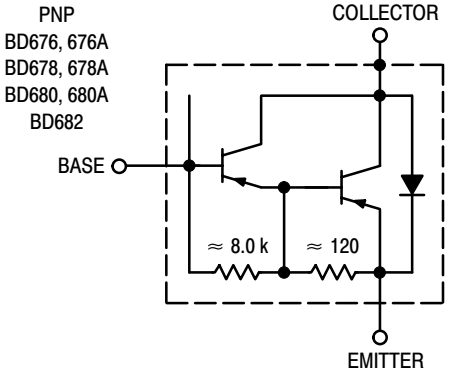


Figure 3. Darlington Circuit Schematic

ORDERING INFORMATION

Device	Package	Shipping†
BD676	TO−225AA	500 Units / Box
BD676G	TO−225AA (Pb−Free)	
BD676A	TO−225AA	500 Units / Box
BD678	TO−225AA	500 Units / Box
BD678A	TO−225AA	
BD680	TO−225AA	500 Units / Box
BD680A	TO−225AA	
BD682	TO−225AA	500 Units / Box
BD682G	TO−225AA (Pb−Free)	
BD682T	TO−225AA	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

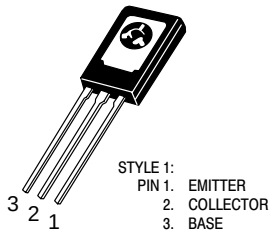
Complementary Plastic Silicon Power Transistors

. . . designed for lower power audio amplifier and low current, high−speed switching applications.

- Low Collector−Emitter Sustaining Voltage — $V_{CEO(sus)}$ 60 Vdc (Min) — BD787, BD788
- High Current−Gain — Bandwidth Product — f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Collector−Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

NPN
BD787
PNP
BD788

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
15 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD787 BD788	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

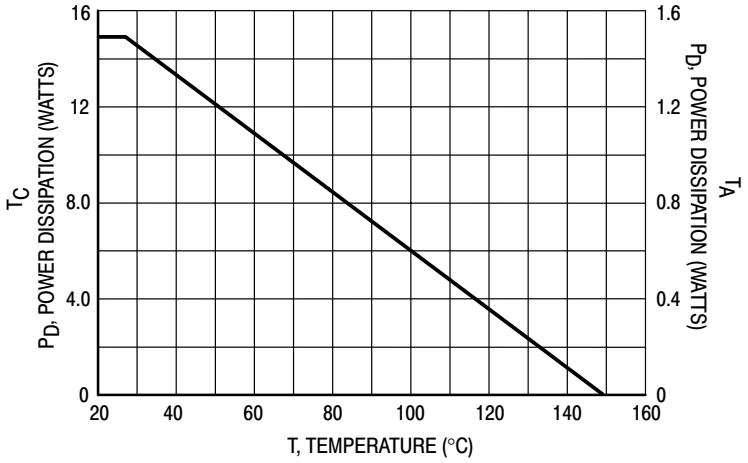


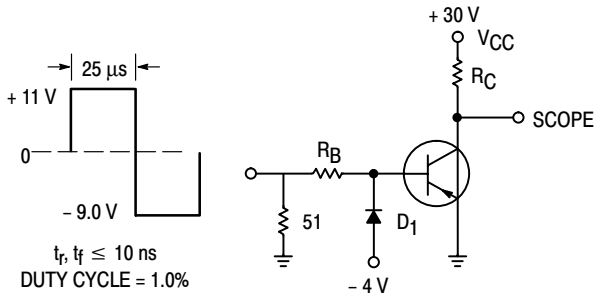
Figure 1. Power Derating

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)		$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0)		I_{CEO}	—	100	μAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	 — —	 1.0 0.1	 μAdc mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 40 25 20 5.0	 250 — — —	—
Collector−Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)		$V_{CE(sat)}$	 — — — —	 0.4 0.6 0.8 2.5	Vdc
Base−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	2.0	Vdc
Base−Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0) (f = 0.1 MHz)	 BD787 BD788	C_{ob}	 — —	 50 70	pF
Small−Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	—	—

*Indicates JEDEC Registered Data

(1) Pulse Test; Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

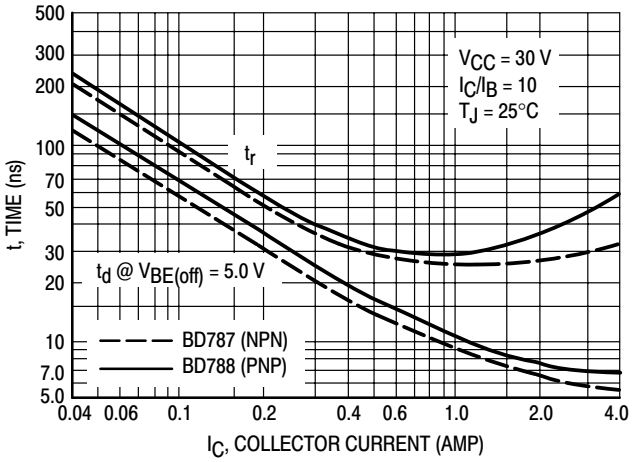


Figure 3. Turn−On Time

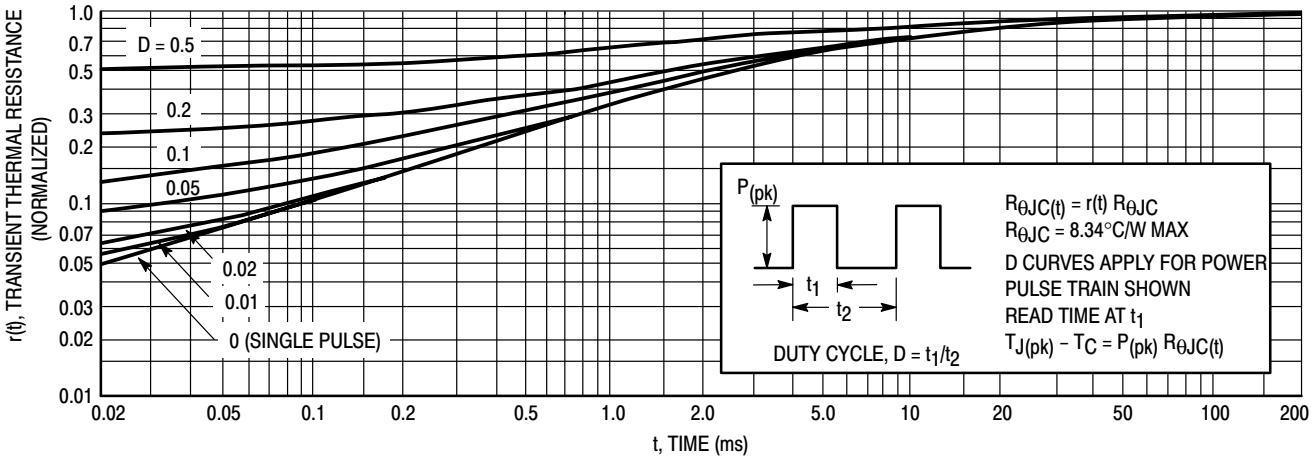


Figure 4. Thermal Response

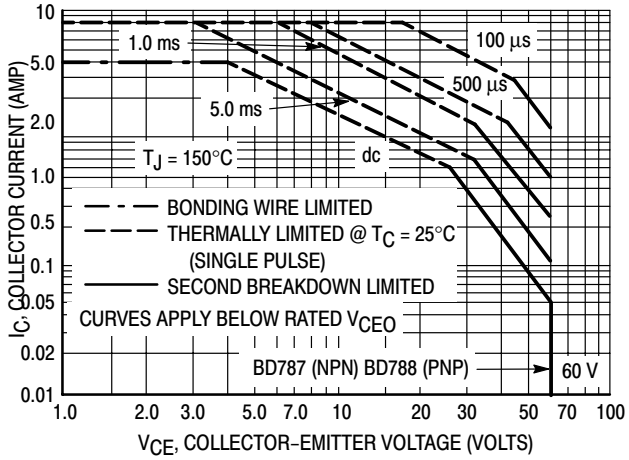


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

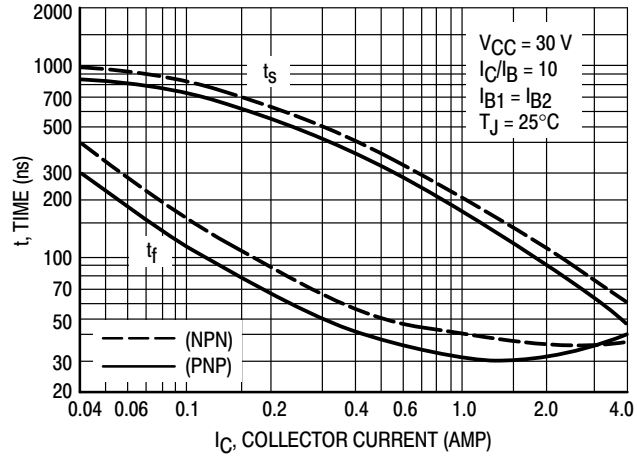


Figure 6. Turn−Off Time

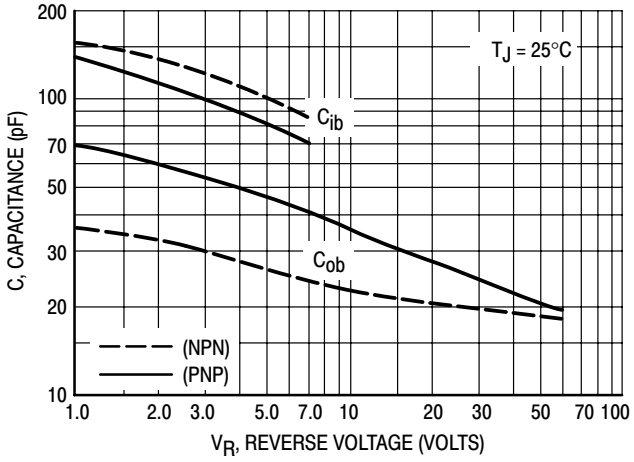
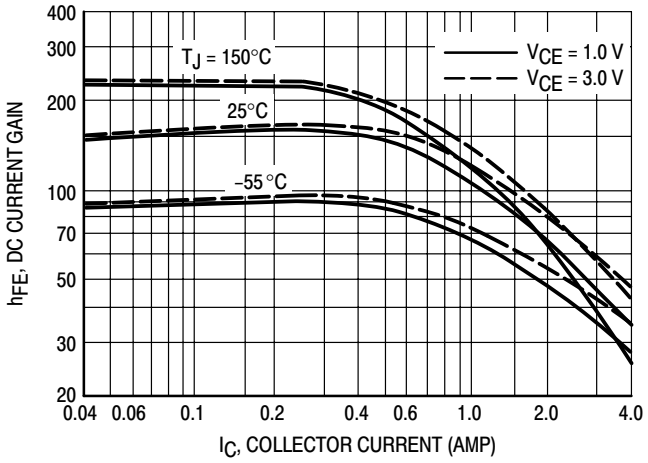


Figure 7. Capacitance

NPN
BD787



NPN
BD788

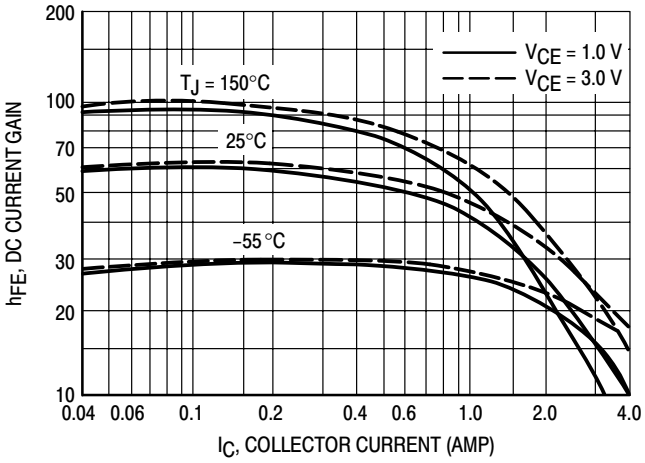
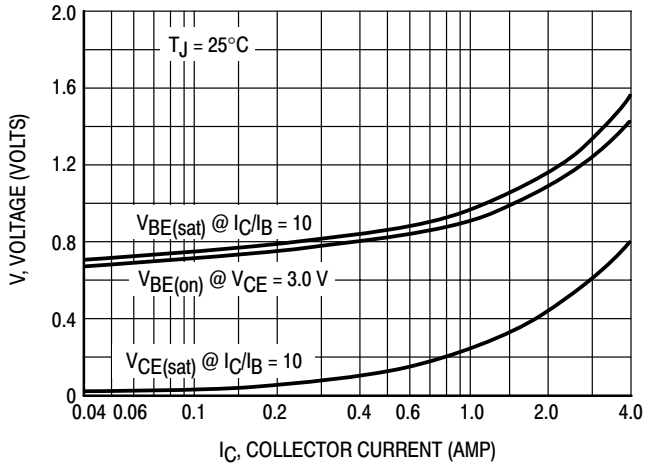


Figure 8. DC Current Gain



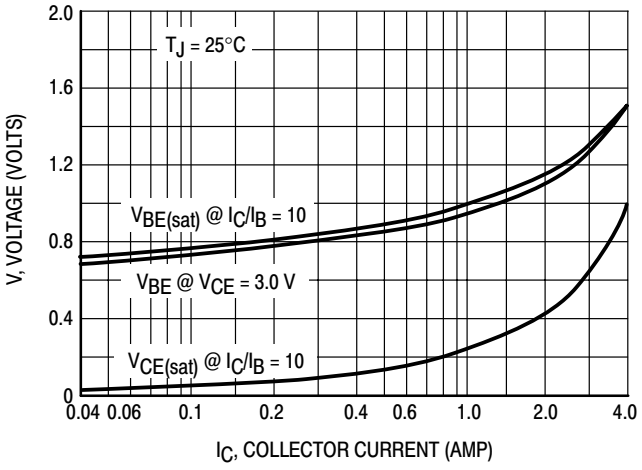


Figure 9. “On” Voltages

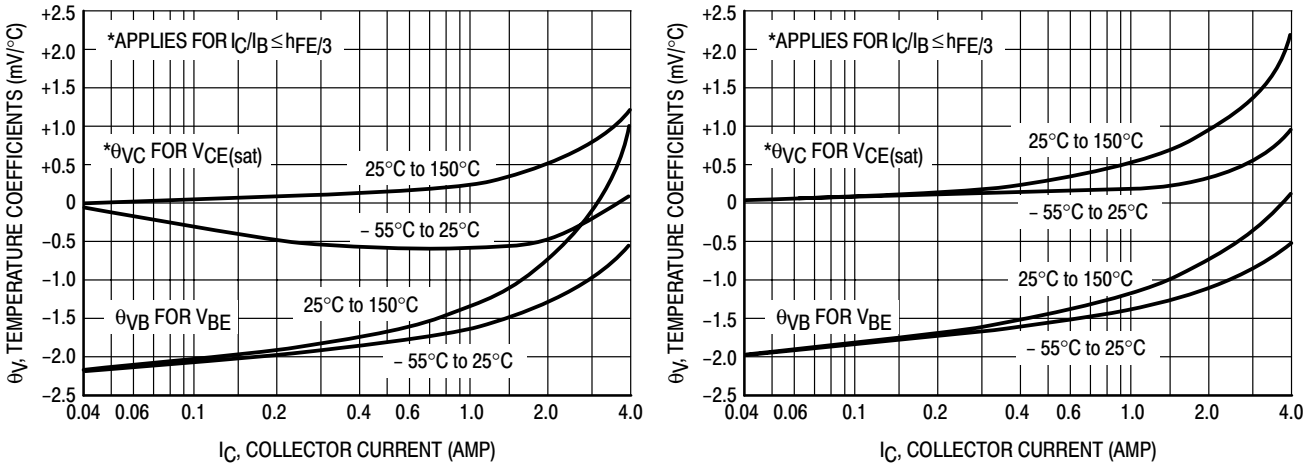


Figure 10. Temperature Coefficients

Plastic High Power Silicon Transistor

NPN
BD809
PNP
BD810

10 AMPERE
POWER TRANSISTORS
PNP SILICON
60, 80 VOLTS
90 WATTS

. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

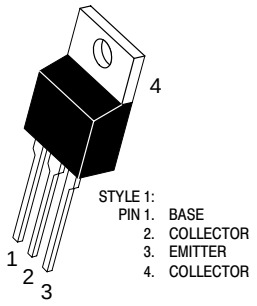
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 2.0 Adc

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W



CASE 221A−09
TO−220AB

April, 2002 − Rev. 1
Publication Order Number:
BD809/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	 80	— —	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	 —	 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
DC Current Gain (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 4.0 A, V_{CE} = 2.0 V)	h_{FE}	 30 15	 — —	
Collector−Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	—	1.1	Vdc
Base−Emitter On Voltage* (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
Current−Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	1.5	—	MHz

*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

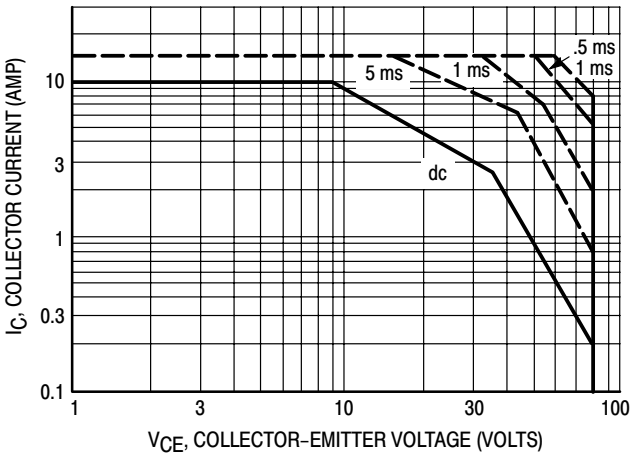


Figure 1. Active Region DC Safe Operating Area (see Note 1)

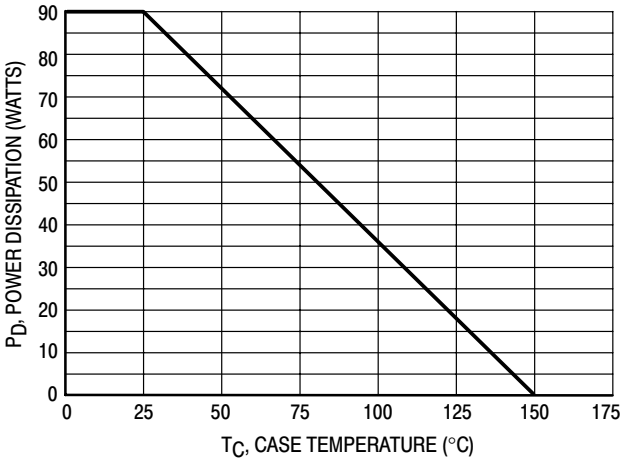


Figure 2. Power−Temperature Derating Curve

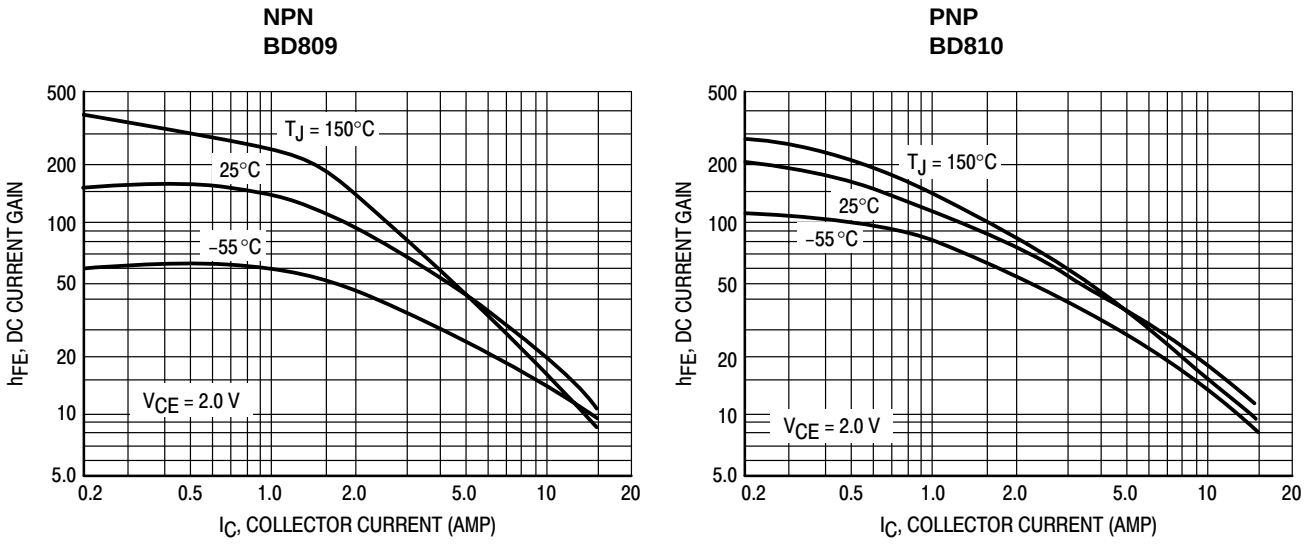


Figure 3. DC Current Gain

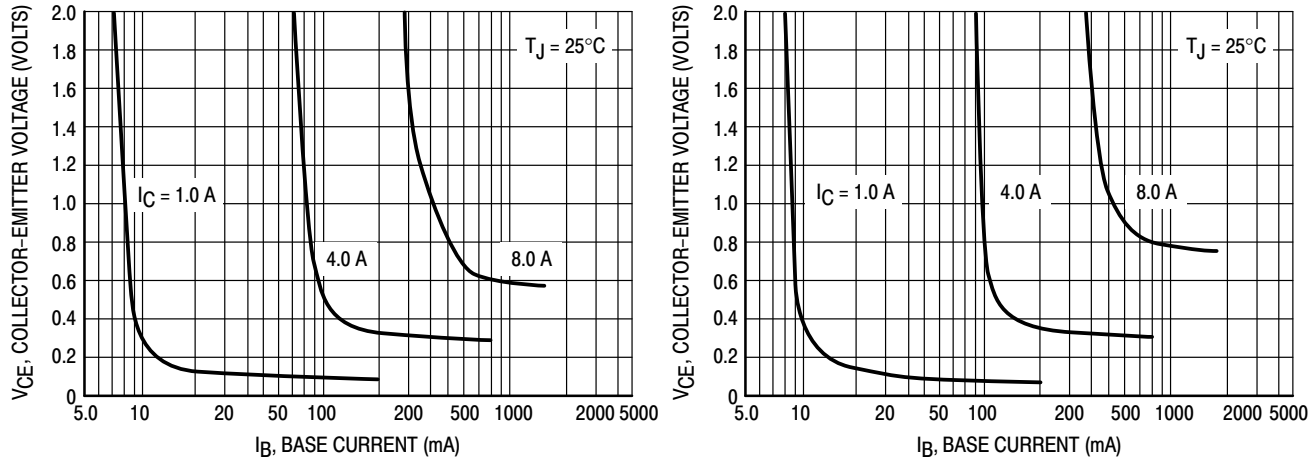


Figure 4. Collector Saturation Region

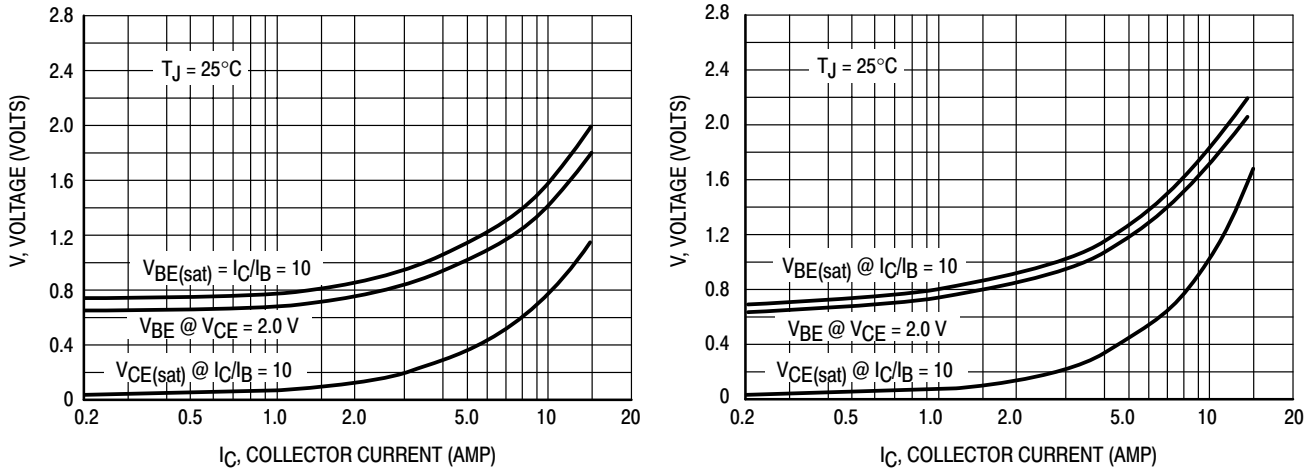


Figure 5. “On” Voltages

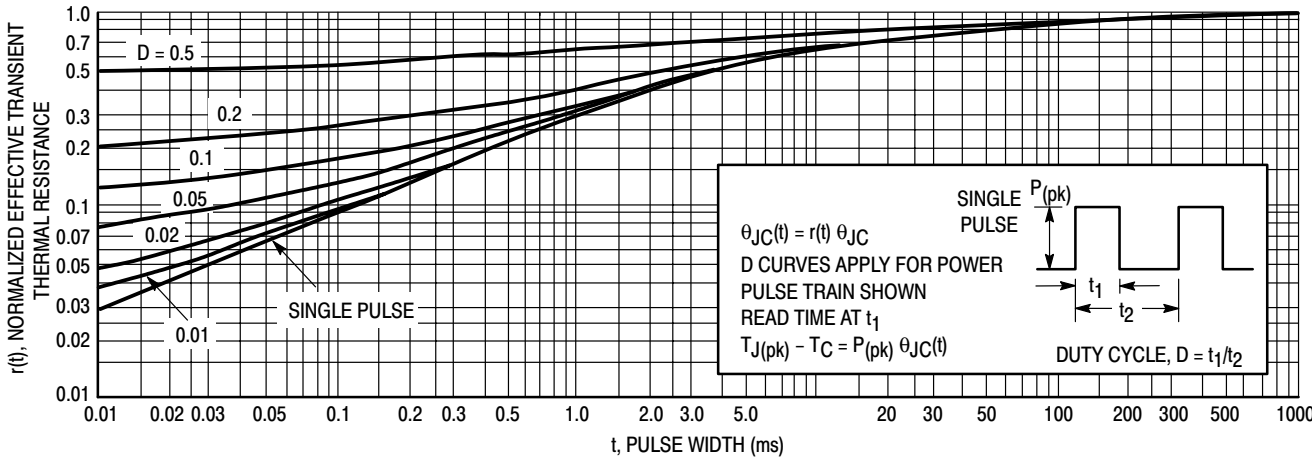


Figure 6. Thermal Response

Note 1:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

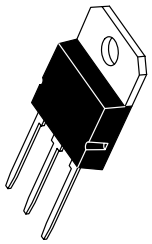
Complementary Silicon Plastic Power Darlingtons

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
  HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built−in Base Emitter Shunt Resistors

NPN
BDV65B
PNP
BDV64B

DARLINGTONS
10 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60−80−100−120 VOLTS
125 WATTS



CASE 340D−02
SOT 93, TO−218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	10 20	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

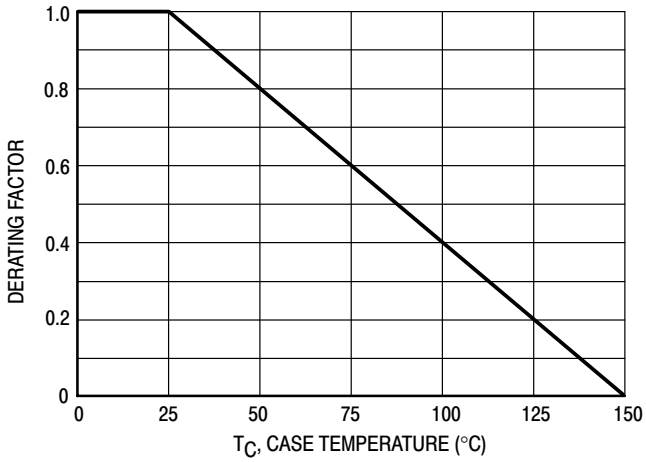


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.4	mAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	—	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	1000	—	—
Collector−Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.02 Adc)	$V_{CE(sat)}$	—	2.0	Vdc
Base−Emitter Saturation Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc

NPN

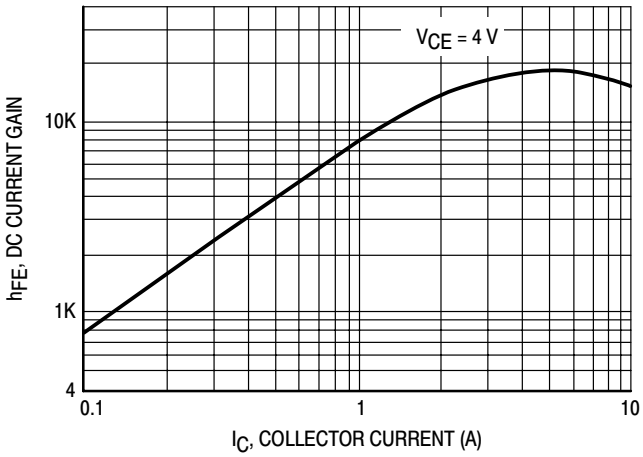


Figure 2. DC Current Gain

PNP

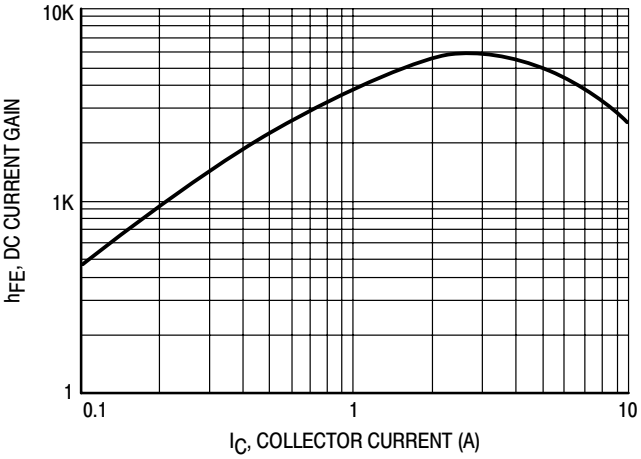


Figure 3. DC Current Gain

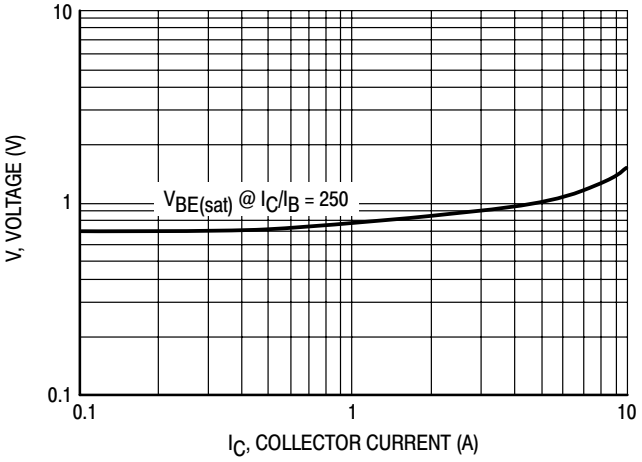


Figure 4. "On" Voltages

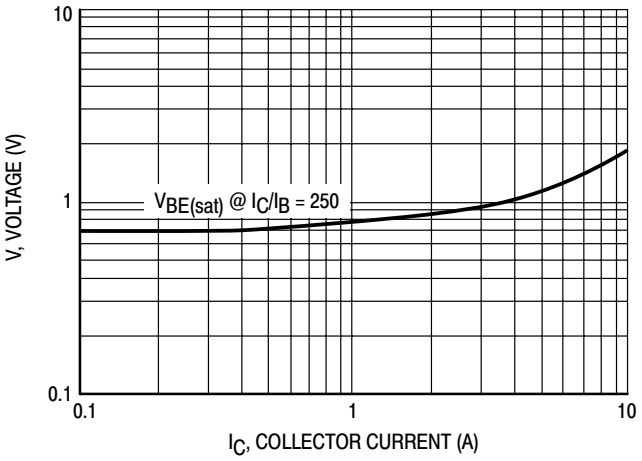


Figure 5. "On" Voltages

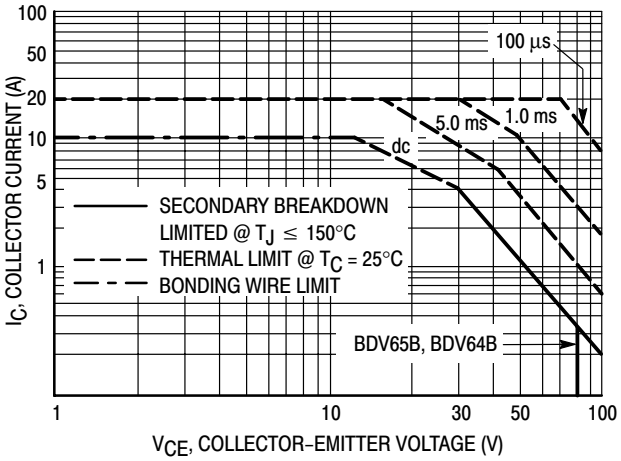


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

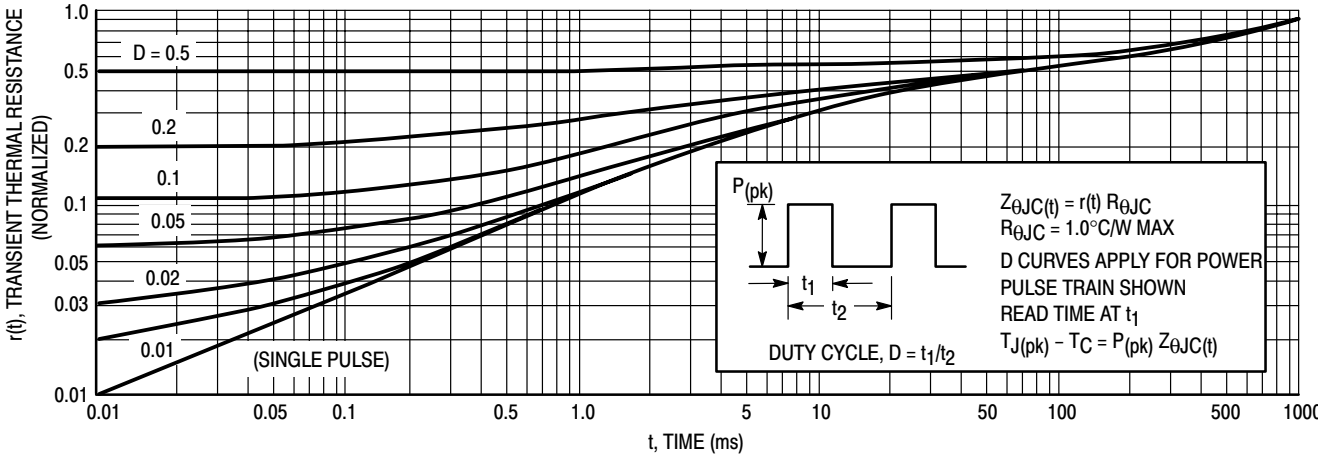


Figure 7. Thermal Response

BDW42* - NPN, BDW46, BDW47* - PNP

Preferred Device

Darlington Complementary Silicon Power Transistors

This series of plastic, medium−power silicon NPN and PNP Darlington transistors are designed for general purpose and low speed switching applications.

Features

- Pb−Free Package is Available**
- High DC Current Gain − h_{FE} = 2500 (typ) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 80 Vdc (min) − BDW46
  100 Vdc (min.) − BDW42/BDW47
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.0 Vdc (max) @ I_C = 5.0 Adc
  3.0 Vdc (max) @ I_C = 10.0 Adc
- Monolithic Construction with Built−In Base Emitter Shunt resistors
- TO−220AB Compact Package

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BDW46 BDW42, BDW47	V_{CEO}	 80 100	Vdc
Collector-Base Voltage BDW46 BDW42, BDW47	V_{CB}	 80 100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	15	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 85 0.68	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

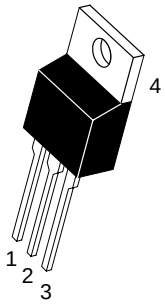
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.47	°C/W

**For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

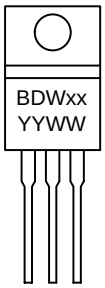
http://onsemi.com

15 A DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 80−100 V, 85 W



TO−220AB
CASE 221A
STYLE 1

MARKING DIAGRAM



xx = 42, 46 or 47
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
BDW42	TO−220AB	50 Units/Rail
BDW46	TO−220AB	50 Units/Rail
BDW47	TO−220AB	50 Units/Rail
BDW47G	TO−220AB (Pb−Free)	50 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

***Preferred** devices are ON Semiconductor recommended choices for future use and best overall value

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage (Note 2)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	BDW46		80	−	
	BDW42/BDW47		100	−	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	BDW46		−	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	BDW42/BDW47		−	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 80 Vdc, I_E = 0)	BDW46		−	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	BDW42/BDW47		−	1.0	
Emitter Cutoff Current		I_{EBO}	−	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (Note 2)					
DC Current Gain		h_{FE}			
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			1000	−	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			250	−	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 10 mAdc)			−	2.0	
(I_C = 10 Adc, I_B = 50 mAdc)			−	3.0	
Base−Emitter On Voltage		$V_{BE(on)}$	−	3.0	Vdc
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)					
SECOND BREAKDOWN (Note 3)					
Second Breakdown Collector		$I_{S/b}$			Adc
Current with Base Forward Biased					
BDW42	V_{CE} = 28.4 Vdc		3.0	−	
	V_{CE} = 40 Vdc		1.2	−	
BDW46/BDW47	V_{CE} = 22.5 Vdc		3.8	−	
	V_{CE} = 36 Vdc		1.2	−	
DYNAMIC CHARACTERISTICS					
Magnitude of common emitter small signal short circuit current transfer ratio		f_T	4.0	−	MHz
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDW42		−	200	
	BDW46/BDW47		−	300	
Small−Signal Current Gain		h_{fe}	300	−	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)					

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
3. Pulse Test non repetitive: Pulse Width = 250 ms.

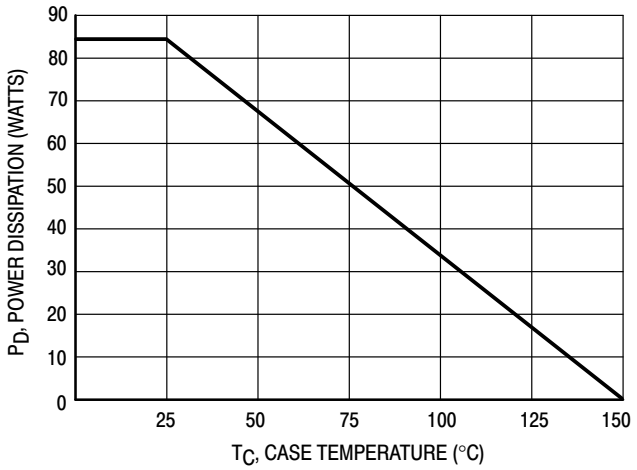


Figure 1. Power Temperature Derating Curve

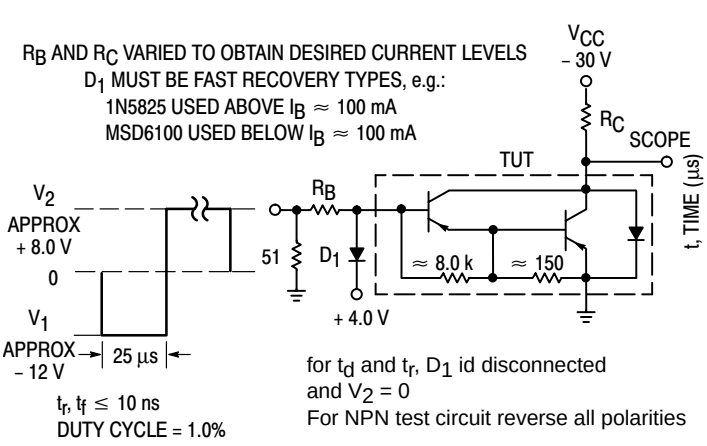


Figure 2. Switching Times Test Circuit

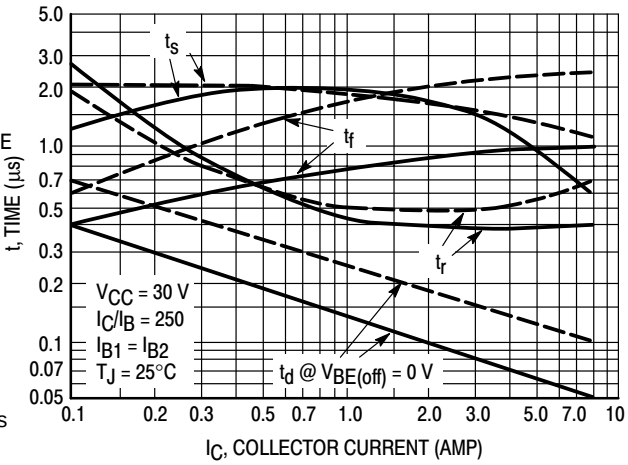


Figure 3. Switching Times

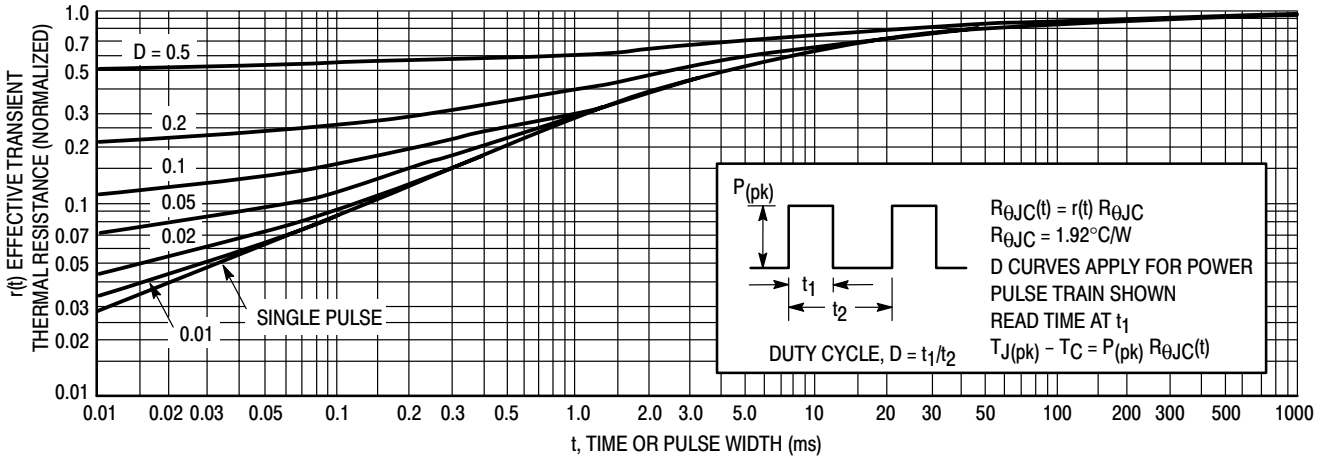


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

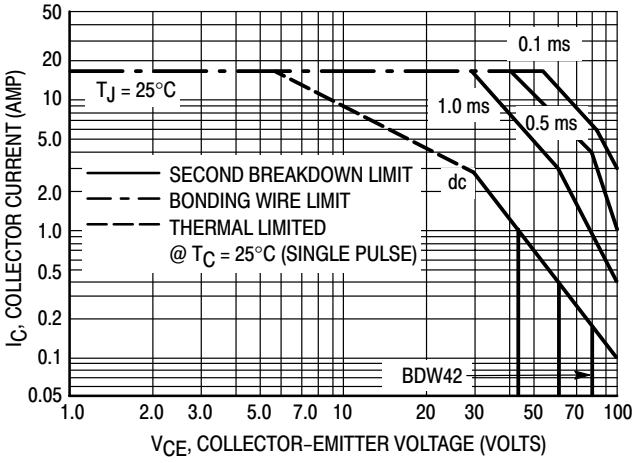


Figure 5. BDW42

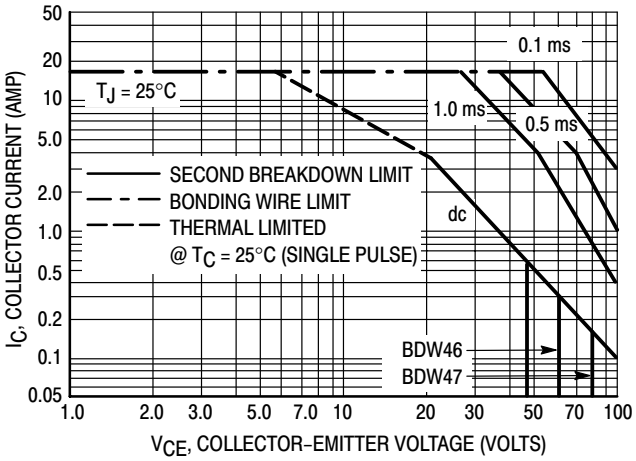


Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 and 6 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

*Linear extrapolation

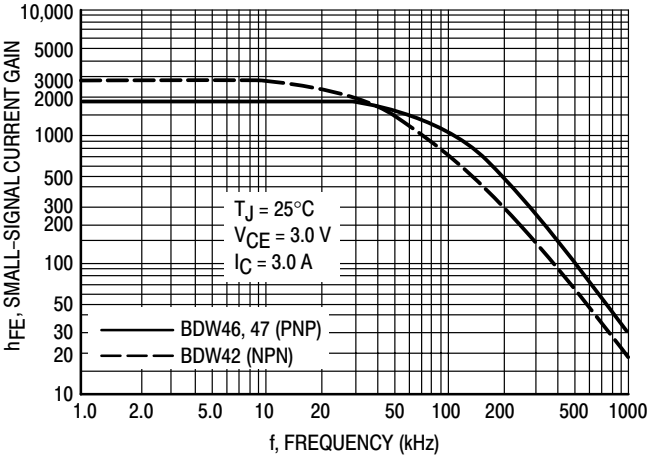


Figure 7. Small−Signal Current Gain

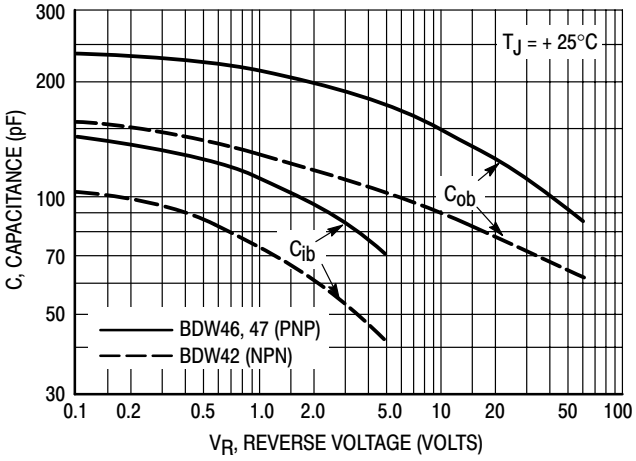
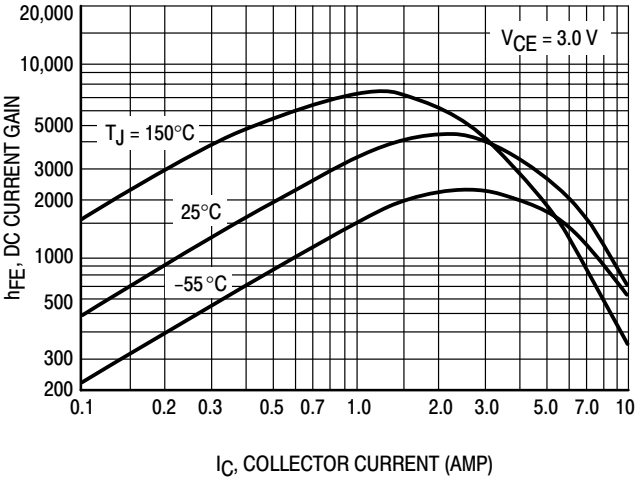


Figure 8. Capacitance

BDW42 (NPN)



BDW46, 47 (PNP)

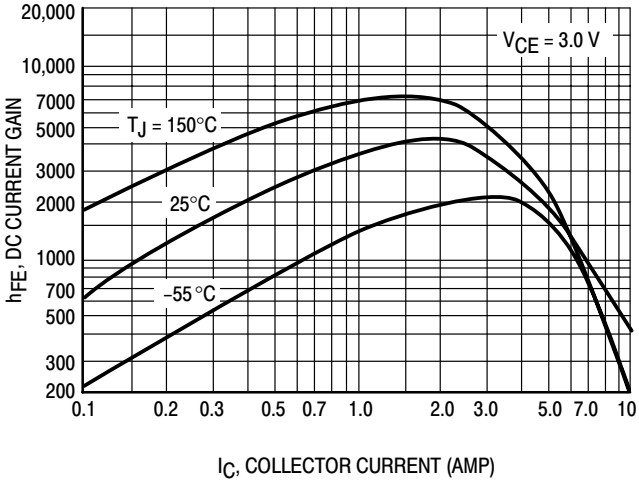
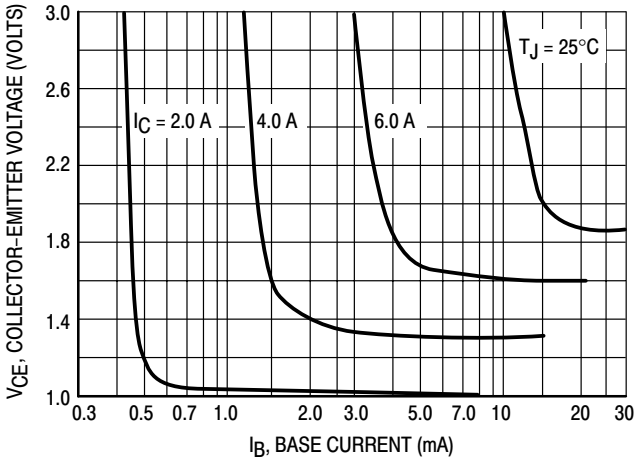


Figure 9. DC Current Gain



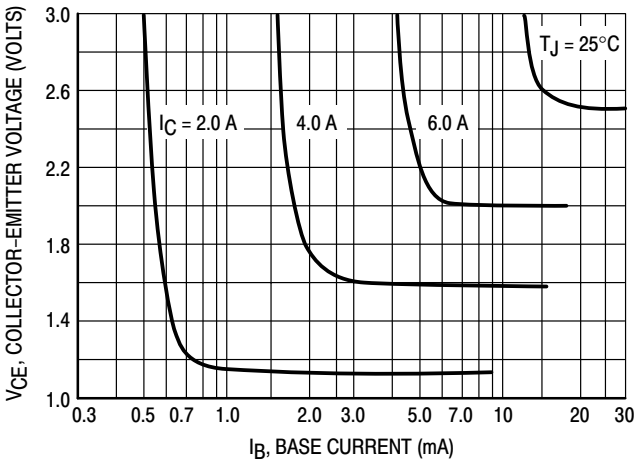
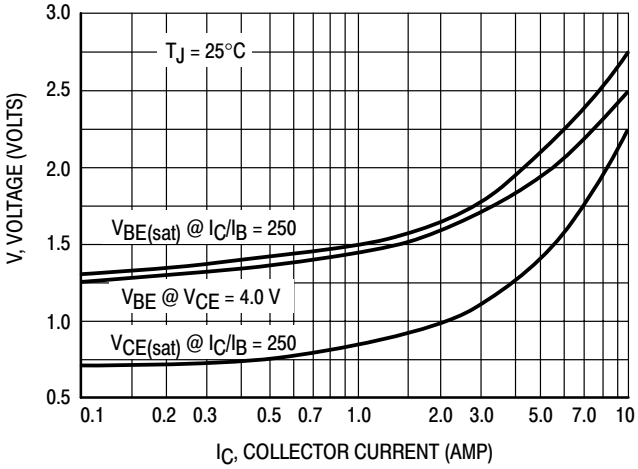


Figure 10. Collector Saturation Region



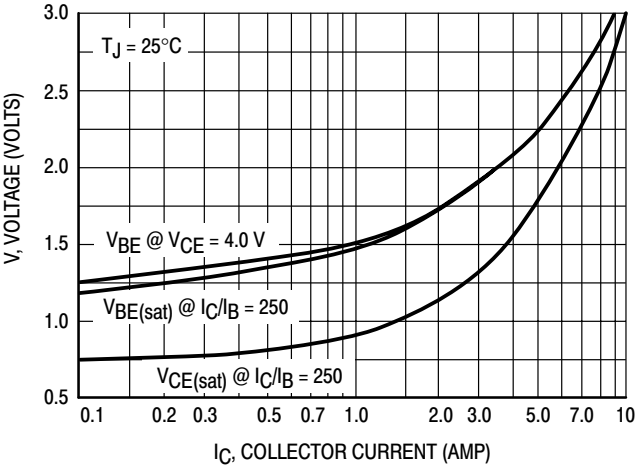


Figure 11. “On” Voltages

BDW42 (NPN) **BDW46, 47 (PNP)**

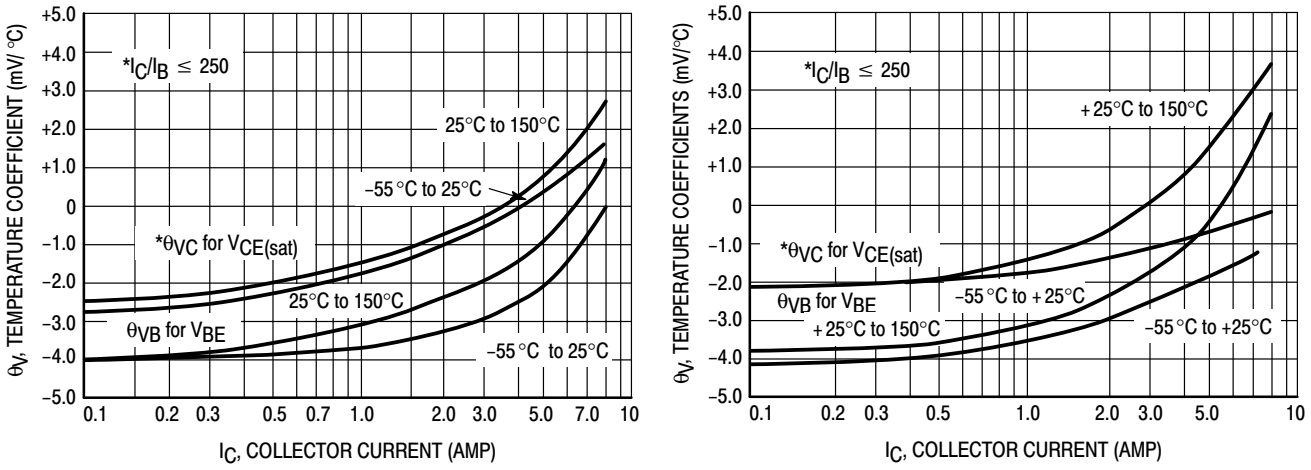


Figure 12. Temperature Coefficients

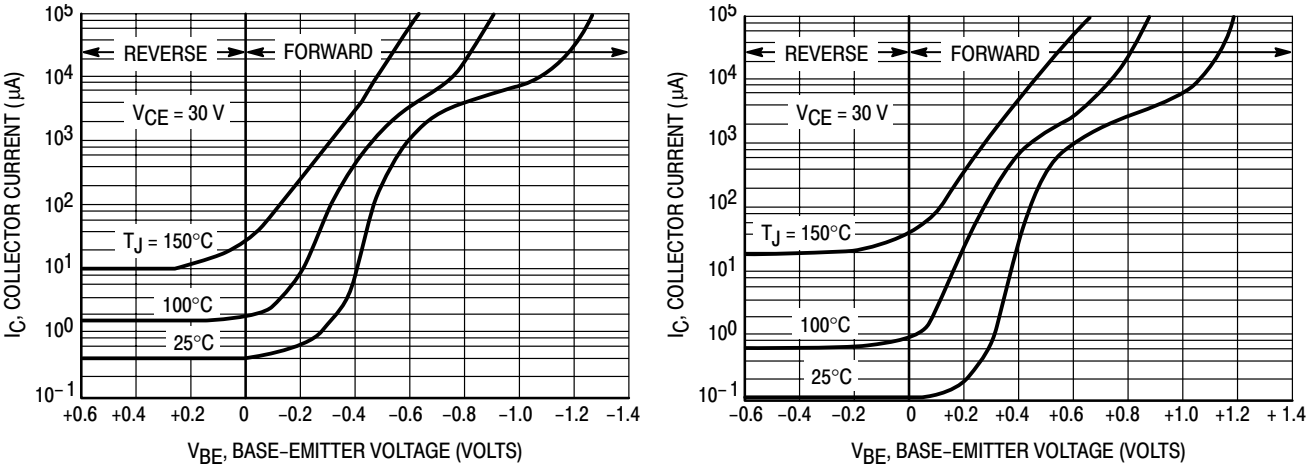


Figure 13. Collector Cut−Off Region

Figure 14. Darlington Schematic

Darlington Complementary Silicon Power Transistors

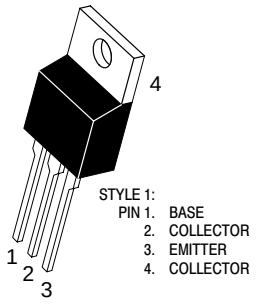
. . . designed for general purpose and low speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (typ.) at I_C = 4.0
- Collector−Emitter Sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDX33B, 34B
  100 Vdc (min.) — BDX33C, 34C
- Low Collector−Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max.) at I_C = 3.0 Adc — BDX33B, 33C/34B, 34C
- Monolithic Construction with Build−In Base−Emitter Shunt resistors
- TO−220AB Compact Package

NPN
BDX33B
BDX33C*
PNP
BDX34B
BDX34C*

***ON Semiconductor Preferred Device**

DARLINGTON
10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80−100 VOLTS
70 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector−Emitter Voltage	V_{CEO}	80	100	Vdc
Collector−Base Voltage	V_{CB}	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15		Adc
Base Current	I_B	0.25		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 70 0.56		 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

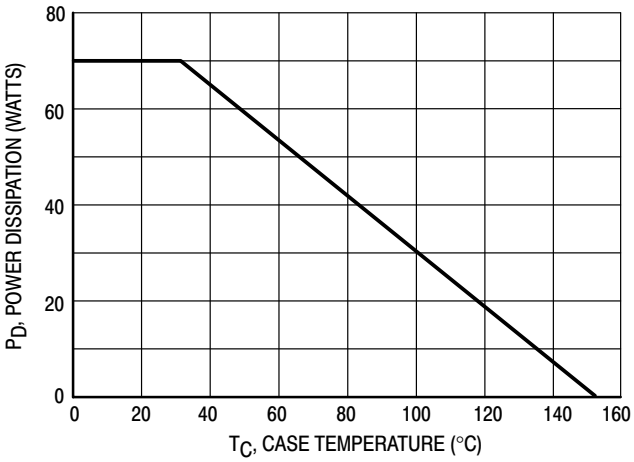


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector−Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)	BDX33B/BDX34B BDX33C/BDX33C	$V_{CER(sus)}$	 80 100	 — —	Vdc
Collector−Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEX(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 1/2 rated V_{CEO}, I_B = 0)	T_C = 25°C T_C = 100°C	I_{CEO}	 — —	 0.5 10	mAdc
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)	T_C = 25°C T_C = 100°C	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	h_{FE}	750	—	—
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc)	BDX33B, 33C/34B, 34C	$V_{CE(sat)}$	—	2.5	Vdc
Base−Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	$V_{BE(on)}$	—	2.5	Vdc
Diode Forward Voltage (I_C = 8.0 Adc)		V_F	—	4.0	Vdc

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
[2] Pulse Test non repetitive: Pulse Width = 0.25 s.

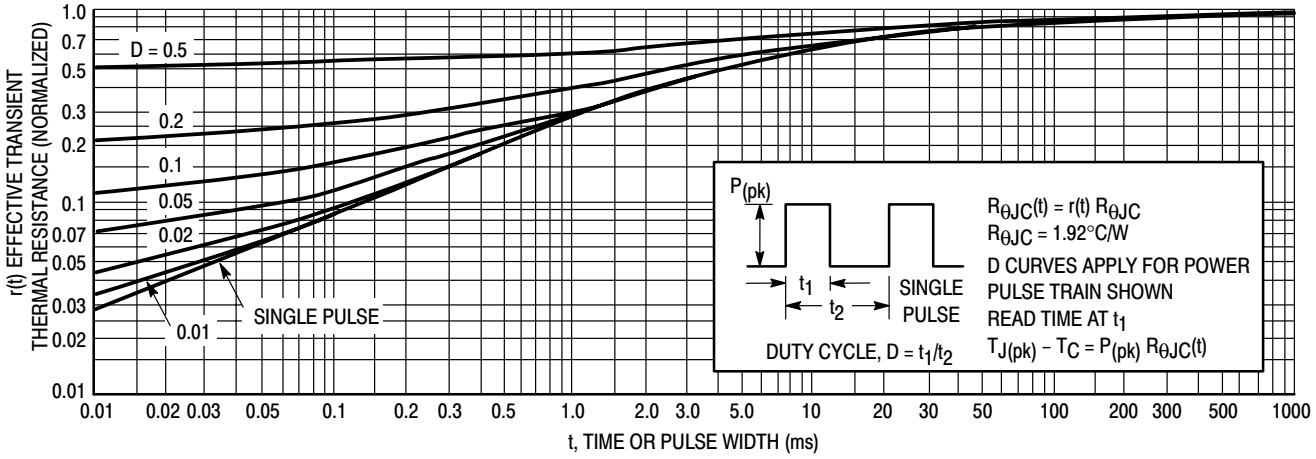


Figure 1. Thermal Response

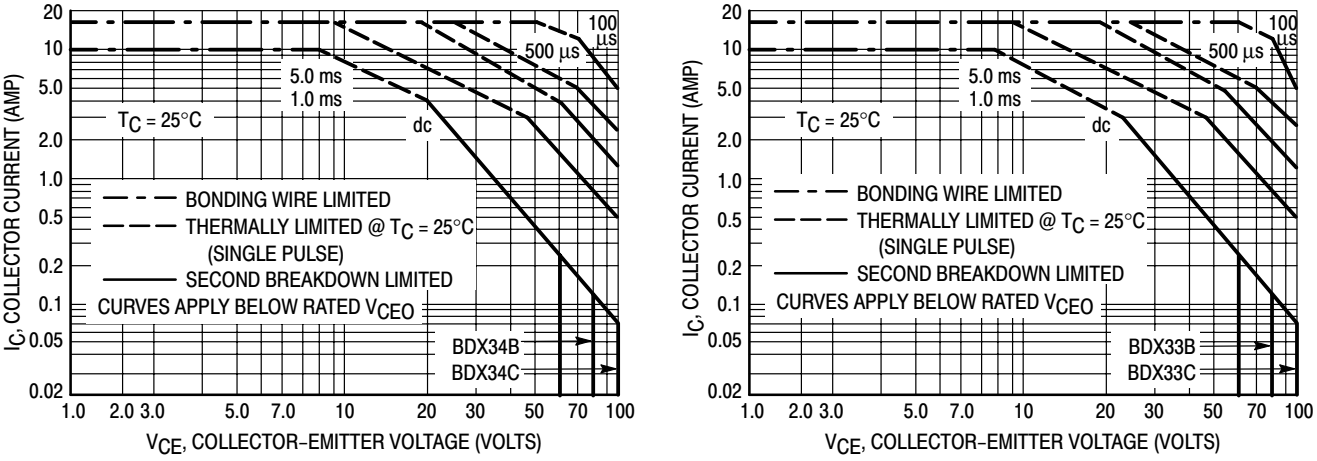


Figure 2. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ = 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

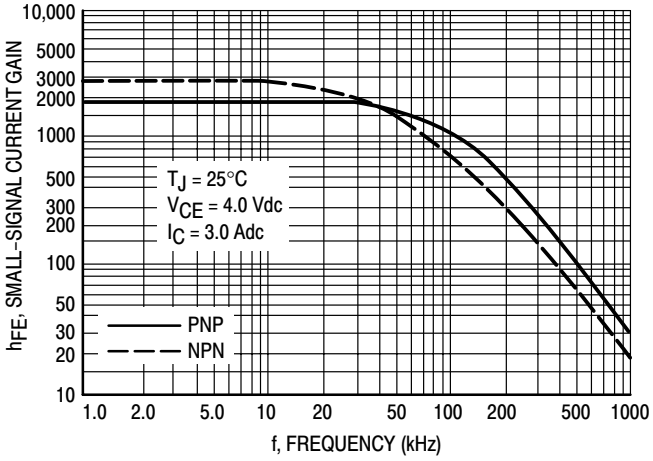


Figure 3. Small−Signal Current Gain

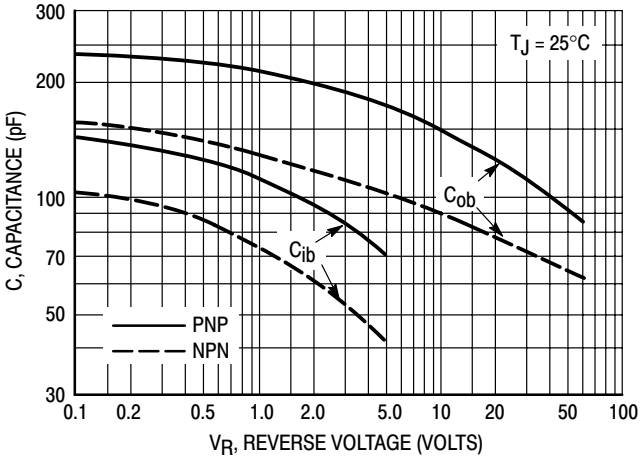


Figure 4. Capacitance

NPN
BDX33B, 33C

PNP
BDX34B, 34C

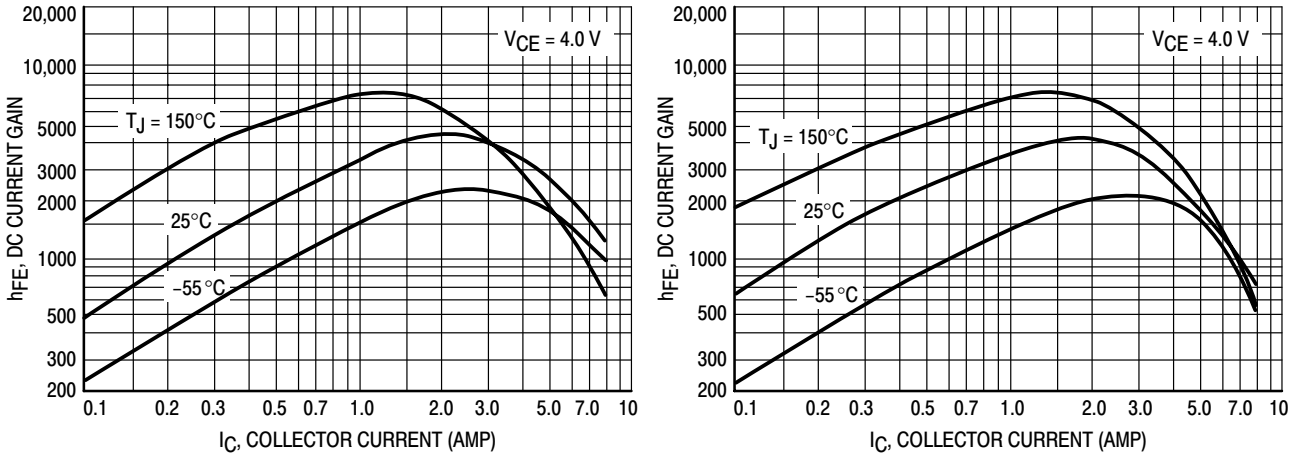


Figure 5. DC Current Gain

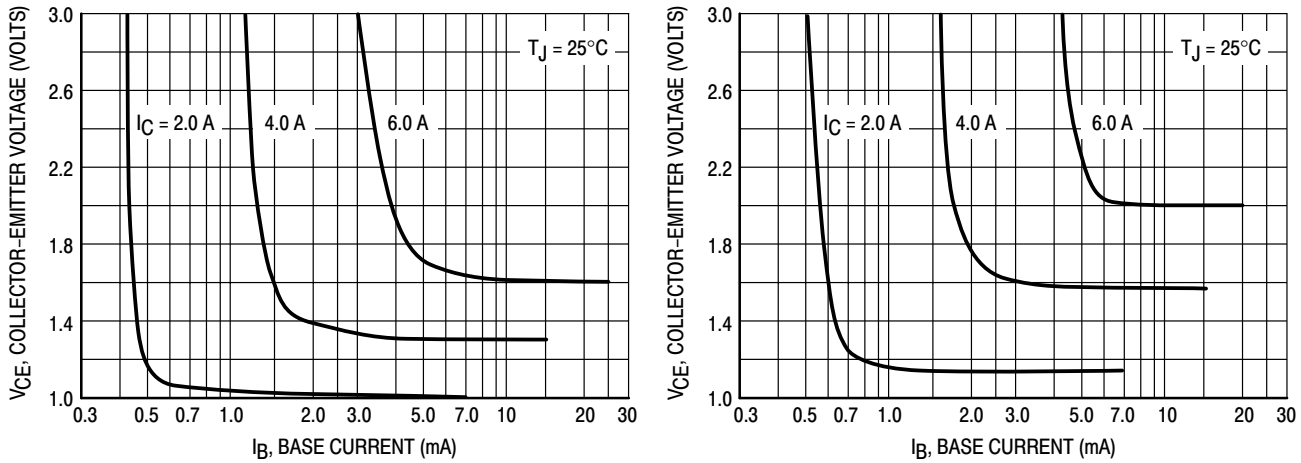


Figure 6. Collector Saturation Region

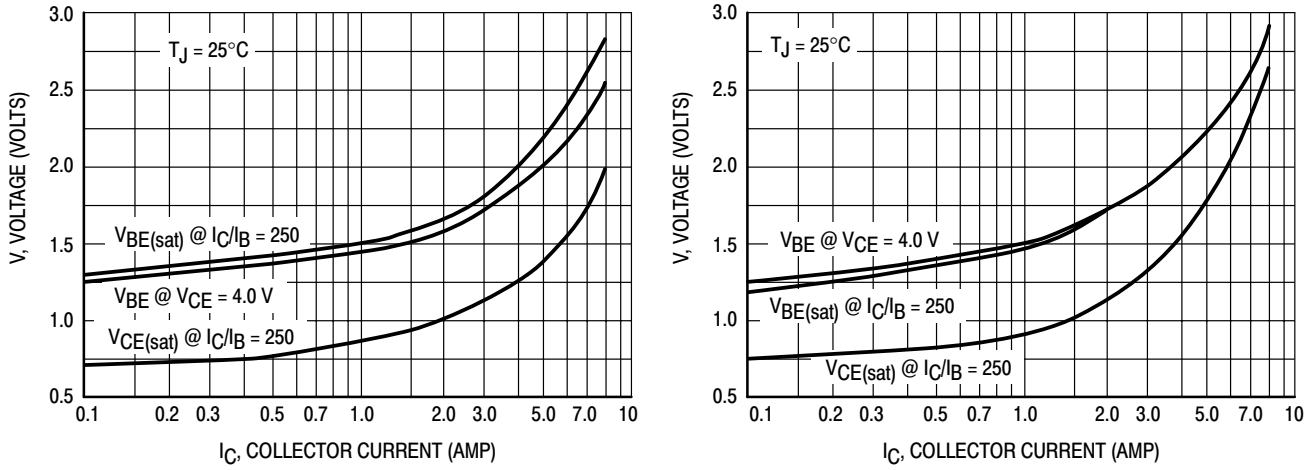


Figure 7. “On” Voltages

BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)

Plastic Medium-Power Complementary Silicon Transistors

ON Semiconductor®

http://onsemi.com

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
80−100 VOLTS
65 WATTS

. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector Emitter Sustaining Voltage − @ 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) − BDX53B, 54B
  = 100 Vdc (Min) − BDX53C, 54C
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package

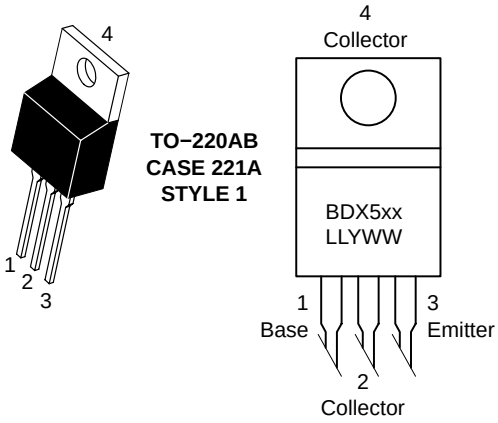
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage BDX53B, BDX54B BDX53C, BDX54C	V_{CEO}	 80 100	Vdc
Collector−Base Voltage BDX53B, BDX54B BDX53C, BDX54C	V_{CB}	 80 100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	8.0 12	Adc
Base Current	I_B	0.2	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.48	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

MARKING DIAGRAM & PIN ASSIGNMENT



BDX5xx	= Device Code
xx	= 3B, 3C, 4B, 4C
LL	= Location Code
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
BDX53B	TO−220AB	50 Units/Rail
BDX53C	TO−220AB	50 Units/Rail
BDX54B	TO−220AB	50 Units/Rail
BDX54C	TO−220AB	50 Units/Rail

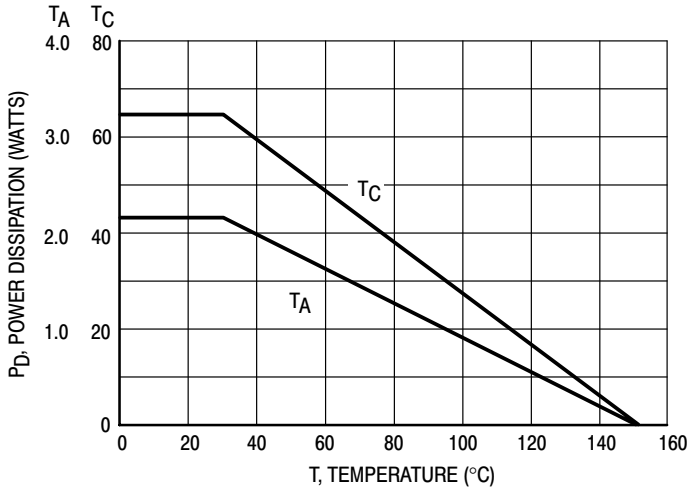


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	BDX53B, BDX54B		80	−	
	BDX53C, BDX54C		100	−	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	BDX53B, BDX54B		−	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	BDX53C, BDX54C		−	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 80 Vdc, I_E = 0)	BDX53B, BDX54B		−	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	BDX53C, BDX54C		−	0.2	
ON CHARACTERISTICS (Note 1)					
DC Current Gain		h_{FE}	750	−	−
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			−	2.0	
			−	4.0	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$	−	2.5	Vdc
(I_C = 3.0 Adc, I_C = 12 mA)					
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain		h_{fe}	4.0	−	−
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53B, 53C		−	300	
	BDX54B, 54C		−	200	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

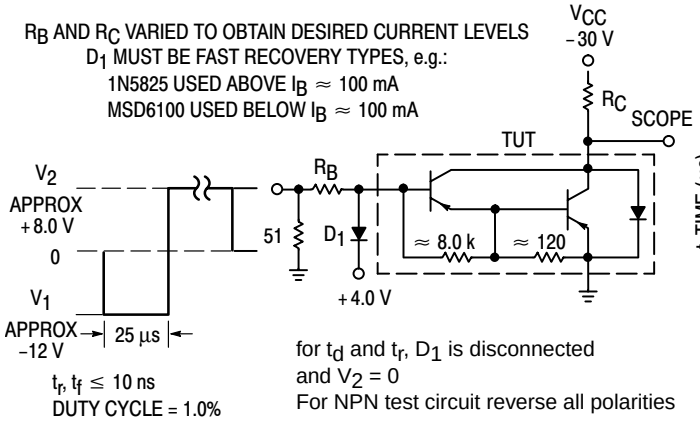


Figure 2. Switching Time Test Circuit

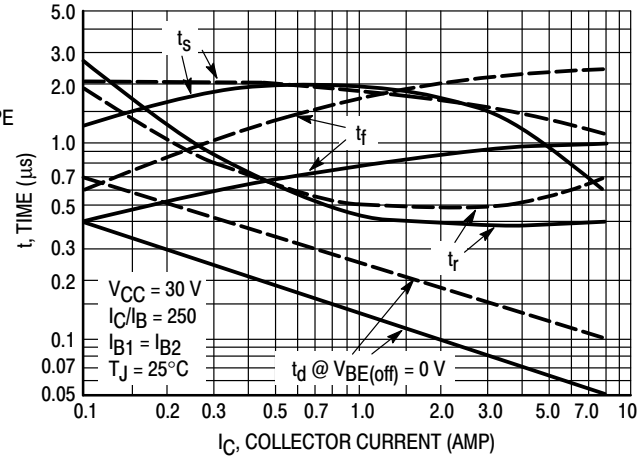


Figure 3. Switching Times

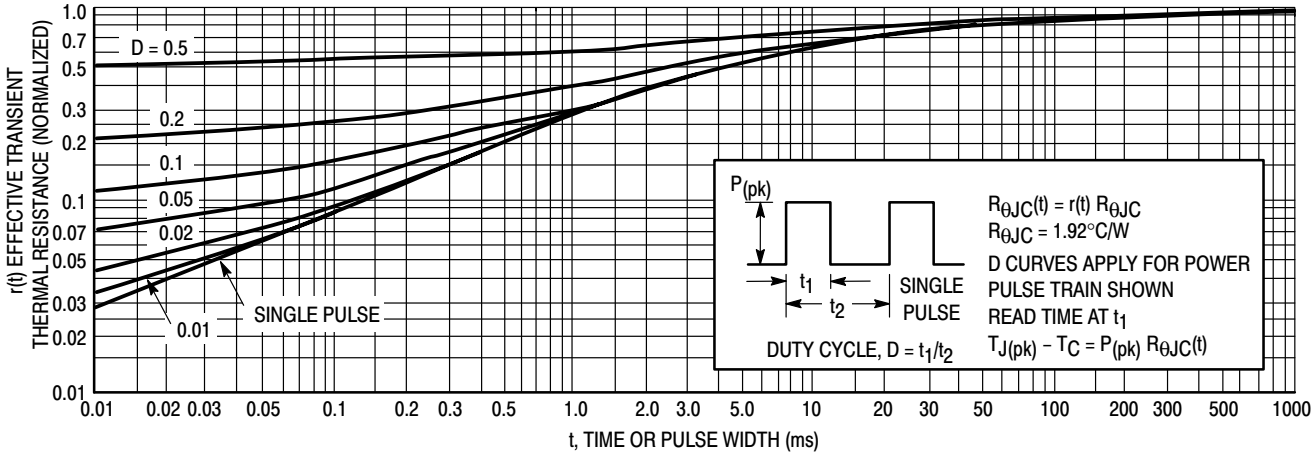


Figure 4. Thermal Response

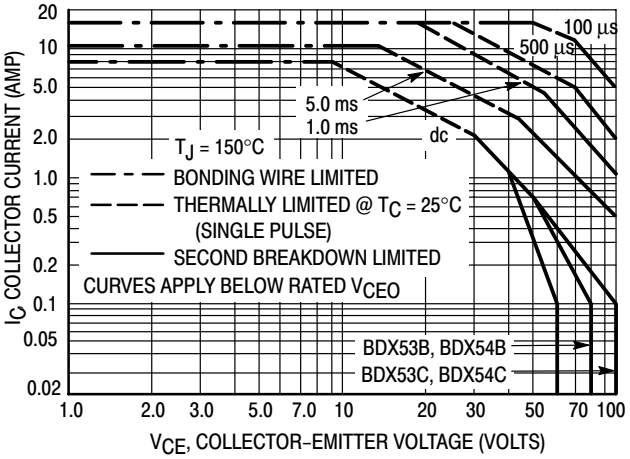


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

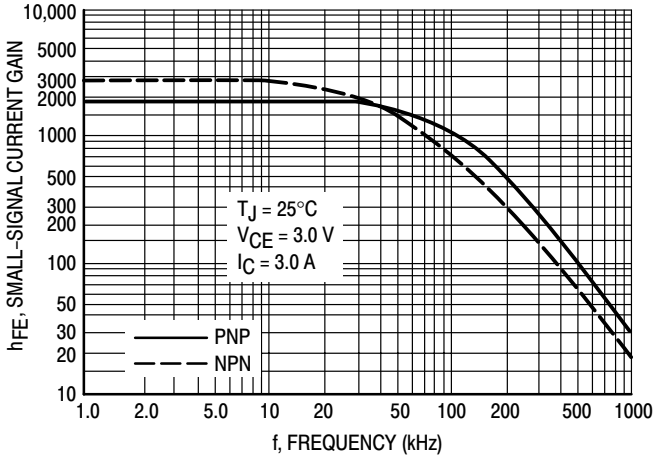


Figure 6. Small-Signal Current Gain

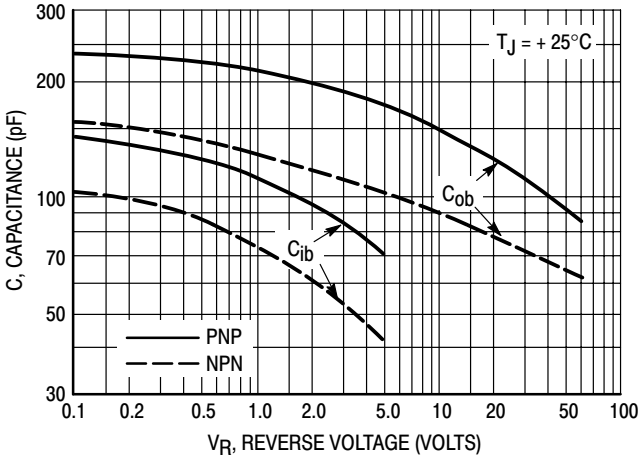
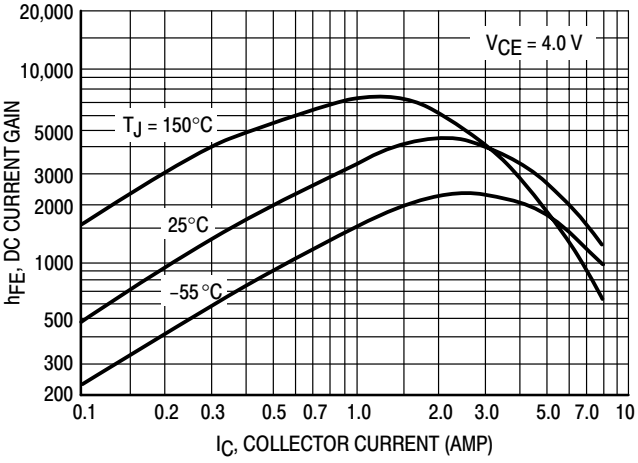


Figure 7. Capacitance

NPN
BDX53B, 53C



PNP
BDX54B, 54C

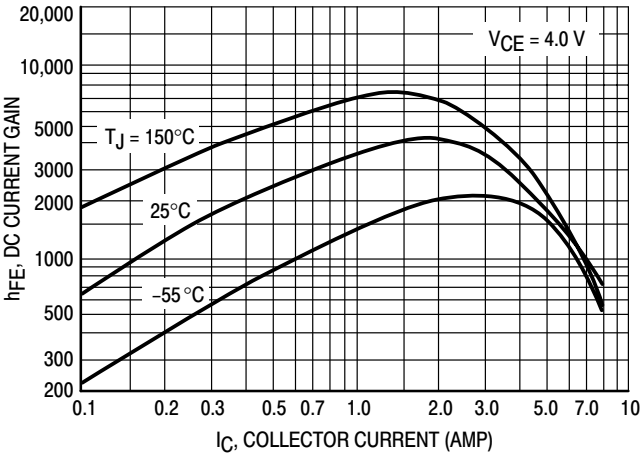
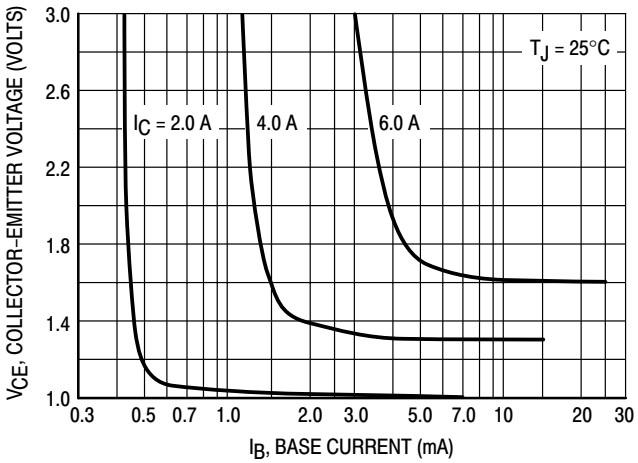


Figure 8. DC Current Gain



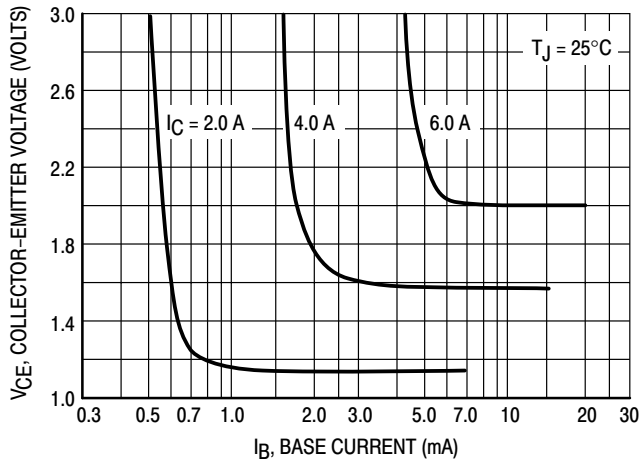
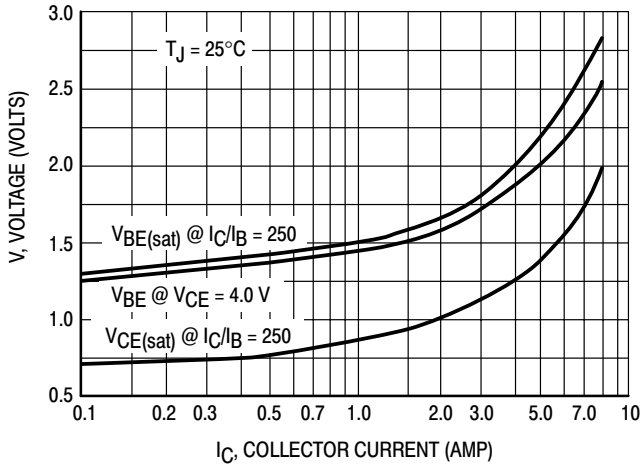


Figure 9. Collector Saturation Region



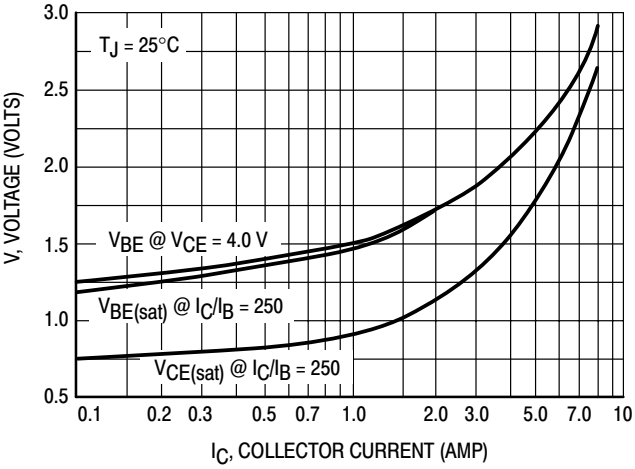


Figure 10. “On” Voltages

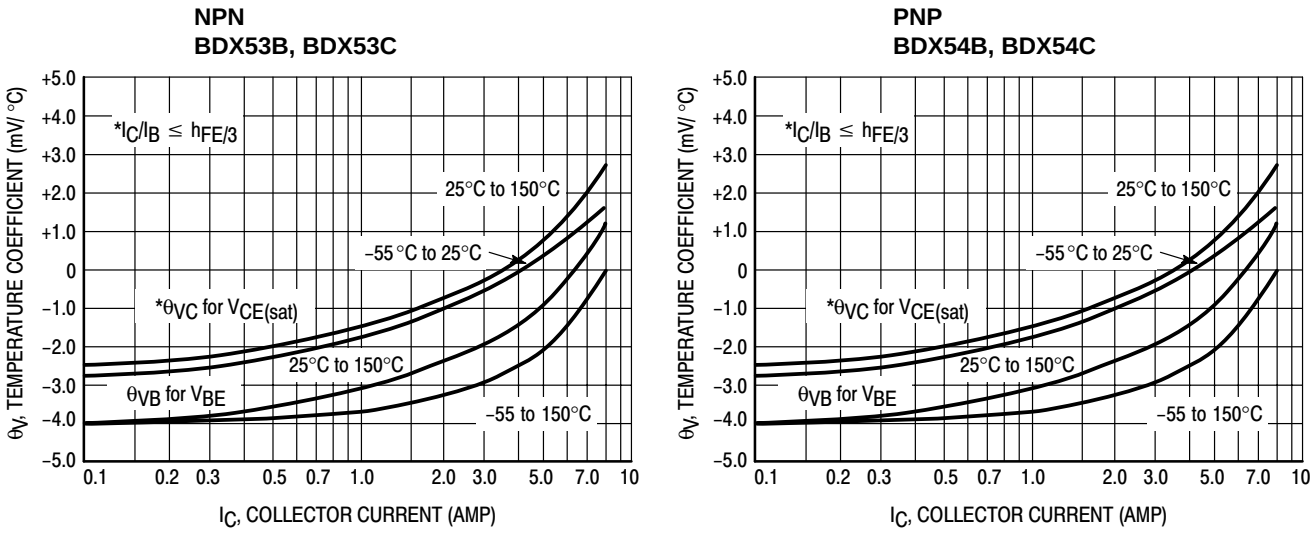


Figure 11. Temperature Coefficients

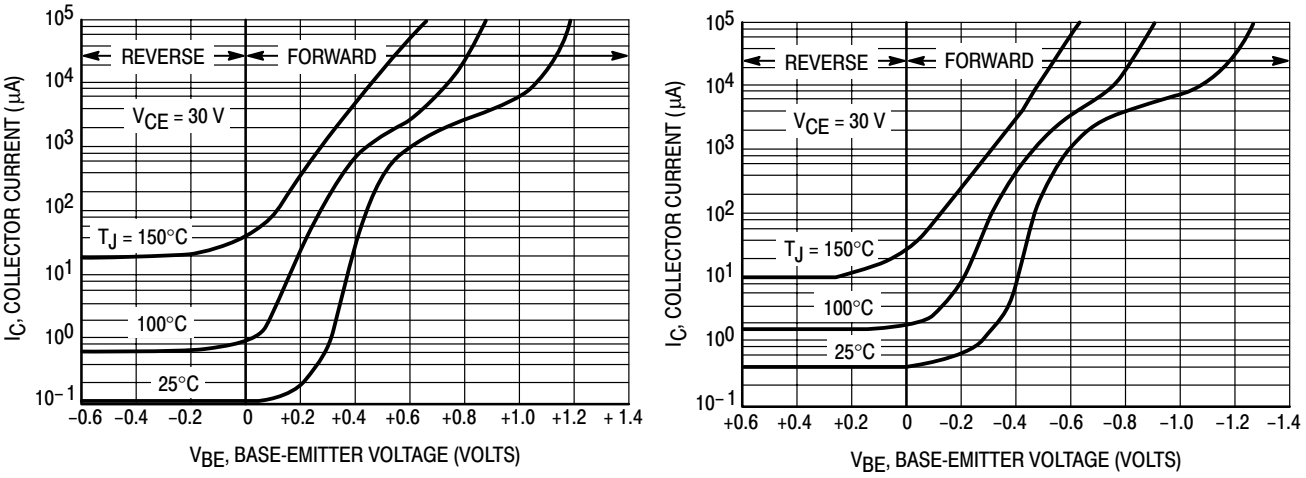


Figure 12. Collector Cut−Off Region

Figure 13. Darlington Schematic

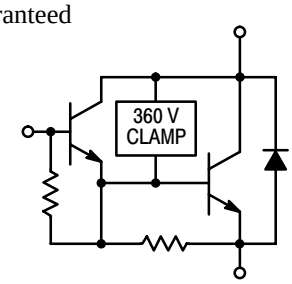
BU323Z

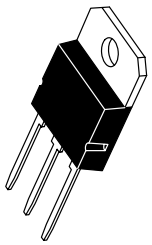
NPN Silicon Power Darlington
High Voltage Autoprotected

AUTOPROTECTED DARLINGTON
10 AMPERES
360−450 VOLTS CLAMP
150 WATTS

The BU323Z is a planar, monolithic, high−voltage power Darlington with a built−in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control, and exhibit the following main features:

- Integrated High−Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the −40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times
- Offered in Plastic SOT−93/TO−218 Type or TO−220 Packages





CASE 340D−02
SOT−93/TO−218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector−Emitter Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak	I_B I_{BM}	3.0 6.0	Adc
Total Power Dissipation (T_C = 25°C) Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector−Emitter Clamping Voltage (I_C = 7.0 A) (T_C = −40°C to +125°C)	V_{CLAMP}	350	—	450	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 200 V, I_B = 0)	I_{CEO}	—	—	100	μAdc
Emitter−Base Leakage Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	50	mAdc
ON CHARACTERISTICS (1)					
Base−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 100 mAdc) (I_C = 10 Adc, I_B = 0.25 Adc)	$V_{BE(sat)}$	 — —	 — —	 2.2 2.5	Vdc
Collector−Emitter Saturation Voltage (I_C = 7.0 Adc, I_B = 70 mAdc) (T_C = 125°C) (I_C = 8.0 Adc, I_B = 0.1 Adc) (T_C = 125°C) (I_C = 10 Adc, I_B = 0.25 Adc)	$V_{CE(sat)}$	 — — — — —	 — — — — —	 1.6 1.8 1.8 2.1 1.7	Vdc
Base−Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (T_C = −40°C to +125°C) (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	 1.1 1.3	 — —	 2.1 2.3	Vdc
Diode Forward Voltage Drop (I_F = 10 Adc)	V_F	—	—	2.5	Vdc
DC Current Gain (I_C = 6.5 Adc, V_{CE} = 1.5 Vdc) (T_C = −40°C to +125°C) (I_C = 5.0 Adc, V_{CE} = 4.6 Vdc)	h_{FE}	 150 500	 — —	 — 3400	—
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	—	2.0	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	200	pF
Input Capacitance (V_{EB} = 6.0 V)	C_{ib}	—	—	550	pF
CLAMPING ENERGY (see notes)					
Repetitive Non−Destructive Energy Dissipated at turn−off: (I_C = 7.0 A, L = 8.0 mH, R_{BE} = 100 Ω) (see Figures 2 and 4)	W_{CLAMP}	200	—	—	mJ

SWITCHING CHARACTERISTICS: Inductive Load (L = 10 mH)

Fall Time	(I_C = 6.5 A, I_{B1} = 45 mA, $V_{BE(off)}$ = 0, $R_{BE(off)}$ = 0, V_{CC} = 14 V, V_Z = 300 V)	t_{fi}	—	625	—	ns
Storage Time		t_{si}	—	10	30	μs
Cross−over Time		t_c	—	1.7	—	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

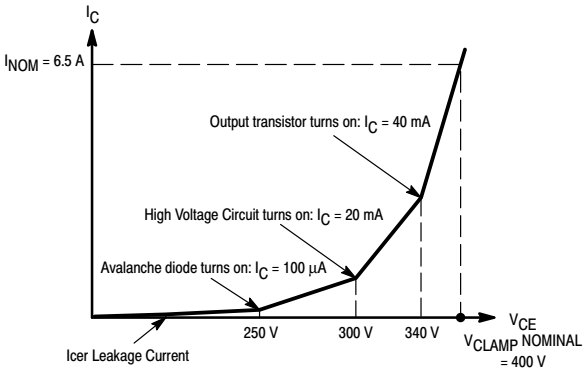


Figure 1. $I_C = f(V_{CE})$ Curve Shape

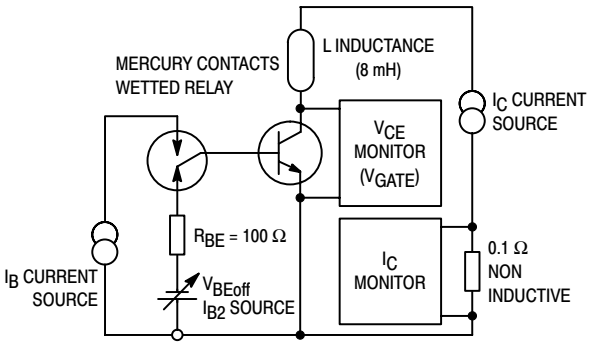


Figure 2. Basic Energy Test Circuit

By design, the BU323Z has a built−in avalanche diode and a special high voltage driving circuit. During an auto−protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in "FBSOA." Because of the built−in zener and associated network, the $I_C = f(V_{CE})$ curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1.

The bias parameters, V_{CLAMP}, I_{B1}, $V_{BE(off)}$, I_{B2}, I_C, and the inductance, are applied according to the Device Under Test (DUT) specifications. V_{CE} and I_C are monitored by the test system while making sure the load line remains within the limits as described in Figure 4.

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2 and 4, to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:
$I_{C(peak)}$ = 7.0 A, I_CH = 5.0 A, I_CL = 100 mA, I_B = 100 mA, R_{BE} = 100 Ω, V_{gate} = 280 V, L = 8.0 mH

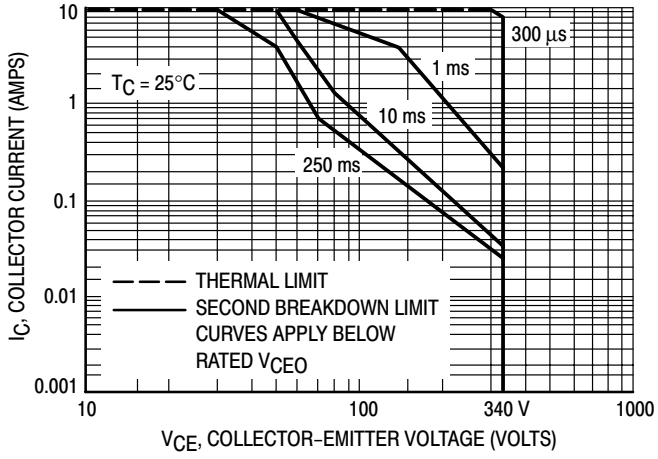
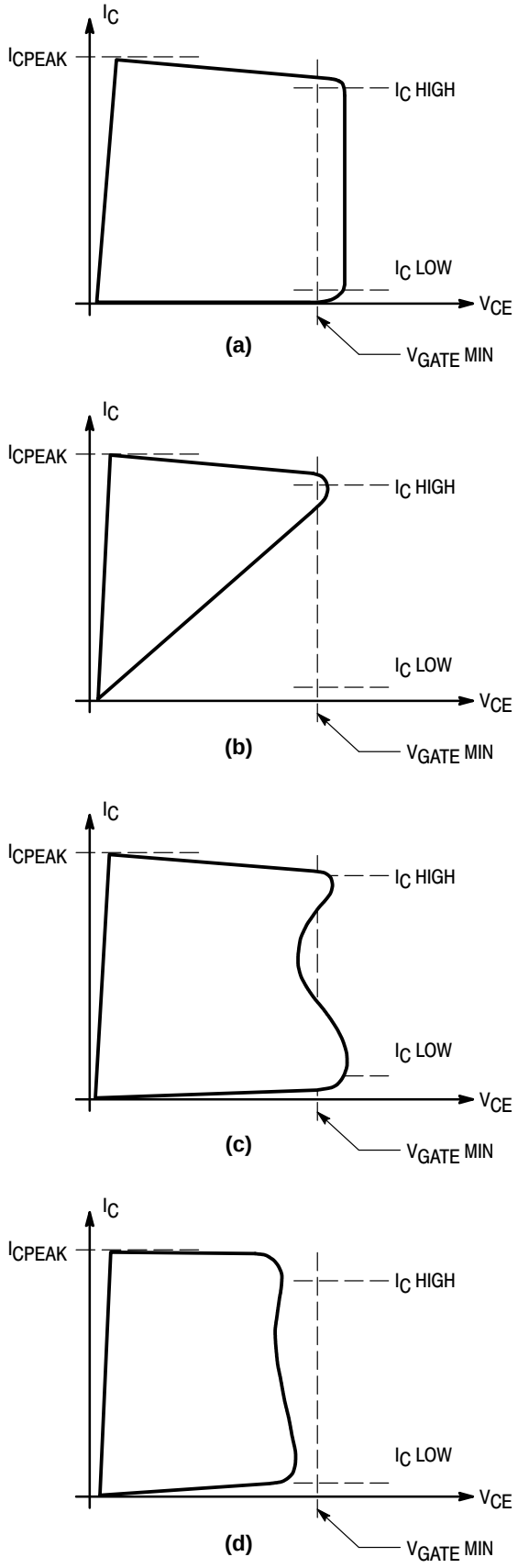


Figure 3. Forward Bias Safe Operating Area



The shaded area represents the amount of energy the device can sustain, under given DC biases ($I_C/I_B/V_{BE(off)}/R_{BE}$), without an external clamp; see the test schematic diagram, Figure 2.

The transistor PASSES the Energy test if, for the inductive load and $I_{CPEAK}/I_B/V_{BE(off)}$ biases, the V_{CE} remains outside the shaded area and greater than the V_{GATE} minimum limit, Figure 4a.

The transistor FAILS if the V_{CE} is less than the V_{GATE} (minimum limit) at any point along the V_{CE}/I_C curve as shown on Figures 4b, and 4c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.

The transistor FAILS if its Collector/Emitter breakdown voltage is less than the V_{GATE} value, Figure 4d.

Figure 4. Energy Test Criteria for BU323Z

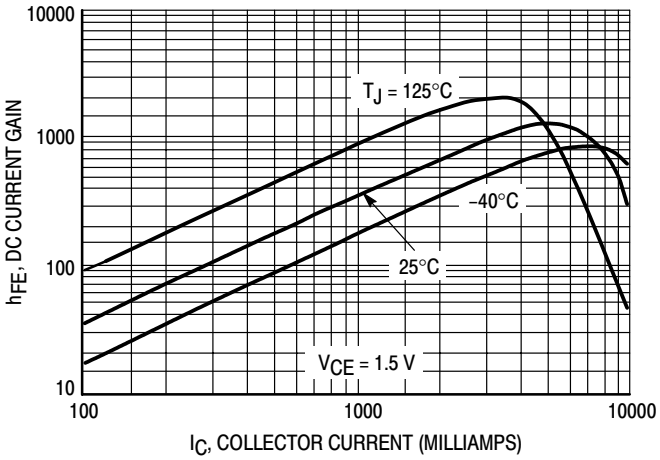


Figure 5. DC Current Gain

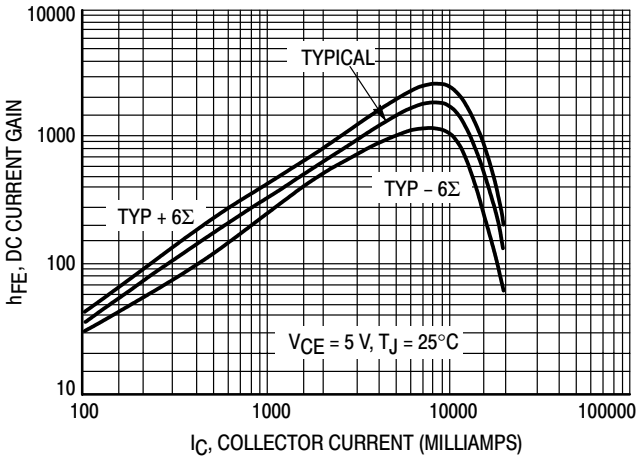


Figure 6. DC Current Gain

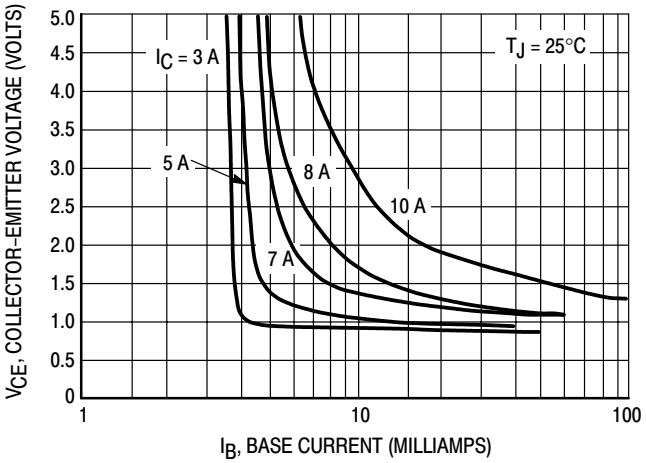


Figure 7. Collector Saturation Region

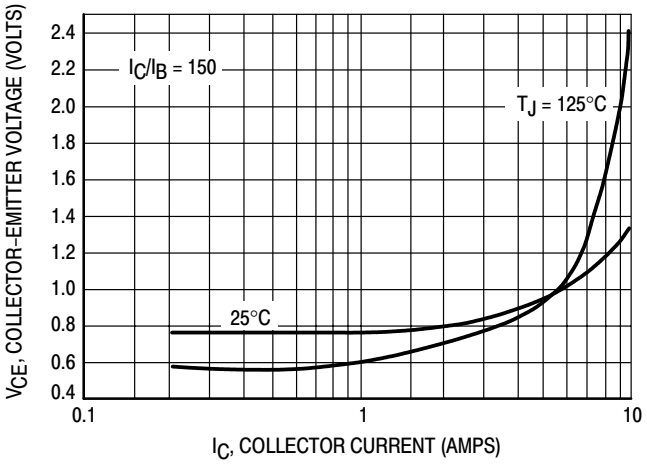


Figure 8. Collector−Emitter Saturation Voltage

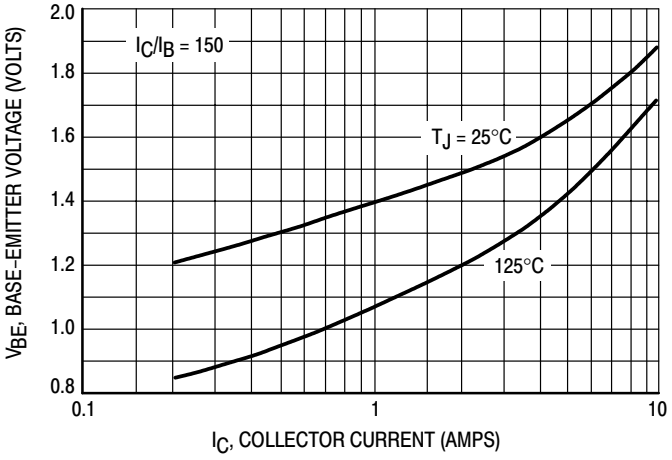


Figure 9. Base−Emitter Saturation Voltage

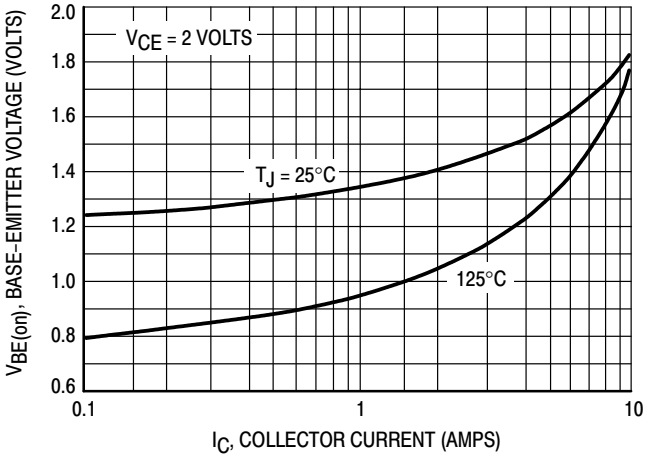


Figure 10. Base−Emitter “ON” Voltages

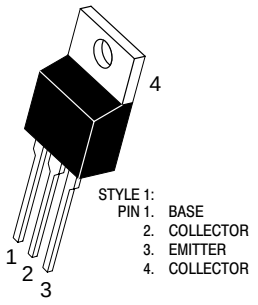
BU406
BU407

NPN Power Transistors

These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed: t_f = 750 ns (max)
- Low Saturation Voltage: $V_{CE(sat)}$ = 1 V (max) @ 5 A
- Packaged in Compact JEDEC TO−220AB

7 AMPERES
NPN SILICON
POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	BU406	BU407	Unit
Collector−Emitter Voltage	V_{CEO}	200	150	Vdc
Collector−Emitter Voltage	V_{CEV}	400	330	Vdc
Collector−Base Voltage	V_{CBO}	400	330	Vdc
Emitter Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous Peak Repetitive Peak (10 ms)	I_C	7 10 15		Adc
Base Current	I_B	4		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage(1) (I_C = 100 mAdc, I_B = 0)	BU406 BU407	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0) (V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0, T_C = 150°C)		I_{CES}	 — — —	 — — —	 5 0.1 1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	BU406, BU407	I_{EBO}	—	—	1	mAdc
ON CHARACTERISTICS (1)						
Collector−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	—	—	1.2	Vdc
Forward Diode Voltage (I_{EC} = 5 Adc) “D” only		V_{EC}	—	—	2	Volts
DYNAMIC CHARACTERISTICS						
Current−Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 20 MHz)		f_T	10	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS						
Inductive Load Crossover Time (V_{CC} = 40 Vdc, I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc, L = 150 μH)		t_c	—	—	0.75	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

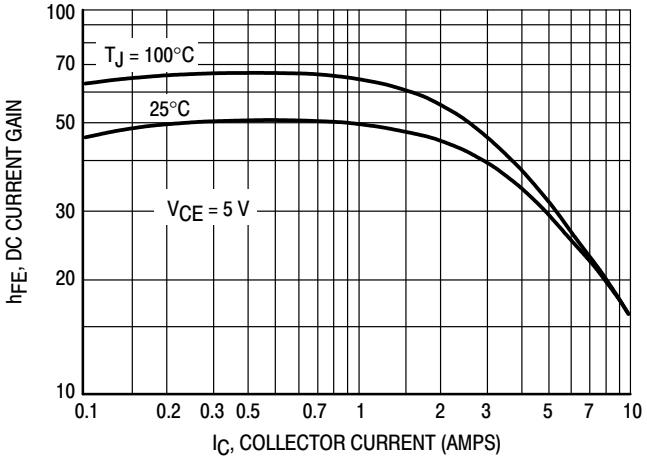


Figure 11. DC Current Gain

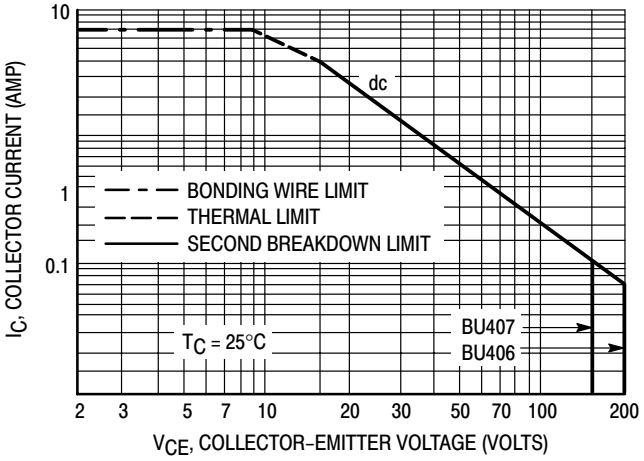


Figure 12. Maximum Rated Forward Bias Safe Operating Area

BUB323Z

NPN Silicon Power Darlington

High Voltage Autoprotected D^{2}PAK for Surface Mount

The BUB323Z is a planar, monolithic, high−voltage power Darlington with a built−in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control, and exhibit the following main features:

- Integrated High−Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the −40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector−Emitter Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous − Peak	I_C I_{CM}	10 20	Adc
Base Current − Continuous − Peak	I_B I_{BM}	3.0 6.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 150 1.0	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175	°C

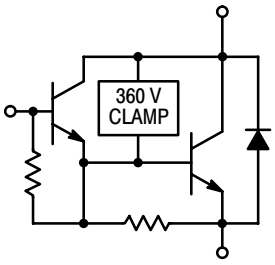
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	260	°C

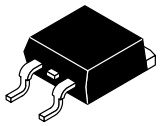
ON Semiconductor™

http://onsemi.com

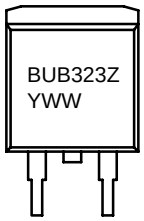
AUTOPROTECTED DARLINGTON 10 AMPERES 360−450 VOLTS CLAMP 150 WATTS



MARKING DIAGRAM



D^{2}PAK
CASE 418B
STYLE 1



BUB323Z = Specific Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BUB323Z	D^{2}PAK	50 Units/Rail
BUB323ZT4	D^{2}PAK	800/Tape & Reel

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 1)						
Collector−Emitter Clamping Voltage (I_C = 7.0 A) (T_C = −40°C to +125°C)		V_{CLAMP}	350	−	450	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 200 V, I_B = 0)		I_{CEO}	−	−	100	μAdc
Emitter−Base Leakage Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	−	−	50	mAdc
ON CHARACTERISTICS (Note 1)						
Base−Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 100 mAdc)			−	−	2.2	
(I_C = 10 Adc, I_B = 0.25 Adc)			−	−	2.5	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 7.0 Adc, I_B = 70 mAdc)			−	−	1.6	
	(T_C = 125°C)		−	−	1.8	
(I_C = 8.0 Adc, I_B = 0.1 Adc)			−	−	1.8	
	(T_C = 125°C)		−	−	2.1	
(I_C = 10 Adc, I_B = 0.25 Adc)			−	−	1.7	
Base−Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	(T_C = −40°C to +125°C)		1.1	−	2.1	
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)			1.3	−	2.3	
Diode Forward Voltage Drop (I_F = 10 Adc)		V_F	−	−	2.5	Vdc
DC Current Gain		h_{FE}				−
(I_C = 6.5 Adc, V_{CE} = 1.5 Vdc)	(T_C = −40°C to +125°C)		150	−	−	
(I_C = 5.0 Adc, V_{CE} = 4.6 Vdc)			500	−	3400	
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	−	−	2.0	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	−	−	200	pF
Input Capacitance (V_{EB} = 6.0 V)		C_{ib}	−	−	550	pF
CLAMPING ENERGY (see notes)						
Repetitive Non−Destructive Energy Dissipated at turn−off: (I_C = 7.0 A, L = 8.0 mH, R_{BE} = 100 Ω) (see Figures 2 and 4)		W_{CLAMP}	200	−	−	mJ
SWITCHING CHARACTERISTICS: Inductive Load (L = 10 mH)						
Fall Time	(I_C = 6.5 A, I_{B1} = 45 mA, $V_{BE(off)}$ = 0, $R_{BE(off)}$ = 0, V_{CC} = 14 V, V_Z = 300 V)	t_{fi}	−	625	−	ns
Storage Time		t_{si}	−	10	30	μs
Cross−over Time		t_c	−	1.7	−	μs

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

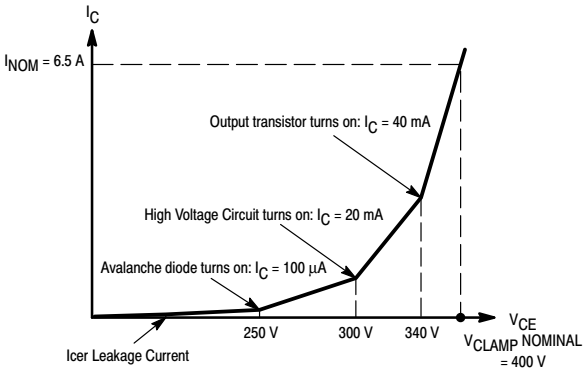


Figure 1. $I_C = f(V_{CE})$ Curve Shape

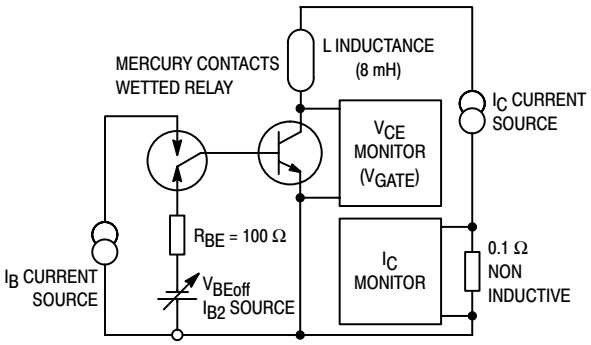


Figure 2. Basic Energy Test Circuit

By design, the BU323Z has a built−in avalanche diode and a special high voltage driving circuit. During an auto−protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in "FBSOA." Because of the built−in zener and associated network, the $I_C = f(V_{CE})$ curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1.

The bias parameters, V_{CLAMP}, I_{B1}, $V_{BE(off)}$, I_{B2}, I_C, and the inductance, are applied according to the Device Under Test (DUT) specifications. V_{CE} and I_C are monitored by the test system while making sure the load line remains within the limits as described in Figure 4.

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2 and 4, to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:
$I_{C(peak)}$ = 7.0 A, I_CH = 5.0 A, I_CL = 100 mA, I_B = 100 mA, R_{BE} = 100 Ω, V_{gate} = 280 V, L = 8.0 mH

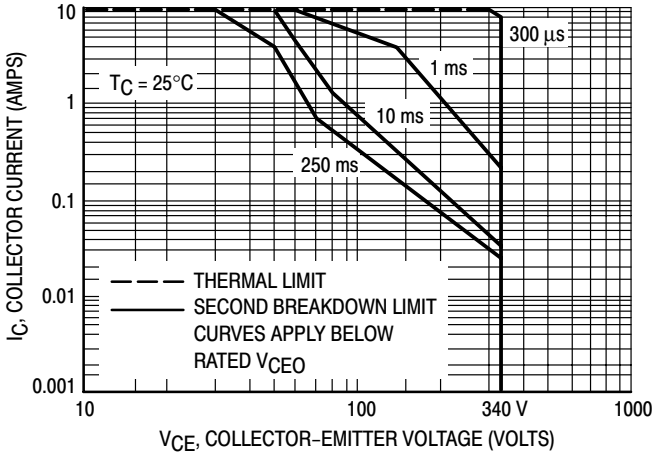
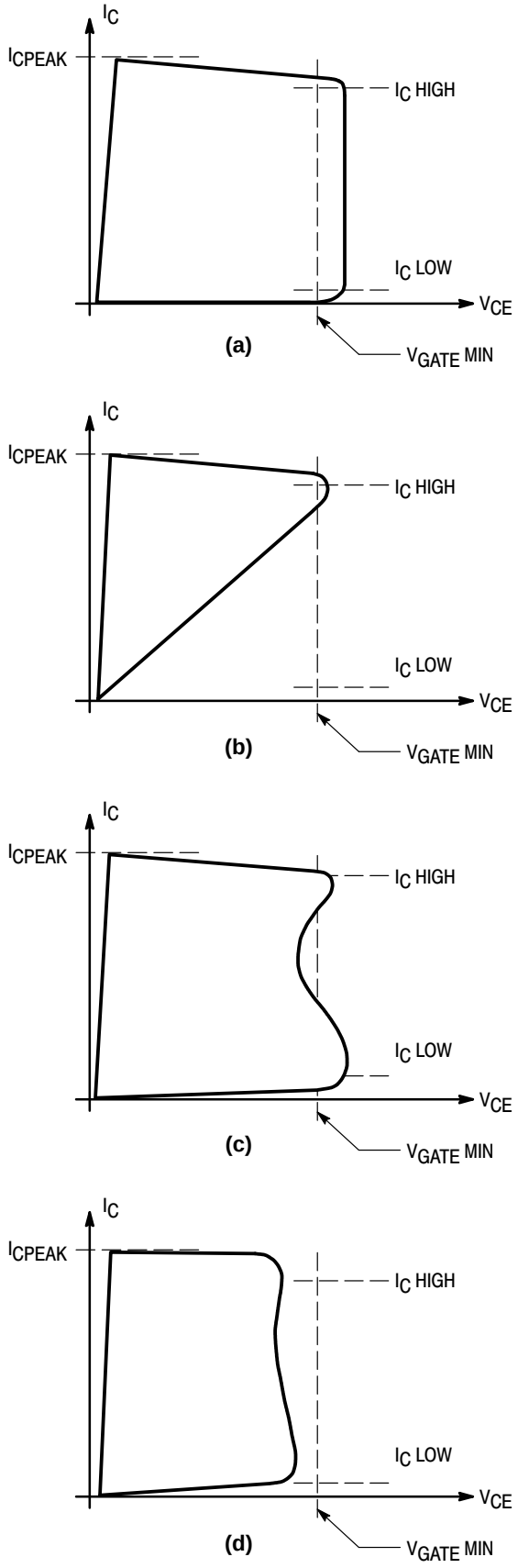


Figure 3. Forward Bias Safe Operating Area



The shaded area represents the amount of energy the device can sustain, under given DC biases ($I_C/I_B/V_{BE(off)}/R_{BE}$), without an external clamp; see the test schematic diagram, Figure 2.

The transistor PASSES the Energy test if, for the inductive load and $I_{CPEAK}/I_B/V_{BE(off)}$ biases, the V_{CE} remains outside the shaded area and greater than the V_{GATE} minimum limit, Figure 4a.

The transistor FAILS if the V_{CE} is less than the V_{GATE} (minimum limit) at any point along the V_{CE}/I_C curve as shown on Figures 4b, and 4c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.

The transistor FAILS if its Collector/Emitter breakdown voltage is less than the V_{GATE} value, Figure 4d.

Figure 4. Energy Test Criteria for BU323Z

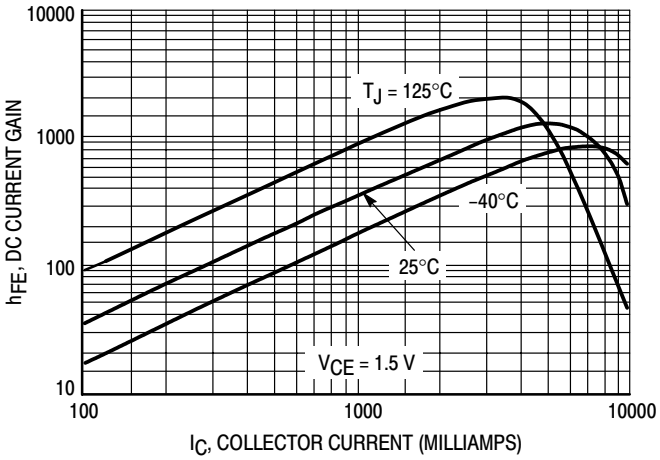


Figure 5. DC Current Gain

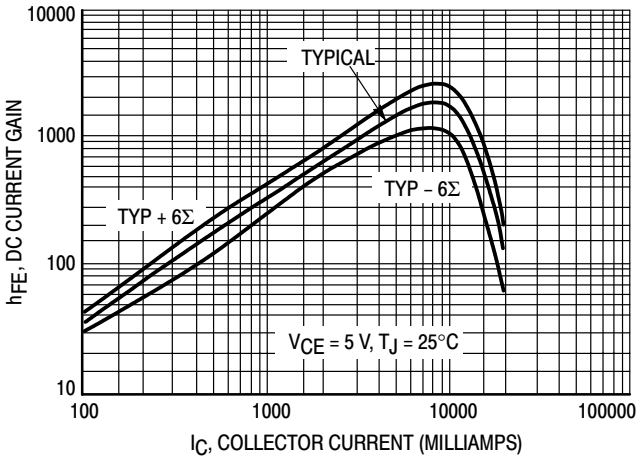


Figure 6. DC Current Gain

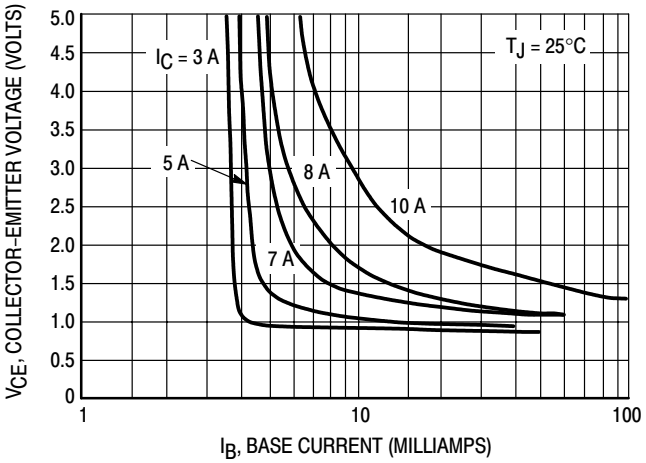


Figure 7. Collector Saturation Region

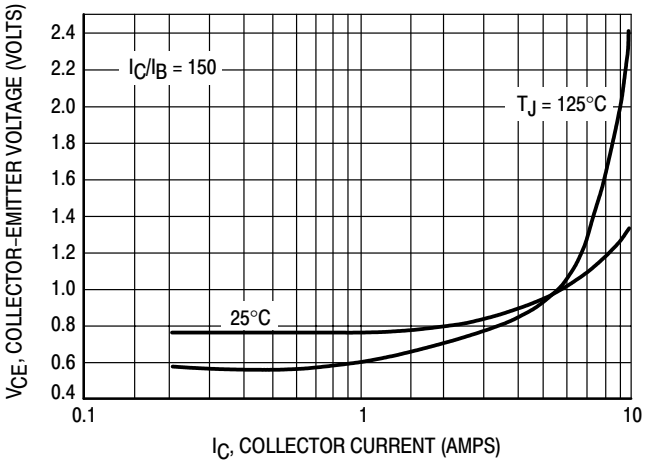


Figure 8. Collector−Emitter Saturation Voltage

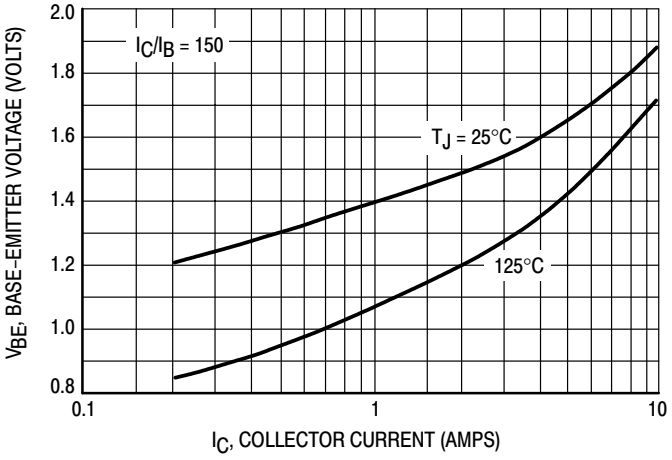


Figure 9. Base−Emitter Saturation Voltage

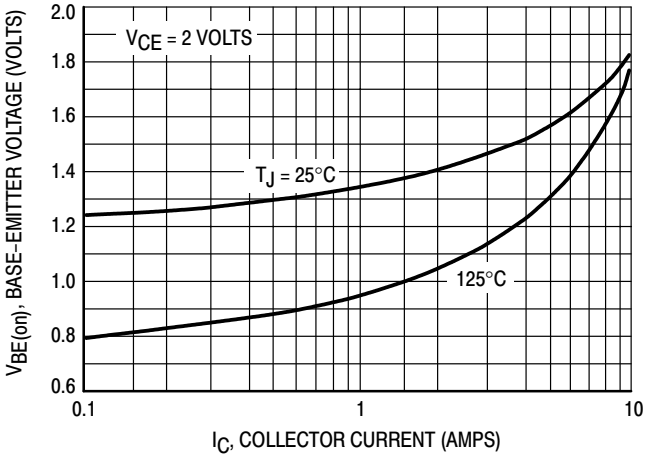
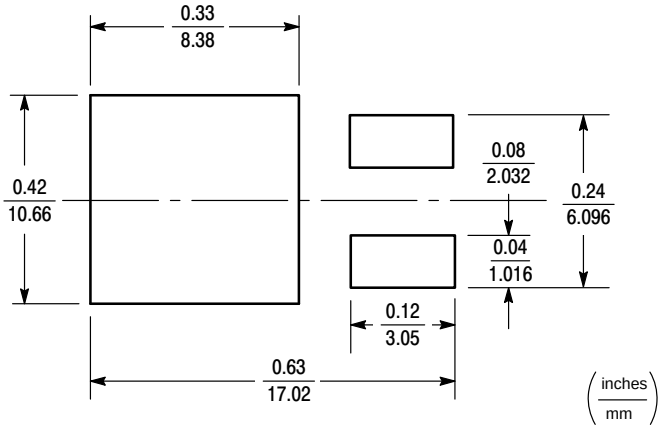


Figure 10. Base−Emitter “ON” Voltages

INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus Collector pad area is shown in Figure 11

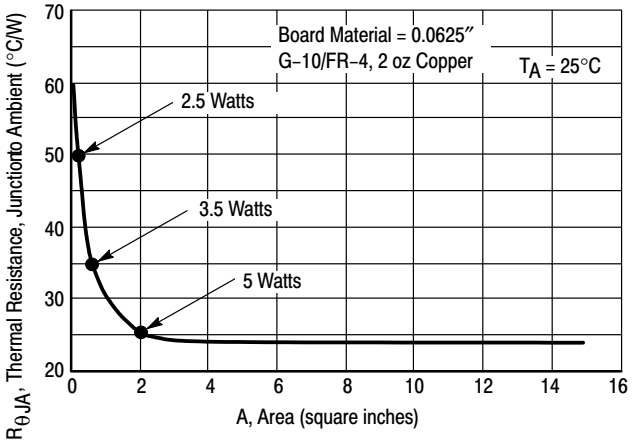


Figure 11. Thermal Resistance versus Collector Pad Area for the D2PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC−59, SC−70/SOT−323, SOD−123, SOT−23, SOT−143, SOT−223, SO−8, SO−14, SO−16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 12 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

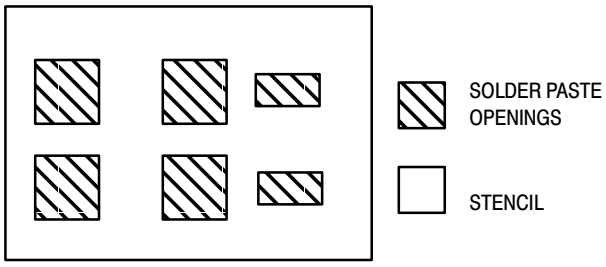


Figure 12. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* * Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 13 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

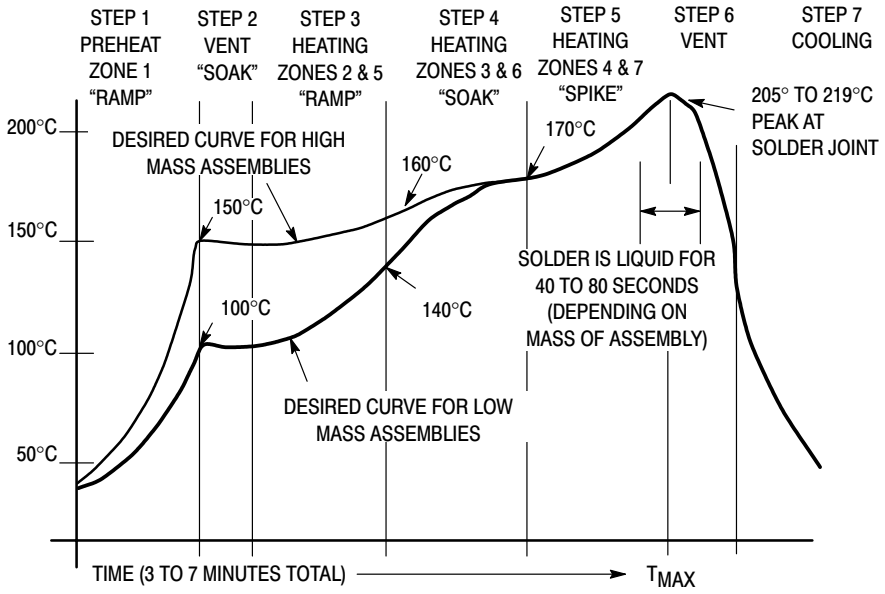


Figure 13. Typical Solder Heating Profile

BUH100

SWITCHMODE™ NPN Silicon Planar Power Transistor

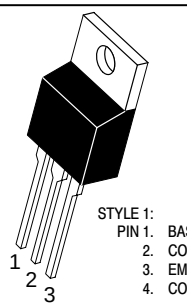
POWER TRANSISTOR
10 AMPERES
700 VOLTS
100 WATTS

The BUH100 has an application specific state−of−art die designed for use in 100 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start−up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 10	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	100 0.8	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	460		Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	860		Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C	$V_{BE(sat)}$		1	1.1	Vdc
Collector−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.37 0.37	0.6 0.6	Vdc
(I_C = 7 Adc, I_B = 1.5 Adc)	@ T_C = 25°C @ T_C = 125°C			0.5 0.6	0.75 1.5	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 16	24 28		—
(I_C = 5 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 10	15 14.5		—
(I_C = 7 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		8 7	12 10.5		—
(I_C = 10 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	9.5 8		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1} (See Figure 19)	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$		1.1		V
		@ T_C = 125°C			2.1		V
	I_C = 7.5 Adc, I_{B1} = 1.5 Adc, V_{CC} = 300 V	@ T_C = 25°C			1.7		V
		@ T_C = 125°C			5		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		100	150	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		1300	1750	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn−on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		130 140	200	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		6.8 8.5	8	μs
Turn−on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		140 150	200	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.4 4.3	4	μs
Turn−on Time	I_C = 5 Adc, I_{B1} = 1 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		250 800	500	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.9 3.6	3.5	μs
Turn−on Time	I_C = 7.5 Adc, I_{B1} = 1.5 Adc I_{B2} = 1.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		500 900	700	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.1 2.5	2.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		150 180	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		5.1 5.8	6	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		230 300	325	ns
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		150 170	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.5 2.8	3	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		260 300	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 1 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		100 140	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.9 4.6	3.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		220 450	300	ns
Fall Time	I_C = 7.5 Adc I_{B1} = 1.5 Adc I_{B2} = 1.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		100 150	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2 2.5	2.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

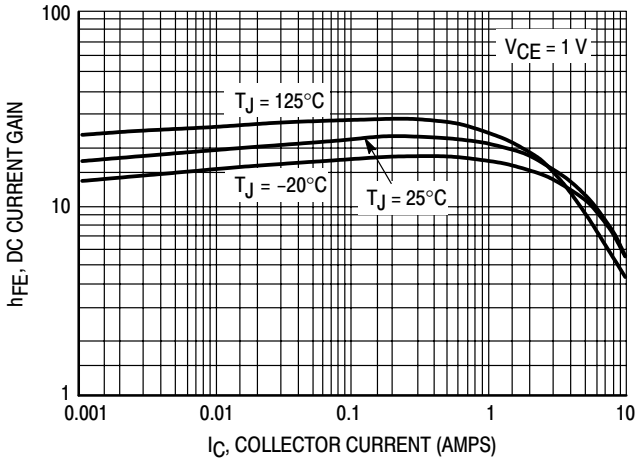


Figure 14. DC Current Gain @ 1 Volt

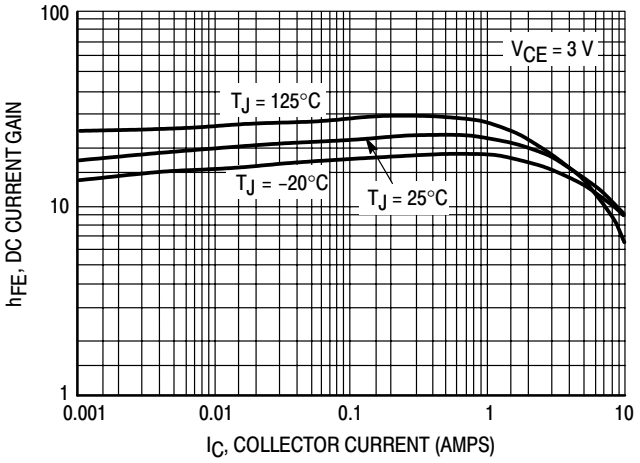


Figure 15. DC Current Gain @ 3 Volt

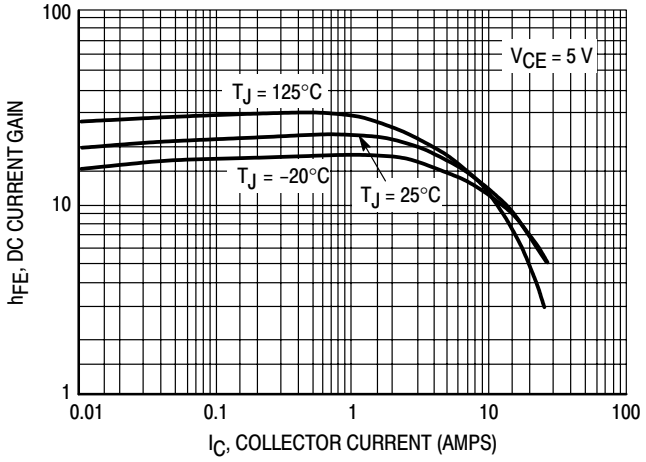


Figure 16. DC Current Gain @ 5 Volt

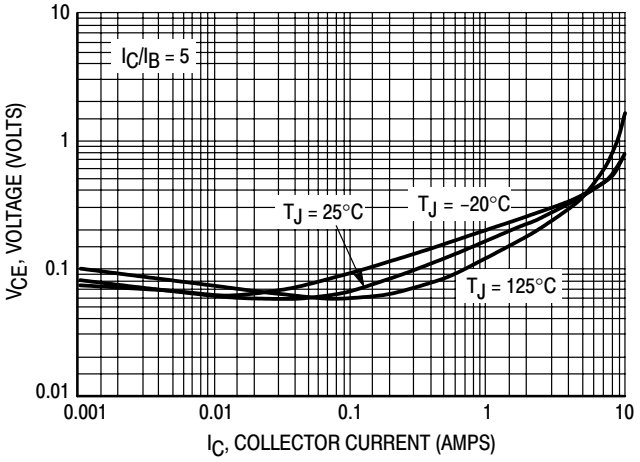


Figure 17. Collector−Emitter Saturation Voltage

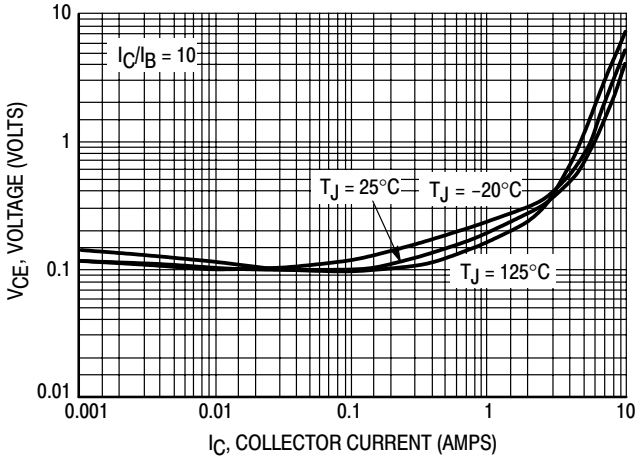


Figure 18. Collector−Emitter Saturation Voltage

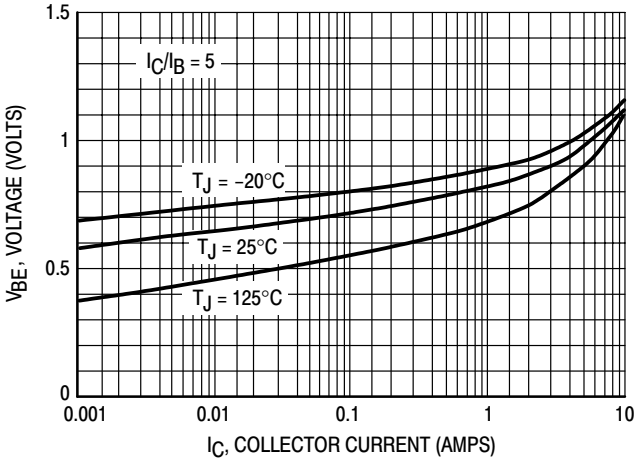


Figure 19. Base−Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

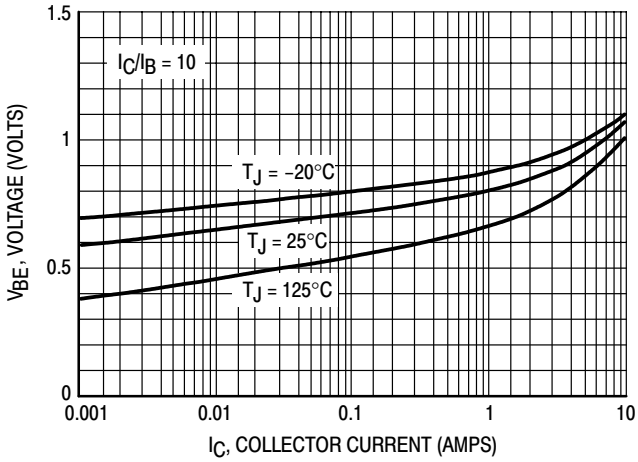


Figure 20. Base−Emitter Saturation Region

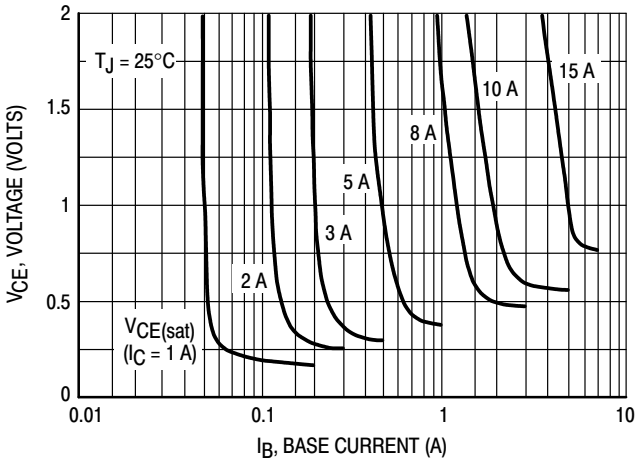


Figure 21. Collector Saturation Region

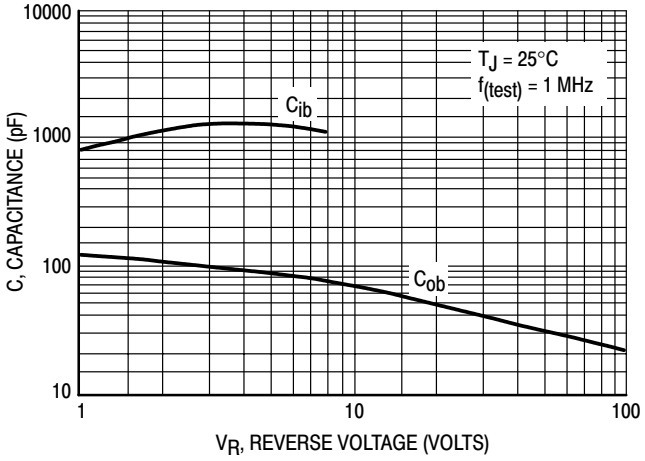


Figure 22. Capacitance

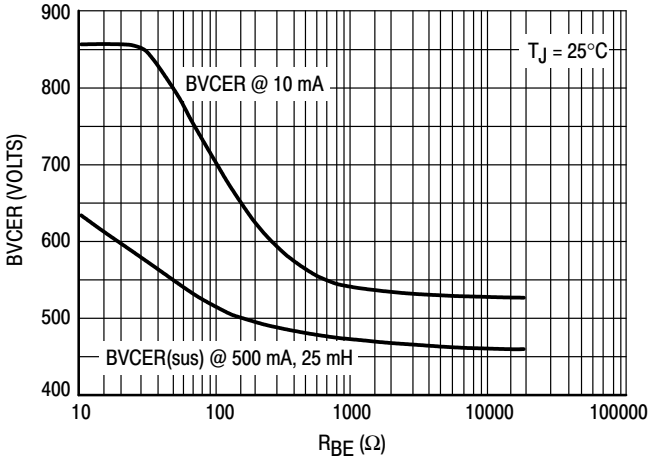


Figure 23. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

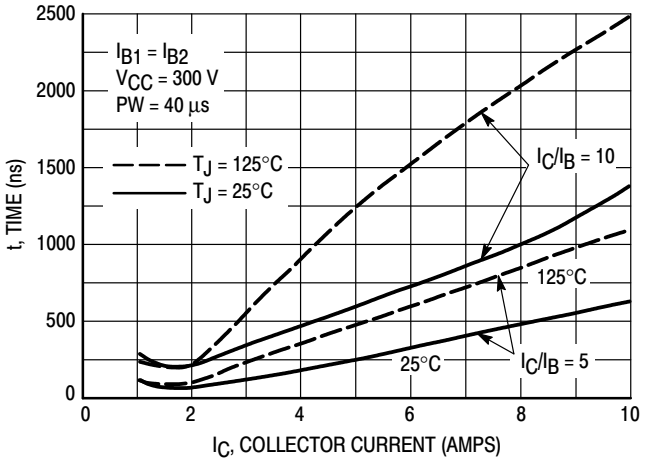


Figure 24. Resistive Switching Time, t_{on}

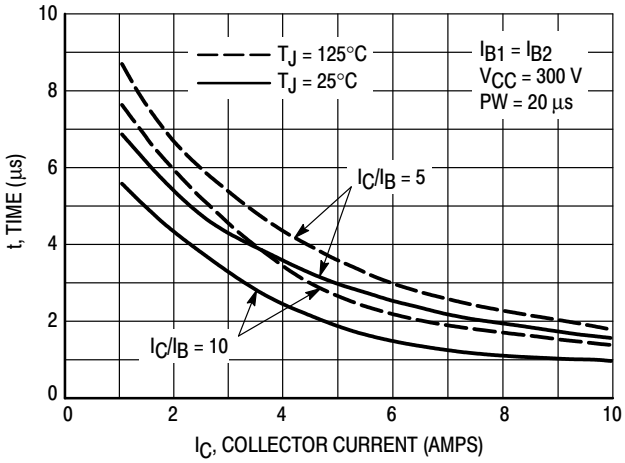


Figure 25. Resistive Switch Time, t_{off}

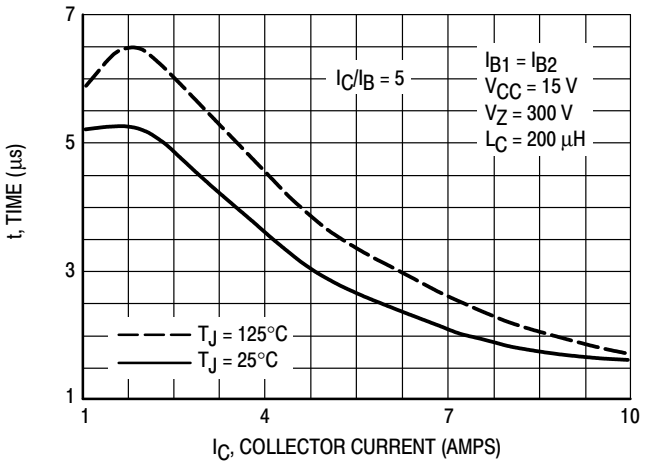


Figure 26. Inductive Storage Time, t_{si}

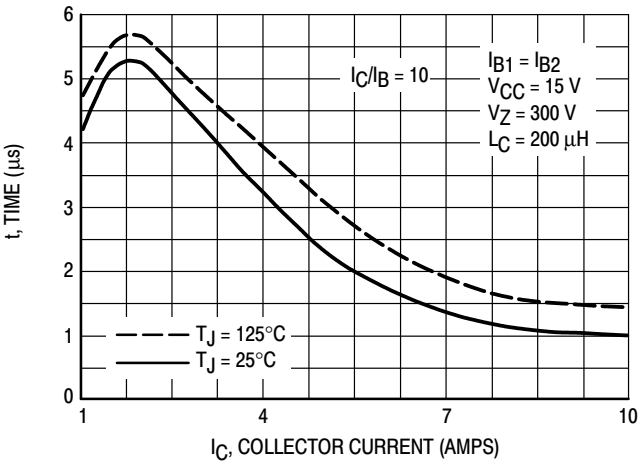


Figure 13 Bis. Inductive Storage Time, t_{si}

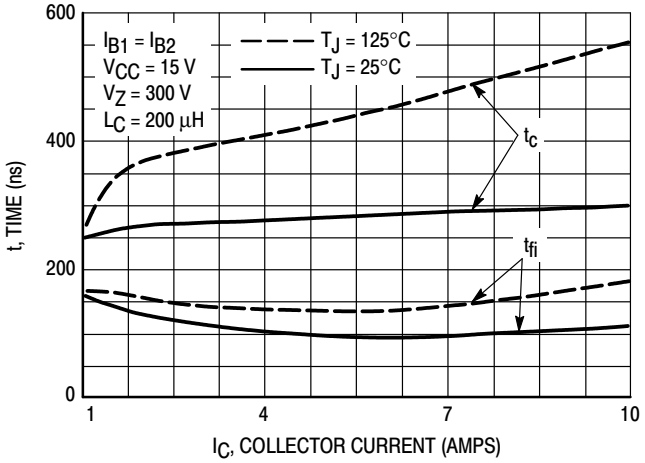


Figure 27. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

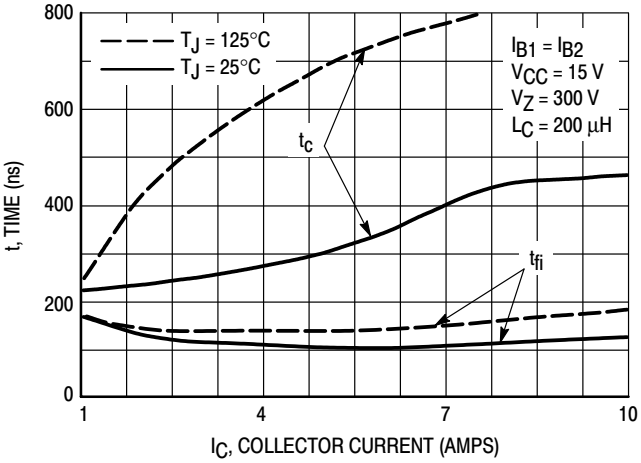


Figure 28. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

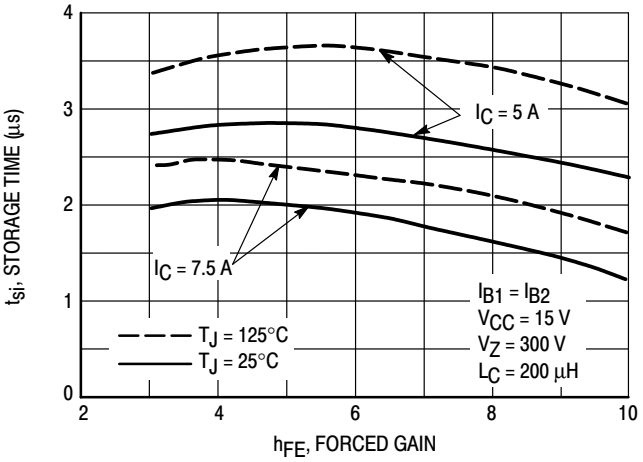


Figure 29. Inductive Storage Time

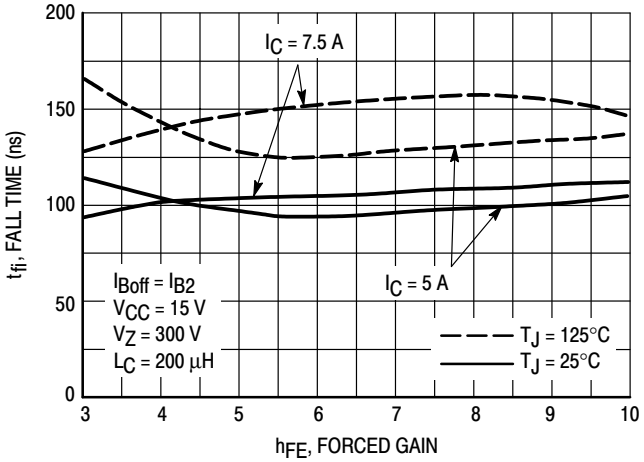


Figure 30. Inductive Fall Time

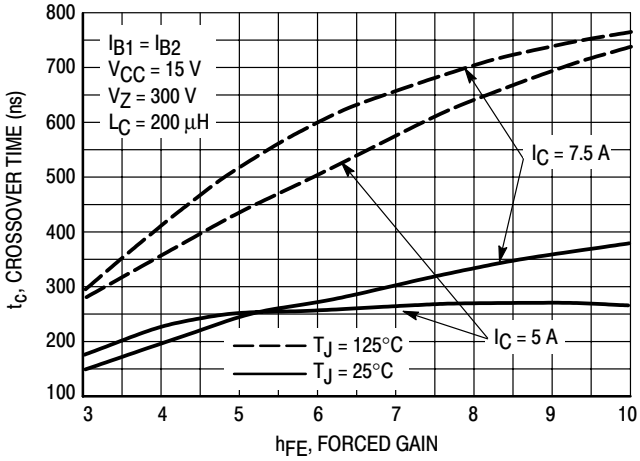


Figure 31. Inductive Crossover Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

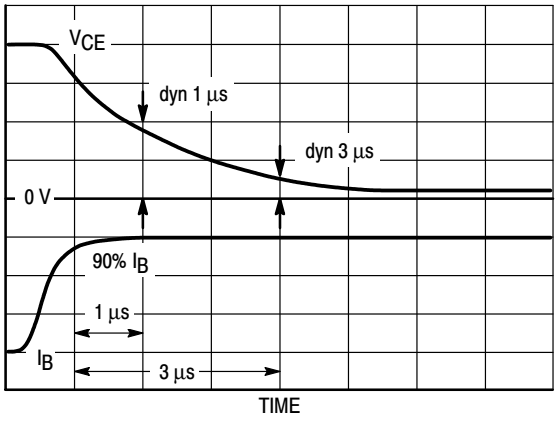


Figure 32. Dynamic Saturation Voltage Measurements

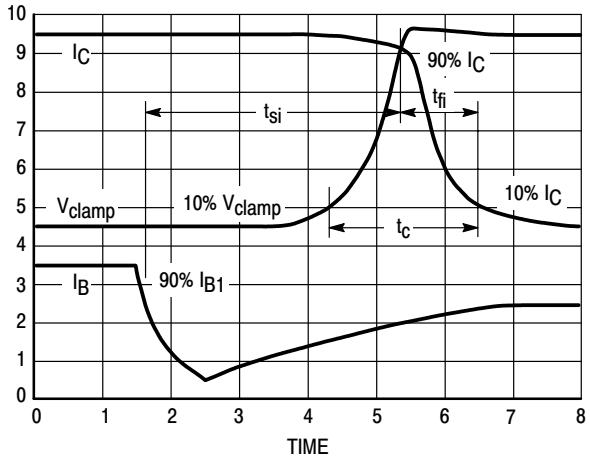
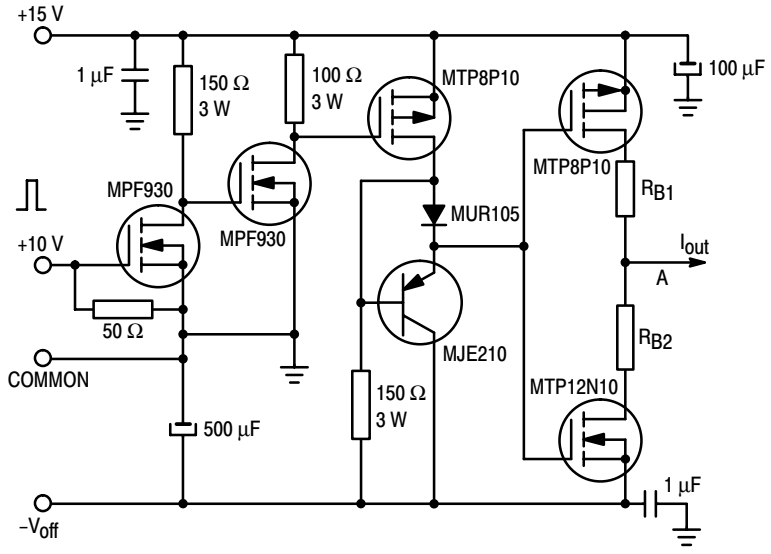
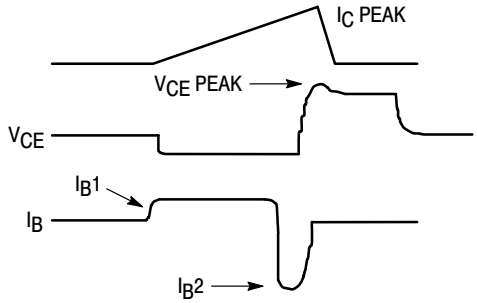


Figure 33. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	**Inductive Switching**	**RBSOA**
L = 10 mH	L = 200 μH	L = 500 μH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

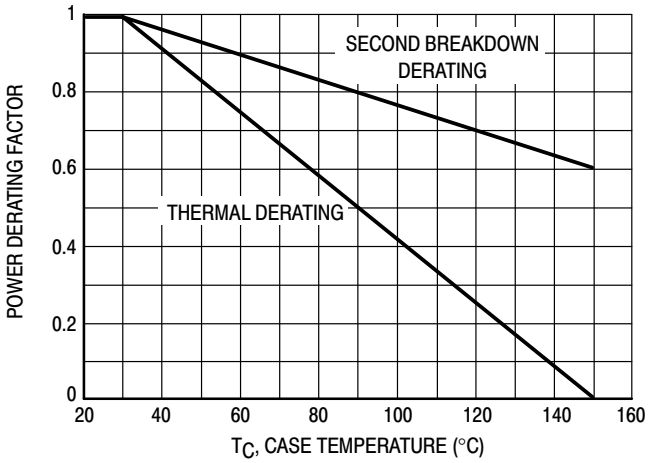


Figure 34. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

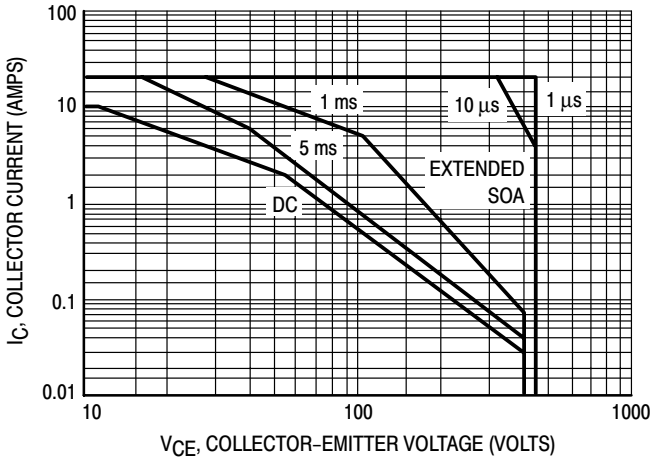


Figure 35. Forward Bias Safe Operating Area

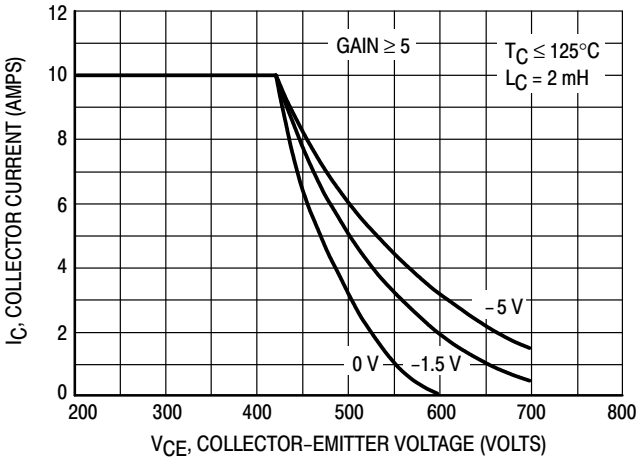


Figure 36. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

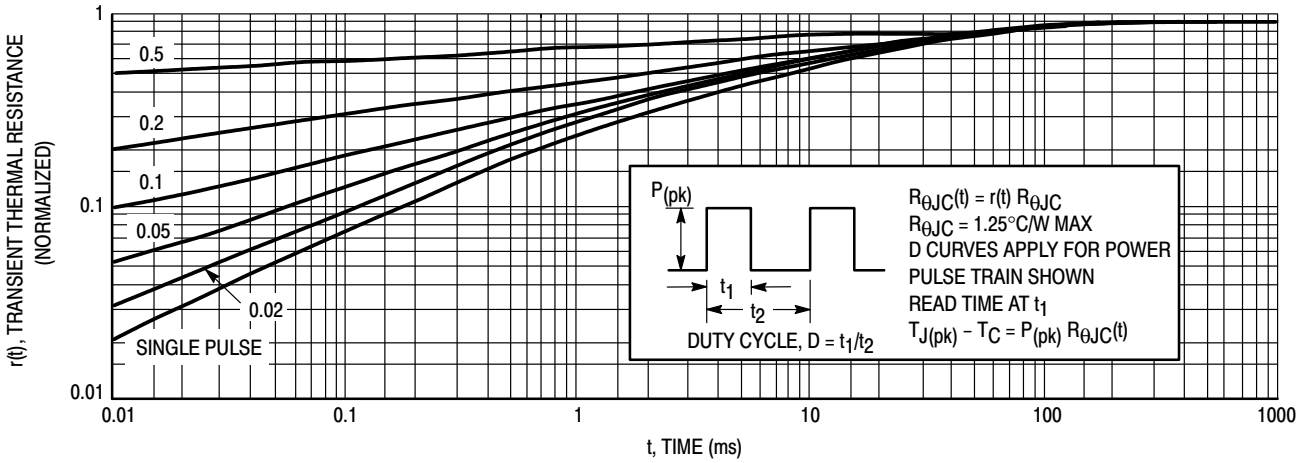


Figure 37. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH100

BUH150

SWITCHMODE™ NPN Silicon Planar Power Transistor

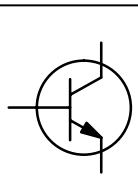
POWER TRANSISTOR
15 AMPERES
700 VOLTS
150 WATTS

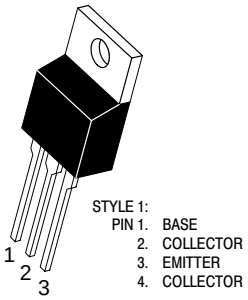
The BUH150 has an application specific state−of−art die designed for use in 150 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start−up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions





CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 25	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	150 1.2	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.85 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	460		Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	860		Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.3		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc)		$V_{BE(sat)}$		1	1.25	Vdc
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.16 0.15	0.4 0.4	Vdc
(I_C = 10 Adc, I_B = 2 Adc)	@ T_C = 25°C			0.45	1	Vdc
(I_C = 20 Adc, I_B = 4 Adc)	@ T_C = 25°C			2	5	Vdc
DC Current Gain (I_C = 20 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	4 2.5	7 4.5		—
(I_C = 10 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		8 6	12 10		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		12 14	20 22		—
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C		10	20		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1} (see Figure 19)	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$		1.5		V
		@ T_C = 125°C			2.8		V
	I_C = 10 Adc, I_{B1} = 2 Adc, V_{CC} = 300 V	@ T_C = 25°C			2.4		V
		@ T_C = 125°C			5		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		100	150	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		1300	1750	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		200	300	ns
Storage Time		@ T_C = 25°C	t_s		5.3	6.5	μs
Fall Time		@ T_C = 25°C	t_f		240	350	ns
Turn−off Time		@ T_C = 25°C	t_{off}		5.6	7	μs
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		100	200	ns
Storage Time		@ T_C = 25°C	t_s		6.1	7.5	μs
Fall Time		@ T_C = 25°C	t_f		320	500	ns
Turn−off Time		@ T_C = 25°C	t_{off}		6.5	8	μs
Turn−on Time	I_C = 5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		450 800	650	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.5 3.9	3	μs
Turn−on Time	I_C = 10 Adc, I_{B1} = 2 Adc I_{B2} = 2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		500 900	700	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.25 2.75	2.75	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 2 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 160	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		6.5 8	8	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		235 240	350	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 170	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		6 7.8	7.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 270	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 140	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		3.25 4.6	3.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		275 450	350	ns
Fall Time	I_C = 10 Adc I_{B1} = 2 Adc I_{B2} = 2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 160	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.3 2.8	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

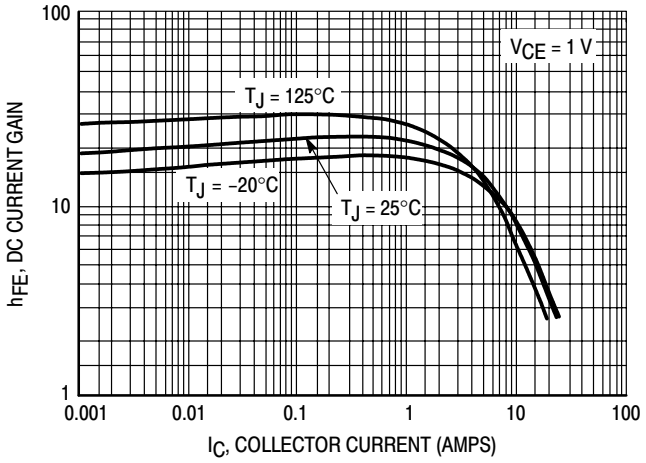


Figure 38. DC Current Gain @ 1 Volt

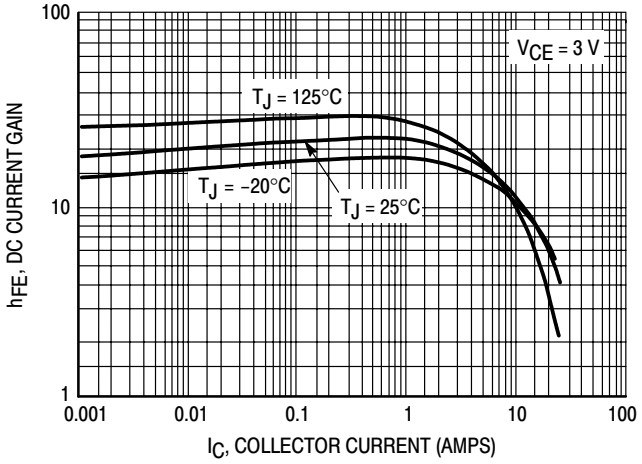


Figure 39. DC Current Gain @ 3 Volt

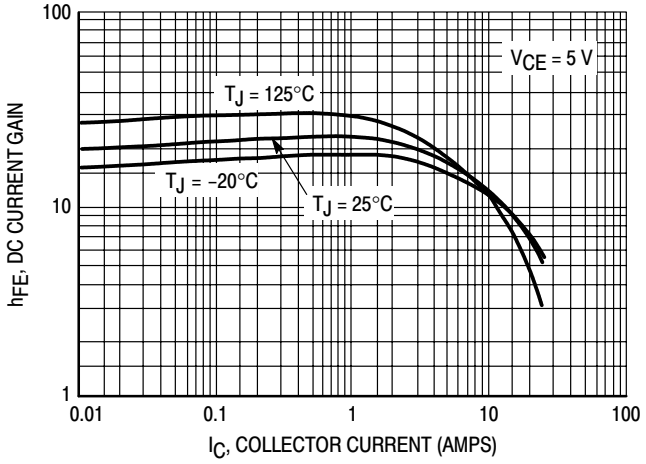


Figure 40. DC Current Gain @ 5 Volt

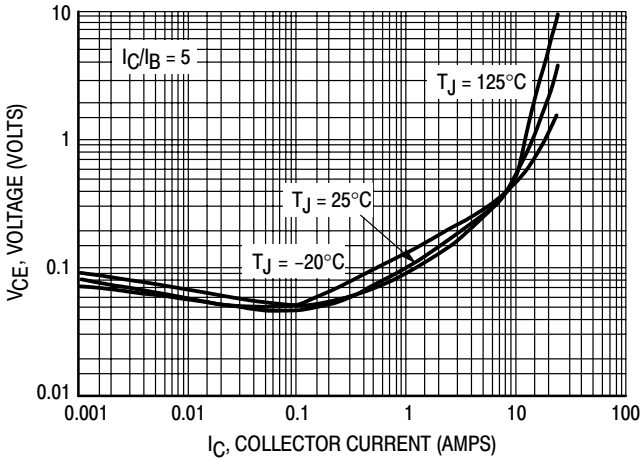


Figure 41. Collector−Emitter Saturation Voltage

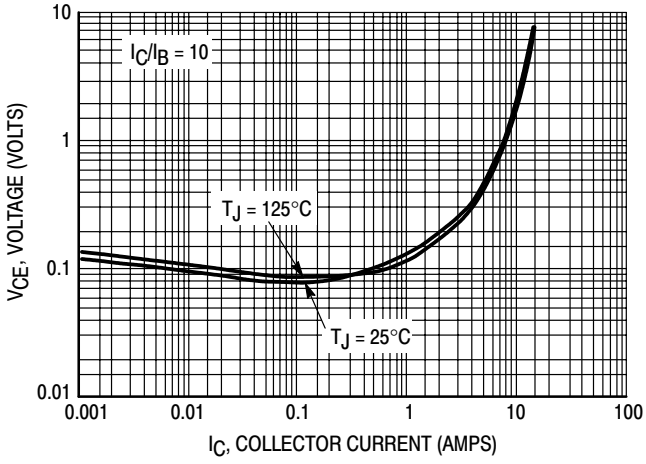


Figure 42. Collector−Emitter Saturation Voltage

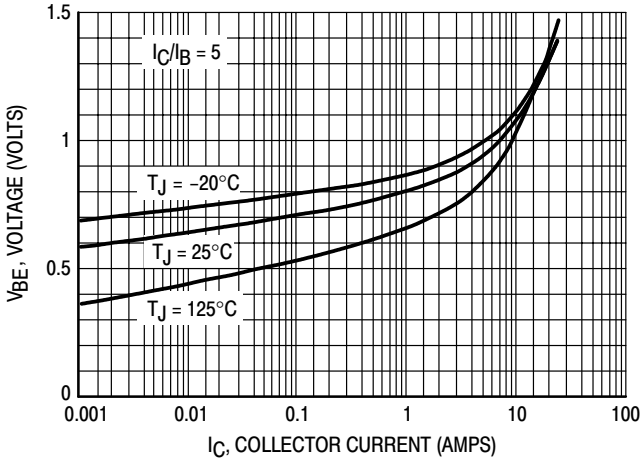


Figure 43. Base−Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

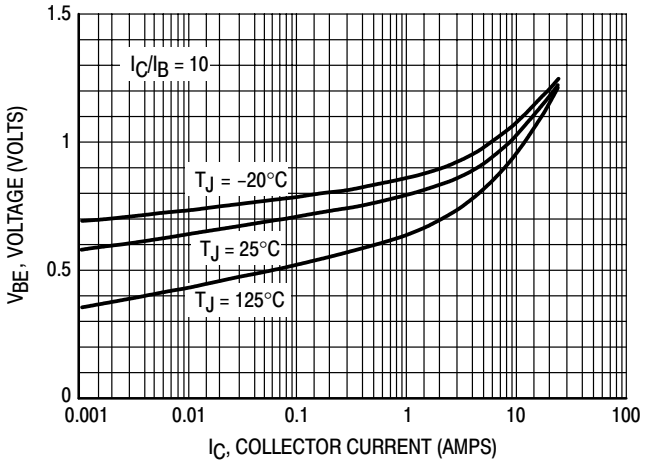


Figure 44. Base−Emitter Saturation Region

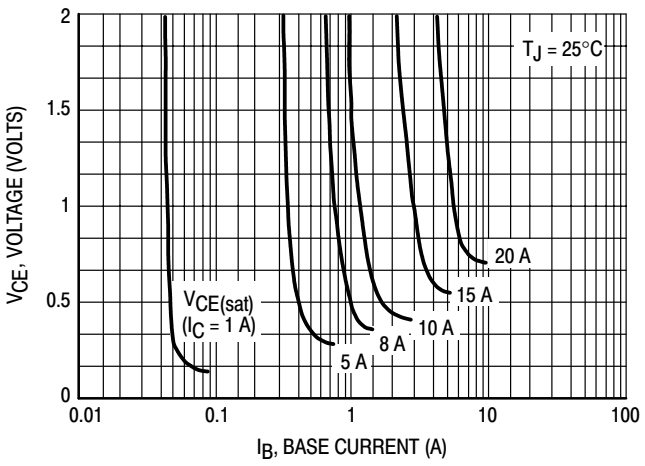


Figure 45. Collector Saturation Region

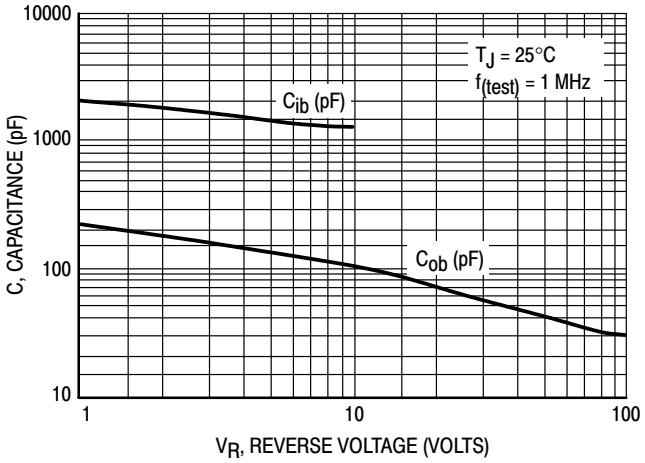


Figure 46. Capacitance

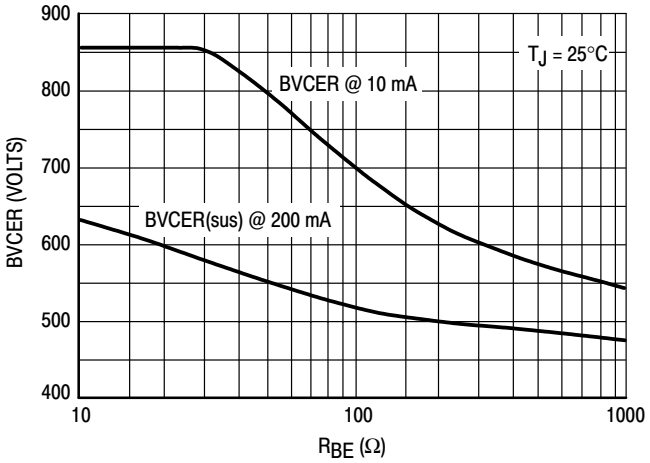


Figure 47. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

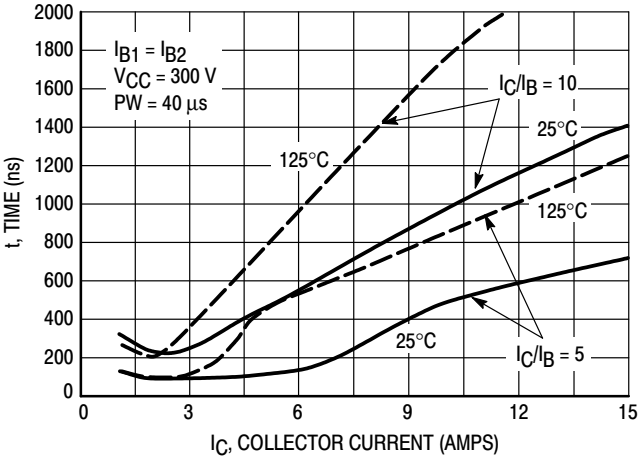


Figure 48. Resistive Switching, t_{on}

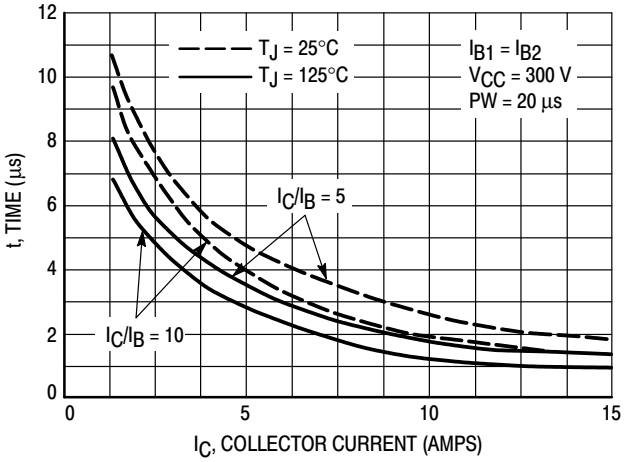


Figure 49. Resistive Switch Time, t_{off}

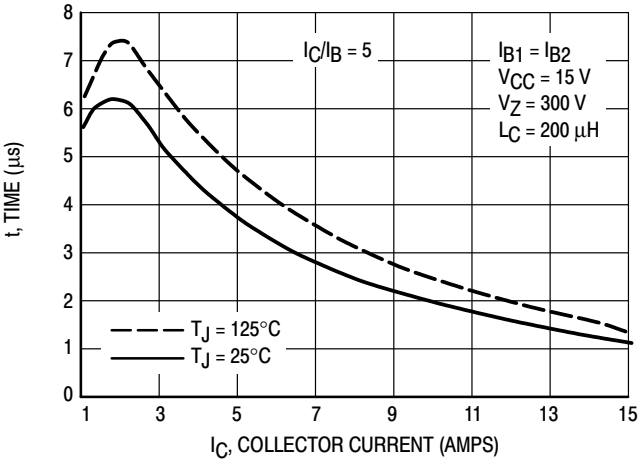


Figure 50. Inductive Storage Time, t_{si}

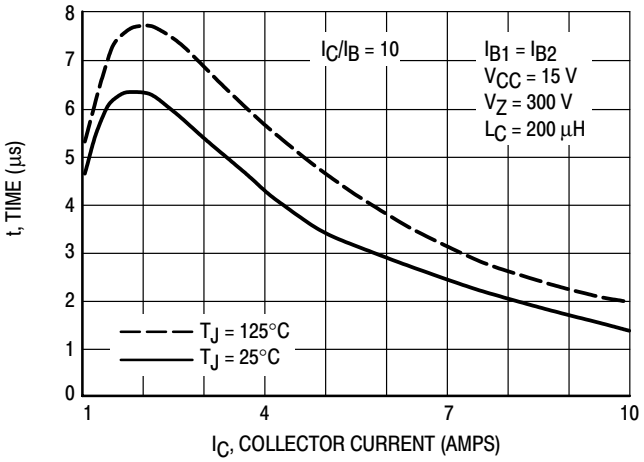


Figure 13 Bis. Inductive Storage Time, t_{si}

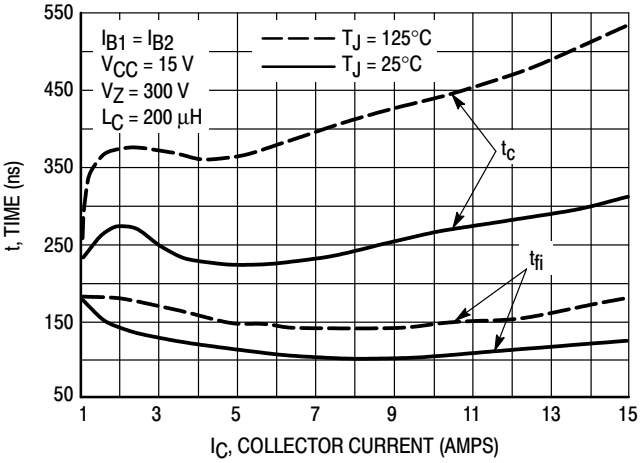


Figure 51. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

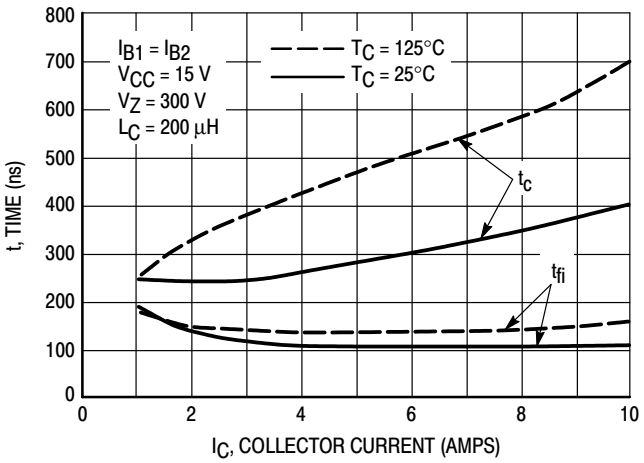


Figure 52. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

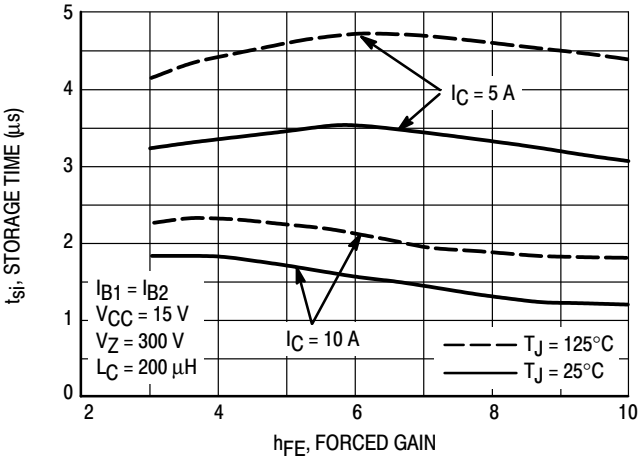


Figure 53. Inductive Storage Time

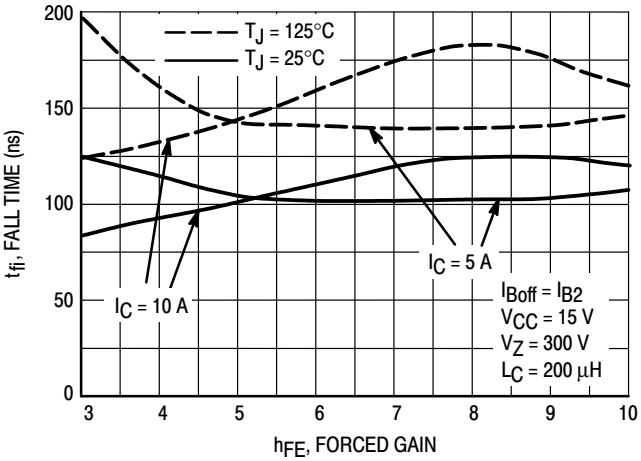


Figure 54. Inductive Fall Time

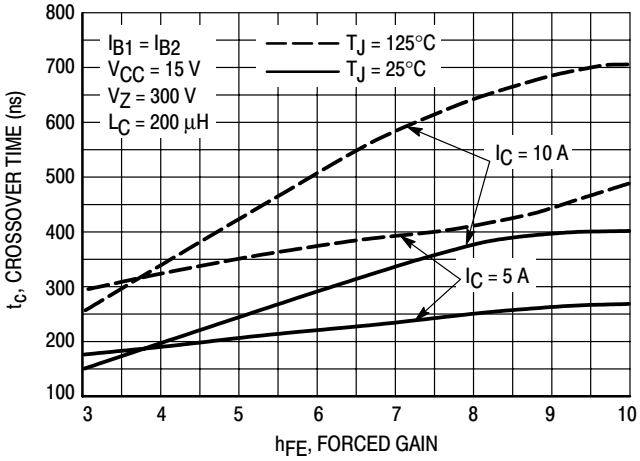


Figure 55. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

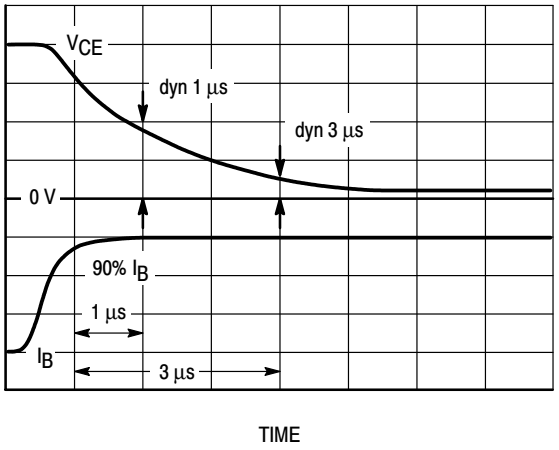


Figure 56. Dynamic Saturation Voltage Measurements

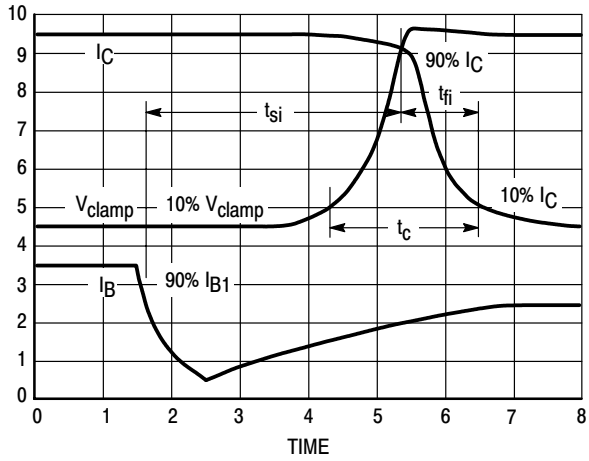
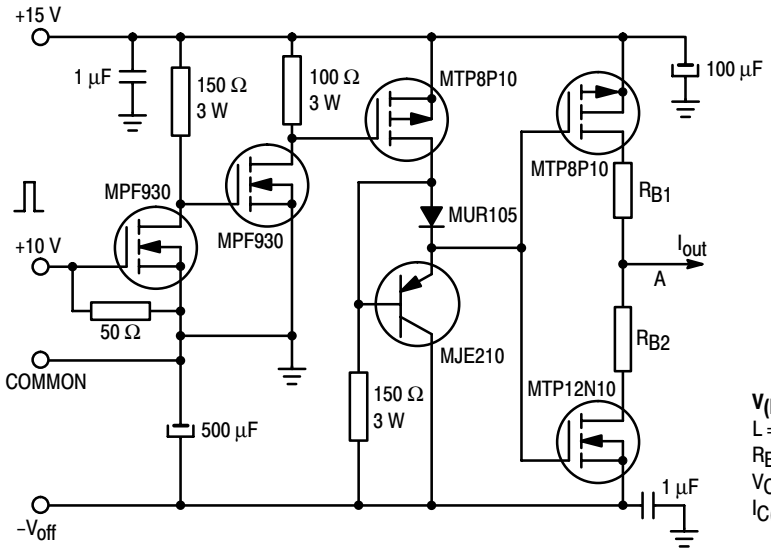
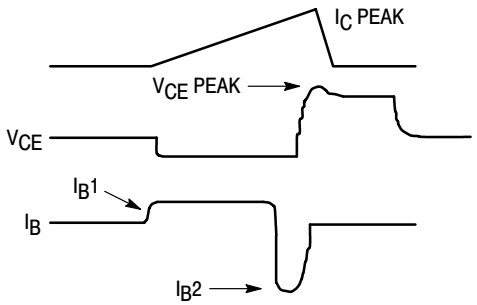


Figure 57. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

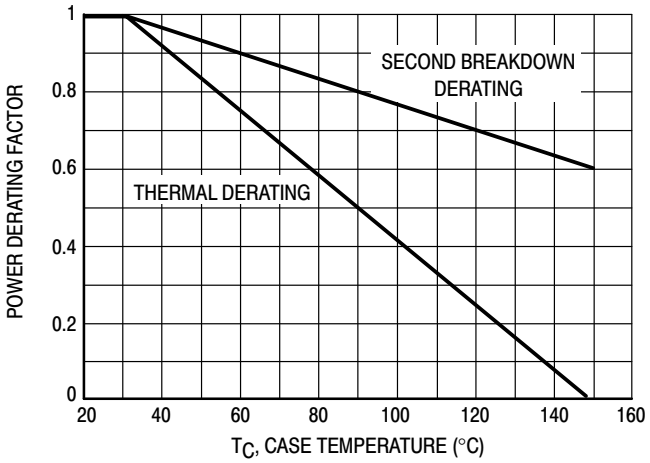


Figure 58. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 59 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 59 may be found at any case temperature by using the appropriate curve on Figure 58.

$T_{J(pk)}$ may be calculated from the data in Figure 61. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 60). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

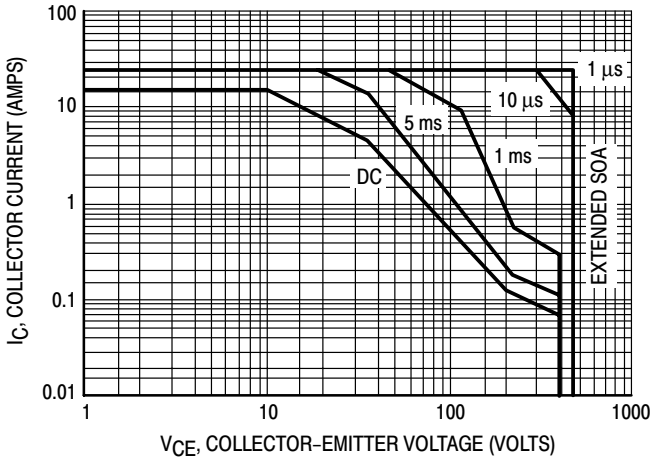


Figure 59. Forward Bias Safe Operating Area

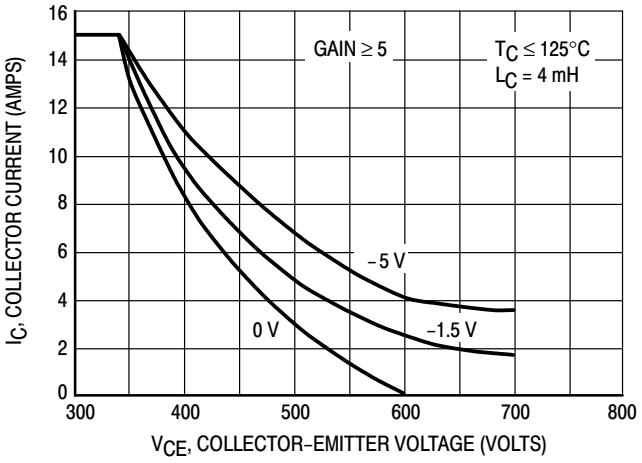


Figure 60. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

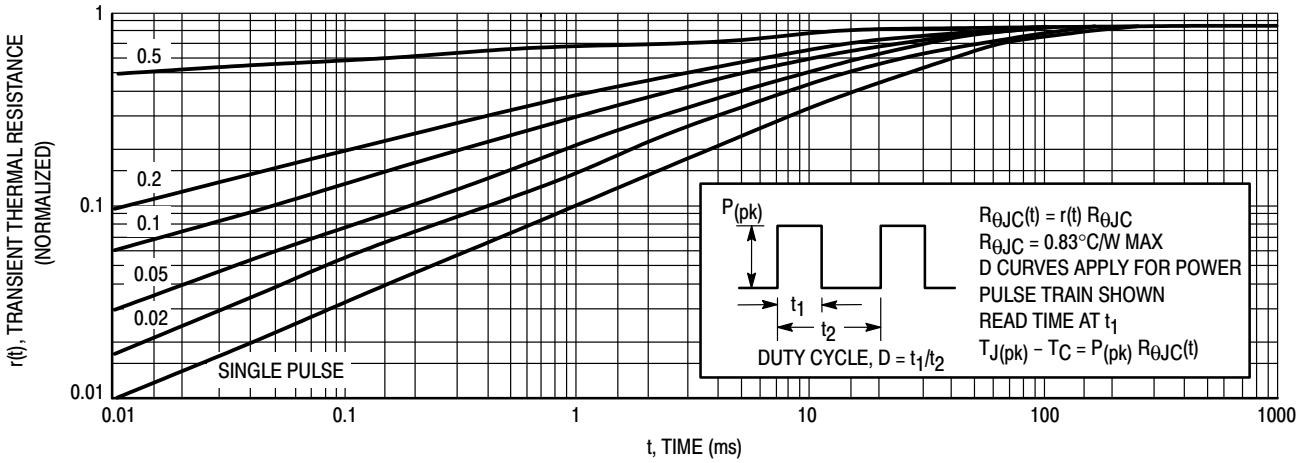


Figure 61. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH150

BUH50

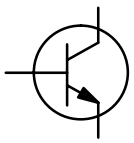
POWER TRANSISTOR
4 AMPERES
800 VOLTS
50 WATTS

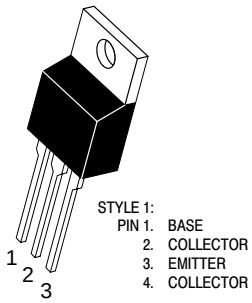
SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH50 has an application specific state−of−art die designed for use in 50 Watts HALOGEN electronic transformers and SWITCHMODE applications.

This high voltage/high speed transistor exhibits the following main feature:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproductible Parametric Distributions
- Specified Dynamic Saturation Data
- Full Characterization at 125°C





CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter−Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	500			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc) (I_C = 2 Adc, I_B = 0.66 Adc) 25°C (I_C = 2 Adc, I_B = 0.66 Adc) 100°C		$V_{BE(sat)}$		 0.86 0.94 0.85	 1.2 1.6 1.5	Vdc
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc)	@ T_C = 25°C	$V_{CE(sat)}$		0.2	0.5	Vdc
(I_C = 2 Adc, I_B = 0.66 Adc)	@ T_C = 25°C @ T_C = 125°C			0.32 0.29	0.6 0.7	
(I_C = 3 Adc, I_B = 1 Adc)	@ T_C = 25°C			0.5	1	
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C	h_{FE}	7	13		—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		5	10		—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4			MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		50	100	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}		850	1200	pF
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 A, I_{B1} = 0.33 A, V_{CC} = 300 V; @ 1 μs; @ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		1.75 5		V
	@ 3 μs; @ T_C = 25°C @ T_C = 125°C			0.3 0.5		V
	I_C = 2 A, I_{B1} = 0.66 A, V_{CC} = 300 V; @ 1 μs; @ T_C = 25°C @ T_C = 125°C			6 14		V
	@ 3 μs; @ T_C = 25°C @ T_C = 125°C			0.75 4		V

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		95	250	ns
Turn−off Time		@ T_C = 25°C	t_{off}		2.5	3.5	μs
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		110	250	ns
Turn−off Time		@ T_C = 25°C	t_{off}		0.95	2	μs
Turn−on Time	I_C = 1 Adc, I_{B1} = 0.3 Adc I_{B2} = 0.3 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		100	200	ns
Turn−off Time		@ T_C = 25°C	t_{off}		2.9	3.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		80 95	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.2 1.7	2.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 180	300	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.66 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		90 100	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.7 2.5	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		190 220	350	ns

TYPICAL STATIC CHARACTERISTICS

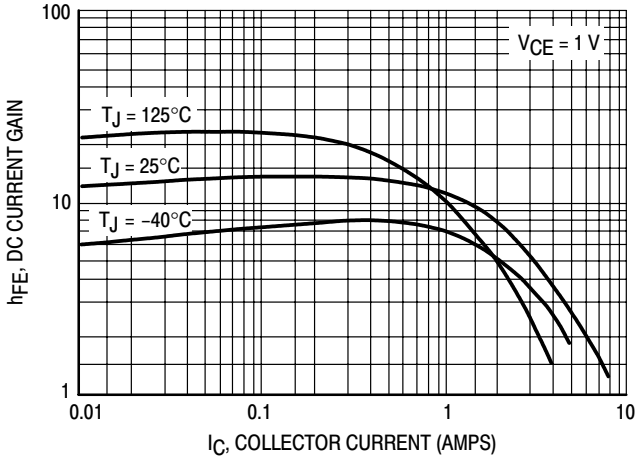


Figure 62. DC Current Gain @ 1 Volt

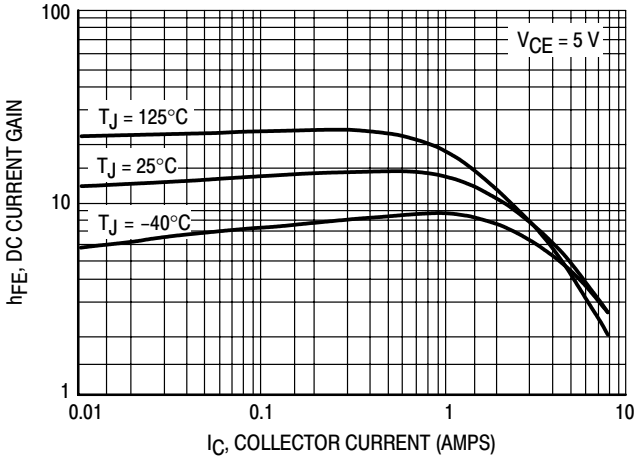


Figure 63. DC Current Gain @ 5 Volt

TYPICAL STATIC CHARACTERISTICS

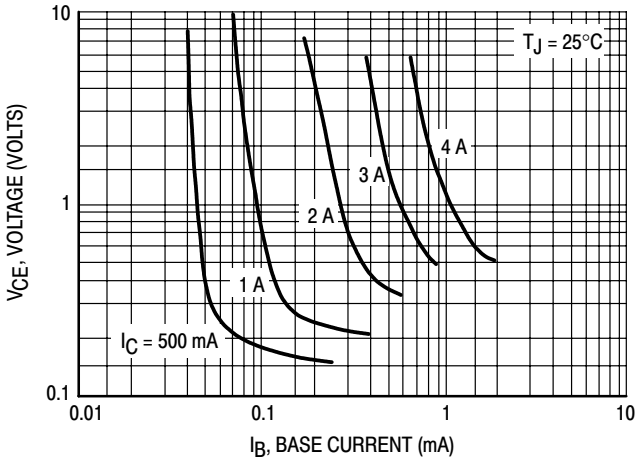


Figure 64. Collector Saturation Region

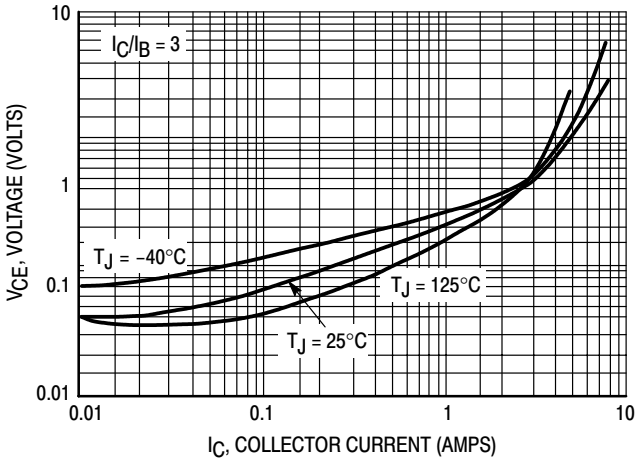


Figure 65. Collector−Emitter Saturation Voltage

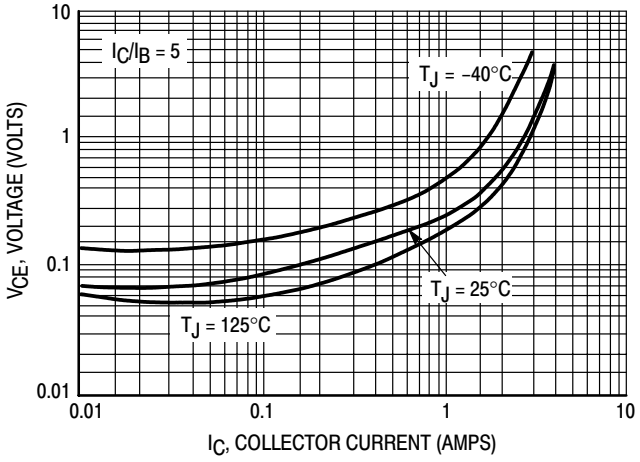


Figure 66. Collector−Emitter Saturation Voltage

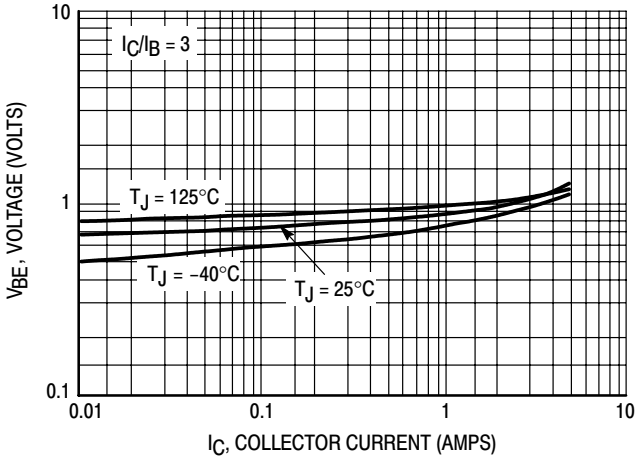


Figure 67. Base−Emitter Saturation Region

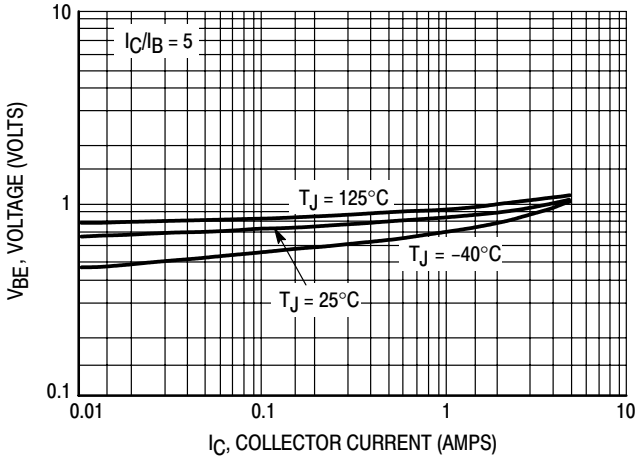


Figure 68. Base−Emitter Saturation Region

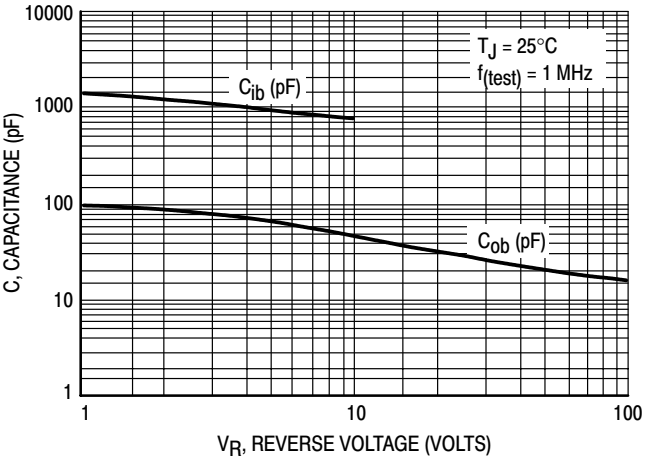


Figure 69. Capacitance

TYPICAL SWITCHING CHARACTERISTICS

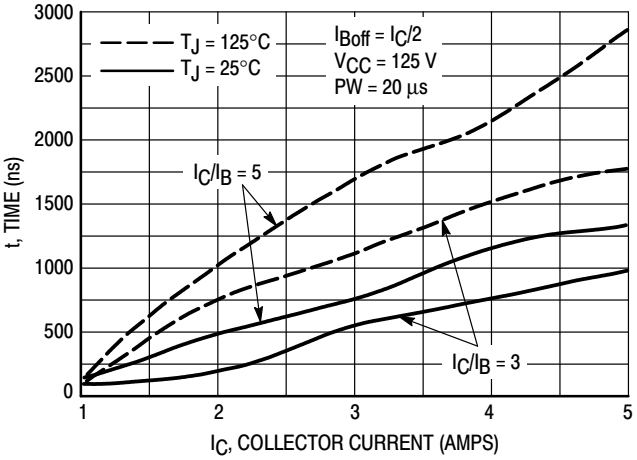


Figure 70. Resistive Switching, t_{on}

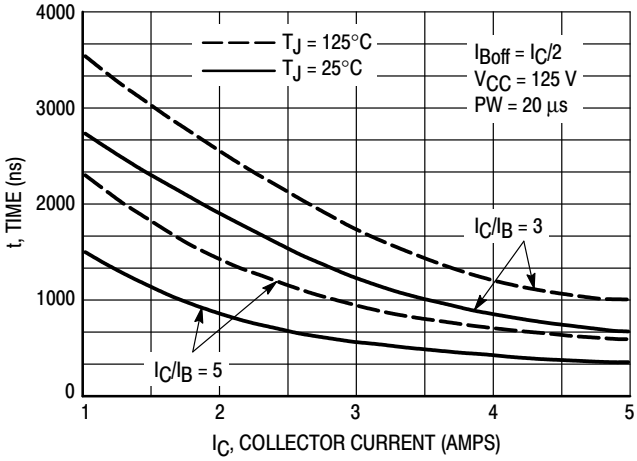


Figure 71. Resistive Switch Time, t_{off}

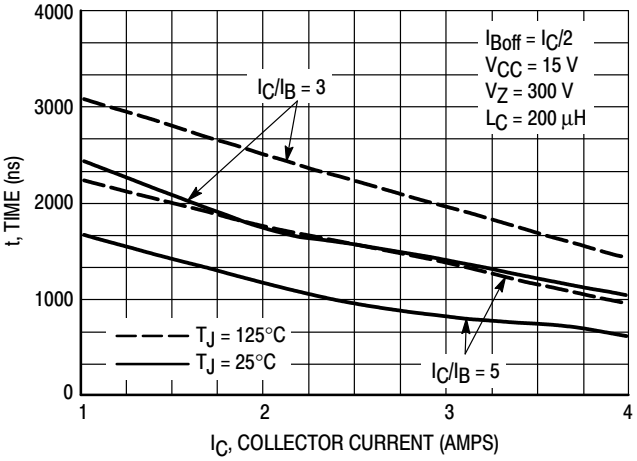


Figure 72. Inductive Storage Time, t_{si}

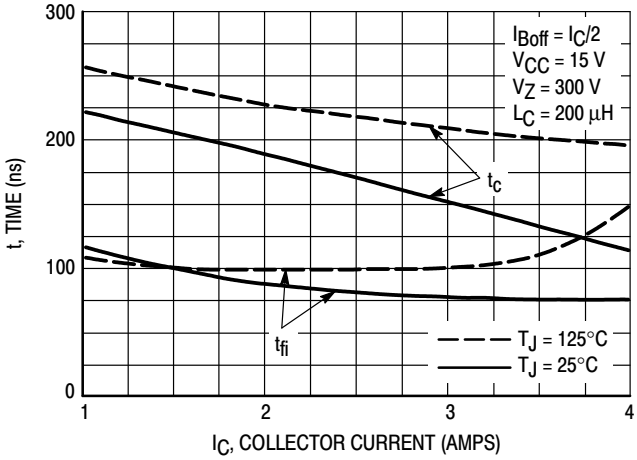


Figure 73. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 3

TYPICAL CHARACTERISTICS

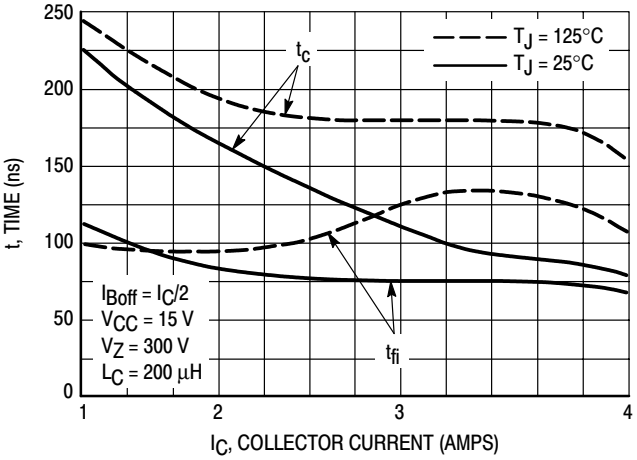


Figure 74. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

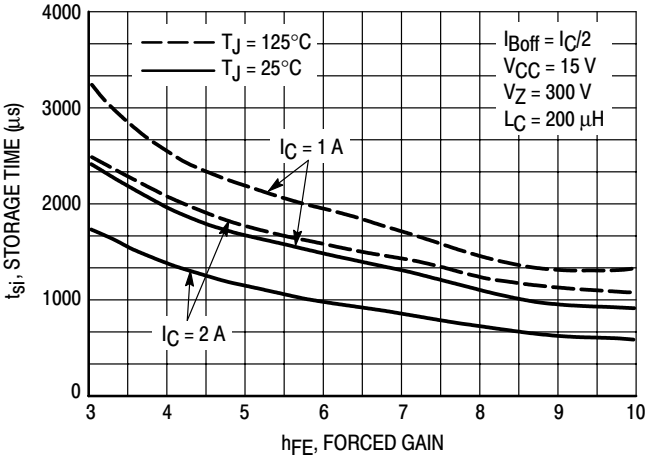


Figure 75. Inductive Storage Time

TYPICAL CHARACTERISTICS

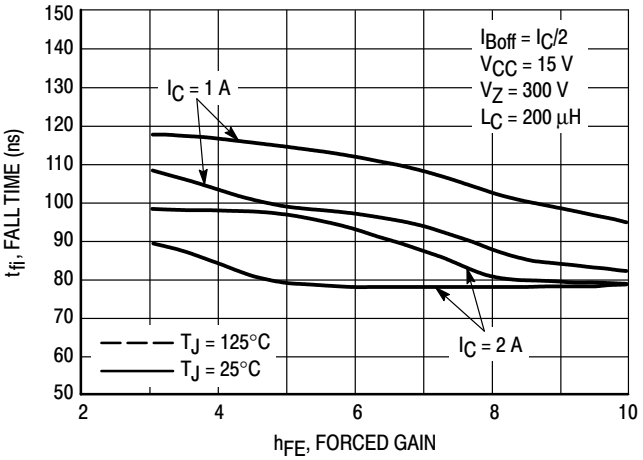


Figure 76. Inductive Fall Time

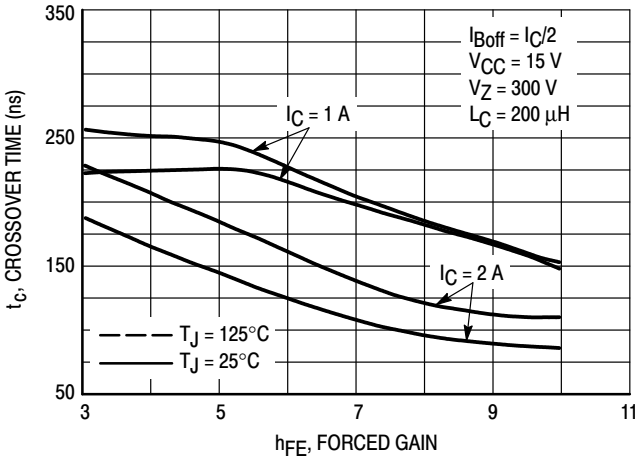


Figure 77. Inductive Crossover Time

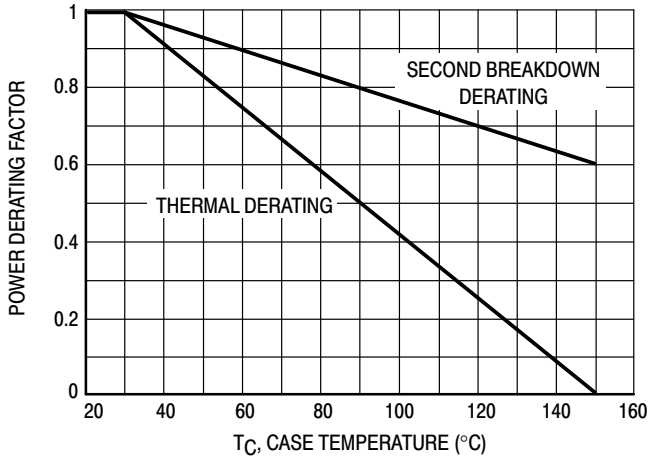


Figure 78. Forward Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 81 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 81 may be found at any case temperature by using the appropriate curve on Figure 78.

$T_{J(pk)}$ may be calculated from the data in Figure 83. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 82). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL CHARACTERISTICS

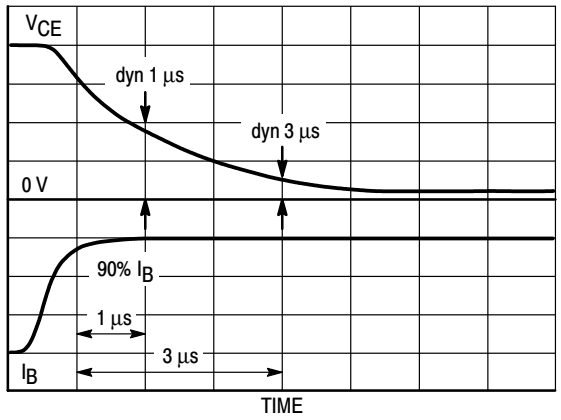


Figure 79. Dynamic Saturation Voltage

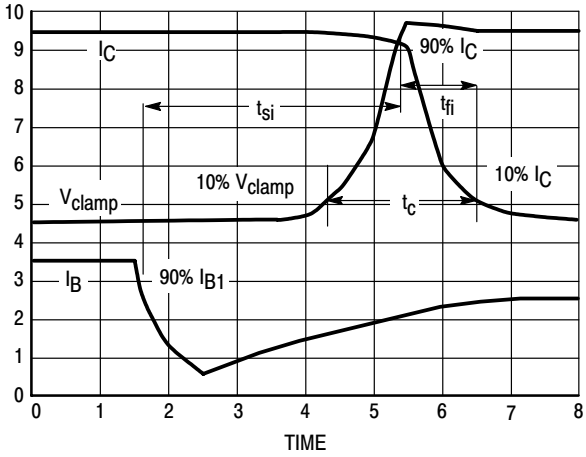


Figure 80. Inductive Switching Measurements

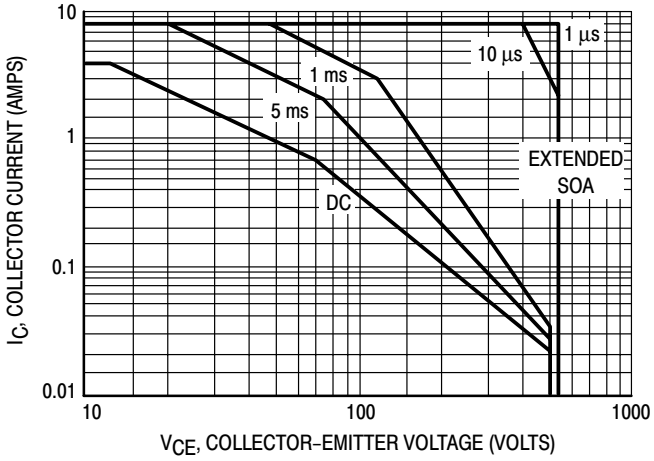


Figure 81. Forward Bias Safe Operating Area

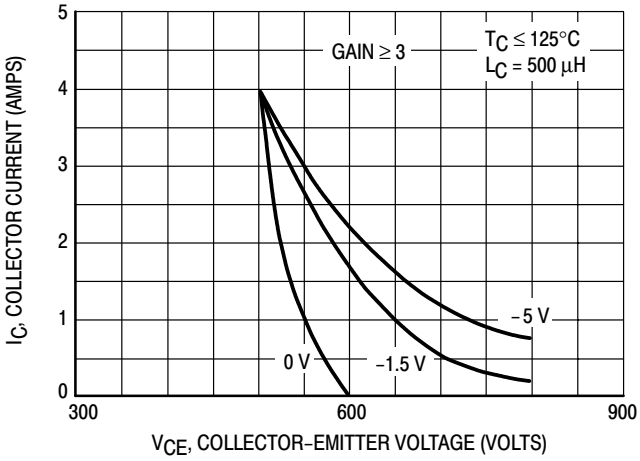
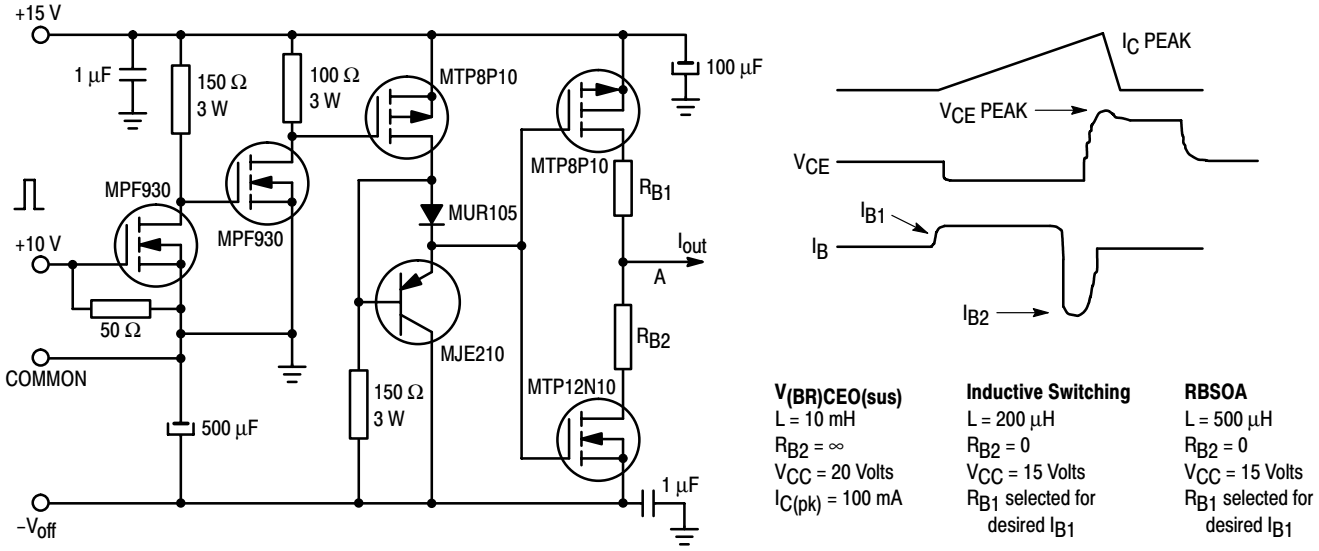


Figure 82. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



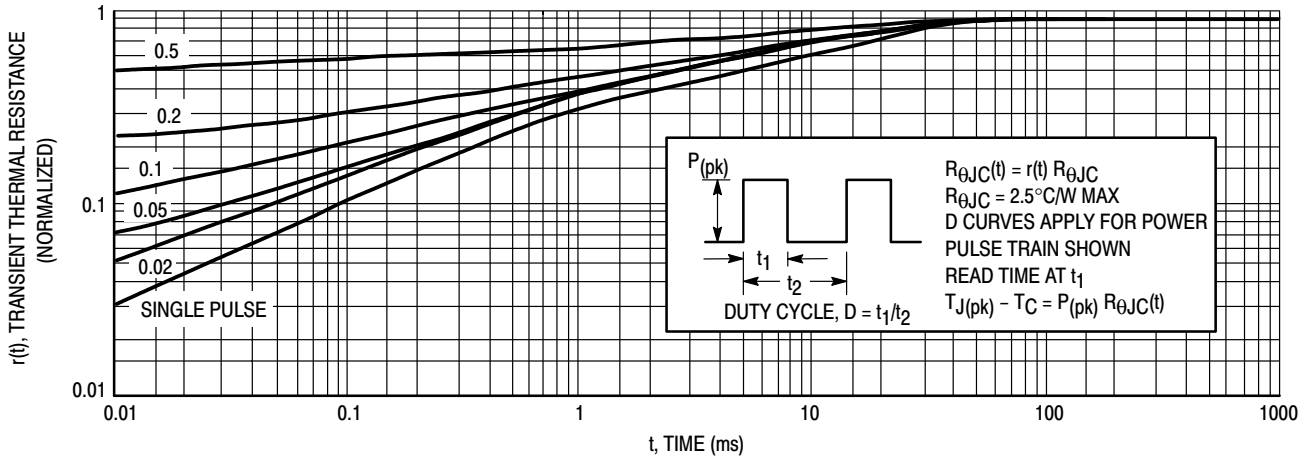


Figure 83. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH50

BUH51

SWITCHMODE™ NPN Silicon Planar Power Transistor

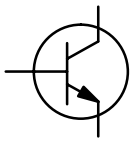
POWER TRANSISTOR
3 AMPERES
800 VOLTS
50 WATTS

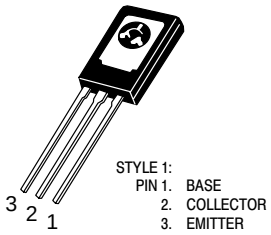
The BUH51 has an application specific state−of−art die designed for use in 50 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start−up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  High and Flat DC Current Gain h_{FE}
  Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Providing Tight and Reproducible
  Parametric Distributions





CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter−Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	3 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 100	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	500	550		Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	800	950		Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.92 0.8	1.1	Vdc
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.3 0.32	0.5 0.6	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	8 6	10 8		—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		5 4	7.5 6.2		—
(I_C = 0.8 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 8	14 13		—
(I_C = 10 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		14 18	20 25		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc, I_{B1} = 0.2 Adc, V_{CC} = 300V	@ T_C = 25°C	$V_{CE(dsat)}$		1.7		V
		@ T_C = 125°C			6		V
	I_C = 2 Adc, I_{B1} = 0.4 Adc, V_{CC} = 300V	@ T_C = 25°C			5.1		V
		@ T_C = 125°C			15		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		34	100	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		200	500	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn−on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		110 125	150	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.5 4.1	4	μs
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		700 1250	1000	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.75 2.1	2	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		200 320	300	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		3.4 4	3.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		350 640	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		140 300	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.3 2.8	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		400 725	600	ns

TYPICAL STATIC CHARACTERISTICS

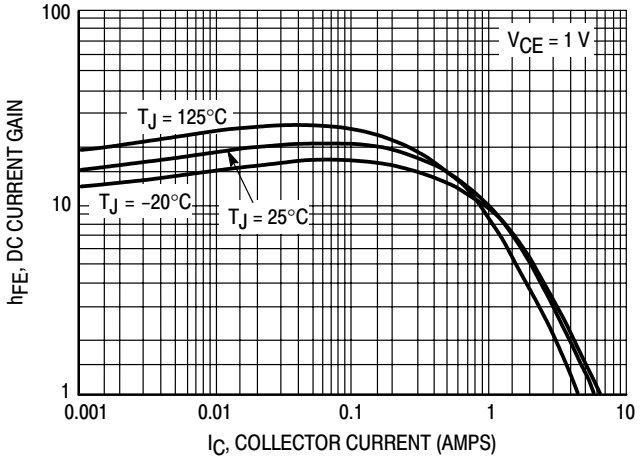


Figure 84. DC Current Gain @ 1 Volt

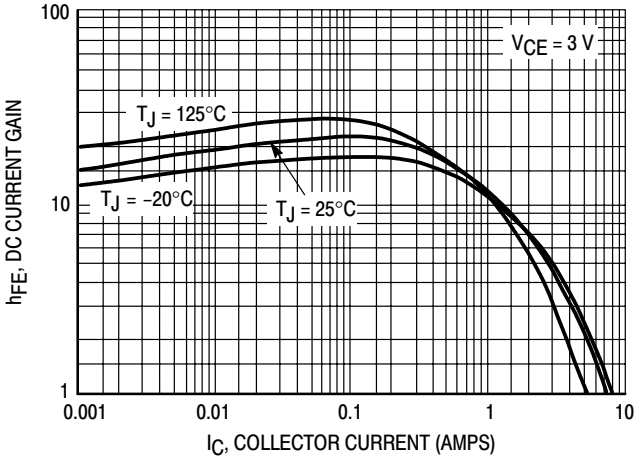


Figure 85. DC Current Gain @ 3 Volt

TYPICAL STATIC CHARACTERISTICS

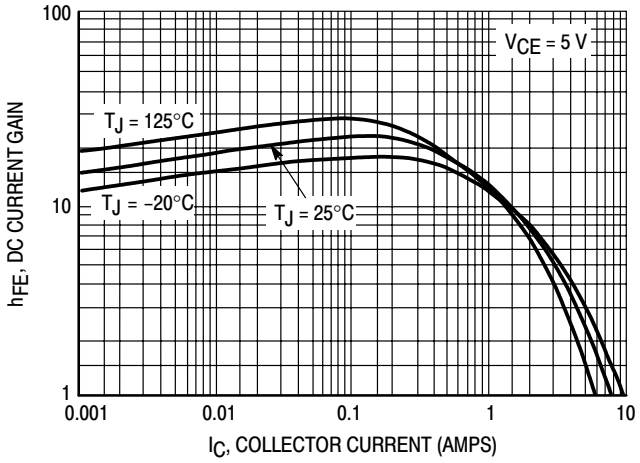


Figure 86. DC Current Gain @ 5 Volt

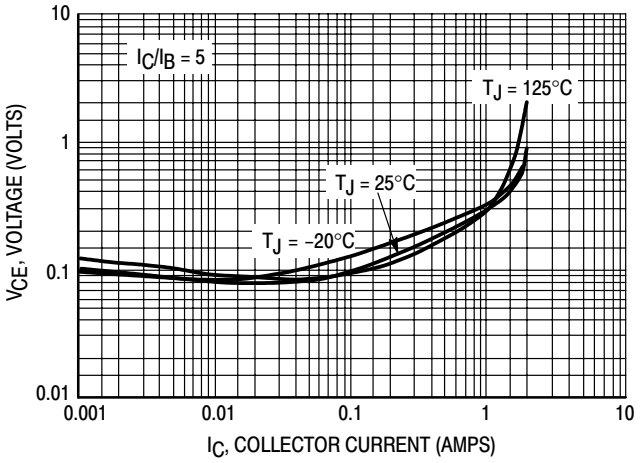


Figure 87. Collector−Emitter Saturation Voltage

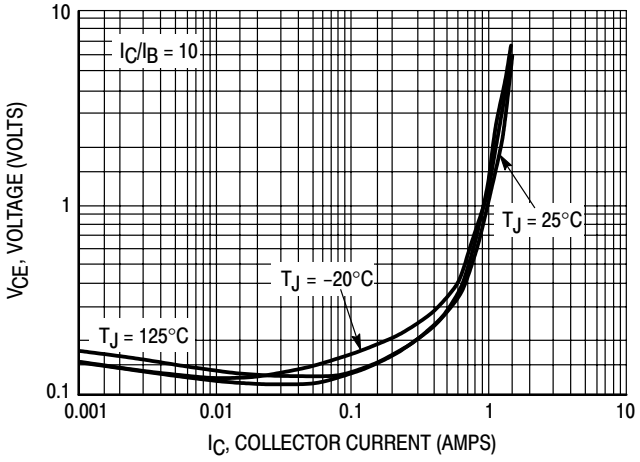


Figure 88. Collector−Emitter Saturation Voltage

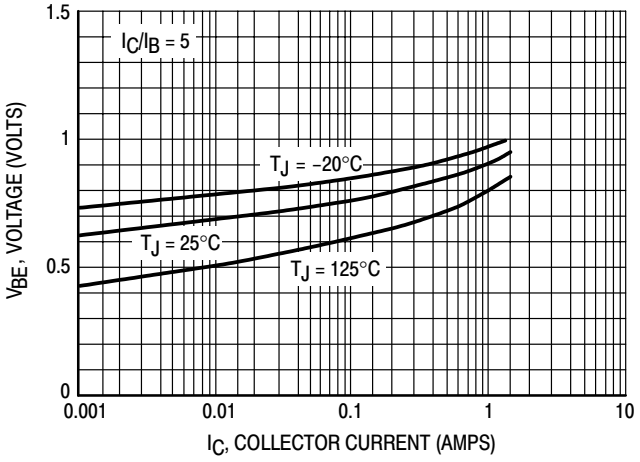


Figure 89. Base−Emitter Saturation Region

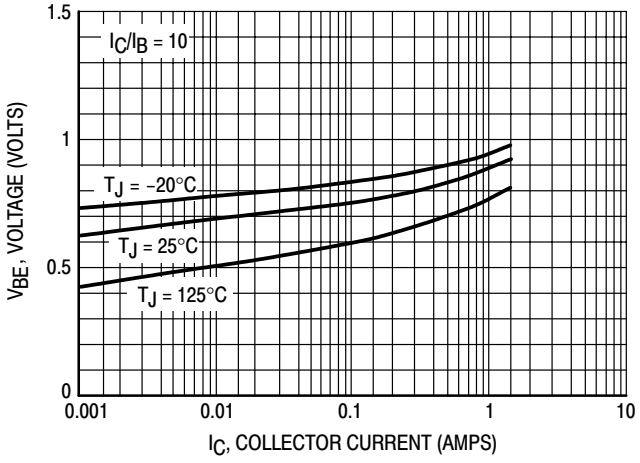


Figure 90. Base−Emitter Saturation Region

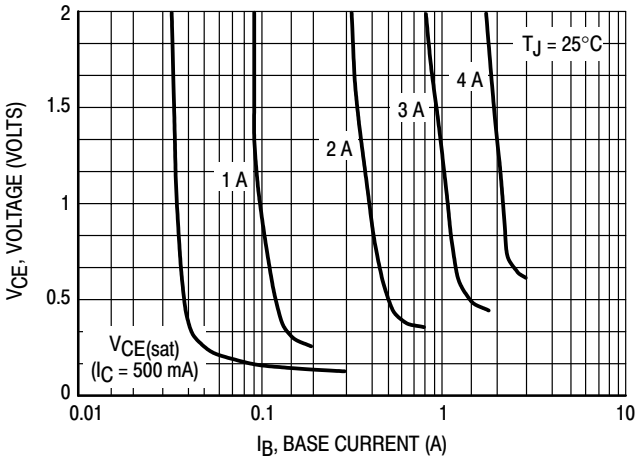


Figure 91. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

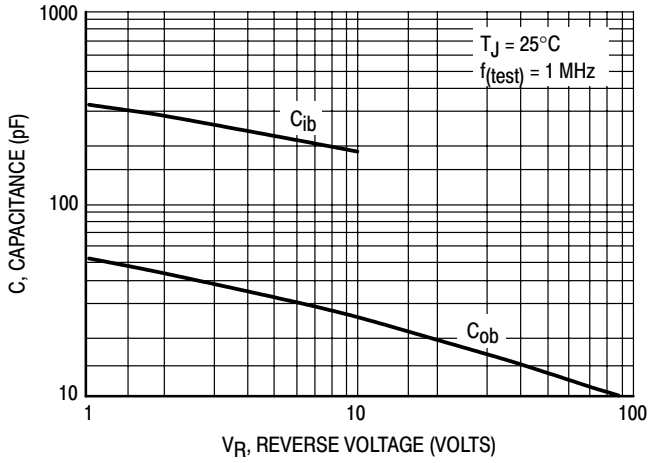


Figure 92. Capacitance

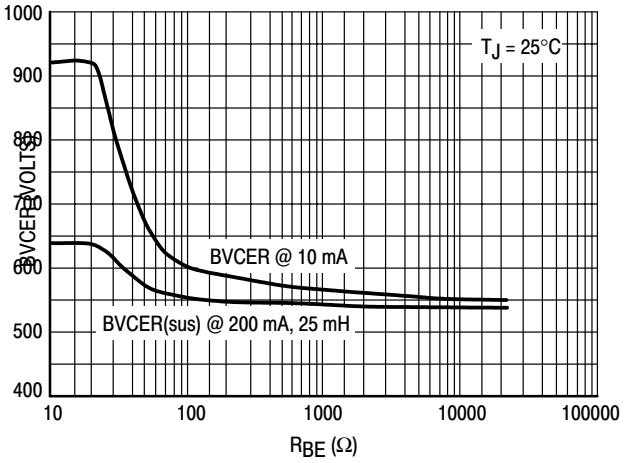


Figure 93. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

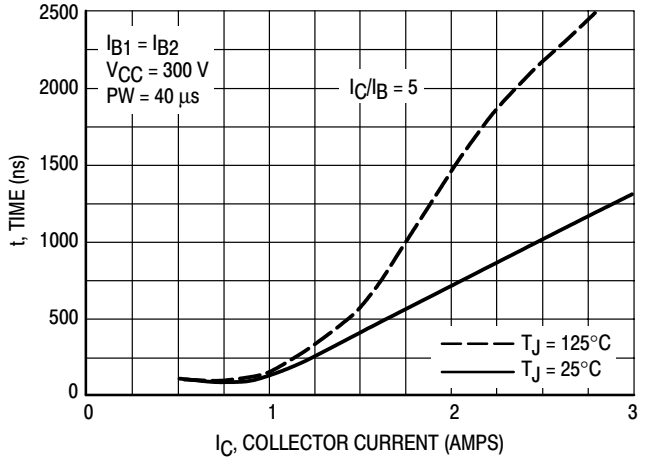


Figure 94. Resistive Switching, t_{on}

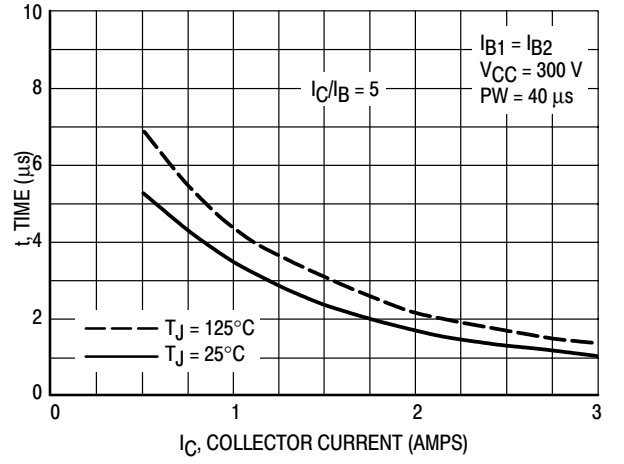


Figure 95. Resistive Switch Time, t_{off}

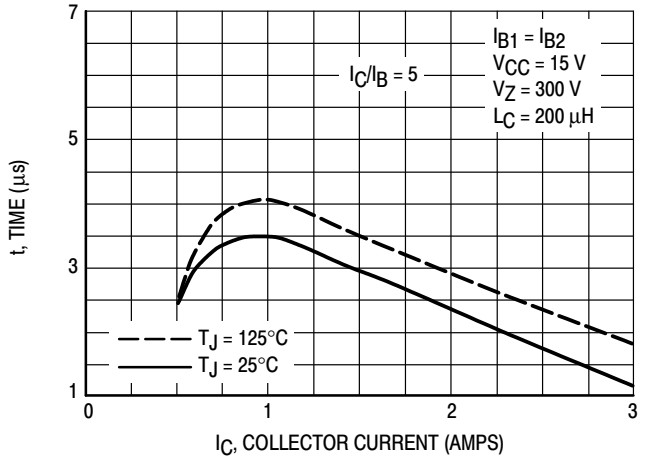


Figure 96. Inductive Storage Time, t_{si}

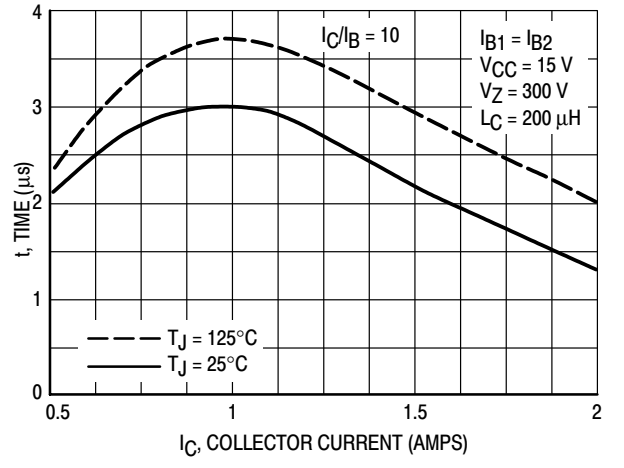


Figure 13 Bis. Inductive Storage Time, t_{si}

TYPICAL SWITCHING CHARACTERISTICS

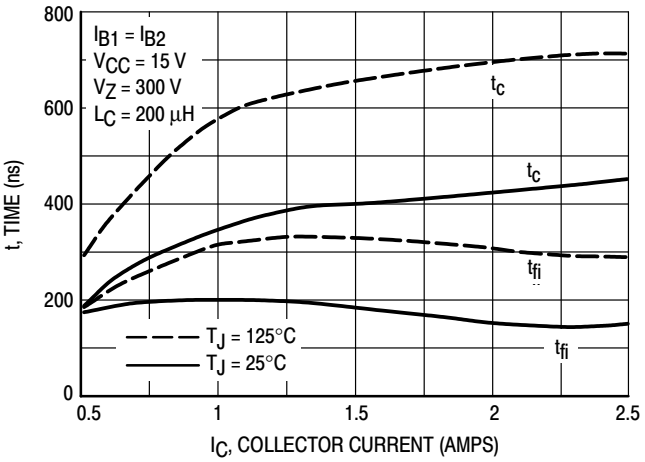


Figure 97. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

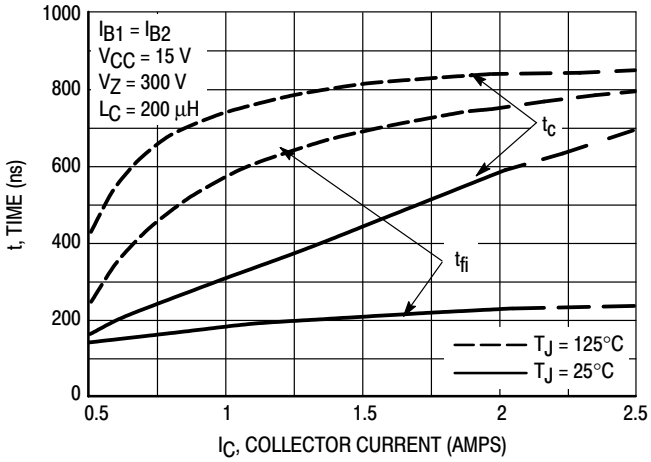


Figure 98. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

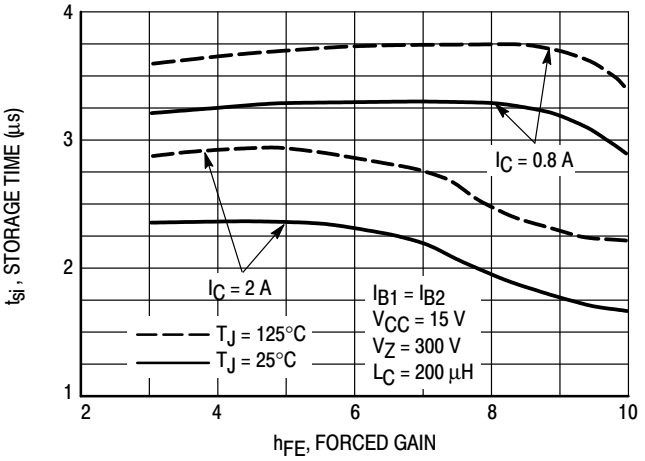


Figure 99. Inductive Storage Time

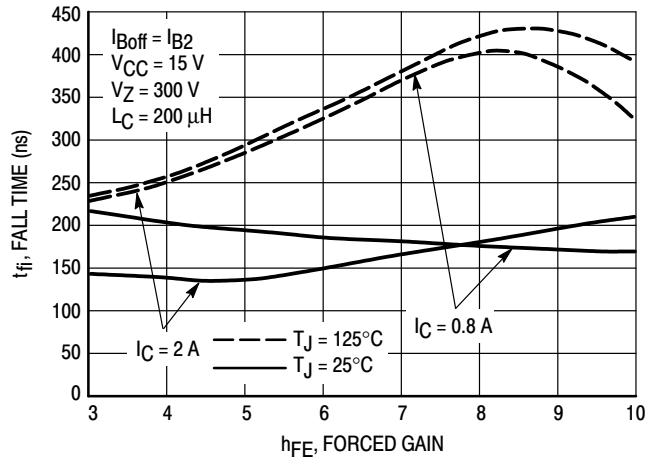


Figure 100. Inductive Fall Time

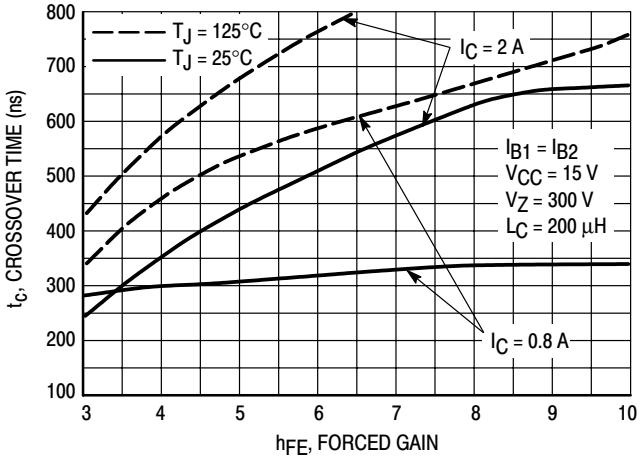


Figure 101. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

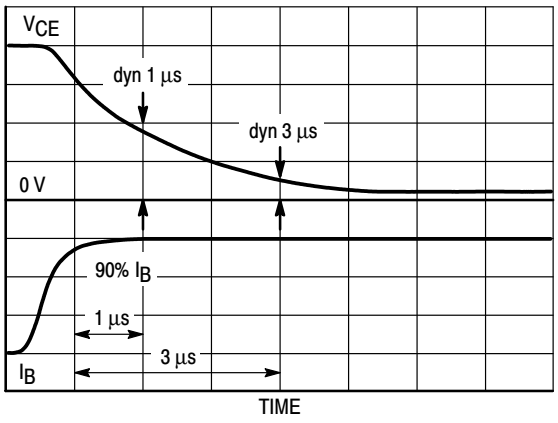


Figure 102. Dynamic Saturation Voltage Measurements

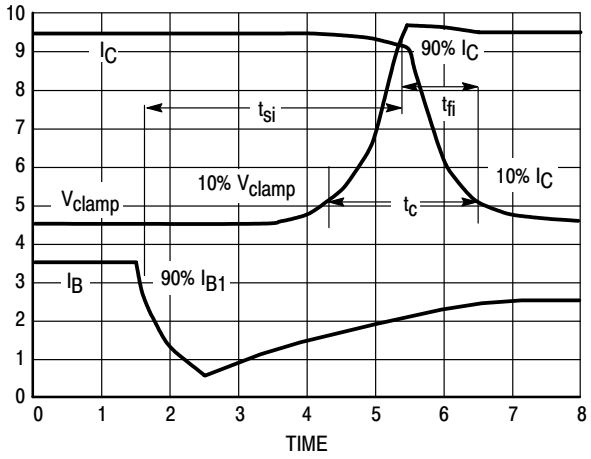
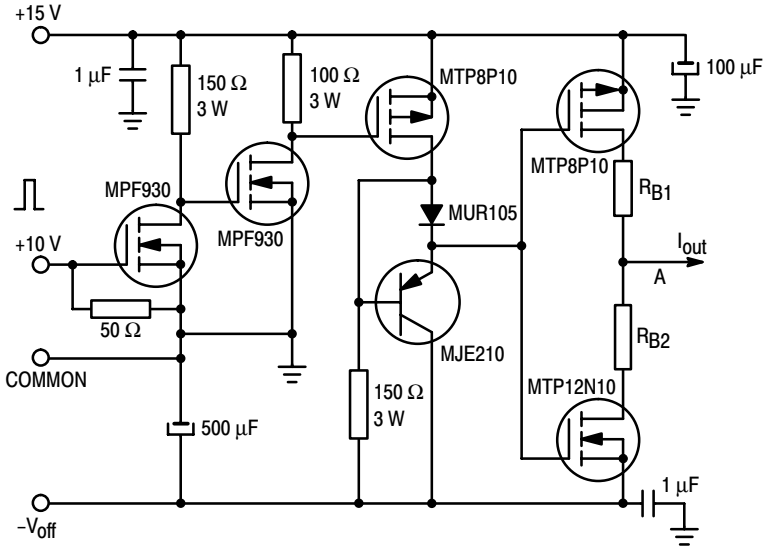
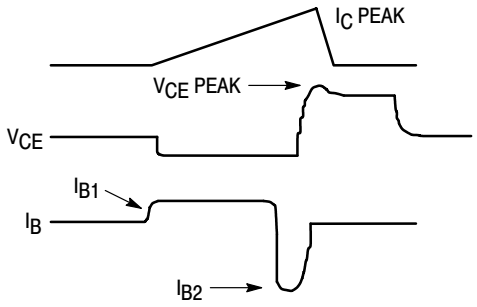


Figure 103. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

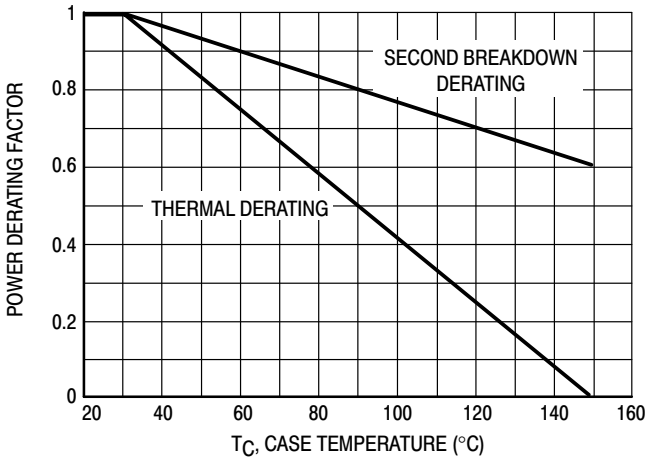


Figure 104. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 105 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 105 may be found at any case temperature by using the appropriate curve on Figure 104.

$T_{J(pk)}$ may be calculated from the data in Figure 107. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 106). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

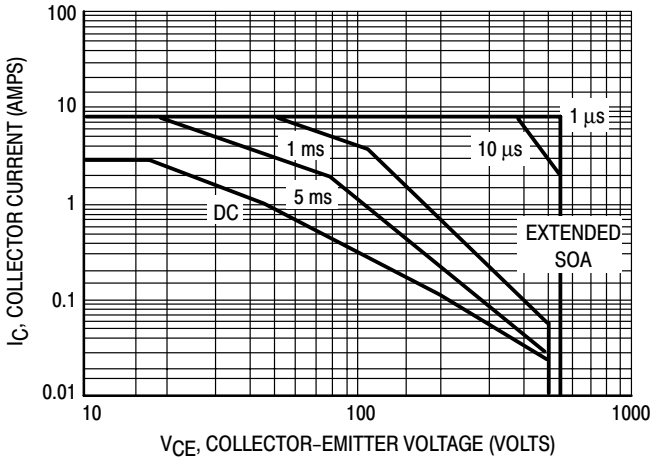


Figure 105. Forward Bias Safe Operating Area

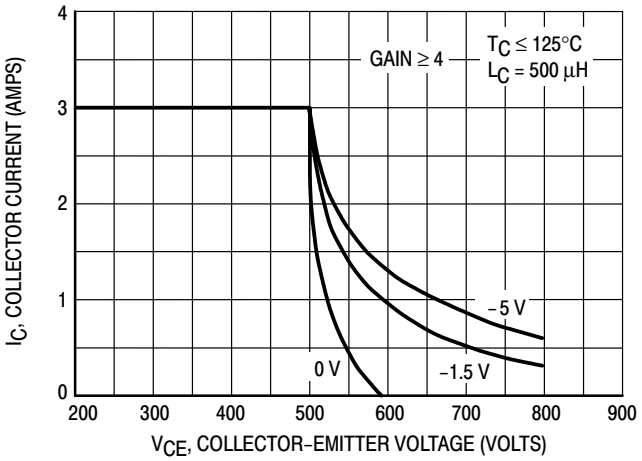


Figure 106. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

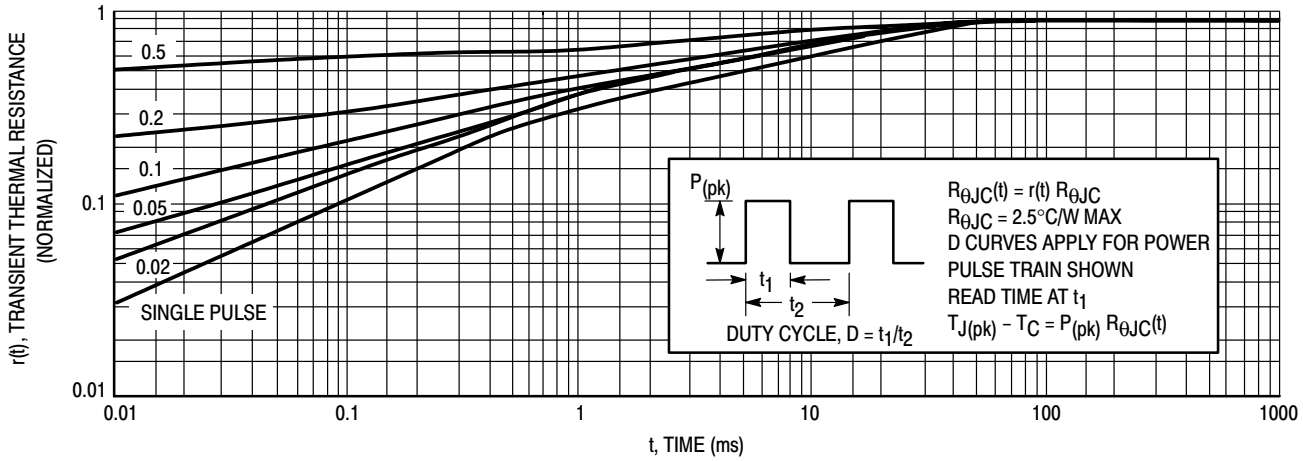


Figure 107. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH51

BUL146
BUL146F

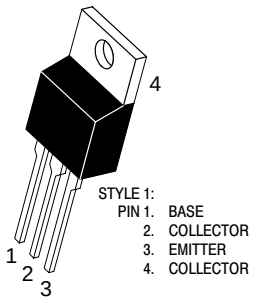
POWER TRANSISTOR
6.0 AMPERES
700 VOLTS
40 and 100 WATTS

SWITCHMODE™

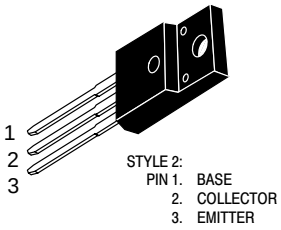
NPN Bipolar Power Transistor For Switching Power Supply Applications

The BUL146/BUL146F have an applications specific state−of−the−art die designed for use in fluorescent electric lamp ballasts to 130 Watts and in Switchmode Power supplies for all types of electronic equipment. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Full Characterization at 125°C
- Two Packages Choices: Standard TO220 or Isolated TO220
- Parametric Distributions are Tight and Consistent Lot−to−Lot
- BUL146F, Case 221D, is UL Recognized to 3500 V_{RMS}: File # E69369



BUL146
CASE 221A−09
TO−220AB



CASE 221D−02
ISOLATED TO−220 TYPE
BUL146F

MAXIMUM RATINGS

Rating	Symbol	BUL146	BUL146F	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter−Base Voltage	V_{EBO}	9.0		Vdc
Collector Current − Continuous − Peak(1)	I_C I_{CM}	6.0 15		Adc
Base Current − Continuous − Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolation Voltage: (2) (for 1 sec, R.H. $\leq$ 30%, T_C = 25° C)	V_{ISOL1} V_{ISOL2} V_{ISOL3}	− − −	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	40 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	− 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL146	BUL146F	Unit
Thermal Resistance − Junction to Case − Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	−	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	−	−	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	−	−	100	μAdc
(T_C = 125°C)		−	−	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		−	−	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	−	−	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS − (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Base−Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc)	$V_{BE(sat)}$	−	0.82	1.1	Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)		−	0.93	1.25	
Collector−Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc)	$V_{CE(sat)}$	−	0.22	0.5	Vdc
(T_C = 125°C)		−	0.20	0.5	
(I_C = 3.0 Adc, I_B = 0.6 Adc)		−	0.30	0.7	
(T_C = 125°C)		−	0.30	0.7	
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	−	34	−
(T_C = 125°C)		−	30	−	
(I_C = 1.3 Adc, V_{CE} = 1.0 Vdc)		12	20	−	
(T_C = 125°C)		12	20	−	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		8.0	13	−	
(T_C = 125°C)		7.0	12	−	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	−	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	−	14	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{OB}	−	95	150	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{IB}	−	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18) — (I_C = 1.3 Adc I_{B1} = 300 mAdc V_{CC} = 300 V) — 1.0 μs	$V_{CE(dsat)}$	−	2.5	−	V
(T_C = 125°C)		−	6.5	−	
3.0 μs		−	0.6	−	
(T_C = 125°C)		−	2.5	−	
(I_C = 3.0 Adc I_{B1} = 0.6 Adc V_{CC} = 300 V) — 1.0 μs		−	3.0	−	
(T_C = 125°C)		−	7.0	−	
3.0 μs		−	0.75	−	
(T_C = 125°C)		−	1.4	−	

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn−On Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	− −	100 90	200 −	ns
Turn−Off Time	(T_C = 125°C)	t_{off}	− −	1.35 1.90	2.5 −	μs
Turn−On Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B1} = 1.5 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	− −	90 100	150 −	ns
Turn−Off Time	(T_C = 125°C)	t_{off}	− −	1.7 2.1	2.5 −	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc) (T_C = 125°C)	t_{fi}	− −	115 120	200 −	ns
Storage Time	(T_C = 125°C)	t_{si}	− −	1.35 1.75	2.5 −	μs
Crossover Time	(T_C = 125°C)	t_c	− −	200 210	350 −	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B2} = 1.5 Adc) (T_C = 125°C)	t_{fi}	− −	85 100	150 −	ns
Storage Time	(T_C = 125°C)	t_{si}	− −	1.75 2.25	2.5 −	μs
Crossover Time	(T_C = 125°C)	t_c	− −	175 200	300 −	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B2} = 0.6 Adc) (T_C = 125°C)	t_{fi}	80 −	− 210	180 −	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 −	− 4.5	3.8 −	μs
Crossover Time	(T_C = 125°C)	t_c	− −	230 400	350 −	ns

TYPICAL STATIC CHARACTERISTICS

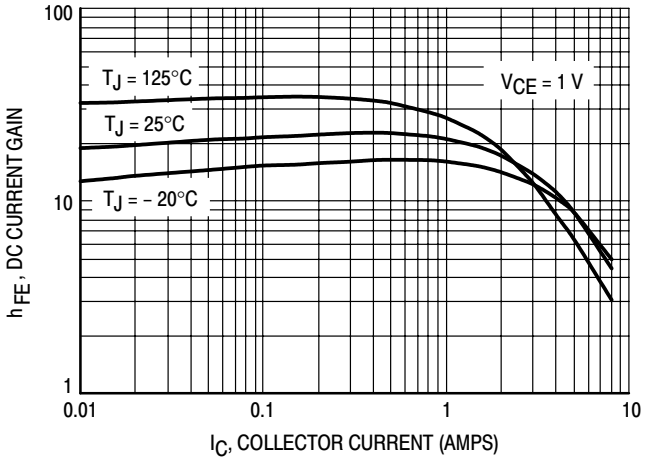


Figure 1. DC Current Gain @ 1 Volt

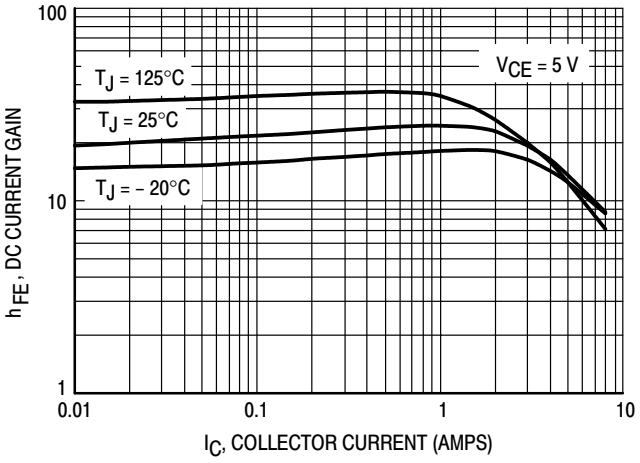


Figure 2. DC Current Gain @ 5 Volts

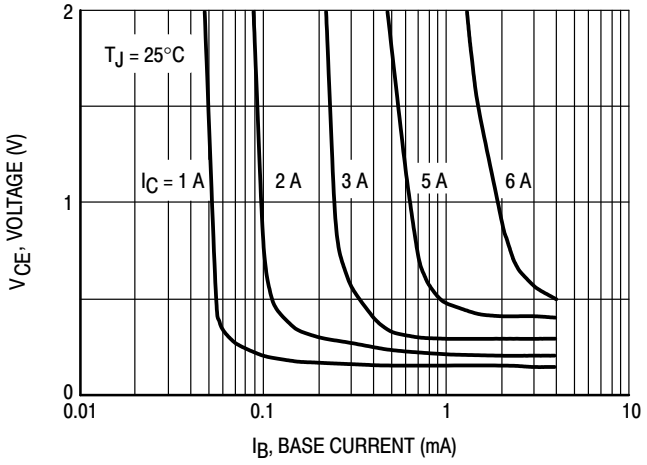


Figure 3. Collector Saturation Region

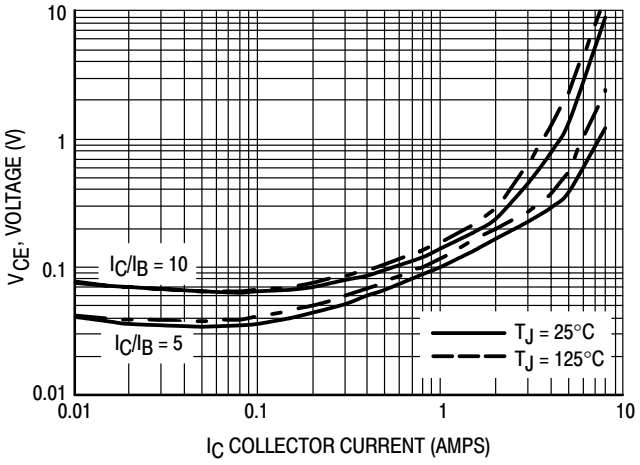


Figure 4. Collector−Emitter Saturation Voltage

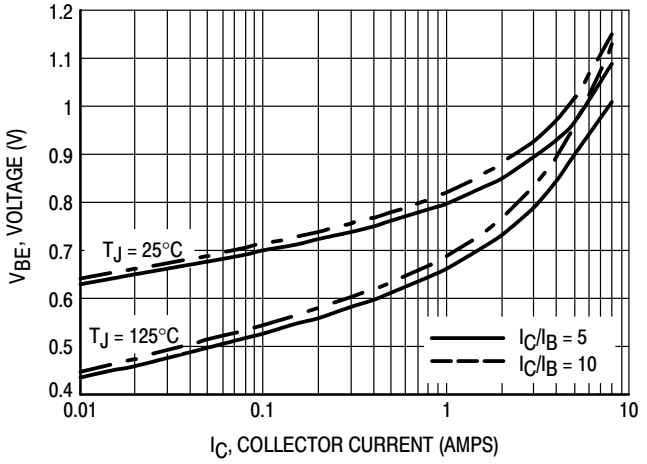


Figure 5. Base−Emitter Saturation Region

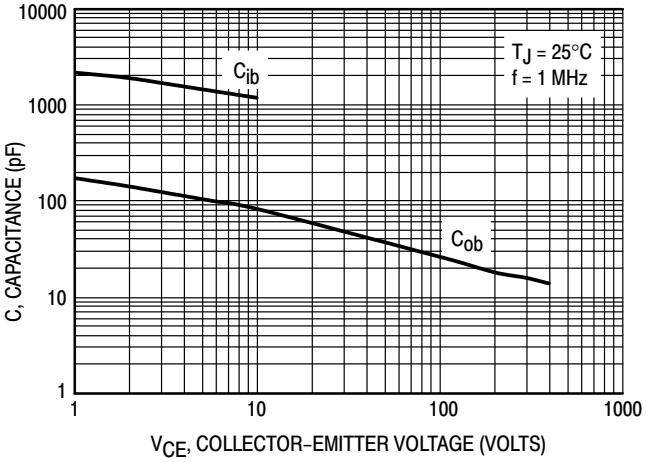


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

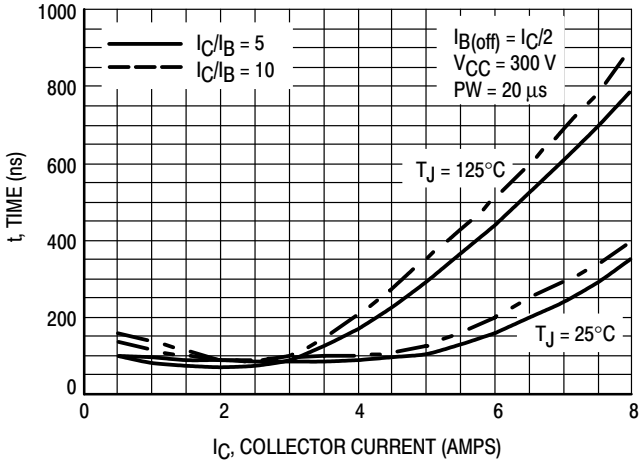


Figure 7. Resistive Switching, t_{on}

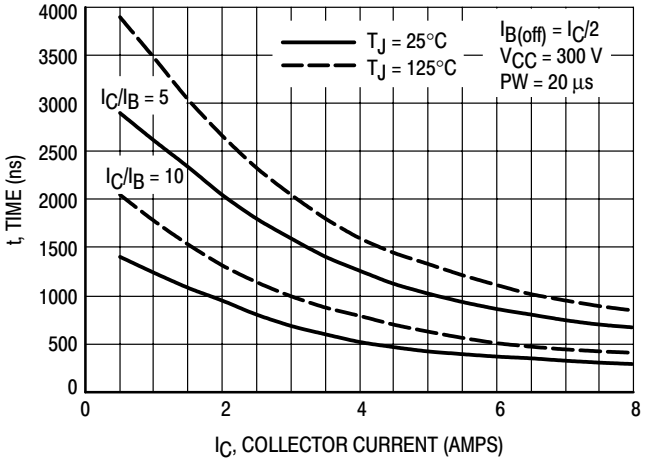


Figure 8. Resistive Switching, t_{off}

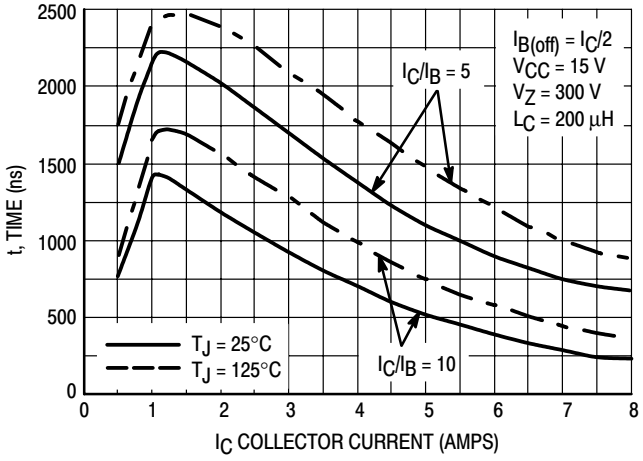


Figure 9. Inductive Storage Time, t_{si}

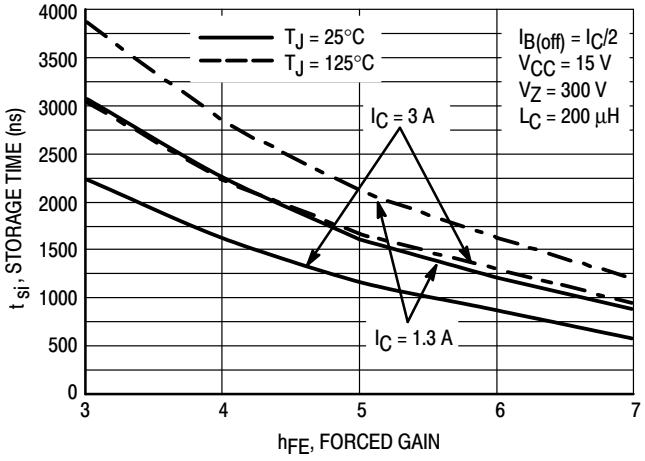


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

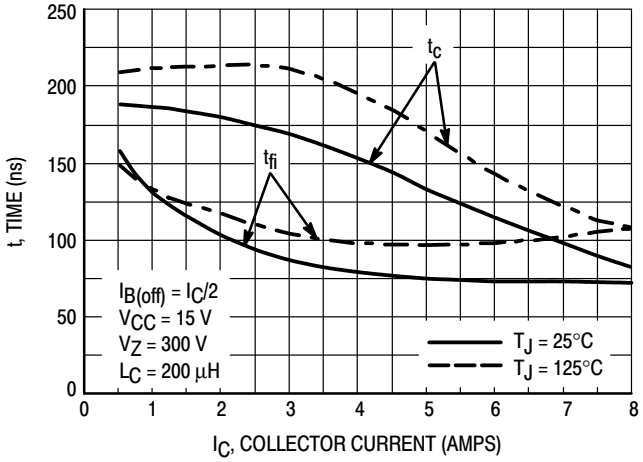


Figure 11. Inductive Switching, t_c and t_{fi}
$I_C/I_B = 5$

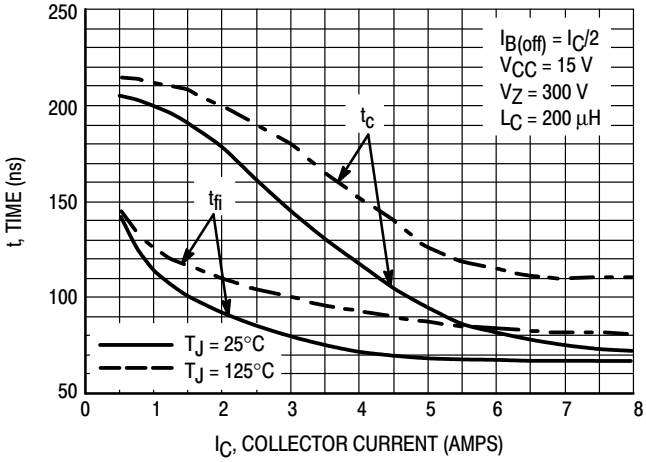


Figure 12. Inductive Switching, t_c and t_{fi}
$I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

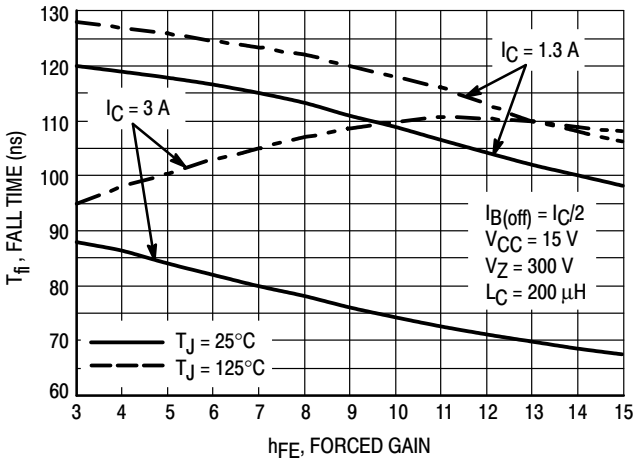


Figure 13. Inductive Fall Time

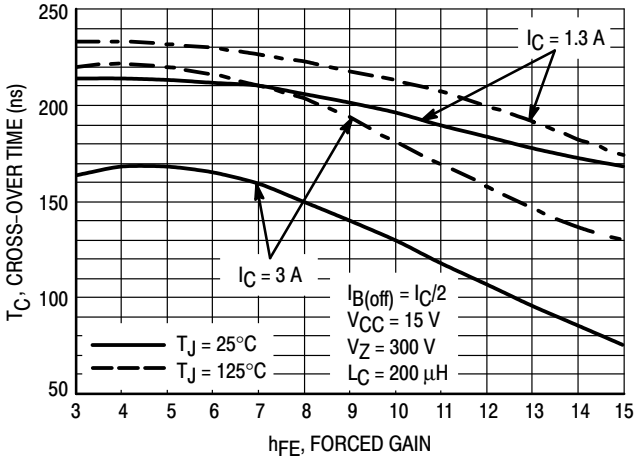


Figure 14. Inductive Cross−Over Time

GUARANTEED SAFE OPERATING AREA INFORMATION

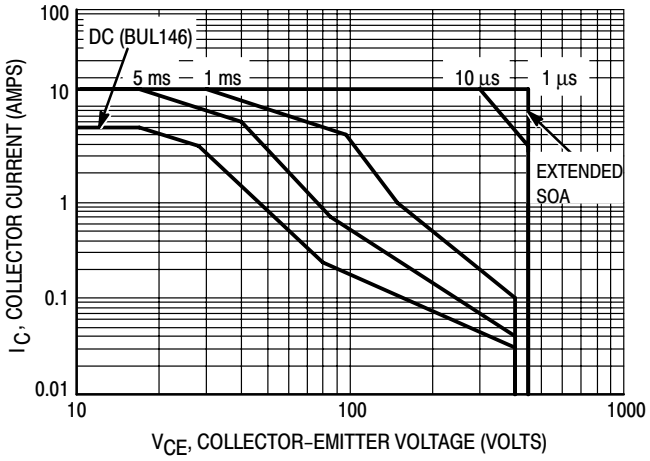


Figure 15. Forward Bias Safe Operating Area

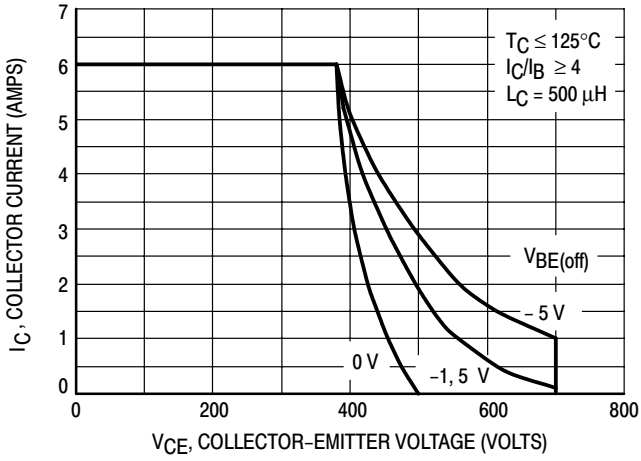


Figure 16. Reverse Bias Switching Safe Operating Area

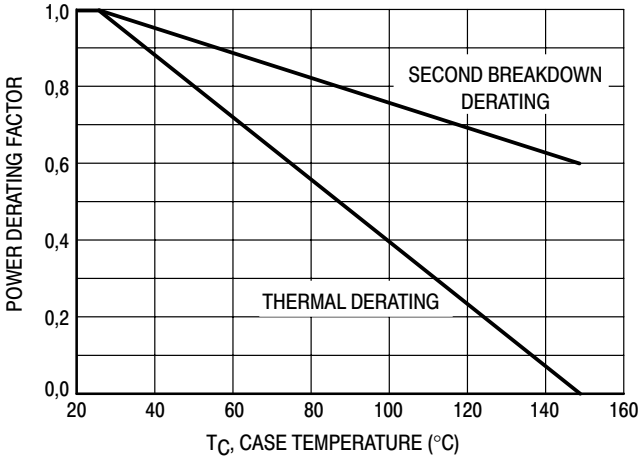


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

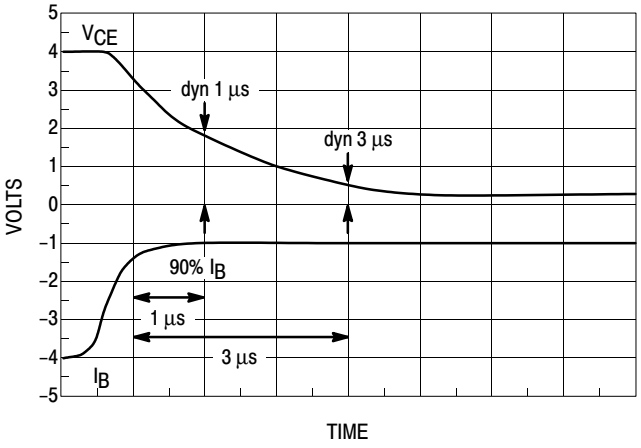


Figure 18. Dynamic Saturation Voltage Measurements

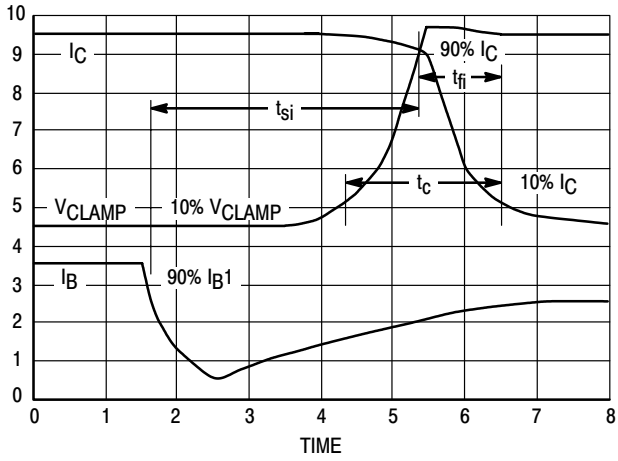
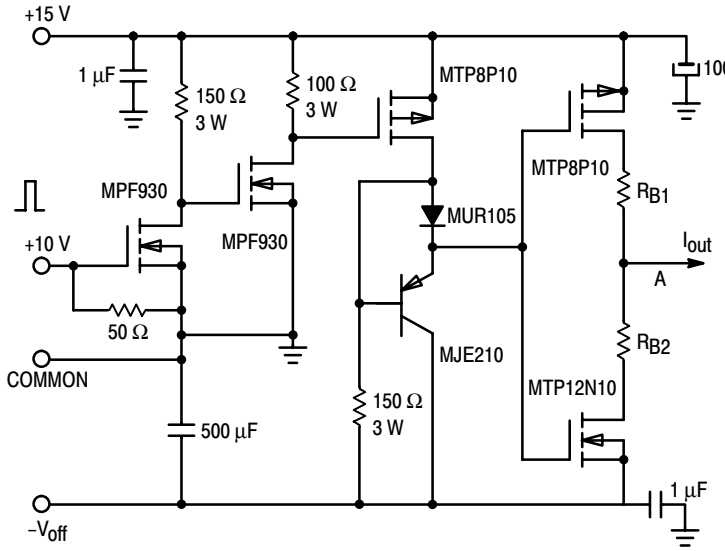
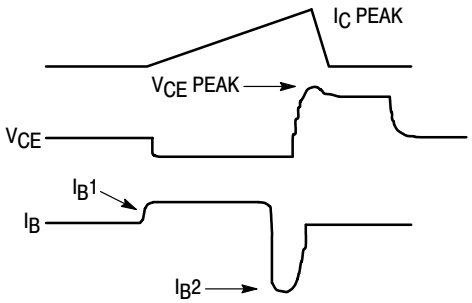


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

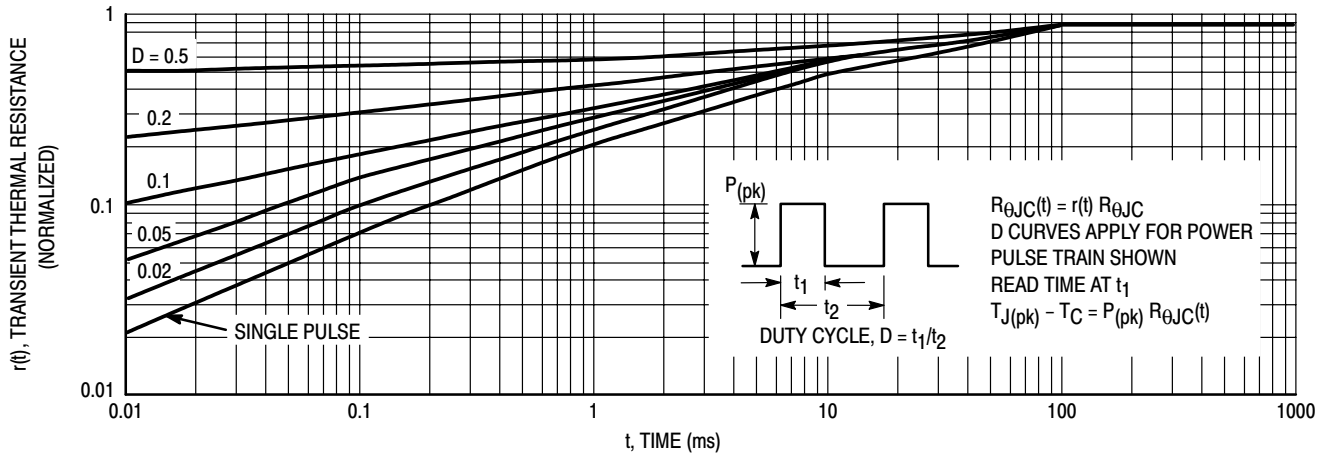


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL146

TYPICAL THERMAL RESPONSE

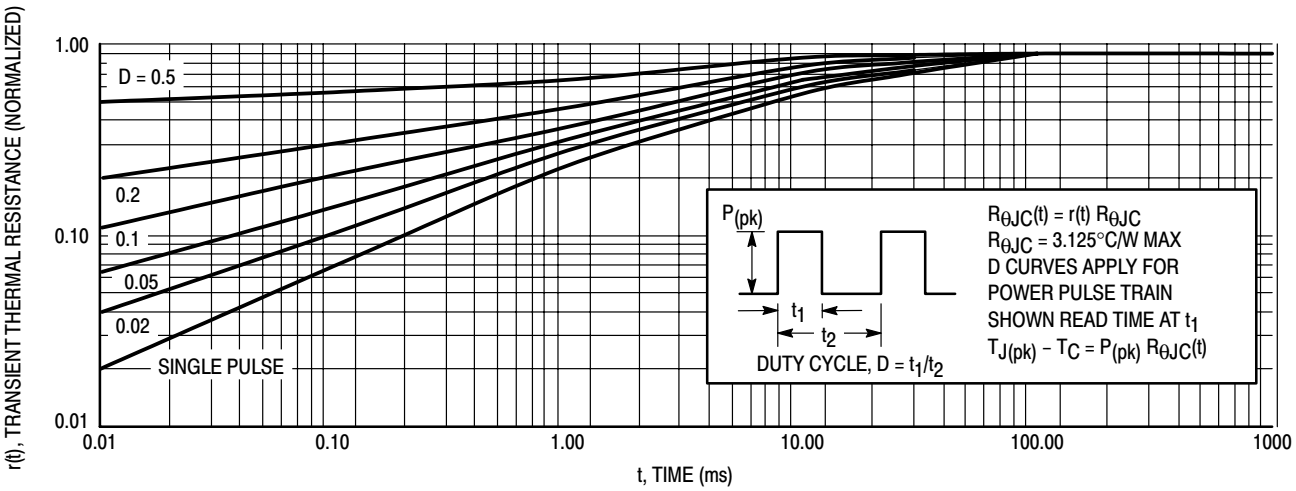


Figure 21. Typical Thermal Response for BUL146F

TEST CONDITIONS FOR ISOLATION TESTS*

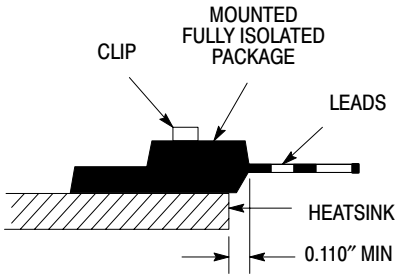


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

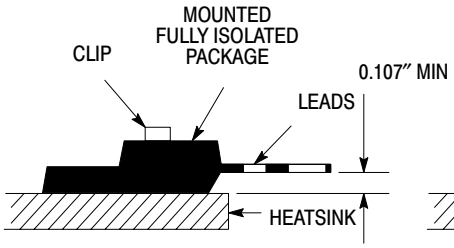


Figure 22b. Clip Mounting Position for Isolation Test Number 2

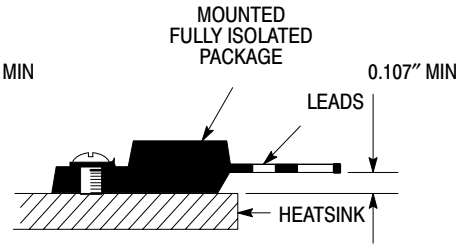


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

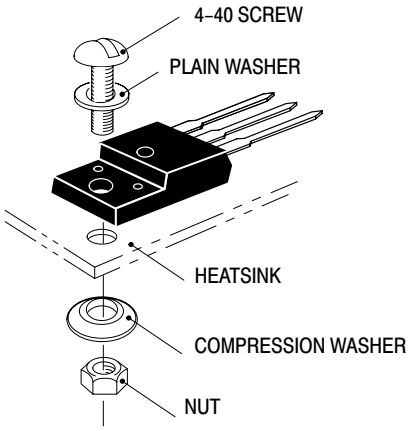


Figure 23a. Screw−Mounted

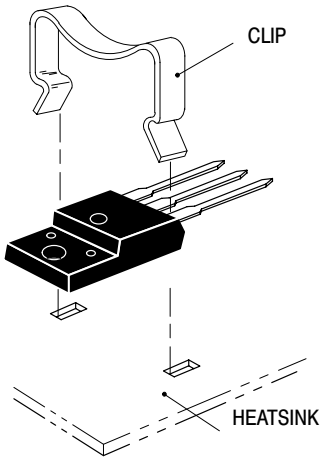


Figure 23b. Clip−Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

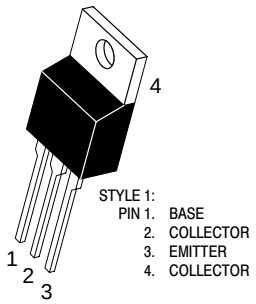
BUL147

SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
8.0 AMPERES
700 VOLTS
45 and 125 WATTS

The BUL147 have an applications specific state−of−the−art die designed for use in electric fluorescent lamp ballasts to 180 Watts and in Switchmode Power supplies for all types of electronic equipment. These high−voltage/high−speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Parametric Distributions are Tight and Consistent Lot−to−Lot
- Two Package Choices: Standard TO−220 or Isolated TO−220



BUL147
CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	BUL147	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	− 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS					
Base−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.92	1.25	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		—	0.25	0.5	
(T_C = 125°C)		—	0.3	0.5	
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.35	0.7	
(T_C = 125°C)		—	0.35	0.8	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	—	34	—
(T_C = 125°C)		—	30	—	
(I_C = 4.5 Adc, V_{CE} = 1.0 Vdc)		8.0	12	—	
(T_C = 125°C)		7.0	11	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (T_C = 25°C to 125°C)		10	18	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	—	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	100	175	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{ib}	—	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18) — (I_C = 2.0 Adc, I_{B1} = 200 mAdc, V_{CC} = 300 V) — 1.0 μs	$V_{CE(dsat)}$	—	3.0	—	Volts
(T_C = 125°C)		—	5.5	—	
3.0 μs		—	0.8	—	
(T_C = 125°C)		—	1.4	—	
(I_C = 5.0 Adc, I_{B1} = 0.9 Adc, V_{CC} = 300 V) — 1.0 μs		—	3.3	—	
(T_C = 125°C)		—	8.5	—	
3.0 μs		—	0.4	—	
(T_C = 125°C)		—	1.0	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn−On Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 1.0 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	200 190	350 —	ns
Turn−Off Time	(T_C = 125°C)	t_{off}	— —	1.0 1.6	2.5 —	μs
Turn−On Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B1} = 2.25 Adc, V_{CC} = 300 V) (T_C = 125°C)	t_{on}	— —	85 100	150 —	ns
Turn−Off Time	(T_C = 125°C)	t_{off}	— —	1.5 2.0	2.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 1.0 Adc) (T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.3 1.9	2.5 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	210 230	350 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B2} = 2.25 Adc) (T_C = 125°C)	t_{fi}	— —	80 100	150 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.6 2.1	3.2 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	170 200	300 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B2} = 0.9 Adc) (T_C = 125°C)	t_{fi}	60 —	— 150	180 —	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 —	— 4.3	3.8 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	200 330	350 —	ns

TYPICAL STATIC CHARACTERISTICS

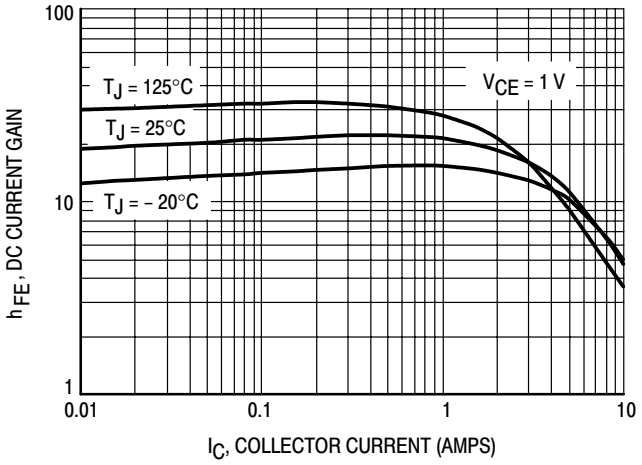


Figure 1. DC Current Gain @ 1 Volt

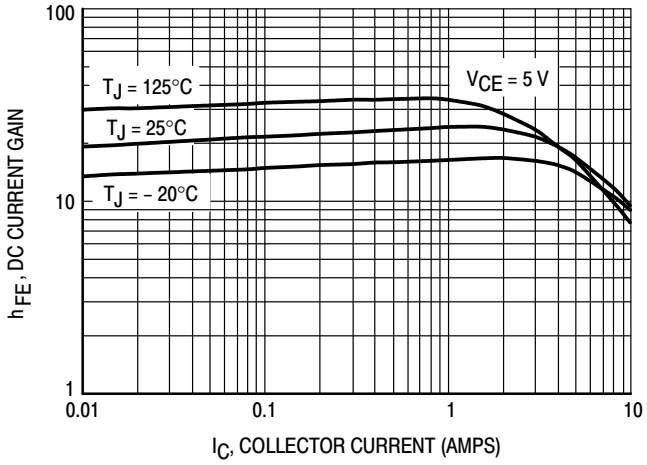


Figure 2. DC Current Gain @ 5 Volts

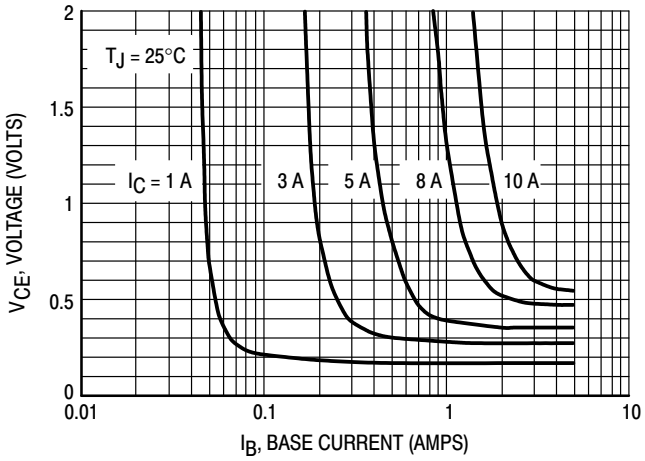


Figure 3. Collector Saturation Region

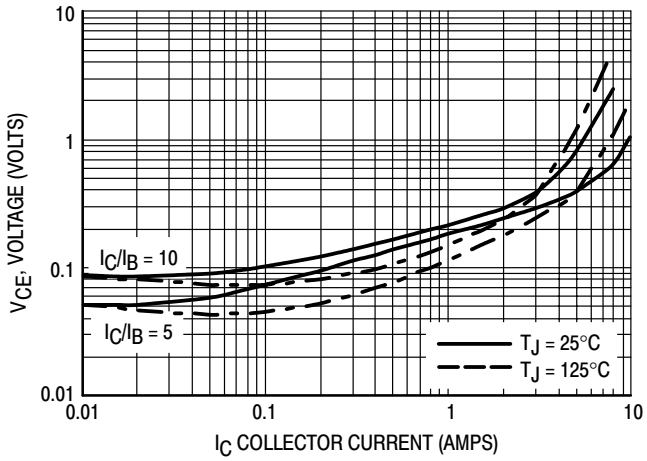


Figure 4. Collector−Emitter Saturation Voltage

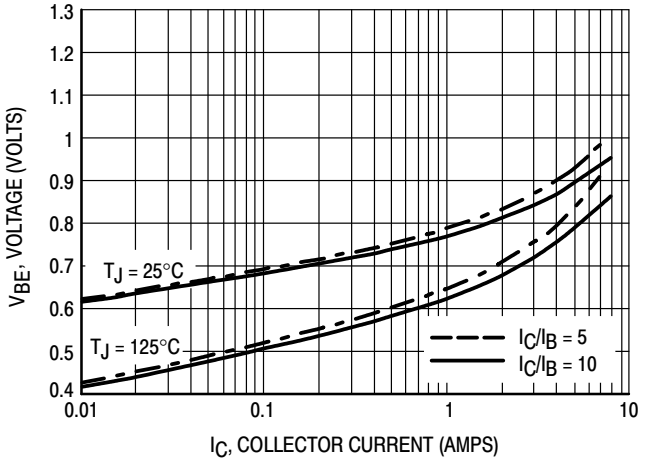


Figure 5. Base−Emitter Saturation Region

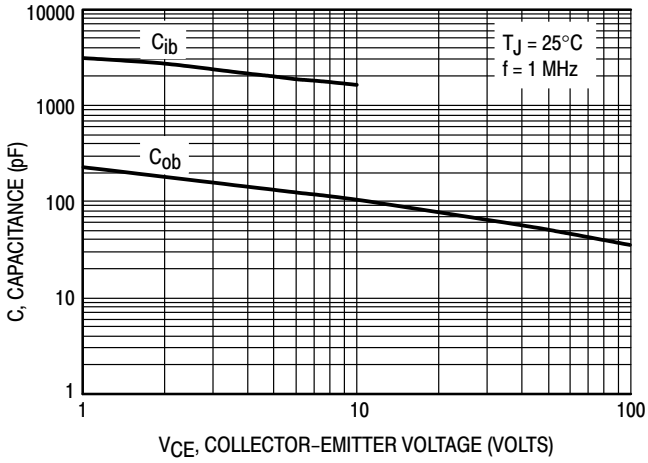


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

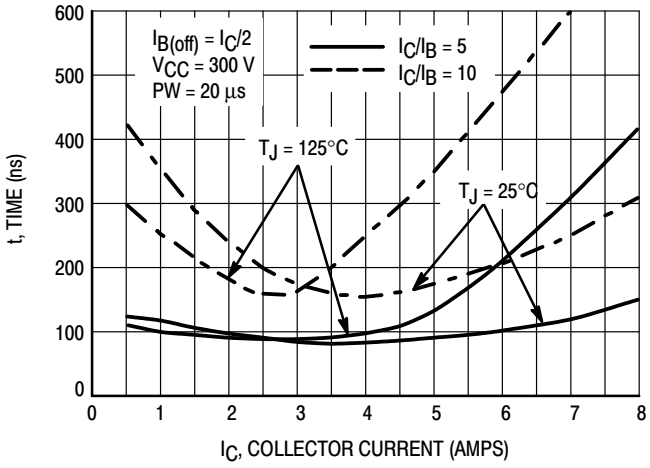


Figure 7. Resistive Switching, t_{on}

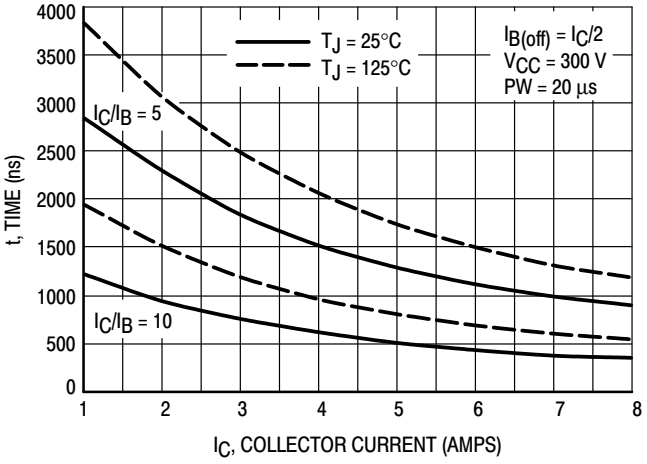


Figure 8. Resistive Switching, t_{off}

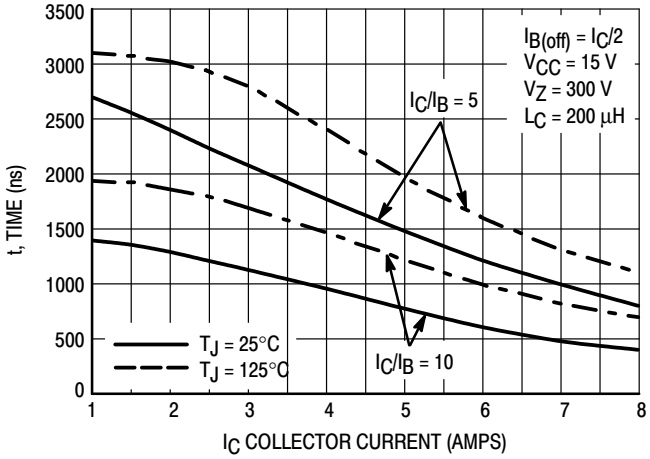


Figure 9. Inductive Storage Time, t_{si}

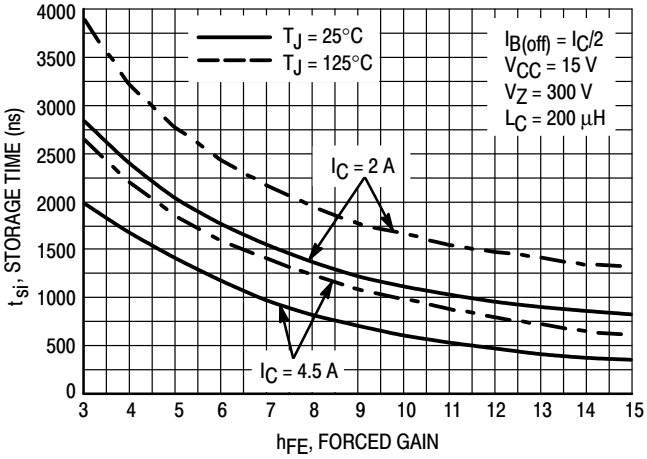


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

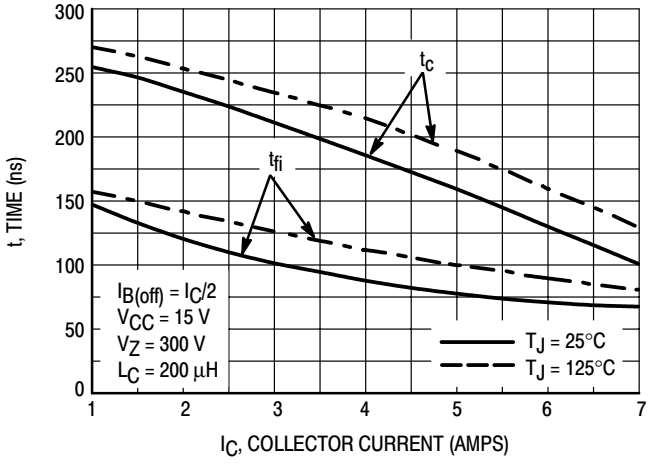


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

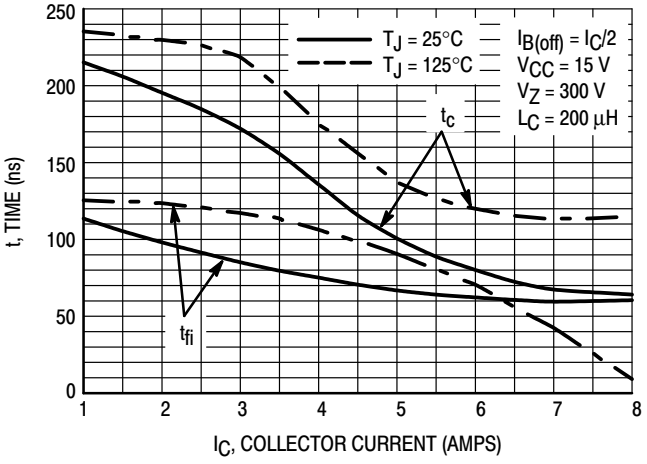


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

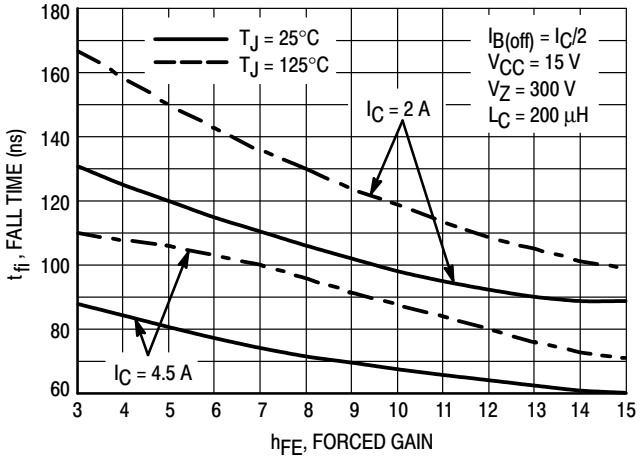


Figure 13. Inductive Fall Time

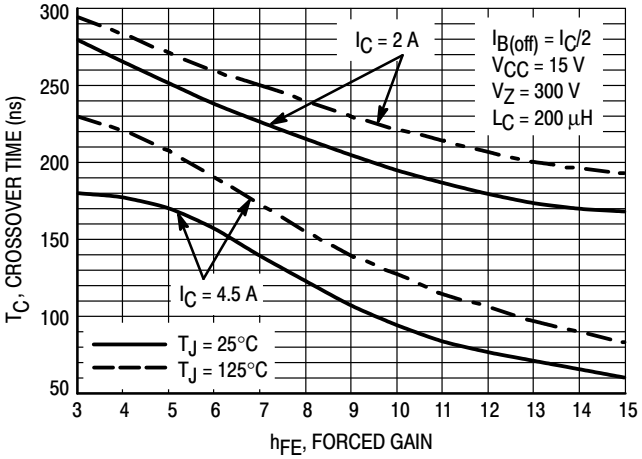


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

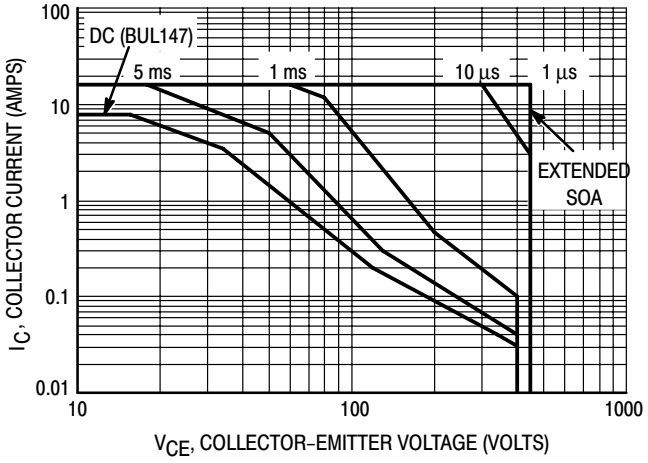


Figure 15. Forward Bias Safe Operating Area

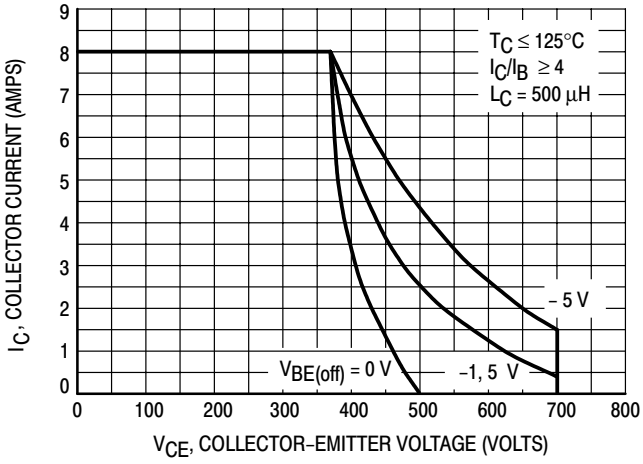


Figure 16. Reverse Bias Switching Safe Operating Area

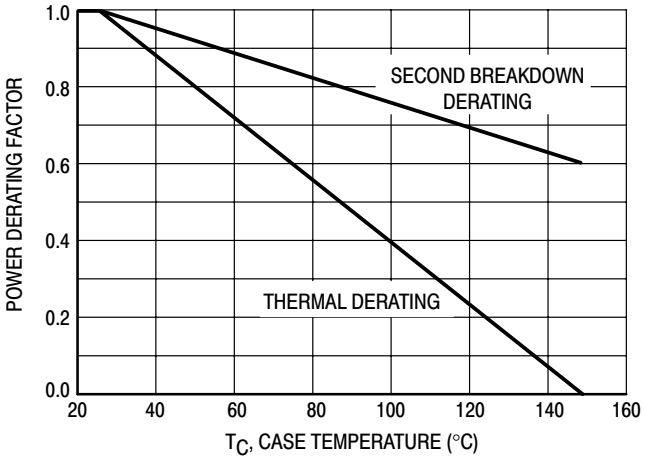


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

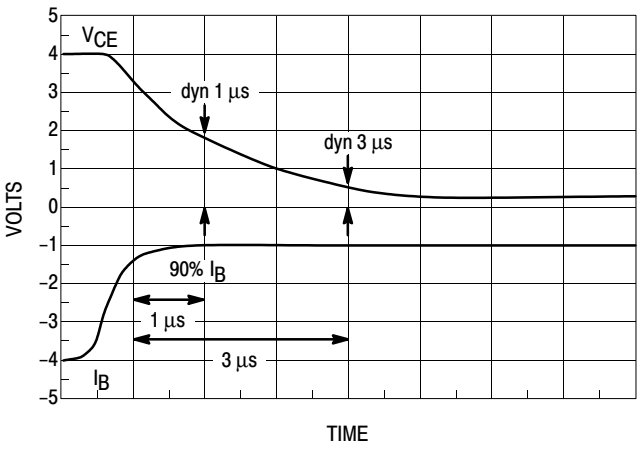


Figure 18. Dynamic Saturation Voltage Measurements

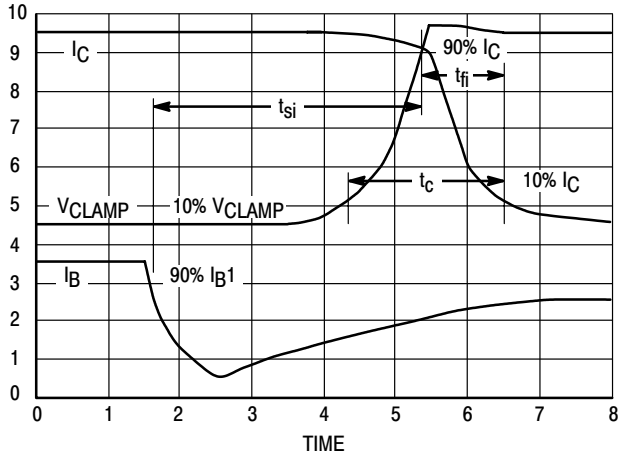
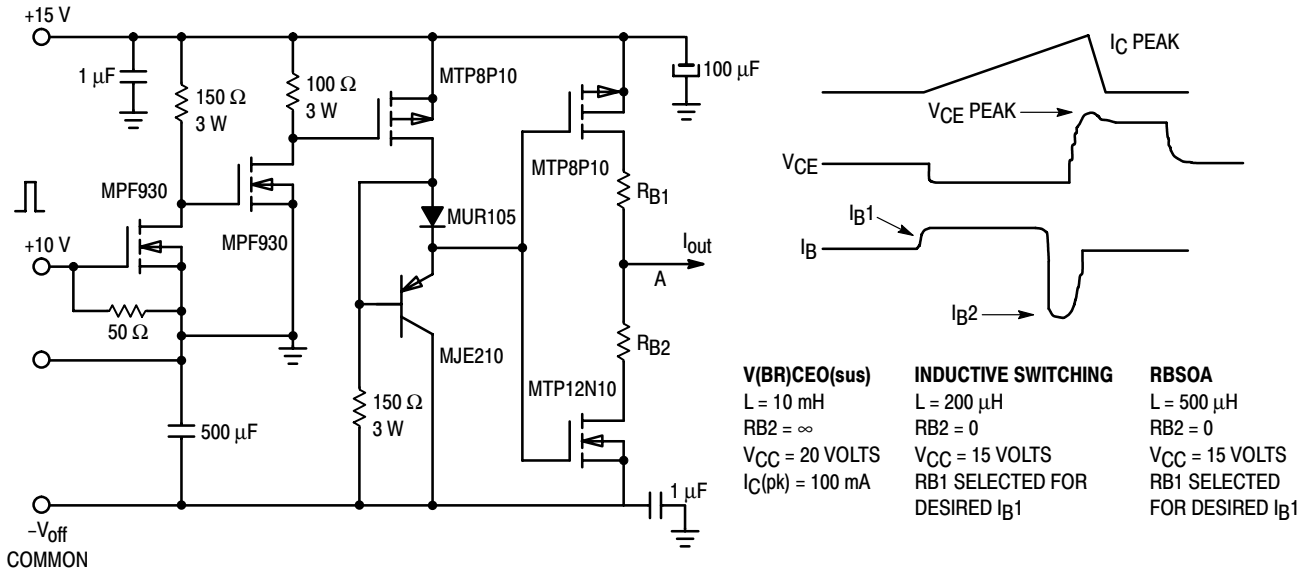


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

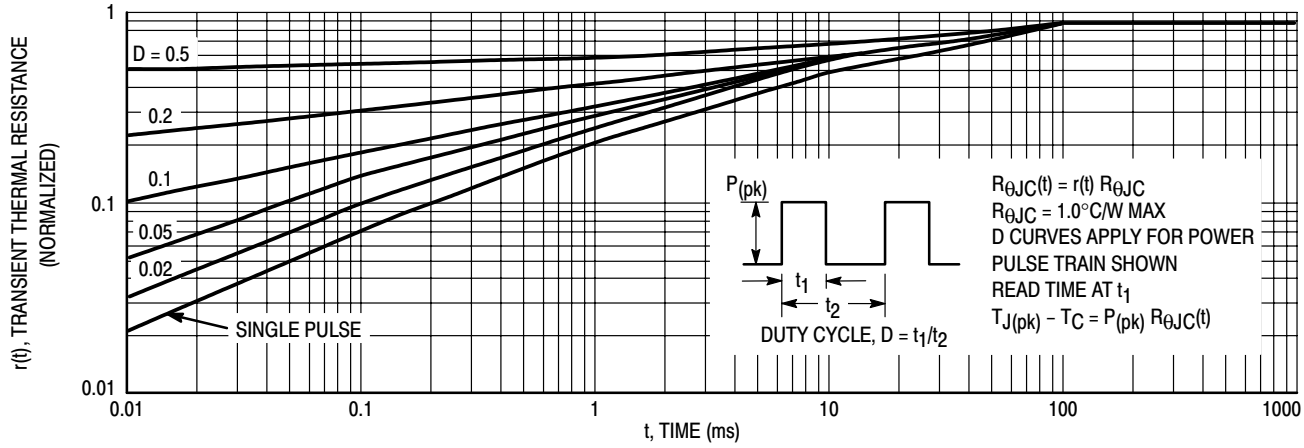


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL147

BUL42D

High Speed, High Gain Bipolar NPN Transistor Integrating an Antisaturation Network and a Transient Voltage Suppression Capability

The BUL42D is a state−of−the−art bipolar transistor. Tight dynamic characteristics and lot to lot minimum spread make it ideally suitable for light ballast applications.

Main Features:

- Free Wheeling Diode Built In
- Flat DC Current Gain
- Fast Switching Times and Tight Distribution
- “Six Sigma” Process Providing Tight and Reproducible Parameter Spreads

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	4.0 8.0	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	1.0 2.0	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to +150	°C

TYPICAL GAIN

Typical Gain @ I_C = 1 A, V_{CE} = 2 V Typical Gain @ I_C = 0.3 A, V_{CE} = 1 V	h_{FE} h_{FE}	13 16	− −

THERMAL CHARACTERISTICS

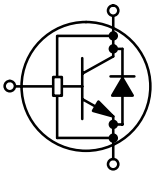
Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Case	$R_{\theta JC}$	1.66	°C/W
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 seconds	T_L	260	°C

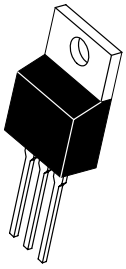
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%

ON Semiconductor®

http://onsemi.com

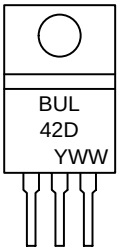
4 AMPERES
700 VOLTS
75 WATTS
POWER TRANSISTOR





TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BUL42D	TO−220	50 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	430	−	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	780	−	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	9.0	12	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}	− −	− −	100 200	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}	− −	− −	10 200	μAdc
Emitter−Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	−	−	100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	−	0.85	1.2	Vdc
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	−	0.2	1.0	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 2 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)		h_{FE}	8.0 10	13 12	− −	−
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1.0 Adc)		V_{EC}	−	0.9	1.5	V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)						
Turn−Off Time (I_C = 1.2 Adc, I_{B1} = 0.4 A, I_{B2} = 0.1 A, V_{CC} = 300 V)		T_{off}	4.6	−	6.55	μs
Fall Time (I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 A, V_{CC} = 150 V, V_{BE} = −2 V)		T_f	−	−	0.8	μs
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 400 mA, I_{B1} = 40 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	− −	2.8 3.2	− −	V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		− −	0.75 1.3	− −	
	I_C = 1 A, I_{B1} = 200 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		− −	2.1 4.7	− −	
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		− −	0.35 0.6	− −	

TYPICAL STATIC CHARACTERISTICS

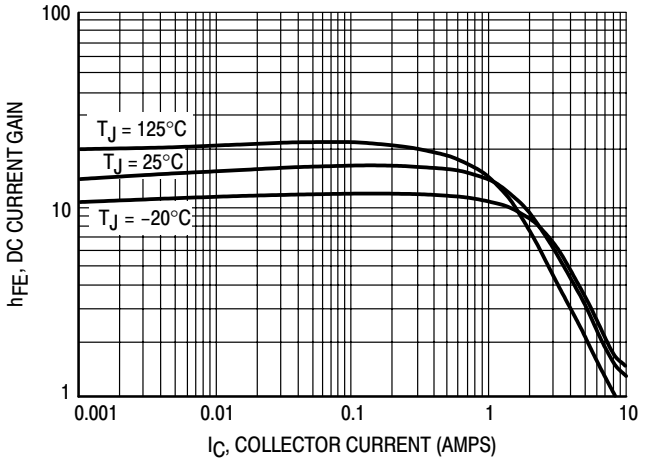


Figure 1. DC Current Gain @ V_{CE} = 1 V

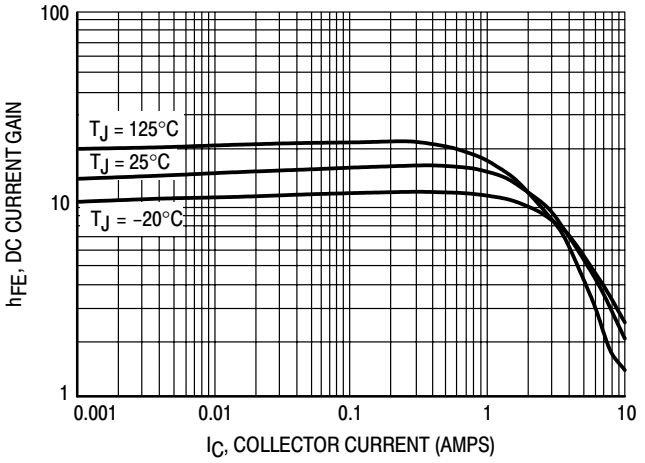


Figure 2. DC Current Gain @ V_{CE} = 5 V

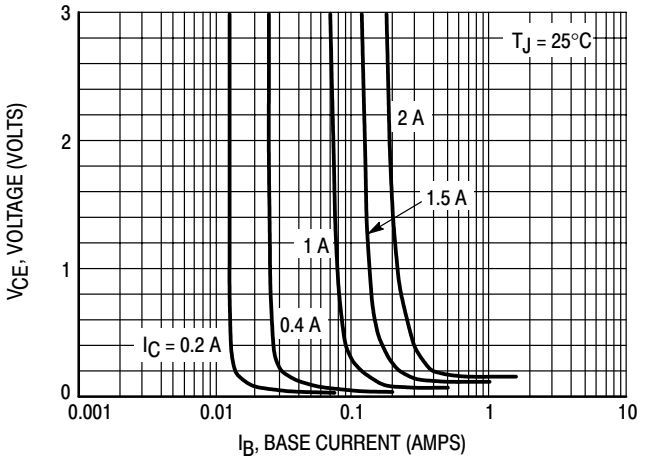


Figure 3. Collector Saturation Region

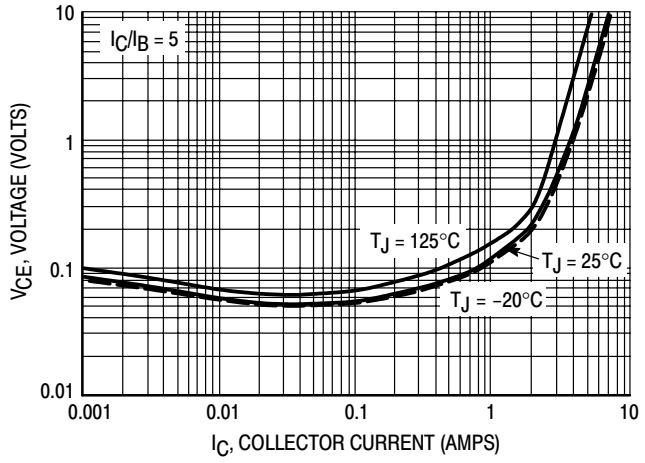


Figure 4. Collector−Emitter Saturation Voltage

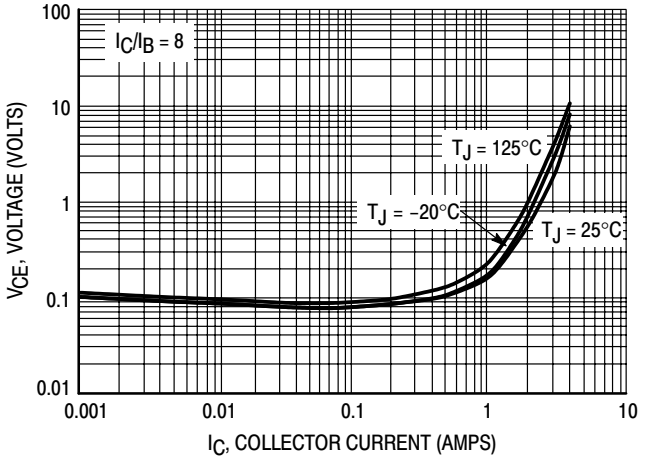


Figure 5. Collector−Emitter Saturation Voltage

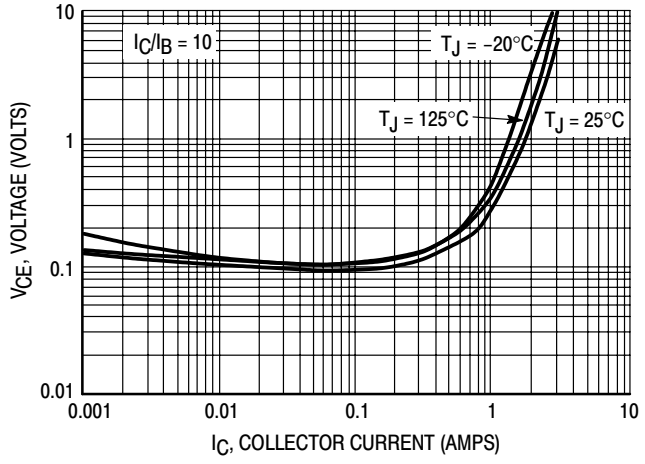


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

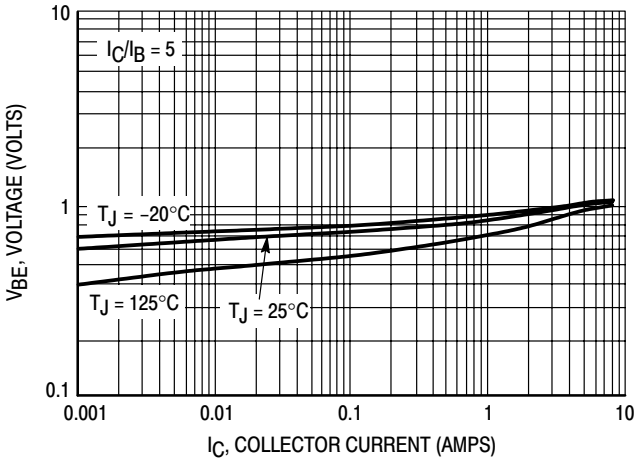


Figure 7. Base−Emitter Saturation Region

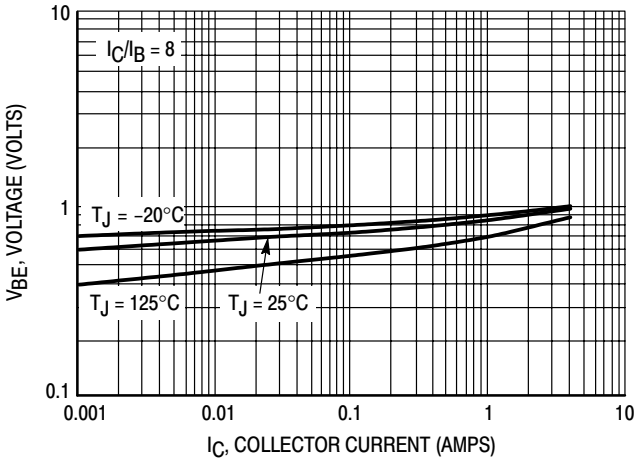


Figure 8. Base−Emitter Saturation Region

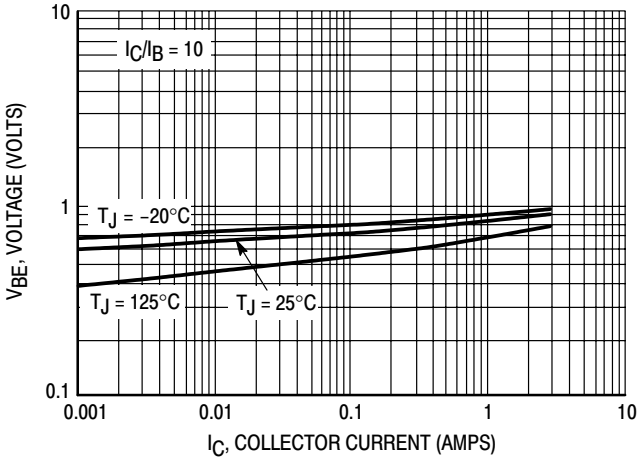


Figure 9. Base−Emitter Saturation Region

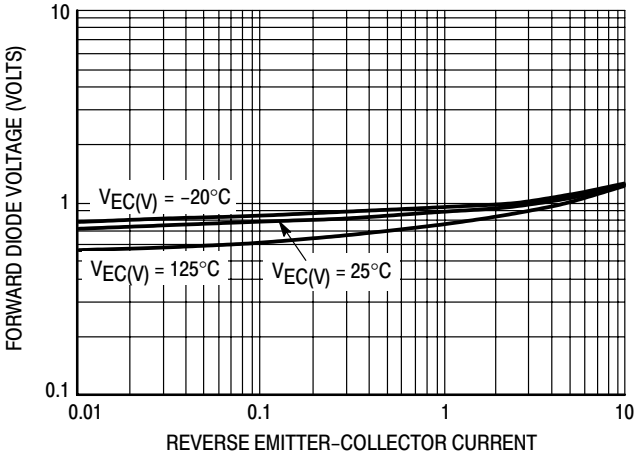


Figure 10. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

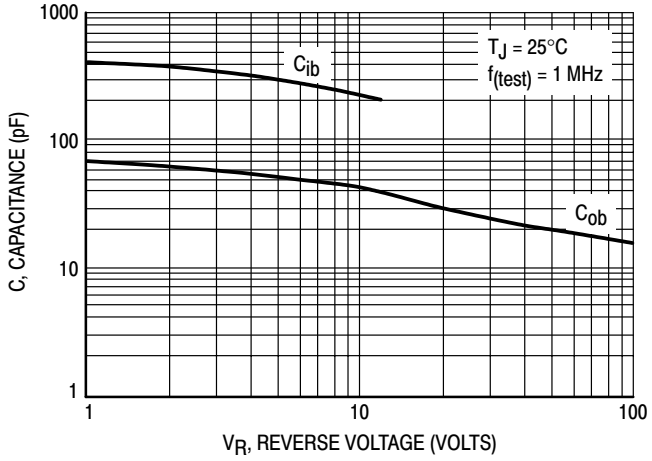


Figure 11. Capacitance

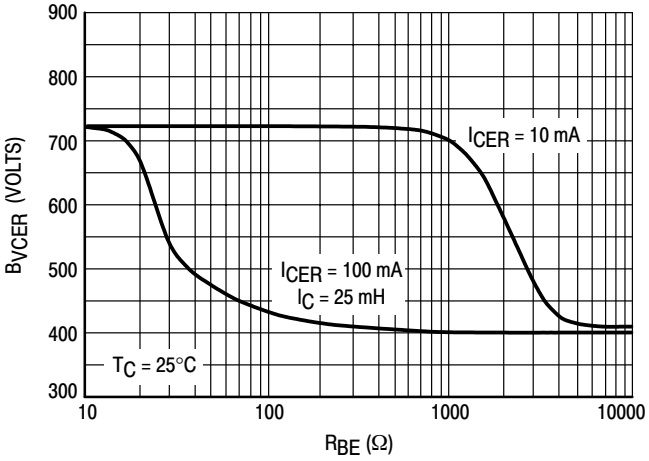


Figure 12. $B_{VCER} = f(R_{BE})$

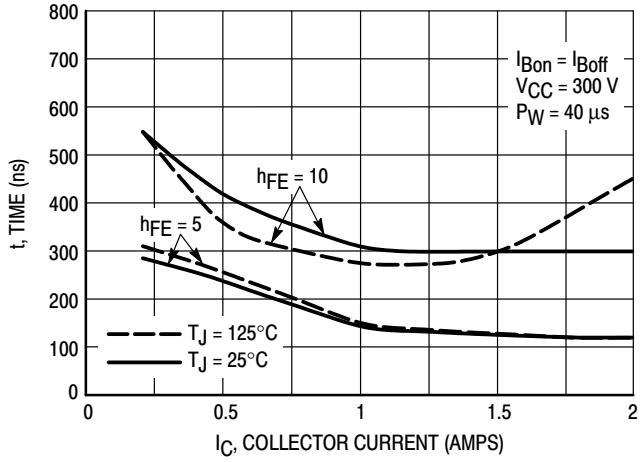


Figure 13. Resistive Switching, t_{on}

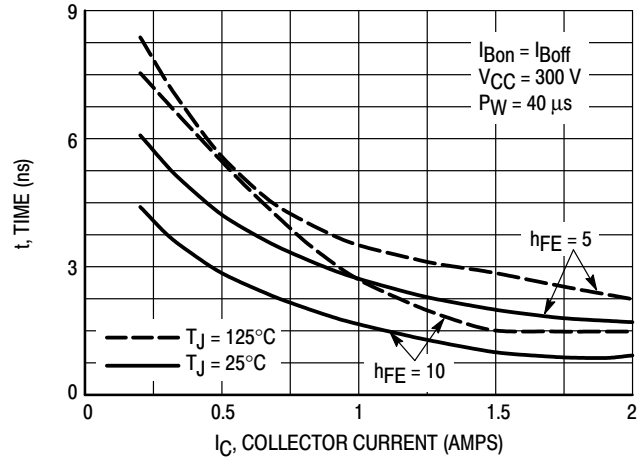


Figure 14. Resistive Switching, t_{off}

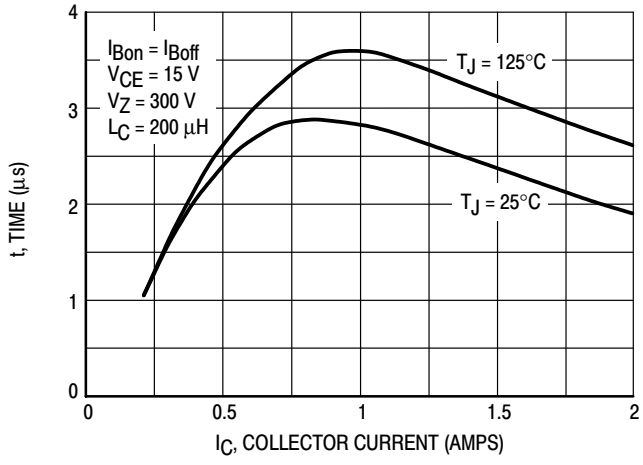


Figure 15. Inductive Storage Time, t_{si} @ h_{FE} = 5

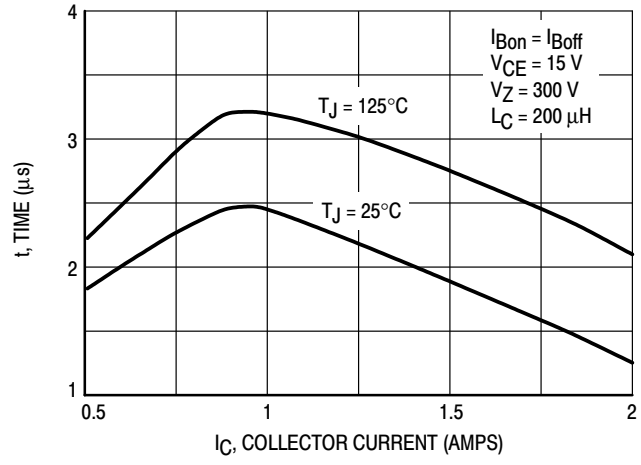


Figure 16. Inductive Storage Time, t_{si} @ h_{FE} = 10

TYPICAL SWITCHING CHARACTERISTICS

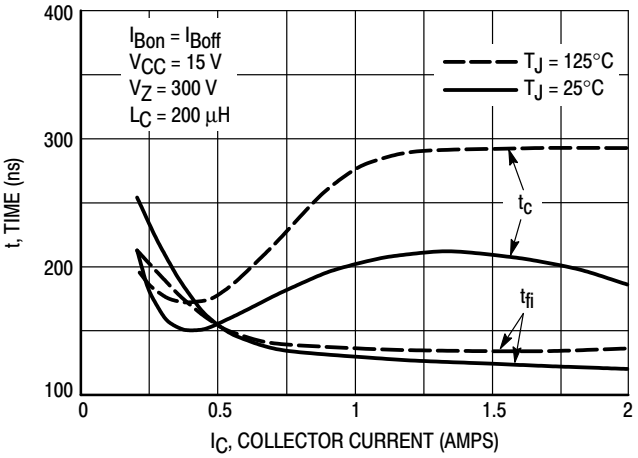


Figure 17. Inductive Fall and Cross Over Time, t_{fi} and t_c @ h_{FE} = 5

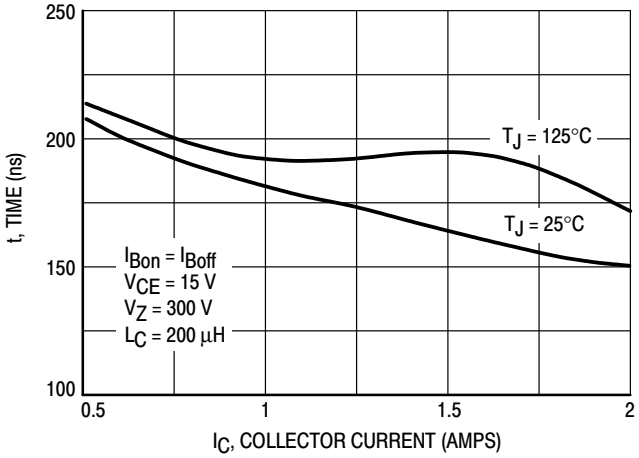


Figure 18. Inductive Fall Time, t_{fi} @ h_{FE} = 10

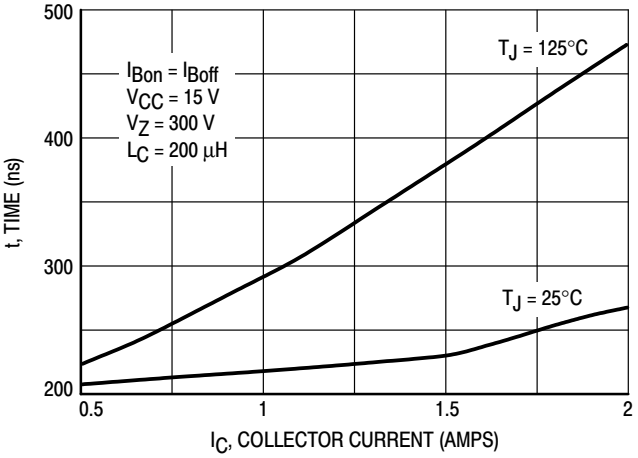


Figure 19. Inductive Cross Over Time, t_c @ h_{FE} = 10

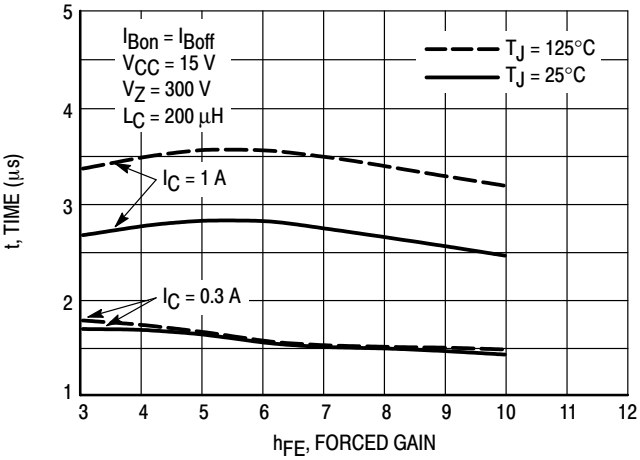


Figure 20. Inductive Storage Time, t_{si}

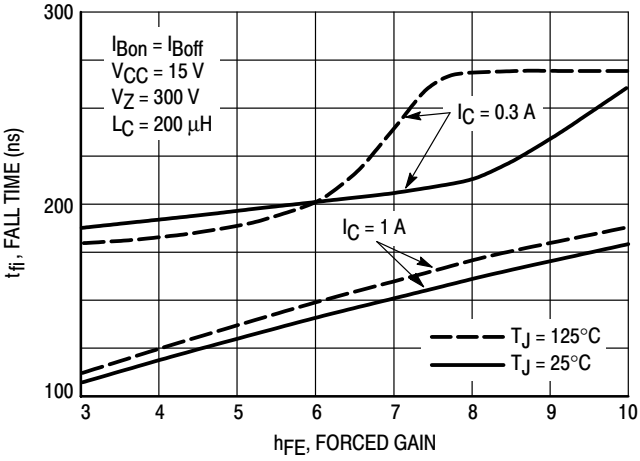


Figure 21. Inductive Fall Time, t_f

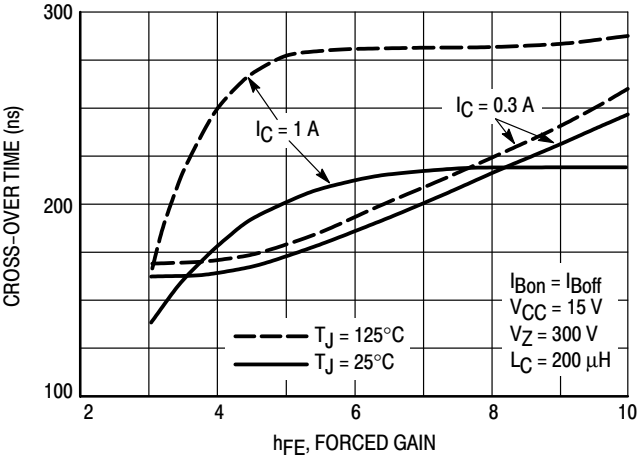


Figure 22. Inductive Cross Over Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

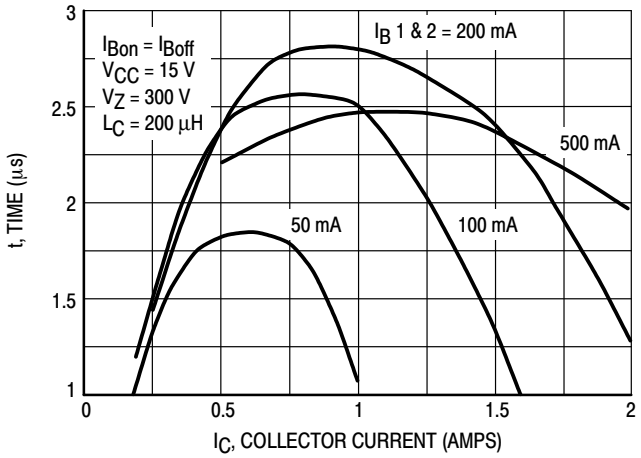


Figure 23. Inductive Storage Time, t_{si}

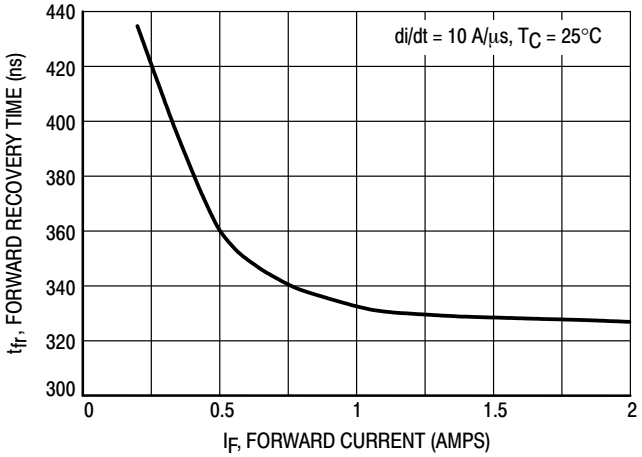


Figure 24. Forward Recovery Time, t_{fr}

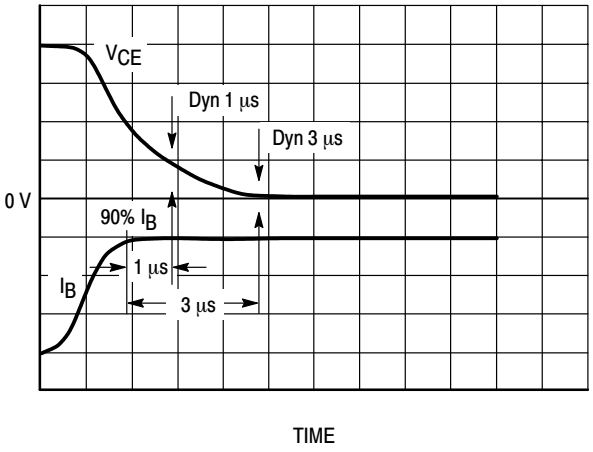


Figure 25. Dynamic Saturation Voltage Measurements

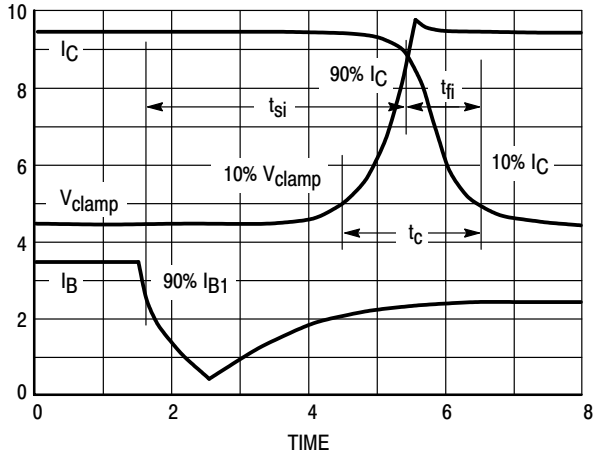
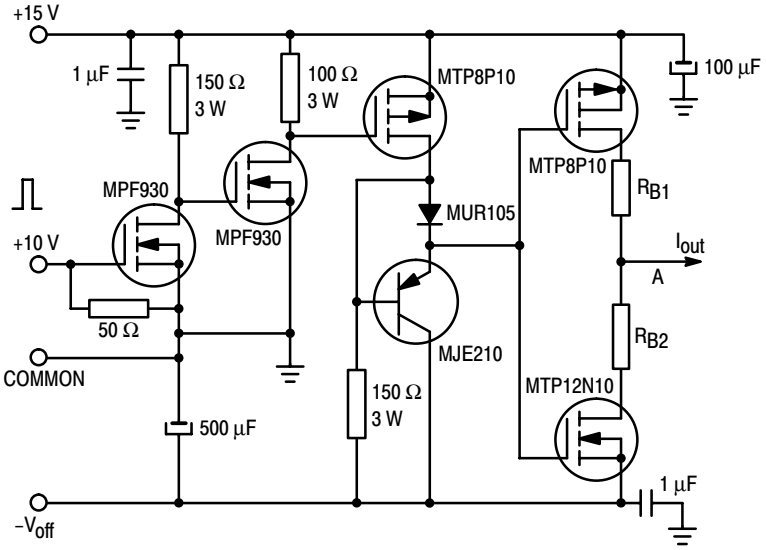
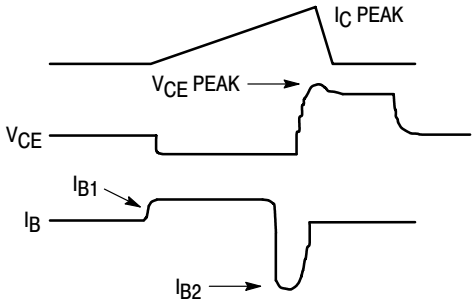


Figure 26. Inductive Switching Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

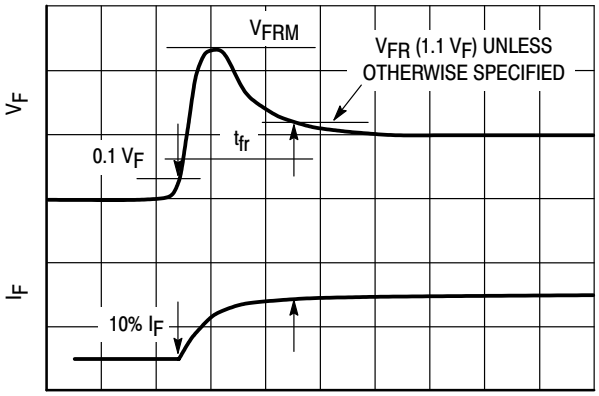


Figure 27. t_{fr} Measurement

MAXIMUM RATINGS

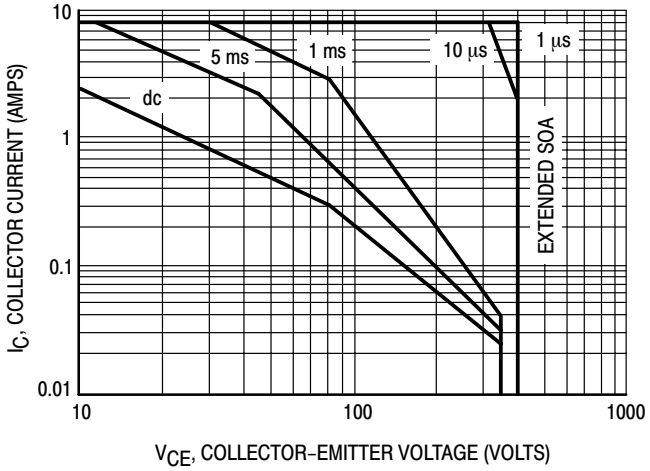


Figure 28. Forward Bias Safe Operating Area

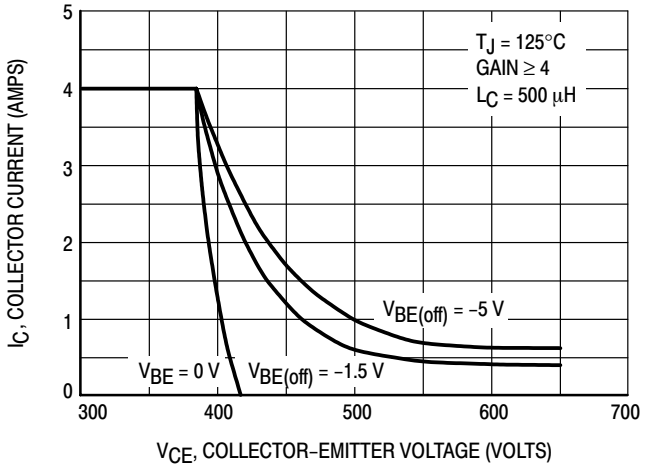


Figure 29. Reverse Bias Safe Operating Area

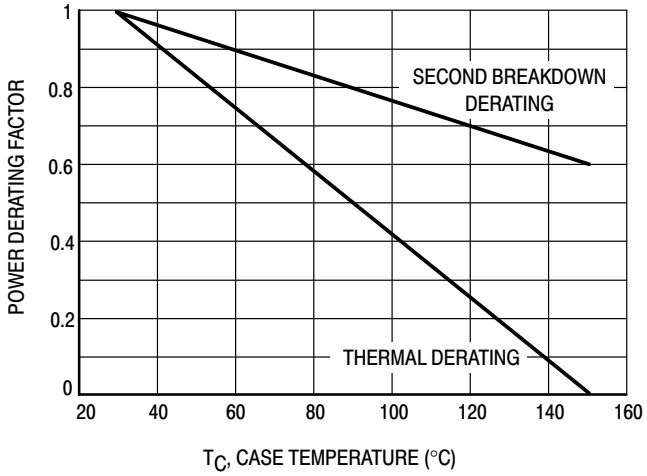


Figure 30. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on $T_C = 25°C$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second Breakdown limitations do not derate like thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{j(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

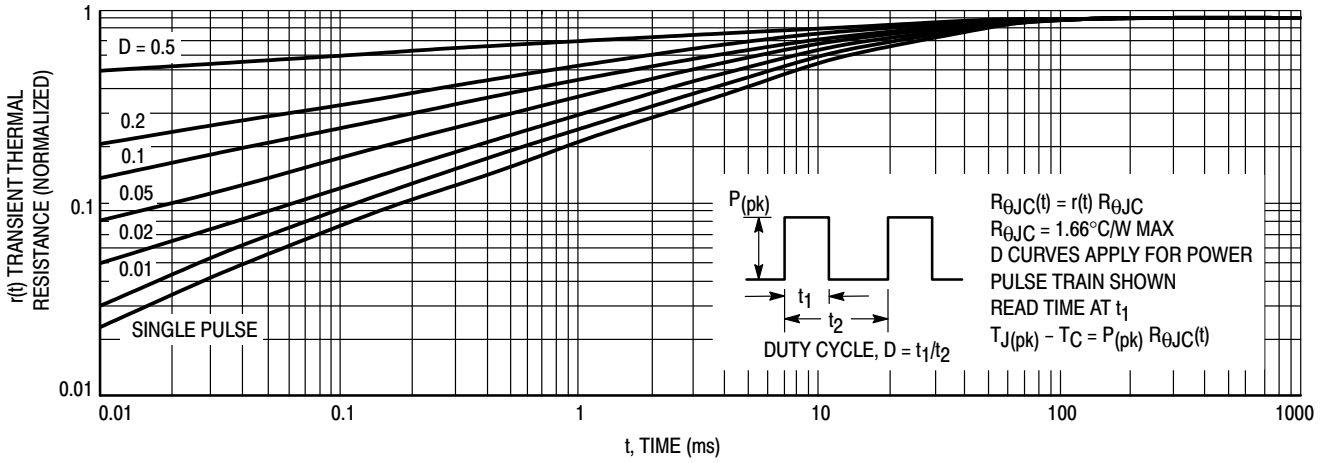


Figure 31. Thermal Response

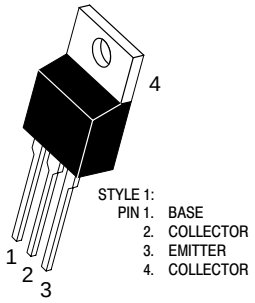
BUL44

SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
2.0 AMPERES
700 VOLTS
40 and 100 WATTS

The BUL44 have an applications specific state−of−the−art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Full Characterization at 125°C
- Tight Parametric Distributions are Consistent Lot−to−Lot



BUL44
CASE 221A−06
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	2.0 5.0	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	1.0 2.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	− 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS					
Base−Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	—	0.85	1.1	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)		—	0.92	1.25	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)		—	0.20	0.5	
(T_C = 125°C)		—	0.20	0.5	
(I_C = 1.0 Adc, I_B = 0.2 Adc)		—	0.25	0.6	
(T_C = 125°C)		—	0.25	0.6	
DC Current Gain	h_{FE}				—
(I_C = 0.2 Adc, V_{CE} = 5.0 Vdc)		14	—	34	
(T_C = 125°C)		—	32	—	
(I_C = 0.4 Adc, V_{CE} = 1.0 Vdc)		12	20	—	
(T_C = 125°C)		12	20	—	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		8.0	14	—	
(T_C = 125°C)		7.0	13	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	22	—	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{OB}	—	38	60	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{IB}	—	380	600	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} — (I_C = 0.4 Adc, I_{B1} = 40 mAdc, V_{CC} = 300 V) — 1.0 μs	$V_{CE(dsat)}$	—	2.5	—	Vdc
(T_C = 125°C)		—	2.7	—	
3.0 μs		—	1.3	—	
(T_C = 125°C)		—	1.15	—	
(I_C = 1.0 Adc, I_{B1} = 0.2 Adc, V_{CC} = 300 V) — 1.0 μs		—	3.2	—	
(T_C = 125°C)		—	7.5	—	
3.0 μs		—	1.25	—	
(T_C = 125°C)		—	1.6	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(continued)

SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)

Turn−On Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc, V_{CC} = 300 V)	(T_C = 125°C)	t_{on}	— —	40 40	100 —	ns
Turn−Off Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc, V_{CC} = 300 V)	(T_C = 125°C)	t_{off}	— —	1.5 2.0	2.5 —	μs
Turn−On Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B1} = 0.5 Adc, V_{CC} = 300 V)	(T_C = 125°C)	t_{on}	— —	85 85	150 —	ns
Turn−Off Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc, V_{CC} = 300 V)	(T_C = 125°C)	t_{off}	— —	1.75 2.10	2.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)

Fall Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc)	(T_C = 125°C)	t_{fi}	— —	125 120	200 —	ns
Storage Time		(T_C = 125°C)	t_{si}	— —	0.7 0.8	1.25 —	μs
Crossover Time		(T_C = 125°C)	t_c	— —	110 110	200 —	ns
Fall Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc)	(T_C = 125°C)	t_{fi}	— —	110 120	175 —	ns
Storage Time		(T_C = 125°C)	t_{si}	— —	1.7 2.25	2.75 —	μs
Crossover Time		(T_C = 125°C)	t_c	— —	180 210	300 —	ns
Fall Time	(I_C = 0.8 Adc, I_{B1} = 160 mAdc I_{B2} = 160 mAdc)	(T_C = 125°C)	t_{fi}	70 —	— 180	170 —	ns
Storage Time		(T_C = 125°C)	t_{si}	2.6 —	— 4.2	3.8 —	μs
Crossover Time		(T_C = 125°C)	t_c	— —	190 350	300 —	ns

TYPICAL STATIC CHARACTERISTICS

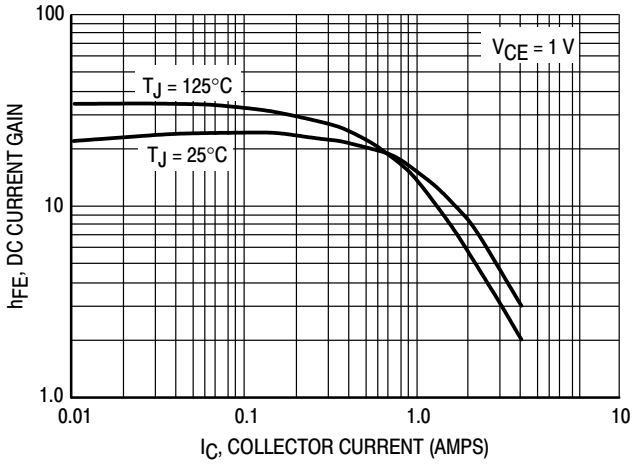


Figure 32. DC Current Gain at 1 Volt

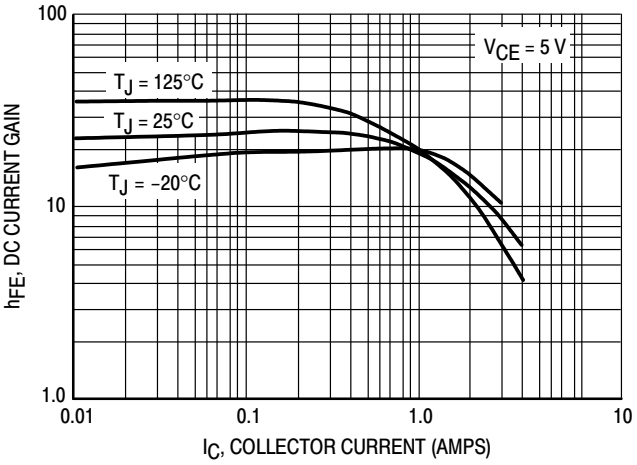


Figure 33. DC Current Gain at 5 Volts

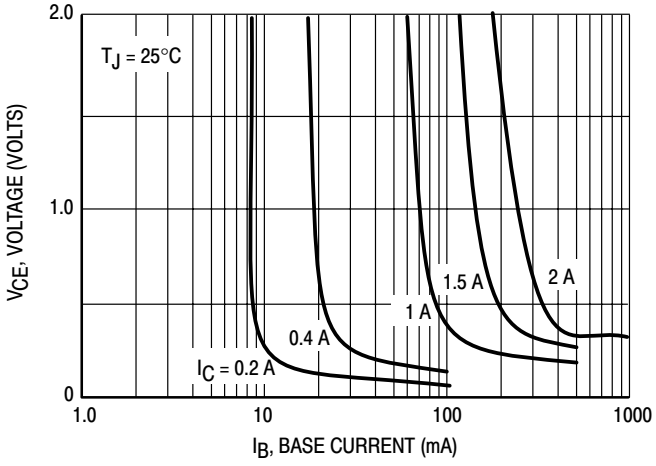


Figure 34. Collector Saturation Region

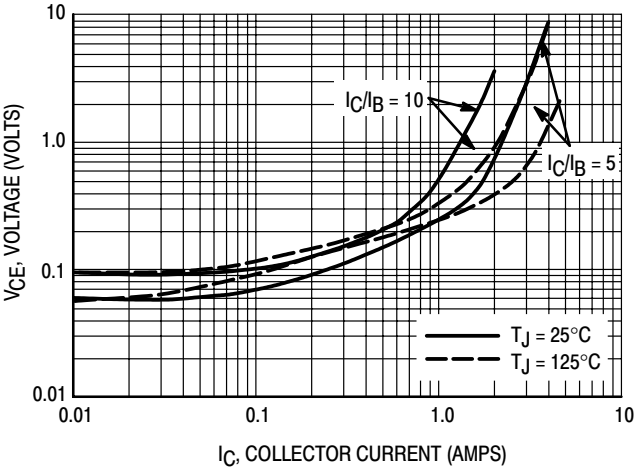


Figure 35. Collector−Emitter Saturation Voltage

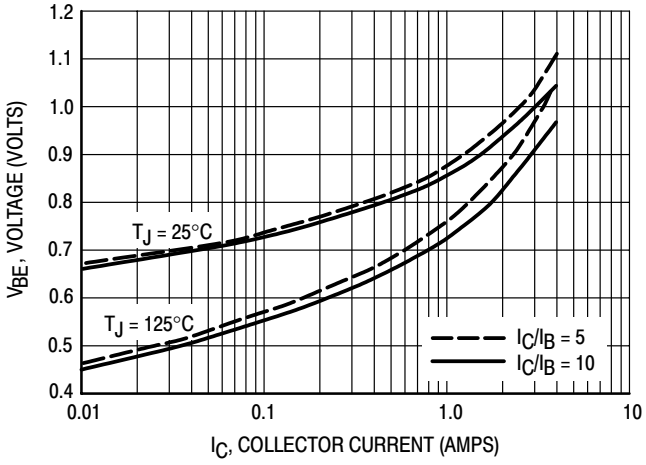


Figure 36. Base−Emitter Saturation Region

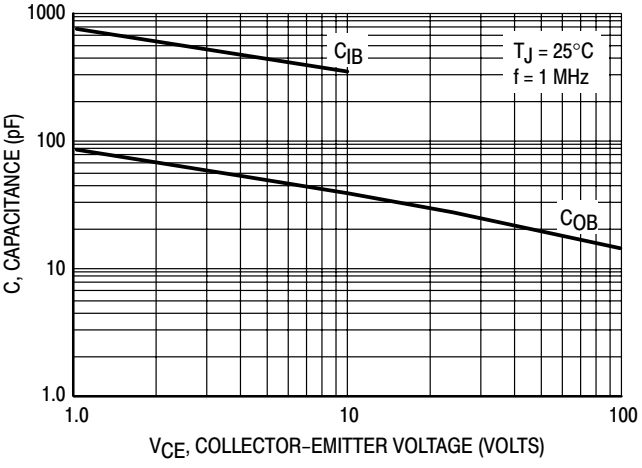


Figure 37. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

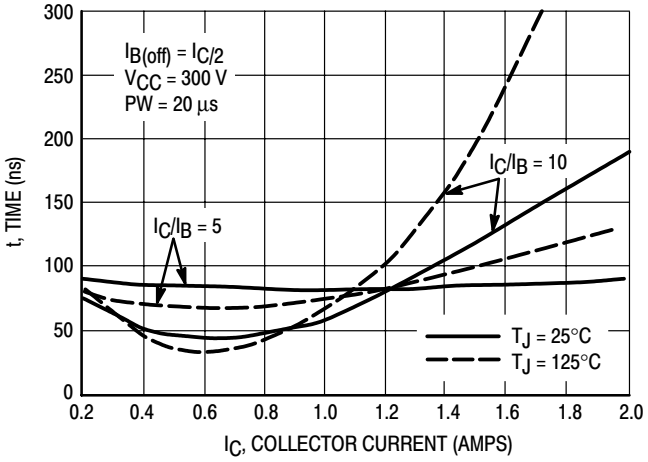


Figure 38. Resistive Switching, t_{on}

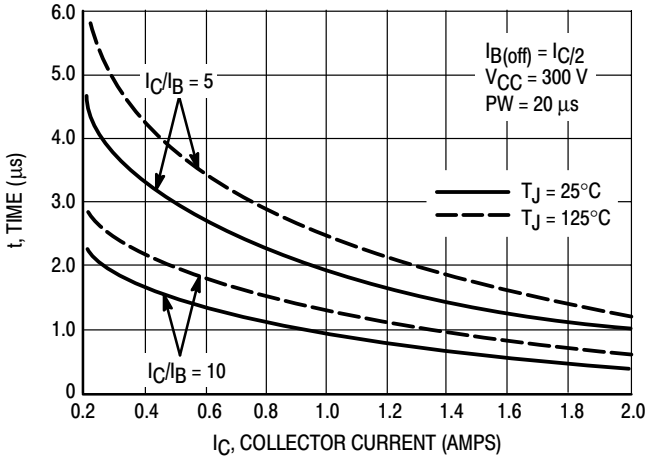


Figure 39. Resistive Switching, t_{off}

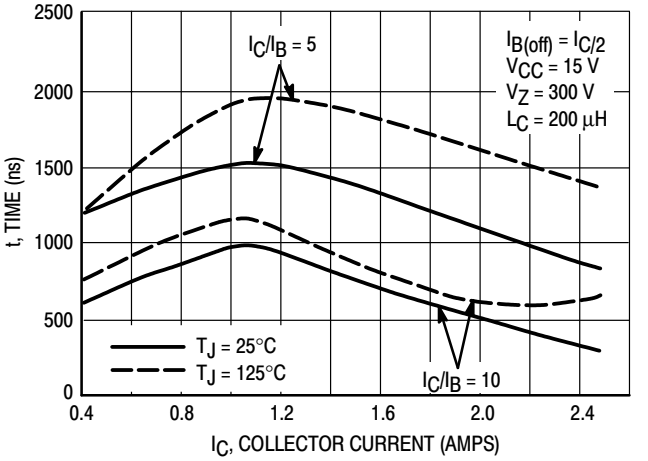


Figure 40. Inductive Storage Time, t_{si}

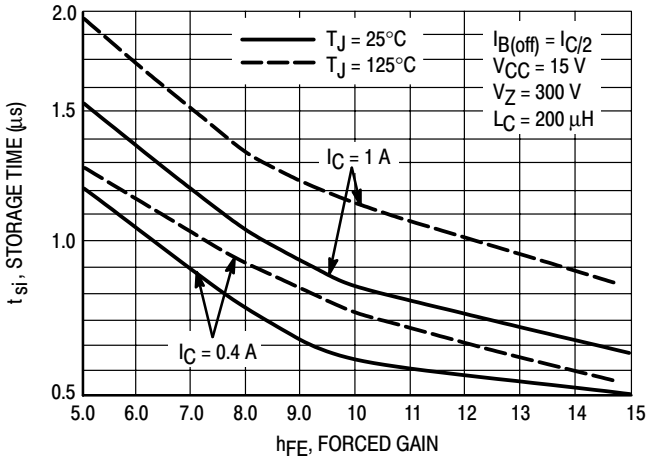


Figure 41. Inductive Storage Time

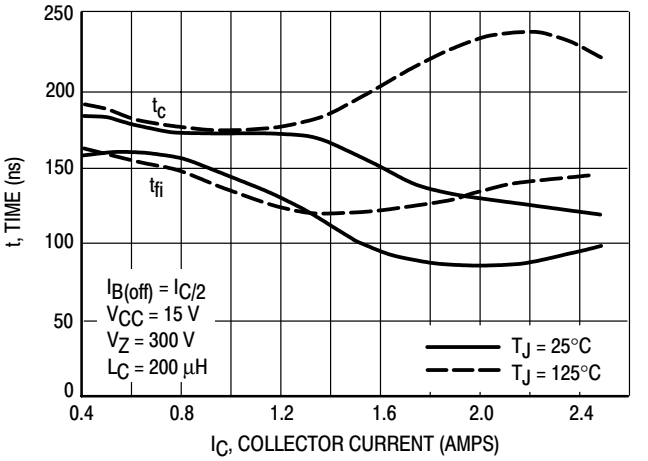


Figure 42. Inductive Switching, t_c and t_{fi} I_C/I_B = 5

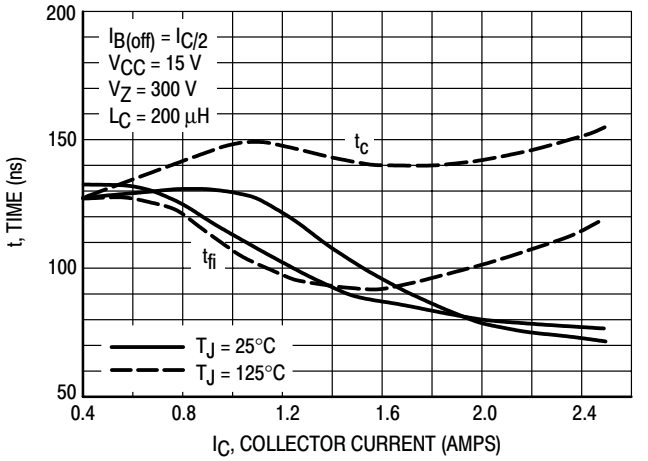


Figure 43. Inductive Switching, t_c and t_{fi} I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

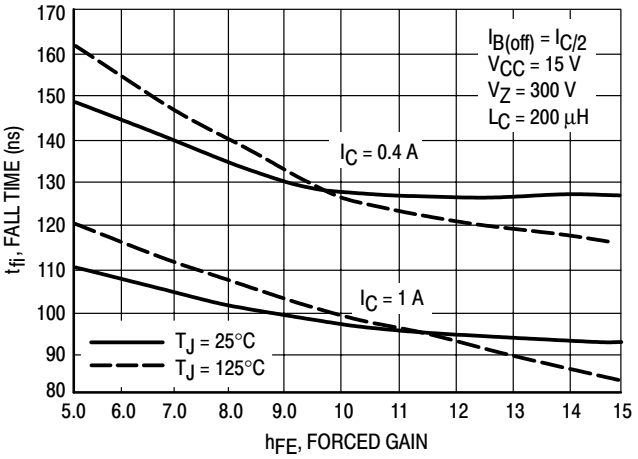


Figure 44. Inductive Fall Time

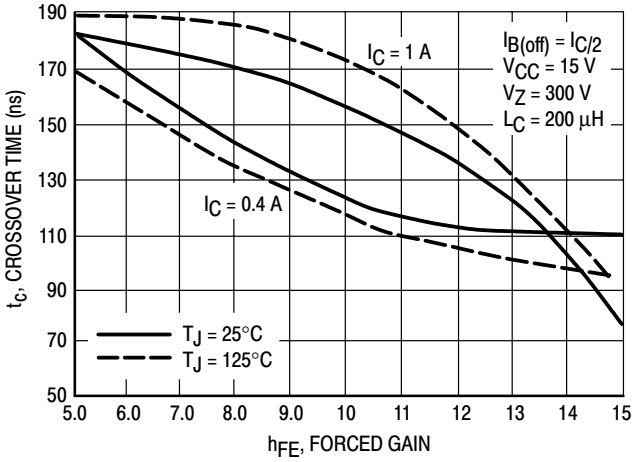


Figure 45. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

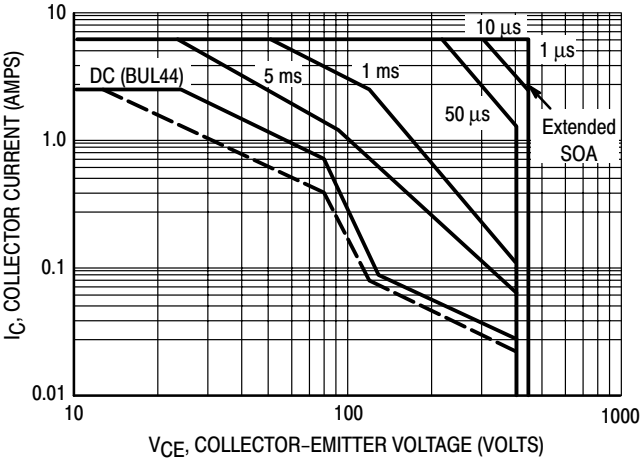


Figure 46. Forward Bias Safe Operating Area

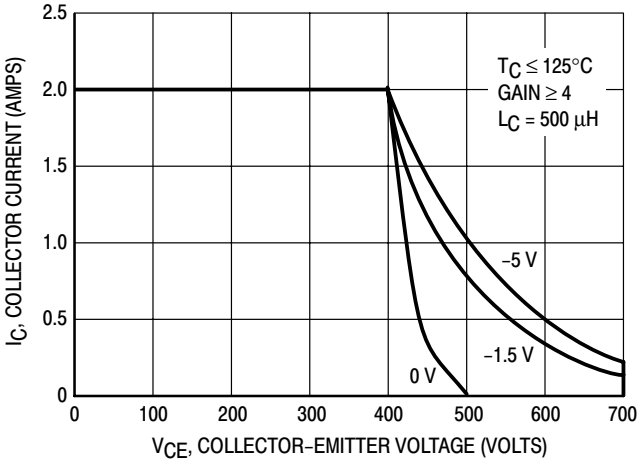


Figure 47. Reverse Bias Switching Safe Operating Area

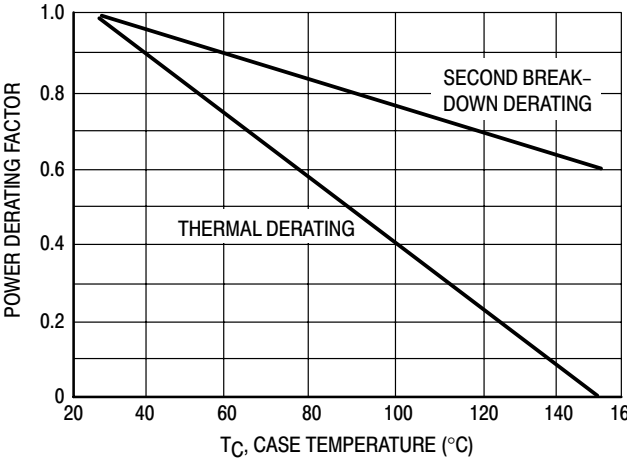


Figure 48. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 46 is based on T_C = 25°C; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on figure 46 may be found at any case temperature by using the appropriate curve on figure 48. $T_{J(PK)}$ may be calculated from the data in figure 51. At any case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 47). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

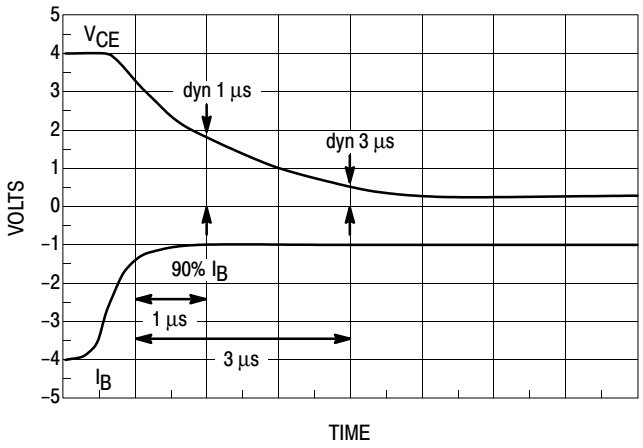


Figure 49. Dynamic Saturation Voltage Measurements

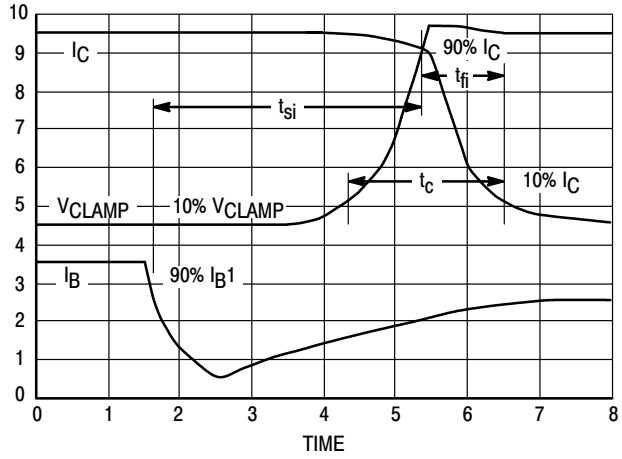
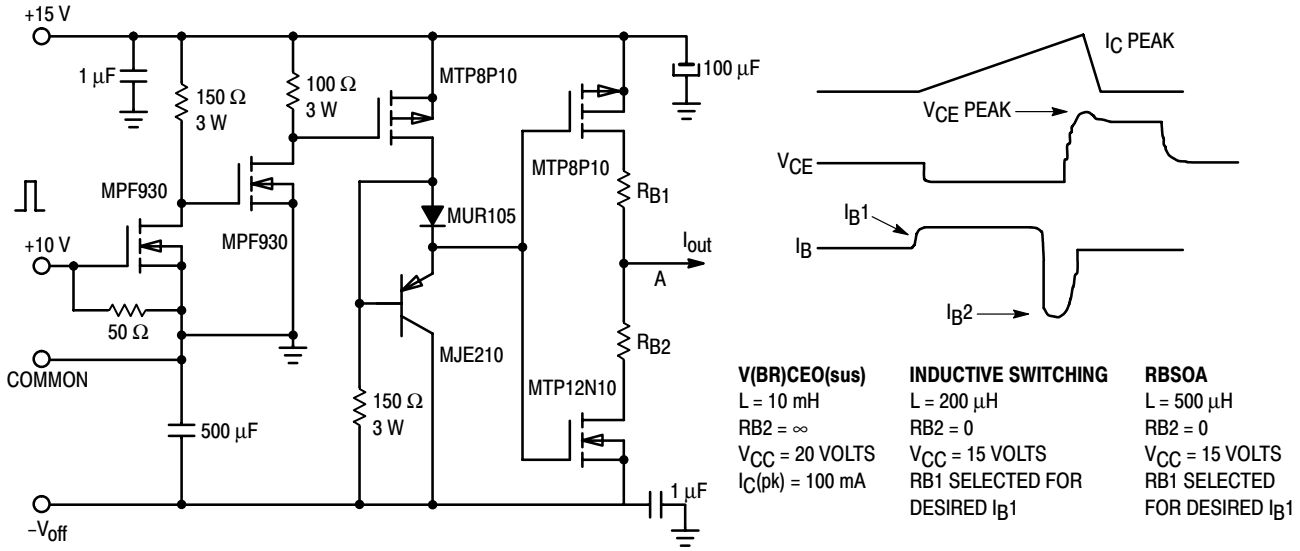


Figure 50. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

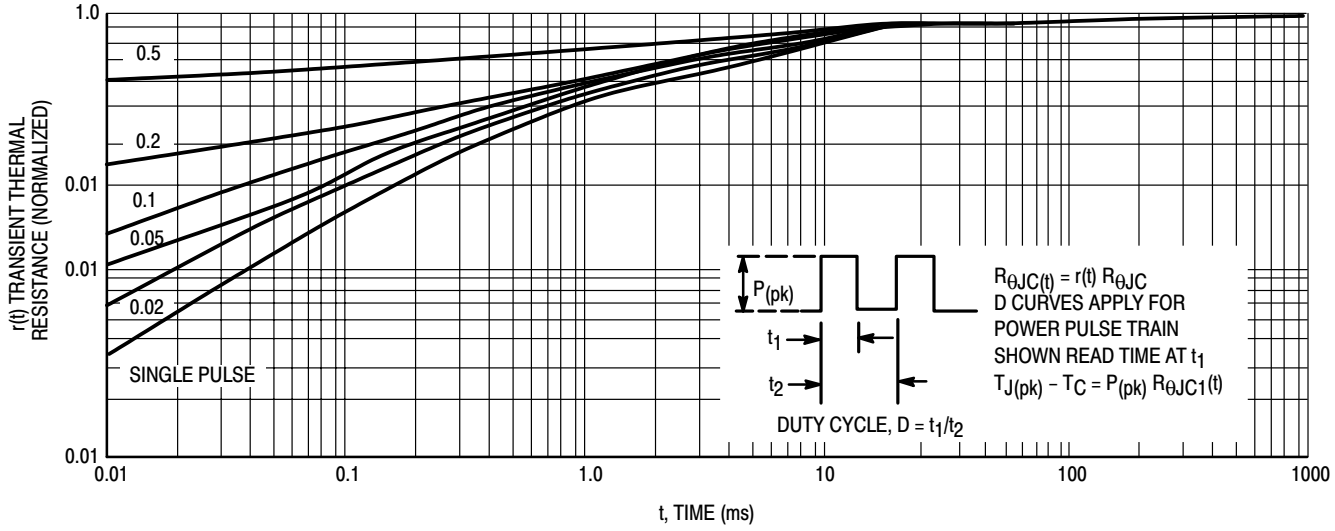
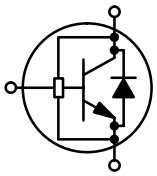


Figure 51. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL44

BUL45D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
5 AMPERES
700 VOLTS
75 WATTS

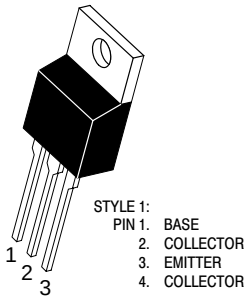


The BUL45D2 is state−of−art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector−Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.65 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	450		Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	910		Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14.1		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter−Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.89 0.79	1 0.9	
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.28 0.32	0.4 0.5	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.32 0.38	0.5 0.6	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.46 0.62	0.75 1	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	22 20	34 29		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 7	14 9.5		
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1 Adc)	@ T_C = 25°C @ T_C = 125°C	V_{EC}		1.04 0.7	1.5	V
(I_{EC} = 2 Adc)	@ T_C = 25°C @ T_C = 125°C			1.2	1.6	
(I_{EC} = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.85 0.62	1.2	
Forward Recovery Time (see Figure 27) (I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C	T_{fr}		330		ns
(I_F = 2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			360		
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			320		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)				f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)				C_{ob}		50	75	pF
Input Capacitance (V_{EB} = 8 Vdc)				C_{ib}		340	500	pF
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 A I_{B1} = 100 mA V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		3.7 9.4		V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C			0.35 2.7		V
	I_C = 2 A I_{B1} = 0.8 A V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C			3.9 12		V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C			0.4 1.5		V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}		90 105	150	ns
Turn−off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.5	1.3	µs
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}		90 110	150	ns
Turn−off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}	2.1	 3.1	2.4	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc		@ T_C = 25°C @ T_C = 125°C	t_f		90 93	150	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s		0.72 1.05	0.9	µs
Crossover Time			@ T_C = 25°C @ T_C = 125°C	t_c		95 95	150	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc		@ T_C = 25°C @ T_C = 125°C	t_f		80 105	150	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s	1.95	 2.9	2.25	µs
Crossover Time			@ T_C = 25°C @ T_C = 125°C	t_c		225 450	300	ns

TYPICAL STATIC CHARACTERISTICS

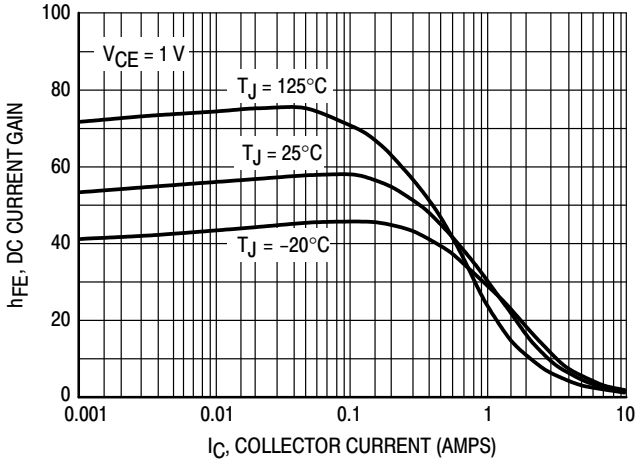


Figure 52. DC Current Gain @ 1 Volt

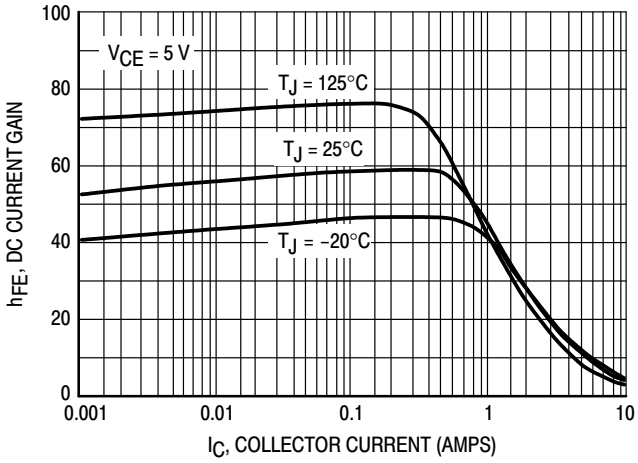


Figure 53. DC Current Gain @ 5 Volt

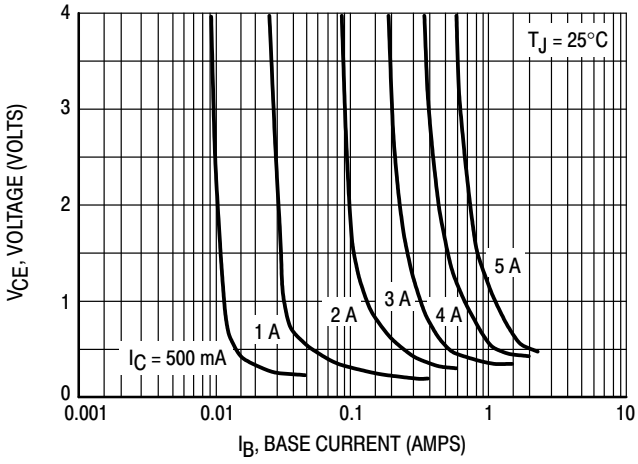


Figure 54. Collector Saturation Region

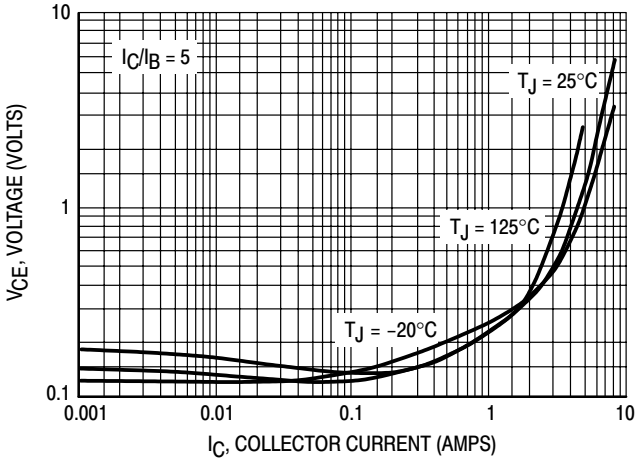


Figure 55. Collector−Emitter Saturation Voltage

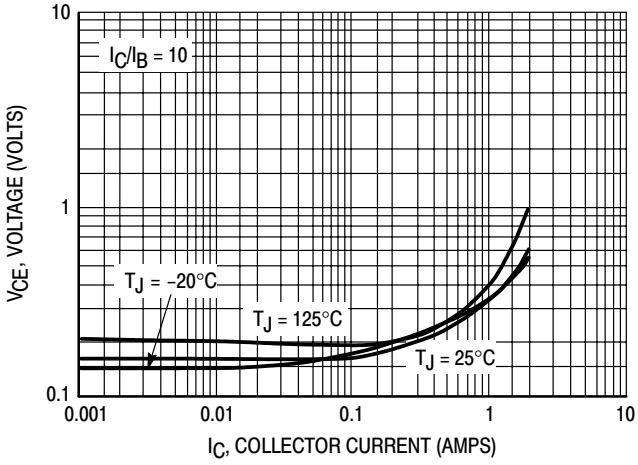


Figure 56. Collector−Emitter Saturation Voltage

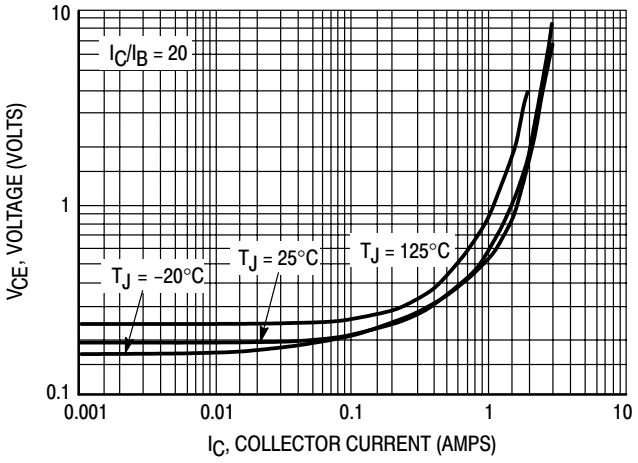


Figure 57. Collector−Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

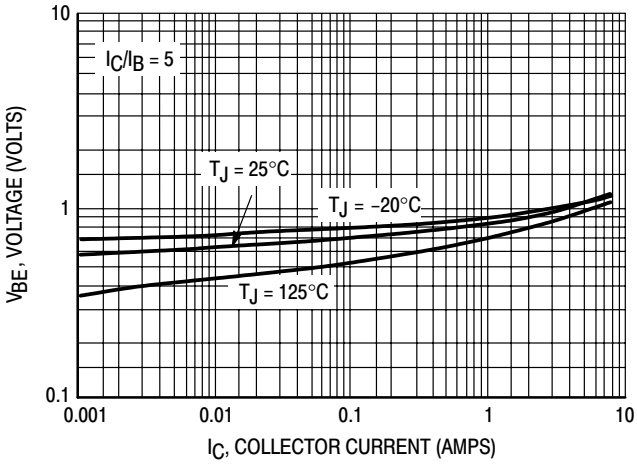


Figure 58. Base−Emitter Saturation Region

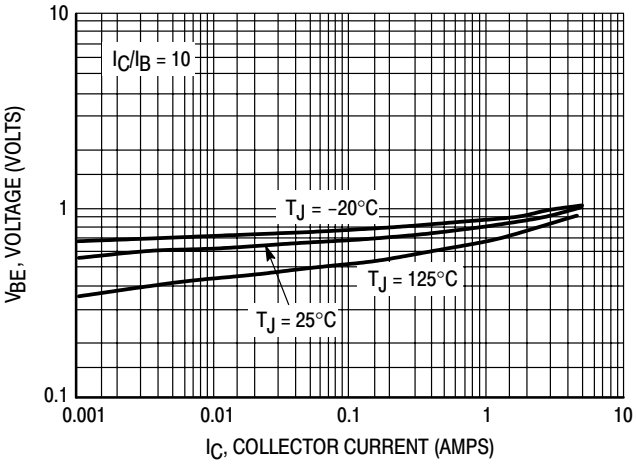


Figure 59. Base−Emitter Saturation Region

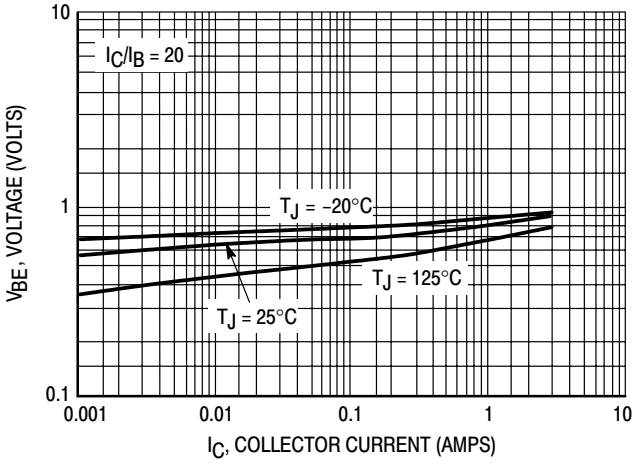


Figure 60. Base−Emitter Saturation Region

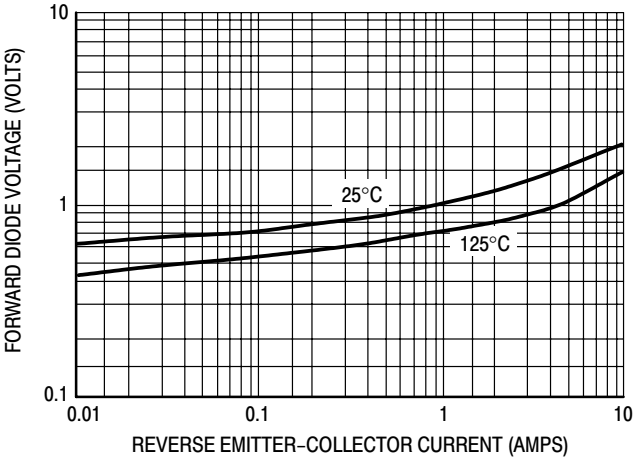


Figure 61. Forward Diode Voltage

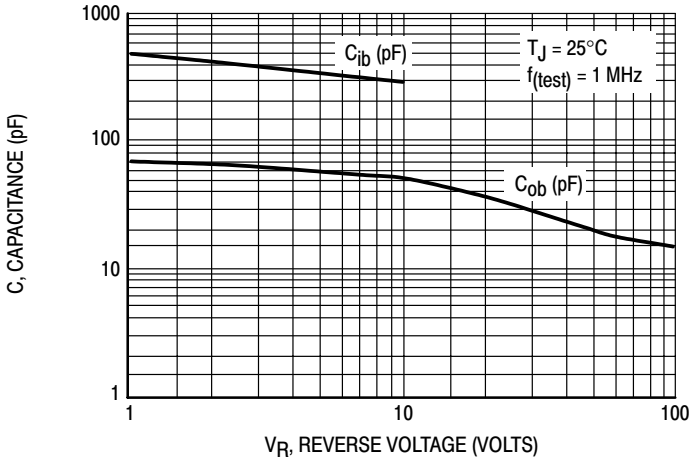


Figure 62. Capacitance

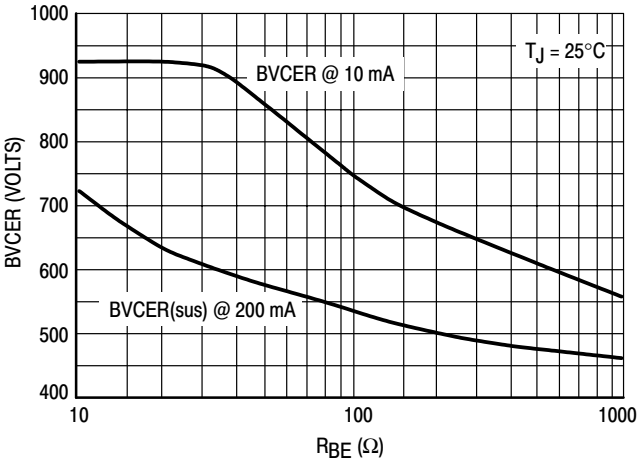


Figure 63. BVCER = f(ICER)

TYPICAL SWITCHING CHARACTERISTICS

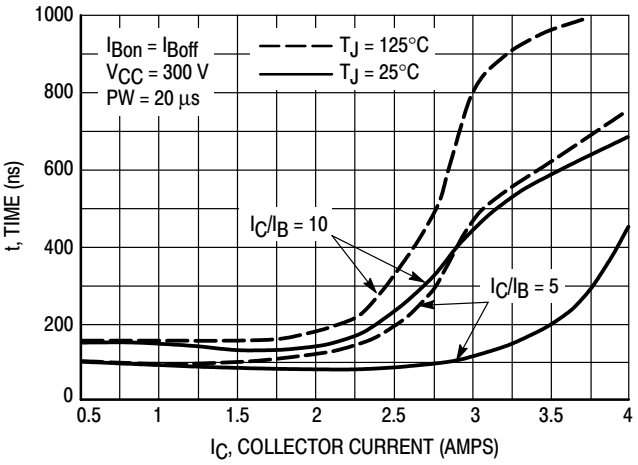


Figure 64. Resistive Switch Time, t_{on}

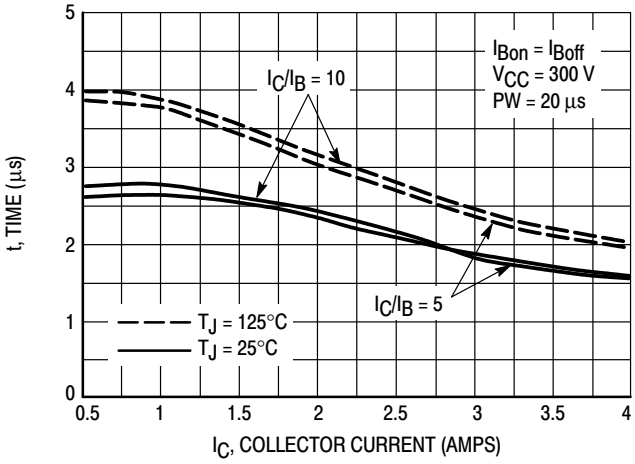


Figure 65. Resistive Switch Time, t_{off}

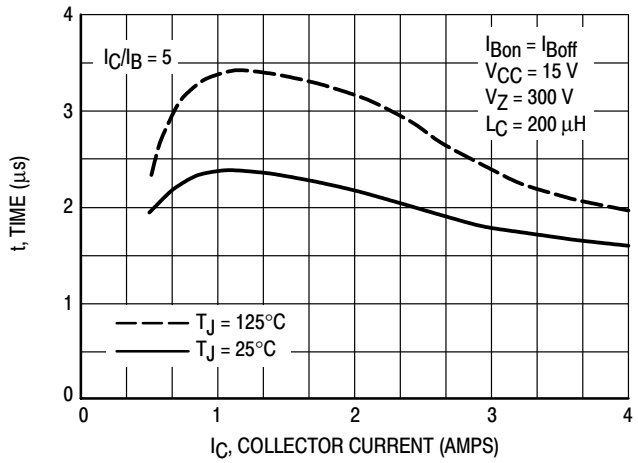


Figure 66. Inductive Storage Time, t_{si} @ I_C/I_B = 5

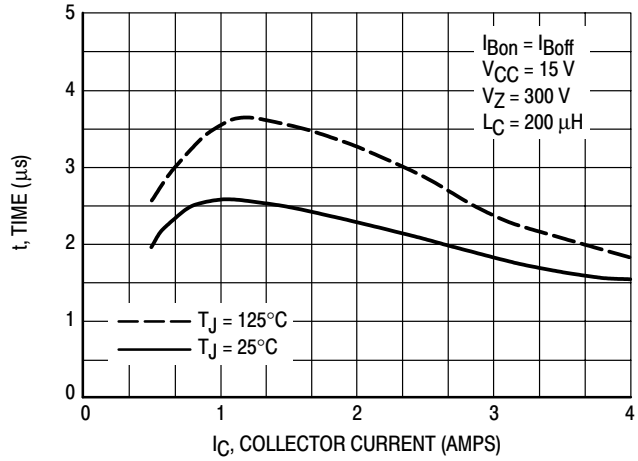


Figure 67. Inductive Storage Time, t_{si} @ I_C/I_B = 10

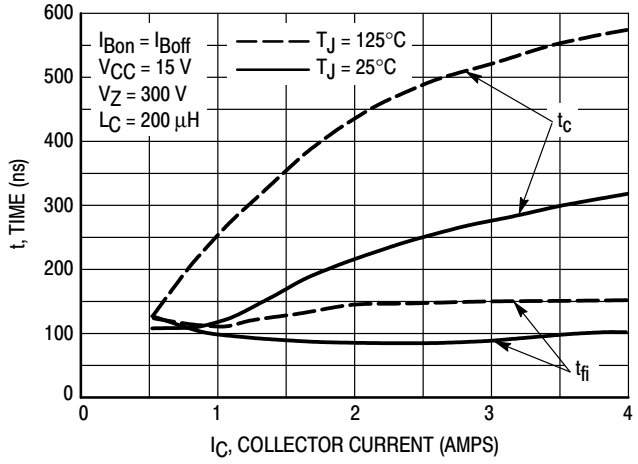


Figure 68. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

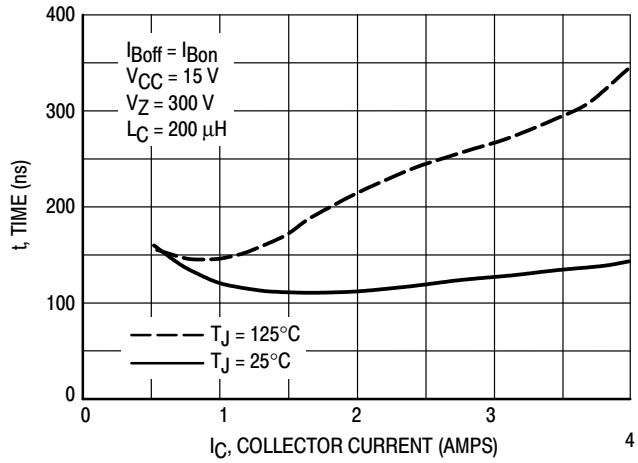


Figure 69. Inductive Switching, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

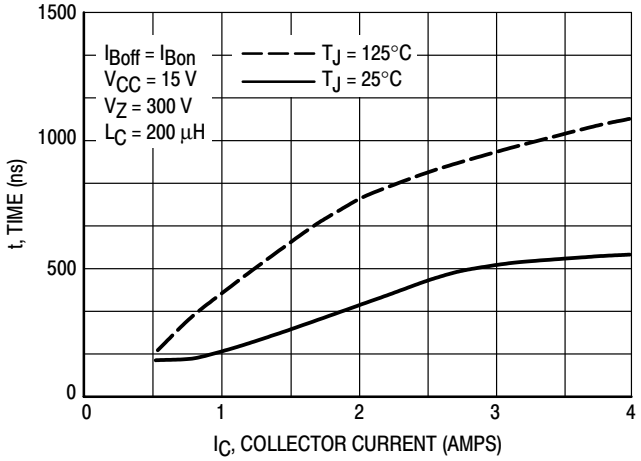


Figure 70. Inductive Switching, t_c @ I_C/I_B = 10

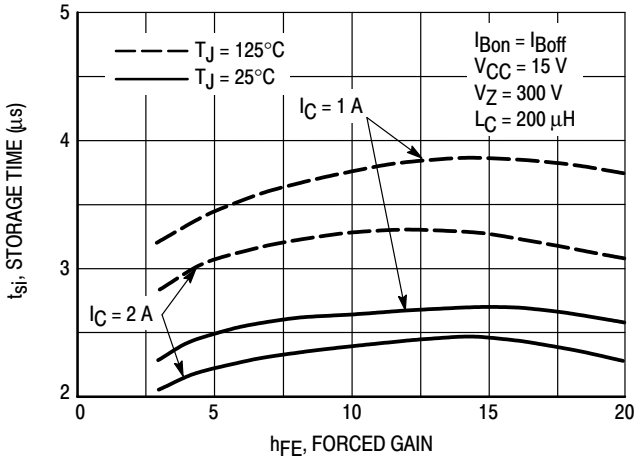


Figure 71. Inductive Storage Time

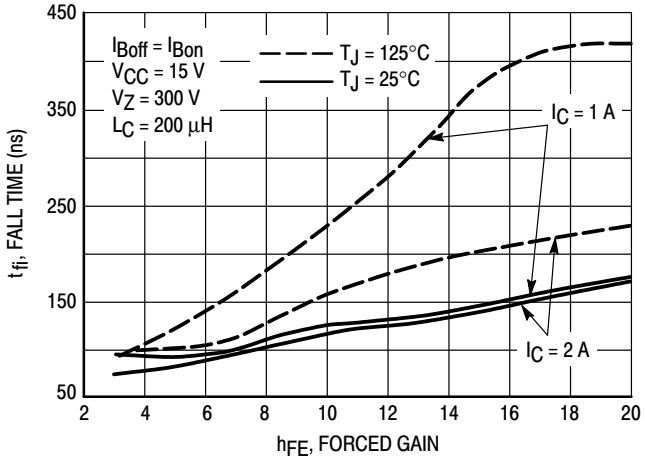


Figure 72. Inductive Fall Time

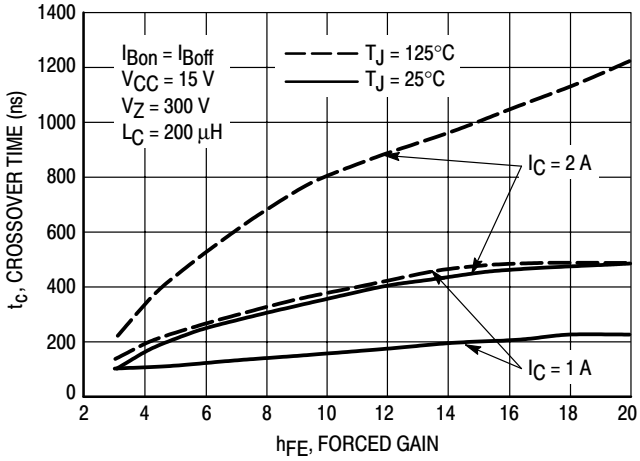


Figure 73. Inductive Crossover Time

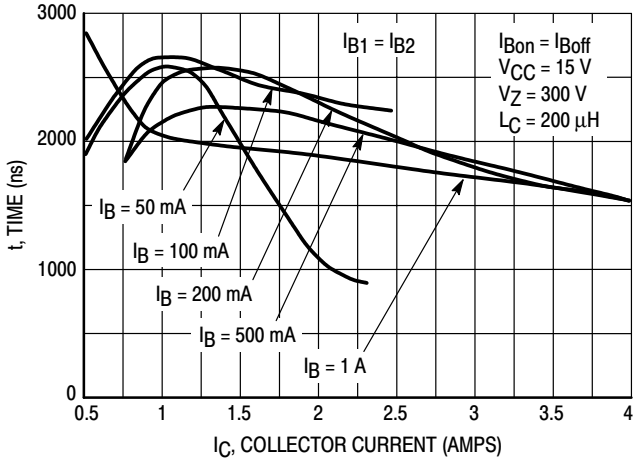


Figure 74. Inductive Storage Time, t_{si}

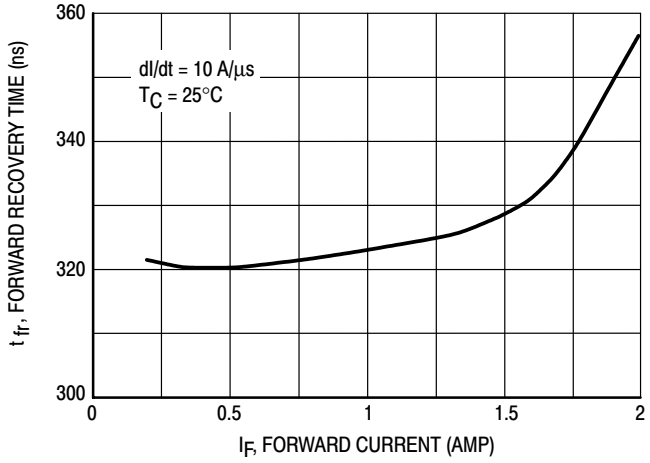


Figure 75. Forward Recovery Time t_{fr}

TYPICAL SWITCHING CHARACTERISTICS

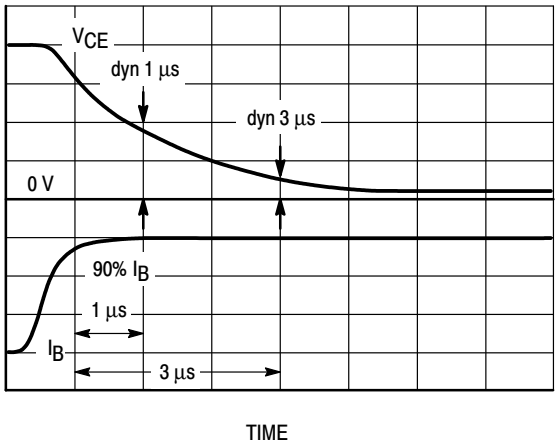


Figure 76. Dynamic Saturation Voltage Measurements

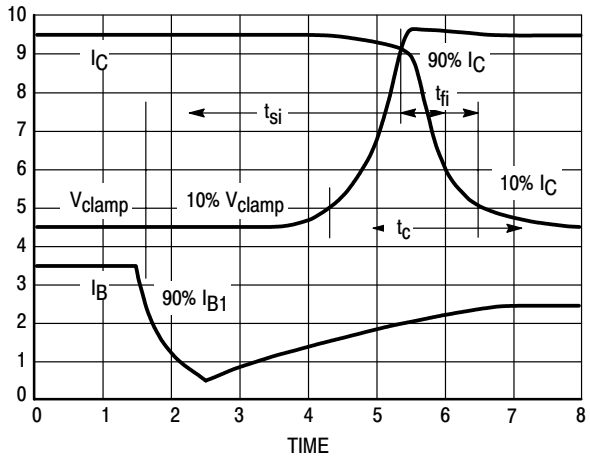


Figure 77. Inductive Switching Measurements

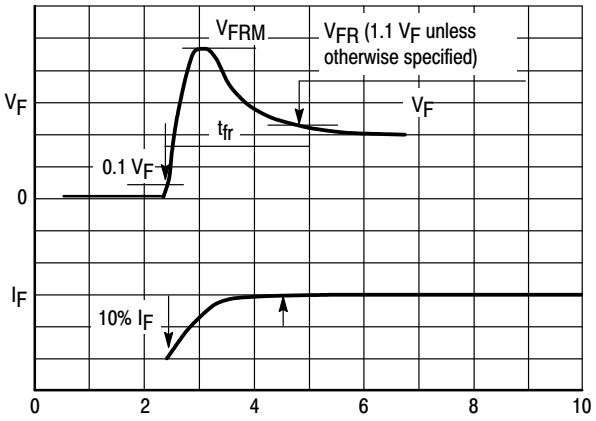
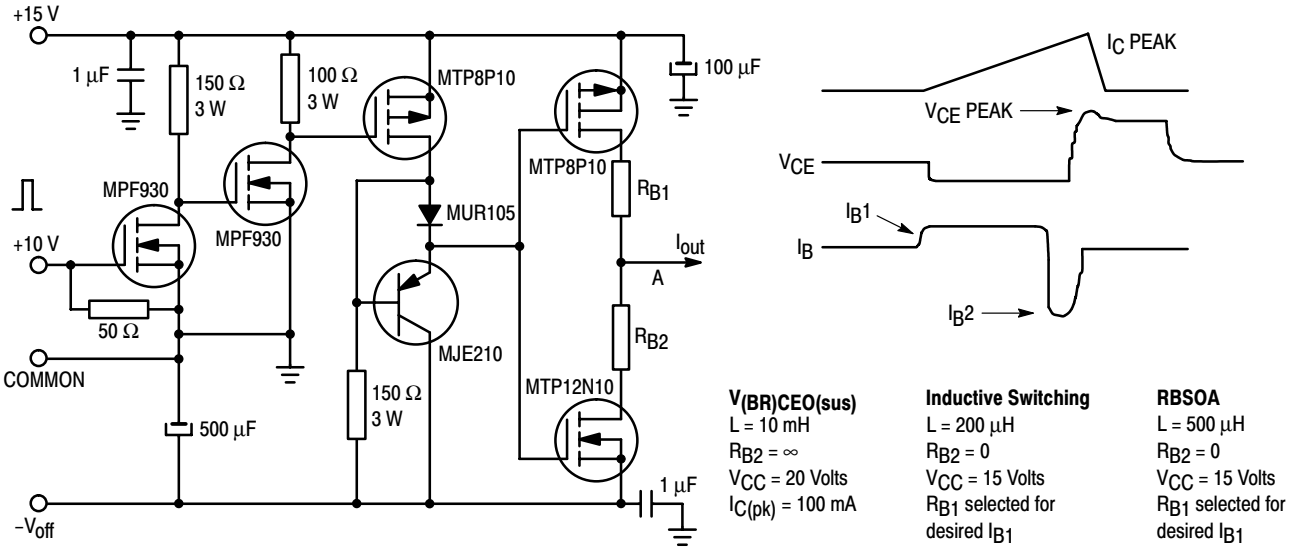


Figure 78. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



TYPICAL CHARACTERISTICS

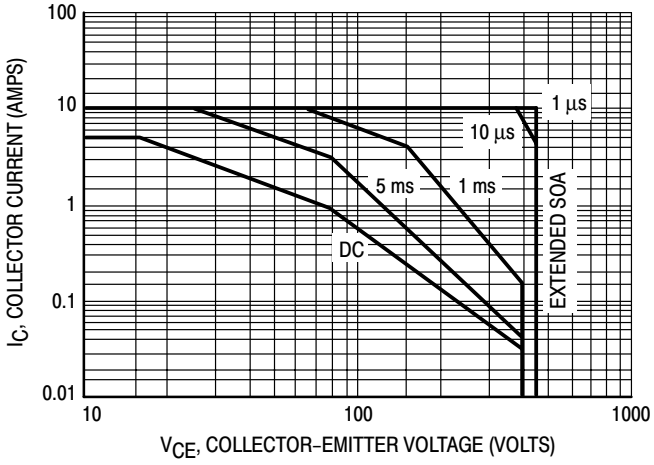


Figure 79. Forward Bias Safe Operating Area

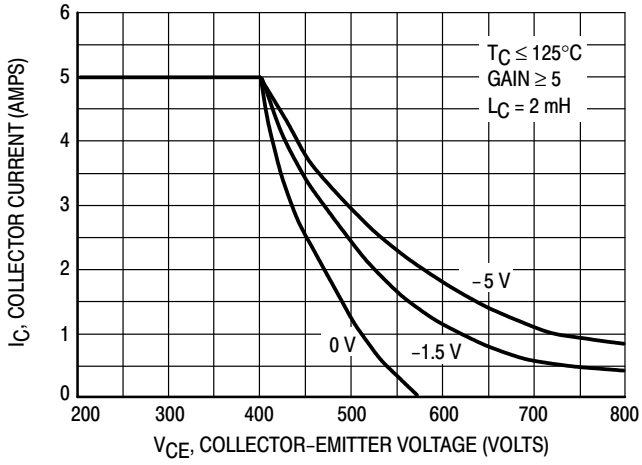


Figure 80. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

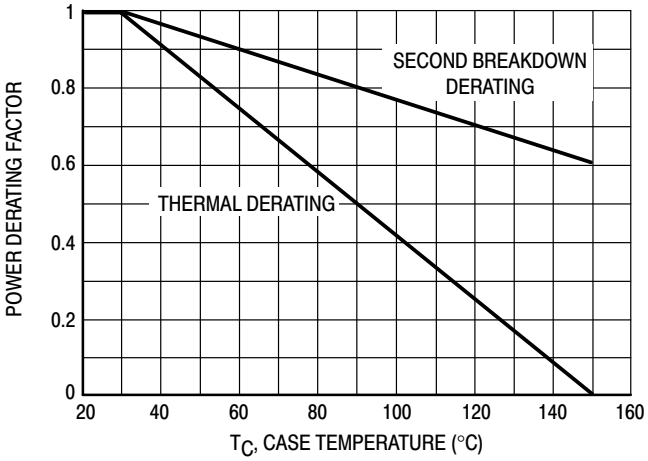


Figure 81. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 79 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 79 may be found at any case temperature by using the appropriate curve on Figure 81.

$T_{J(pk)}$ may be calculated from the data in Figure 82. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 80). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

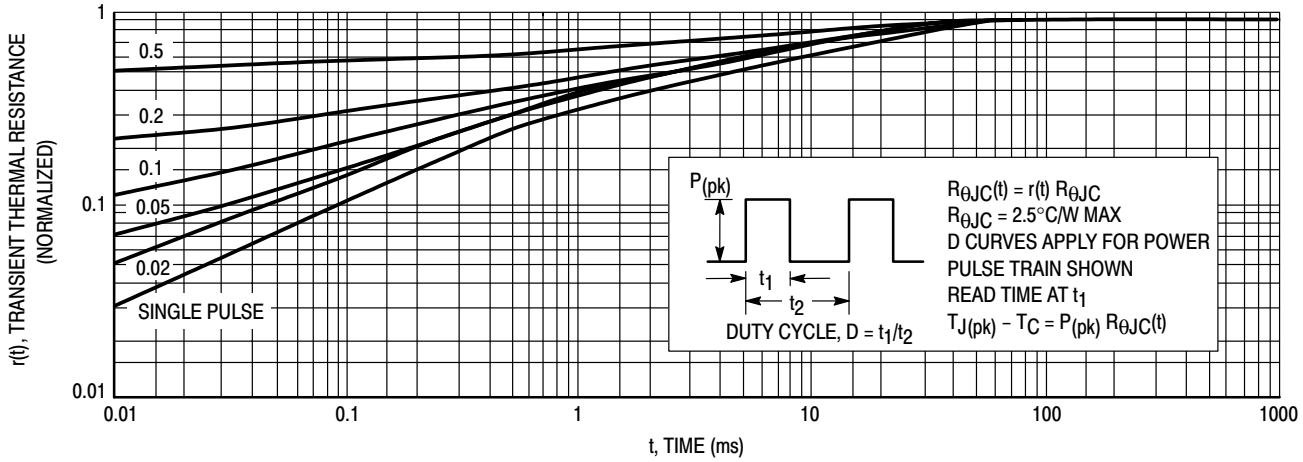


Figure 82. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45D2

BUL45

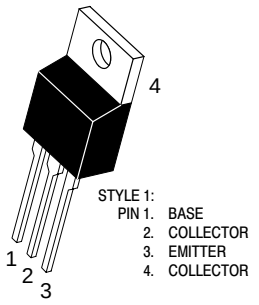
NPN Silicon Power Transistor

High Voltage SWITCHMODE™ Series

POWER TRANSISTOR
5.0 AMPERES
700 VOLTS
35 and 75 WATTS

Designed for use in electronic ballast (light ballast) and in Switchmode Power supplies up to 50 Watts. Main features include:

- Improved Efficiency Due to:
  - Low Base Drive Requirements (High and Flat DC Current Gain h_{FE})
  - Low Power Losses (On−State and Switching Operations)
  - Fast Switching: t_{fi} = 100 ns (typ) and t_{si} = 3.2 μs (typ) @ I_C = 2.0 A, I_{B1} = I_{B2} = 0.4 A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot−to−Lot



BUL45
CASE 221A−06
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	− 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (T_C = 125°C)	I_{CES}	— —	— —	10 100	μAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc) (I_C = 2.0 Adc, I_B = 0.4 Adc)				$V_{BE(sat)}$	— —	0.84 0.89	1.2 1.25	Vdc
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc) (T_C = 125°C)				$V_{CE(sat)}$	— —	0.175 0.150	0.25 —	Vdc
Collector−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.4 Adc) (T_C = 125°C)				$V_{CE(sat)}$	— —	0.25 0.275	0.4 —	Vdc
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc) (T_C = 125°C) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (T_C = 125°C) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				h_{FE}	14 — 7.0 5.0 10	— 32 14 12 22	34 — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	12	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	50	75	pF
Input Capacitance (V_{EB} = 8.0 Vdc)				C_{ib}	—	920	1200	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.0 Adc I_{B1} = 100 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	V_{CE} (Dyn sat)	— —	1.75 4.4	— —	Vdc
		3.0 μs	(T_C = 125°C)		— —	0.5 1.0	— —	
	(I_C = 2.0 Adc I_{B1} = 400 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	1.85 6.0	— —	
		3.0 μs	(T_C = 125°C)		— —	0.5 1.0	— —	

SWITCHING CHARACTERISTICS: Resistive Load

Turn−On Time	(I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.4 Adc Pulse Width = 20 μs, (T_C = 125°C) Duty Cycle < 20% V_{CC} = 300 V)	t_{on}	— —	75 120	110 —	ns
Turn−Off Time	(T_C = 125°C)	t_{off}	— —	2.8 3.5	3.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 Vdc, L_C = 200 μH, V_{clamp} = 300 Vdc)

Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc) (T_C = 125°C)	t_{fi}	70 —	— 200	170 —	ns
Storage Time	(T_C = 125°C)	t_{si}	2.6 —	— 4.2	3.8 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	230 400	350 —	ns
Fall Time	(I_C = 1.0 Adc, I_{B1} = 100 mAdc I_{B2} = 0.5 Adc) (T_C = 125°C)	t_{fi}	— —	110 100	150 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.1 1.5	1.7 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	170 170	250 —	ns
Fall Time	(I_C = 2.0 Adc, I_{B1} = 250 mAdc I_{B2} = 2.0 Adc) (T_C = 125°C)	t_{fi}	—	80	120	ns
Storage Time	(T_C = 125°C)	t_{si}	—	0.6	0.9	μs
Crossover Time	(T_C = 125°C)	t_c	—	175	300	ns

TYPICAL STATIC CHARACTERISTICS

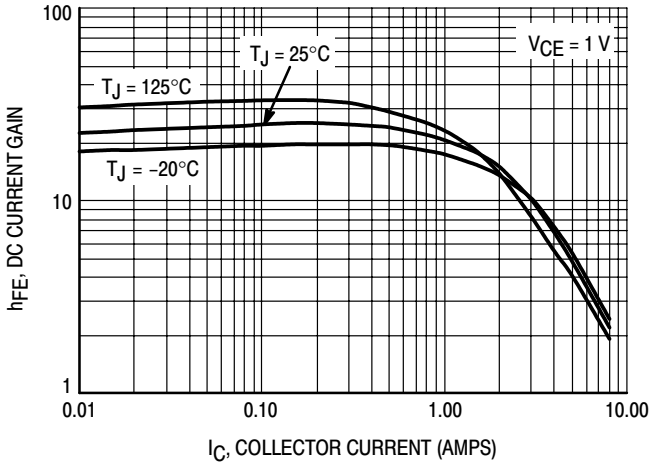


Figure 1. DC Current Gain @ 1 Volt

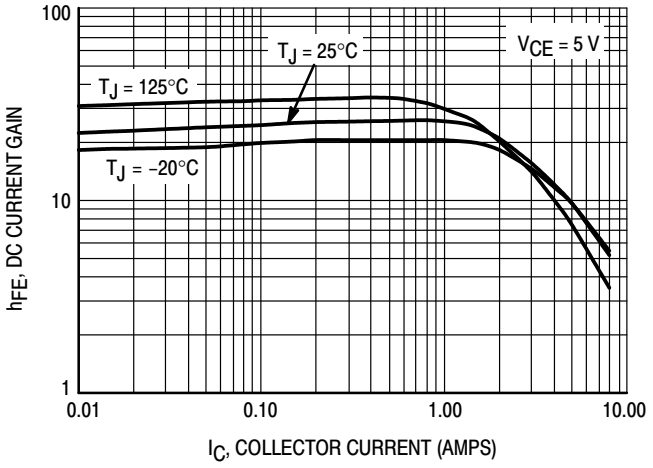


Figure 2. DC Current Gain at @ 5 Volts

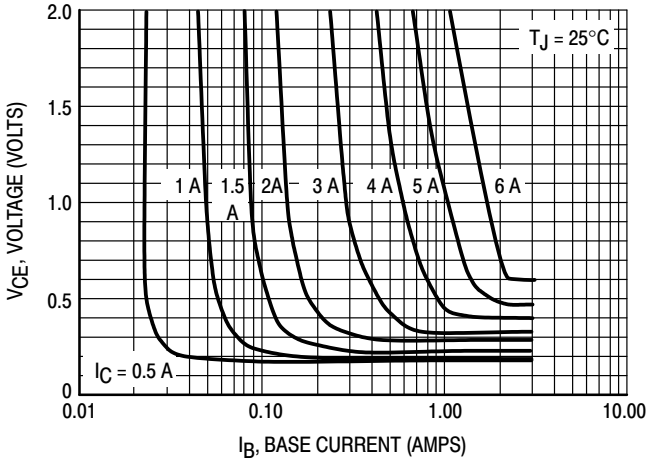


Figure 3. Collector−Emitter Saturation Region

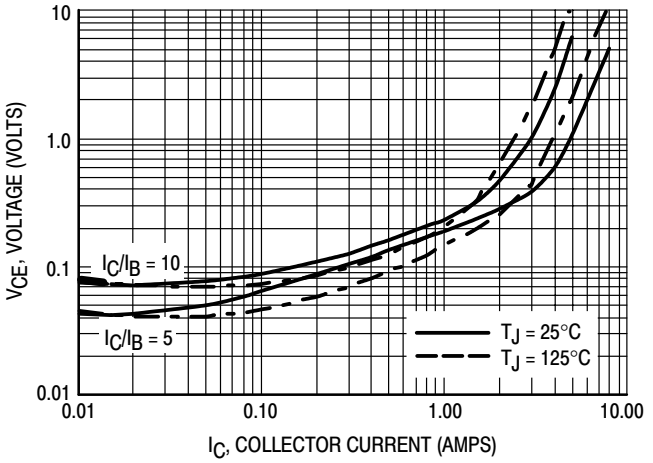


Figure 4. Collector−Emitter Saturation Voltage

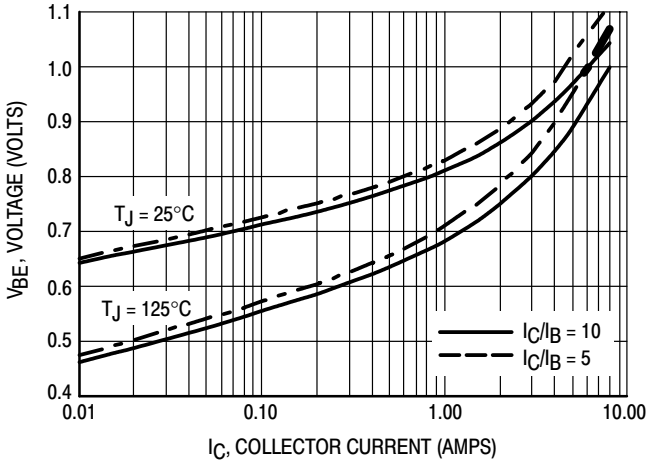


Figure 5. Base−Emitter Saturation Region

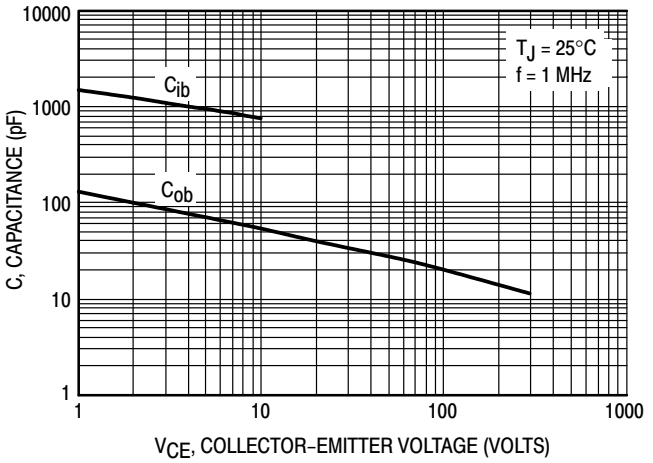


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

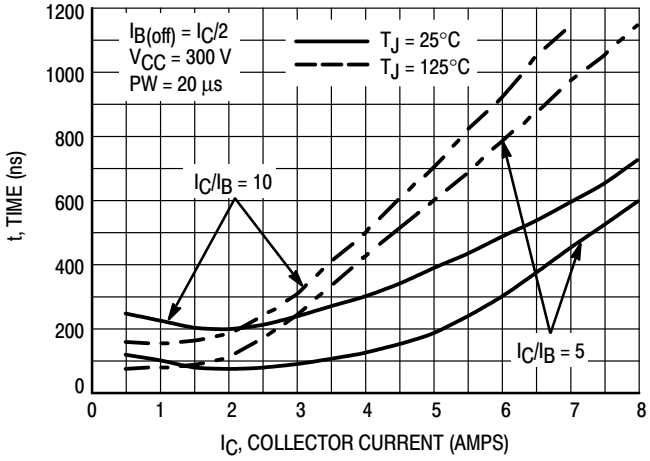


Figure 7. Resistive Switching, t_{on}

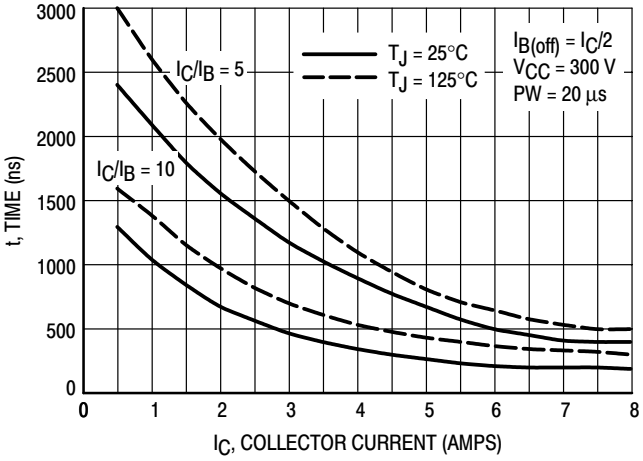


Figure 8. Resistive Switching, t_{off}

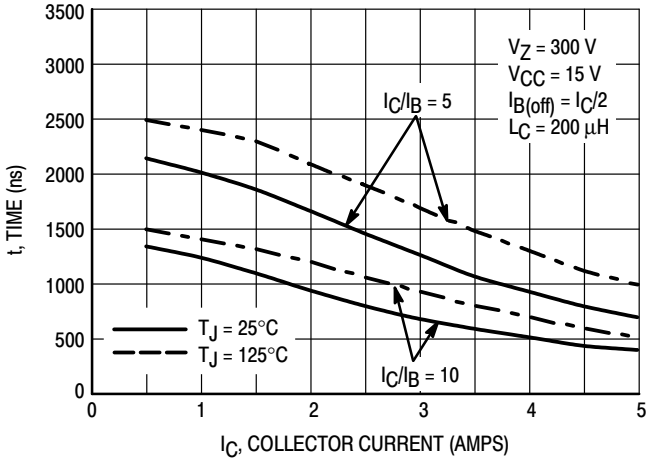


Figure 9. Inductive Storage Time, t_{si}

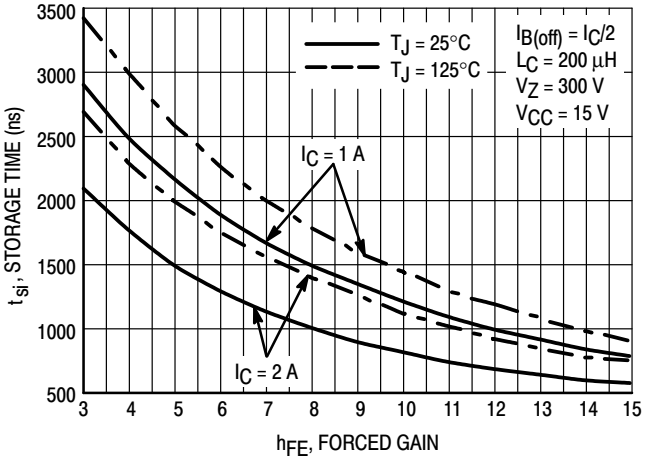


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

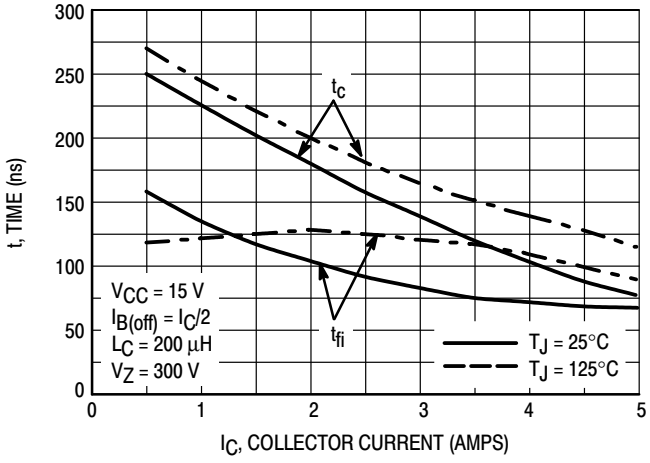


Figure 11. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 5$

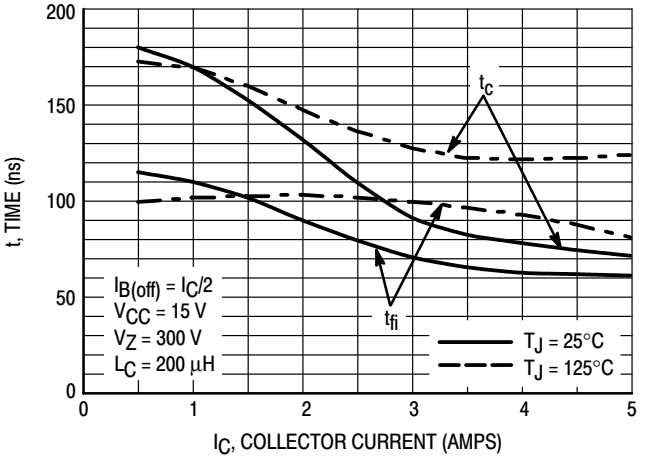


Figure 12. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

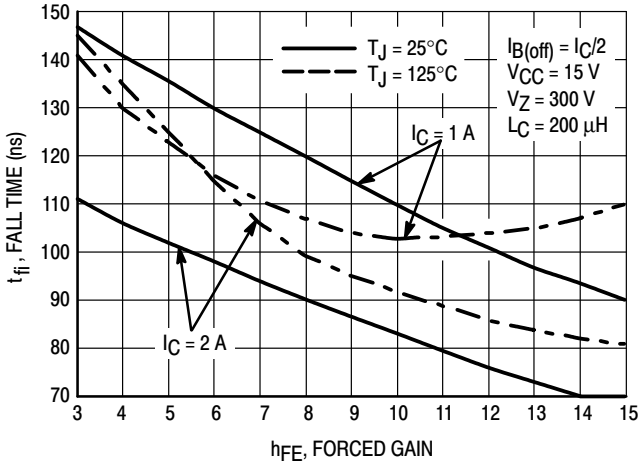


Figure 13. Inductive Fall Time, $t_{fi}(h_{FE})$

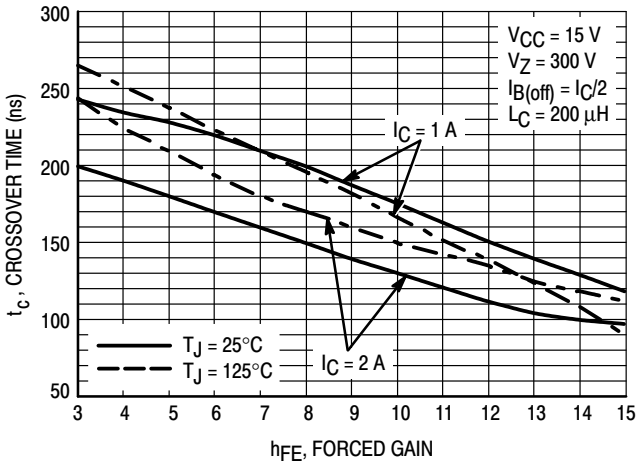


Figure 14. Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

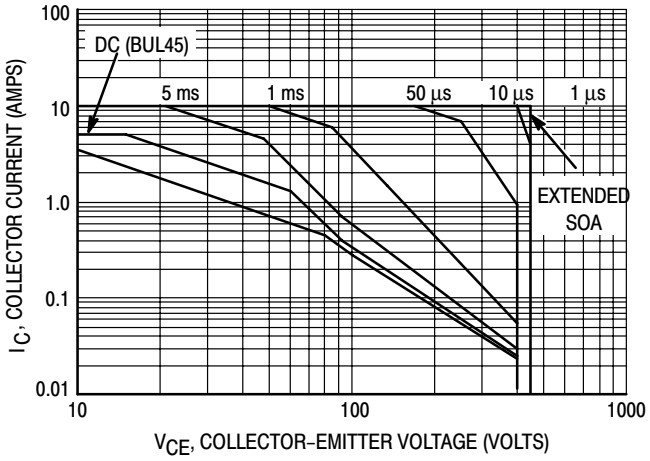


Figure 15. Forward Bias Safe Operating Area

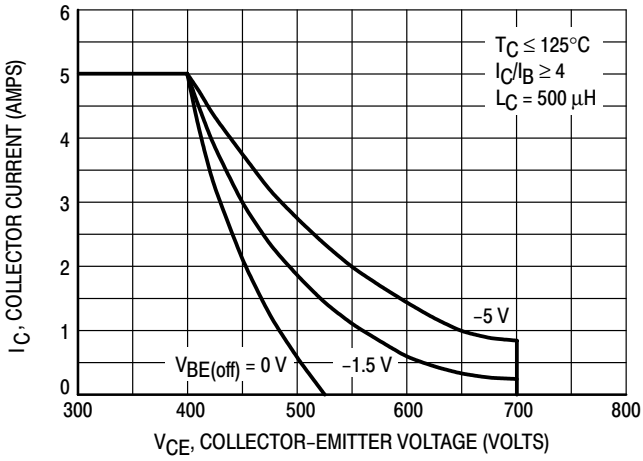


Figure 16. Reverse Bias Switching Safe Operating Area

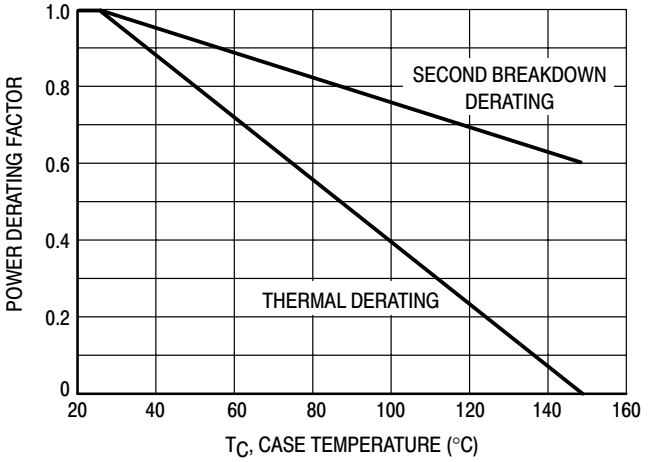


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

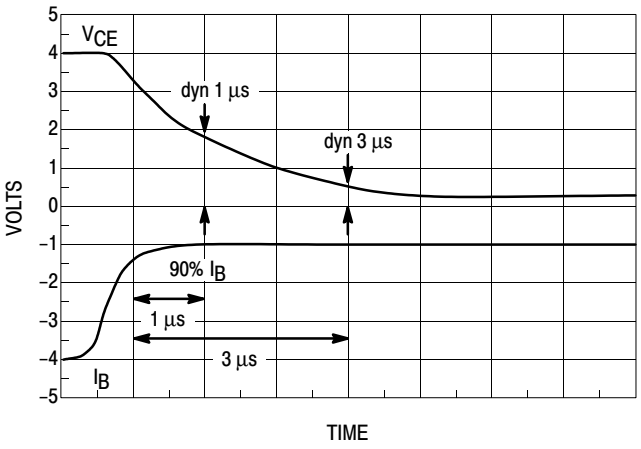


Figure 18. Dynamic Saturation Voltage Measurements

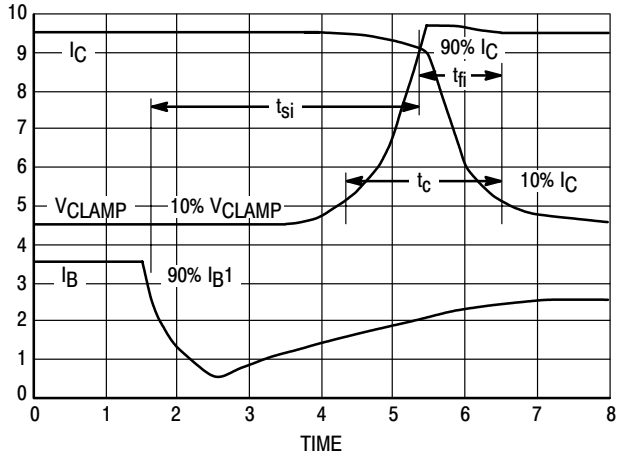
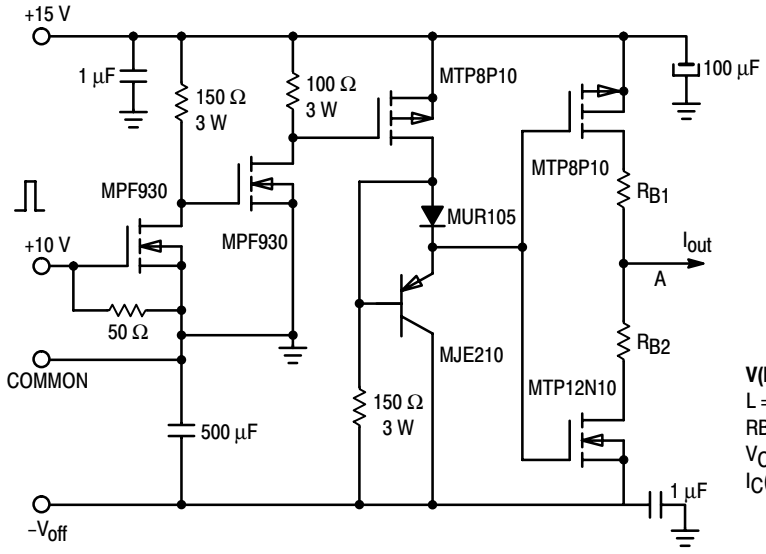
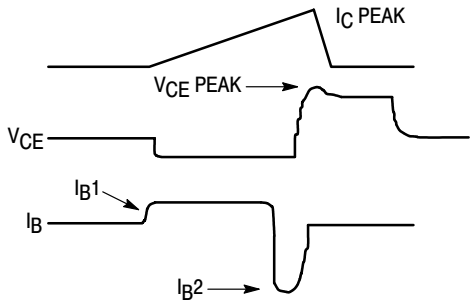


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

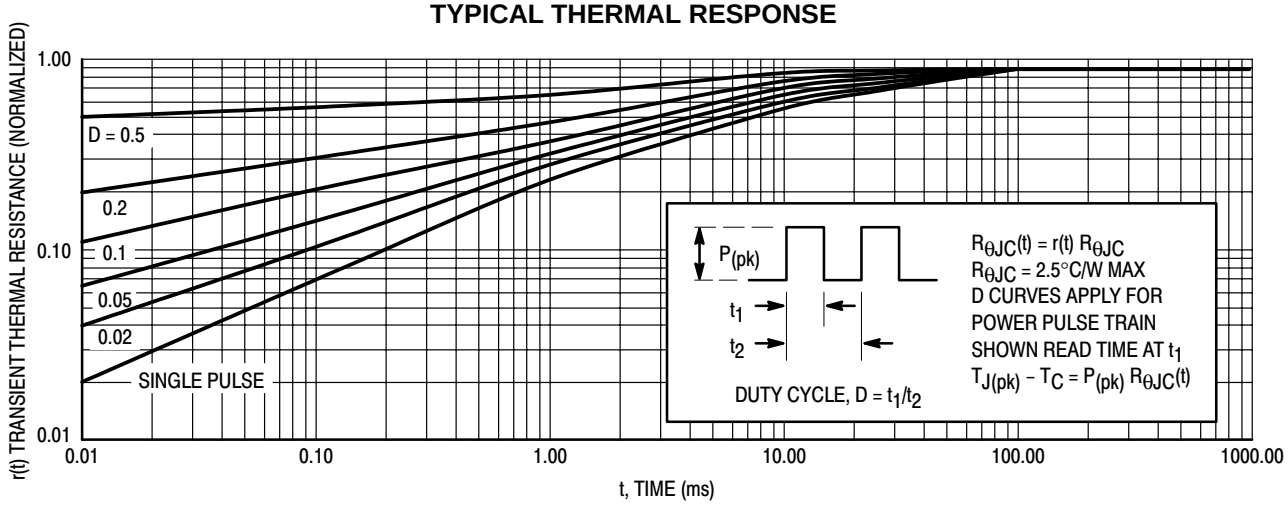
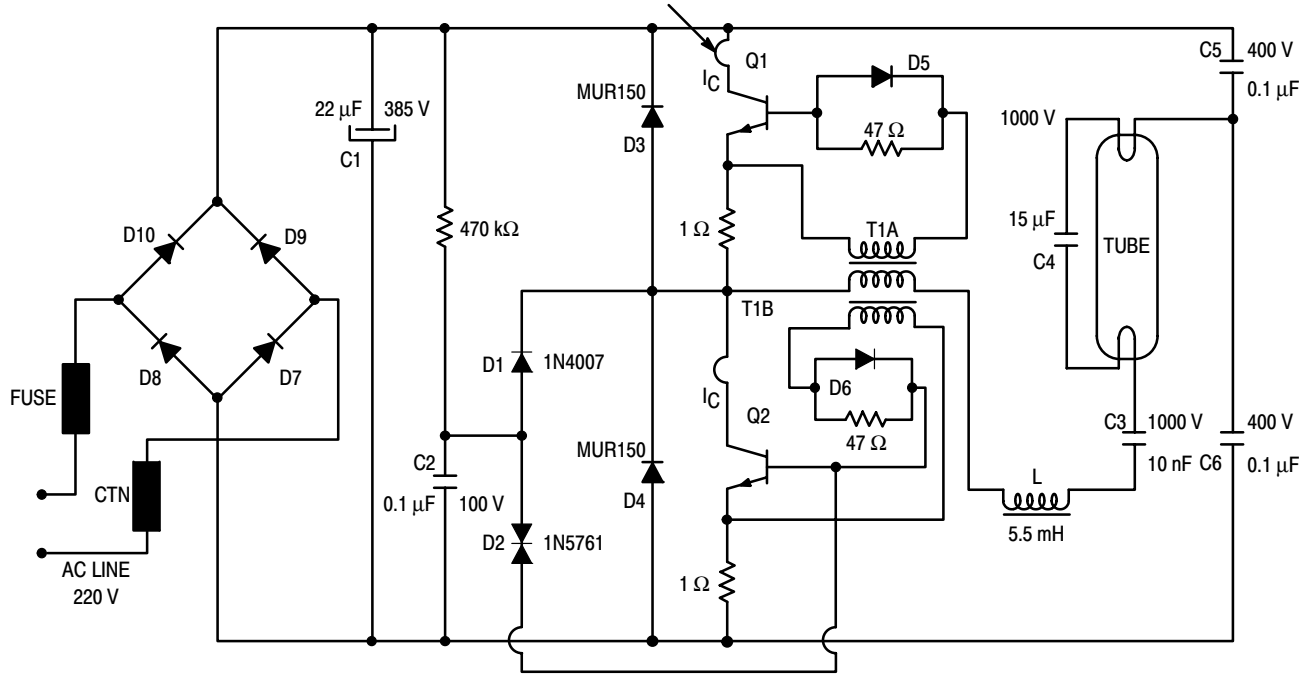


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45

The BUL45 Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by ON Semiconductor applications was built to demonstrate how well these devices operate. The circuit and detailed component list are provided below.



Components Lists

Q1 = Q2 = BUL45 Transistor
D1 = 1N4007 Rectifier
D2 = 1N5761 Rectifier
D3 = D4 = MUR150
D5 = D6 = MUR105
D7 = D8 = D9 = D10 = 1N400
CTN = 47 Ω @ 25°C
L = RM10 core, A1 = 400, B51 (LCC) 75 turns, wire ∅ = 0.6 mm
T1 = FT10 toroid, T4A (LCC)
Primary: 4 turns
Secondaries: T1A: 4 turns
T1B: 4 turns

All resistors are 1/4 Watt, ±5%
R1 = 470 kΩ
R2 = R3 = 47 Ω
R4 = R5 = 1 Ω (these resistors are optional, and might be replaced by a short circuit)
C1 = 22 μF/385 V
C2 = 0.1 μF
C3 = 10 nF/1000 V
C4 = 15 nF/1000 V
C5 = C6 = 0.1 μF/400 V

NOTES:
1. Since this design does not include the line input filter, it cannot be used “as−is” in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re−calculated with any other loads.

Figure 21. Application Example

BUL642D2

High Speed, High Gain Bipolar NPN Transistor with Integrated Collector-Emitter and Built-in Efficient Antisaturation Network

The BUL642D2 is a state−of−the−art High Speed High Gain Bipolar Transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (150 ns on storage time) make it ideally suitable for Light Ballast Application. A new development process brings avalanche energy capability, making the device extremely rugged.

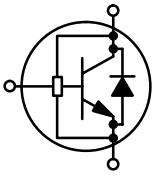
Main Features:

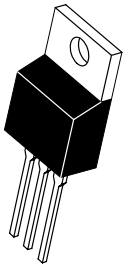
- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 300 mA/5 V
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector−Emitter Free Wheeling Diode
- Fully Characterized Dynamic V_{CEsat}
- “Six Sigma” Process Providing Tight and Reproducible Parameter Spreads
- Avalanche Energy 20 mJ Typical Capability

ON Semiconductor®

http://onsemi.com

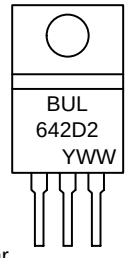
3 AMPERES
825 VOLTS
75 WATTS
POWER TRANSISTOR





TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BUL642D2	TO−220	50 Units/Rail

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	440	Vdc
Collector−Base Breakdown Voltage	V_{CES}	825	Vdc
Emitter−Base Voltage	V_{EBO}	11	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	3.0 8.0	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	2.0 4.0	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to +150	°C

TYPICAL GAIN

Typical Gain @ I_C = 1 A, V_{CE} = 2 V Typical Gain @ I_C = 0.3 A, V_{CE} = 1 V	h_{FE} h_{FE}	45 50	− −

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Case	$R_{\theta JC}$	1.6	°C/W
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 seconds	T_L	260	°C

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector−Emitter Sustaining Voltage (I_C = 200 mA, L = 25 mH)			$V_{CEO(sus)}$	440	−	−	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)			V_{CBO}	825	−	−	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)			V_{EBO}	11	−	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		@ T_C = 25°C @ T_C = 125°C	I_{CEO}	− −	− −	200 1000	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)		@ T_C = 25°C @ T_C = 125°C	I_{CES}	− −	− −	100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)			I_{EBO}	−	−	100	μAdc
ON CHARACTERISTICS							
Base−Emitter Saturation Voltage (IC = 0.5 Adc, I_B = 100 mAdc (I_C = 1 Adc, I_B = 0.2 Adc)			$V_{BE(sat)}$	− −	− −	1.1 1.5	Vdc
Collector−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 0.2 Adc)			$V_{CE(sat)}$	− −	− −	0.5 1.5	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 1 Vdc) (I_C = 0.5 Adc, V_{CE} = 3 Vdc)			h_{FE}	16 18	− −	− −	−
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage:	I_C = 0.5 Adc I_{B1} = 50 mAdc V_{CC} = 125 Vdc	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	− −	2.0 5.0	− −	V
		@ 3 μs	@ T_C = 25°C		− −	0.2 1.3	− −	
	I_C = 1 Adc I_{B1} = 100 mAdc V_{CC} = 300 Vdc	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		− −	4.5 10	− −	
		@ 3 μs	@ T_C = 25°C		− −	1.0 3.0	− −	
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz			f_T	−	13	−	MHz
Output Capacitance @ V_{cb} = 10 V, I_E = 0, f = 1 MHz			C_{ob}	−	70	150	pF
Input Capacitance @ V_{EB} = 8 V, f = 1 MHz			C_{ib}	−	500	1000	pF
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 0.5 Adc) (I_{EC} = 1.0 Adc)			V_{EC}	− −	0.8 1.0	1.5 2.0	V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 70 μs)							
Delay Time	I_C = 0.5 Adc		t_d	−	60	400	ns
Rise Time	I_{B1} = 45 mA		t_r	−	160	1100	ns
Storage Time	I_{B2} = 500 mA		t_s	−	0.5	1400	μs
Fall Time	V_{CC} = 125 V		t_f	−	0.4	600	ns

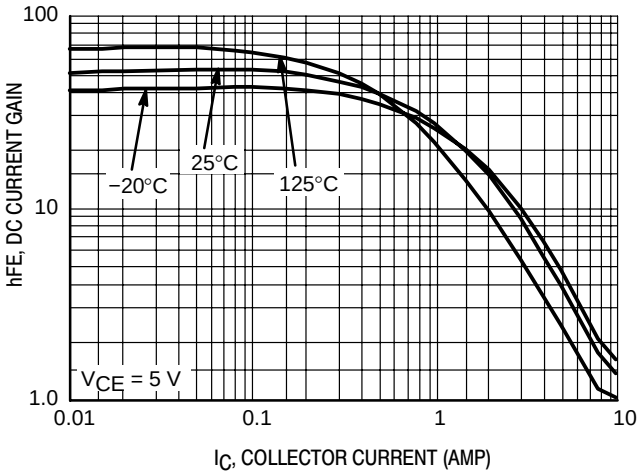


Figure 1. DC Current Gain

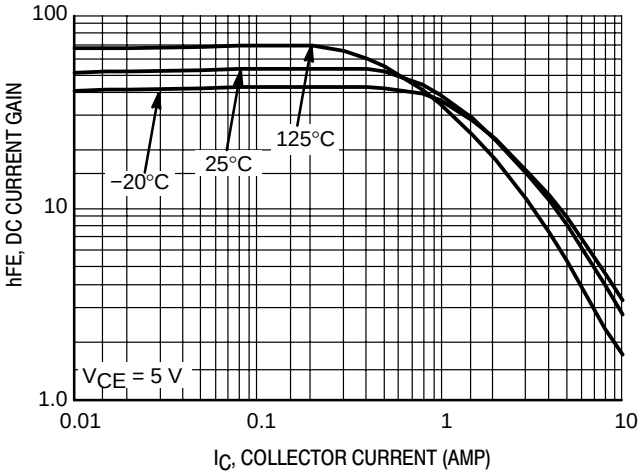


Figure 2. DC Current Gain

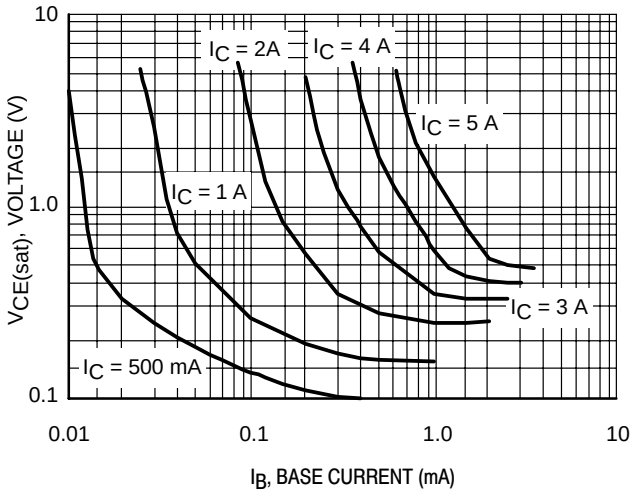


Figure 3. Collector Saturation Region

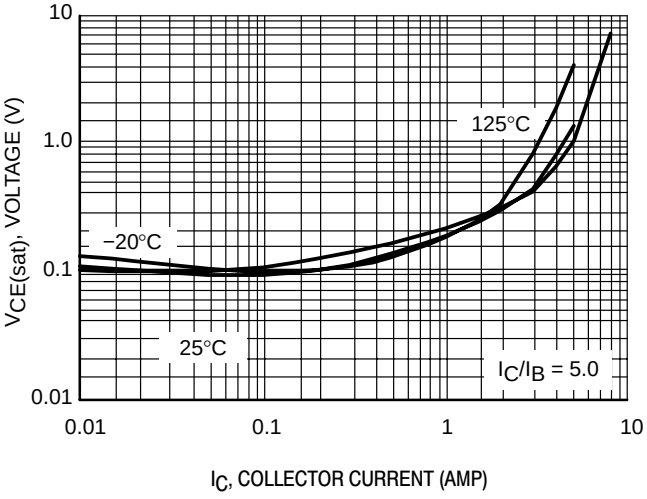


Figure 4. Collector−Emitter Saturation Voltage

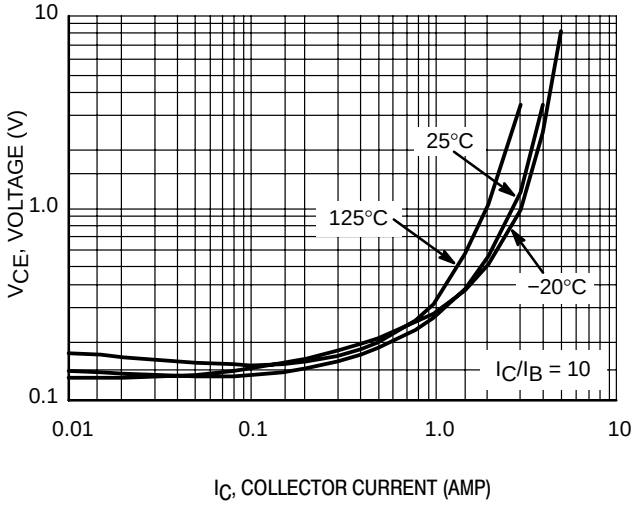


Figure 5. Collector−Emitter Saturation Voltage

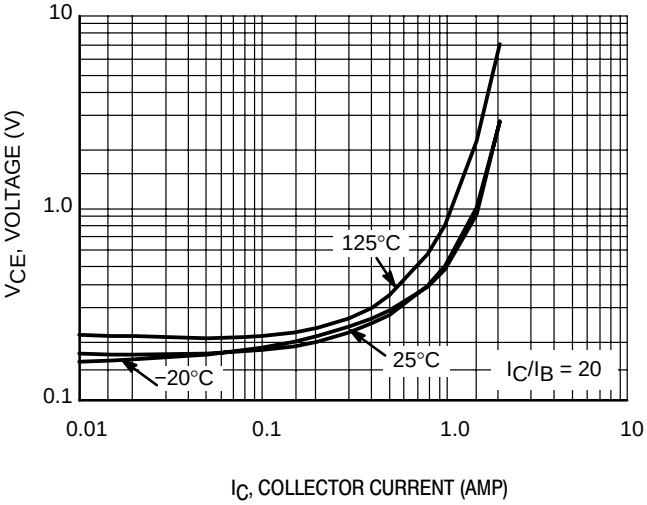


Figure 6. Collector−Emitter Saturation Voltage

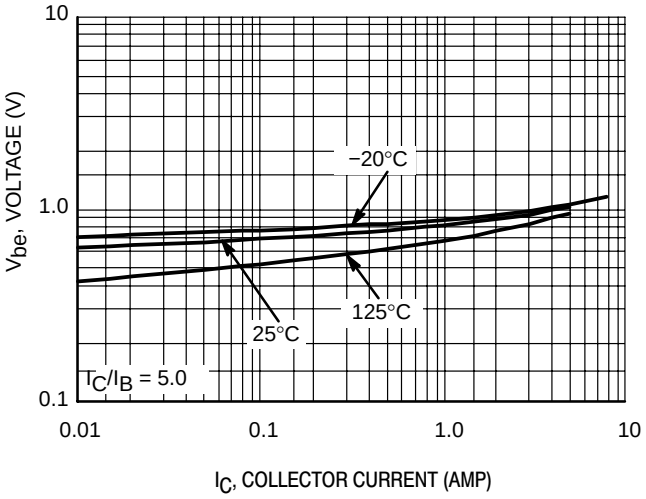


Figure 7. Base−Emitter Saturation Voltage

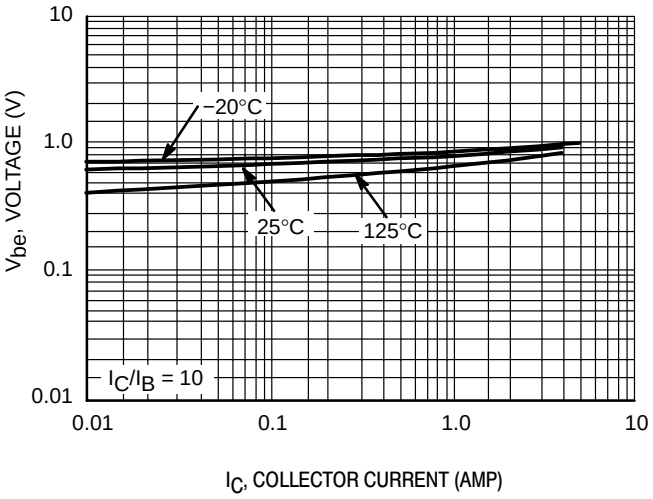


Figure 8. Base−Emitter Saturation Voltage

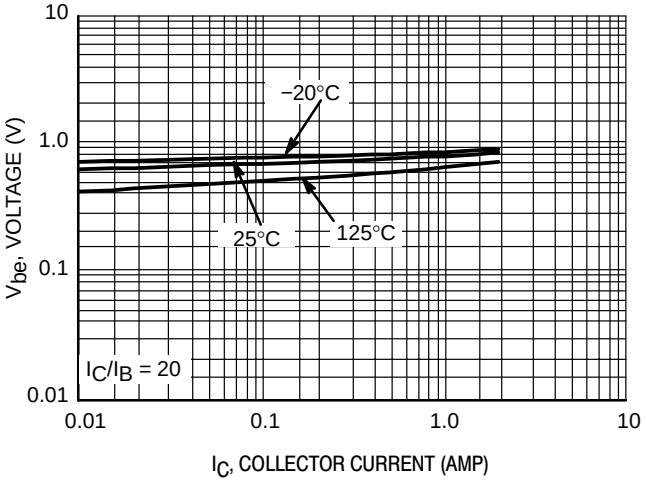


Figure 9. Base−Emitter Saturation Voltage

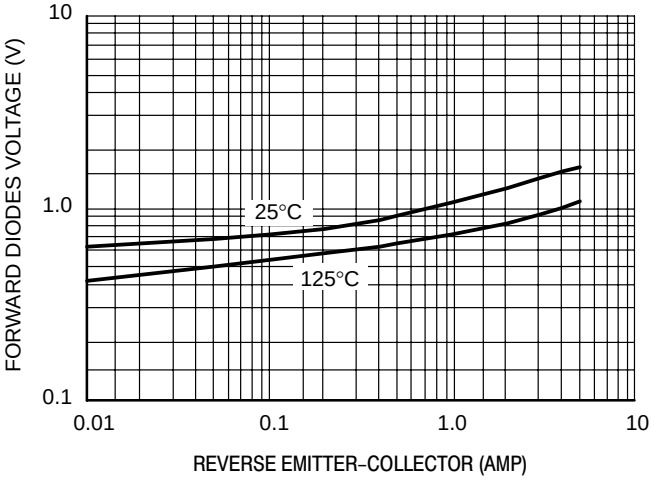


Figure 10. Forward Diode Voltage

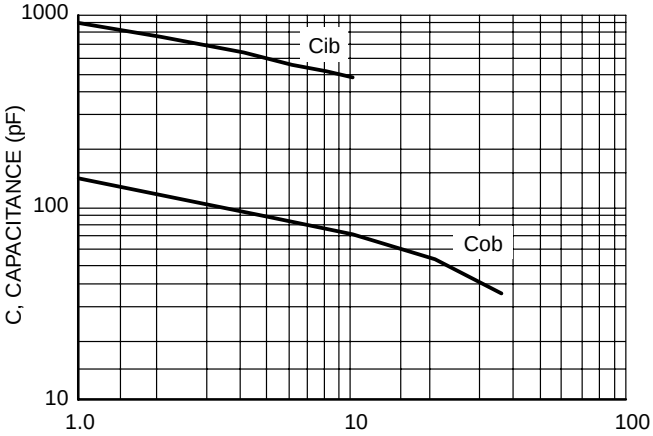


Figure 11. Capacitance

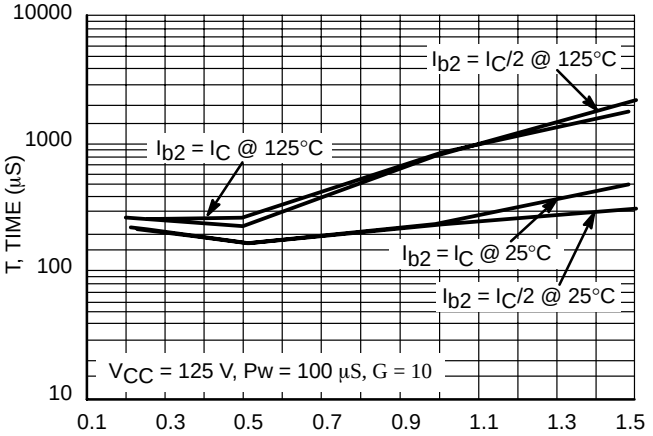


Figure 12. Resistive Switch Time, Storage Time T_{ON}

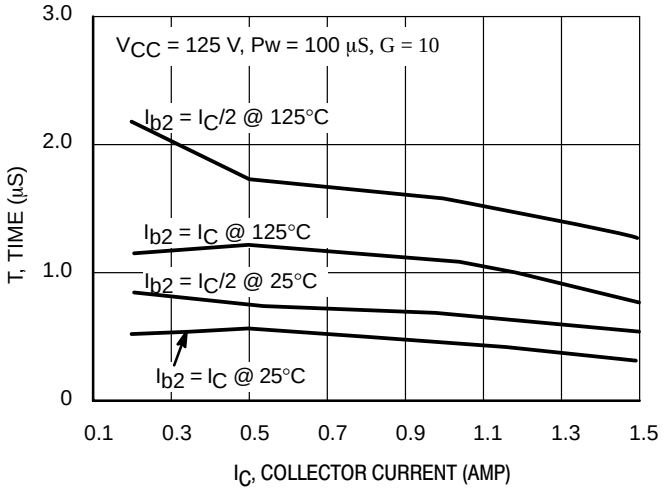


Figure 13. Resistive Switch Time, Storage Time

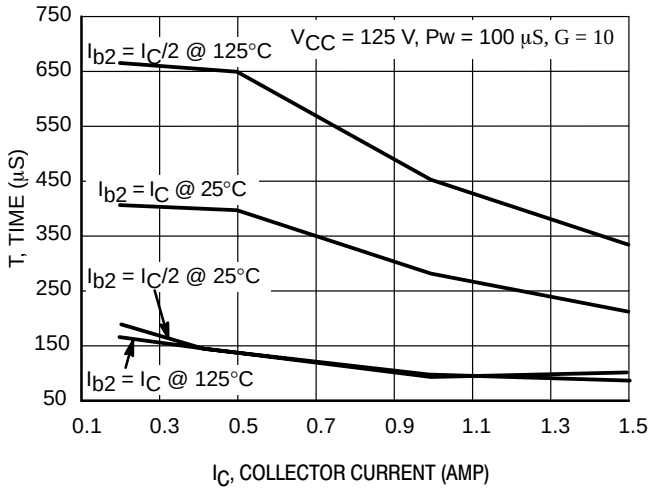


Figure 14. Resistive Switch Time, Fall Time

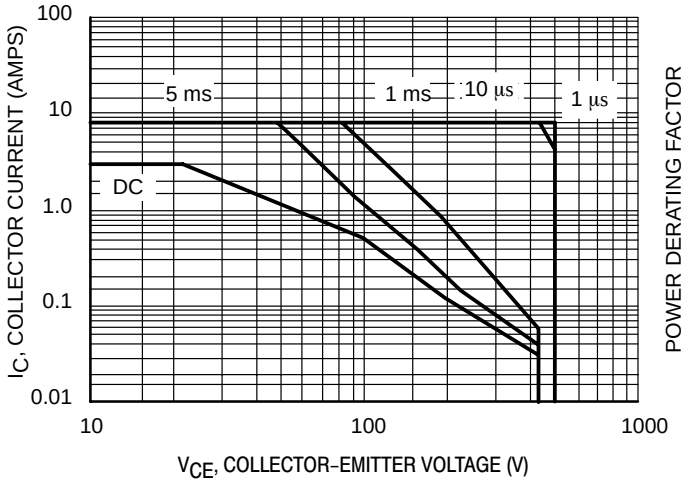


Figure 15.

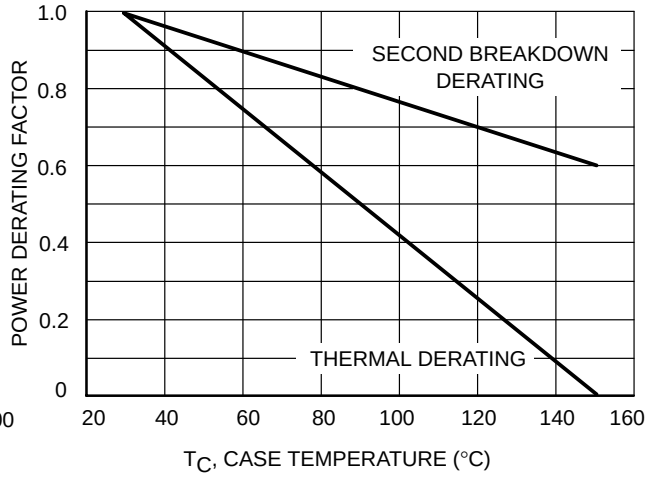
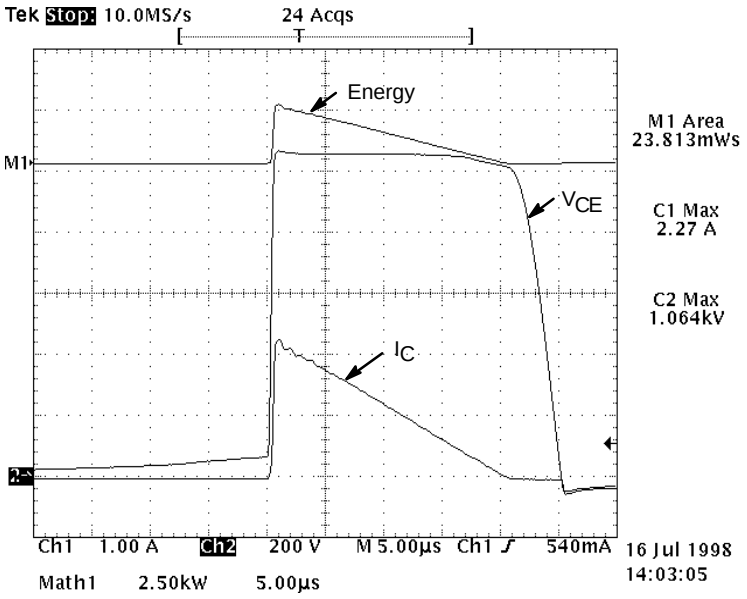


Figure 16. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25°C$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits do not derate like thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{j(pk)}$ may be calculated from the data in Figure 18. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



NPD CHARACTERIZATION LAB

Figure 17. Typical Avalanche Energy Test/Waveforms

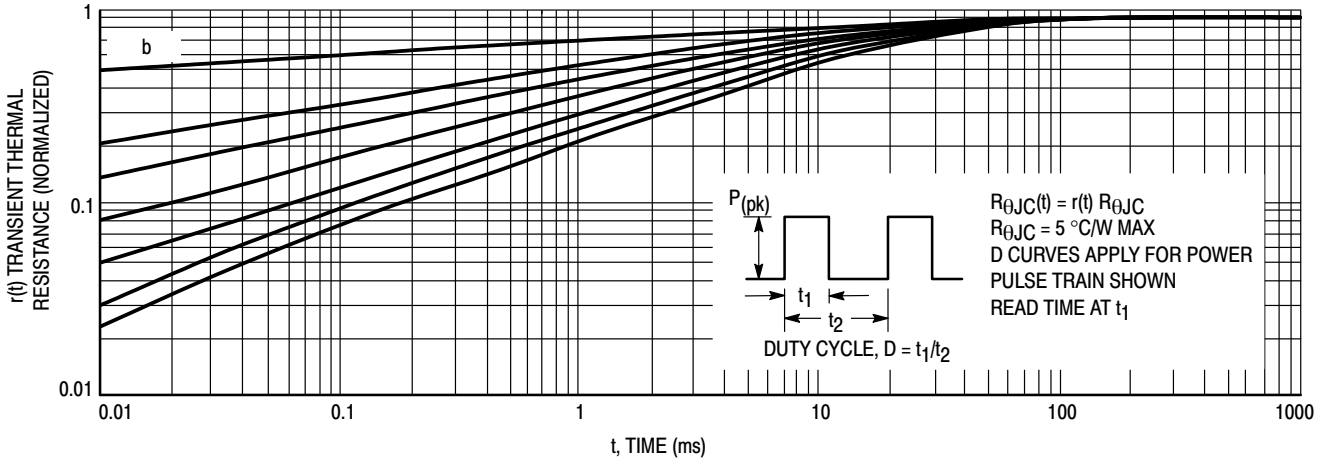


Figure 18. Thermal Response

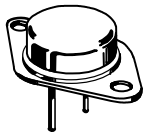
SWITCHMODE™ Series NPN Silicon Power Transistor

BUV21

40 AMPERES NPN SILICON POWER METAL TRANSISTOR 200 VOLTS 250 WATTS

. . . designed for high speed, high current, high power applications.

- High DC current gain:
  h_{FE} min. = 20 at I_C = 12 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$
  max. = 0.6 V at I_C = 8 A
- Very fast switching times:
  TF max. = 0.4 μs at I_C = 25 A



CASE 197A−05 TO−204AE (TO−3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector−Base Voltage	V_{CBO}	250	Vdc
Emitter−Base Voltage	V_{EBO}	7	Vdc
Collector−Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	250	Vdc
Collector−Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector−Current — Continuous — Peak (PW ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base−Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

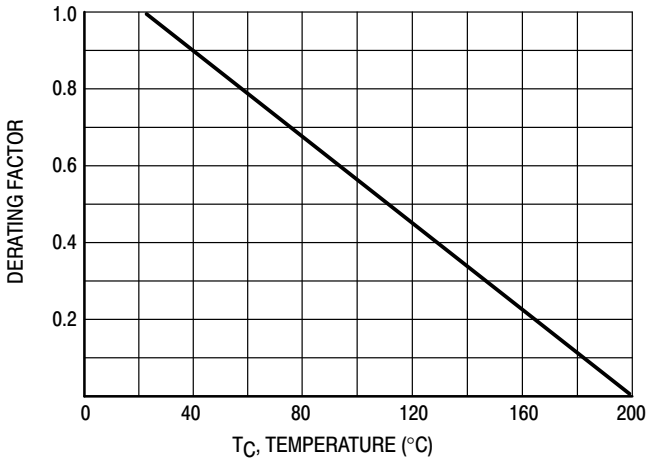


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector−Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 250 V, V_{BE} = −1.5 V) (V_{CE} = 250 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		3.0 12.0	mAdc
Collector−Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		3.0	mAdc
Emitter−Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter−Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 12 A, V_{CE} = 2 V) (I_C = 25 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector−Emitter Saturation Voltage (I_C = 12 A, I_B = 1.2 A) (I_C = 25 A, I_B = 3 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base−Emitter Saturation Voltage (I_C = 25 A, I_B = 3 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Turn-on Time	(I_C = 25 A, I_{B1} = I_{B2} = 3 A, V_{CC} = 100 V, R_C = 4 Ω)	t_{on}		1.0	μs
Storage Time		t_s		1.8	
Fall Time		t_f		0.4	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

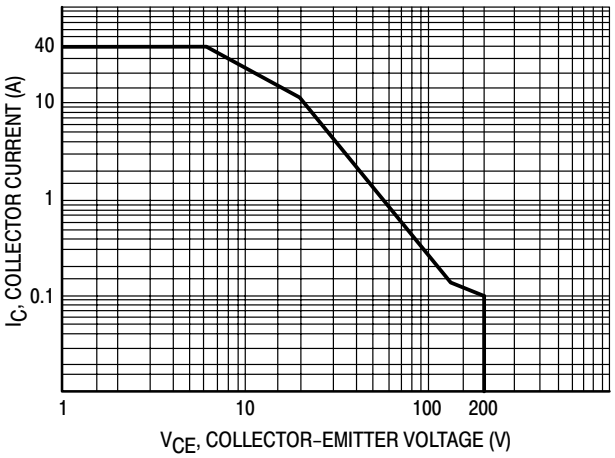


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

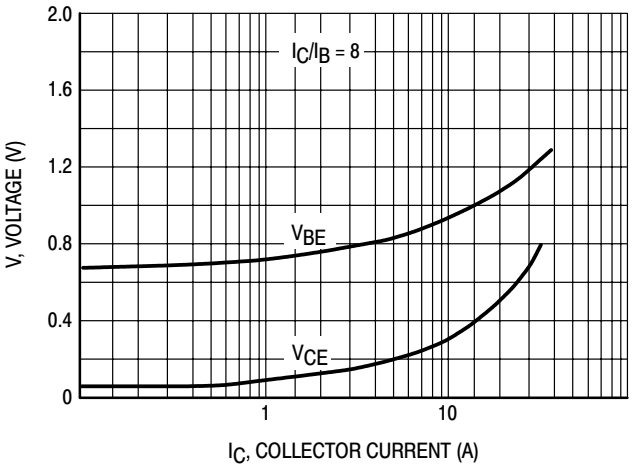


Figure 3. “On” Voltages

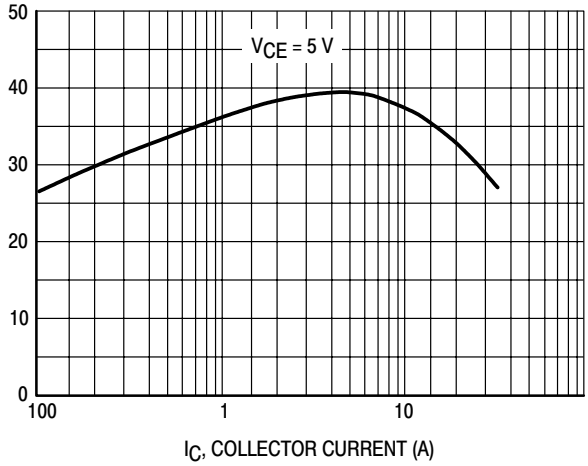


Figure 4. DC Current Gain

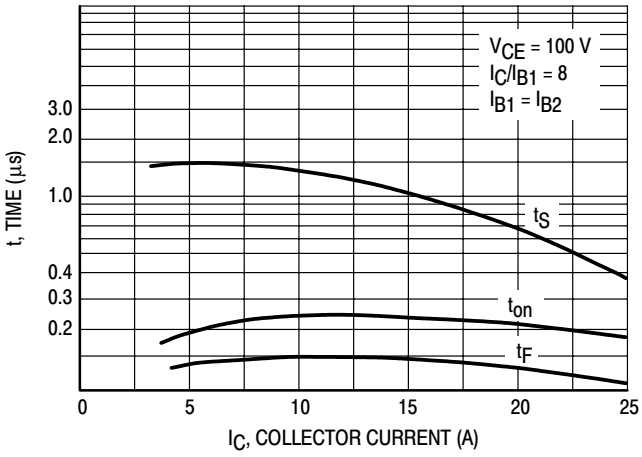
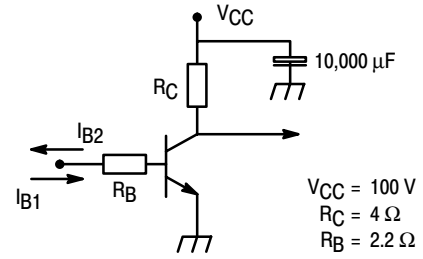


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

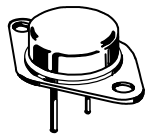
BUV22

SWITCHMODE™ Series NPN Silicon Power Transistor

40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
250 VOLTS
250 WATTS

. . . designed for high current, high speed, high power applications.

- High DC current gain:
  HFE min. = 20 at I_C = 10 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$
  max. = 1.0 V at I_C = 10 A
- Very fast switching times:
  T_F max. = 0.35 μs at I_C = 20 A



CASE 197A−05
TO−204AE
(TO−3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector−Base Voltage	V_{CBO}	300	Vdc
Emitter−Base Voltage	V_{EBO}	7	Vdc
Collector−Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	300	Vdc
Collector−Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	290	Vdc
Collector−Current — Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base−Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

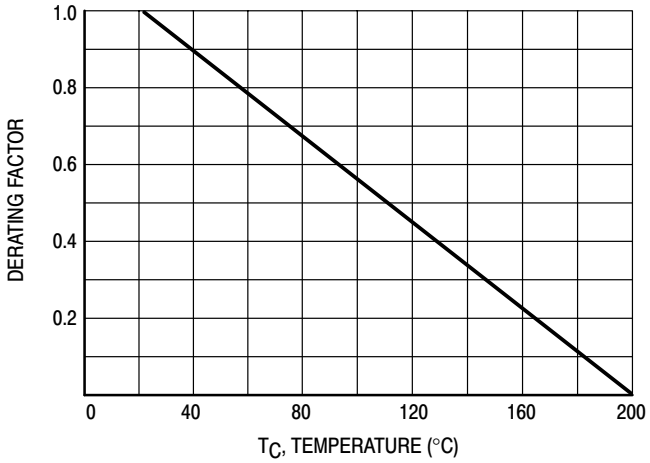


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]					
Collector−Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)		$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 300 V, V_{BE} = −1.5 V) (V_{CE} = 300 V, V_{BE} = −1.5 V, T_C = 125°C)		I_{CEX}		3.0 12.0	mAdc
Collector−Emitter Cutoff Current (V_{CE} = 200 V)		I_{CEO}		3.0	mAdc
Emitter−Base Reverse Voltage (I_E = 50 mA)		V_{EBO}	7		V
Emitter−Cutoff Current (V_{EB} = 5 V)		I_{EBO}		1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)		$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 10 A, V_{CE} = 4 V) (I_C = 20 A, V_{CE} = 4 V)		h_{FE}	20 10	60	
Collector−Emitter Saturation Voltage (I_C = 10 A, I_B = 1 A) (I_C = 20 A, I_B = 2.5 A)		$V_{CE(sat)}$		1.0 1.5	Vdc
Base−Emitter Saturation Voltage (I_C = 40 A, I_B = 4 A)		$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)		f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)					
Turn−on Time	(I_C = 20 A, I_{B1} = I_{B2} = 2.5 A, V_{CC} = 100 V, R_C = 5 Ω)	t_{on}		0.8	μs
Storage Time		t_s		2.0	
Fall Time		t_f		0.35	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

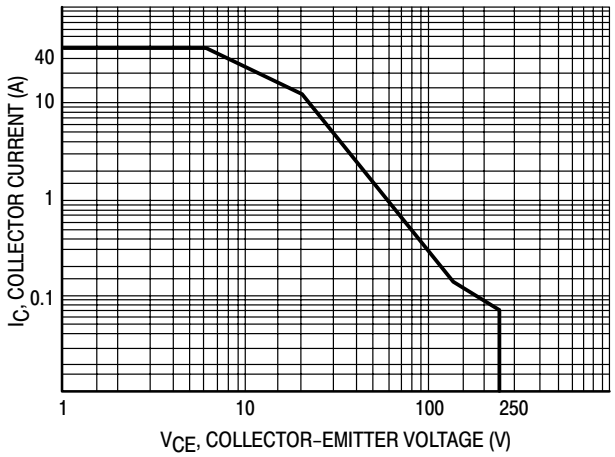


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

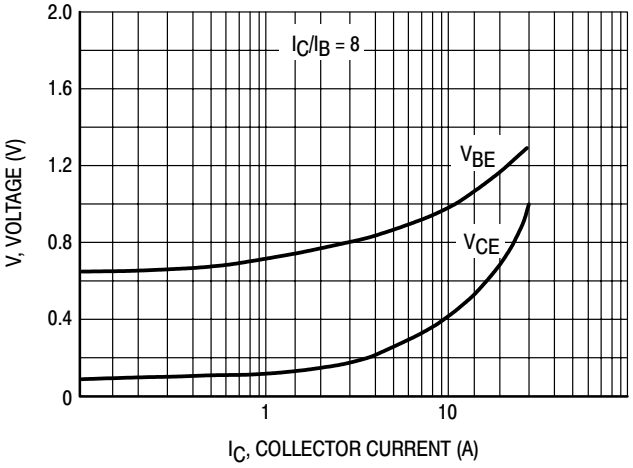


Figure 3. “On” Voltages

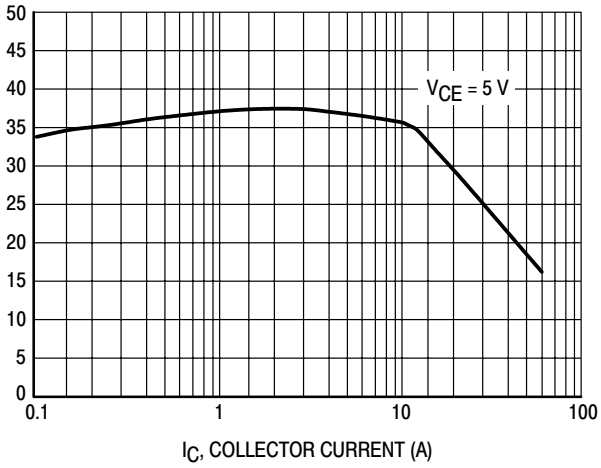


Figure 4. DC Current Gain

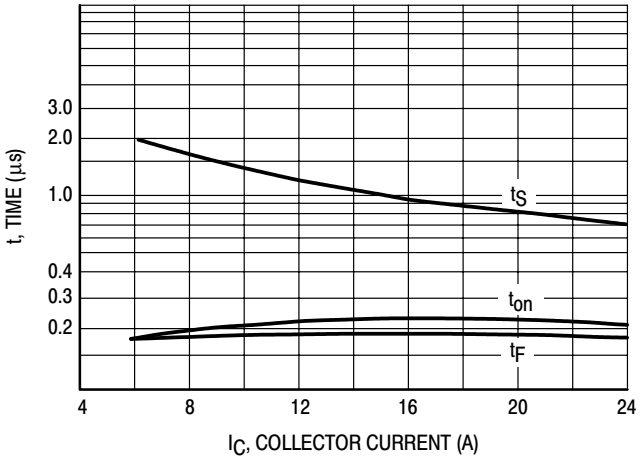
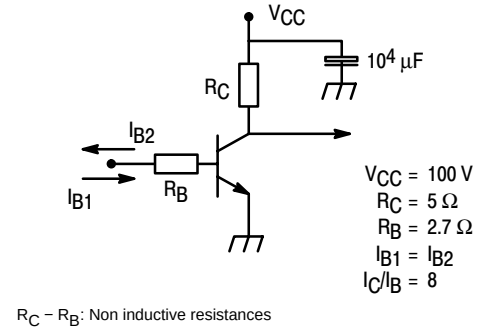


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

BUV26

Switchmode Series NPN Silicon Power Transistor

Designed for high−speed applications such as:

- Switchmode Power Supplies
- High Frequency Converters
- Relay Drivers
- Driver

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	90	Vdc
Collector−Base Voltage	V_{CBO}	180	Vdc
Emitter−Base Voltage	V_{EBO}	7.0	Vdc
Collector Current − Continuous − Peak (pw 10 ms)	I_C I_{CM}	20 30	Adc Apk
Base Current − Continuous	I_B I_{BM}	4.0 6.0	Adc Adc
Total Power Dissipation @ T_C = 25°C Total Power Dissipation @ T_C = 60°C	P_D P_D	85 65	Watts Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

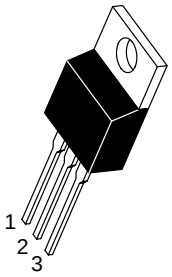
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.76	°C/W

ON Semiconductor®

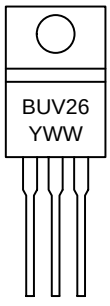
http://onsemi.com

12 AMPERES
NPN SILICON
POWER TRANSISTORS
90 VOLTS
85 WATTS



TO−220
CASE 221A
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
TBD	TO−220	50 Units/Rail

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)		$V_{CEO(sus)}$	90	−	Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 180 V, V_{BE} = −1.5 V, T_C = 125°C)		I_{CEX}	−	1.0	mAdc
Emitter Base Reverse Voltage (I_E = 50 mA)		V_{EBO}	7.0	30	V
Emitter Cutoff Current (V_{EB} = 5.0 V)		I_{EBO}	−	1.0	mAdc
Collector Cutoff Current (V_{CE} = 180 V, R_{BE} = 50 Ω, T_C = 125°C)		I_{CER}	−	3.0	mAdc
ON CHARACTERISTICS					
Collector−Emitter Saturation Voltage (I_C = 6.0 A, I_B = 0.4 A) (I_C = 12 A, I_B = 1.2 A)		$V_{CE(sat)}$	− −	0.6 1.5	Vdc
Base−Emitter Saturation Voltage (I_C = 12 A, I_B = 1.2 A)		$V_{BE(sat)}$	−	2.0	Vdc
SWITCHING CHARACTERISTICS (Resistive Load)					
Turn On Time	I_C = 12 A, I_B = 1.2 A	t_{on}	−	0.6	μs
Storage Time	V_{CC} = 50 V, V_{BE} = 6.0 V	t_s	−	1.0	
Fall Time	RB2 = 2.5 Ω	t_f	−	0.15	
SWITCHING CHARACTERISTICS (Inductive Load)					
Storage Time	V_{CC} = 50 V, I_C = 12 A $I_{B(end)}$ = 1.2 A, V_B = 5.0 V L_B = 0.5 pH, T_J = 125°C	T_s	−	2.0	μs
Fall Time		T_f	−	.15	

2. Pulse Test: Pulse width ≤ 300 μs; Duty cycle ≤ 2%.

BUV27

NPN Silicon Power Transistor

Designed for use in switching regulators and motor control.

Features

- Low Collection Emitter Saturation Voltage
- Fast Switching Speed

ON Semiconductor®

http://onsemi.com

POWER TRANSISTOR
12 AMPERES
120 VOLTS
70 WATTS

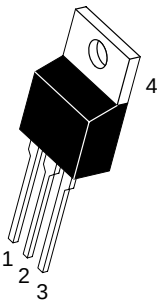
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	120	Vdc
Collector−Emitter Breakdown Voltage	V_{CBO}	240	Vdc
Emitter−Base Voltage	V_{EBO}	7.0	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	12 20	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	70 0.56	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	− 65 to 150	°C

THERMAL CHARACTERISTICS

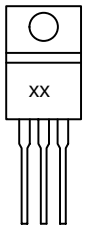
Rating	Symbol	Max	Unit
Thermal Resistance − Junction to Case − Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.78 62.5	°C/W

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



TO−220AB
CASE 221A
STYLE 1

MARKING DIAGRAM



xx = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
BUV27	TO−220AB	50 per Rail
BUV27	TO−220AB	3000 per Carton

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{CER}	Collector Cut−off Current (R_{BE} = 50 Ω)	V_{CE} = 240 V, T_C = 125°C			3.0	mA
I_{CEX}	Collector Cut−off Current	V_{CE} = 240 V, V_{BE} = −1.5 V, T_C = 125°C			1.0	mA
I_{EBO}	Emitter Cut−off Current (I_C = 0)	V_{BE} = 5 V			1.0	mA
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage	I_C = 0.2 A, L = 25 mH	120			V
V_{EBO}	Emitter−Base Voltage (I_C = 0)	I_E = 50 mA	7.0		30	V
$V_{CE(sat)}$ (Note 2)	Collector−Emitter Saturation Voltage	I_C = 4 A, I_B = 0.4 A I_C = 8 A, I_B = 0.8 A			0.7 1.5	V
$V_{BE(sat)}$ (Note 2)	Base−Emitter Saturation Voltage	I_C = 8 A, I_B = 0.8 A			2.0	V
Resistive Load						
t_{on} t_s t_f	Turn−on Time Storage Time Fall Time	V_{CC} = 90 V, I_C = 8 A V_{BE} = −6 V, I_{B1} = 0.8 A R_{BB} = 3.75 Ω		0.4 0.5 0.12	0.8 1.2 0.25	ms μs μs
Inductive Load						
t_s t_f	Storage Time Fall Time	V_{CC} = 90 V, I_C = 8 A I_{B1} = 0.8 A, V_{BE} = −5 V L_B = 1 μH		0.6 0.04		μs
t_s t_f	Storage Time Fall Time	V_{CC} = 90 V, I_C = 8 A I_{B1} = 0.8 A, V_{BE} = −5 V L_B = 1 μH, T_J = 125°C			2.0 0.15	

2. Pulsed: Pulse Duration = 300 μs, Duty Cycle = 2%

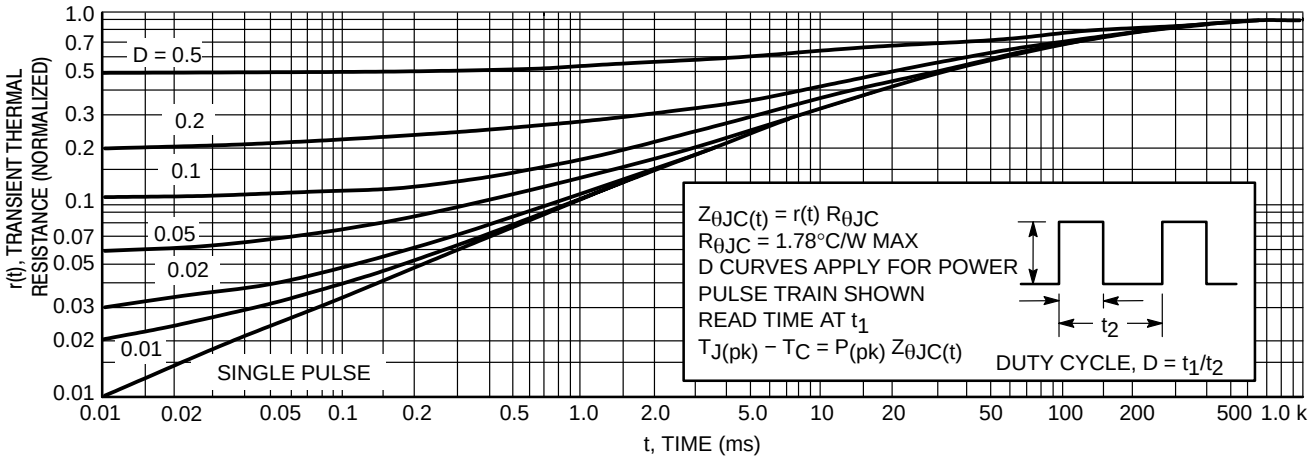


Figure 7. Thermal Response

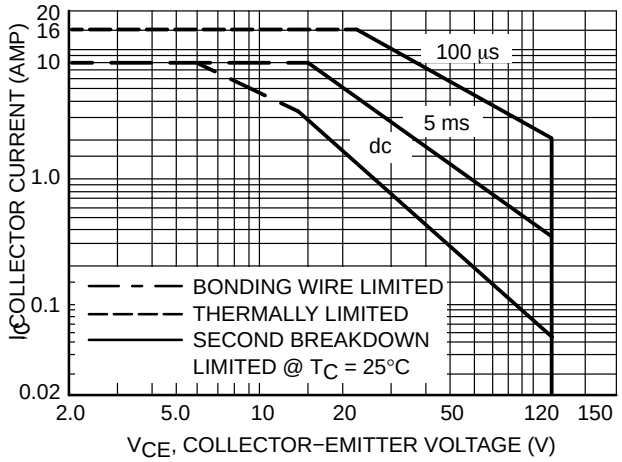


Figure 8. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 8 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

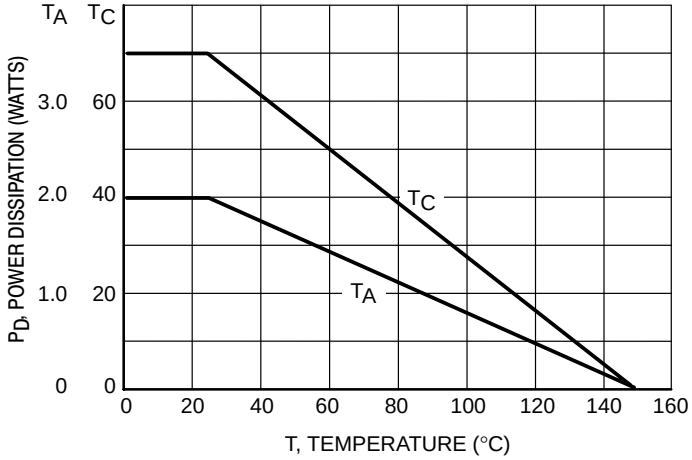


Figure 9. Power Derating

BUX85

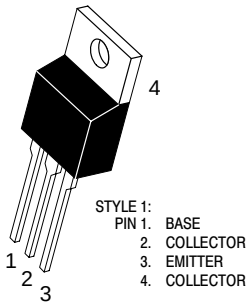
SWITCHMODE™ NPN Silicon Power Transistors

The BUX85 is designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

Specifications Features:

- $V_{CEO(sus)}$ 450 V
- $V_{CES(sus)}$ 1000 V
- Fall time = 0.3 μs (typ) at I_C = 1.0 A
- $V_{CE(sat)}$ = 1.0 V (max) at I_C = 1.0 A, I_B = 0.2 A

2 AMPERES
POWER TRANSISTOR
NPN SILICON
450 VOLTS
50 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	BUX84	BUX85	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector−Emitter Voltage	V_{CES}	800	1000	Vdc
Emitter Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous — Peak (1)	 I_C I_{CM}	 2 3.0		Adc
Base Current — Continuous — Peak (1)	 I_B I_{BM}	 0.75 1.0		Adc
Reverse Base Current — Peak	I_{BM}	1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 400		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, (L = 25 mH) See fig. 1		$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CES} = Rated Value) (V_{CES} = Rated Value, T_C = 125°C)		I_{CES}	 — —	 — —	 0.2 1.5	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)		I_{EBO}	—	—	1	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5 V)		h_{FE}	30	50	—	—
Collector−Emitter Saturation Voltage (I_C = 0.3 Adc, I_B = 30 mAdc) (I_C = 1 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	 — —	 — —	 0.8 1	Vdc
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	—	—	1.1	Vdc
DYNAMIC CHARACTERISTICS						
Current−Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 1 0 Vdc, f = 1 MHz)		f_T	4	—	—	MHz
SWITCHING CHARACTERISTICS						
Turn−on Time	V_{CC} = 250 Vdc, I_C = 1 A I_{B1} = 0.2 A, I_{B2} = 0.4 A See fig. 2	t_{on}	—	0.3	0.5	μs
Storage Time		t_s	—	2	3.5	μs
Fall Time		t_f	—	0.3	—	μs
Fall Time	Same above cond. at T_C = 95°C	t_f	—	—	1.4	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦2%.

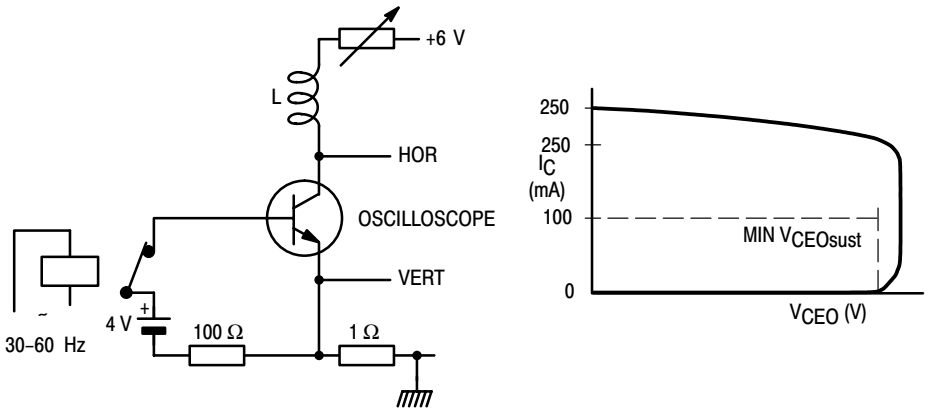
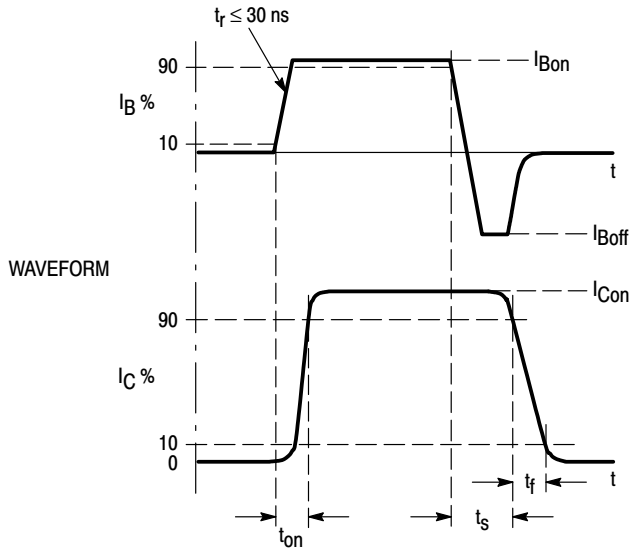


Figure 1. Test Circuit for $V_{CEOsust}$



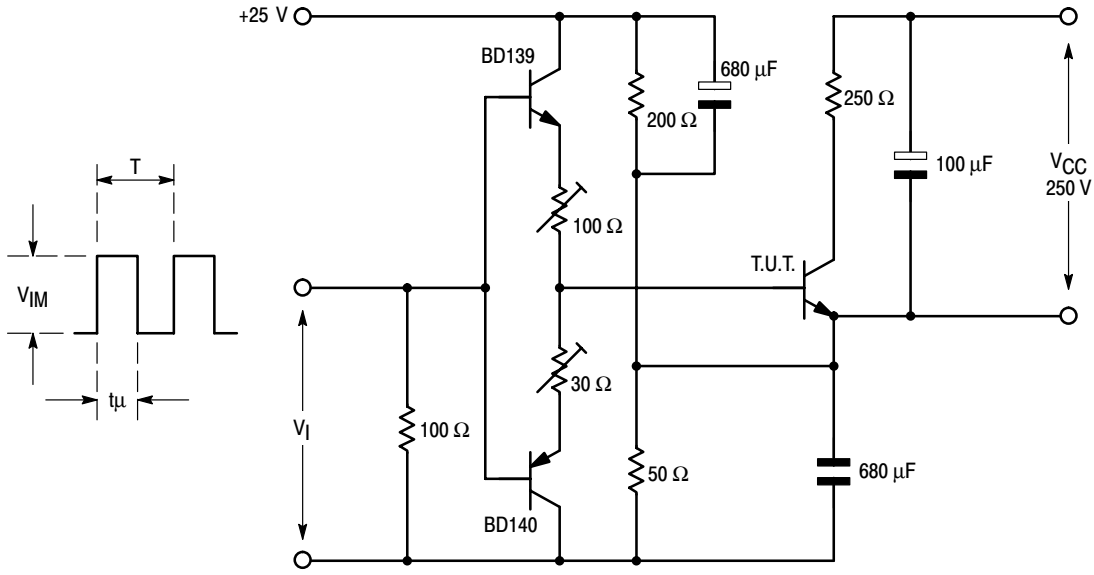


Figure 2. Switching Times/Test Circuit

D44H Series (NPN), D45H Series (PNP)

Preferred Devices

Complementary Silicon Power Transistors

These series of plastic, silicon NPN and PNP power transistors can be used as general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

Features

- Pb−Free Package is Available
- Low Collector−Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage D44H8, D45H8 D44H11, D45H11	V_{CEO}	 60 80	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	 10 20	Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	 50 2.0	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

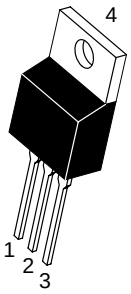
1. Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

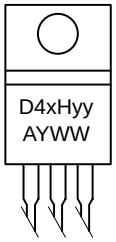
http://onsemi.com

10 A COMPLEMENTARY SILICON POWER TRANSISTORS 60, 80 V



TO−220AB
CASE 221A
STYLE 1

MARKING DIAGRAM



x = 4 or 5
yy = 8 or 11
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
D44H8	TO−220	50 Units/Rail
D44H11	TO−220	50 Units/Rail
D45H8	TO−220	50 Units/Rail
D45H8G	TO−220 (Pb−Free)	50 Units/Rail
D45H11	TO−220	50 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain		h_{FE}			−
(V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)					
	D44H8, 11		20	−	
	D45H8, 11		40	−	
(V_{CE} = 1.0 Vdc, I_C = 4.0 Adc)	D44H8, 11		20	−	
	D45H8, 11		40	−	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	−	−	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)		I_{EBO}	−	−	100	μA
ON CHARACTERISTICS						
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44H/D45H8, 11		−	−	1.0	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D44H		−	−	1.0	
Base−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	−	−	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Collector Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, f_{test} = 1.0 MHz)	D44H Series		−	130	−	
	D45H Series		−	230	−	
Gain Bandwidth Product		f_T				MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	D44H Series		−	50	−	
	D45H Series		−	40	−	
SWITCHING TIMES						
Delay and Rise Times		$t_d + t_r$				ns
(I_C = 5.0 Adc, I_{B1} = 0.5 Adc)	D44H Series		−	300	−	
	D45H Series		−	135	−	
Storage Time		t_s				ns
(I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	D44H Series		−	500	−	
	D45H Series		−	500	−	
Fall Time		t_f				ns
(I_C = 5.0 Adc, I_{B1} = 102 = 0.5 Adc)	D44H Series		−	140	−	
	D45H Series		−	100	−	

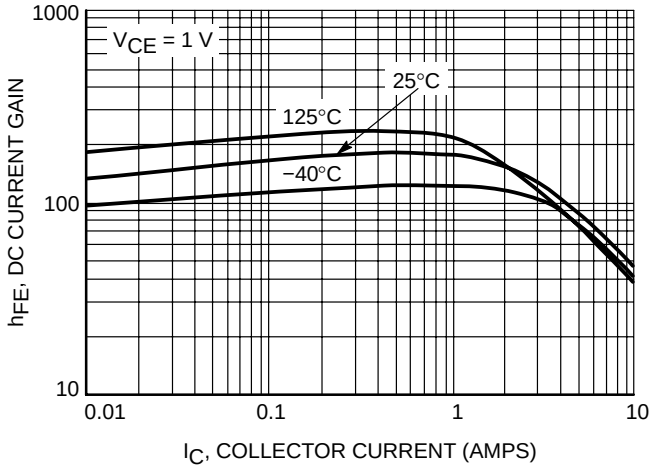


Figure 1. D44H11 DC Current Gain

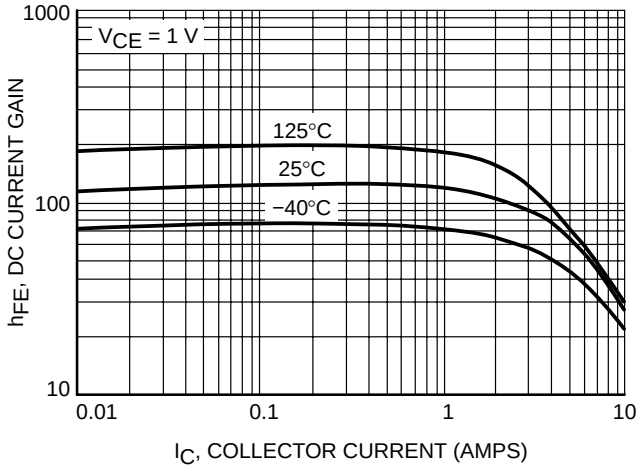


Figure 2. D45H11 DC Current Gain

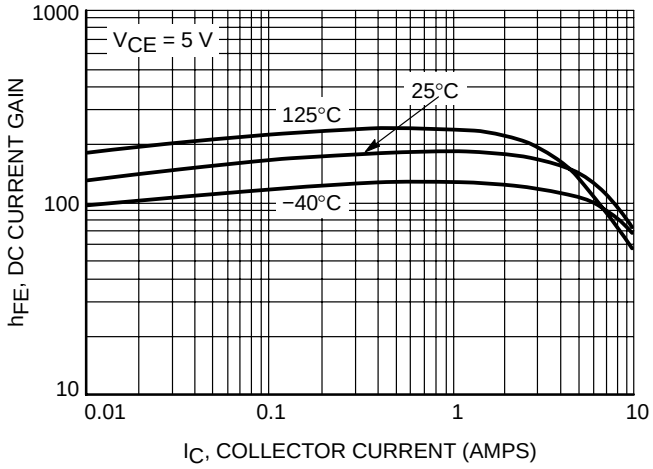


Figure 3. D44H11 DC Current Gain

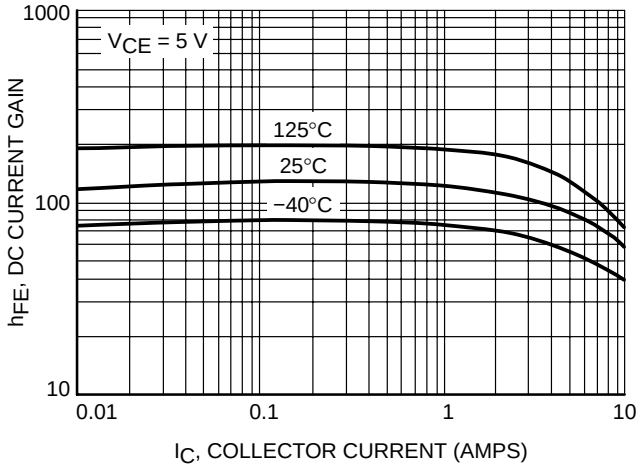


Figure 4. D45H11 DC Current Gain

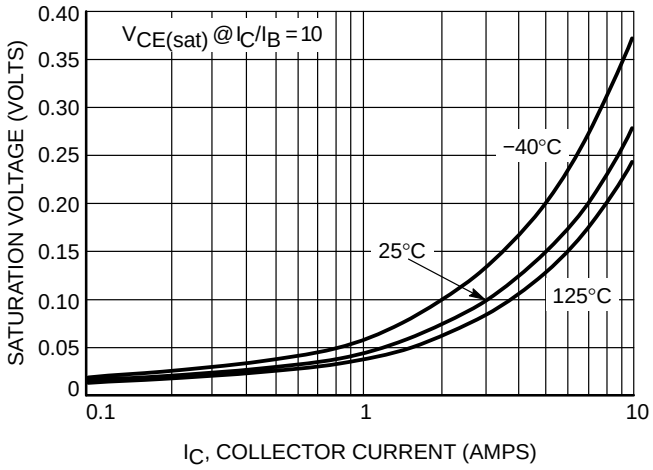


Figure 5. D44H11 ON−Voltage

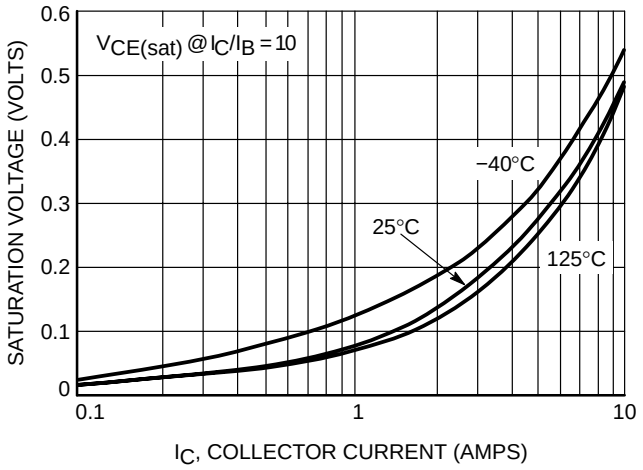


Figure 6. D45H11 ON−Voltage

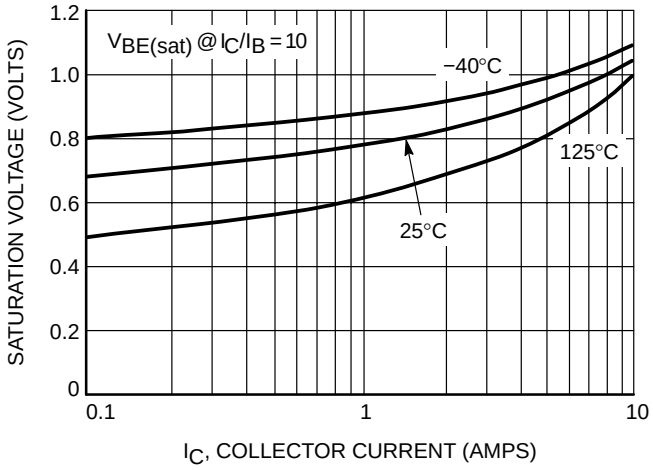


Figure 7. D44H11 ON−Voltage

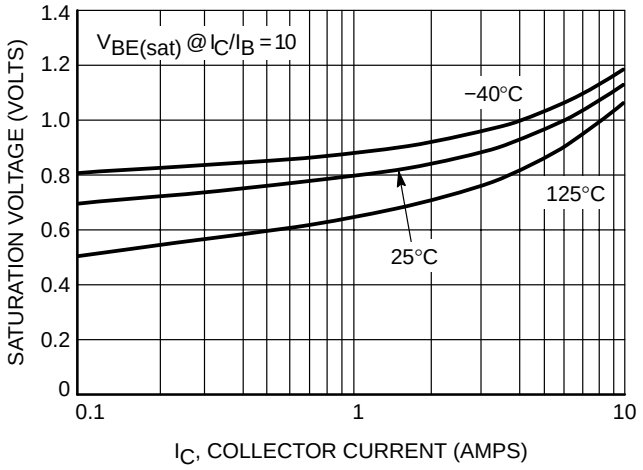


Figure 8. D45H11 ON−Voltage

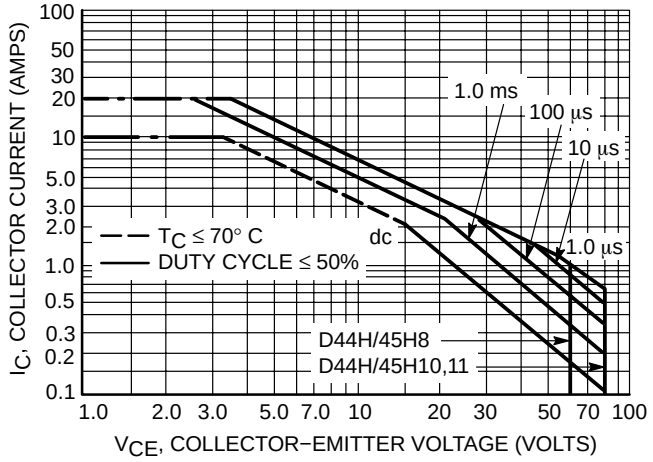


Figure 9. Maximum Rated Forward Bias Safe Operating Area

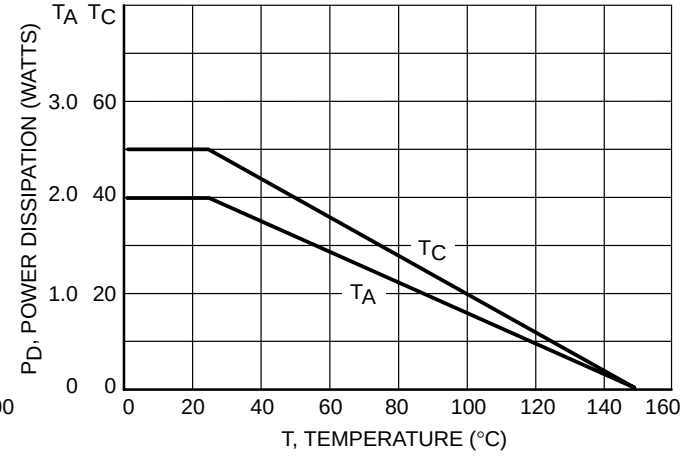


Figure 10. Power Derating

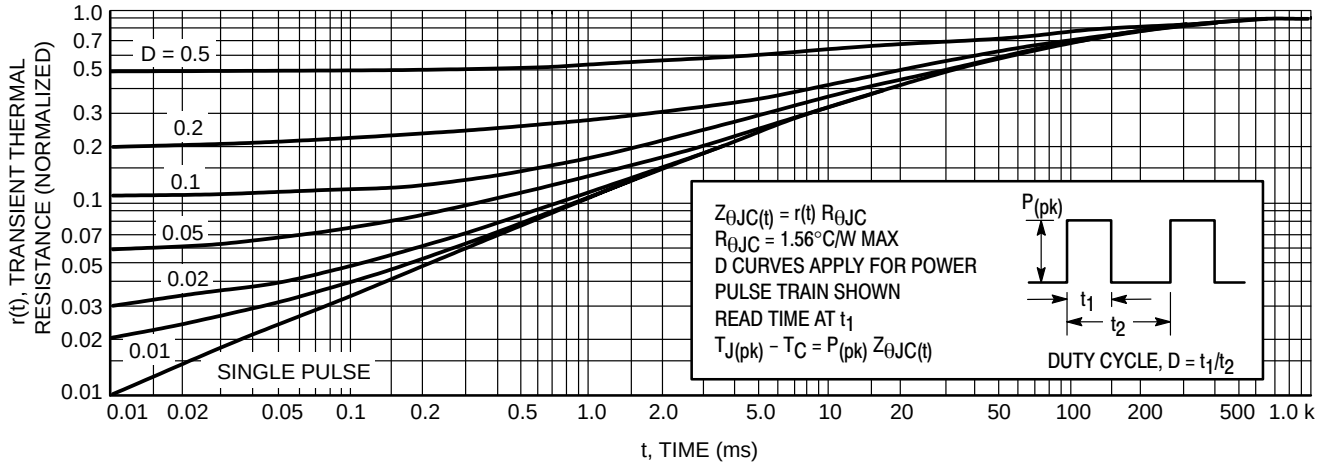


Figure 11. Thermal Response

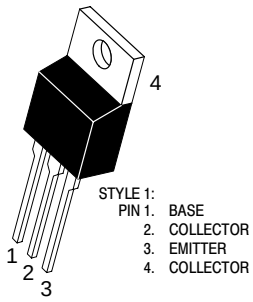
Complementary Silicon Power Transistors

NPN
D44VH
PNP
D45VH

These complementary silicon power transistors are designed for high−speed switching applications, such as switching regulators and high frequency inverters. The devices are also well−suited for drivers for high power switching circuits.

- Fast Switching —
  t_f = 90 ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 VOLTS
83 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Emitter Voltage	V_{CEV}	100	Vdc
Emitter Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(2) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

NOTE: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.

April, 2002 − Rev. 3
Publication Order Number:
D44VH/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (2) (I_C = 25 mAdc, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector−Emitter Cutoff Current		I_{CEV}				μAdc
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc)			—	—	10	
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)			—	—	100	
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)			35	—	—	
(I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)			20	—	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44VH10		—	—	0.4	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D45VH10		—	—	1.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)	D44VH10		—	—	0.8	
	D45VH10		—	—	1.5	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44VH10		—	—	1.2	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D45VH10		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	D44VH10		—	—	1.1	
(I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C)	D45VH10		—	—	1.5	
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	—	50	—	MHz
Output Capacitance		C_{ob}				pF
(V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz)	D44VH10		—	120	—	
	D45VH10		—	275	—	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	—	—	50	ns
Rise Time		t_r	—	—	250	
Storage Time		t_s	—	—	700	
Fall Time		t_f	—	—	90	

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

D45C12 (PNP), D44C12 (NPN)

Complementary Silicon Power Transistor

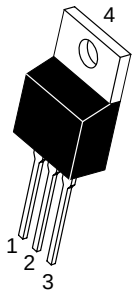
. . . for general purpose driver or medium power output stages in CW or switching applications.

- Low Collector−Emitter Saturation Voltage — 0.5 V (Max)
- High f_t for Good Frequency Response
- Low Leakage Current

ON Semiconductor®

http://onsemi.com

4.0 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 80 VOLTS



TO−220AB
CASE 221A
STYLE 1

MAXIMUM RATINGS

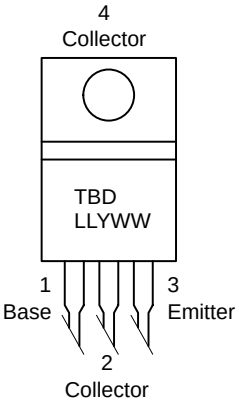
Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Emitter Voltage	VCES	90	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C	4.0 6.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	30 1.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

MARKING DIAGRAM & PIN ASSIGNMENT



TBD = Device Code
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
D45C12	TO−220AB	50 Units/Rail
D44C12	TO−220AB	50 Units/Rail

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 0.2 Adc) (V_{CE} = 1.0 Vdc, I_C = 1.0 Adc) (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	h_{FE}	 40 20 20	 120 — —	—

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	0.1	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	10	μA
ON CHARACTERISTICS					
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	0.135	0.5	Vdc
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	—	0.85	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{cb}	—	125	—	pF
Gain Bandwidth Product (I_C = 20 mA, V_{CE} = 4.0 Vdc, f = 20 MHz)	f_T	—	40	—	MHz
SWITCHING TIMES					
Delay and Rise Times (I_C = 1.0 Adc, I_{B1} = 0.1 Adc)	$t_d + t_r$	—	50	75	ns
Storage Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_s	—	350	550	ns
Fall Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_f	—	50	75	ns

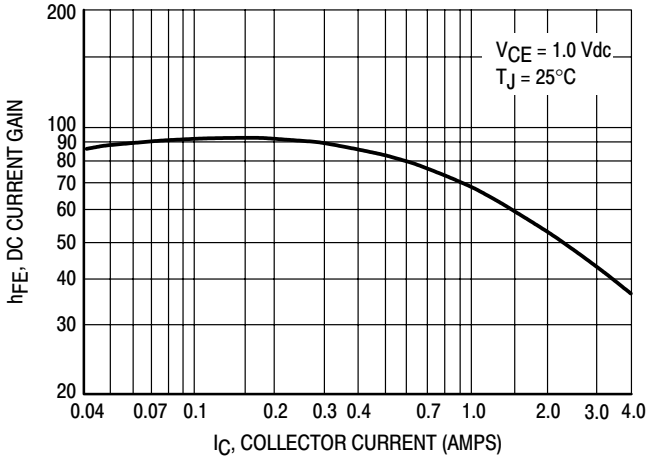


Figure 12. Typical DC Current Gain

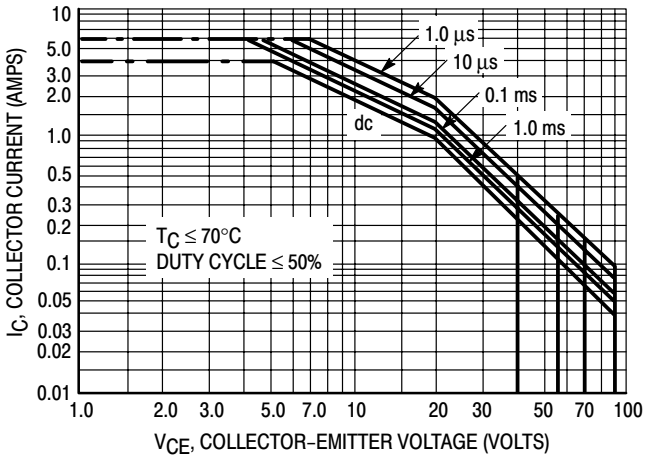


Figure 13. Maximum Rated Forward Bias Safe Operating Area

High-Current Complementary Silicon Transistors

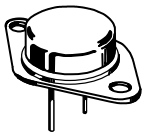
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 1000 (Min) @ I_C − 20 Adc
- Monolithic Construction with Built−in Base Emitter Shunt Resistor
- Junction Temperature to +200°C

PNP
MJ11015
NPN
MJ11012
MJ11016*

*ON Semiconductor Preferred Device

30 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60−120 VOLTS
200 WATTS



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS

Rating	Symbol	MJ11012	MJ11015 MJ11016	Unit
Collector−Emitter Voltage	V_{CEO}	60	120	Vdc
Collector−Base Voltage	V_{CB}	60	120	Vdc
Emitter−Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	30		Adc
Base Current	I_B	1		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 1.15		Watts W/°C
Operating Storage Junction Temperature Range	T_J, T_{stg}	−55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	°C

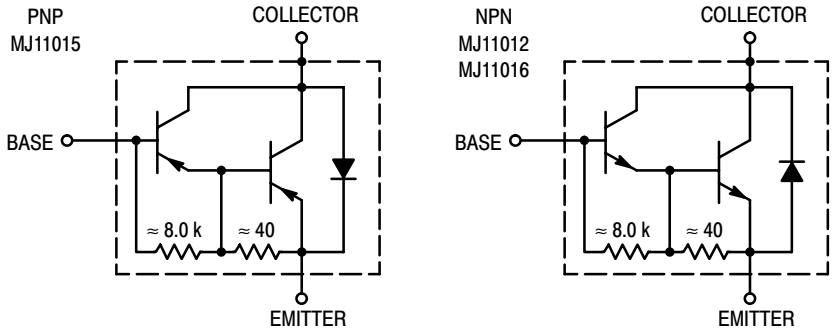


Figure 1. Darlington Circuit Schematic

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 − Rev. 4
Publication Order Number:
MJ11012/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage(1)		$V_{(BR)CEO}$			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ11012		60	—	
	MJ11015, MJ11016		120	—	
Collector−Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm)	MJ11012		—	1	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm)	MJ11015, MJ11016		—	1	
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11012		—	5	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11015, MJ11016		—	5	
Emitter Cutoff Current		I_{EBO}	—	5	mAdc
(V_{BE} = 5 Vdc, I_C = 0)					
Collector−Emitter Leakage Current		I_{CEO}	—	1	mAdc
(V_{CE} = 50 Vdc, I_B = 0)					
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			—
(I_C = 20 Adc,V_{CE} = 5 Vdc)			1000	—	
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 200 mAdc)			—	3	
(I_C = 30 Adc, I_B = 300 mAdc)			—	4	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 A, I_B = 200 mAdc)			—	3.5	
(I_C = 30 A, I_B = 300 mAdc)			—	5	
DYNAMIC CHARACTERISTICS					
Current−Gain Bandwidth Product		h_{fe}	4	—	MHz
(I_C = 10 A, V_{CE} = 3 Vdc, f = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

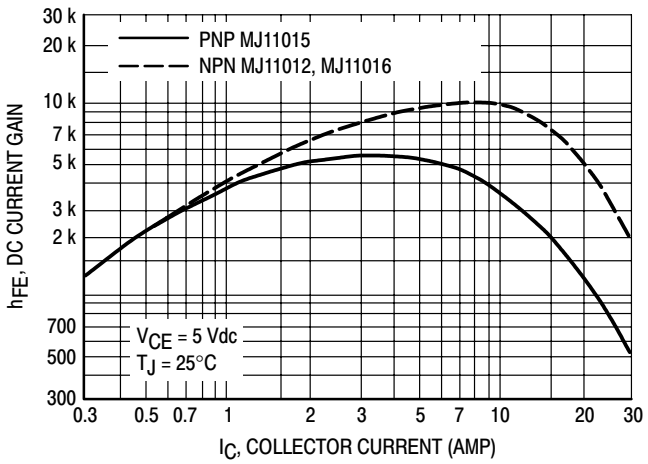


Figure 2. DC Current Gain (1)

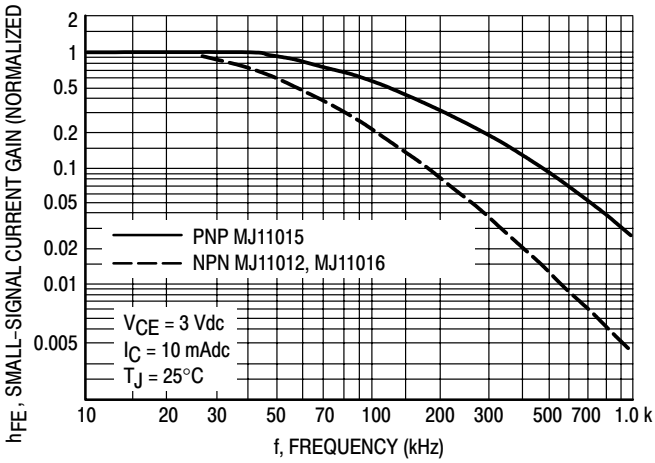


Figure 3. Small−Signal Current Gain

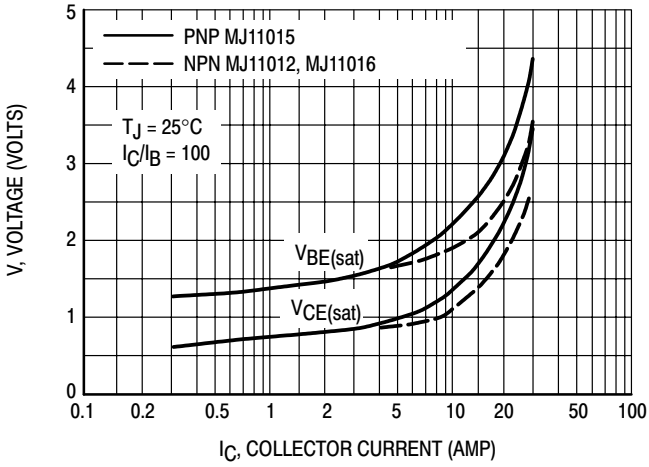


Figure 4. “On” Voltages (1)

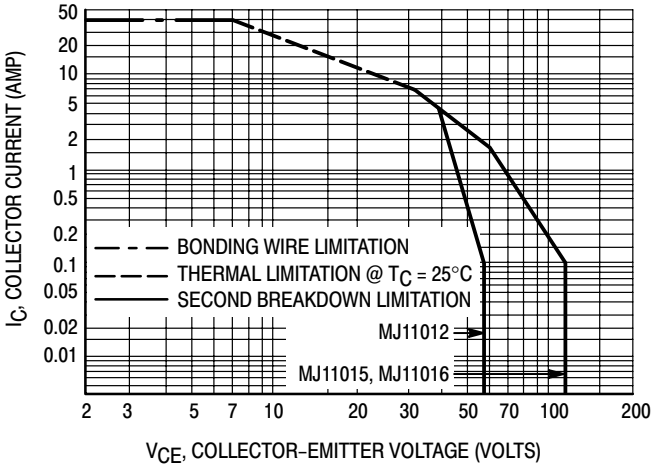


Figure 5. Active Region DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

(PNP) MJ11021
(NPN) MJ11022

Complementary Darlington Silicon Power Transistors

. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc −
  h_{FE} = 400 Min (All Types)
- Collector−Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 250 Vdc (Min) − MJ11022, 21
- Low Collector−Emitter Saturation
  $V_{CE(sat)}$ = 1.0 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- 100% SOA Tested @
  V_{CE} = 44 V
  I_C = 4.0 A
  t = 250 ms

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	250	Vdc
Emitter−Base Voltage	V_{EBO}	50	Vdc
Collector Current − Continuous − Peak (Note 2)	I_C	15 30	Adc
Base Current	I_B	0.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	175 1.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +175 − 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.86	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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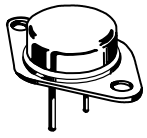
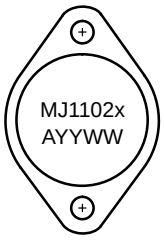
15 AMPERE COMPLEMENTARY DARLINGTON POWER TRANSISTORS 250 VOLTS 175 WATTS



TO−204 (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM



x = 1 or 2
A = Location Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJ11021	TO−204	100 Units/Tray
MJ11022	TO−204	100 Units/Tray

Publication Order Number:

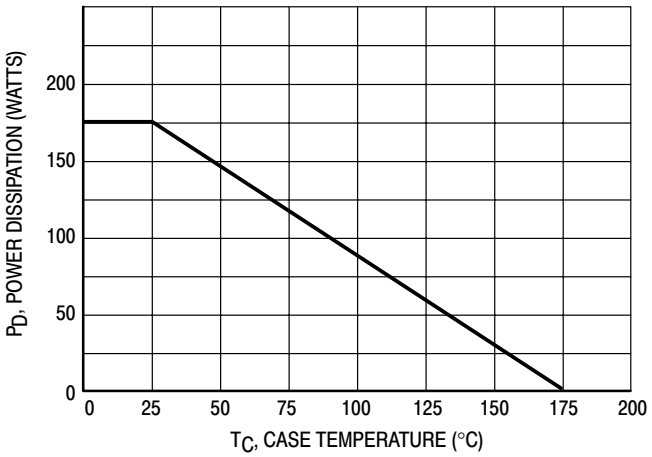


Figure 1. Power Derating

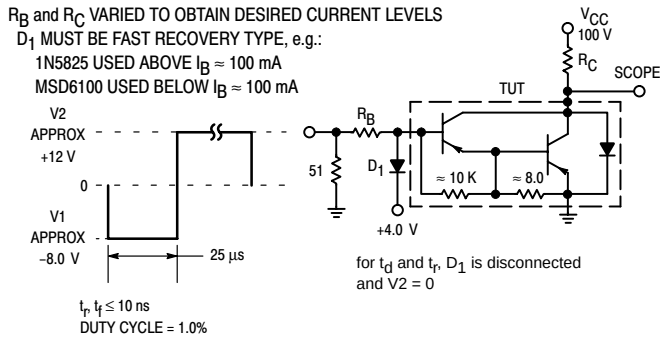
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 0.1 Adc, I_B = 0) MJ11021, MJ11022	$V_{CEO(sus)}$	 250	 —	Vdc
Collector Cutoff Current (V_{CE} = 125, I_B = 0) MJ11021, MJ11022	I_{CEO}	 —	 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)	I_{CEV}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 400 100	 15,000 —	—
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)	$V_{CE(sat)}$	 — —	 2.0 3.4	Vdc
Base−Emitter On Voltage I_C = 10 A, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
Base−Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)	$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$[h_{fe}]$	3.0	—	Mhz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJ11022 MJ11021	C_{ob}	 — —	 400 600	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 50 V) (See Figure 2.)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	10.0	2.5	μs

1. Pulsed Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

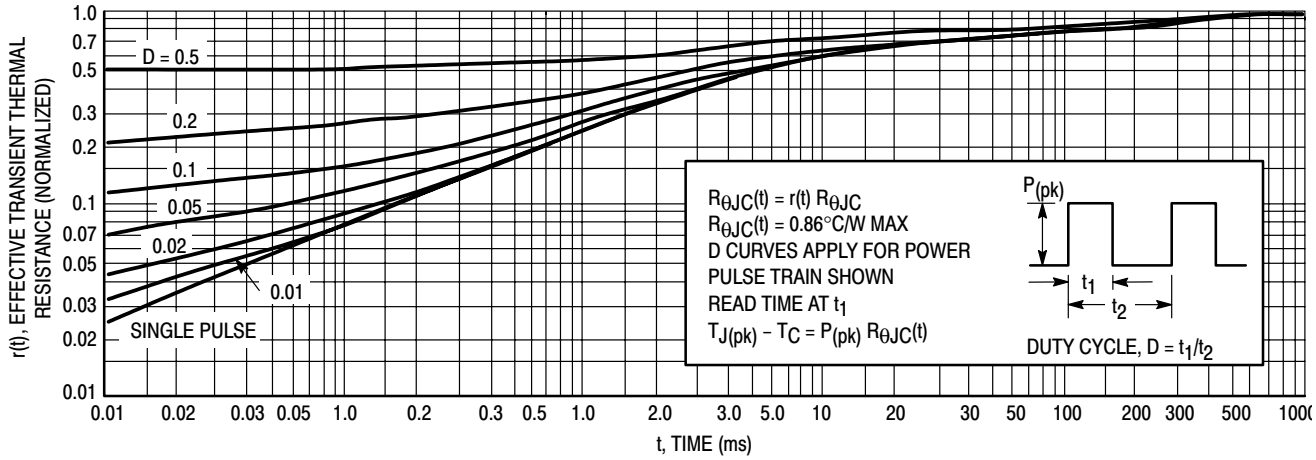


Figure 3. Thermal Response

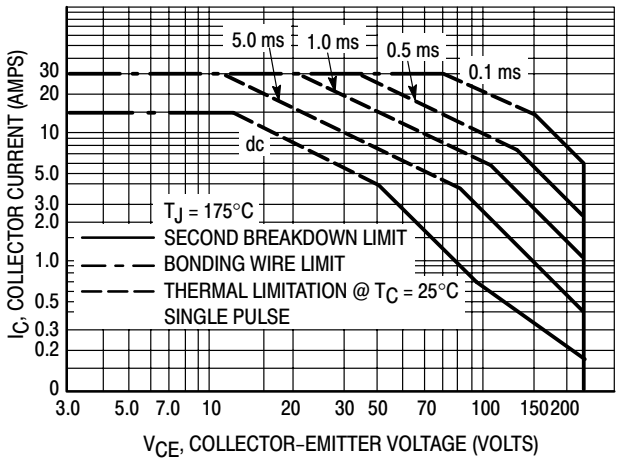


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

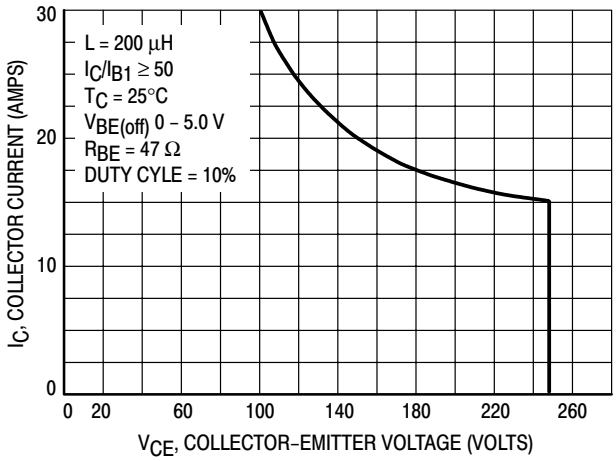


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 175°C, T_C is variable dependIng on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 175°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be hold to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

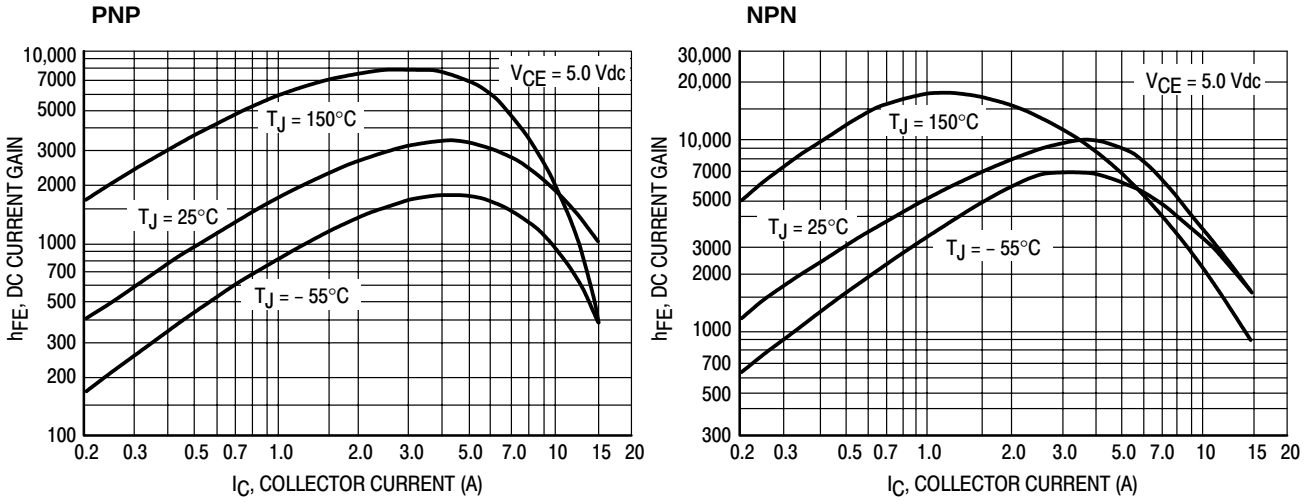


Figure 6. DC Current Gain

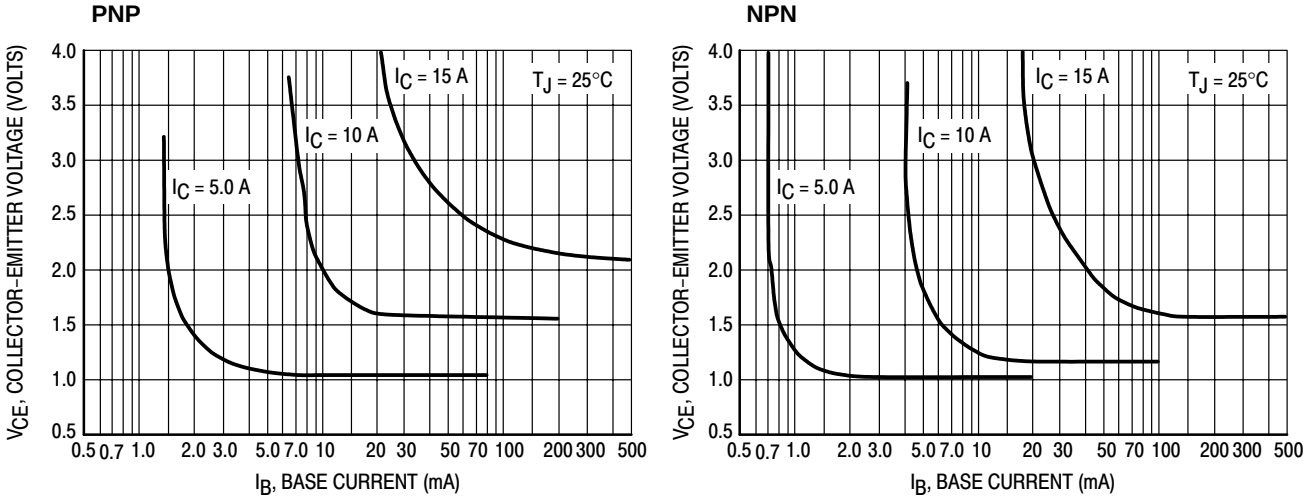


Figure 7. Collector Saturation Region

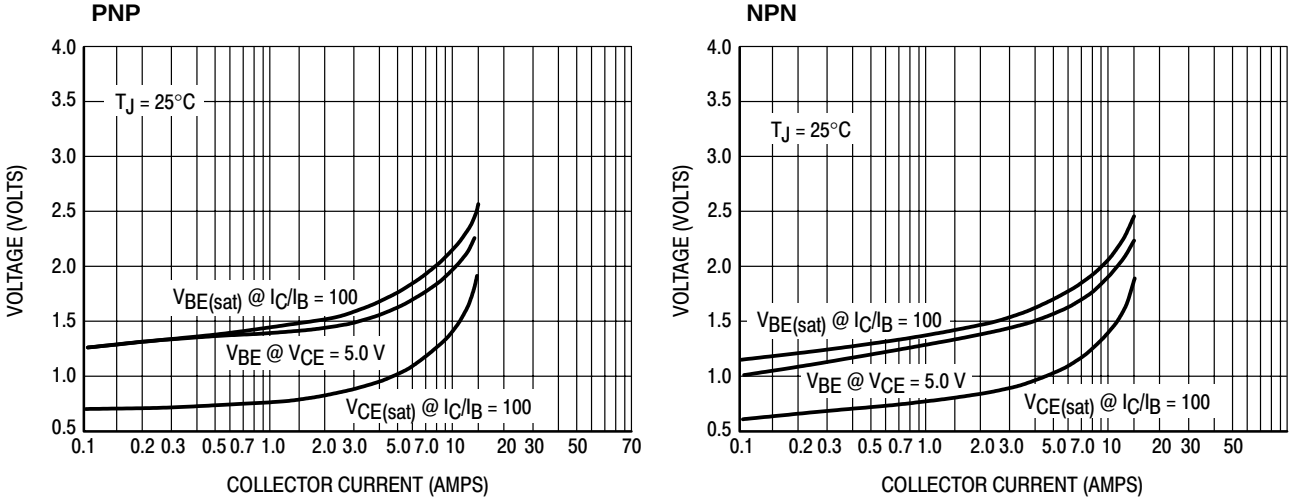


Figure 8. “On” Voltages

(NPN) MJ11028, MJ11030, MJ11032 (PNP) MJ11029, MJ11033

High-Current Complementary Silicon Power Transistors

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain −
  h_{FE} = 1000 (Min) @ I_C = 25 Adc
  h_{FE} = 400 (Min) @ I_C = 50 Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built−In Base−Emitter Shunt Resistor
- Junction Temperature to +200°C

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	MJ11028/29 MJ11030 MJ11032/33	V_{CEO}	60 90 120	Vdc
Collector−Base Voltage	MJ11028/29 MJ11030 MJ11032/33	V_{CBO}	60 90 120	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current − Continuous − Peak (Note 2)		I_C	50 100	Adc
Base Current − Continuous		I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C @ T_C = 100°C		P_D	300 1.71	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	°C
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.58	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

ON Semiconductor®

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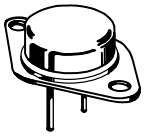
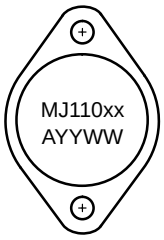
50 AMPERE COMPLEMENTARY DARLINGTON POWER TRANSISTORS 60 − 120 VOLTS 300 WATTS



TO−204 (TO−3)
CASE 197A
STYLE 1

MARKING DIAGRAM



xx = 28, 29, 30, 32, 33
A = Location Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJ110xx	TO−204	100 Units/Tray

Publication Order Number:

(NPN) MJ11028, MJ11030, MJ11032 (PNP) MJ11029, MJ11033

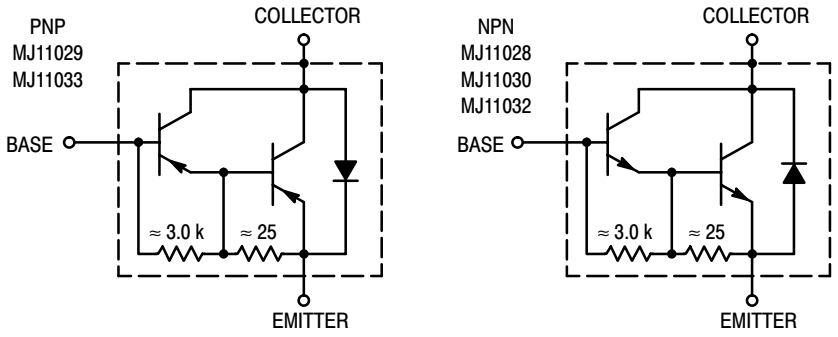


Figure 1. Darlington Circuit Schematic

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (Note 1) (I_C = 1 00 mAdc, I_B = 0)	MJ11028, MJ11029 MJ11030 MJ11032, MJ11033	$V_{(BR)CEO}$	60 90 120	— — —	Vdc
Collector−Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11028, MJ11029		—	2	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm)	MJ11030		—	2	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11032, MJ11033		—	2	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11028, MJ11029		—	10	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11032, MJ11033		—	10	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
Collector−Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	2	mAdc
ON CHARACTERISTICS (Note 1)					
DC Current Gain		h_{FE}			—
(I_C = 25 Adc, V_{CE} = 5 Vdc)			1 k	18 k	
(I_C = 50 Adc, V_{CE} = 5 Vdc)			400	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 250 mAdc)			—	2.5	
(I_C = 50 Adc, I_B = 500 mAdc)			—	3.5	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 200 mAdc)			—	3.0	
(I_C = 50 Adc, I_B = 300 mAdc)			—	4.5	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

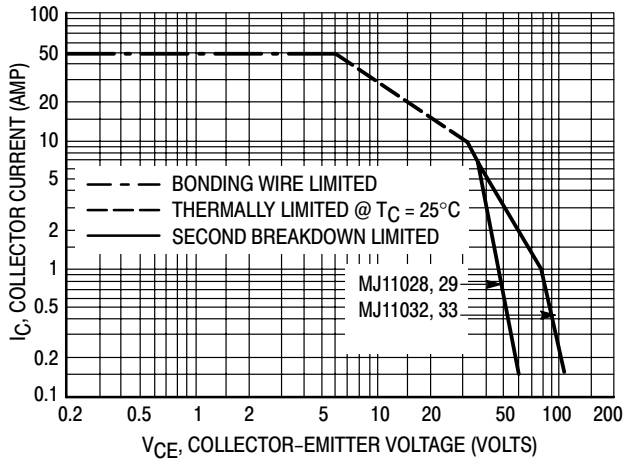


Figure 2. DC Safe Operating Area

There are two limitations on the power−handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

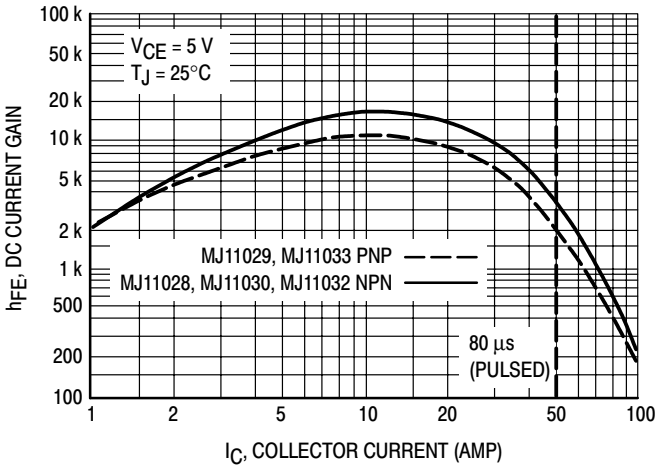


Figure 3. DC Current Gain

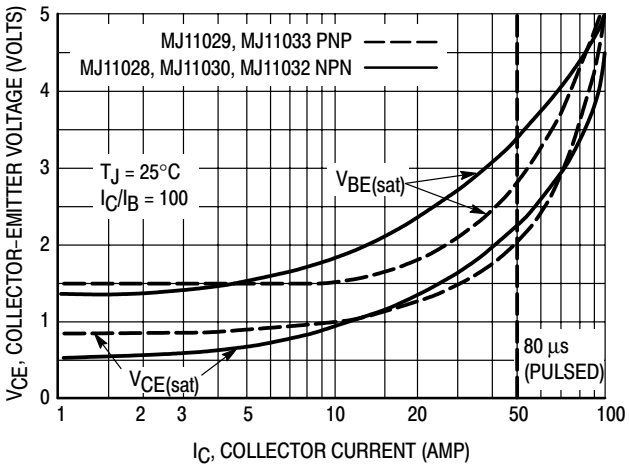


Figure 4. “On” Voltage

MJ14001 (PNP), MJ14002* (NPN), MJ14003* (PNP)

*Preferred Devices

High-Current Complementary Silicon Power Transistors

Designed for use in high−power amplifier and switching circuit applications.

- High Current Capability −
  I_C Continuous = 60 Amperes
- DC Current Gain −
  h_{FE} = 15−100 @ I_C = 50 Adc
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

MAXIMUM RATINGS

Rating	Symbol	MJ14001	MJ14002 MJ14003	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector Base Voltage	V_{CBO}	60	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0		Vdc
Collector Current − Continuous	I_C	60		Adc
Base Current − Continuous	I_B	15		Adc
Emitter Current − Continuous	I_E	75		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

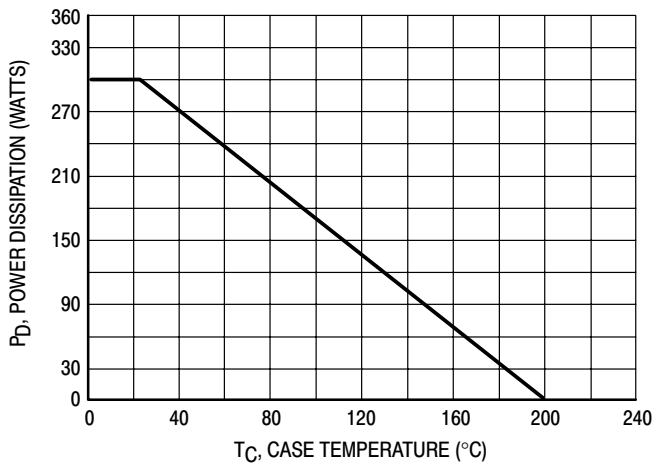


Figure 1. Power Derating

ON Semiconductor®

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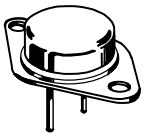
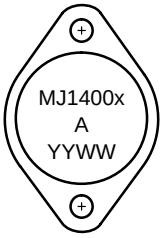
COMPLEMENTARY SILICON POWER TRANSISTORS 60 AMPERES 60−80 VOLTS 300 WATTS



TO−204 (TO−3)
STYLE 1
CASE 197A

MARKING DIAGRAM



MJ1400x = Device Code
A = Assembly Location
YY = Year
WW = Work Week
x = 1, 2, or 3

ORDERING INFORMATION

Device	Package	Shipping
MJ14001	TO−3	100 Units/Tray
MJ14002	TO−3	100 Units/Tray
MJ14003	TO−3	100 Units/Tray

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJ14001		60	−	
	MJ14002, MJ14003		80	−	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 Vdc, I_B = 0)	MJ14001		−	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ14402, MJ14003		−	1.0	
Collector Cutoff Current		I_{CEX}			mA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14001		−	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14002, MJ14003		−	1.0	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 60 Vdc, I_E = 0)	MJ14001		−	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	MJ14002, MJ14003		−	1.0	
Emitter Cutoff Current		I_{EBO}	−	1.0	mA
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (Note 2)		h_{FE}			−
(I_C = 25 Adc, V_{CE} = 3.0 V)			30	−	
(I_C = 50 Adc, V_{CE} = 3.0 V)			15	100	
(I_C = 60 Adc, V_{CE} = 3.0 V)			5.0	−	
Collector−Emitter Saturation Voltage (Note 2)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			−	1.0	
(I_C = 50 Adc, I_B = 5.0 Adc)			−	2.5	
(I_C = 60 Adc, I_B = 12 Adc)			−	3.0	
Base−Emitter Saturation Voltage (Note 2)		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			−	2.0	
(I_C = 50 Adc, I_B = 5.0 Adc)			−	3.0	
(I_C = 60 Adc, I_B = 12 Adc)			−	4.0	
DYNAMIC CHARACTERISTICS					
Output Capacitance		C_{ob}	−	2000	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)					

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

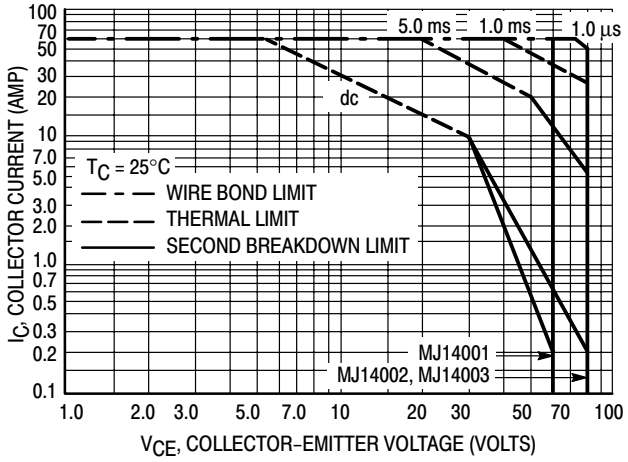


Figure 2. Maximum Rated Forward Biased Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL ELECTRICAL CHARACTERISTICS

MJ14002 (NPN)

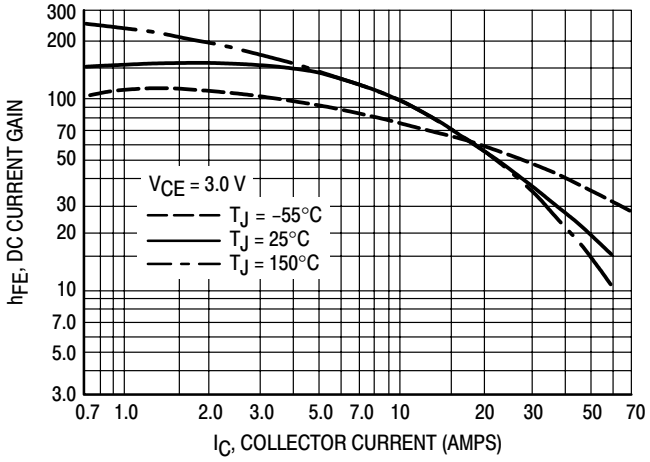


Figure 3. DC Current Gain

MJ14001, MJ14003 (PNP)

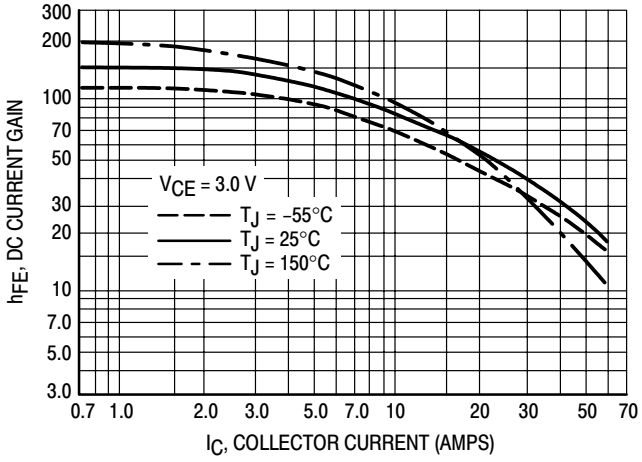


Figure 4. DC Current Gain

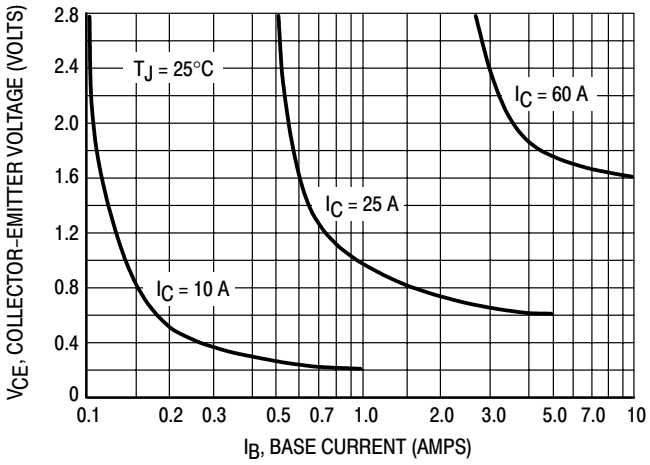


Figure 5. Collector Saturation Region

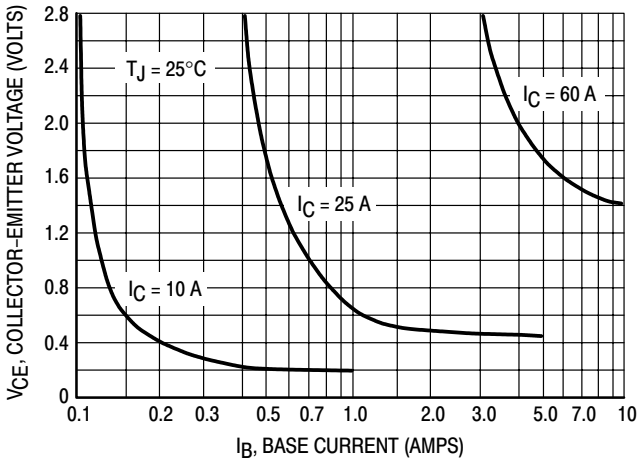


Figure 6. Collector Saturation Region

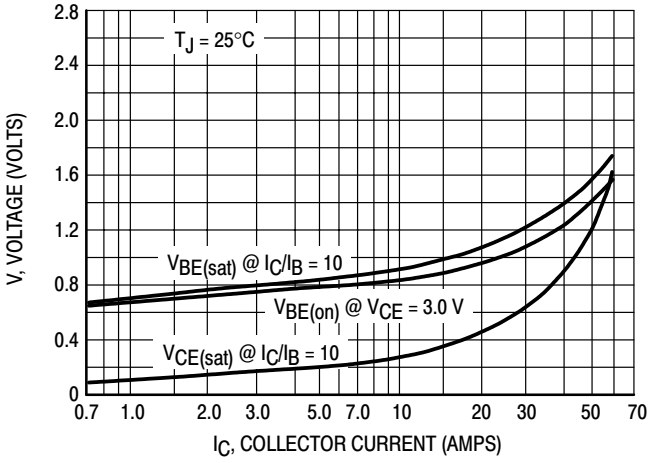


Figure 7. “On” Voltages

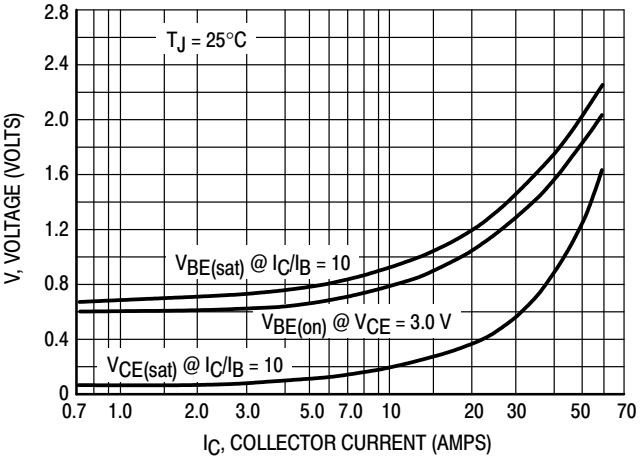


Figure 8. “On” Voltages

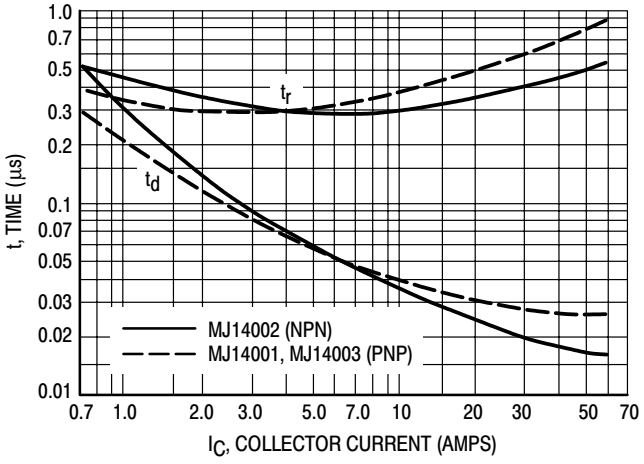


Figure 9. Turn−On Switching Times

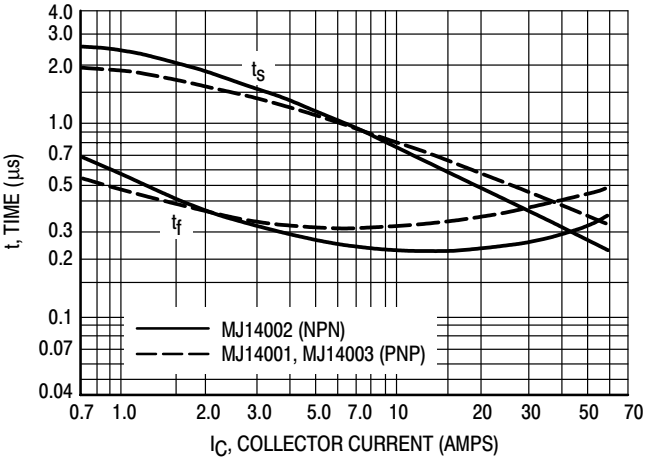


Figure 10. Turn−Off Switching Times

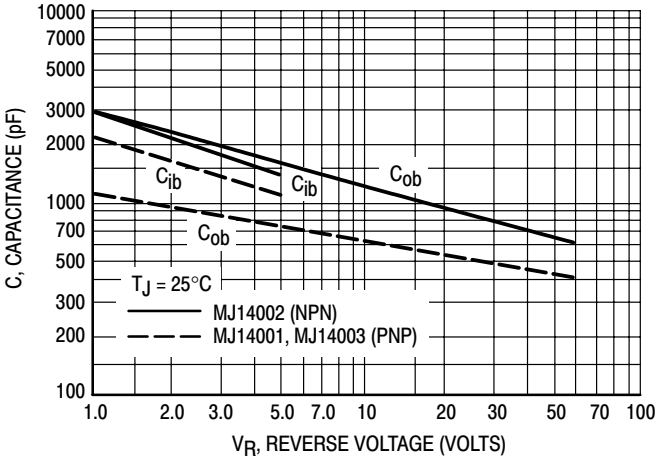
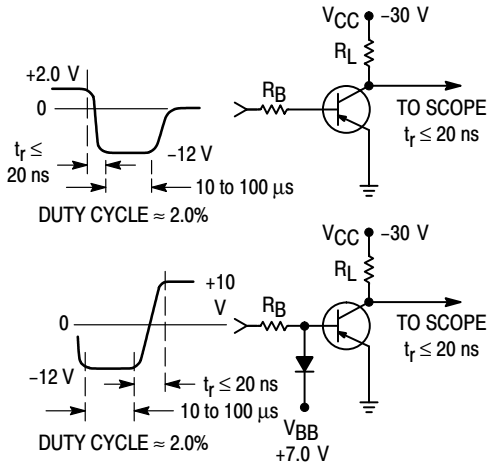


Figure 11. Capacitance Variation



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 12. Switching Test Circuit

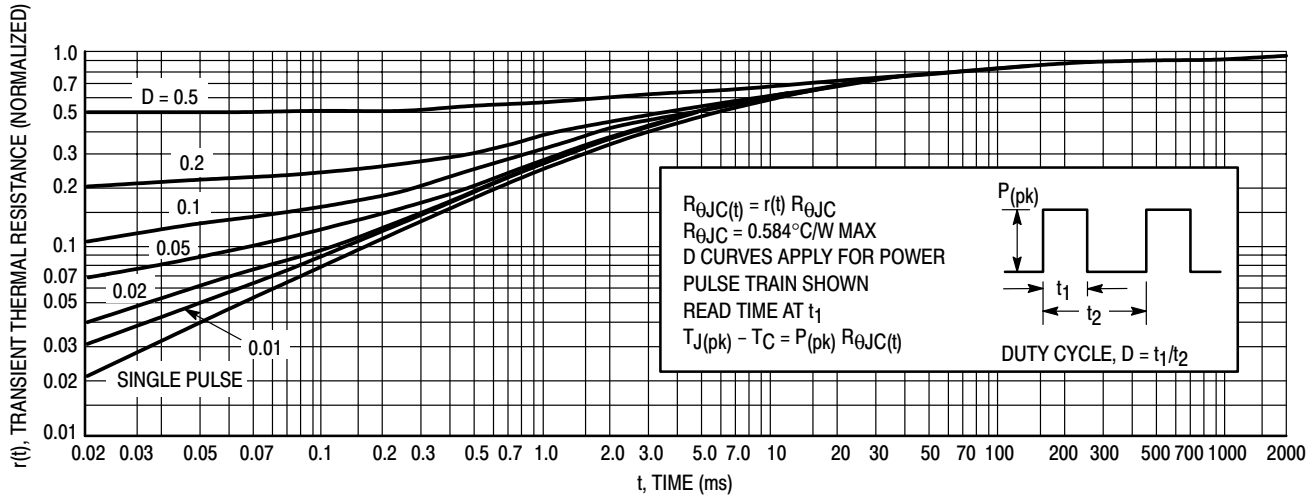


Figure 13. Thermal Response

MJ15001 (NPN), MJ15002 (PNP)

Complementary Silicon Power Transistors

The MJ15001 and MJ15002 are EpiBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) −
  5.0 A @ 40 V
  0.5 A @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain −
  h_{FE} = 25 (Min) @ I_C = 4 Adc

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CBO}	140	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current − Continuous	I_B	5	Adc
Emitter Current − Continuous	I_E	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

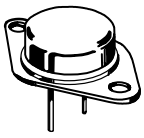
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤ 10 seconds	T_L	265	°C

ON Semiconductor®

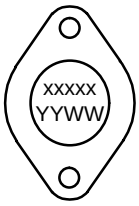
http://onsemi.com

20 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
140 V 250 W



TO−204 (TO−3)
CASE 1−07

MARKING DIAGRAM



xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJ15001	TO−204AA (TO−3)	100 Foams
MJ15002	TO−204AA (TO−3)	100 Foams

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C, = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	−	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 − −	 100 2.0	 μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	−	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	−	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non−repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non−repetitive))	$I_{S/b}$	 5.0 0.5	 − −	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	−
Collector−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	−	1.0	Vdc
Base−Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	−	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2.0	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	1000	pF

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

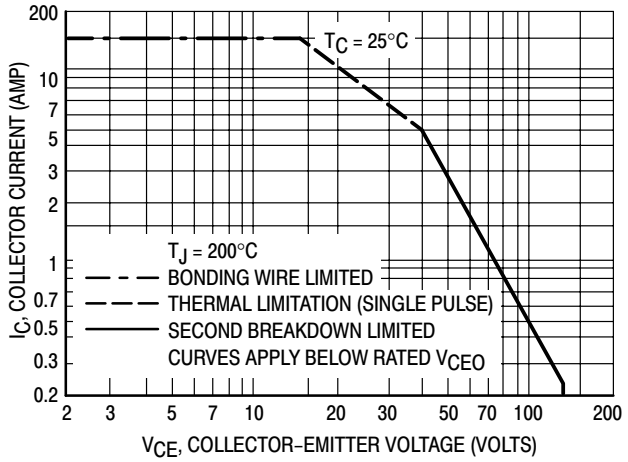


Figure 1. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J\,(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

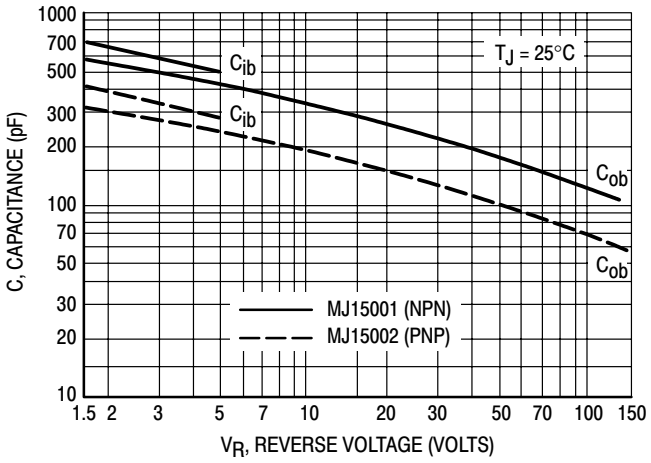


Figure 2. Capacitances

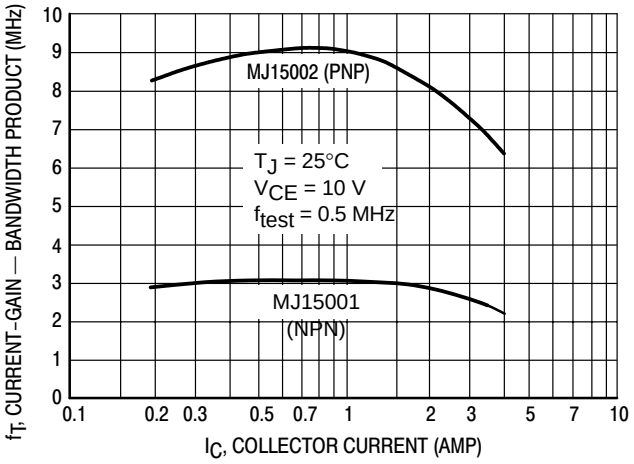


Figure 3. Current−Gain — Bandwidth Product

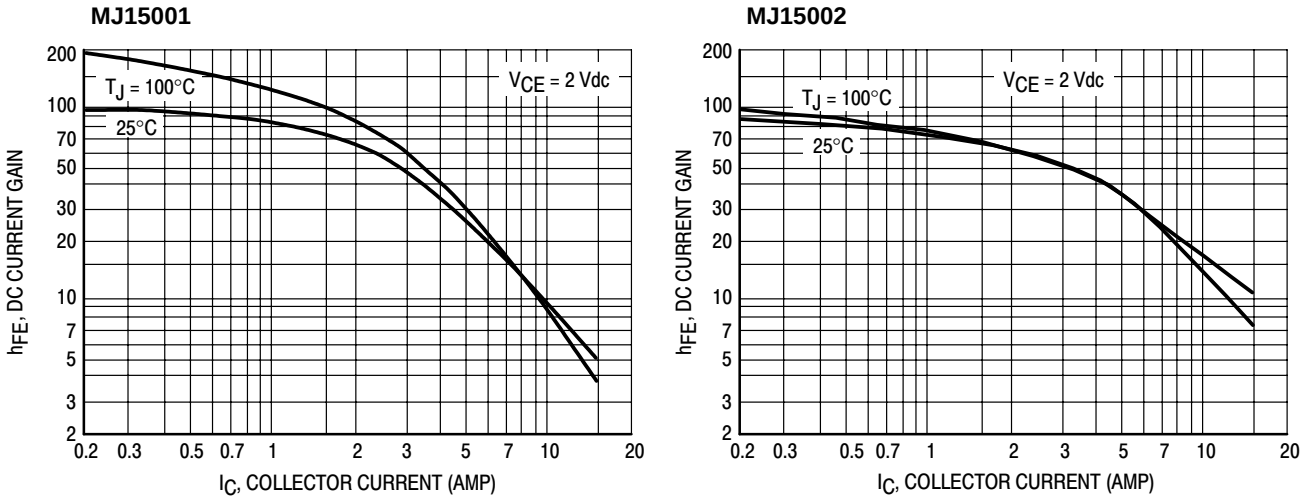


Figure 4. DC Current Gain

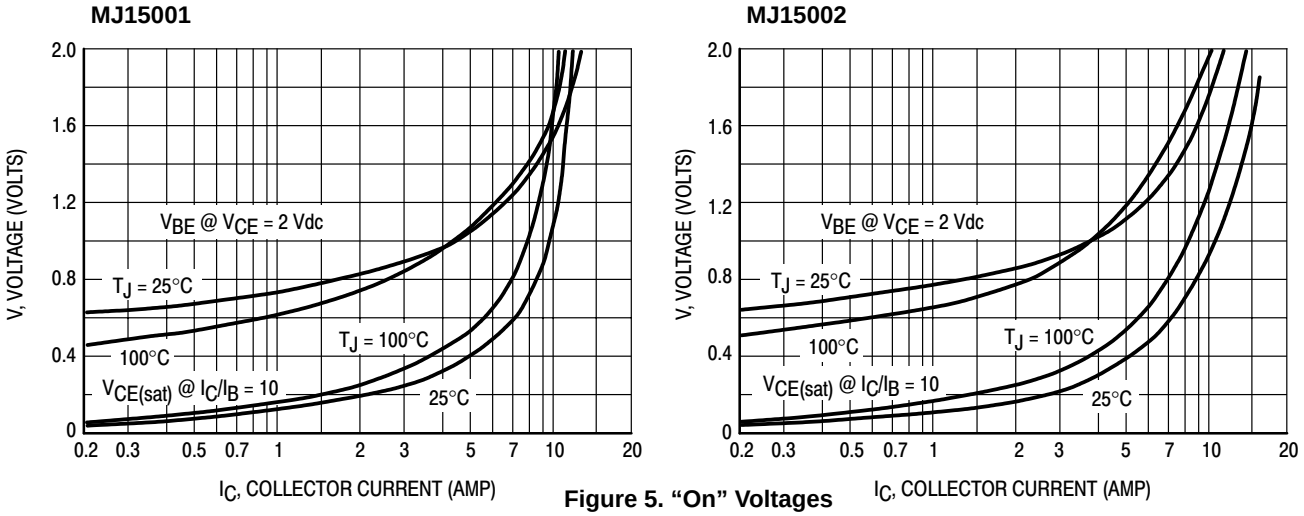


Figure 5. “On” Voltages

MJ15003 (NPN), MJ15004 (PNP)

Preferred Device

Complementary Silicon Power Transistors

The MJ15003 and MJ15004 are PowerBase™ power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) − 5.0 A @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain − h_{FE} = 25 (Min) @ I_C = 5 Adc

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CBO}	140	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector Current − Continuous	I_C	20	Adc
Base Current − Continuous	I_B	5	Adc
Emitter Current − Continuous	I_E	25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

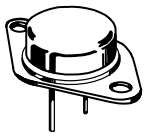
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.70	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤ 10 seconds	T_L	265	°C

ON Semiconductor®

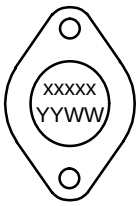
http://onsemi.com

20 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
140 V 250 W



TO−204AA (TO−3)
CASE 1−07

MARKING DIAGRAM



xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJ15003	TO−204AA (TO−3)	100 Foams
MJ15004	TO−204AA (TO−3)	100 Foams

Preferred devices are recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage (Note 4) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 100 2	 μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Baised (V_{CE} = 50 Vdc, t = 1 s (non repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non repetitive))	$I_{S/b}$	 5.0 1.0	 – –	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	
Collector Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
Base Emitter On Voltage (I_C = 5 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	c_{ob}	–	1000	pF

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

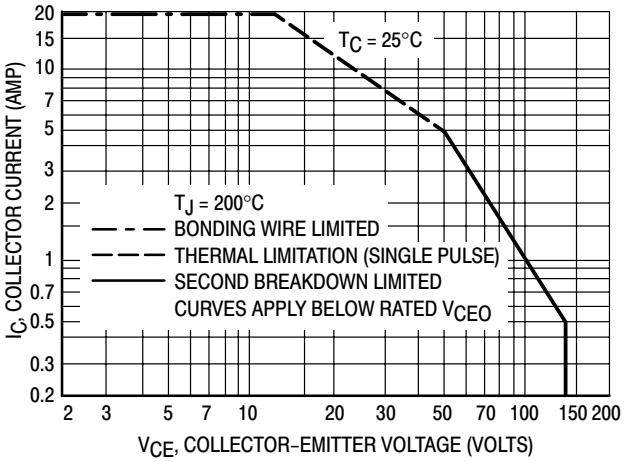


Figure 1. Active−Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

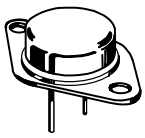
The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Silicon Power Transistors

NPN
MJ15011*
PNP
MJ15012*

*ON Semiconductor Preferred Device

10 AMPERE
COMPLEMENTARY
POWER TRANSISTORS
250 VOLTS
200 WATTS



CASE 1−07
TO−204AA
(TO−3)

The MJ15011 and MJ15012 are PowerBase power transistors designed for high−power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc−to−dc converters or inverters.

- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Emitter Voltage	V_{CEX}	250	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 − Rev. 2
Publication Order Number:
MJ15011/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{(BR)CEO}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	—	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 15 Vdc)	I_{CEX}	—	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	—	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	 20 5	 100 —	—
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.2 Adc) (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	 — —	 0.8 2 5	Vdc
Base−Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	—	750	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 0.5 s) (V_{CE} = 100 Vdc, t = 0.5 s)	$I_{S/b}$	 5 1.4	 — —	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

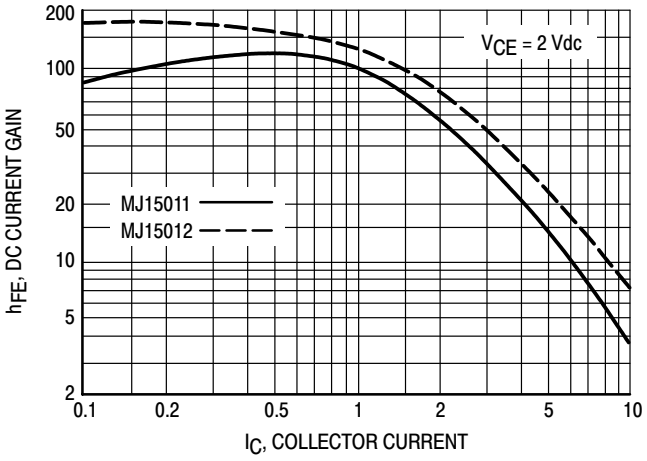


Figure 2. DC Current Gain

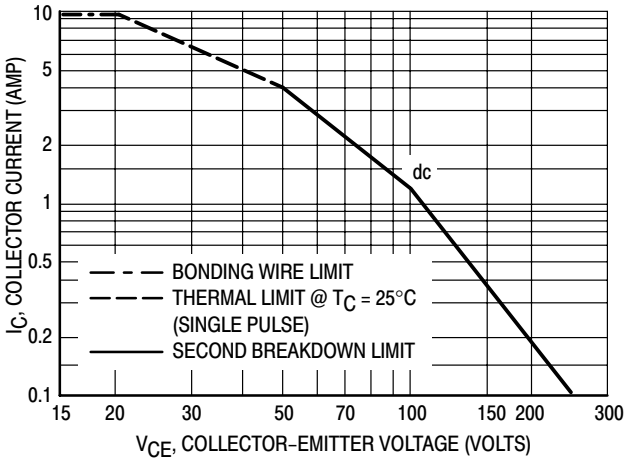


Figure 3. Active Region Safe Operating Area

Complementary Silicon Power Transistors

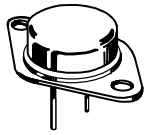
. . . designed for use as high frequency drivers in Audio Amplifiers.

- High Gain Complementary Silicon Power Transistors
- Safe Operating Area 100% Tested 50 V, 3.0 A, 1.0 Sec.
- Excellent Frequency Response —
  f_T = 20 MHz min.

NPN
MJ15020*
PNP
MJ15021*

*ON Semiconductor Preferred Device

4.0 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
150 WATTS



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS

Rating	Symbol	MJ15020 MJ15021	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	250	Vdc
Emitter−Base Voltage	V_{EBO}	7.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	6.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

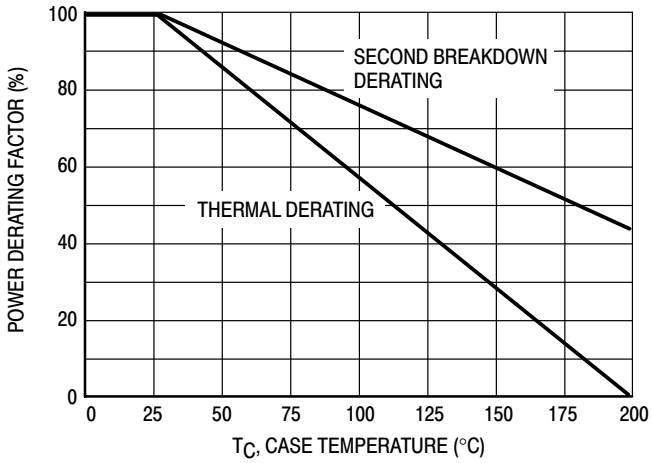


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 − Rev. 0
Publication Order Number:
MJ15020/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0) MJ15020, MJ15021	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) MJ15020, MJ15021	I_{CEO}	—	500	μAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	500	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward−Biased (V_{CE} = 50 Vdc, t = 0.5 s (non−repetitive)	$I_{S/b}$	3.0	—	Adc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 V) (I_C = 3.0 Adc, V_{CE} = 4.0 V)	h_{FE}	30 10	— —	
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	1.0	Vdc
Base−Emitter on Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	20	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, F_{test} = 1.0 MHz)	C_{ob}	—	500	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

TYPICAL DYNAMIC CHARACTERISTICS

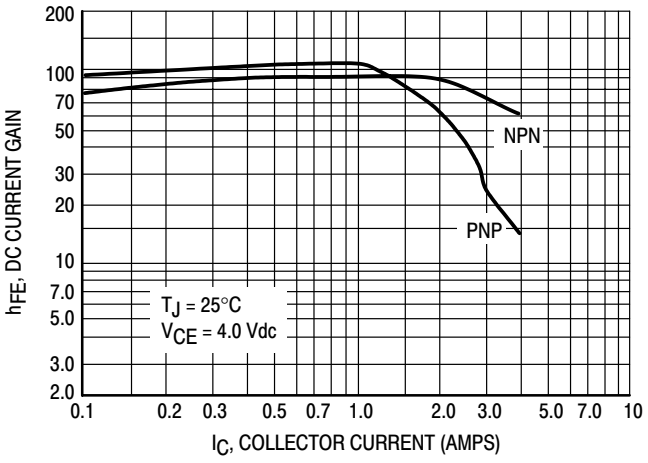


Figure 2. DC Current Gain

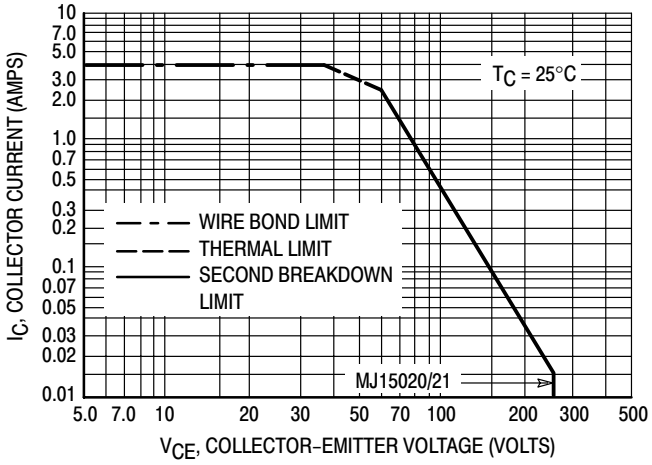
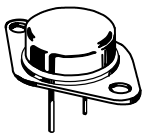


Figure 3. Maximum Rated Forward Biased Safe Operating Area

NPN
MJ15022
MJ15024 *

*ON Semiconductor Preferred Device

16 AMPERE
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 1−07
TO−204AA
(TO−3)

Silicon Power Transistors

The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  2 A @ 80 V
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 8 Adc

MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector−Emitter Voltage	V_{CEO}	200	250	Vdc
Collector−Base Voltage	V_{CBO}	350	400	Vdc
Emitter−Base Voltage	V_{EBO}	5		Vdc
Collector−Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 − Rev. 9
Publication Order Number:
MJ15022/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	 MJ15022 MJ15024	$V_{CEO(sus)}$	 200 250	 — —	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15022 MJ15024	I_{CEX}	 — —	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 vdc, I_B = 0)	 MJ15022 MJ15024	I_{CEO}	 — —	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)		I_{EBO}	—	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non−repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non−repetitive))		$I_{S/b}$	 5 2	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 —	—
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 — —	 1.4 4.0	Vdc
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

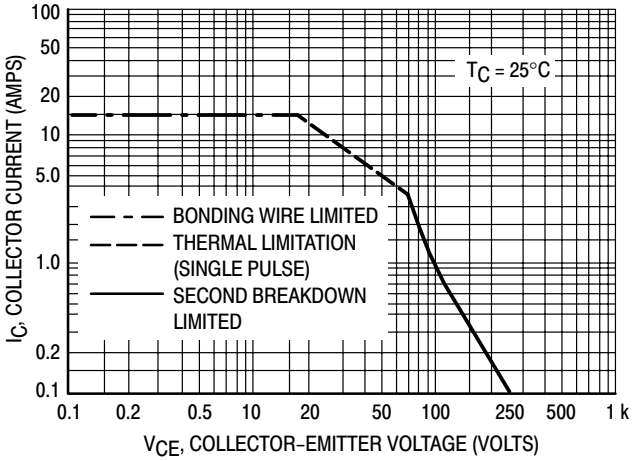


Figure 1. Active−Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values Ion than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

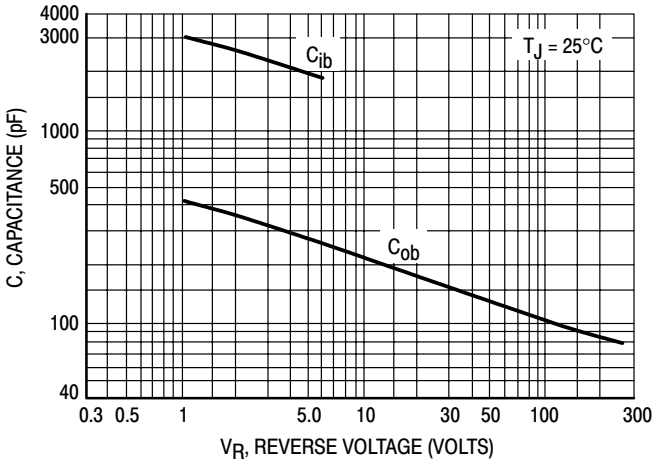


Figure 2. Capacitances

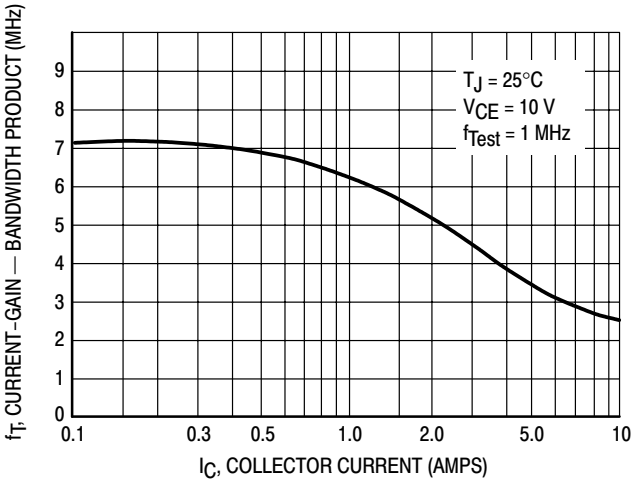


Figure 3. Current−Gain — Bandwidth Product

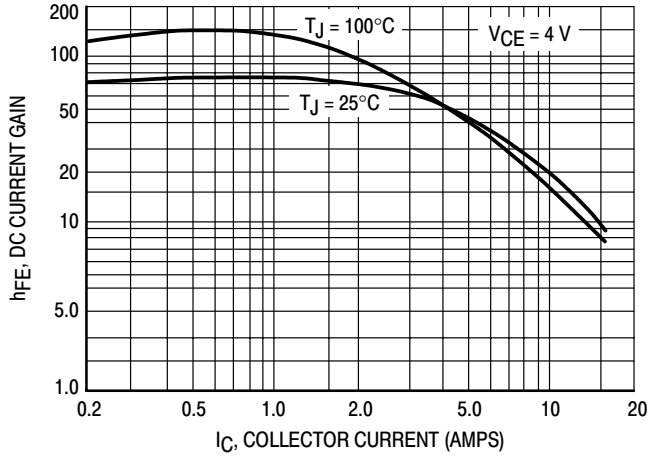


Figure 4. DC Current Gain

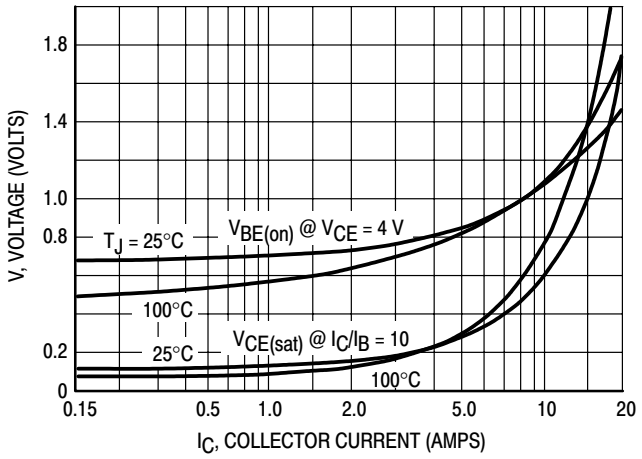


Figure 5. “On” Voltage

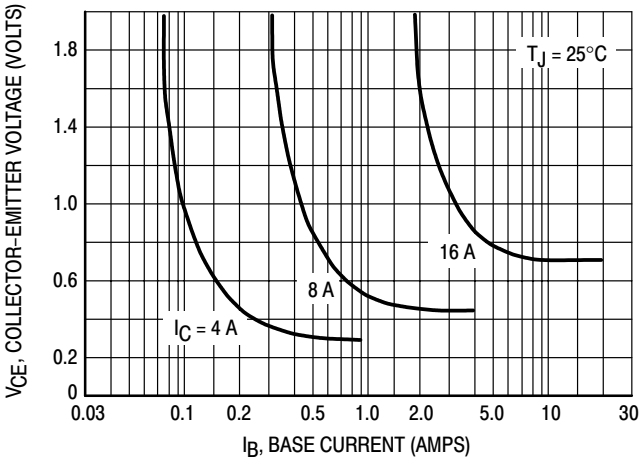
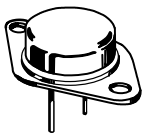


Figure 6. Collector Saturation Region

PNP
MJ15023
MJ15025 *

*ON Semiconductor Preferred Device

16 AMPERE
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 1−07
TO−204AA
(TO−3)

Silicon Power Transistors

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  2 A @ 80 V
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 8 Adc

MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector−Emitter Voltage	V_{CEO}	200	250	Vdc
Collector−Base Voltage	V_{CBO}	350	400	Vdc
Emitter−Base Voltage	V_{EBO}	5		Vdc
Collector−Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 − Rev. 9
Publication Order Number:
MJ15023/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ15023 MJ15025	$V_{CEO(sus)}$	 200 250	 — —	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15023 MJ15025	I_{CEX}	 — —	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	 MJ15023 MJ15025	I_{CEO}	 — —	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)	Both	I_{EBO}	—	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non−repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non−repetitive))		$I_{S/b}$	 5 2	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 —	—
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 —	 1.4 4.0	Vdc
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	600	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

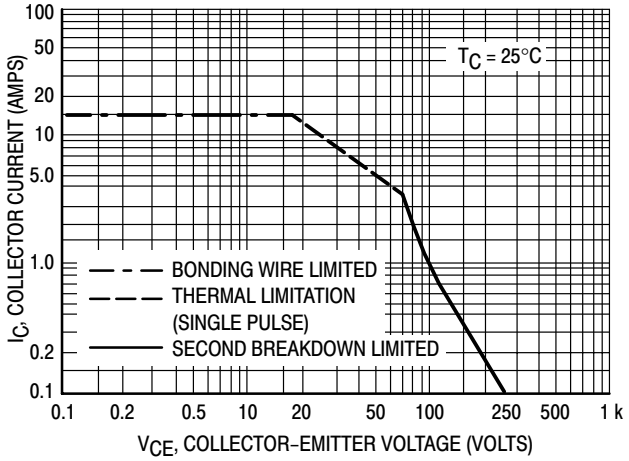


Figure 1. Active−Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

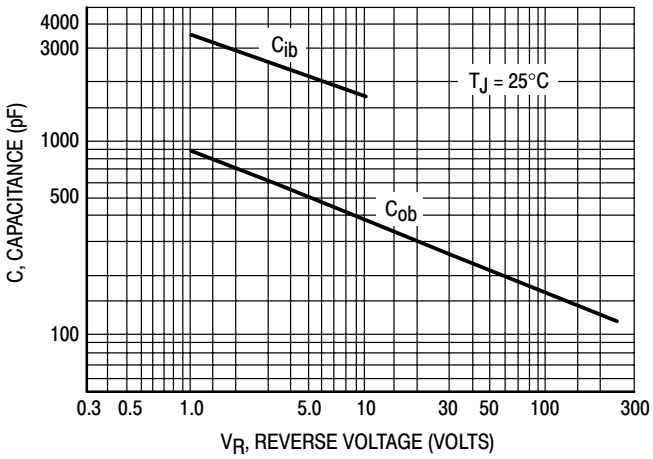


Figure 2. Capacitances

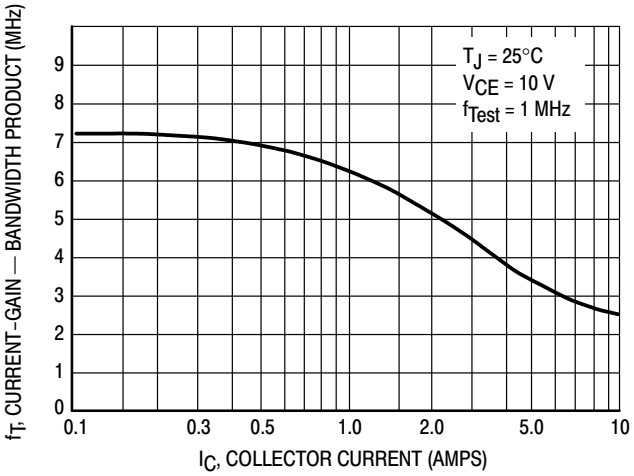


Figure 3. Current−Gain — Bandwidth Product

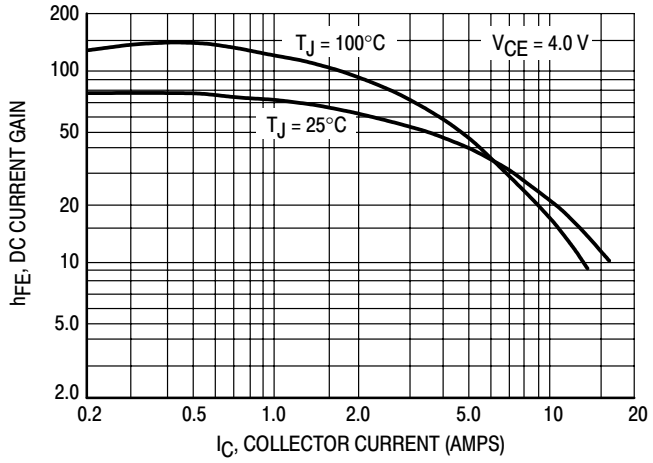


Figure 4. DC Current Gain

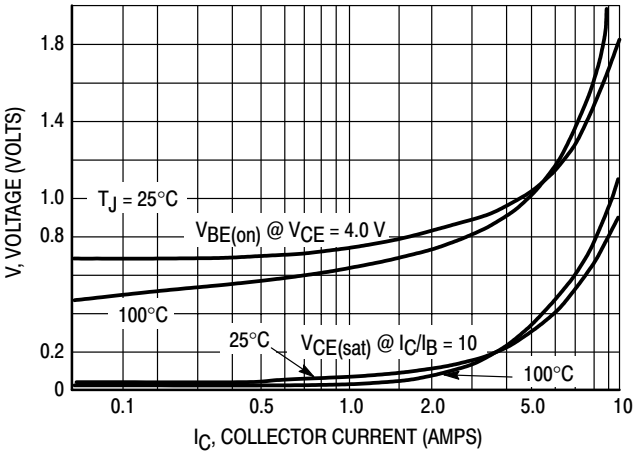


Figure 5. “On” Voltages

Silicon Power Transistors

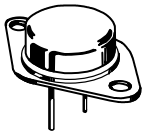
PNP
MJ21193*
NPN
MJ21194*

*ON Semiconductor Preferred Device

The MJ21193 and MJ21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain −
  h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.5 A, 80 V, 1 Second

16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
250 WATTS



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS

Rating	Sym-bol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current — Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%. (continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 − Rev. 3
Publication Order Number:
MJ21193/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive) (V_{CE} = 80 Vdc, t = 1 s (non−repetitive)	$I_{S/b}$	 5 2.5	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, I_B = 5 Adc)	h_{FE}	 25 8	 — —	75	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 — —	 1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched ed (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 — —	 0.8 0.08	 — —	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJ21193

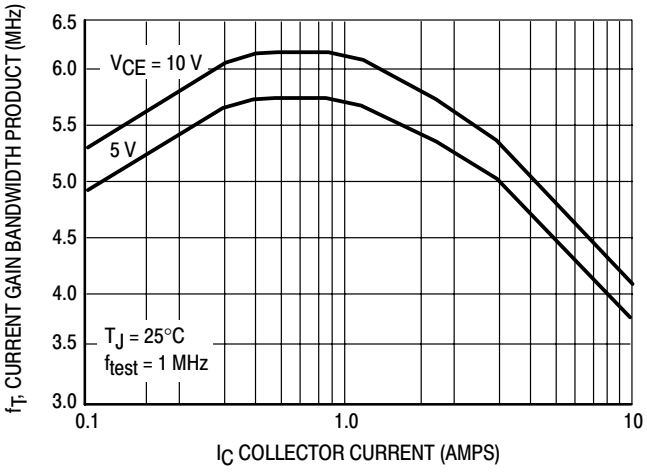


Figure 1. Typical Current Gain Bandwidth Product

NPN MJ21194

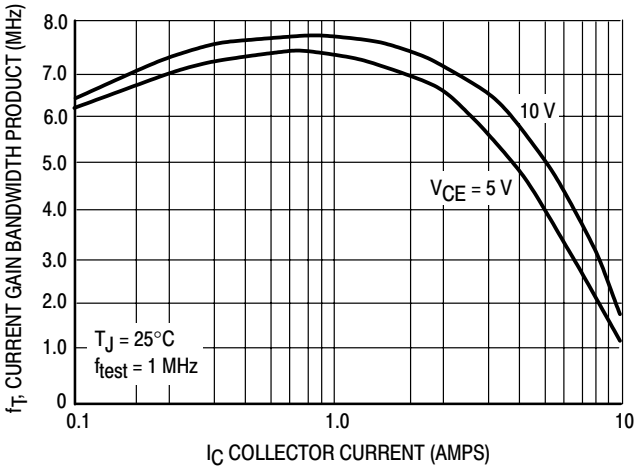


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJ21193

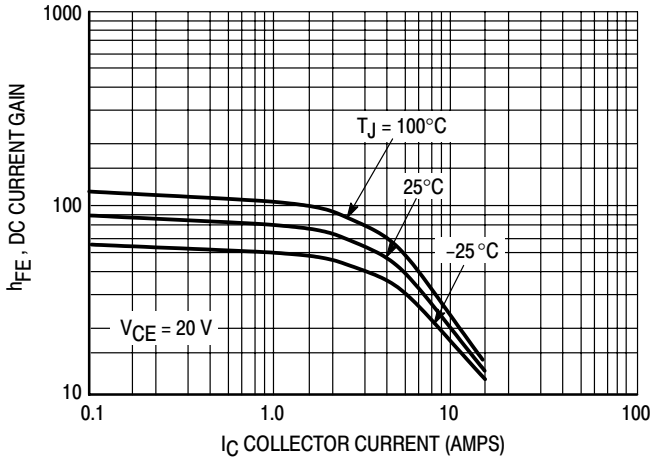


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJ21194

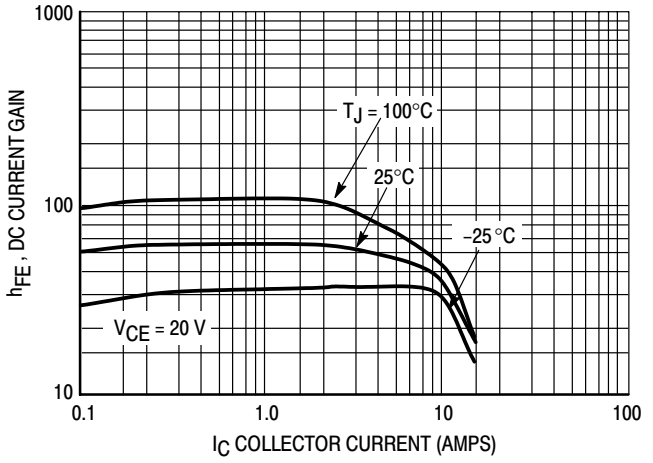


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJ21193

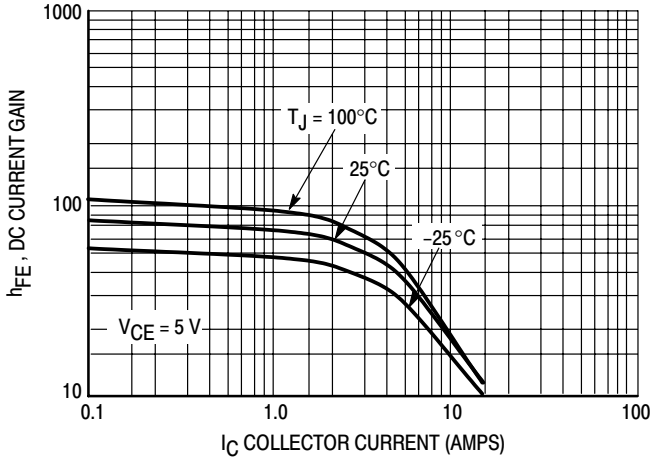


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ21194

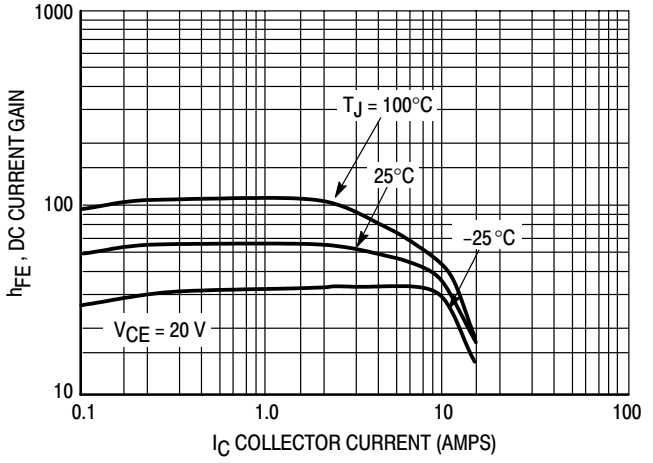


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJ21193

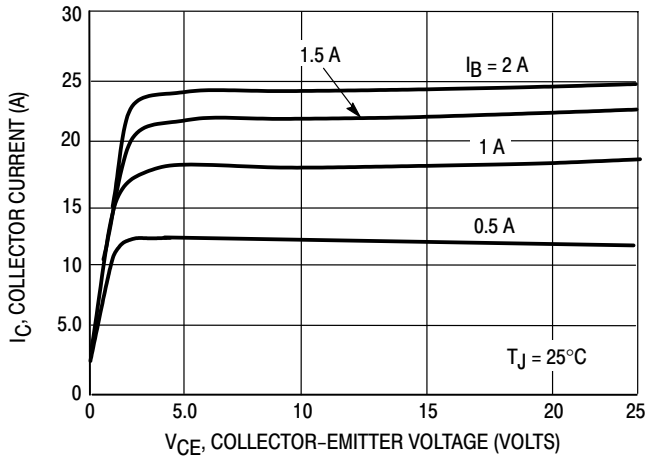


Figure 7. Typical Output Characteristics

NPN MJ21194

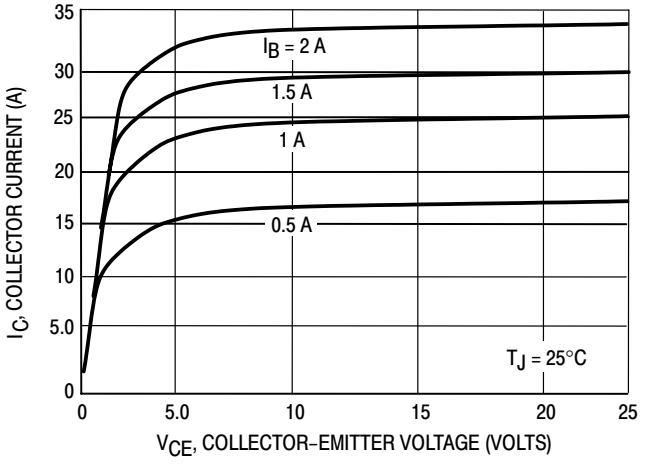


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21193

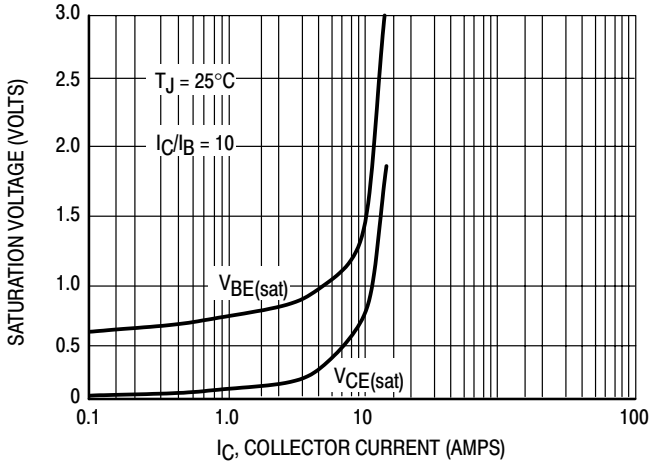


Figure 9. Typical Saturation Voltages

NPN MJ21194

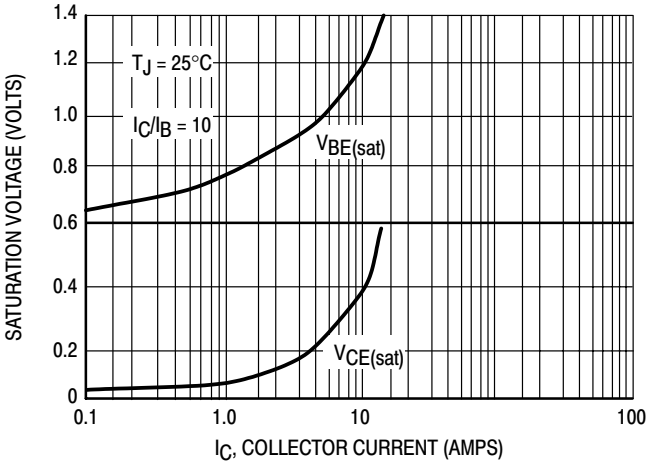


Figure 10. Typical Saturation Voltages

PNP MJ21193

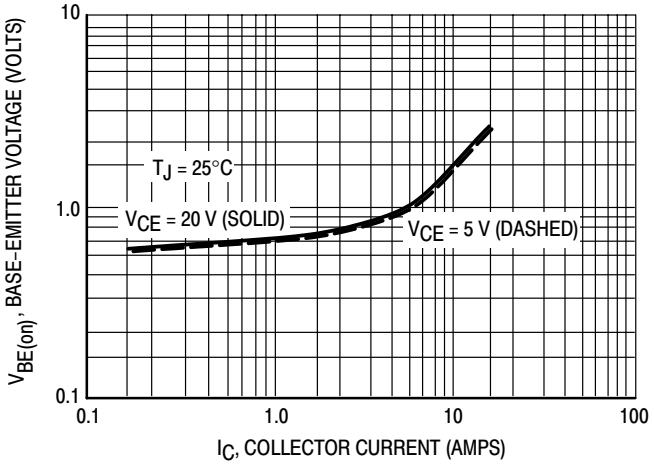


Figure 11. Typical Base−Emitter Voltage

NPN MJ21194

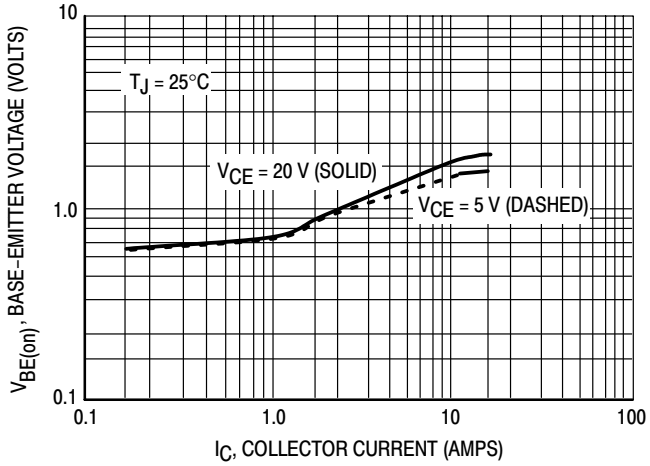


Figure 12. Typical Base−Emitter Voltage

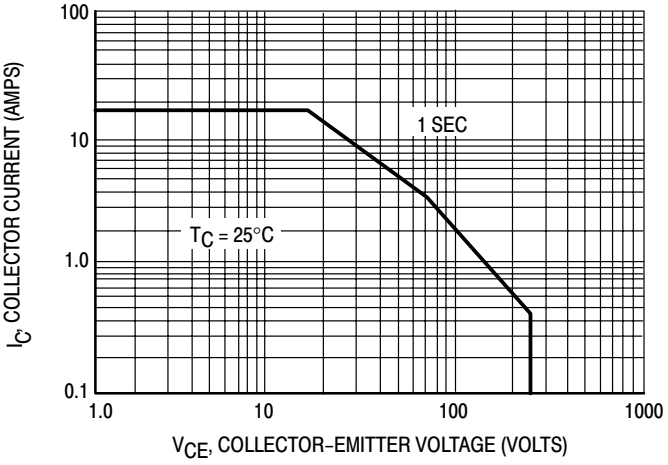


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

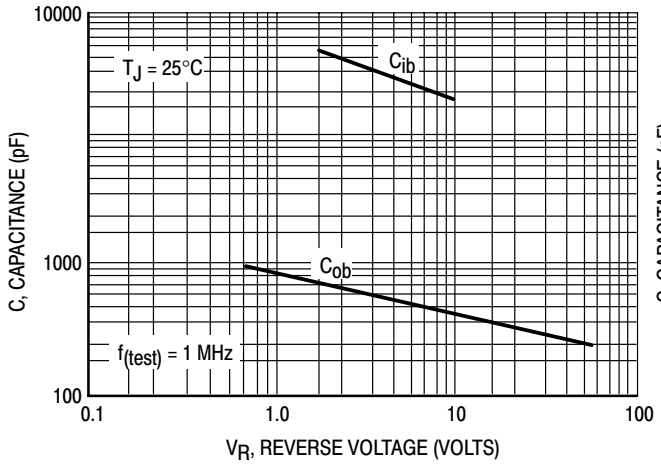


Figure 14. MJ21193 Typical Capacitance

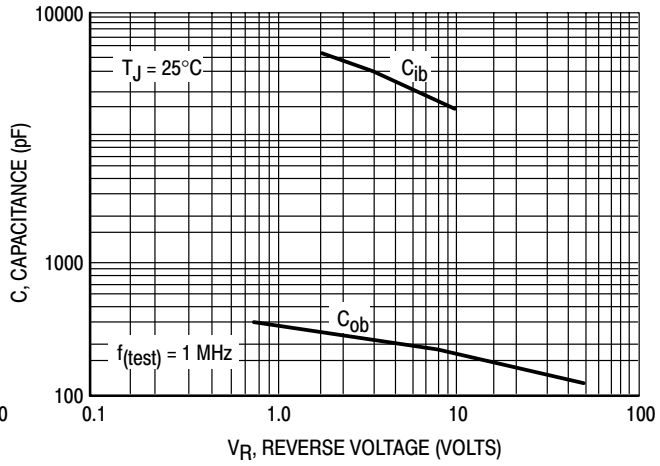


Figure 15. MJ21194 Typical Capacitance

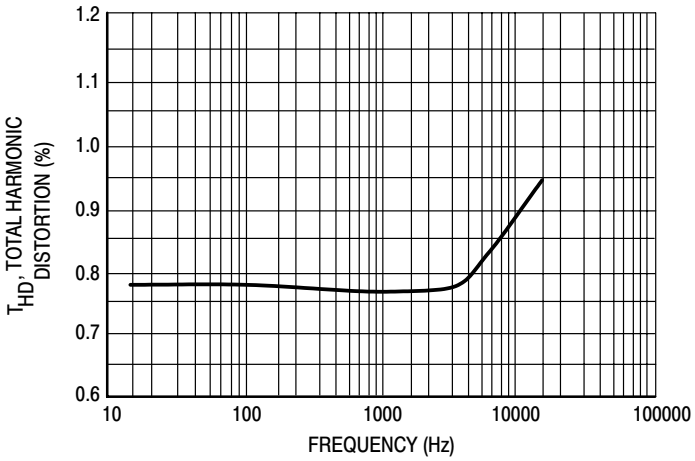


Figure 16. Typical Total Harmonic Distortion

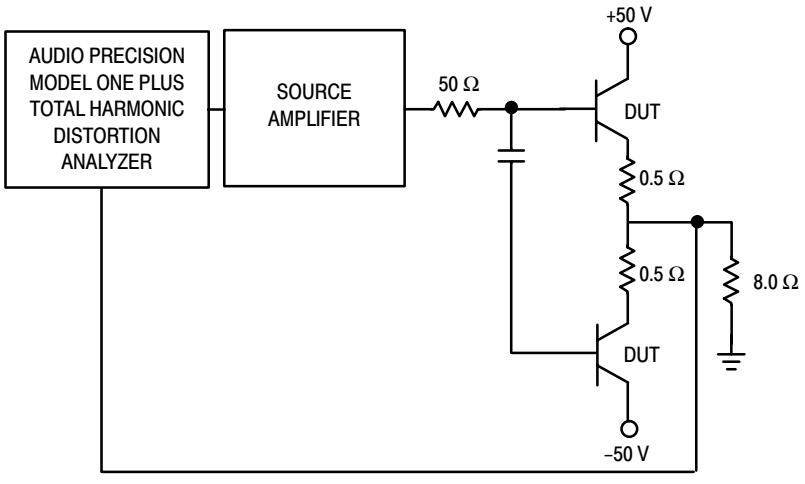


Figure 17. Total Harmonic Distortion Test Circuit

Silicon Power Transistors

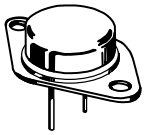
PNP
MJ21195*
NPN
MJ21196*

*ON Semiconductor Preferred Device

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain − h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Second

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 250 WATTS



CASE 1−07 TO−204AA (TO−3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current — Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C ± 5°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2002 − Rev. 3
Publication Order Number:
MJ21195/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive) (V_{CE} = 80 Vdc, t = 1 s (non−repetitive)	$I_{S/b}$	 5 2.5	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, V_{CE} = 5 Vdc)	h_{FE}	 25 8	 — —	75	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 — —	 1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched ed (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 — —	 0.8 0.08	 — —	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJ21195

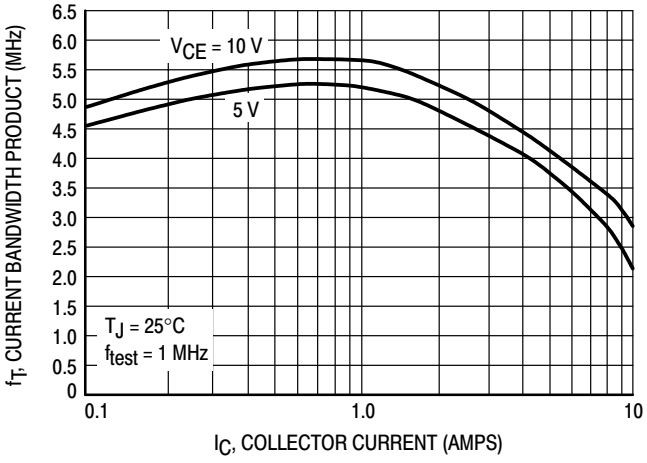


Figure 1. Typical Current Gain Bandwidth Product

NPN MJ21196

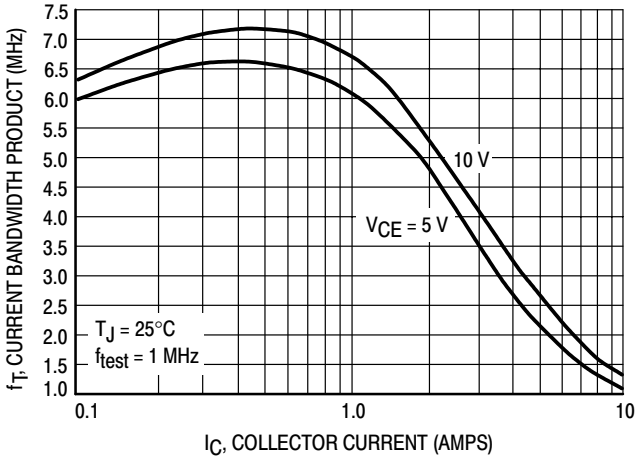


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJ21195

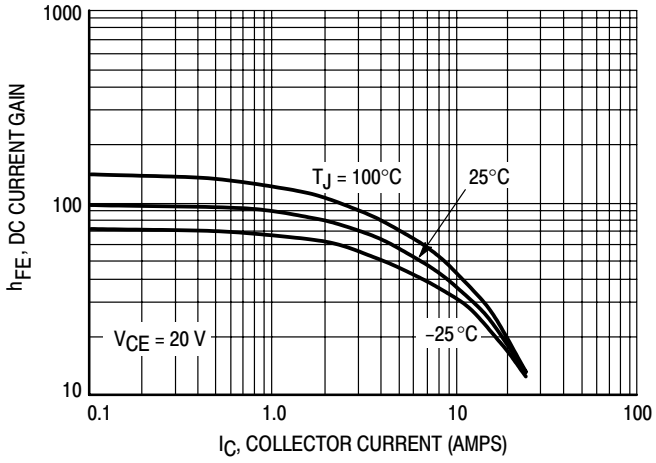


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJ21196

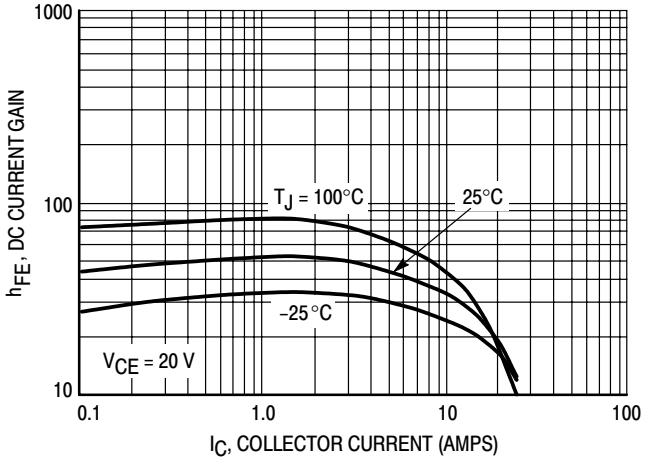


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJ21195

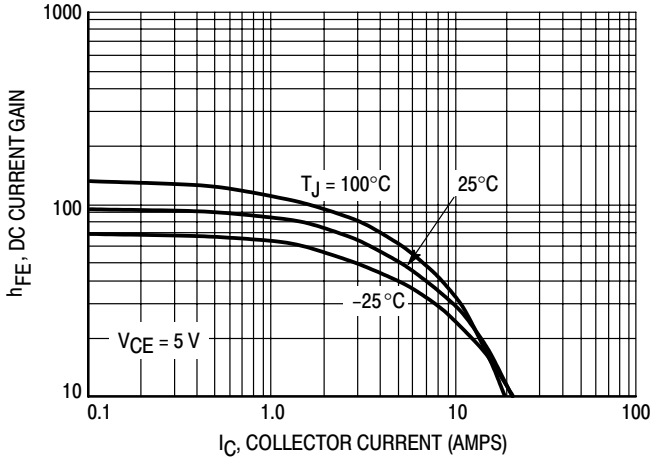


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ21196

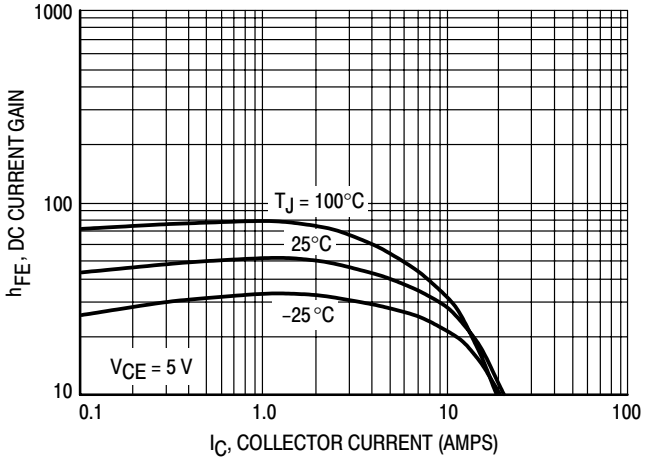


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJ21195

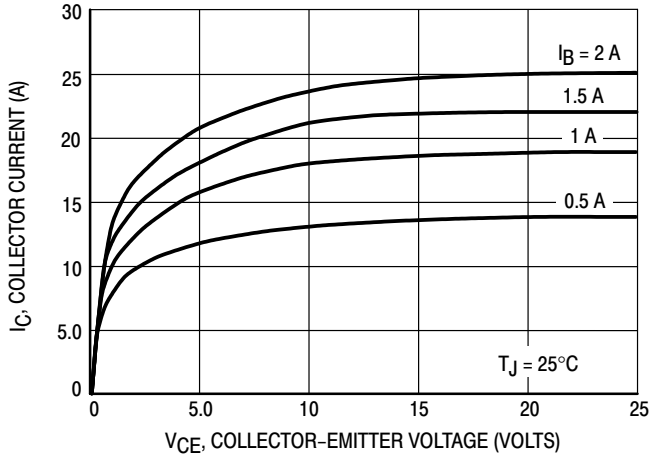


Figure 7. Typical Output Characteristics

NPN MJ21196

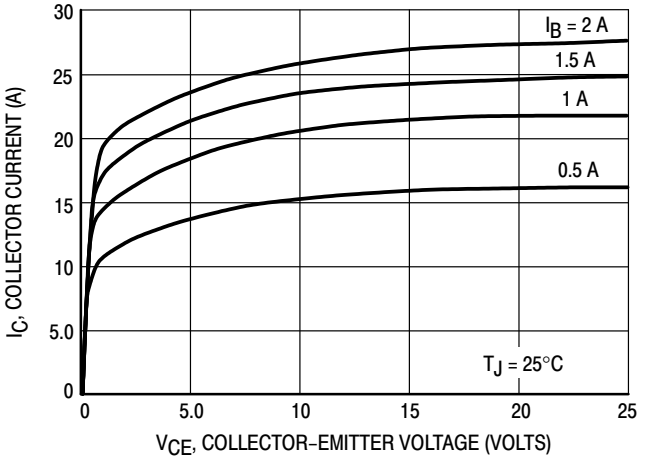


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21195

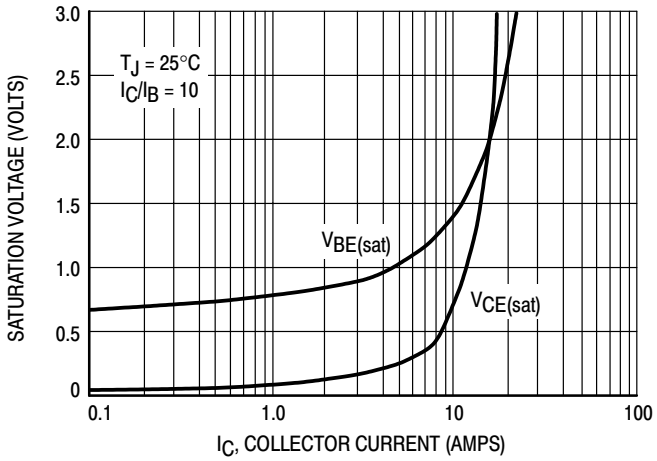


Figure 9. Typical Saturation Voltages

NPN MJ21196

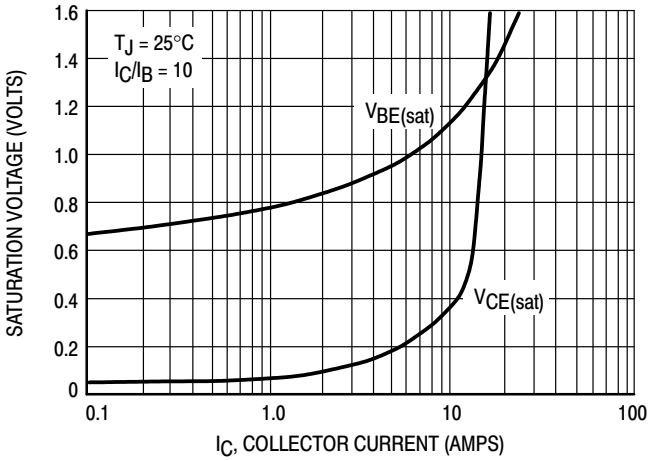


Figure 10. Typical Saturation Voltages

PNP MJ21195

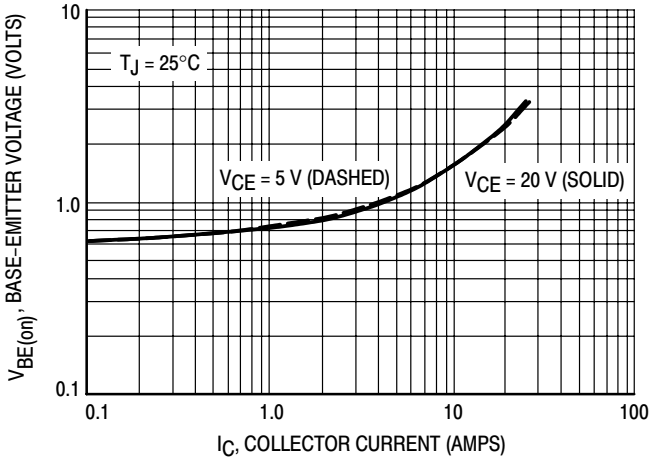


Figure 11. Typical Base−Emitter Voltage

NPN MJ21196

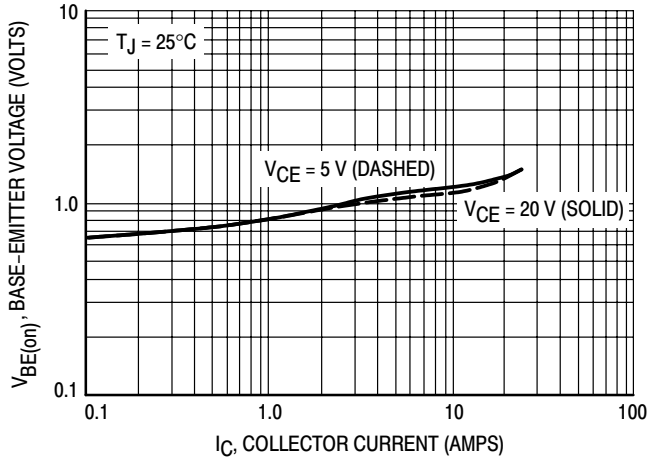


Figure 12. Typical Base−Emitter Voltage

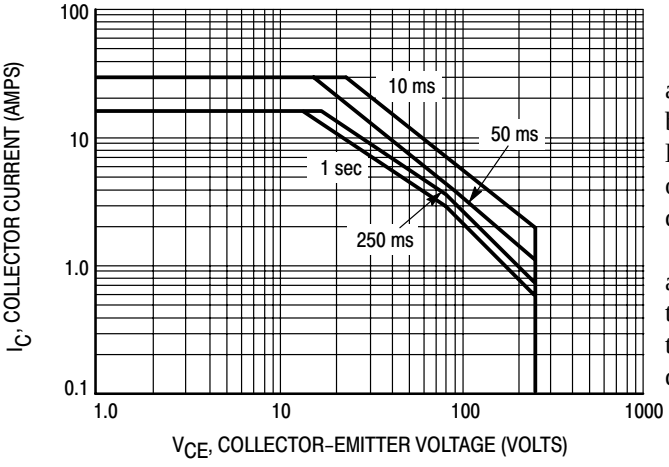


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

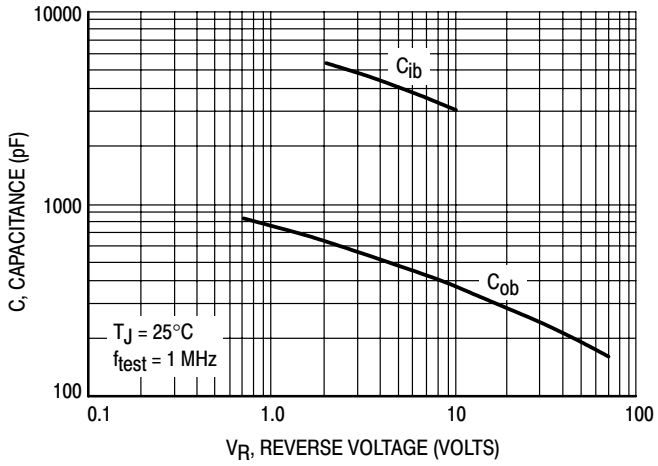


Figure 14. MJ21195 Typical Capacitance

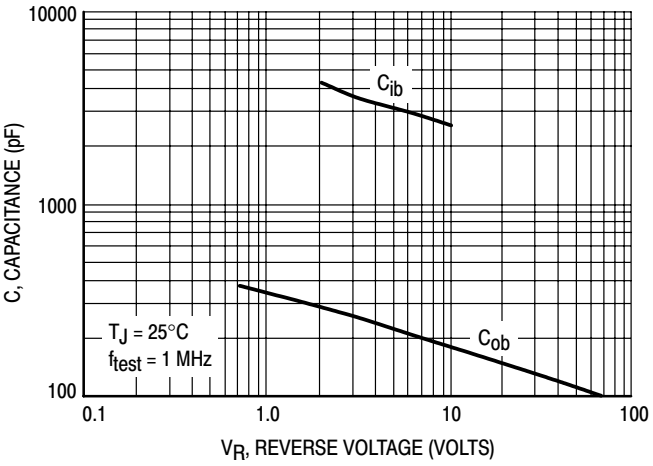


Figure 15. MJ21196 Typical Capacitance

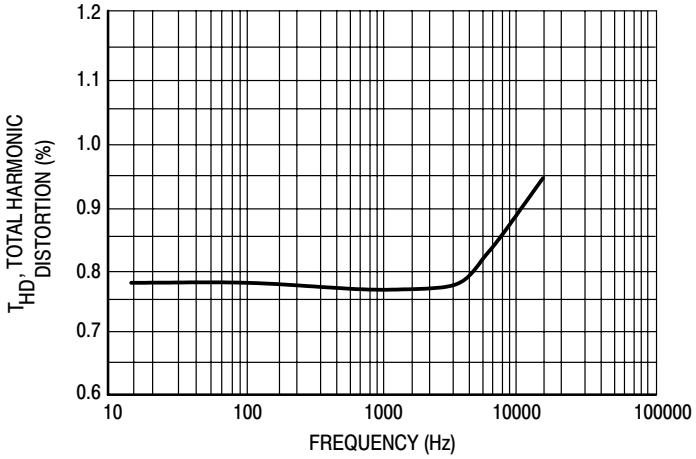


Figure 16. Typical Total Harmonic Distortion

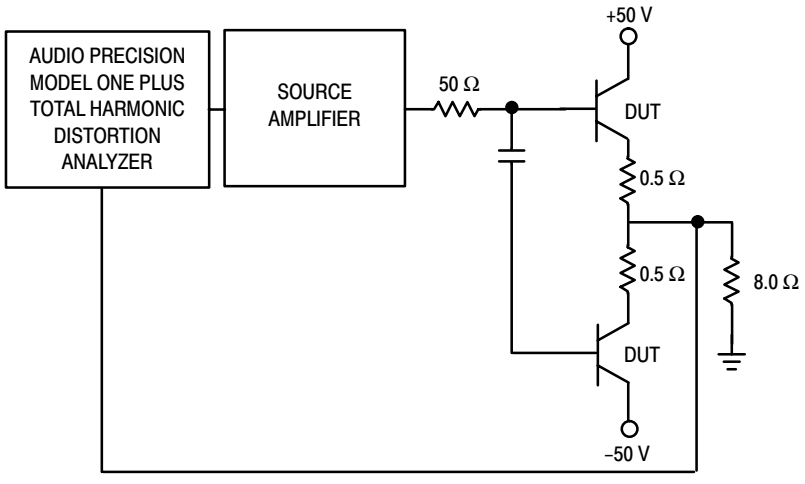


Figure 17. Total Harmonic Distortion Test Circuit

MJ31193 (PNP)
MJ31194 (NPN)

Preferred Devices

Product Preview

Complementary PNP-NPN Silicon Power Transistors

The MJ31193 and MJ31194 are PowerBase™ transistors that are specifically designed for high power audio output.

Features

- High DC Current Gain − h_{FE} = 25 Min @ I_C = 10 A
- Excellent Gain Linearity
- Low Harmonic Distortion
- Ultra High Safe Operation Area

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous − Peak (Note 5)	I_C	20 40	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	300 1.71	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.58	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

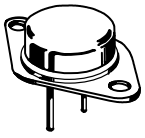
5. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ON Semiconductor®

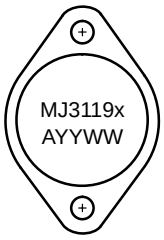
http://onsemi.com

20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 300 WATTS



TO−204 (TO−3)
CASE 197A
STYLE 1

MARKING DIAGRAM



x = 3 or 4
A = Location Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJ31193	TO−204	100 Units/Tray
MJ31194	TO−204	100 Units/Tray

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0 Adc)	I_{CEO}	−	−	100	μAdc
Emitter Cutoff Current (V_{CE} = 5.0 Vdc, I_C = 0 Adc)	I_{EBO}	−	−	10	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	−	−	50	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 20 Adc, I_B = 5.0 Adc)	h_{FE}	 25 10	 − −	 75 −	
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	−	−	1.8	Vdc
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	−	−	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 − −	 0.8 0.08	 − −	%
Current Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	−	−	700	pF

TYPICAL CHARACTERISTICS

PNP MJ31193

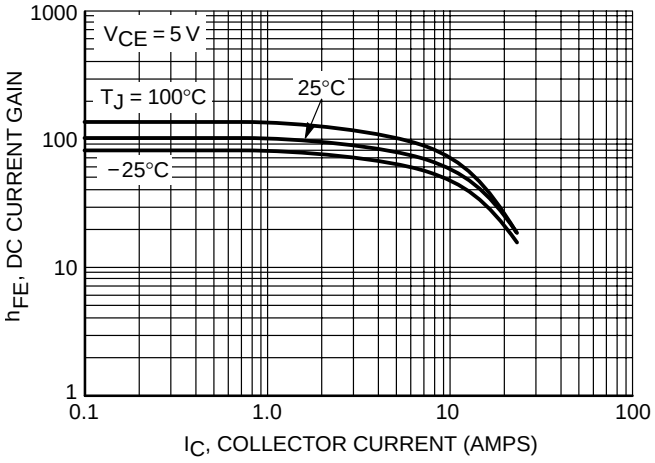


Figure 1. DC Current Gain, V_{CE} = 5 V

NPN MJ31194

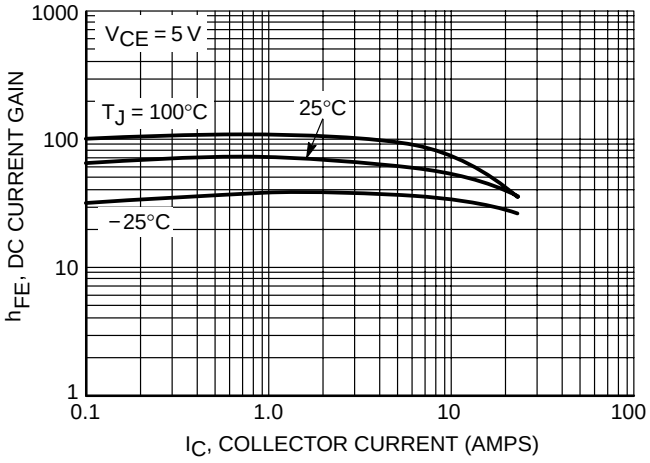


Figure 2. DC Current Gain, V_{CE} = 5 V

PNP MJ31193

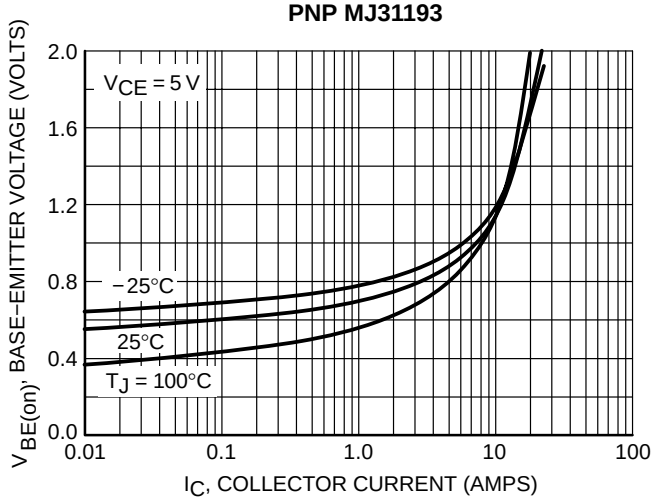


Figure 3. Typical Base−Emitter Voltage

NPN MJ31194

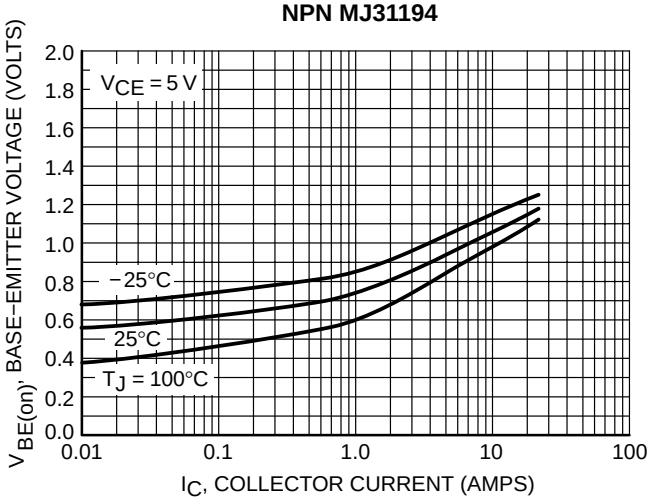


Figure 4. Typical Base−Emitter Voltage

PNP MJ31193

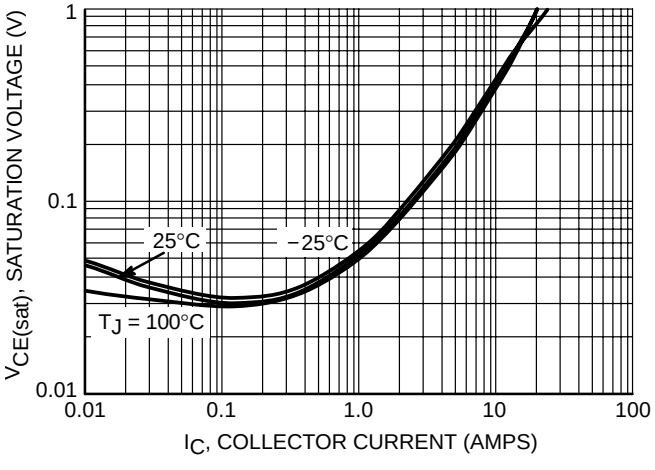


Figure 5. Typical Saturation Voltages

NPN MJ31194

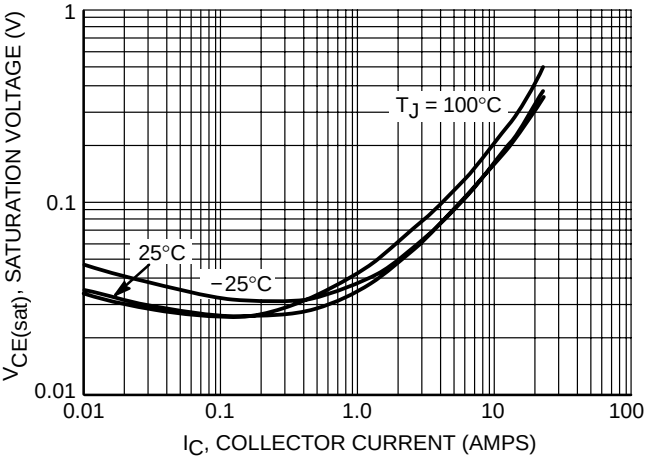


Figure 6. Typical Saturation Voltages

TYPICAL CHARACTERISTICS

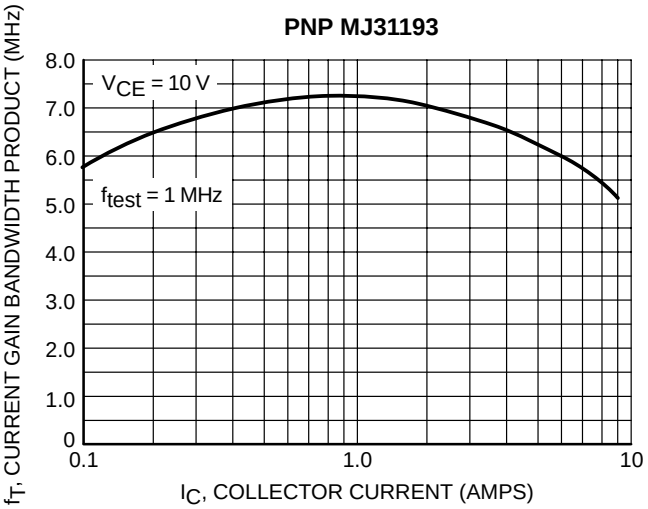


Figure 7. Typical Current Gain Bandwidth Product

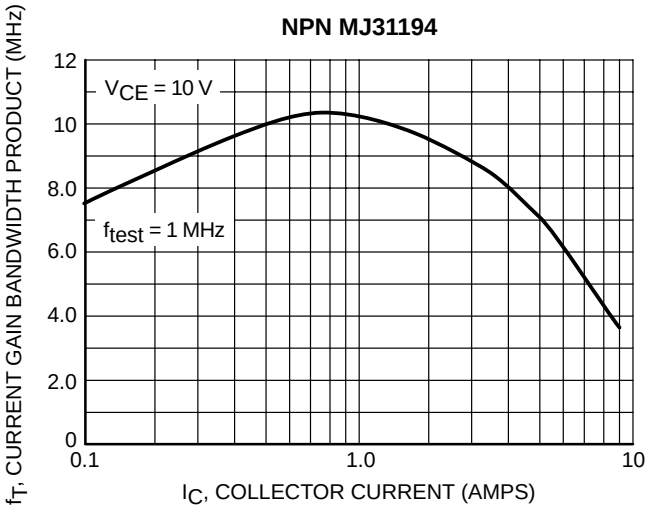


Figure 8. Typical Current Gain Bandwidth Product

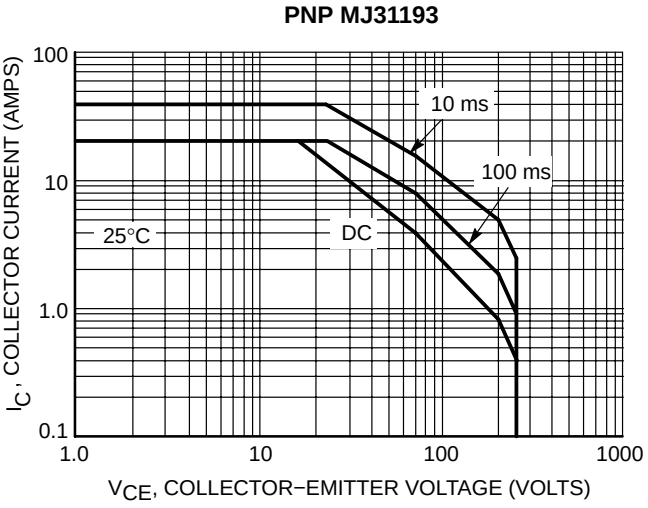


Figure 9. Safe Operating Area

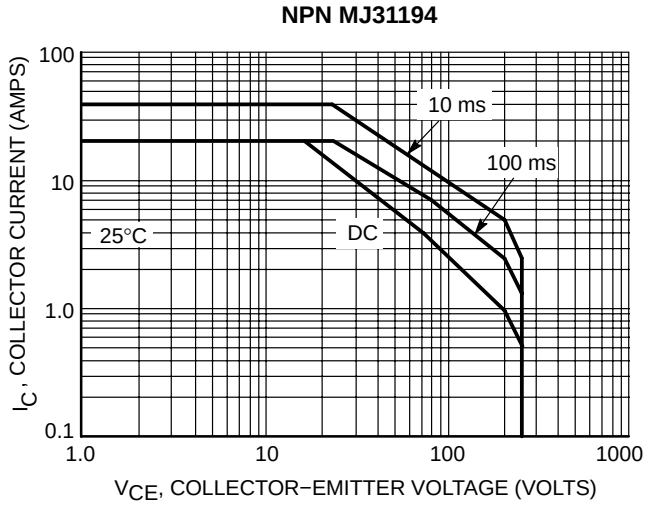


Figure 10. Safe Operating Area

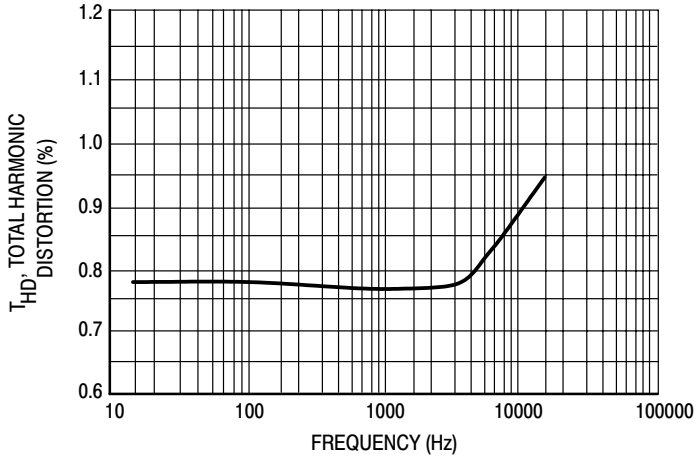


Figure 11. Typical Total Harmonic Distortion

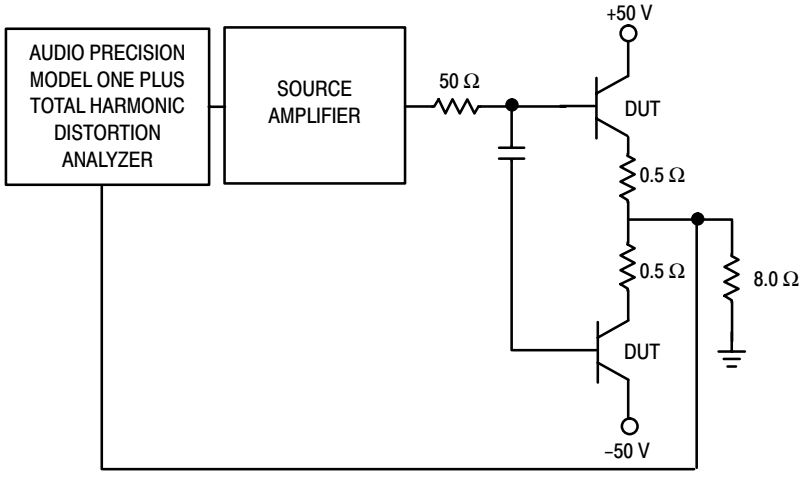


Figure 12. Total Harmonic Distortion Test Circuit

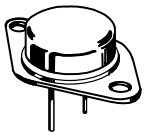
MJ4502

High-Power PNP Silicon Transistor

30 AMPERE
POWER TRANSISTOR
PNP SILICON
100 VOLTS
200 WATTS

. . . for use as an output device in complementary audio amplifiers to 100−Watts music power per channel.

- High DC Current Gain —
  h_{FE} = 25−100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the NPN MJ802



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CER}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Collector−Emitter Voltage	V_{CEO}	90	Vdc
Emitter−Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

MAXIMUM RATINGS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

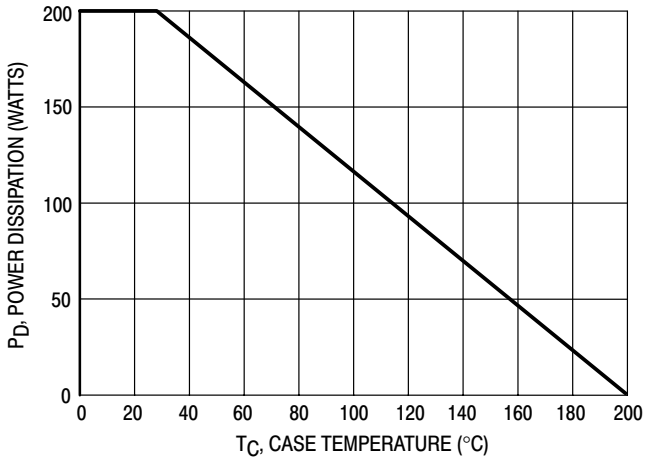


Figure 1. Power−Temperature Derating Curve

April, 2001 − Rev. 9
Publication Order Number:
MJ4502/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage(1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{(BR)CER}$	100	—	Vdc
Collector−Emitter Sustaining Voltage(1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	—	Vdc
Collector−Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter−Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base−Emitter “On” Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Collector−Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base−Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	—	MHz

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

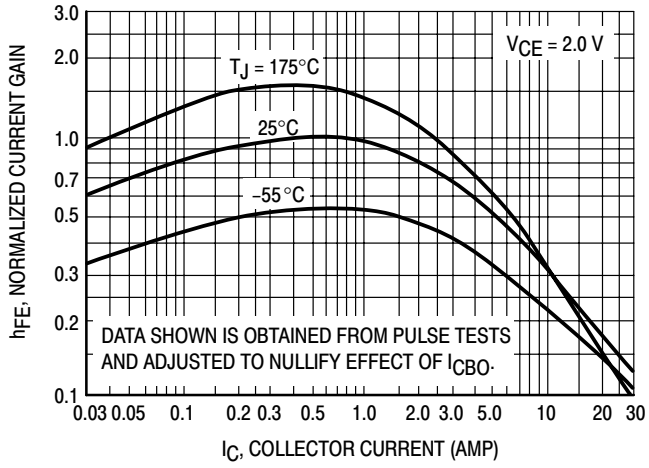


Figure 2. DC Current Gain

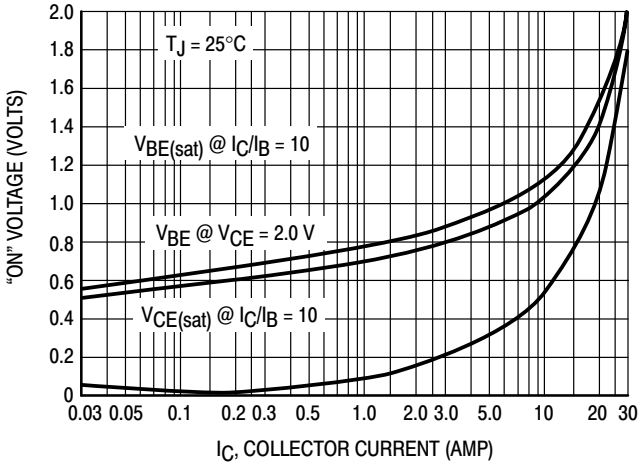


Figure 3. “On” Voltages

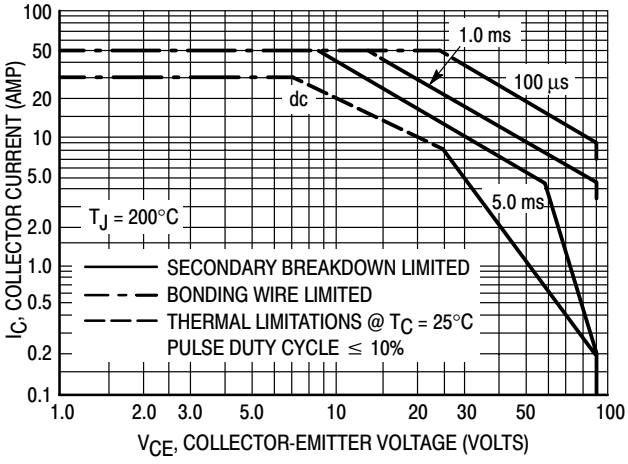


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power−temperature derating must be observed for both steady state and pulse power conditions.

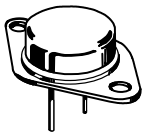
MJ802

High-Power NPN Silicon Transistor

30 AMPERE
POWER TRANSISTOR
NPN SILICON
100 VOLTS
200 WATTS

. . . for use as an output device in complementary audio amplifiers to 100−Watts music power per channel.

- High DC Current Gain —
  h_{FE} = 25−100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502



CASE 1−07
TO−204AA
(TO−3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CER}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Collector−Emitter Voltage	V_{CEO}	90	Vdc
Emitter−Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

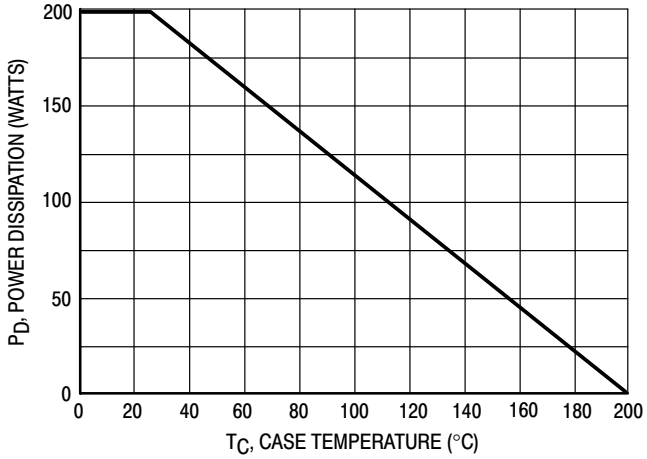


Figure 1. Power−Temperature Derating Curve

Publication Order Number:
M J802/D
April, 2001 − Rev. 9

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage[1] (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	—	Vdc
Collector−Emitter Sustaining Voltage[1] (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	—	Vdc
Collector−Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter−Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain[1] (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base−Emitter “On” Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Collector−Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base−Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	—	MHz

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

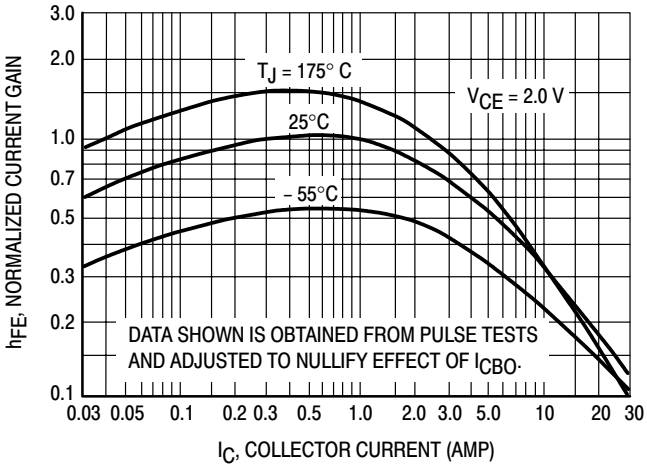


Figure 2. DC Current Gain

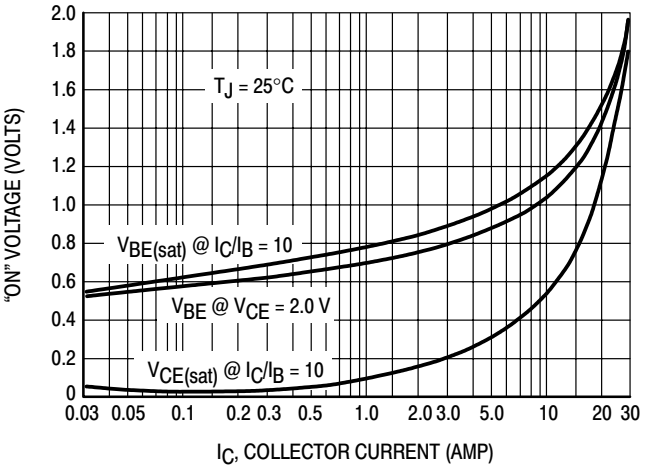


Figure 3. "On" Voltages

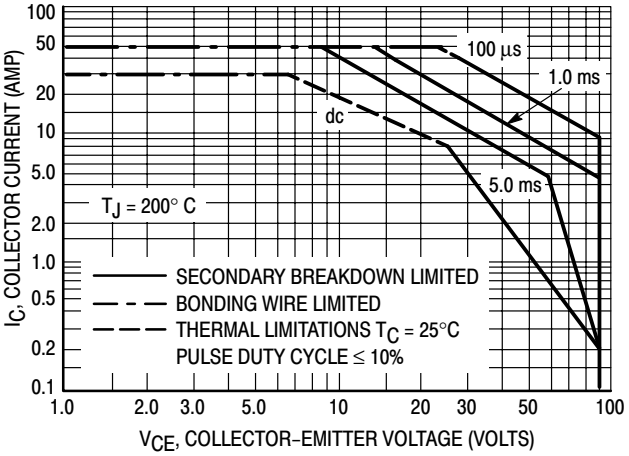


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power temperature derating must be observed for both steady state and pulse power conditions.

MJB41C (NPN), MJB42C (PNP)

Preferred Devices

Complementary Silicon Plastic Power Transistors

D^2PAK for Surface Mount

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape & Reel ("T4" Suffix)
- Electrically the Same as TIP41 and T1P42 Series

ON Semiconductor™

http://onsemi.com

COMPLEMENTARY SILICON POWER TRANSISTORS 6 AMPERES 100 VOLTS 65 WATTS

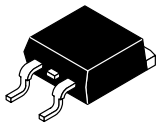
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	6.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Unclamped Inductive Load Energy (Note 1.)	E	62.5	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

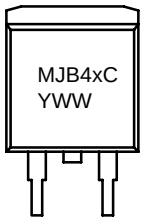
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds	T_L	260	°C

1. I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω
2. When surface mounted to an FR−4 board using the minimum recommended pad size.



D^2PAK
CASE 418B
STYLE 1

MARKING DIAGRAM



MJB4xC = Specific Device Code
x = 1 or 2
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJB41C	D^2PAK	50 Units/Rail
MJB41CT4	D^2PAK	800/Tape & Reel
MJB42C	D^2PAK	50 Units/Rail
MJB42CT4	D^2PAK	800/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 6) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	−	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	−	100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	50	μAdc
ON CHARACTERISTICS (Note 6)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	30 15	− 75	−
Collector−Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	−	1.5	Vdc
Base−Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	−	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	3.0	−	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	−	−

6. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

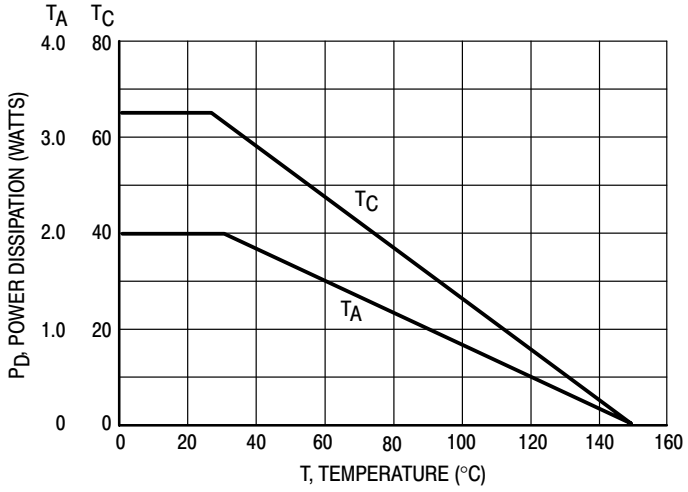
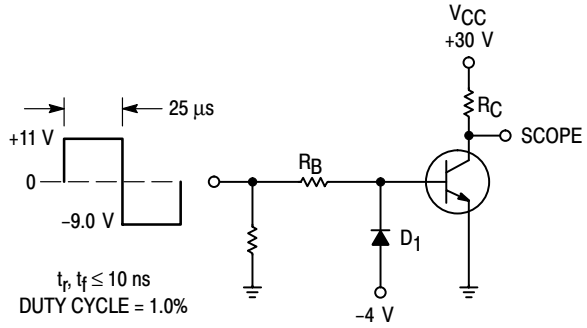


Figure 5. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Figure 6. Switching Time Test Circuit

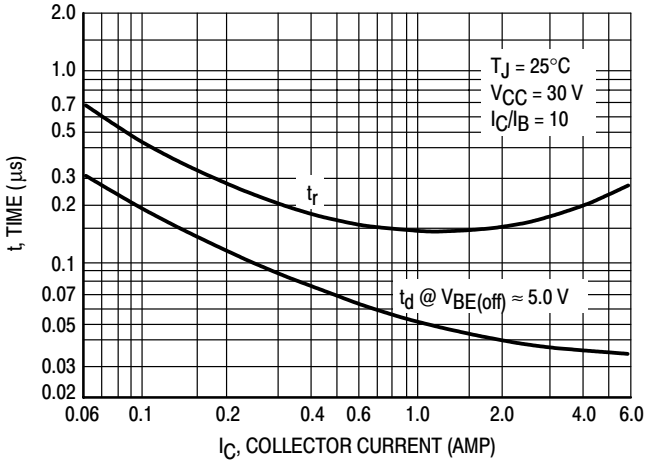


Figure 7. Turn−On Time

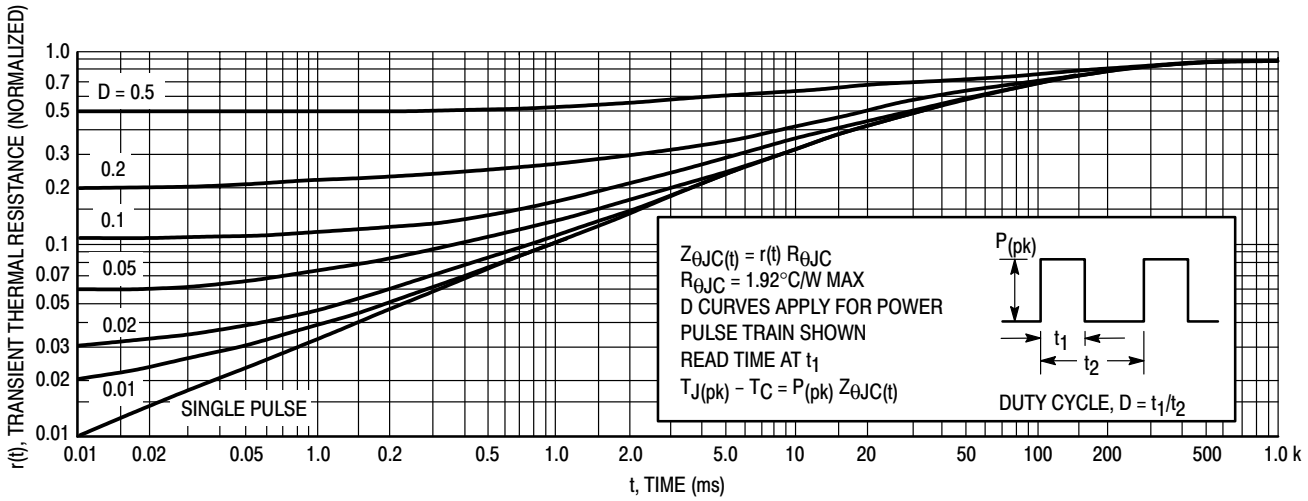


Figure 8. Thermal Response

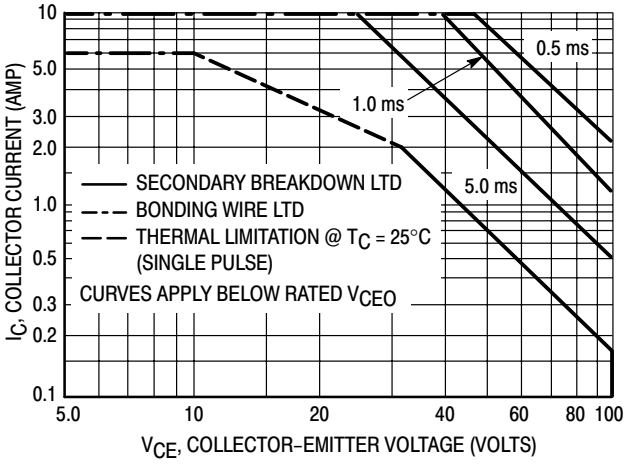


Figure 9. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

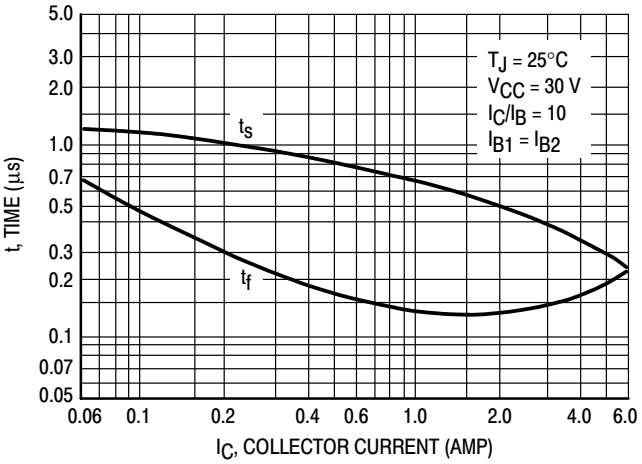


Figure 10. Turn−Off Time

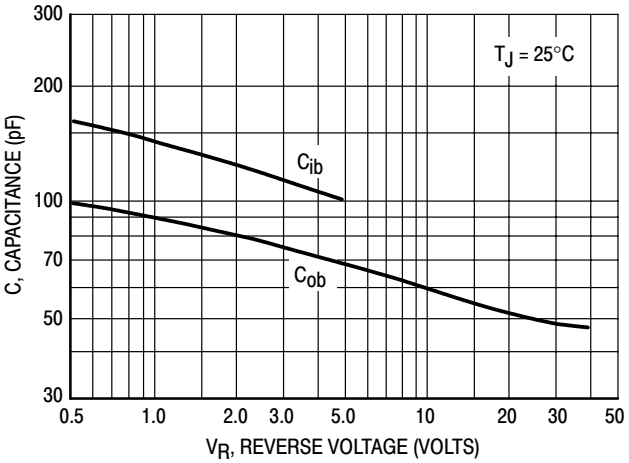


Figure 11. Capacitance

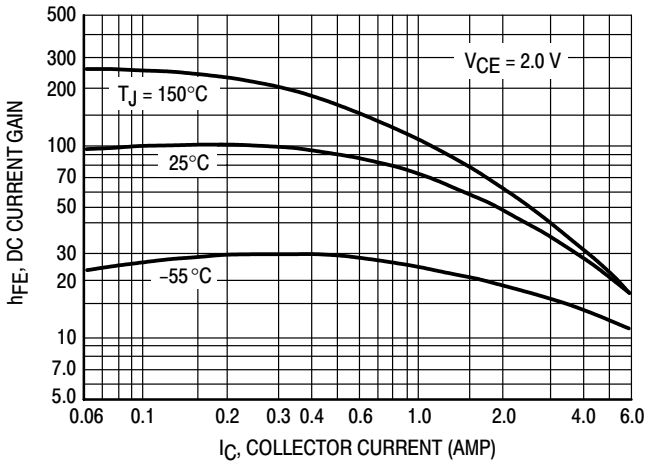


Figure 12. DC Current Gain

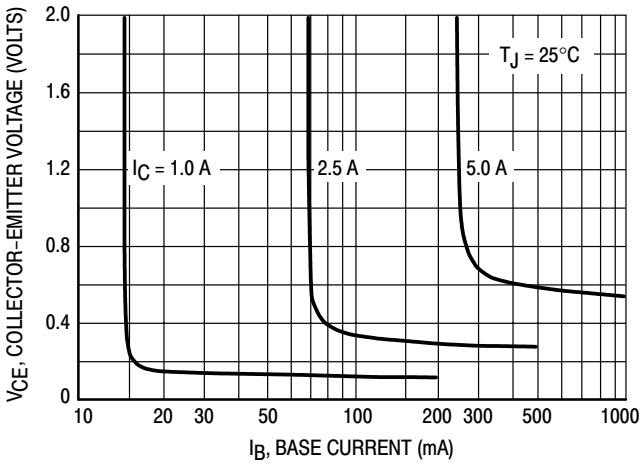


Figure 13. Collector Saturation Region

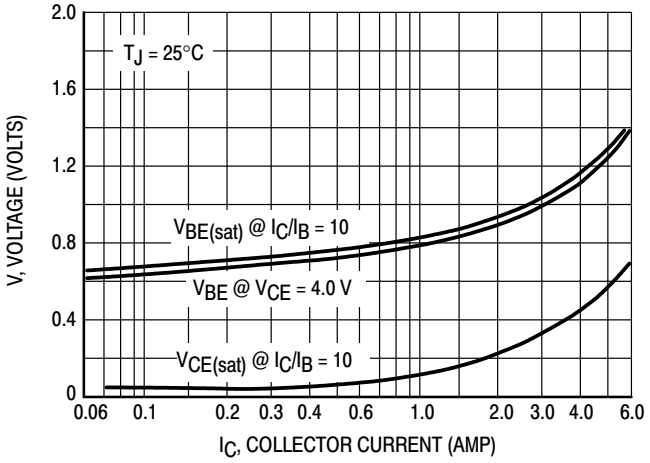


Figure 14. “On” Voltages

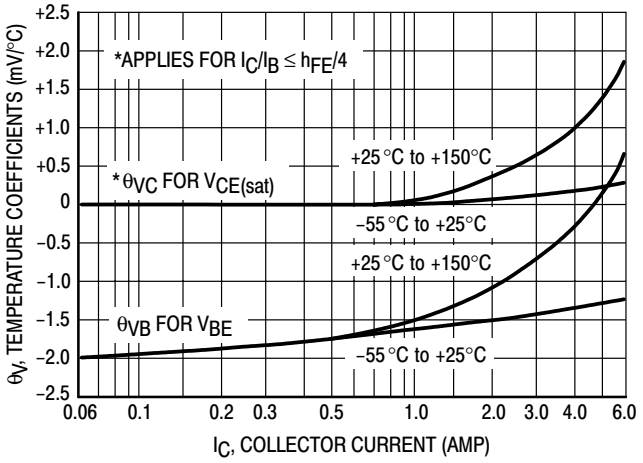


Figure 15. Temperature Coefficients

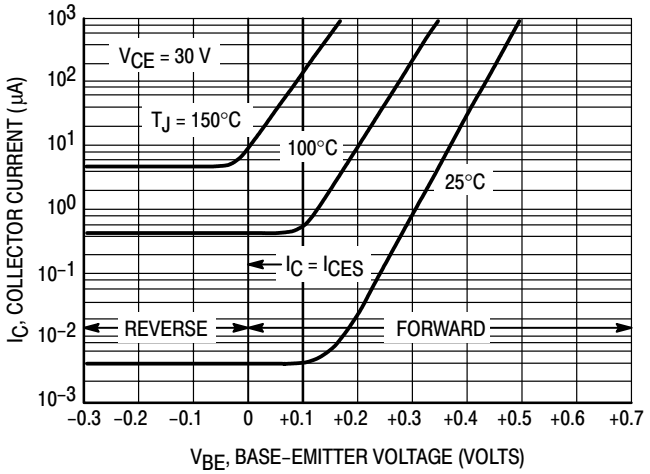


Figure 16. Collector Cut−Off Region

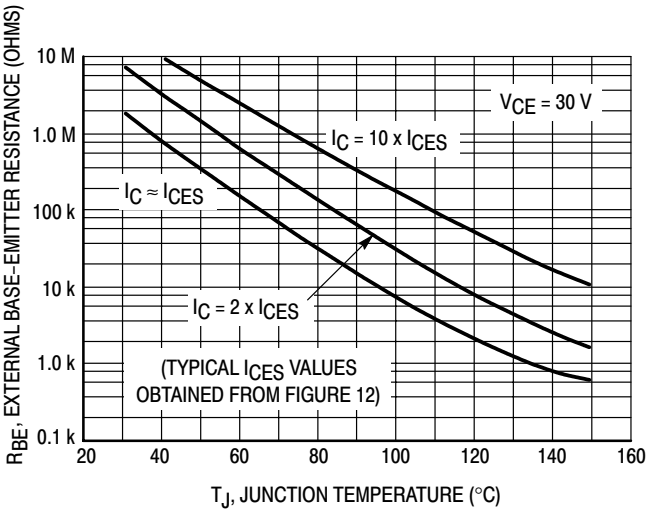
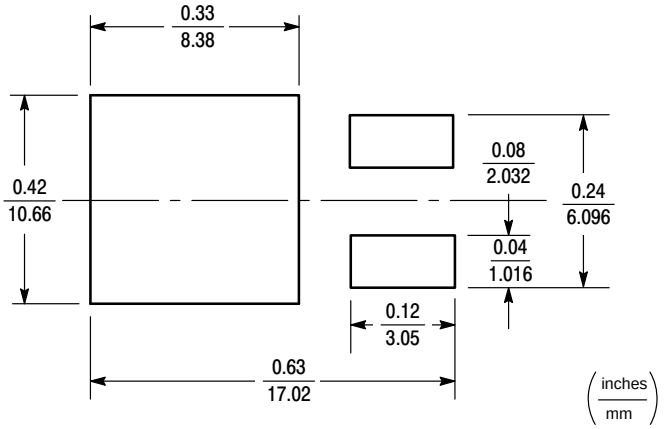


Figure 17. Effects of Base−Emitter Resistance

INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus Collector pad area is shown in Figure 18

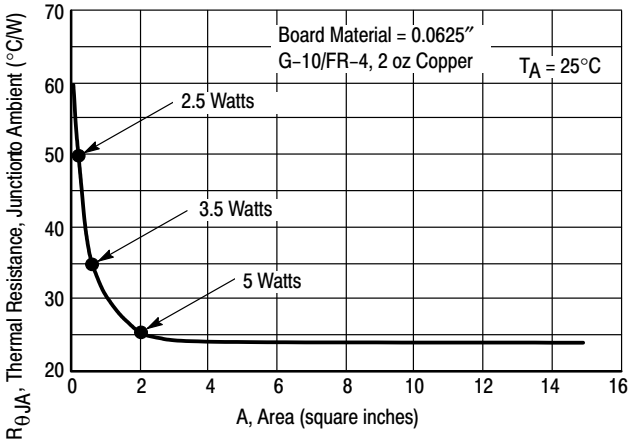


Figure 18. Thermal Resistance versus Collector Pad Area for the D²PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC−59, SC−70/SOT−323, SOD−123, SOT−23, SOT−143, SOT−223, SO−8, SO−14, SO−16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 19 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

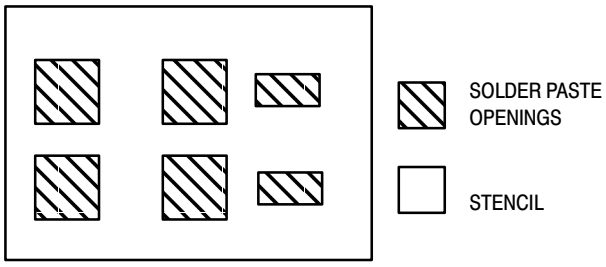


Figure 19. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* * Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 20 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

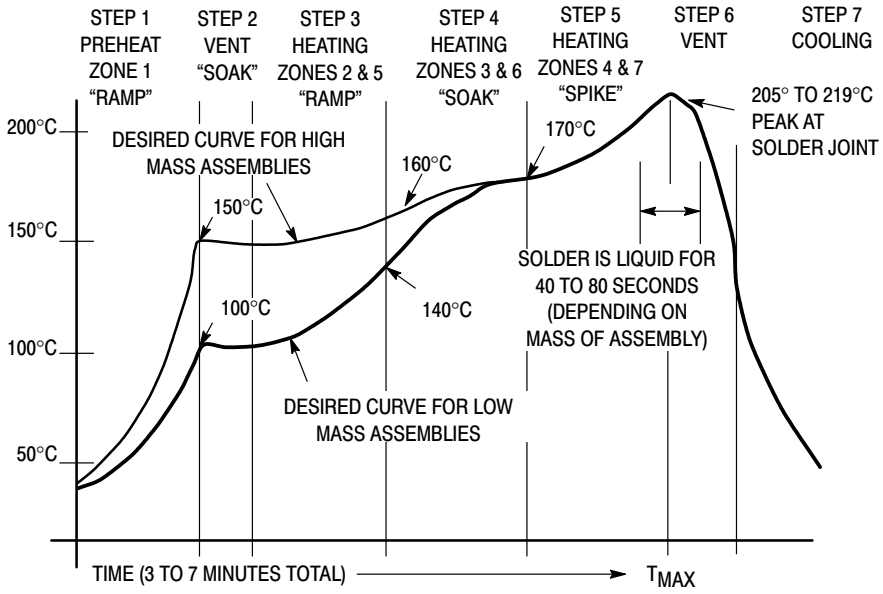


Figure 20. Typical Solder Heating Profile

MJB6488, MJB6491

Product Preview

Complementary Silicon Plastic Power Transistors

. . . designed for use in general−purpose amplifier and switching applications.

- DC Current Gain Specified to 15 A −
  h_{FE}= 20 − 150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 80 Vdc (Min)
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model; 3B, >8000 V,
  Machine Model; C, >400 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CB}	90	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.8 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	70	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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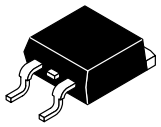
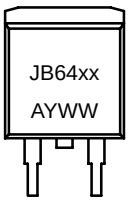
15 A
COMPLEMENTARY SILICON POWER TRANSISTORS
80 V, 75 W



D²PAK
CASE 418B
STYLE 1

MARKING DIAGRAM



xx = 88 or 91
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJB6488	D²PAK	50 Units / Rail
MJB6488T4	D²PAK	800 / Tape & Reel
MJB6491	D²PAK	50 Units / Rail
MJB6491T4	D²PAK	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1)	(I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	−	Vdc
Collector−Emitter Sustaining Voltage (Note 1)	(I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	VCEX	90	−	Vdc
Collector Cutoff Current	(V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	−	1.0	mAdc
Collector Cutoff Current	(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	− −	100 5.0	μAdc mAdc
Emitter Cutoff Current	(V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	10	μA
ON CHARACTERISTICS					
DC Current Gain	(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	150 −	−
Collector−Emitter Saturation Voltage	(I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 15 Adc, I_B = 5.0 Adc)	$V_{CE(sat)}$	− −	1.3 3.5	Vdc
Base−Emitter On Voltage	(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	− −	1.3 3.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 2)	(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)	f_T	5.0	−	MHz
Small−Signal Current Gain	(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	−	−

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

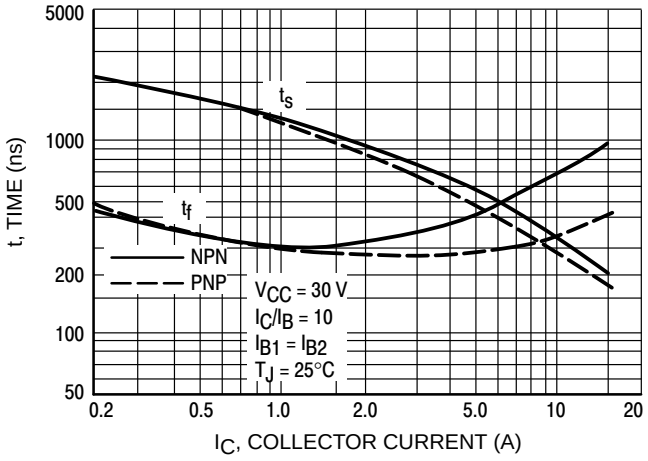


Figure 21. Turn−Off Time

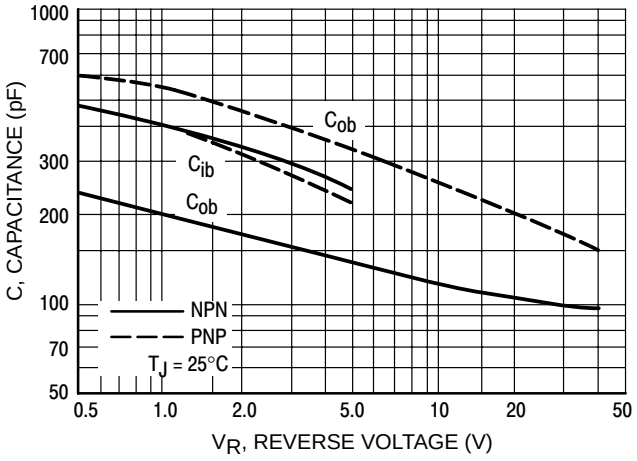


Figure 22. Capacitances

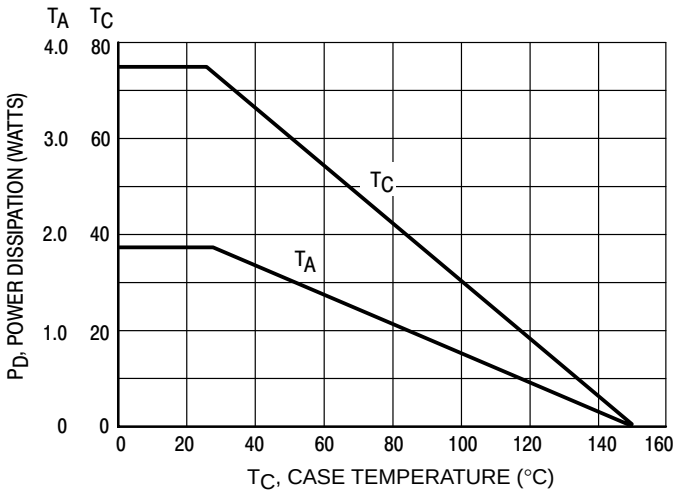
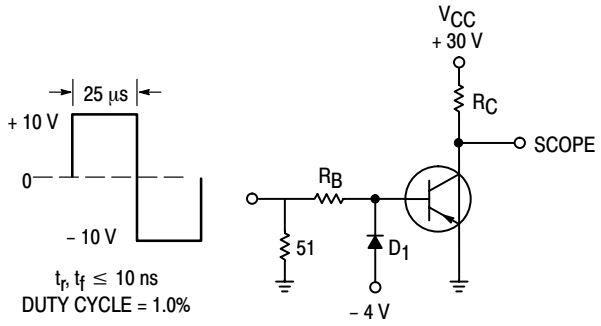


Figure 23. Power Derating



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.
FOR PNP, REVERSE ALL POLARITIES.

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Figure 24. Switching Time Test Circuit

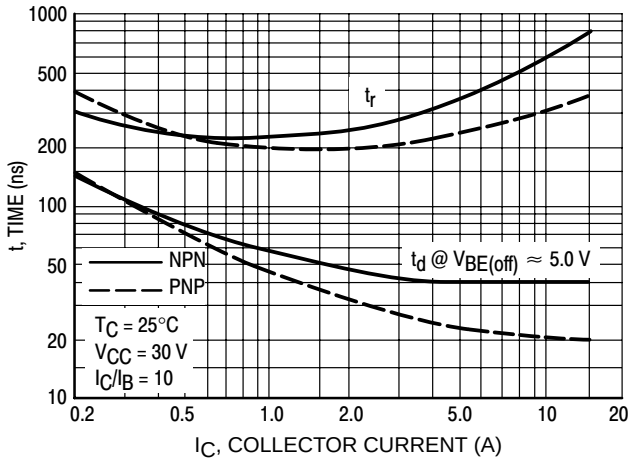


Figure 25. Turn−On Time

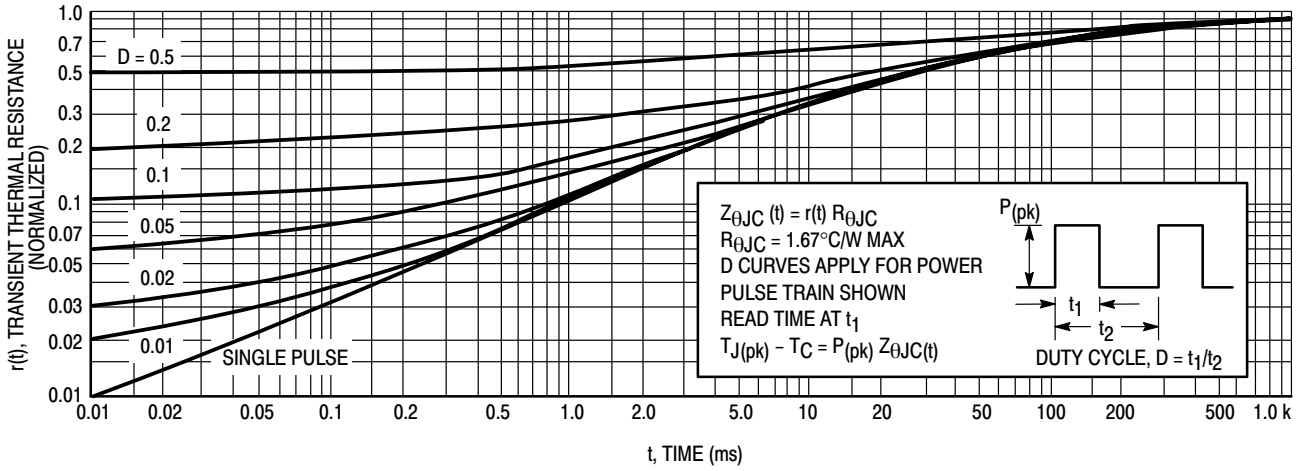


Figure 26. Thermal Response

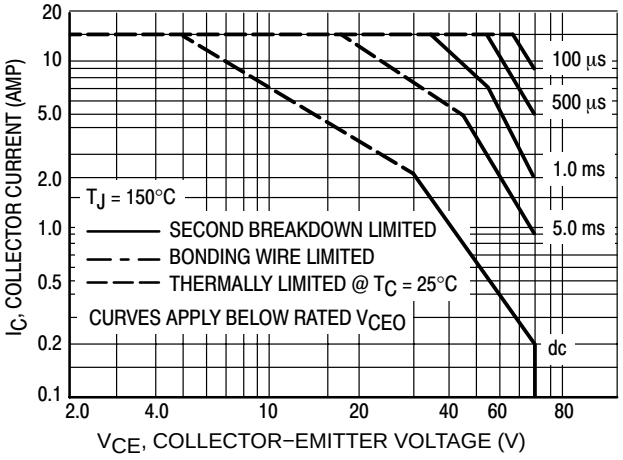


Figure 27. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 27 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 26. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

NPN − MJB6488 **PNP − MJB6491**

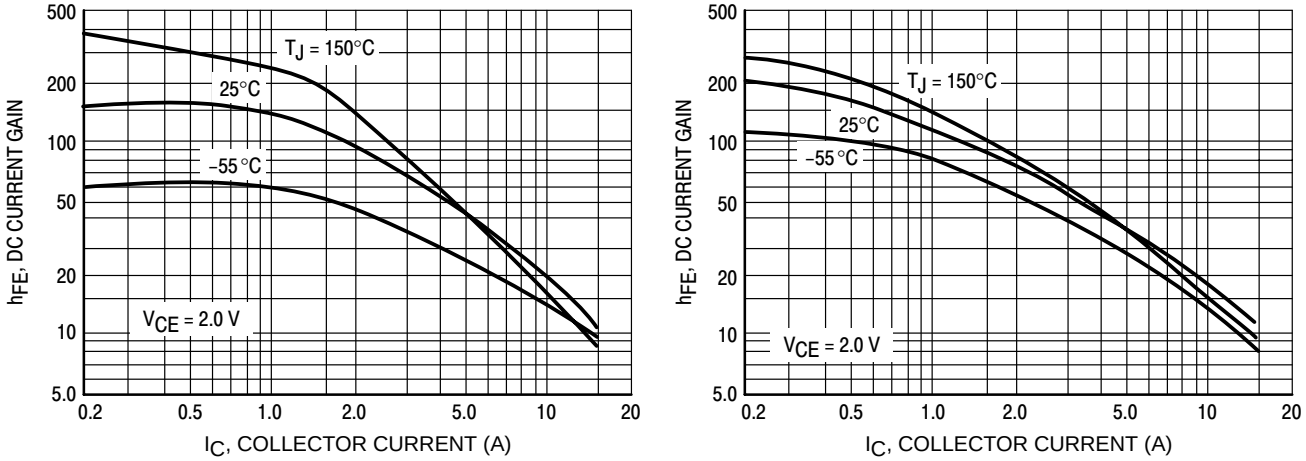


Figure 28. DC Current Gain

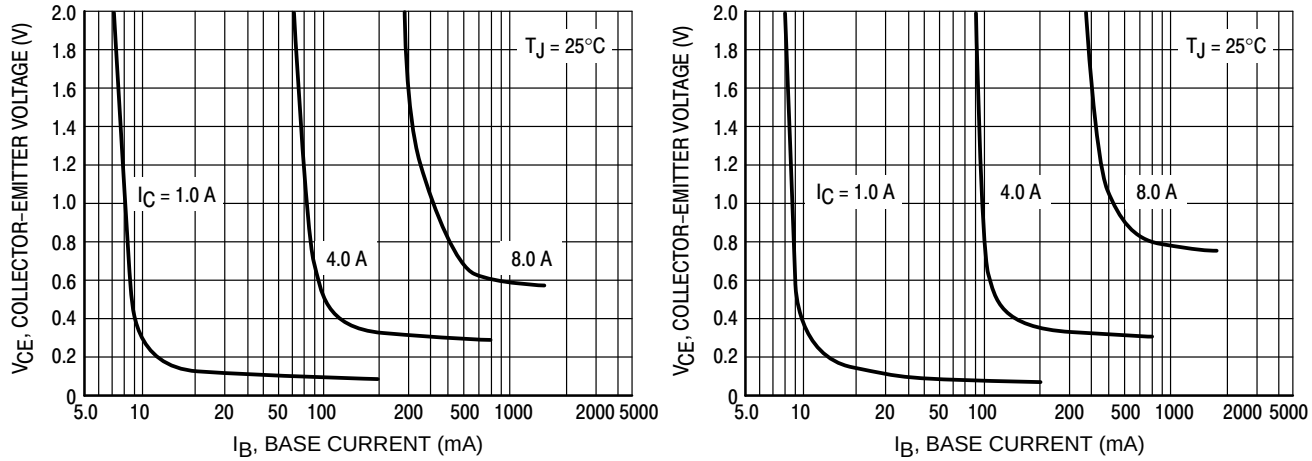


Figure 29. Collector Saturation Region

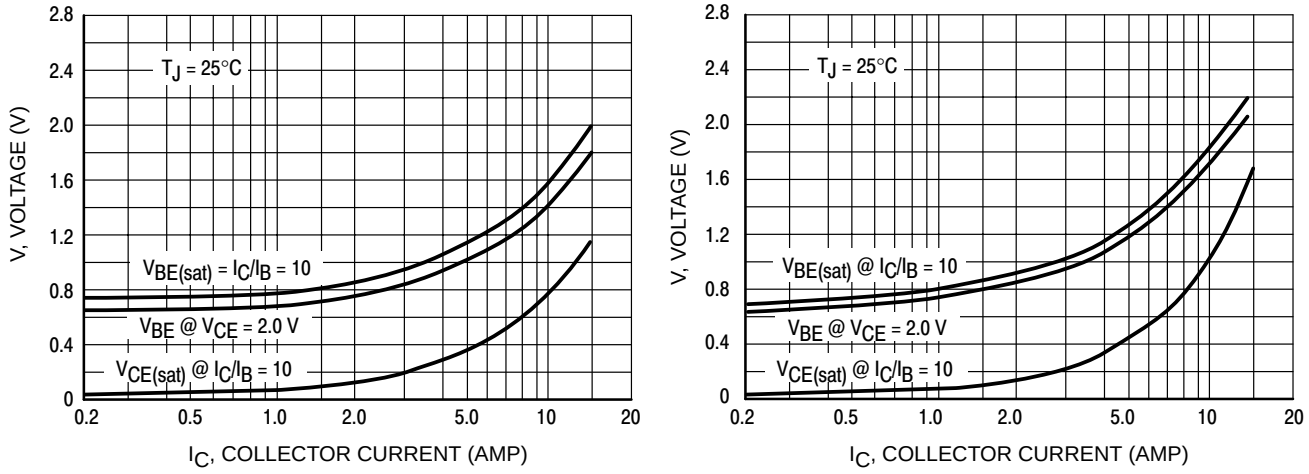


Figure 30. “On” Voltages

MJD112 (NPN)
MJD117 (PNP)

Preferred Device

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

Features

- Pb−Free Packages are Available
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” and “RL” Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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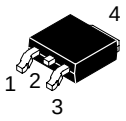
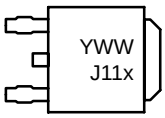
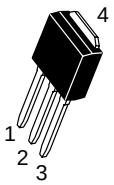
SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS
20 WATTS

MARKING DIAGRAMS

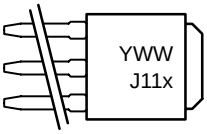


DPAK
CASE 369C





DPAK−3
CASE 369D



Y = Year
WW = Work Week
x = 2 or 7

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 405 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	−	20	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	−	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	2	mAdc
Collector−Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	−	10	μAdc
Emitter−Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 2 Adc, V_{CE} = 3 Vdc) (I_C = 4 Adc, V_{CE} = 3 Vdc)	h_{FE}	 500 1000 200	 − 12,000 −	−
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc) (I_C = 4 Adc, I_B = 40 mAdc)	$V_{CE(sat)}$	 − −	 2 3	Vdc
Base−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	−	4	Vdc
Base−Emitter On Voltage (I_C = 2 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	−	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	25	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD117 MJD112	C_{ob}	 − −	 200 100	pF

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD112	DPAK	369C	75 Units / Rail
MJD112−001	DPAK−3	369D	75 Units / Rail
MJD112RL	DPAK	369C	1800 Tape & Reel
MJD112T4	DPAK	369C	2500 Tape & Reel
MJD112T4G	DPAK (Pb−Free)	369C	2500 Tape & Reel
MJD117	DPAK	369C	75 Units / Rail
MJD117G	DPAK (Pb−Free)	369C	75 Units / Rail
MJD117−001	DPAK−3	369D	75 Units / Rail
MJD117T4	DPAK	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

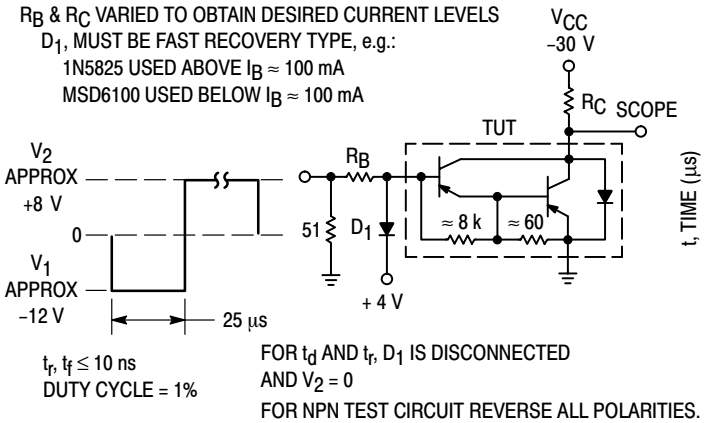


Figure 31. Switching Times Test Circuit

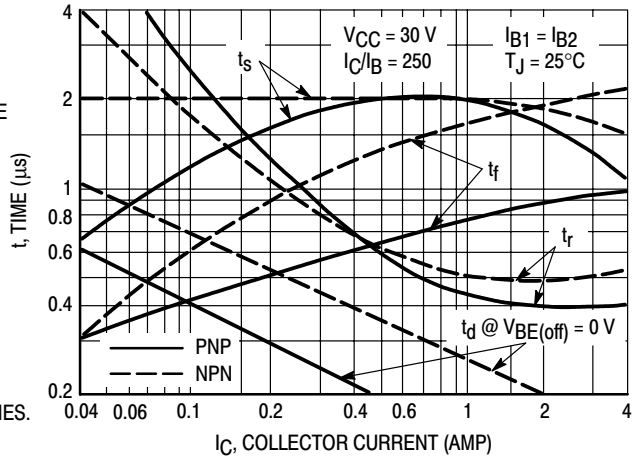


Figure 32. Switching Times

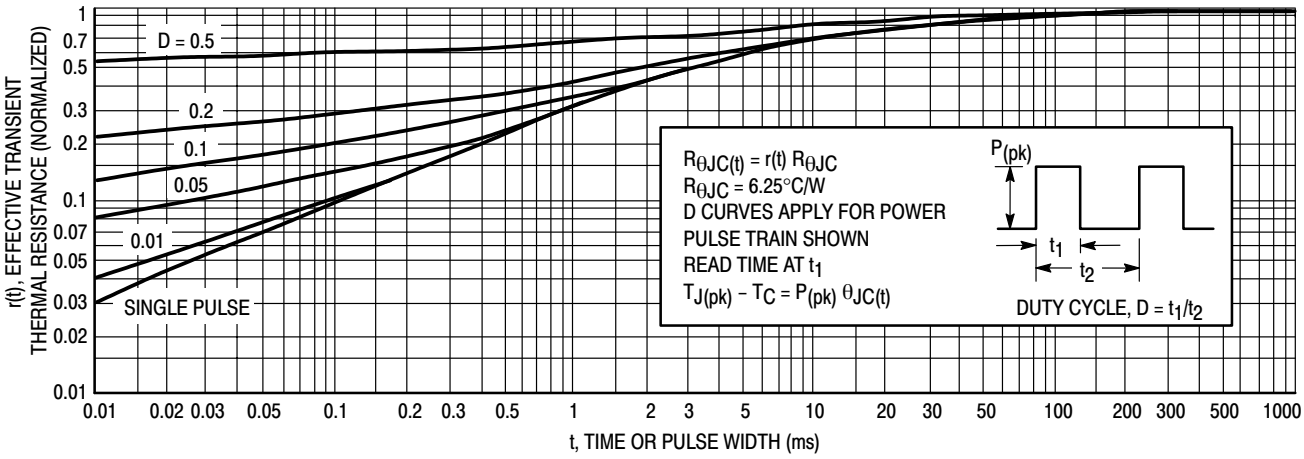


Figure 33. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

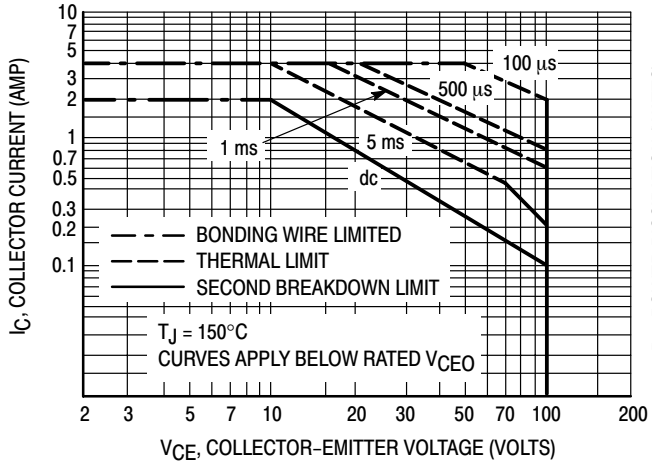


Figure 34. Maximum Rated Forward Biased Safe Operating Area

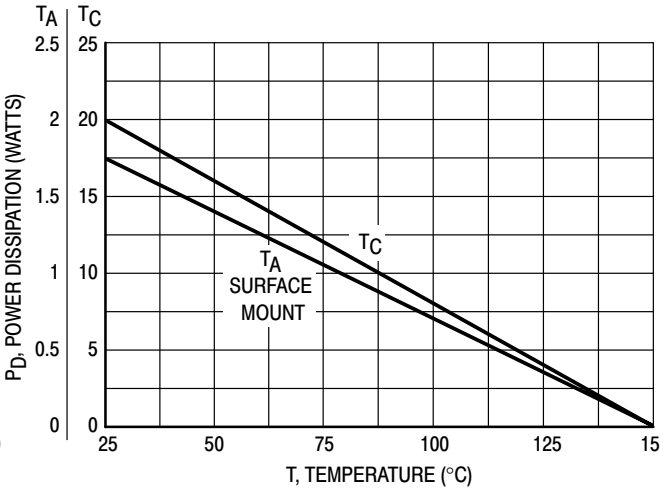


Figure 35. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 35 and 36 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

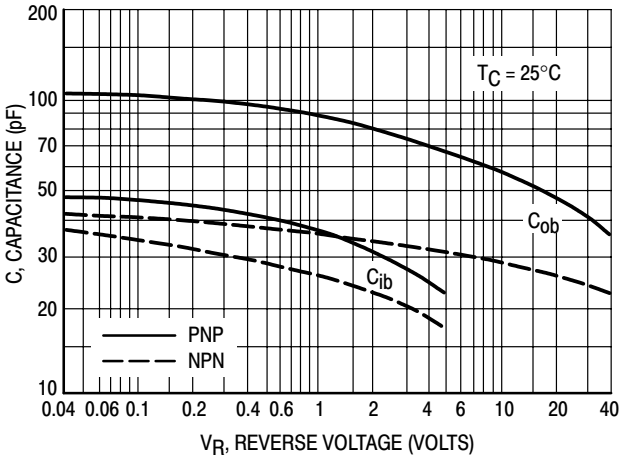


Figure 36. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

NPN MJD112 **PNP MJD117**

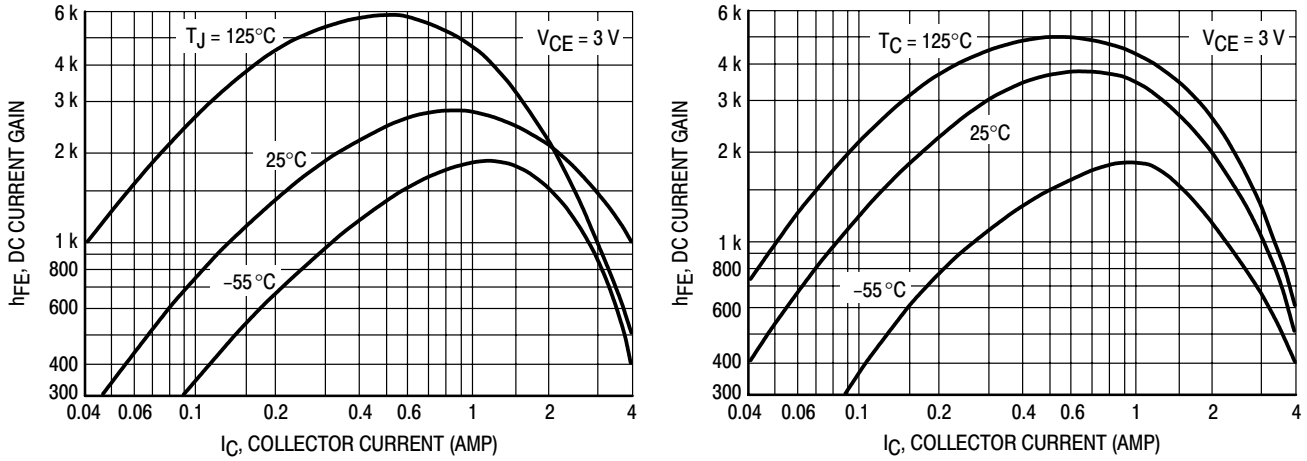


Figure 37. DC Current Gain

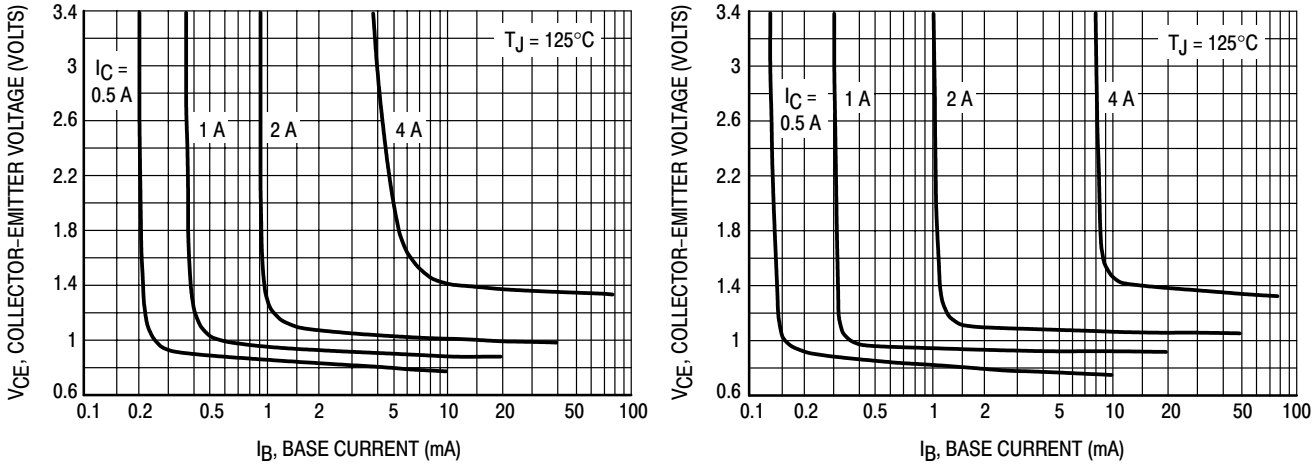


Figure 38. Collector Saturation Region

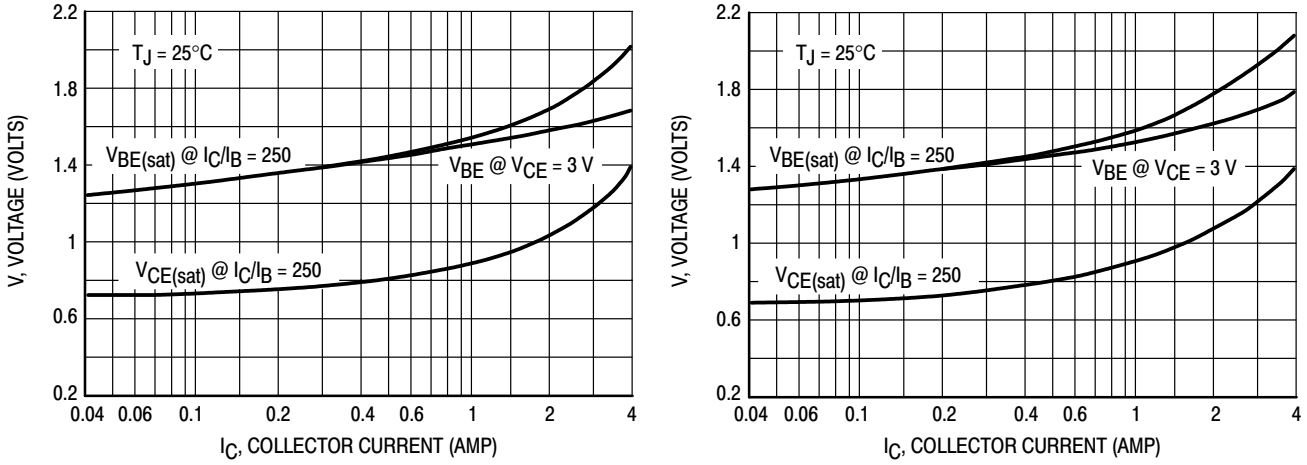


Figure 39. “On Voltages

NPN MJD112 **PNP MJD117**

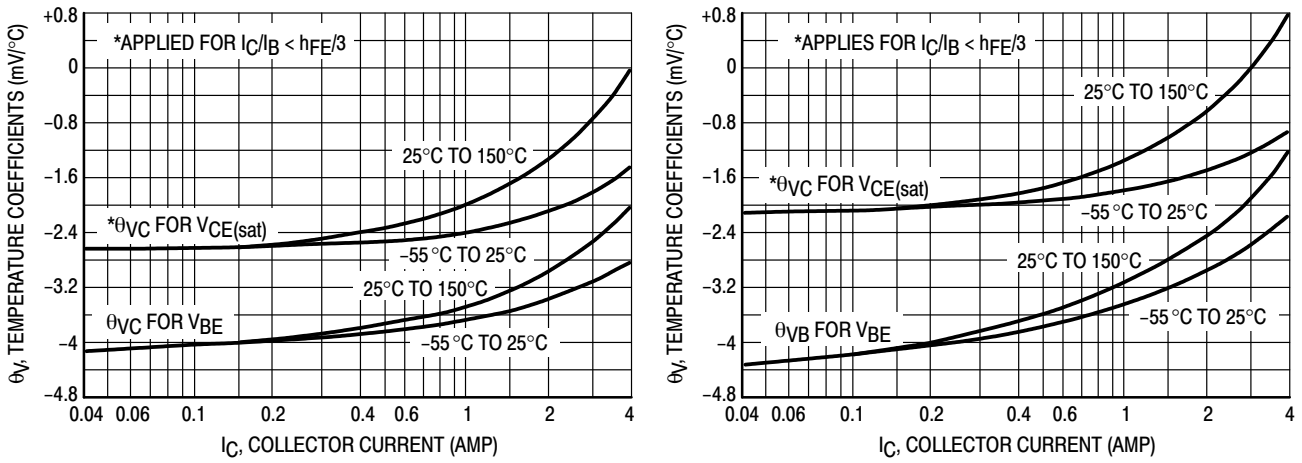


Figure 40. Temperature Coefficients

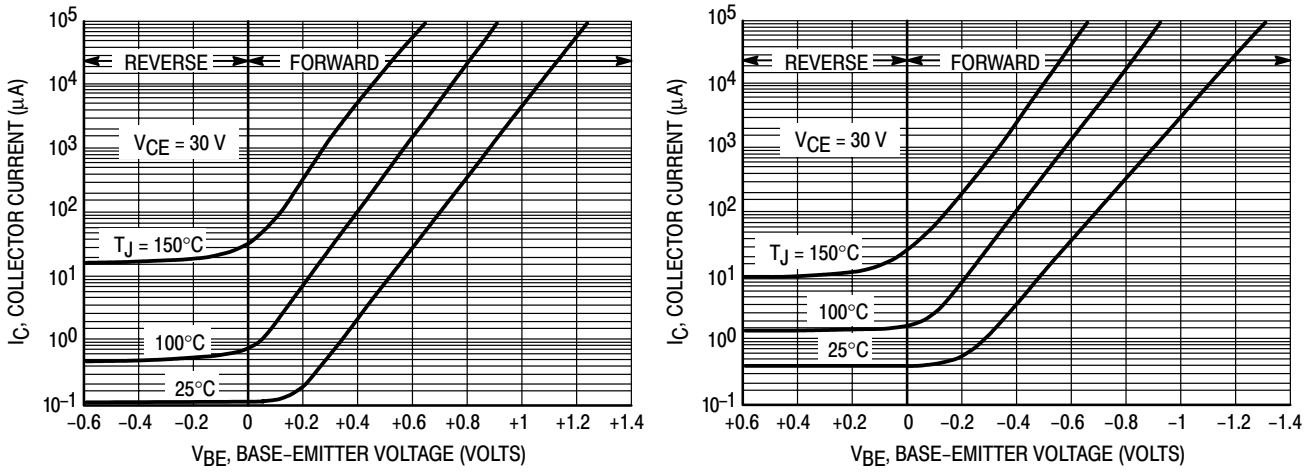


Figure 41. Collector Cut−Off Region

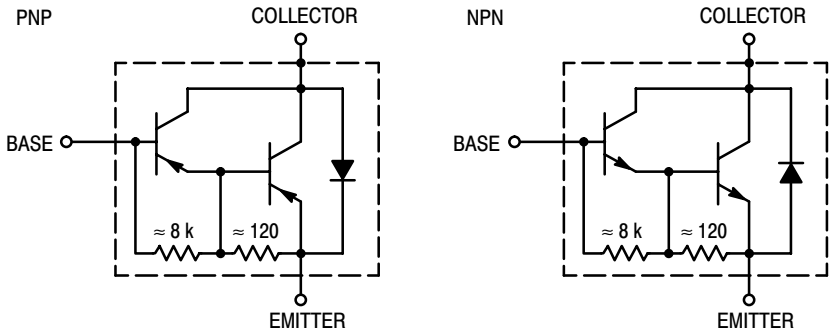


Figure 42. Darlington Schematic

MJD122 (NPN)
MJD127 (PNP)

Preferred Device

Complementary Darlington Power Transistor

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

- Pb−Free Packages are Available
- Lead Formed for Surface Mount Applications in Plastic Sleeves
- Available in 16 mm Tape and Reel (“T4” Suffix)
- Surface Mount Replacements for 2N6040−2N6045 Series, TIP120−TIP122 Series, and TIP125−TIP127 Series
- Monolithic Construction With Built−in Base−Emitter Shunt Resistors
- High DC Current Gain − h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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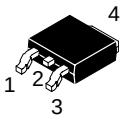
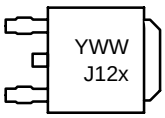
SILICON POWER TRANSISTOR 8 AMPERES 100 VOLTS 20 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week
x = 2 or 7

ORDERING INFORMATION

Device	Package	Shipping†
MJD122	DPAK	75 Units/Rail
MJD122T4	DPAK	2500/Tape & Reel
MJD122T4G	DPAK (Pb−Free)	2500/Tape & Reel
MJD127	DPAK	75 Units/Rail
MJD127G	DPAK (Pb−Free)	75 Units/Rail
MJD127T4	DPAK	2500/Tape & Reel
MJD127T4G	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	−	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	−	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 8 Adc, V_{CE} = 4 Vdc)	h_{FE}	1000 100	12,000 −	−
Collector−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 16 mAdc) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	− −	2 4	Vdc
Base−Emitter Saturation Voltage (Note 1) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	−	4.5	Vdc
Base−Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	−	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain−Bandwidth Product (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	$\|h_{fe}\|$	4	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD127 MJD122	C_{ob}	− −	300 200	pF
Small−Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	300	−	−

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

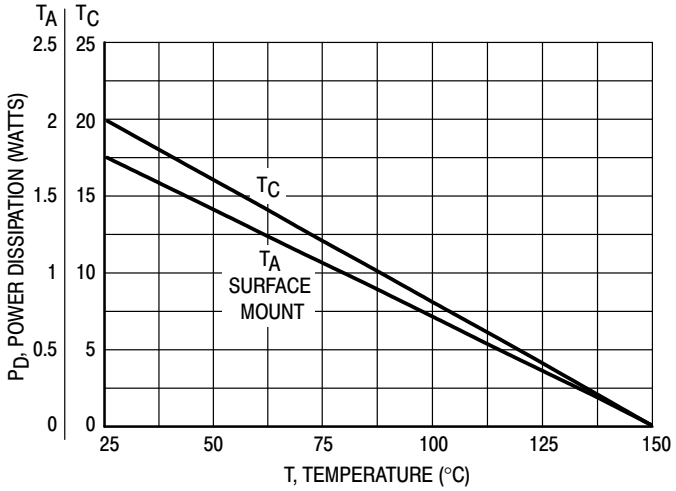


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127 **NPN MJD122**

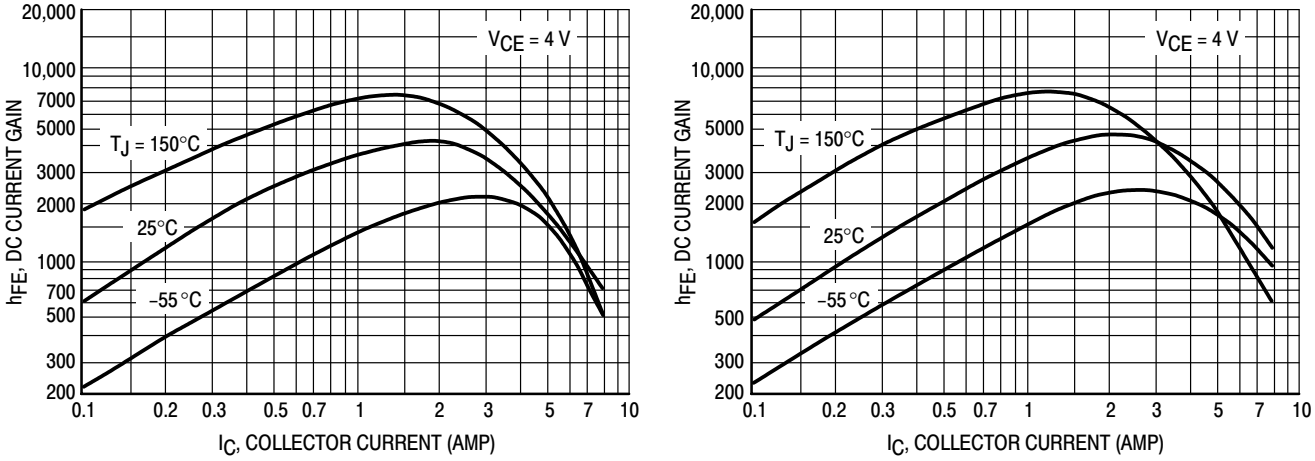


Figure 2. DC Current Gain

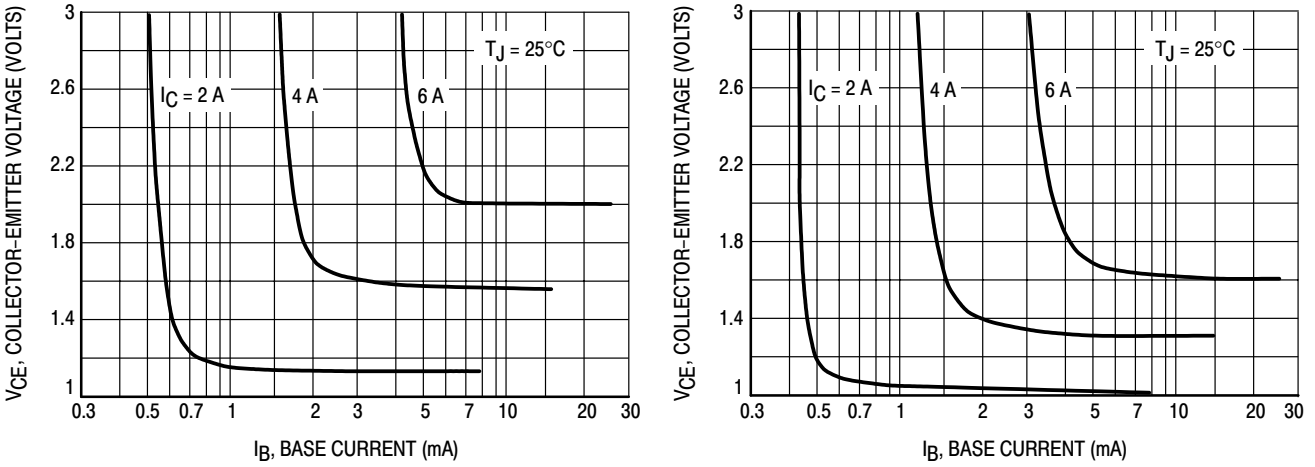


Figure 3. Collector Saturation Region

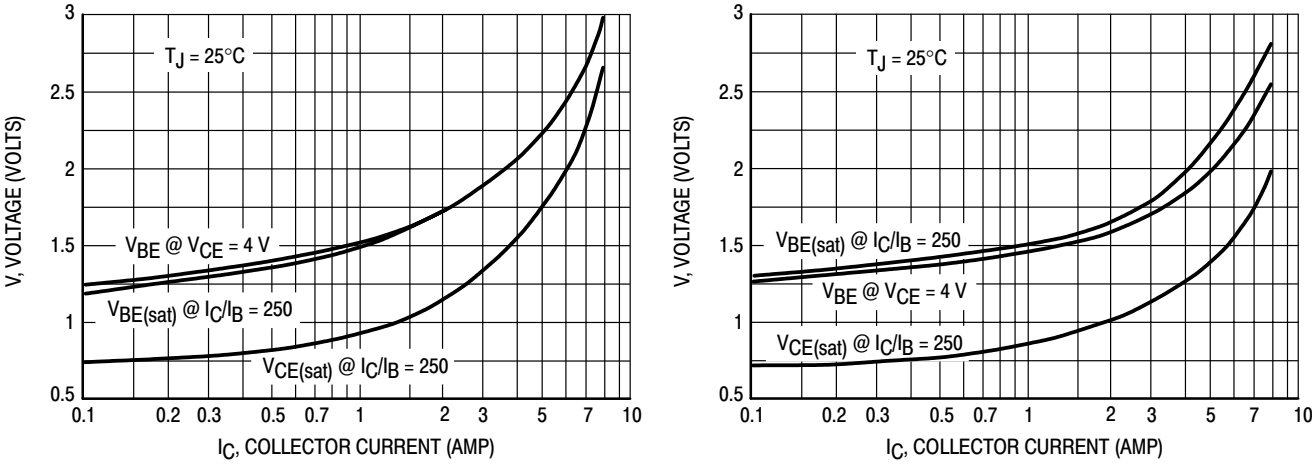


Figure 4. “On” Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127 **NPN MJD122**

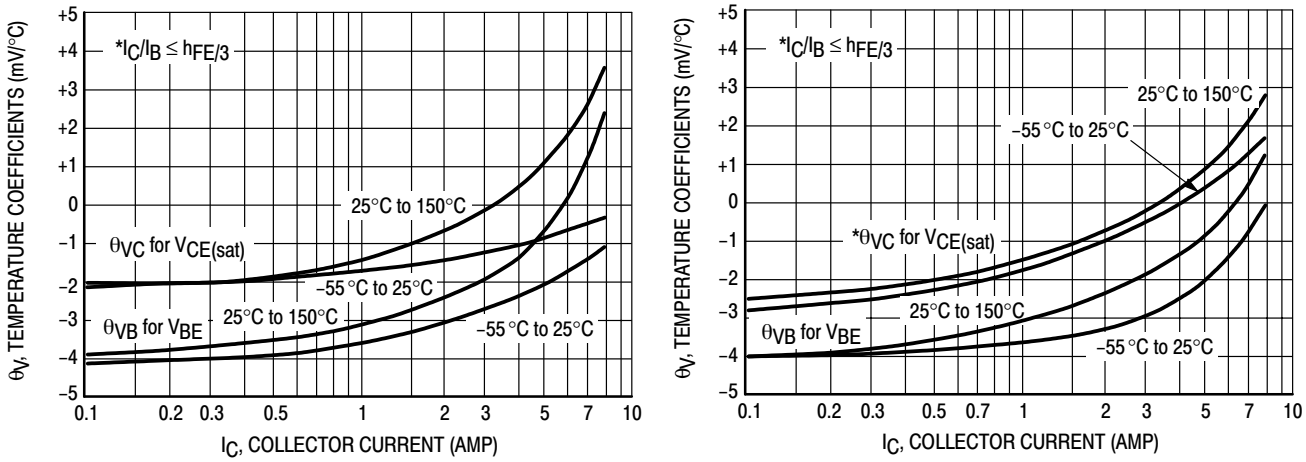


Figure 5. Temperature Coefficients

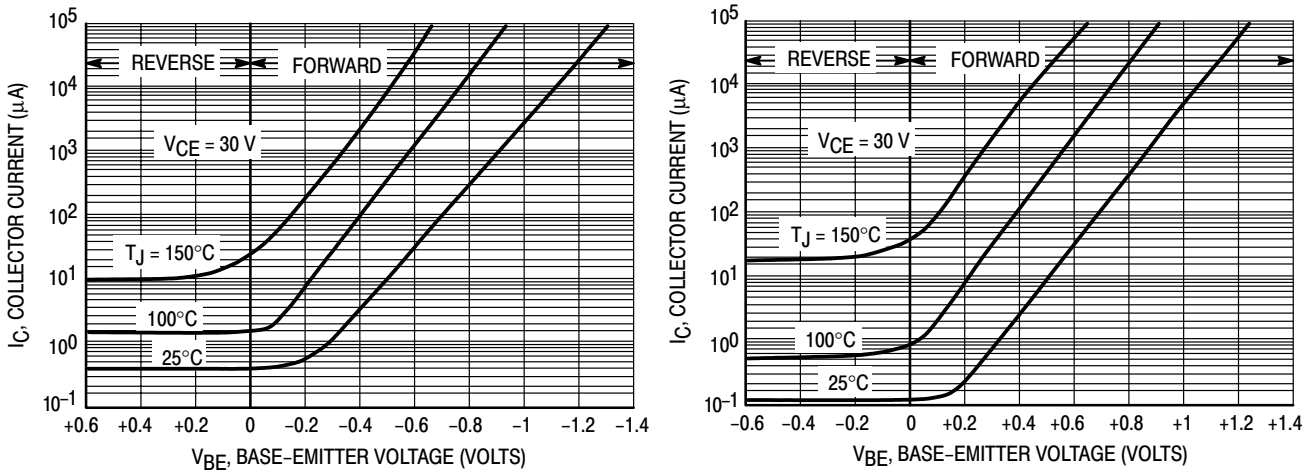


Figure 6. Collector Cut−Off Region

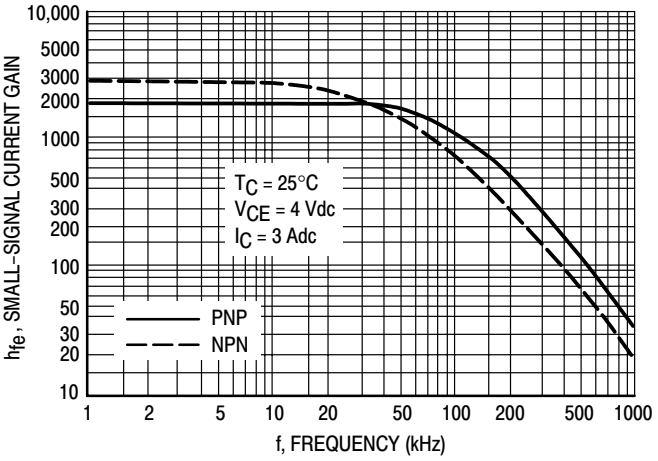


Figure 7. Small−Signal Current Gain

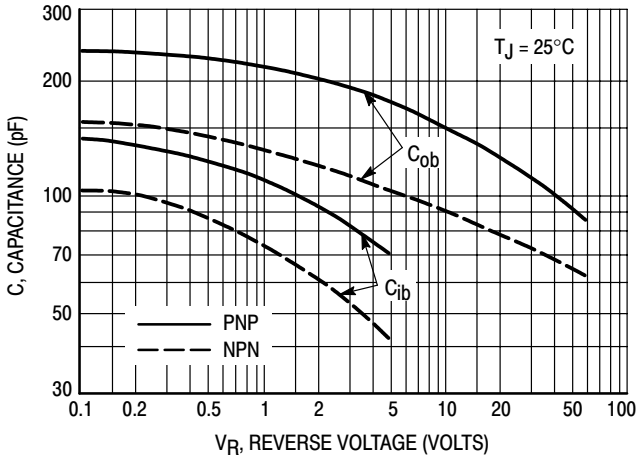


Figure 8. Capacitance

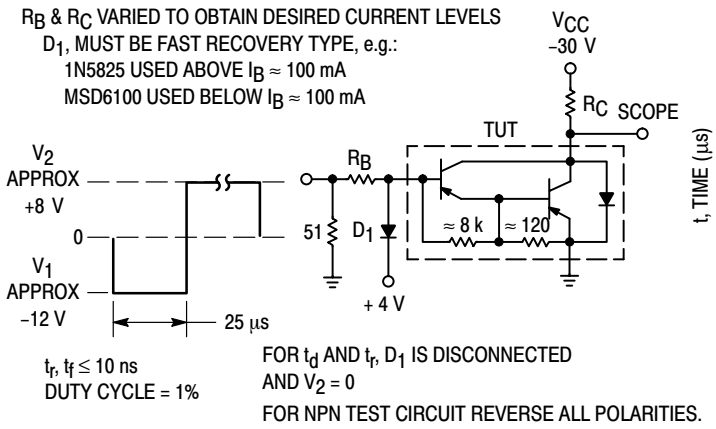


Figure 9. Switching Times Test Circuit

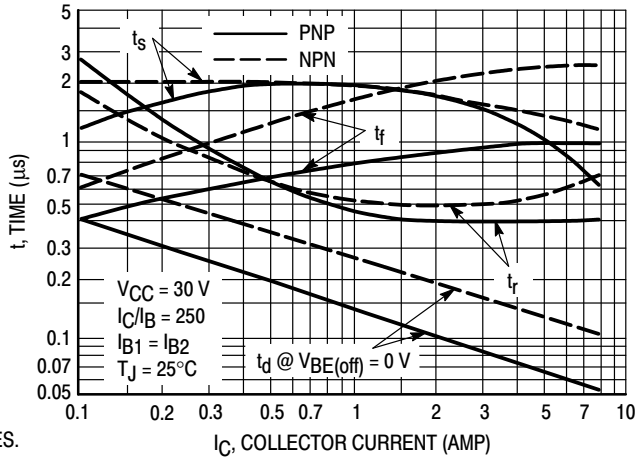


Figure 10. Switching Times

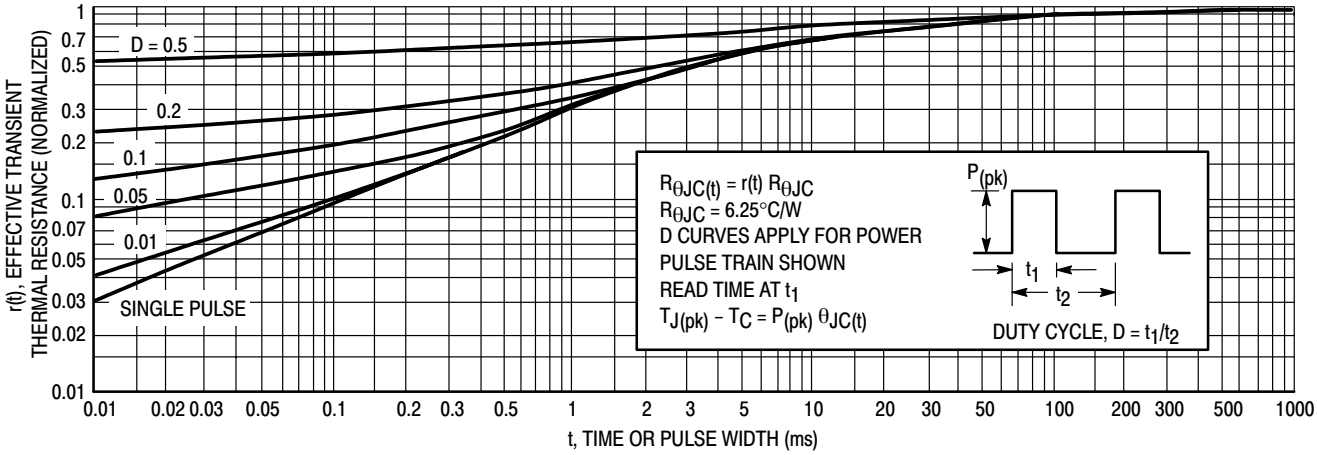


Figure 11. Thermal Response

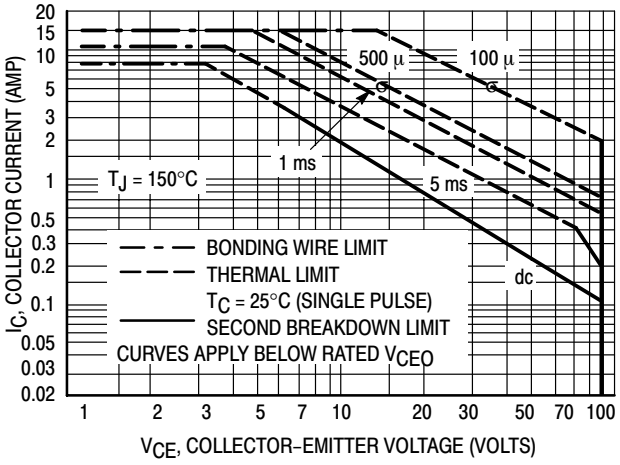


Figure 12. Maximum Forward Bias Safe Operating rea

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD122 (NPN)

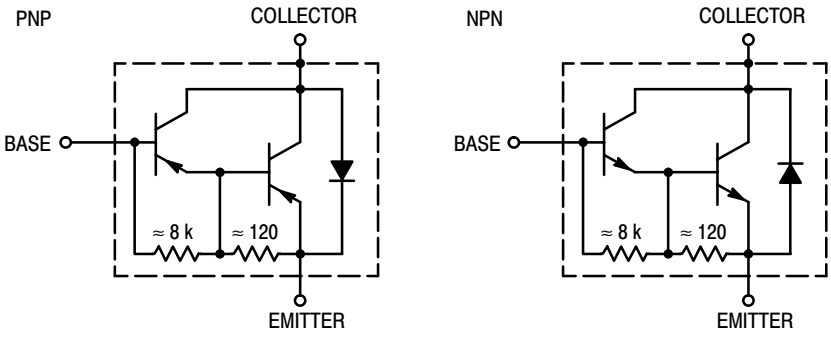


Figure 13. Darlington Schematic

MJD148

NPN Silicon Power Transistor

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- High Gain − 50 Min @ I_C = 2.0 A
- Low Saturation Voltage − 0.5 V @ I_C = 2.0 A
- High Current Gain − Bandwidth Product − f_T = 3.0 MHz Min @ I_C = 250 mAdc
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; >8000 V
  Machine Model, C; >400 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	45	Vdc
Collector−Base Voltage	V_{CB}	45	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous Peak	I_C	4.0 7.0	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation (Note 5) @ T_A = 25°C Derate above 25°C	P_D	 1.75 0.014	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient (Note 5)	$R_{\theta JA}$	71.4	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

5. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

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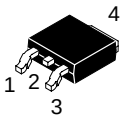
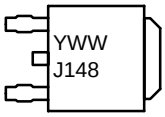
4.0 Amps
45 Volts
20 Watts
POWER TRANSISTOR

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



J148 = Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJD148T4	DPAK	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 6)	I_C = 100 mAdc, I_B = 0	$V_{CEO(sus)}$	45	−	Vdc
Collector Cutoff Current	V_{CB} = 45 Vdc, I_E = 0	I_{CBO}	−	20	μAdc
Emitter Cutoff Current	V_{BE} = 5 Vdc, I_C = 0	I_{EBO}	−	1	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 6)	I_C = 10 mAdc, V_{CE} = 5 Vdc I_C = 0.5 Adc, V_{CE} = 1 Vdc I_C = 2 Adc, V_{CE} = 1 Vdc I_C = 3 Adc, V_{CE} = 1 Vdc	h_{FE}	40 85 50 30	− 375 − −	−
Collector−Emitter Saturation Voltage (Note 6)	I_C = 2 Adc, I_B = 0.2 Adc	$V_{CE(sat)}$	−	0.5	Vdc
Base−Emitter On Voltage (Note 6)	I_C = 2 Adc, V_{CE} = 1 Vdc	$V_{BE(on)}$	−	1.1	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain−Bandwidth Product	I_C = 250 mAdc, V_{CE} = 1 Vdc, f = 1 MHz	f_T	3	−	MHz

6. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

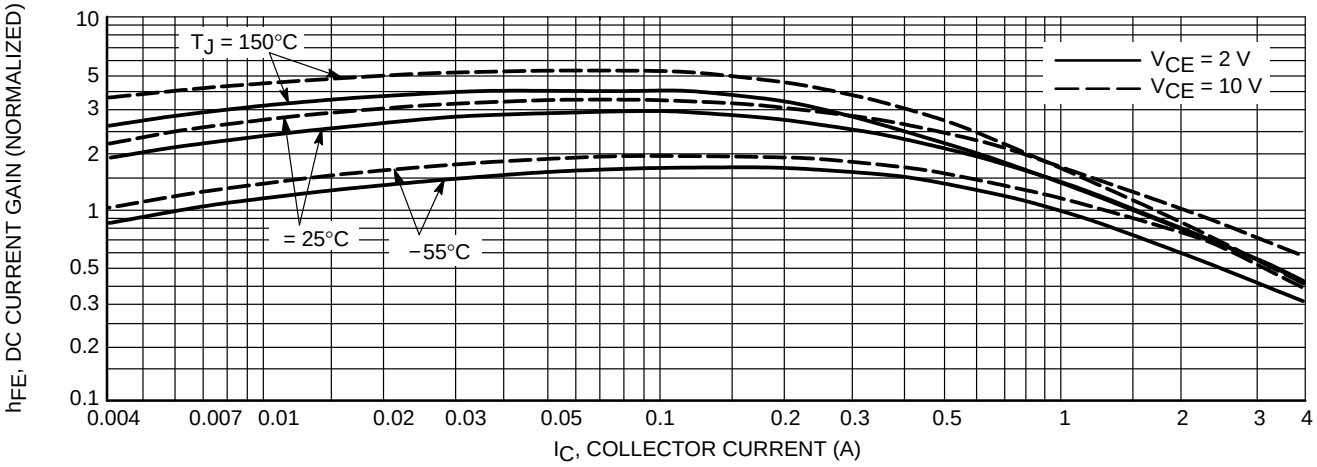


Figure 1. DC Current Gain

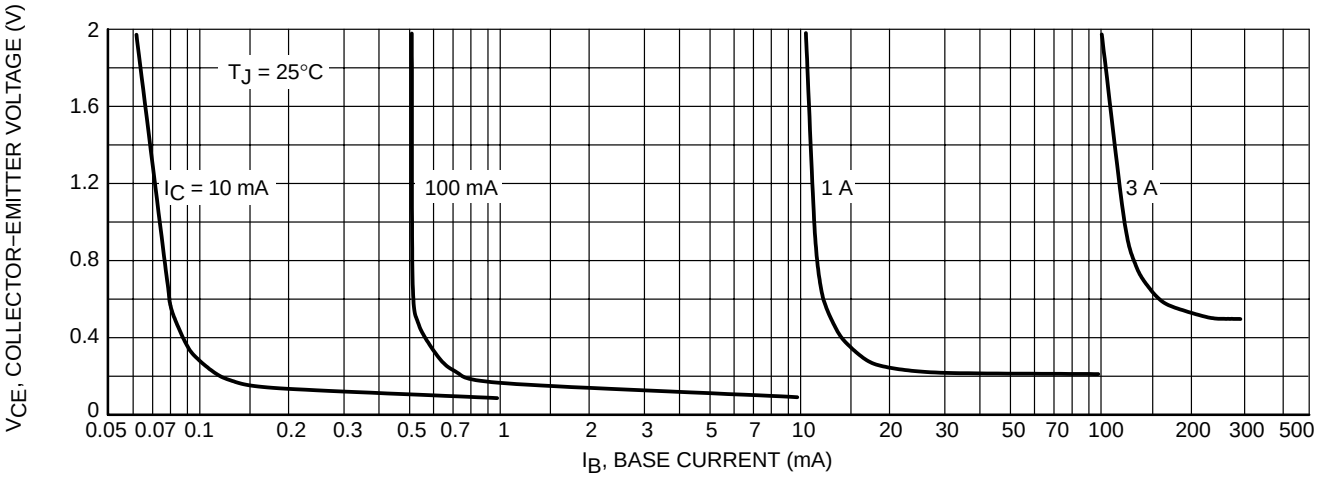


Figure 2. Collector Saturation Region

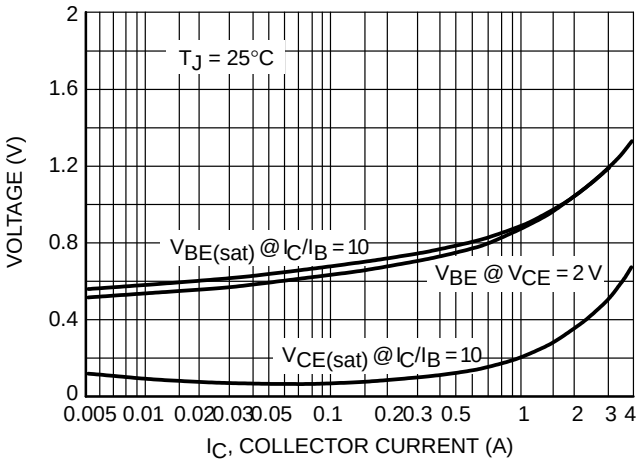


Figure 3. “On” Voltages

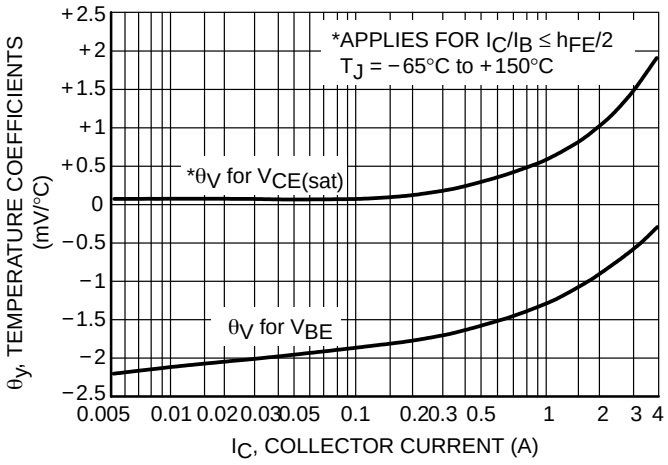


Figure 4. Temperature Coefficients

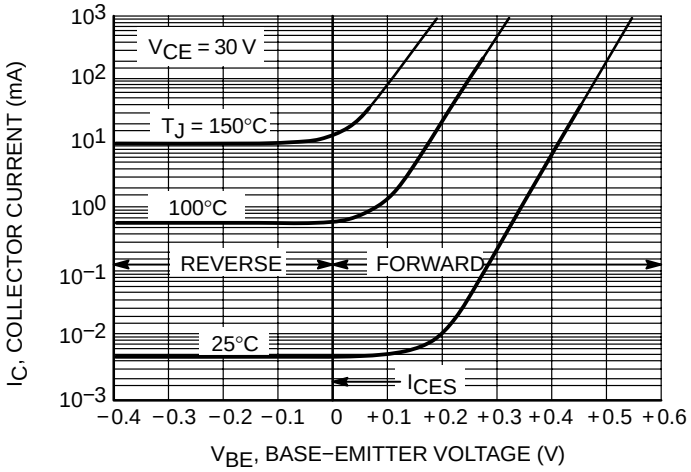


Figure 5. Collector Cut−Off Region

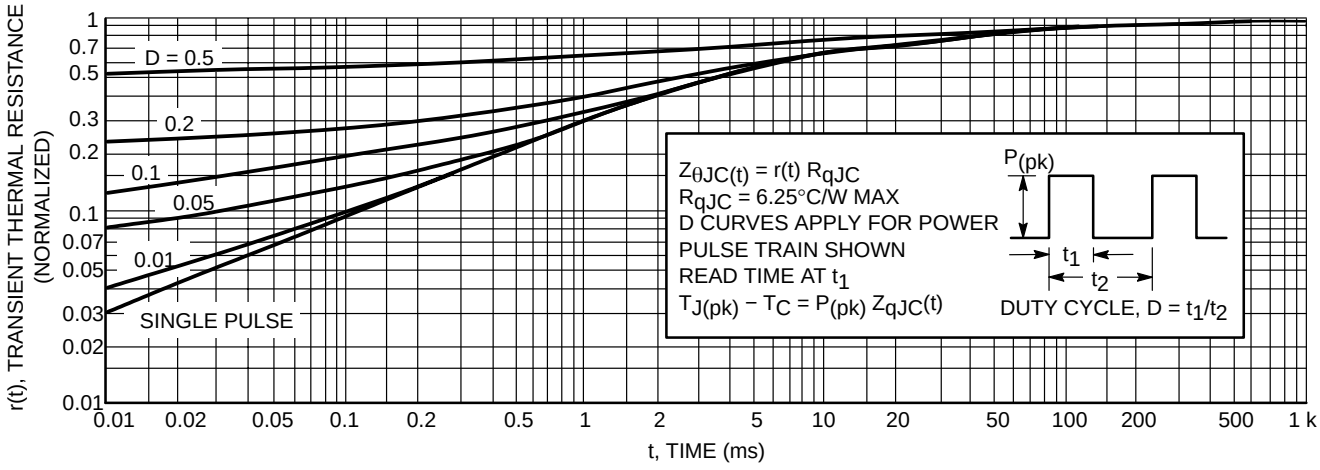


Figure 6. Thermal Response

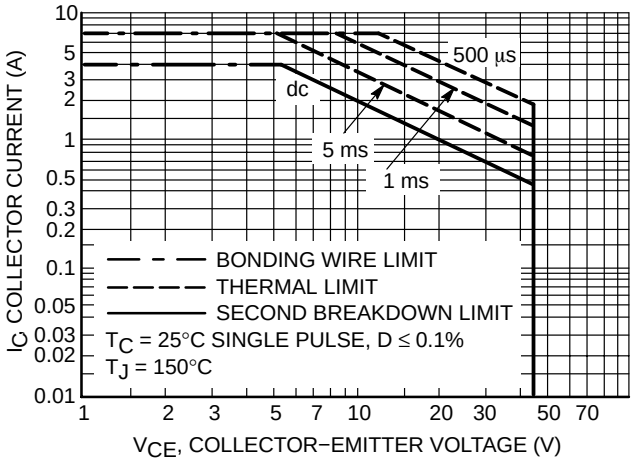


Figure 7. Maximum Rated Forward Bias

FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD18002D2

Bipolar NPN Transistor

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector−Emitter Diode and Built−In Efficient Antisaturation Network

The MJD18002D2 is a state−of−the−art high speed, high gain bipolar transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no longer a need to guarantee an h_{FE} window.

Features

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector−Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic V_{CEsat}
- Characteristics Make It Suitable for PFC Application
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- Six Sigma® Process Providing Tight and Reproductible Parameter Spreads

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	11	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	2.0 5.0	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	1.0 2.0	Adc

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

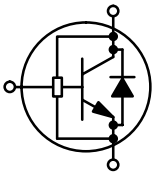
Characteristic	Symbol	Value	Unit
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	5.0	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	71.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 sec.	T_L	260	°C

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%.

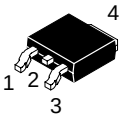
ON Semiconductor®

http://onsemi.com

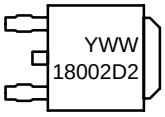
POWER TRANSISTOR
2 AMPERES
1000 VOLTS
50 WATTS



MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week
18002D2 = Device Code

ORDERING INFORMATION

Device	Package	Shipping†
MJD18002D2T4	DPAK	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	570	−	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	1000	1100	−	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	11	14	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}	−	−	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C	I_{CES}	− − −	− − −	100 500 100	μAdc
Emitter−Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	−	−	500	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc) (I_C = 1.0 Adc, I_B = 0.2 Adc)	 @ T_C = 25°C @ T_C = 25°C	$V_{BE(sat)}$	 − −	 0.78 0.87	 1.0 1.1	Vdc
Collector−Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc) (I_C = 1.0 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$	− − − −	0.36 0.50 0.40 0.65	0.6 1.0 0.75 1.2	Vdc
DC Current Gain (I_C = 0.4 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	@ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C	h_{FE}	14 8.0 6.0 4.0	25 15 10 6.0	− − − −	−
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_t	−	13	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	−	50	100	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}	−	340	500	pF
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1.0 Adc) (I_{EC} = 0.4 Adc)	 @ T_C = 25°C @ T_C = 25°C @ T_C = 125°C	V_{EC}	 − − −	 1.2 1.0 0.6	 1.5 1.3 −	Vdc
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/μs) (I_F = 1.0 Adc, di/dt = 10 A/μs)	 @ T_C = 25°C @ T_C = 25°C	t_{fr}	 − −	 517 480	 − −	ns
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage Determinated 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.4 Adc I_{B1} = 40 mA V_{CC} = 300 Vdc I_C = 1 Adc I_{B1} = 0.2 A V_{CC} = 300 Vdc	@ 1 μs @ 3 μs @ 1 μs @ 3 μs	@ T_C = 25°C @ T_C = 25°C @ T_C = 25°C @ T_C = 25°C	$V_{CE(dsat)}$	− − − −	7.4 2.5 11.7 1.3	− − − −	V

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C.S. 10%, Pulse Width = 40 μs)							
Turn−on Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 200 mAdc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}	− −	225 375	350 −	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	0.8 −	− 1.5	1.1 −	μs
Turn−on Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}	− −	100 94	150 −	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	0.95 −	− 1.5	1.25 −	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_f	− −	130 120	175 −	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	0.4 −	− 0.7	0.7 −	μs
Cross−over Time		@ T_C = 25°C @ T_C = 125°C	t_c	− −	110 100	175 −	ns
Fall Time	I_C = 0.8 Adc I_{B1} = 160 mAdc I_{B2} = 160 mAdc	@ T_C = 25°C @ T_C = 125°C	t_f	− −	130 140	175 −	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1 −	− 3.0	2.4 −	μs
Cross−over Time		@ T_C = 25°C @ T_C = 125°C	t_c	− −	275 350	350 −	ns
Fall Time	I_C = 1.0 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f	− −	100 100	150 −	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	− −	1.05 1.45	1.2 −	μs
Cross−over Time		@ T_C = 25°C @ T_C = 125°C	t_c	− −	100 115	150 −	ns

Typical Static Characteristics

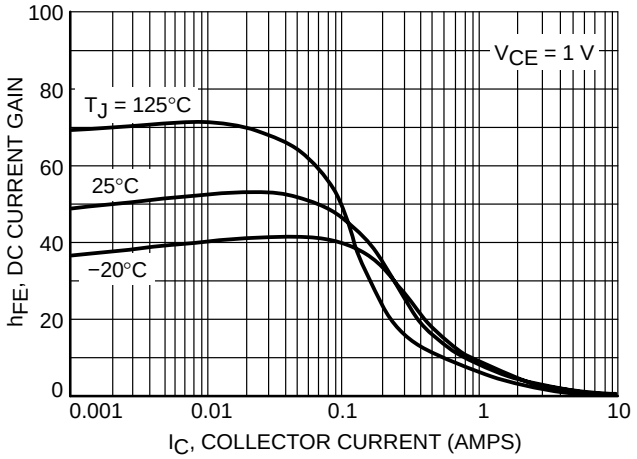


Figure 1. DC Current Gain @ 1 V

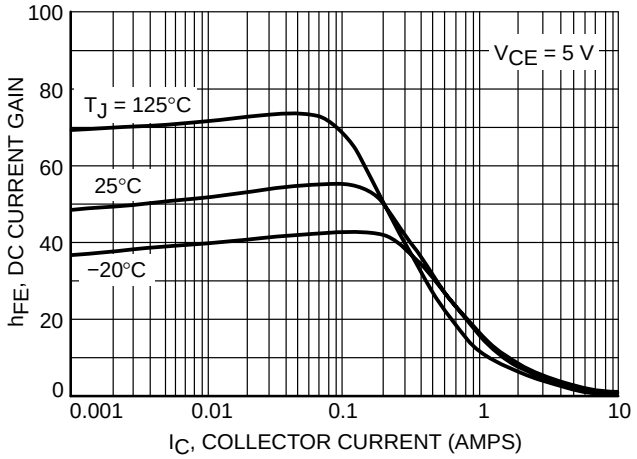


Figure 2. DC Current Gain @ 5 V

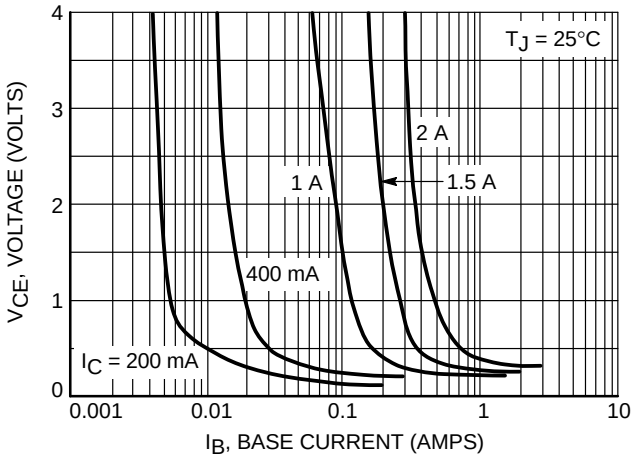


Figure 3. Collector Saturation Region

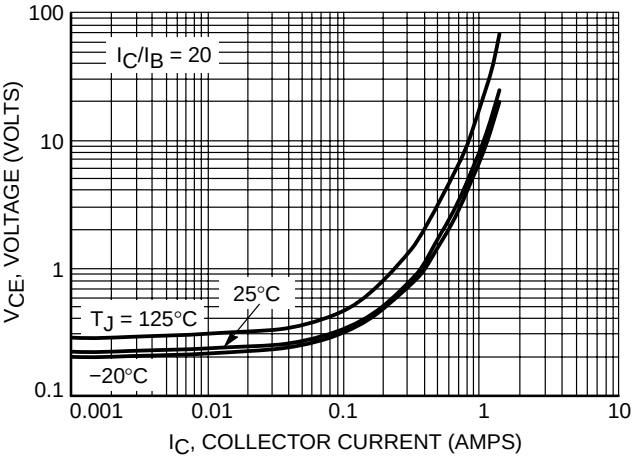


Figure 4. Collector−Emitter Saturation Voltage

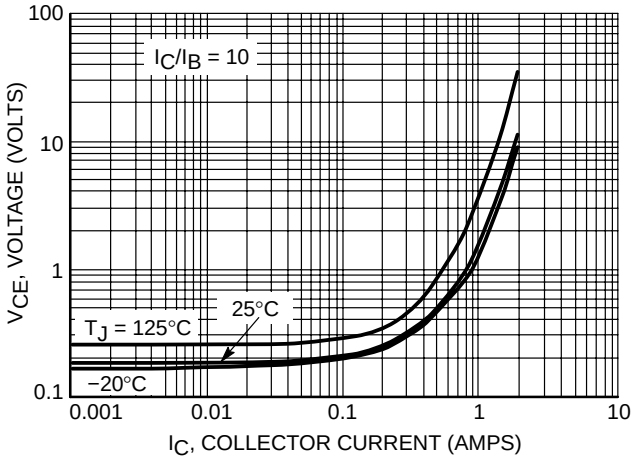


Figure 5. Collector−Emitter Saturation Voltage

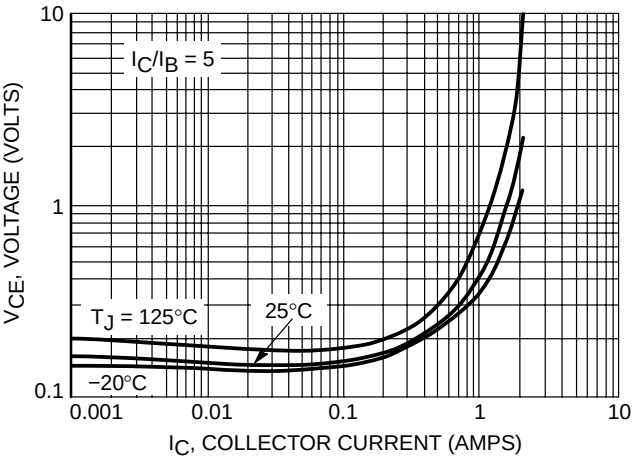


Figure 6. Collector−Emitter Saturation Voltage

Typical Static Characteristics

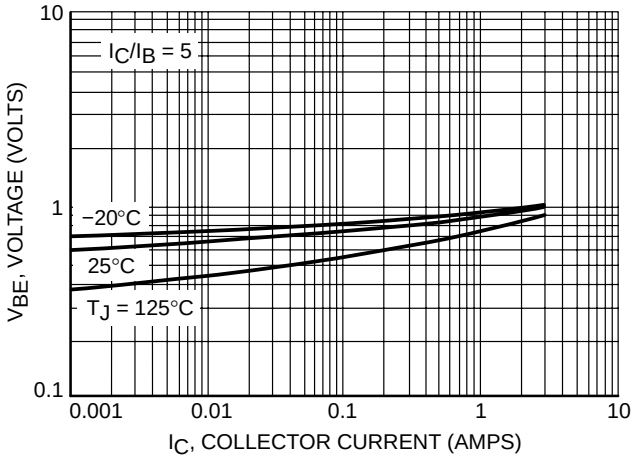


Figure 7. Base−Emitter Saturation Region I_C/I_B = 5

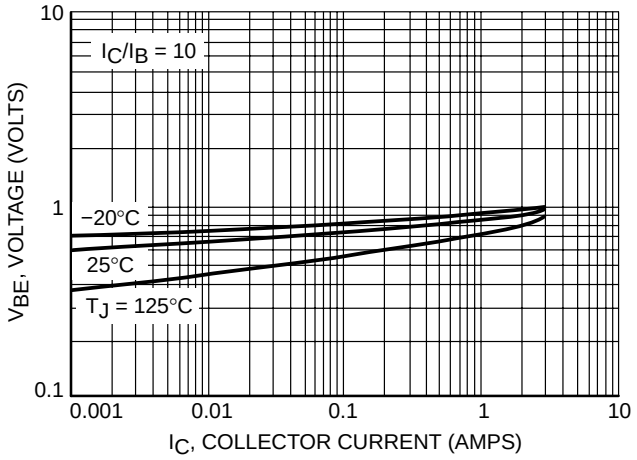


Figure 8. Base−Emitter Saturation Region I_C/I_B = 10

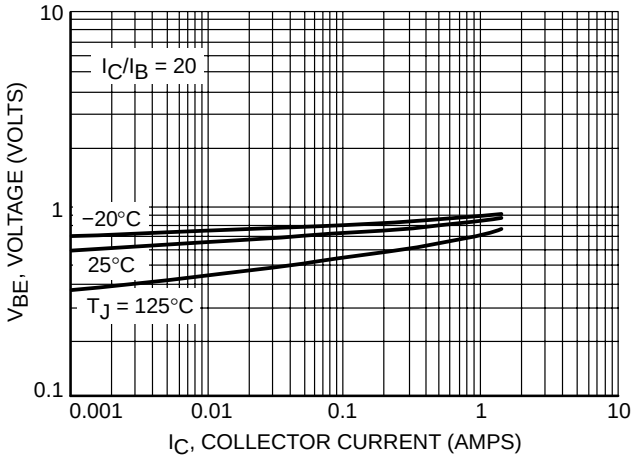


Figure 9. Base−Emitter Saturation Region I_C/I_B = 20

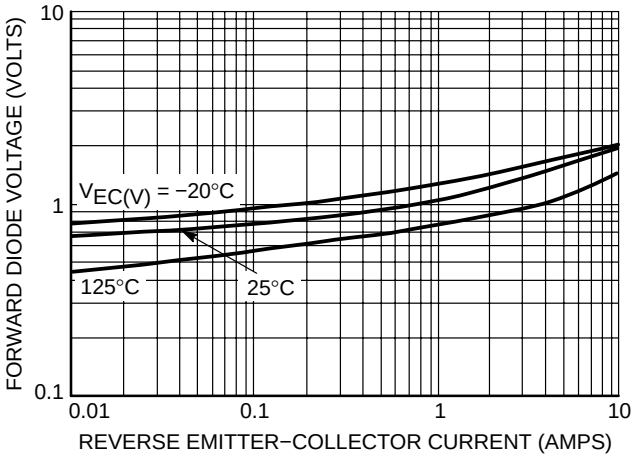


Figure 10. Forward Diode Voltage

Typical Switching Characteristics

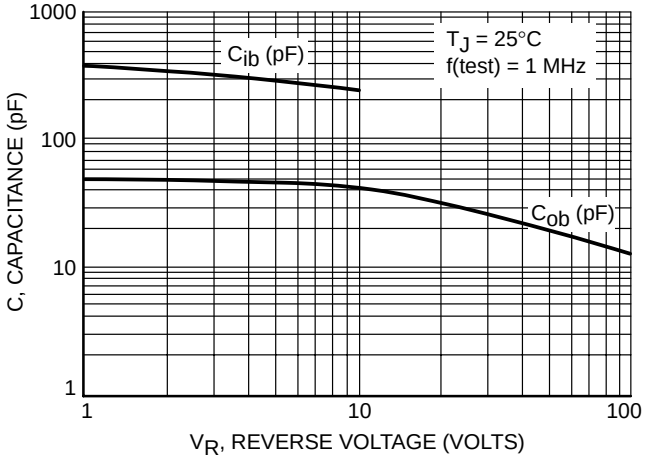


Figure 11. Capacitance

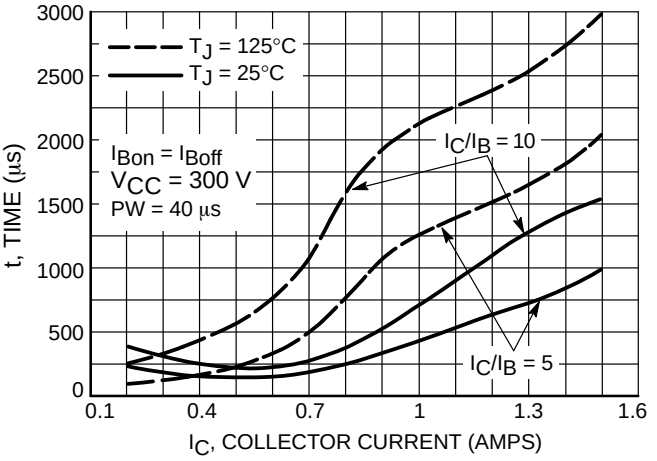


Figure 12. Resistive Switch Time, t_{on}

Typical Switching Characteristics

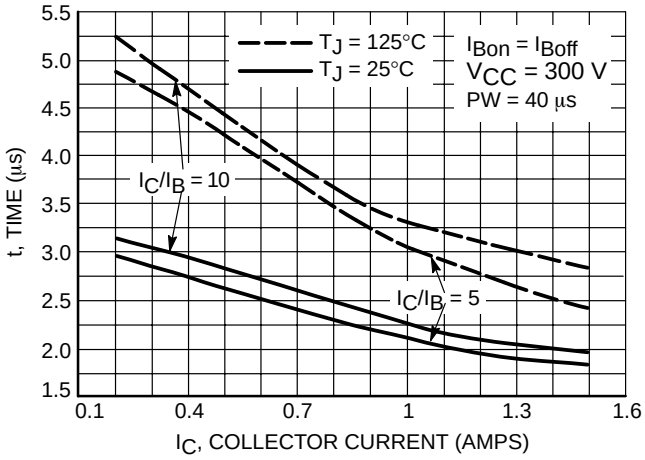


Figure 13. Resistive Switch Time, t_{off}

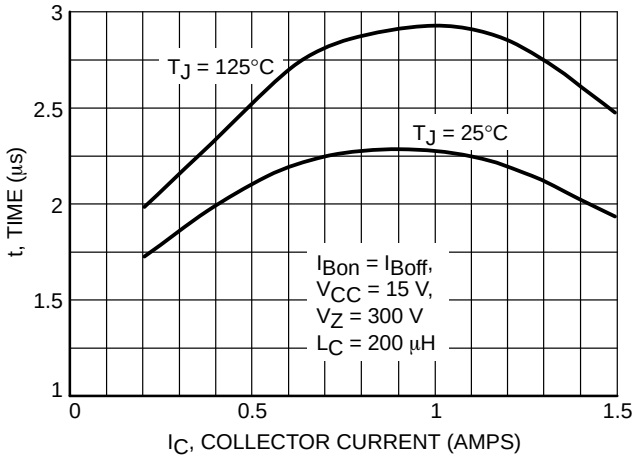


Figure 14. Inductive Storage Time, t_{si} @ I_C/I_B = 5

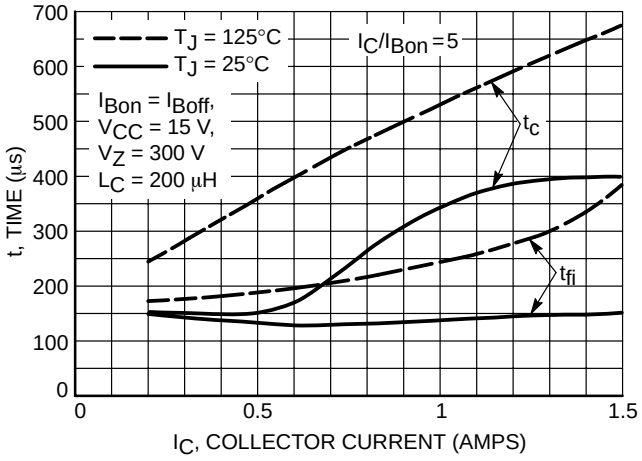


Figure 15. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

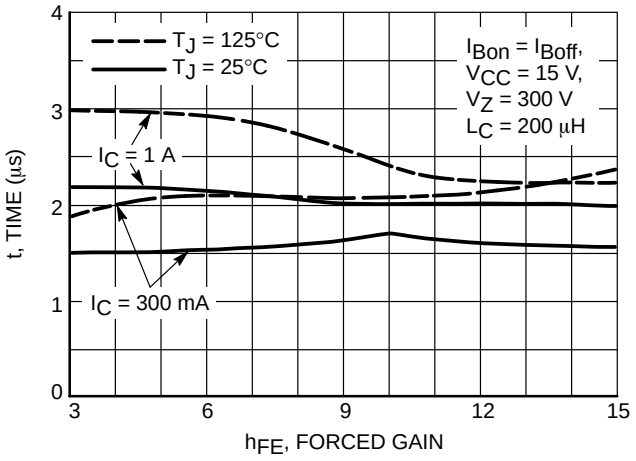


Figure 16. Inductive Storage Time

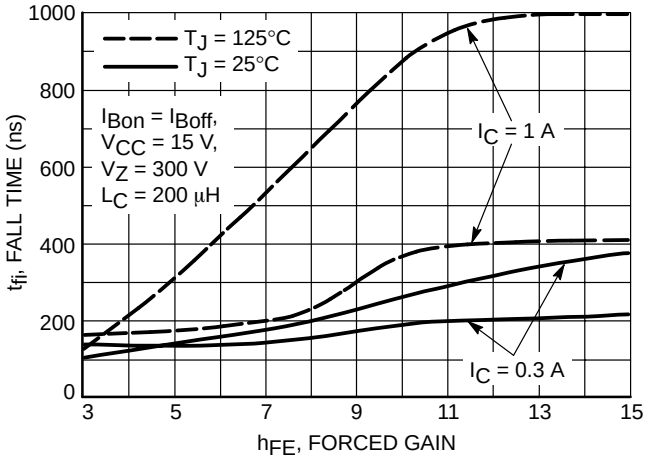


Figure 17. Inductive Fall Time

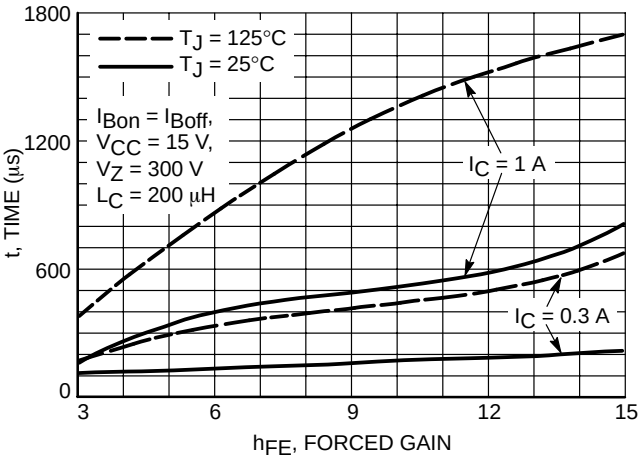


Figure 18. Inductive Cross−Over Time

Typical Switching Characteristics

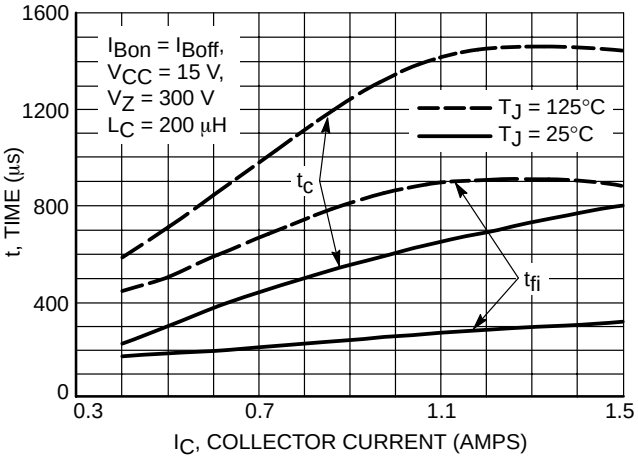


Figure 19. Inductive Switching Time, t_{fi} & T_C @ G = 10

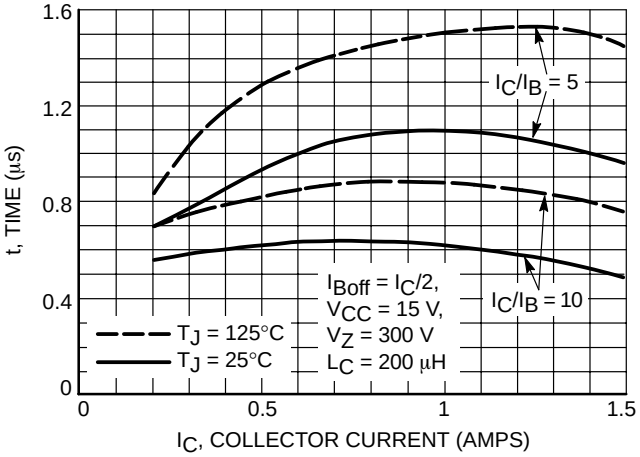


Figure 20. Inductive Switching Time, t_{si}

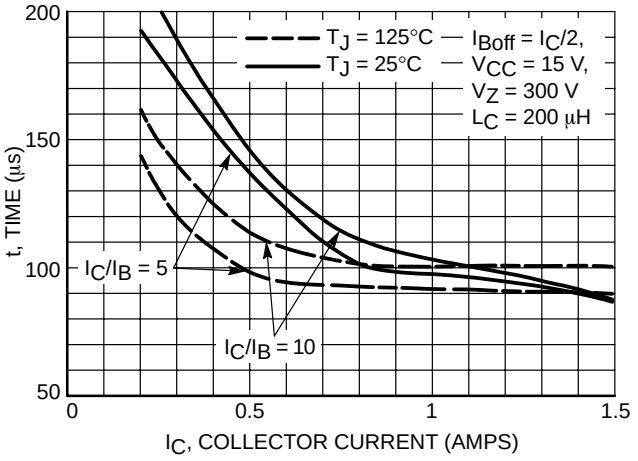


Figure 21. Inductive Storage Time, t_{fi}

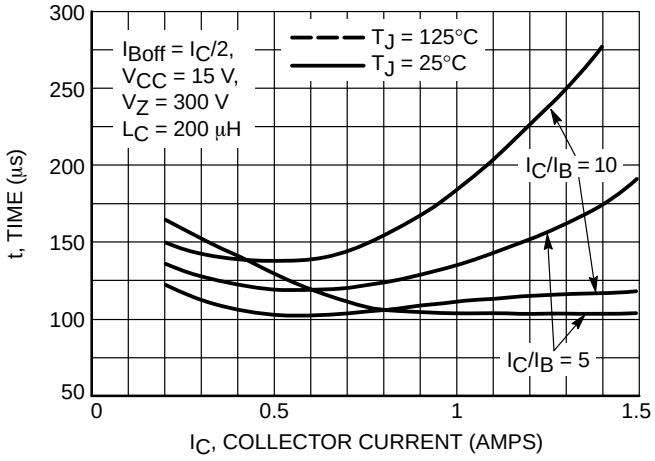


Figure 22. Inductive Storage Time, t_c

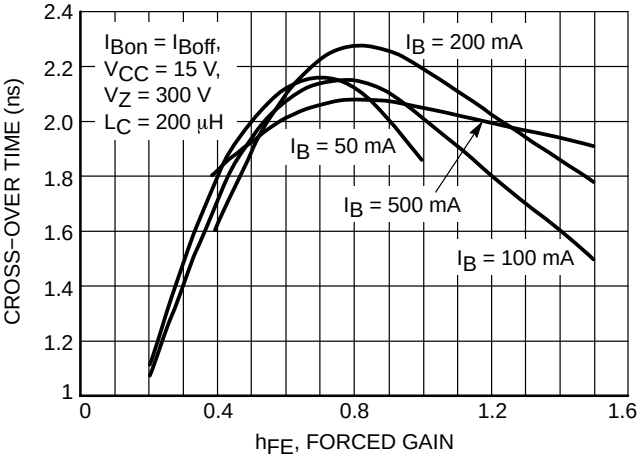


Figure 23. Inductive Storage Time, t_{si}

Figure 24. Dynamic Saturation Voltage Measurements

Typical Switching Characteristics

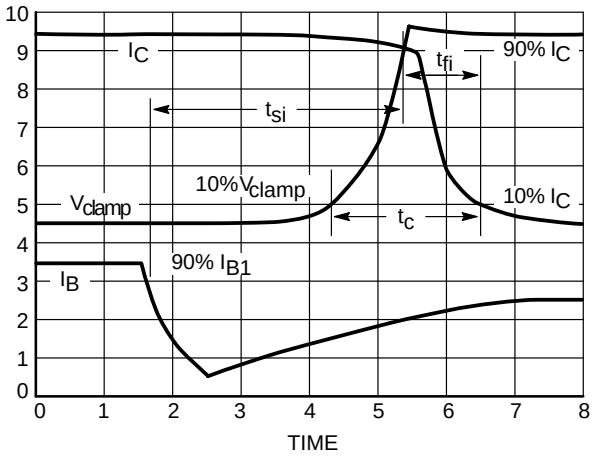
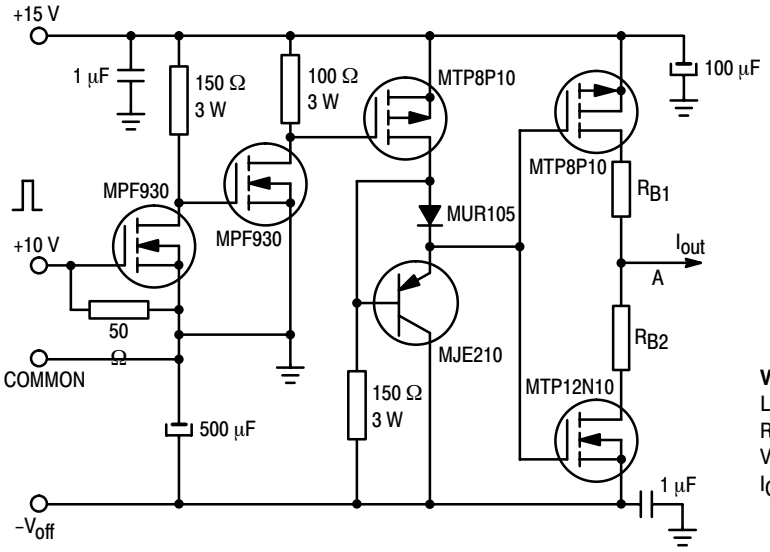
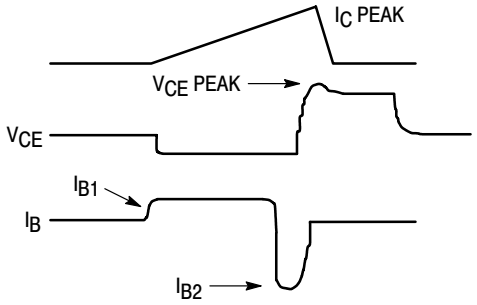


Figure 25. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	**Inductive Switching**	**RBSOA**
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

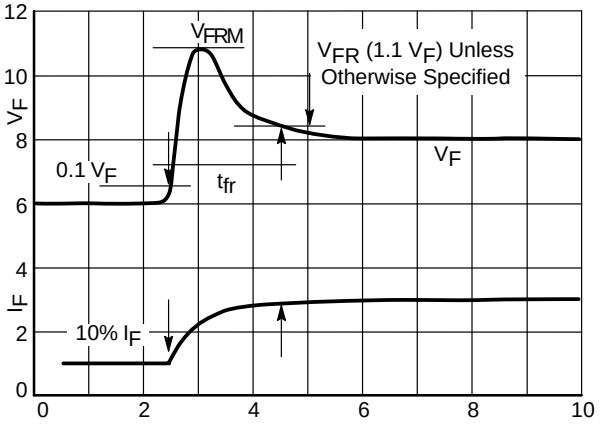


Figure 26. t_{fr} Measurement

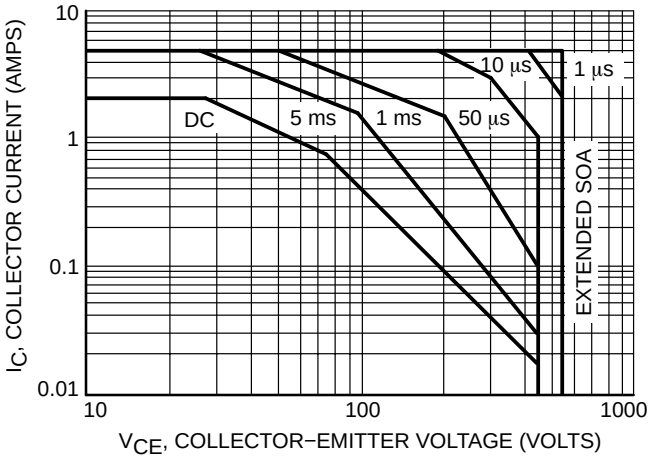


Figure 27. Forward Bias Safe Operating Area

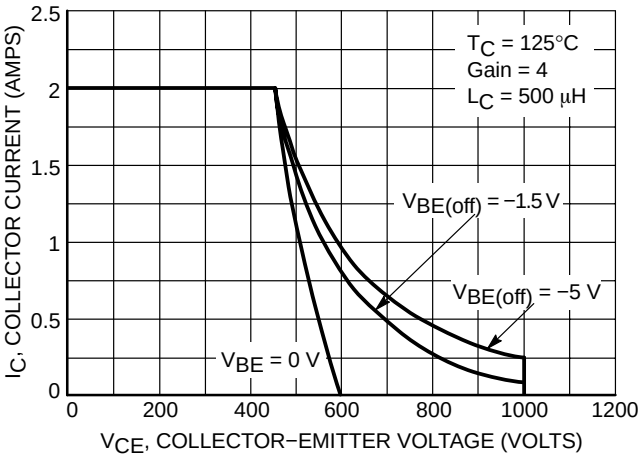


Figure 28. Reverse Bias Safe Operating Area

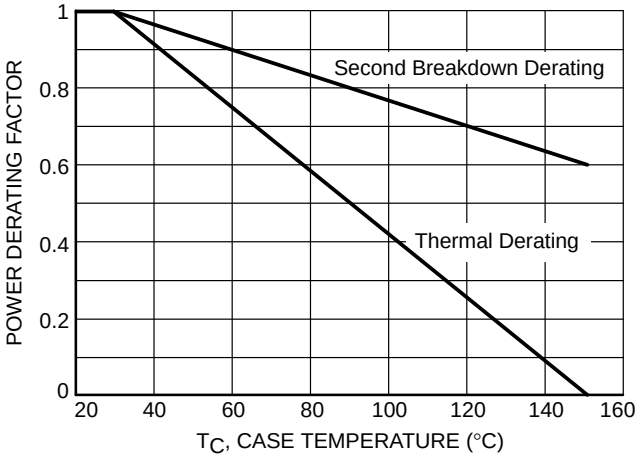


Figure 29. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 27 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second Breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 27 may be found at any case temperature by using the appropriate curve on Figure 29.

$T_{J(pk)}$ may be calculated from the data in Figure 30. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 28). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

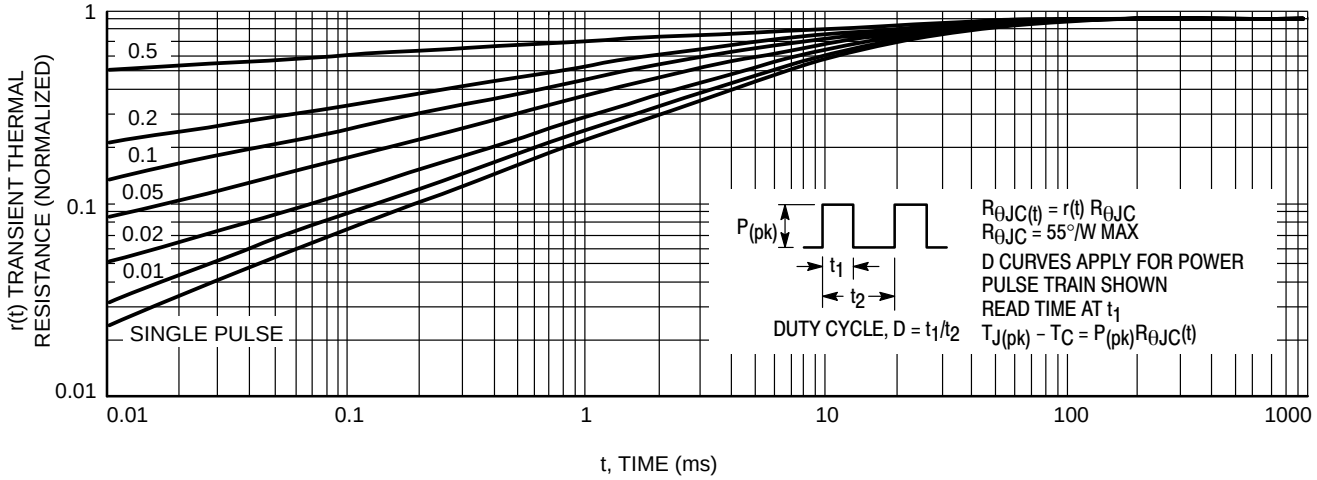


Figure 30. Typical Thermal Response ($Z_{\Omega JC}(t)$) for MJD18002D2

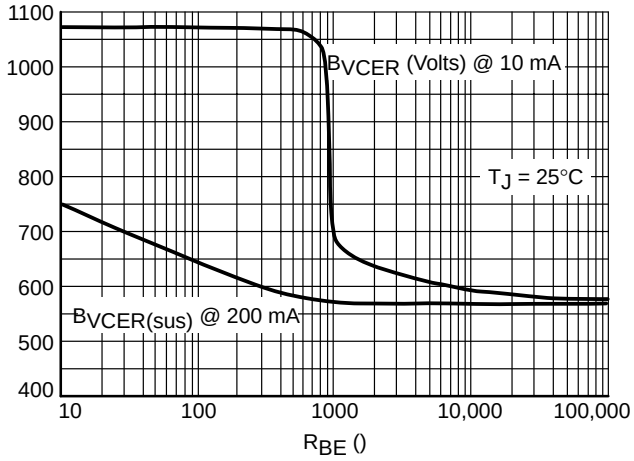


Figure 31. B_{VCER}

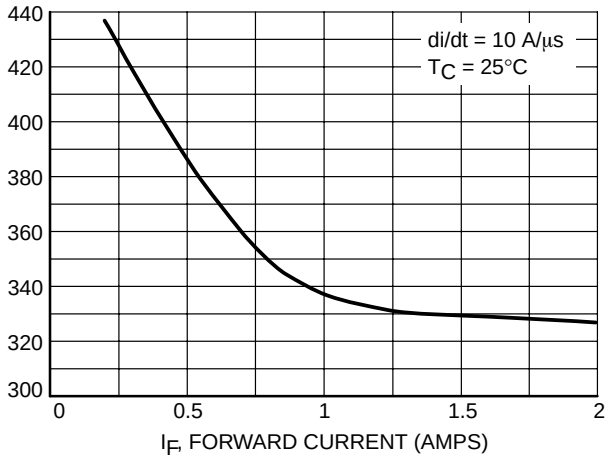


Figure 32. Forward Recovery Time, t_{fr}

MJD200 (NPN)
MJD210 (PNP)

Complementary Plastic Power Transistors

NPN/PNP Silicon DPAK For Surface Mount Applications

Designed for low voltage, low−power, high−gain audio amplifier applications.

Features

- Pb−Free Packages are Available
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain − h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2 Adc
  = 10 (Min) @ I_C = 5 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current−Gain − Bandwidth Product −
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage −
  I_{CBO} = 100 nAdc @ Rated V_{CB}
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

ON Semiconductor®

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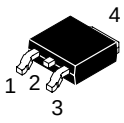
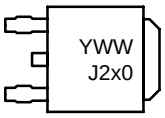
SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y	= Year
WW	= Work Week
x	= 1 or 0

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 433 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Base Voltage	V_{CB}	40	Vdc
Collector−Emitter Voltage	V_{CEO}	25	Vdc
Emitter−Base Voltage	V_{EB}	8	Vdc
Collector Current − Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.4 0.011	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	10	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	89.3	°C/W

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2), (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	−	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 − −	 100 100	nAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}	−	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 2), (I_C = 500 mAdc, V_{CE} = 1 Vdc) (I_C = 2 Adc, V_{CE} = 1 Vdc) (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	 70 45 10	 − 180 −	−
Collector−Emitter Saturation Voltage (Note 2) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 200 mAdc) (I_C = 5 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	 − − −	 0.3 0.75 1.8	Vdc
Base−Emitter Saturation Voltage (Note 2), (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	−	2.5	Vdc
Base−Emitter On Voltage (Note 2), (I_C = 2 Adc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	−	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 3) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	−	MHz
Output Capacitance MJD200 (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD210	C_{ob}	− −	80 120	pF

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
3. $f_T = |h_{fe}| \bullet f_{test}$.

ORDERING INFORMATION

Device	Package Type	Shipping†
MJD200	DPAK	75 Units / Rail
MJD200G	DPAK (Pb−Free)	75 Units / Rail
MJD200RL	DPAK	1800 Tape & Reel
MJD200RLG	DPAK (Pb−Free)	1800 Tape & Reel
MJD200T4	DPAK	2500 Tape & Reel
MJD200T4G	DPAK (Pb−Free)	2500 Tape & Reel
MJD210	DPAK	75 Units / Rail
MJD210RL	DPAK	1800 Tape & Reel
MJD210T4	DPAK	2500 Tape & Reel
MJD210T4G	DPAK (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

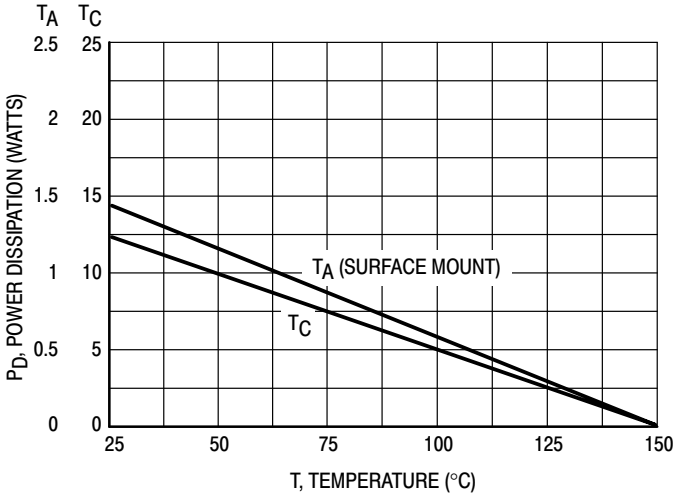


Figure 33. Power Derating

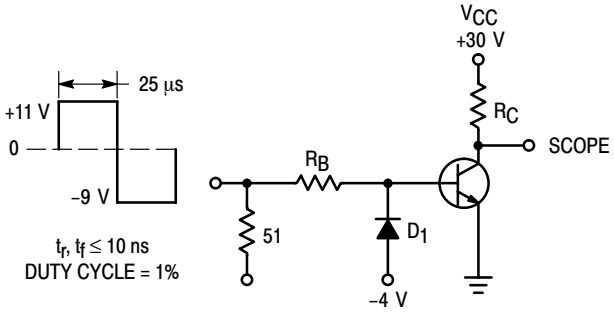


Figure 34. Switching Time Test Circuit

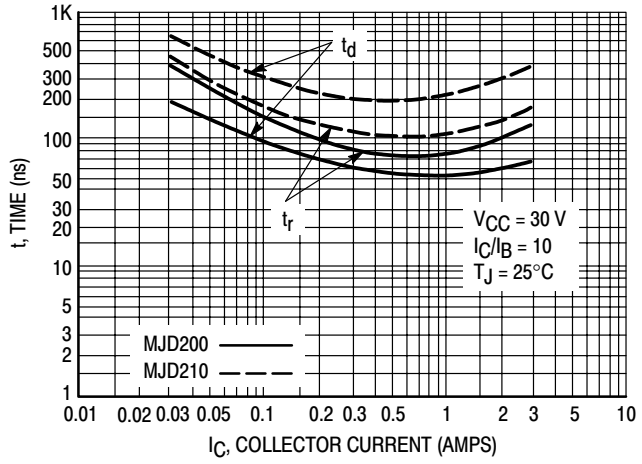


Figure 35. Turn−On Time

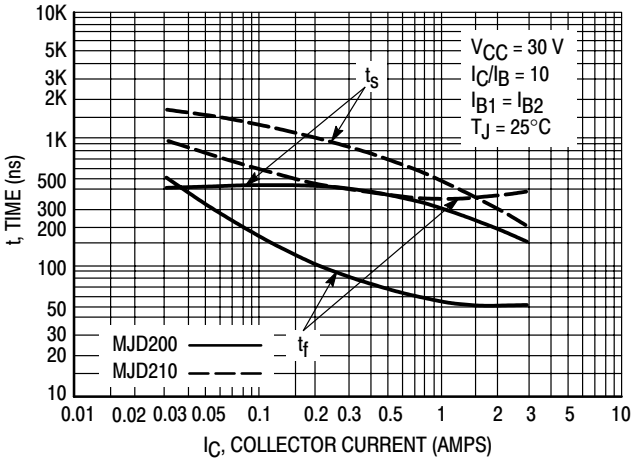
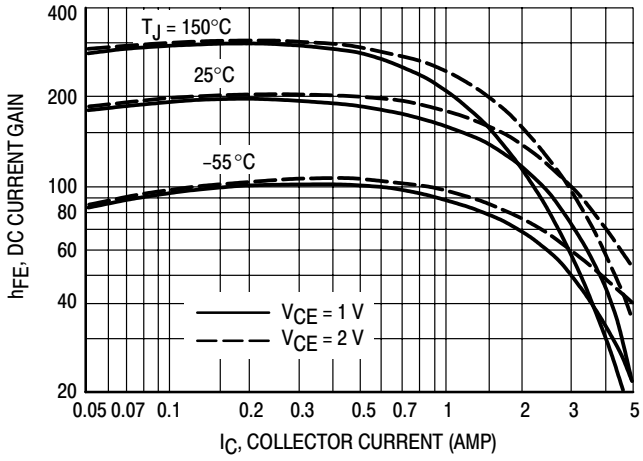


Figure 36. Turn−Off Time

NPN
MJD200



PNP
MJD210

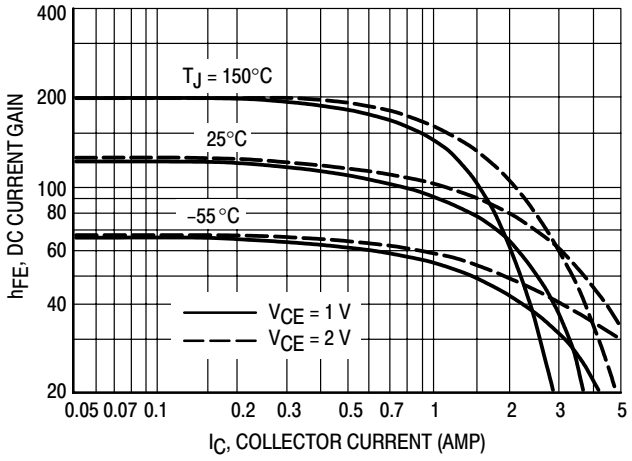
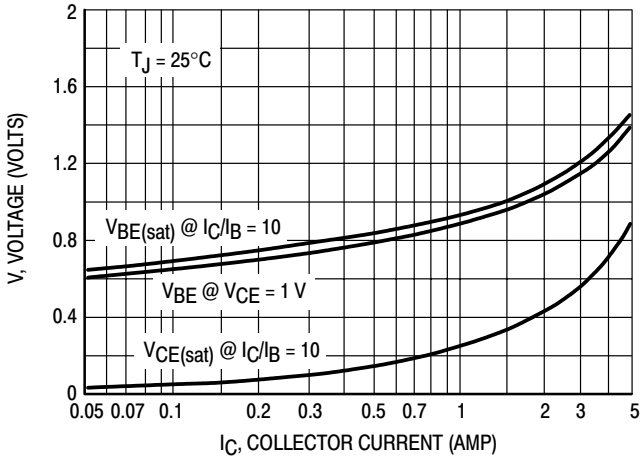


Figure 37. DC Current Gain



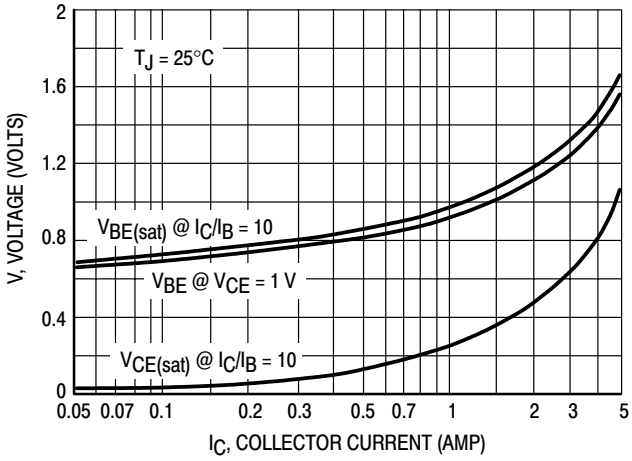
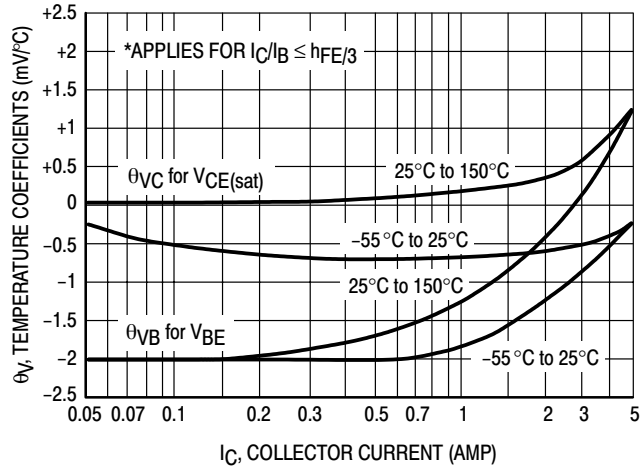


Figure 38. “On” Voltage



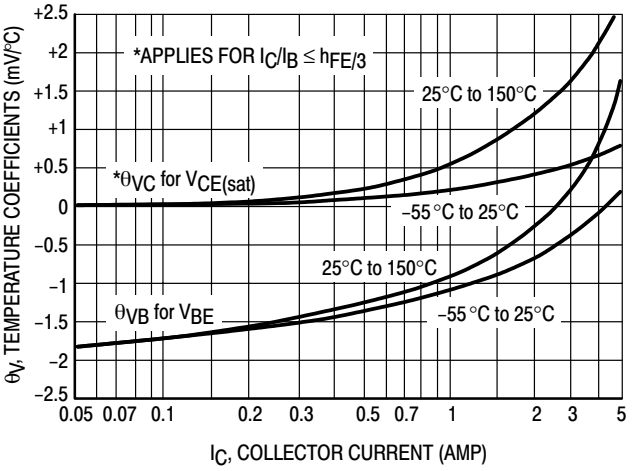


Figure 39. Temperature Coefficients

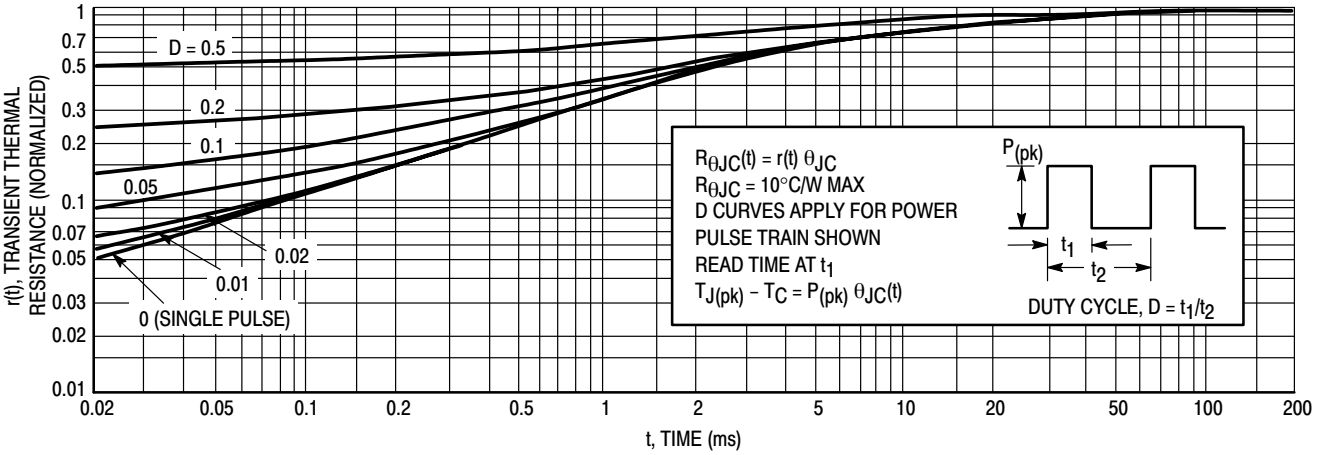


Figure 40. Thermal Response

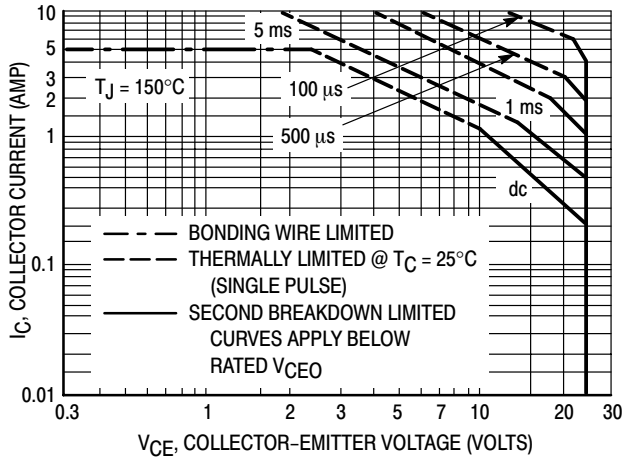


Figure 41. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 41 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

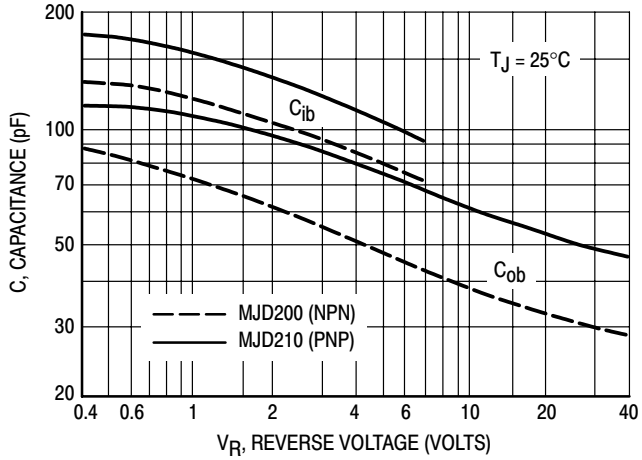


Figure 42. Capacitance

MJD243 (NPN), MJD253 (PNP)

Preferred Device

Complementary Silicon Plastic Power Transistor

DPAK−3 for Surface Mount Applications

Designed for low voltage, low−power, high−gain audio amplifier applications.

Features

- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 100 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain −
  h_{FE} = 40 (Min) @ I_C = 200 mAdc
  = 15 (Min) @ I_C = 1.0 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.6 Vdc (Max) @ I_C = 1.0 Adc
- High Current−Gain − Bandwidth Product −
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage −
  I_{CBO} = 100 nAdc @ Rated V_{CB}
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- Pb−Free Package is Available

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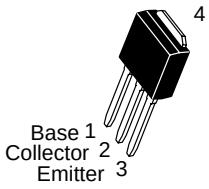
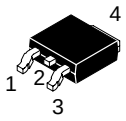
4.0 A, 100 V, 12.5 W
POWER TRANSISTOR

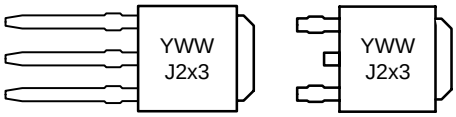


DPAK−3
CASE 369D
STYLE 1



DPAK−3
CASE 369C
STYLE 1

MARKING DIAGRAMS



Y = Year
WW = Work Week
J2x3 = Device Code
x = 4 or 5

ORDERING INFORMATION

Device	Package	Shipping†
MJD243	DPAK−3	75 Units/Rail
MJD243T4	DPAK−3	2500/Tape & Reel
MJD243T4G	DPAK−3 (Pb−Free)	2500/Tape & Reel
MJD253−1	DPAK−3	75 Units/Rail
MJD253T4	DPAK−3	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Base Voltage	V_{CB}	100	Vdc
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current−Continuous −Peak	I_C	4.0 8.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	W W/°C
Total Device Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	1.4 0.011	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted on minimum pad sizes recommended.

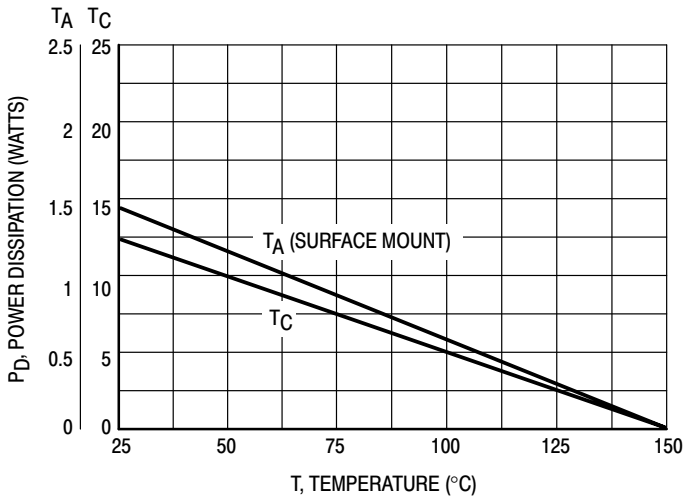


Figure 1. Power Derating

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	− −	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	−	100	nAdc
DC Current Gain (Note 3) (I_C = 200 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40 15	180 −	−
Collector−Emitter Saturation Voltage (Note 3) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	 − −	 0.3 0.6	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	−	1.8	Vdc
Base−Emitter On Voltage (Note 3) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 4) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	−	50	pF

2. When surface mounted on minimum pad sizes recommended.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$.

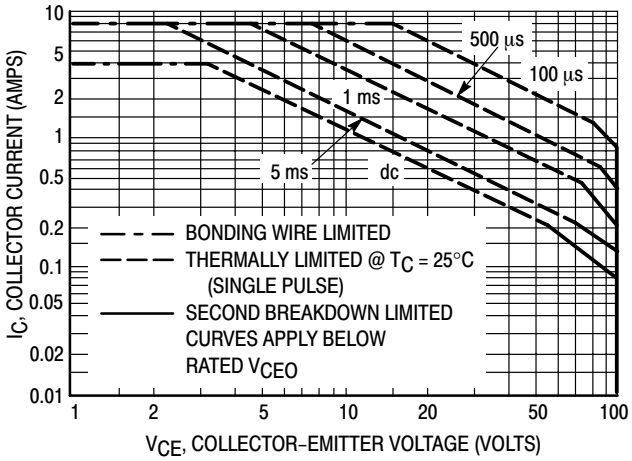


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

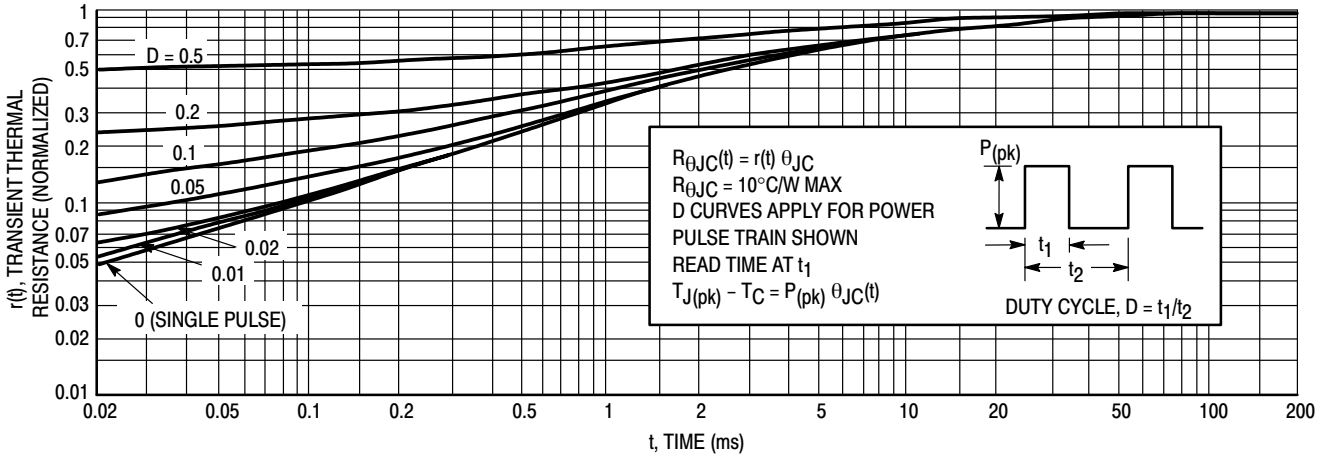
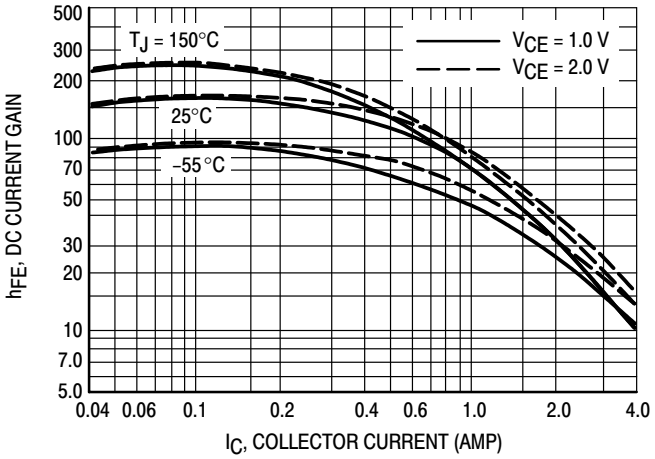


Figure 3. Thermal Response

NPN
MJD243



PNP
MJD253

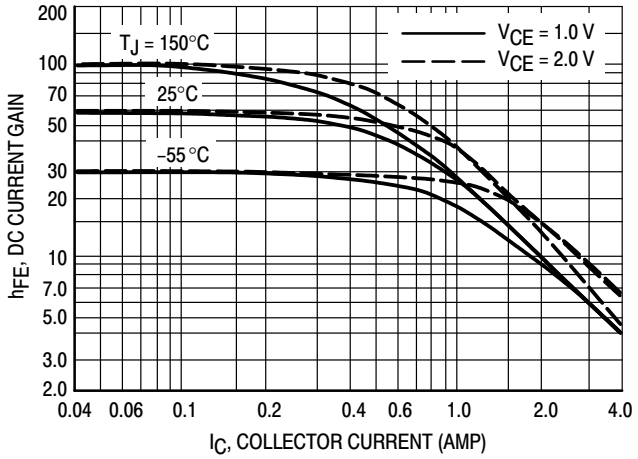
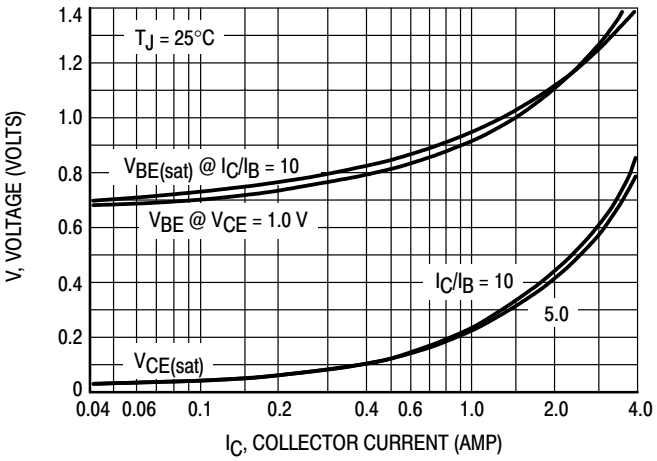


Figure 4. DC Current Gain



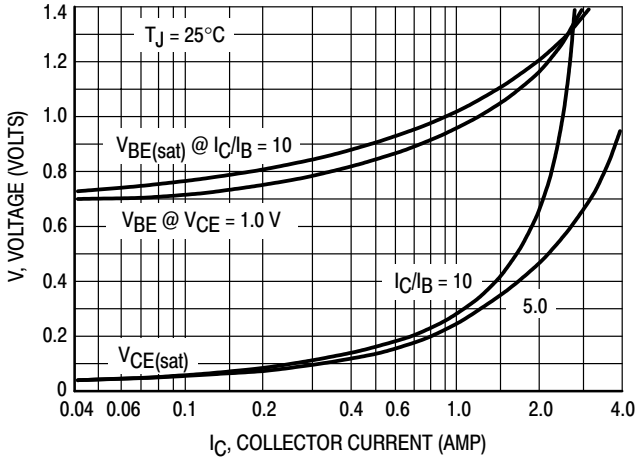
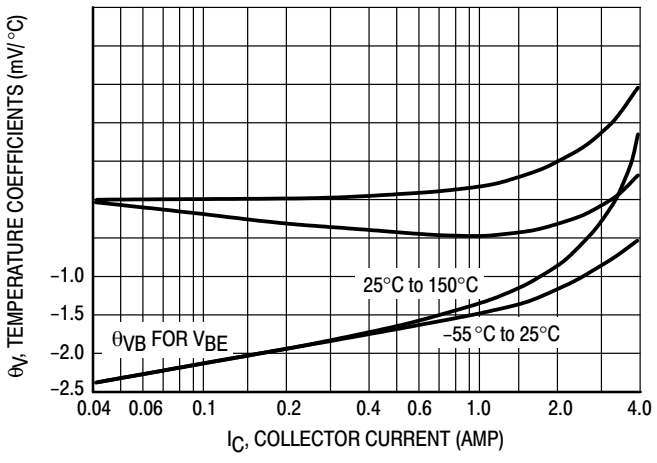


Figure 5. “On” Voltages



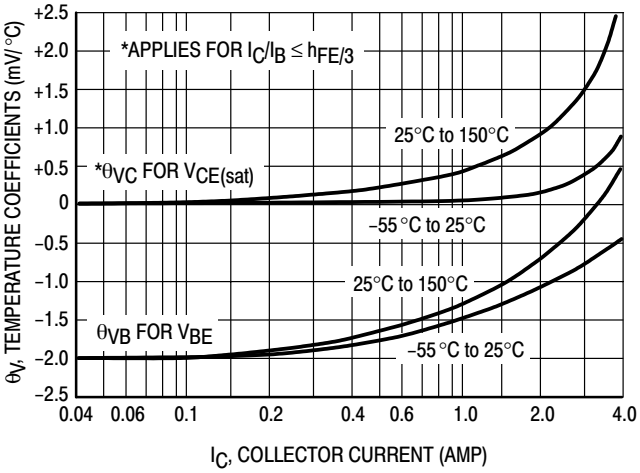
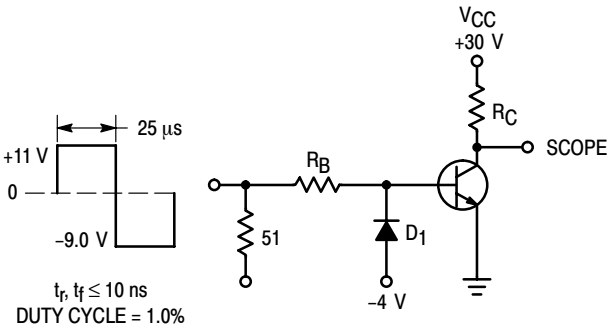


Figure 6. Temperature Coefficients



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 7. Switching Time Test Circuit

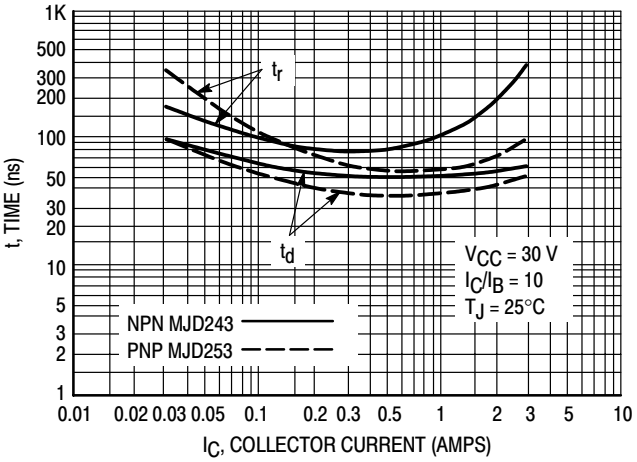


Figure 8. Turn−On Time

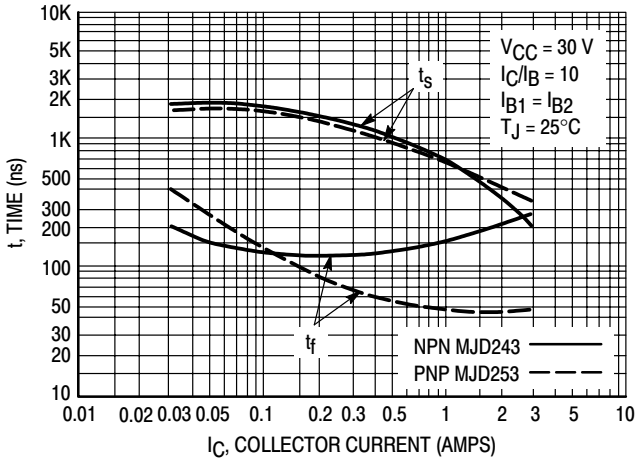


Figure 9. Turn−Off Time

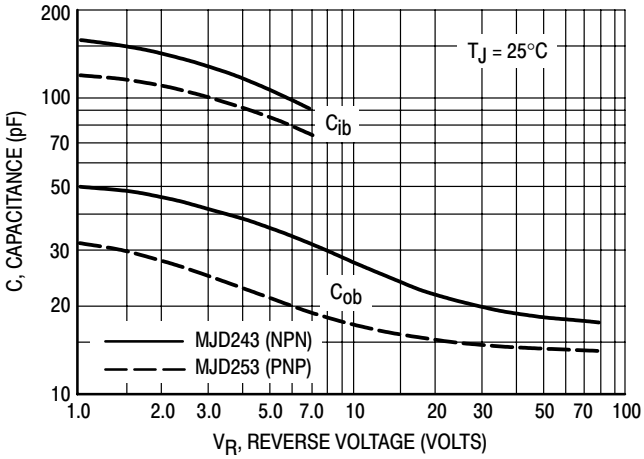


Figure 10. Capacitance

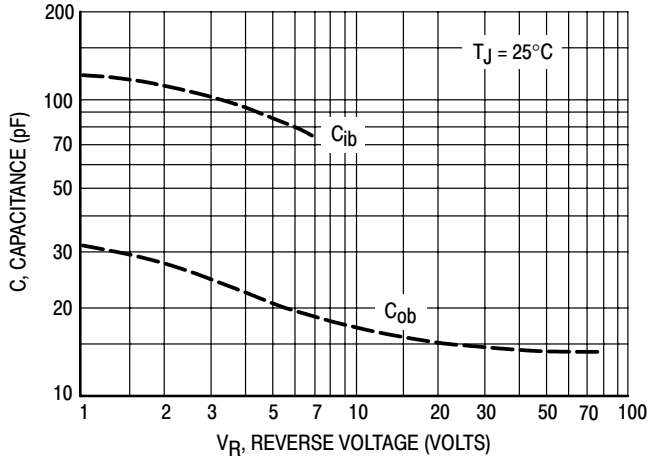


Figure 11. Capacitance

MJD2955 (NPN)
MJD3055 (PNP)

Complementary Power Transistors
DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

- Pb−Free Packages are Available
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to MJE2955 and MJE3055
- DC Current Gain Specified to 10 Amperes
- High Current Gain−Bandwidth Product − f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CB}	70	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D†	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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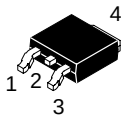
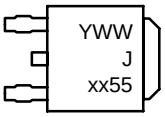
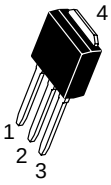
SILICON POWER TRANSISTORS 10 AMPERES 60 VOLTS 20 WATTS

MARKING DIAGRAMS

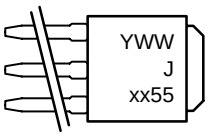


DPAK
CASE 369C
STYLE 1





DPAK−3
CASE 369D
STYLE 1



Y = Year
WW = Work Week
xx = 29 or 30

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 443 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 5) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	−	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	−	50	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 − −	 0.02 2	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 − −	 0.02 2	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (Note 5) (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	 20 5	 100 −	−
Collector−Emitter Saturation Voltage (Note 5) (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 − −	 1.1 8	Vdc
Base−Emitter On Voltage (Note 5) (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	−	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2	−	MHz

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD2955	DPAK	369C	75 Units / Rail
MJD2955G	DPAK (Pb−Free)	369C	75 Units / Rail
MJD2955−001	DPAK−3	369D	75 Units / Rail
MJD2955T4	DPAK	369C	2500 Tape & Reel
MJD2955T4G	DPAK (Pb−Free)	369C	2500 Tape & Reel
MJD3055	DPAK	369C	75 Units / Rail
MJD3055T4	DPAK	369C	2500 Tape & Reel
MJD3055T4G	DPAK (Pb−Free)	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

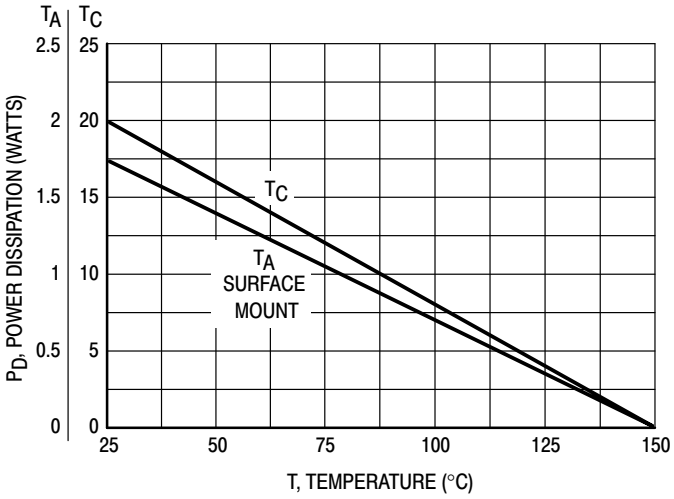


Figure 1. Power Derating

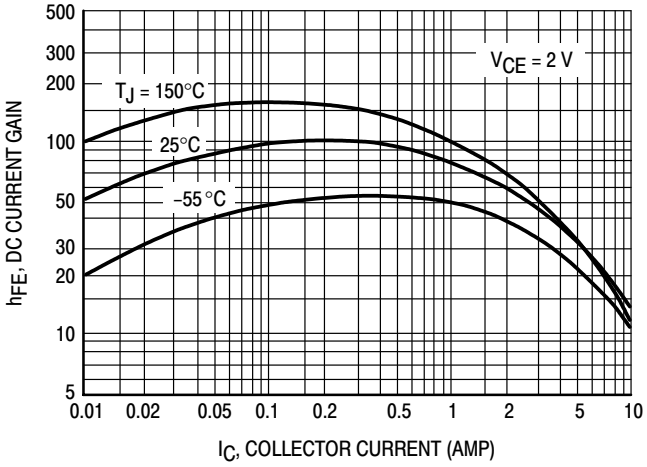


Figure 2. DC Current Gain

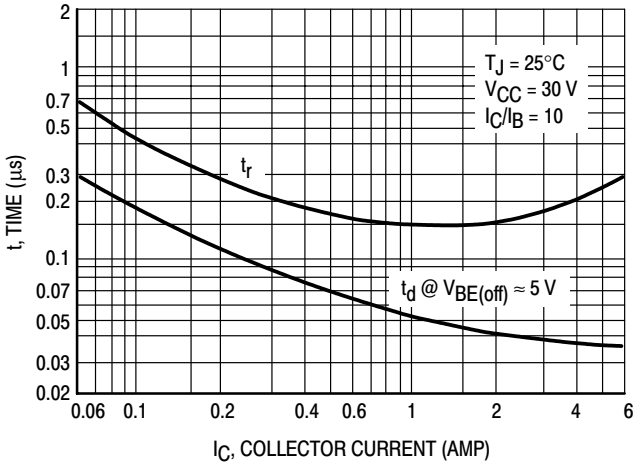


Figure 3. Turn−On Time

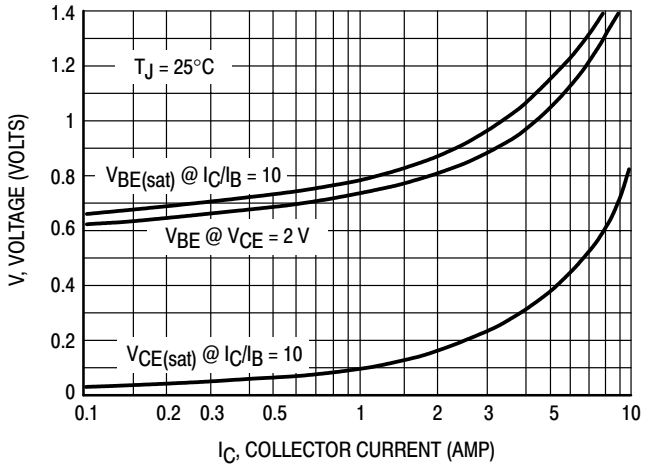


Figure 4. “On” Voltages, MJD3055

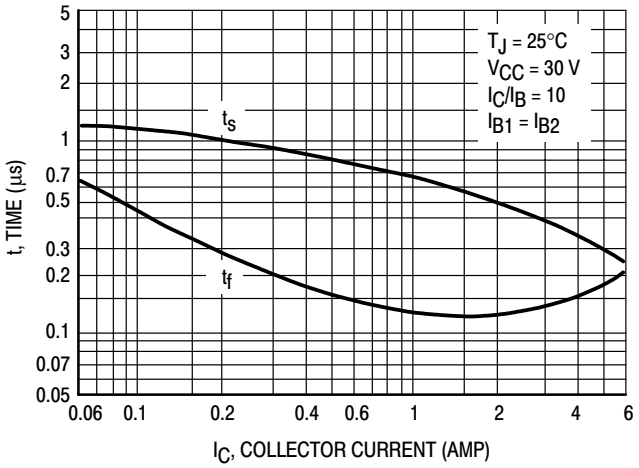


Figure 5. Turn−Off Time

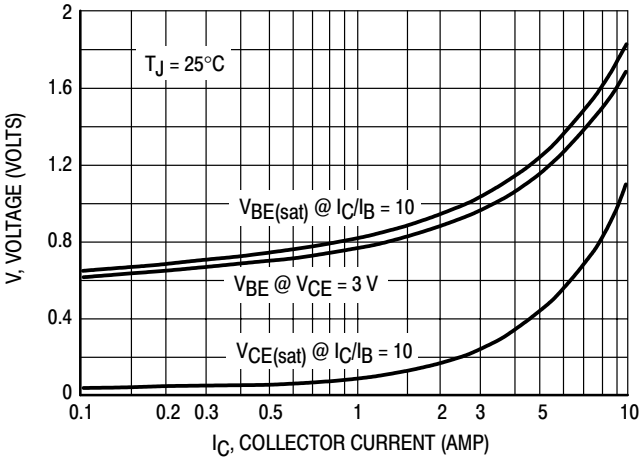


Figure 6. "On" Voltages, MJD2955

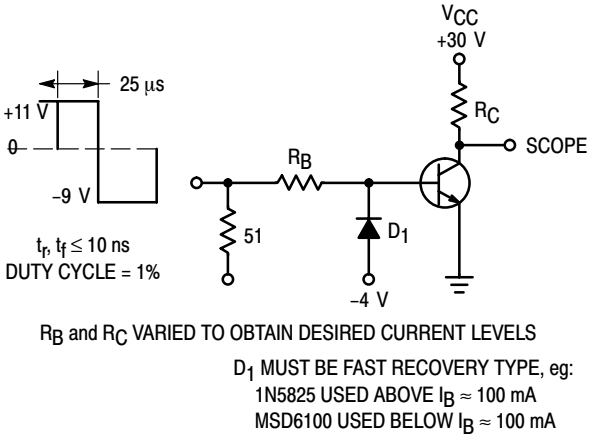


Figure 7. Switching Time Test Circuit

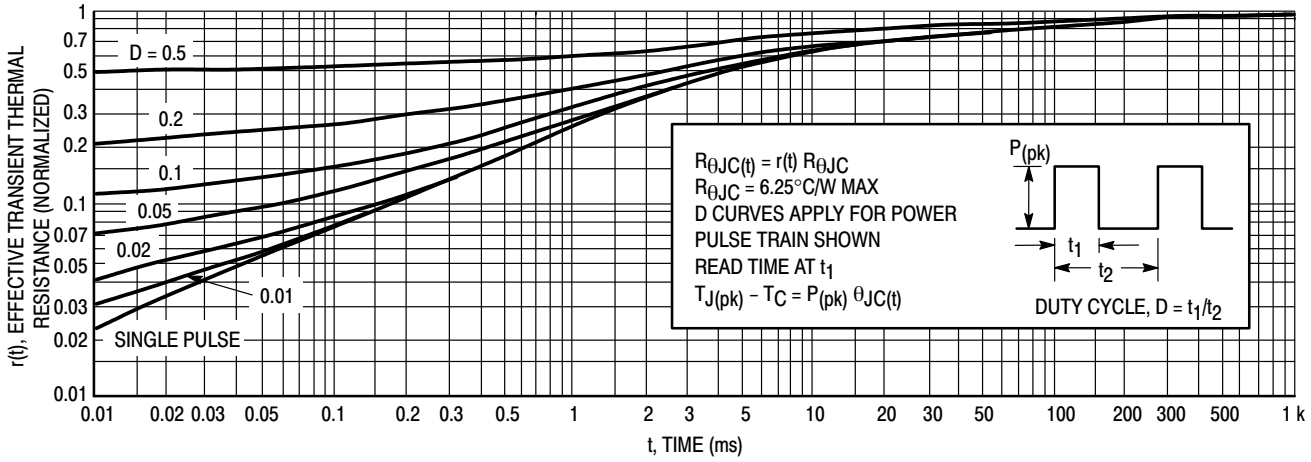


Figure 8. Thermal Response

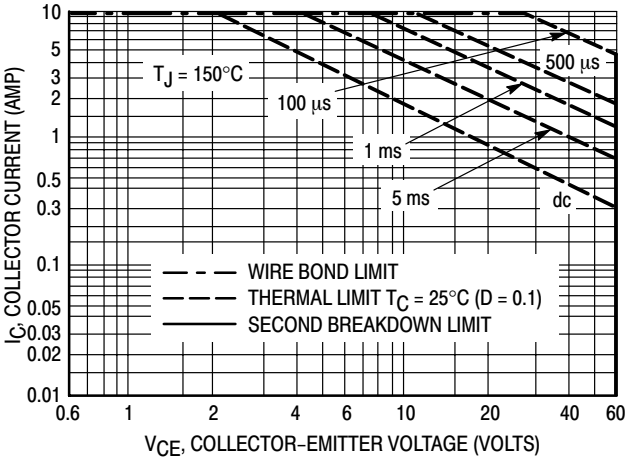


Figure 9. Maximum Forward Bias Safe Operating Area

FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD31, MJD31C (NPN), MJD32, MJD32C (PNP)

MJD31C and MJD32C are Preferred Devices

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

- Pb−Free Packages are Available
- Lead Formed for Surface Mount Applications in Plastic Sleeves
- Straight Lead Version in Plastic Sleeves (“1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage MJD31, MJD32 MJD31C, MJD32C	V_{CEO}	 40 100	Vdc
Collector−Base Voltage MJD31, MJD32 MJD31C, MJD32C	V_{CB}	 40 100	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	3 5	Adc
Base Current	I_B	1	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	8.3	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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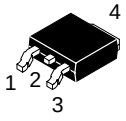
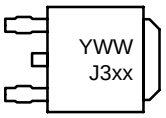
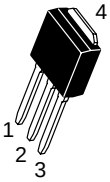
SILICON POWER TRANSISTORS 3 AMPERES 40 AND 100 VOLTS 15 WATTS

MARKING DIAGRAMS

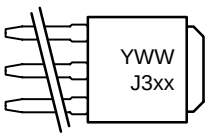


DPAK
CASE 369C
STYLE 1





DPAK−3
CASE 369D
STYLE 1



Y = Year
WW = Work Week
xx = 1, 1C, 2, or 2C

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 450 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 6) (I_C = 30 mAdc, I_B = 0)	MJD31, MJD32 MJD31C, MJD32C	$V_{CEO(sus)}$	 40 100	 − −	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	 MJD31, MJD32 MJD31C, MJD32C	I_{CEO}	−	50	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		ICES	−	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	−	1	mAdc
ON CHARACTERISTICS (Note 6)					
DC Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)		h_{FE}	 25 10	 − 50	−
Collector−Emitter Saturation Voltage (I_C = 3 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	−	1.2	Vdc
Base−Emitter On Voltage (I_C = 3 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	−	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain − Bandwidth Product (Note 7) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3	−	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	−	−

6. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
7. $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

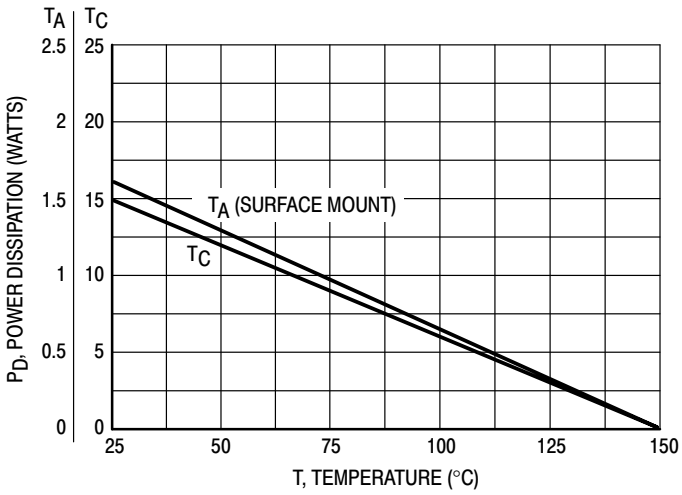
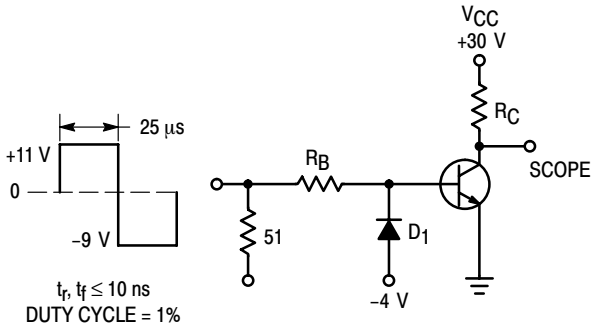


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

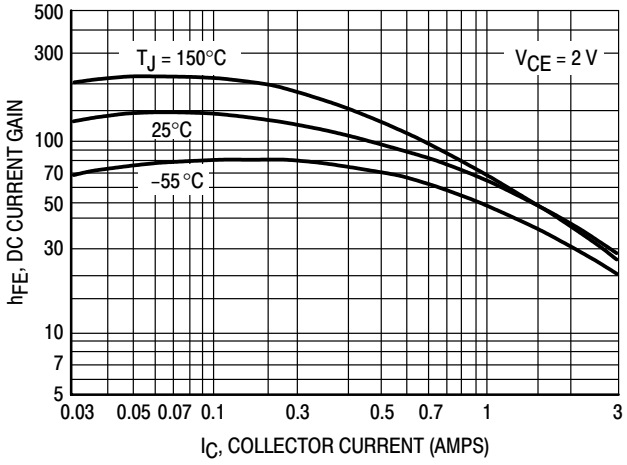


Figure 3. DC Current Gain

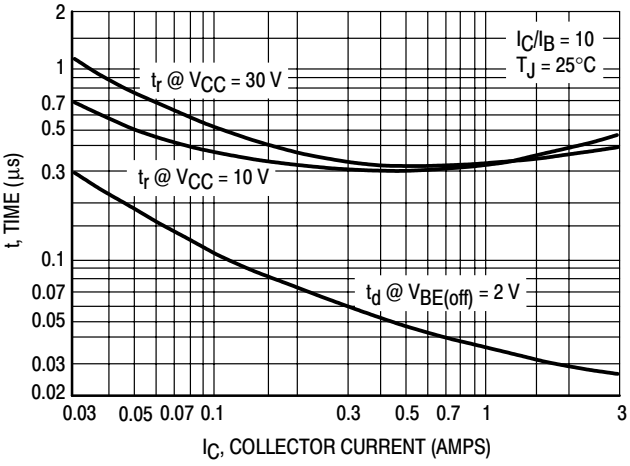


Figure 4. Turn−On Time

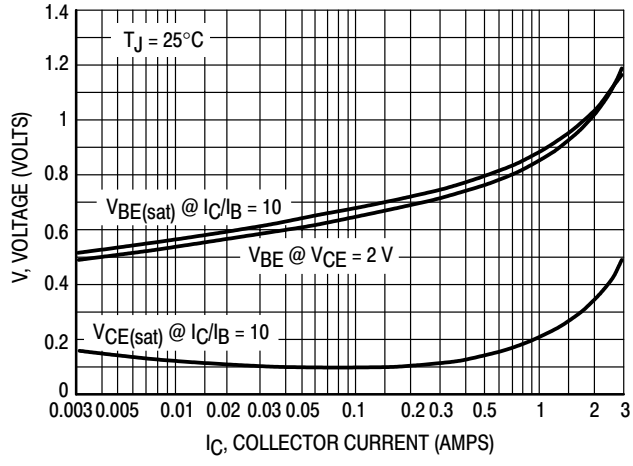


Figure 5. “On” Voltages

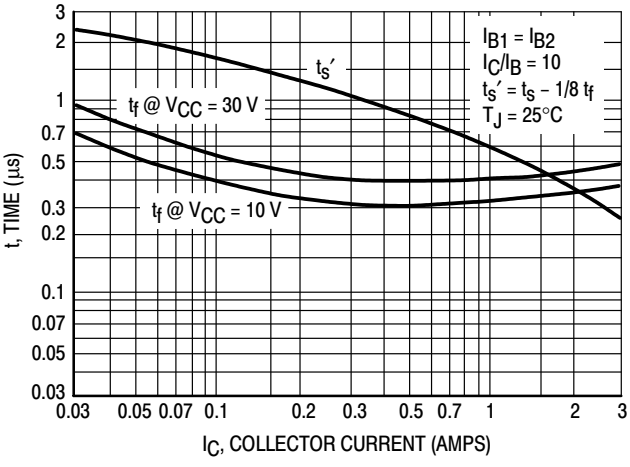


Figure 6. Turn−Off Time

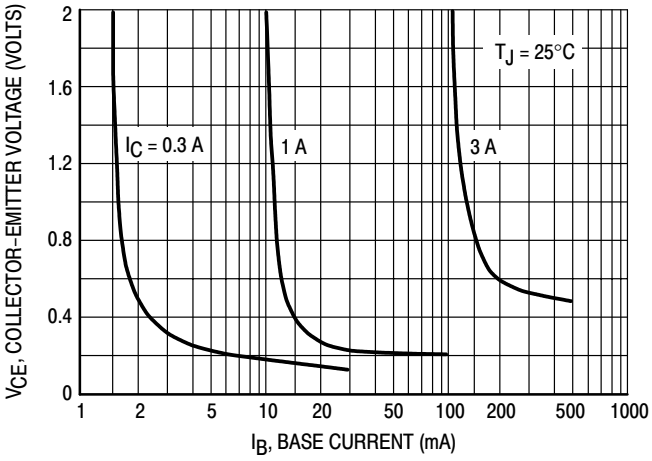


Figure 7. Collector Saturation Region

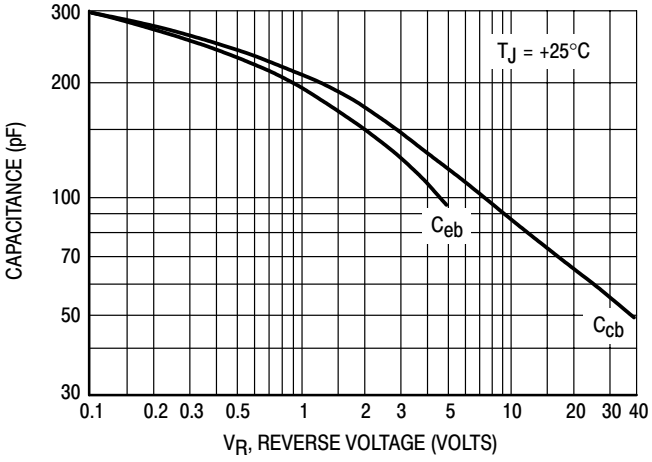


Figure 8. Capacitance

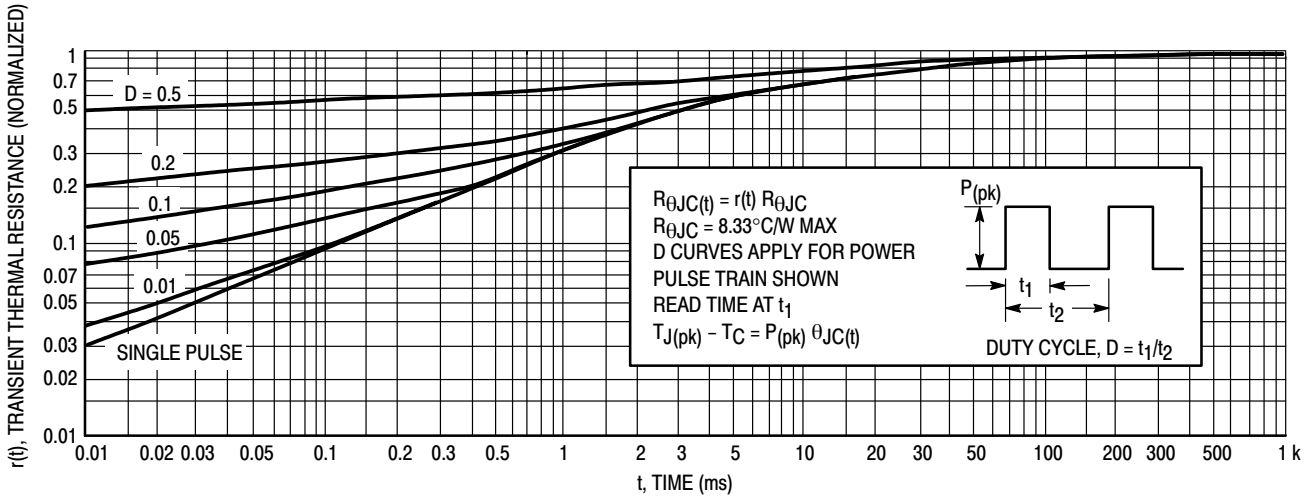


Figure 9. Thermal Response

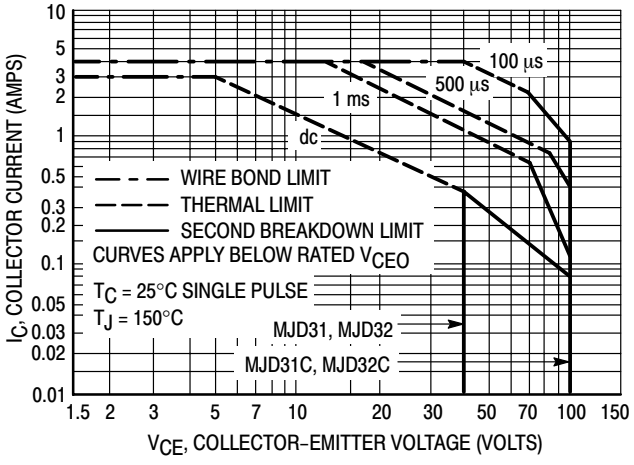


Figure 10. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD31C	DPAK	369C	75 Units / Rail
MJD31CG	DPAK (Pb−Free)	369C	75 Units / Rail
MJD31C1	DPAK−3	369D	75 Units / Rail
MJD31CRL	DPAK	369C	1800 Tape & Reel
MJD31CT4	DPAK	369C	2500 Tape & Reel
MJD31CT4G	DPAK (Pb−Free)	369C	2500 Tape & Reel
MJD31T4	DPAK	369C	2500 Tape & Reel
MJD32C	DPAK	369C	75 Units / Rail
MJD32C1	DPAK−3	369D	75 Units / Rail
MJD32CRL	DPAK	369C	1800 Tape & Reel
MJD32CT4	DPAK	369C	2500 Tape & Reel
MJD32CT4G	DPAK (Pb−Free)	369C	2500 Tape & Reel
MJD32RL	DPAK	369C	1800 Tape & Reel
MJD32RLG	DPAK (Pb−Free)	369C	1800 Tape & Reel
MJD32T4	DPAK	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MJD340 (NPN)
MJD350 (PNP)

Preferred Device

High Voltage Power Transistors

DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

Features

- Pb−Free Packages are Available
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) − $V_{CEO(sus)}$
- 0.5 A Rated Collector Current
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Collector−Base Voltage	V_{CB}	300	Vdc
Emitter−Base Voltage	V_{EB}	3	Vdc
Collector Current − Continuous Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	80	°C/W
Leading Temperature for Soldering Purpose	T_L	260	°C

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

http://onsemi.com

SILICON
POWER TRANSISTORS
0.5 AMPERE
300 VOLTS
15 WATTS

MARKING DIAGRAM

DPAK
CASE 369C
STYLE 1

Y = Year
WW = Work Week
x = 4 or 5

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 452 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 8) (I_C = 1 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	−	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CEO}	−	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)	I_{EBO}	−	0.1	mAdc
ON CHARACTERISTICS (Note 8)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	−

8. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD340	DPAK	369C	75 Units / Rail
MJD340G	DPAK (Pb−Free)	369C	75 Units / Rail
MJD340RL	DPAK	369C	1800 Tape & Reel
MJD340RLG	DPAK (Pb−Free)	369C	1800 Tape & Reel
MJD340T4	DPAK	369C	2500 Tape & Reel
MJD350	DPAK	369C	75 Units / Rail
MJD350T4	DPAK	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

MJD340

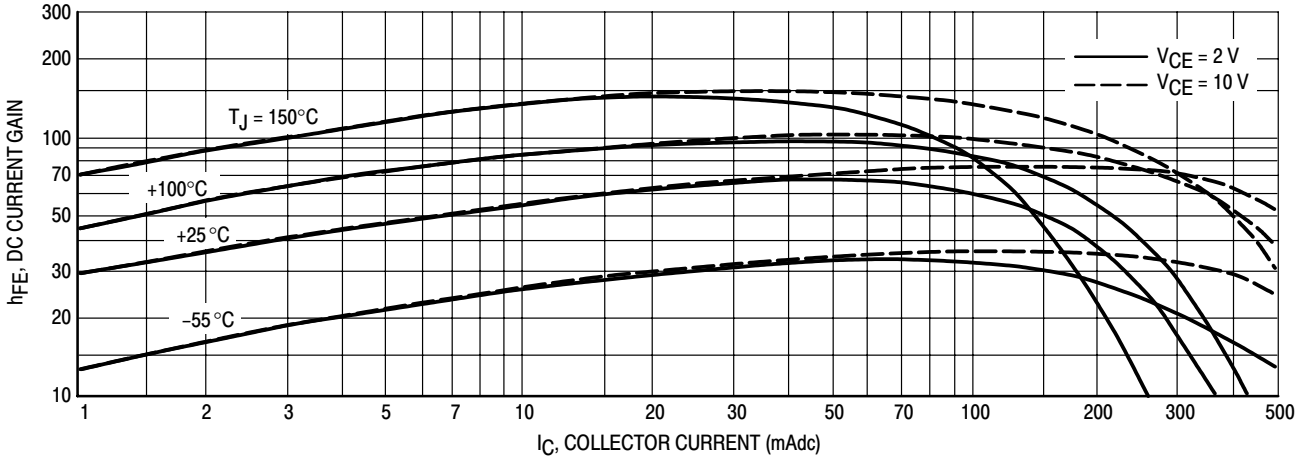


Figure 1. DC Current Gain

MJD340

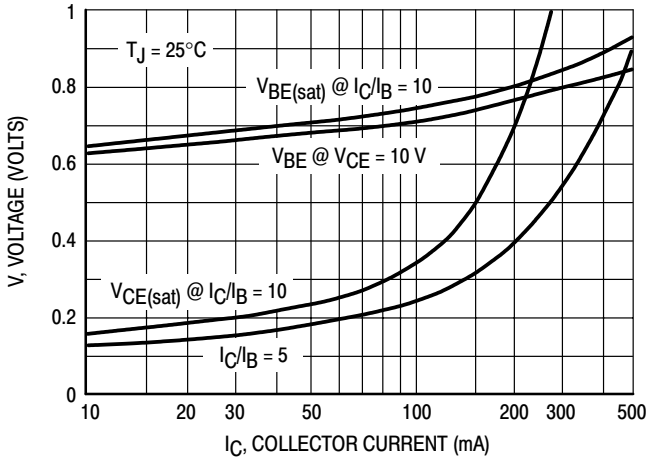


Figure 2. “On” Voltages

MJD350

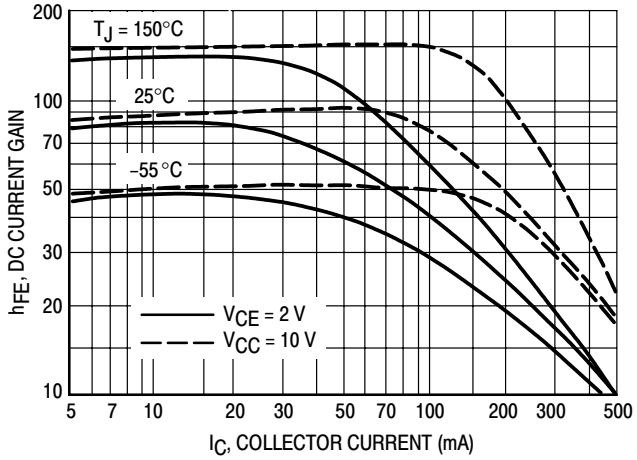


Figure 3. DC Current Gain

MJD350

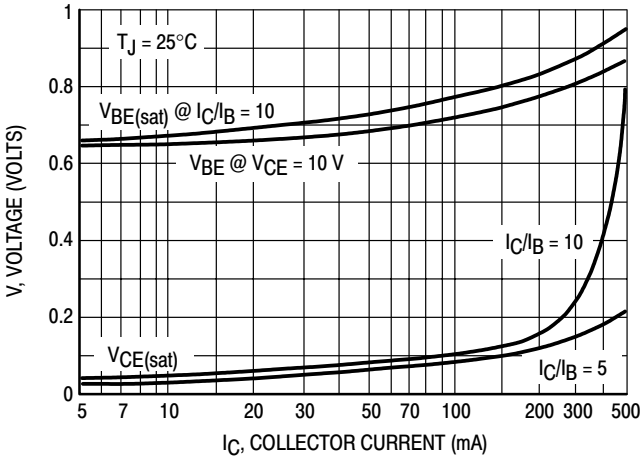


Figure 4. “On” Voltages

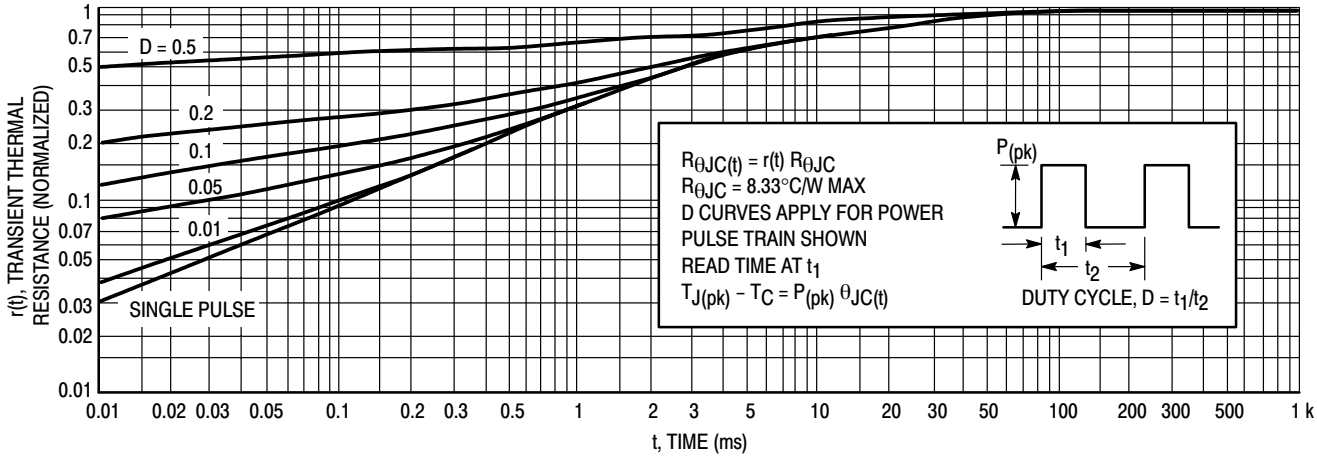


Figure 5. Thermal Response

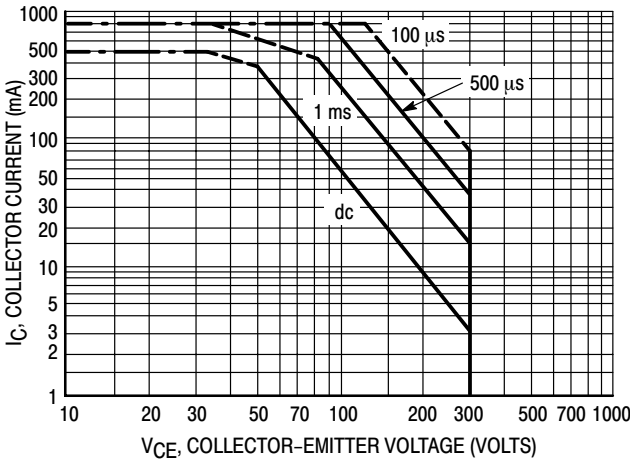


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

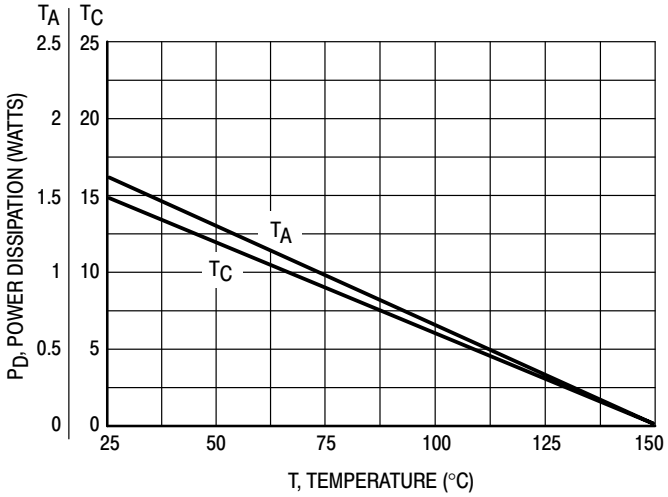


Figure 7. Power Derating

MJD41C (NPN)
MJD42C (PNP)

Preferred Device

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built−in Base − Emitter Resistors
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	6 10	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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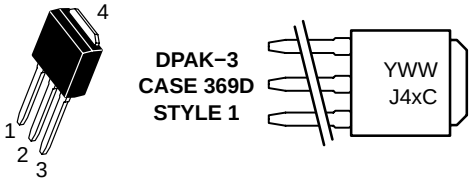
SILICON
POWER TRANSISTORS
6 AMPERES
100 VOLTS
20 WATTS

MARKING DIAGRAMS

DPAK
CASE 369C
STYLE 1



DPAK−3
CASE 369D
STYLE 1

Y = Year
WW = Work Week
x = 1 or 2

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 456 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 9) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	−	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	−	50	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	−	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	0.5	mAdc
ON CHARACTERISTICS (Note 9)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)	h_{FE}	 30 15	 – 75	−
Collector−Emitter Saturation Voltage (I_C = 6 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	−	1.5	Vdc
Base−Emitter On Voltage (I_C = 6 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	−	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (Note 10) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	−	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	20	—	−

9. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
10. $f_T = |h_{fe}| \bullet f_{test}$.

ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD41CRL	DPAK	369C	1800 Tape & Reel
MJD41CT4	DPAK	369C	2500 Tape & Reel
MJD42C	DPAK	369C	75 Units / Rail
MJD42C1	DPAK−3	369D	75 Units / Rail
MJD42CRL	DPAK	369C	1800 Tape & Reel
MJD42CT4	DPAK	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

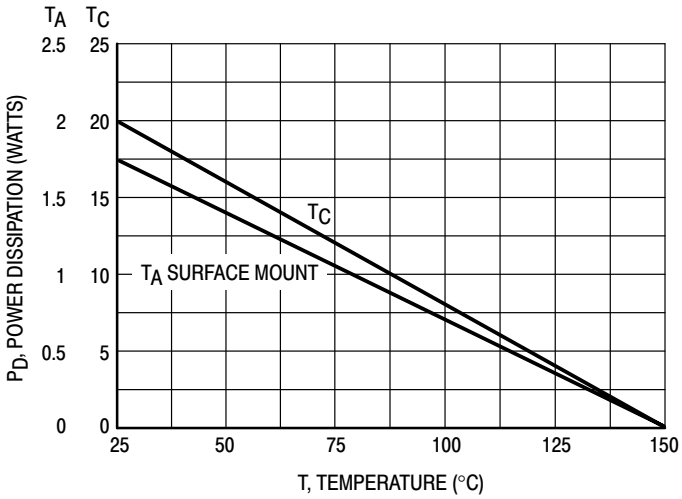
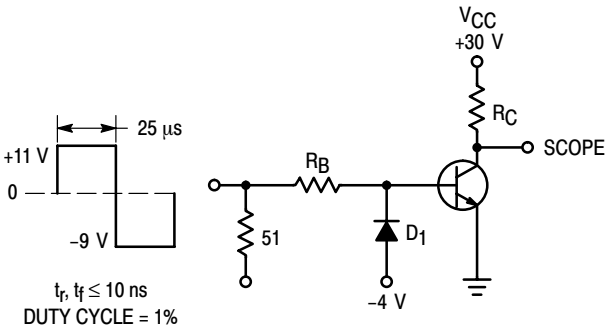


Figure 8. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
MSB5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
REVERSE ALL POLARITIES FOR PNP.

Figure 9. Switching Time Test Circuit

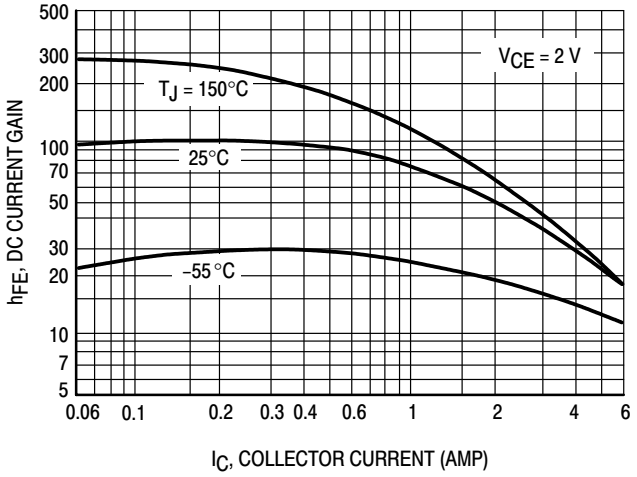


Figure 10. DC Current Gain

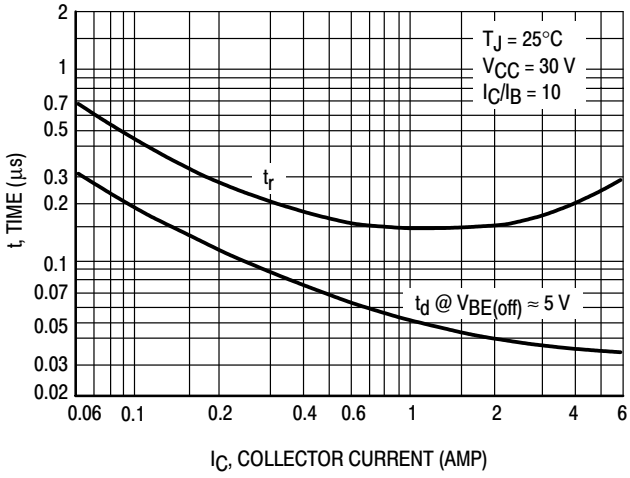


Figure 11. Turn−On Time

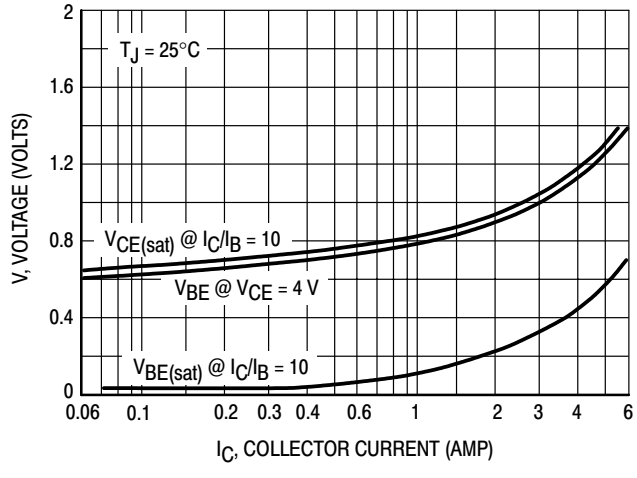


Figure 12. “On” Voltages

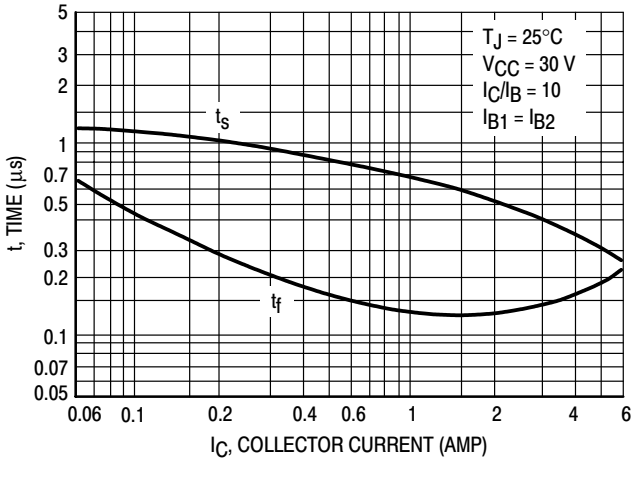


Figure 13. Turn−Off Time

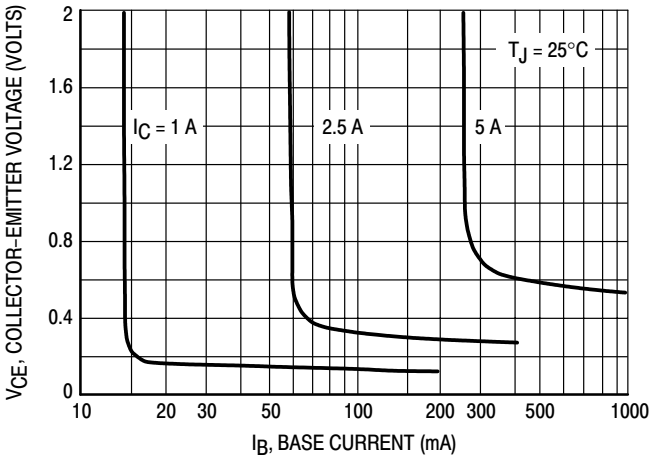


Figure 14. Collector Saturation Region

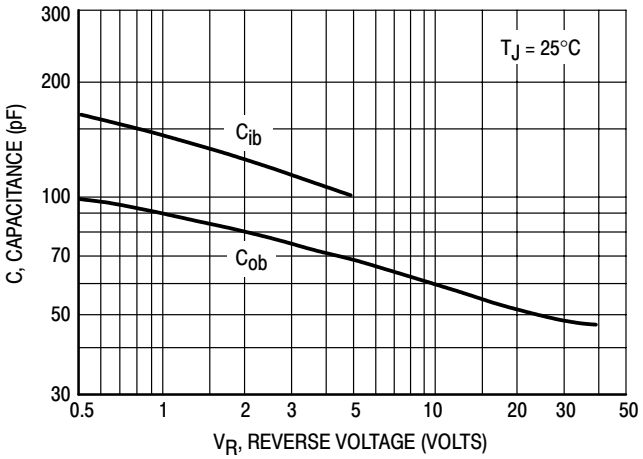


Figure 15. Capacitance

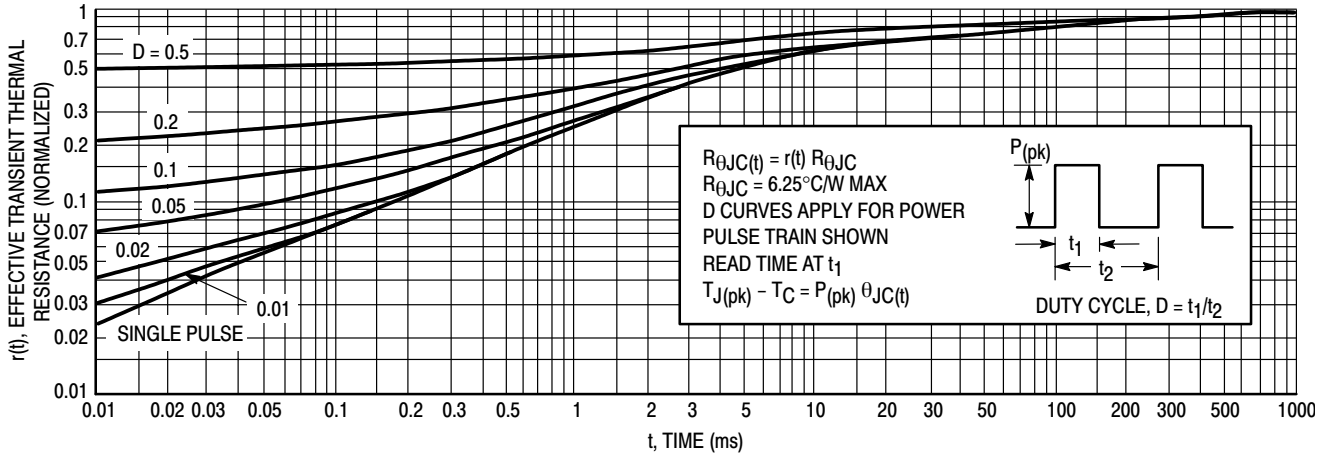


Figure 16. Thermal Response

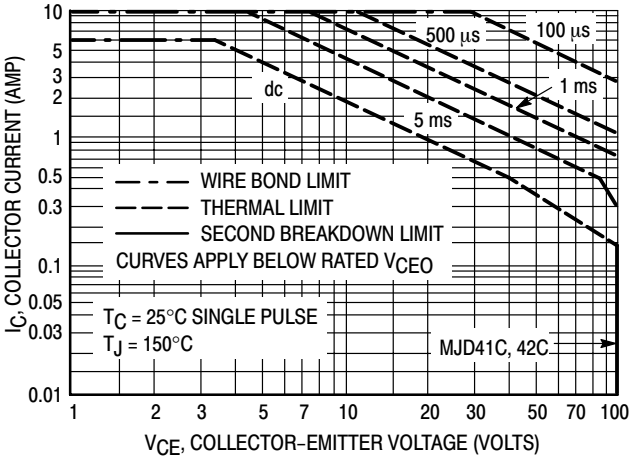


Figure 17. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 17 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJD44E3

Preferred Device

Darlington Power Transistor

DPAK For Surface Mount Applications

Designed for general purpose power and switching output or driver stages in applications such as switching regulators, converters, and power amplifiers.

Features

- Electrically Similar to Popular D44E3 Device
- High DC Gain − 1000 Min @ 5.0 Adc
- Low Sat. Voltage − 1.5 V @ 5.0 Adc
- Compatible With Existing Automatic Pick and Place Equipment
- Epoxy Meets UL 94, V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Emitter−Base Voltage	V_{EB}	7	Vdc
Collector Current − Continuous	I_C	10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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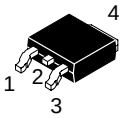
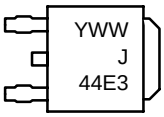
NPN DARLINGTON SILICON POWER TRANSISTORS
10 AMPERES
80 VOLTS
20 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJD44E3T4	DPAK	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	–	–	10	μA
Emitter Cutoff Current (V_{EB} = 7 Vdc)	I_{EBO}	–	–	1	μA
ON CHARACTERISTICS					
Collector−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 10 mAdc) (I_C = 10 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	 – –	 – –	 1.5 2	Vdc
Base−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 10 mAdc)	$V_{BE(sat)}$	–	–	2.5	Vdc
DC Current Gain (V_{CE} = 5 Vdc, I_C = 5 Adc)	h_{FE}	1000	–	–	–
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	C_{cb}	–	–	130	pF
SWITCHING TIMES					
Delay and Rise Times (I_C = 10 Adc, I_{B1} = 20 mAdc)	$t_d + t_r$	–	0.6	–	μs
Storage Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_s	–	2	–	μs
Fall Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_f	–	0.5	–	μs

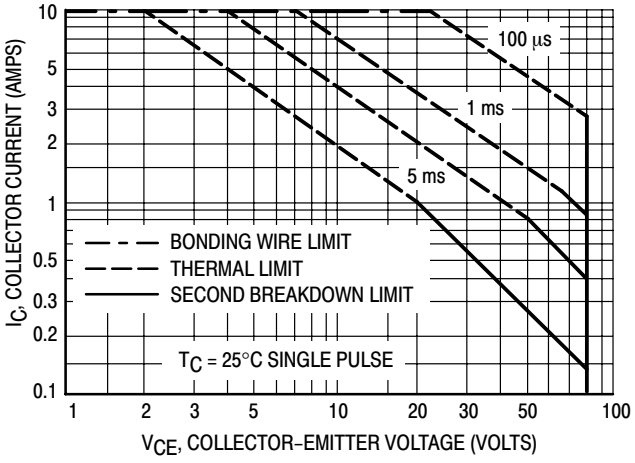


Figure 1. Maximum Forward Bias Safe Operating Area

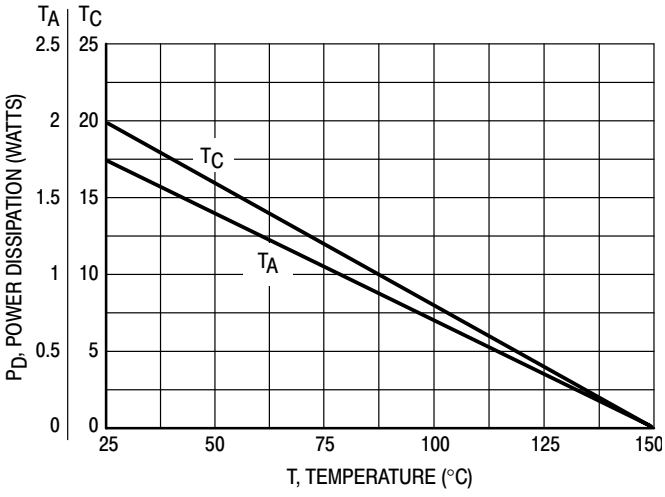


Figure 2. Power Derating

MJD44H11 (NPN)
MJD45H11 (PNP)

Preferred Device

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

Features

- Pb−Free Packages are Available
- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount (“T4” Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 Volt Max @ 8.0 Amperes
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	8 16	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

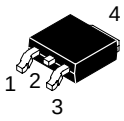
*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

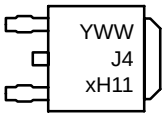
http://onsemi.com

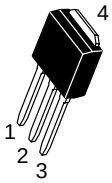
SILICON
POWER TRANSISTORS
8 AMPERES
80 VOLTS
20 WATTS

MARKING DIAGRAMS

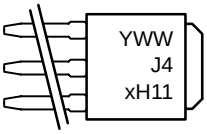


DPAK
CASE 369C
STYLE 1





DPAK−3
CASE 369D
STYLE 1



Y = Year
WW = Work Week
x = 4 or 5

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 463 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	−	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	−	−	10	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	−	−	50	μA
ON CHARACTERISTICS						
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	−	−	1	Vdc
Base−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	−	−	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	−	−	−
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	−	−	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJD44H11 MJD45H11	C_{cb}	 −	 130	 −	pF
			−	230	−	
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJD44H11 MJD45H11	f_T	 −	 50	 −	MHz
			−	40	−	
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJD44H11 MJD45H11	$t_d + t_r$	 −	 300	 −	ns
			−	135	−	
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t_s	 −	 500	 −	ns
			−	500	−	
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t_f	 −	 140	 −	ns
			−	100	−	

ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD44H11	DPAK	369C	75 Units / Rail
MJD44H11−001	DPAK−3	369D	75 Units / Rail
MJD44H11G	DPAK (Pb−Free)	369C	75 Units / Rail
MJD44H11RL	DPAK	369C	1800 Tape & Reel
MJD44H11T4	DPAK	369C	2500 Tape & Reel
MJD44H11T4G	DPAK (Pb−Free)	369C	2500 Tape & Reel
MJD44H11T5	DPAK	369C	2500 Tape & Reel
MJD45H11	DPAK	369C	75 Units / Rail
MJD45H11−001	DPAK−3	369D	75 Units / Rail
MJD45H11G	DPAK (Pb−Free)	369C	75 Units / Rail
MJD45H11RL	DPAK	369C	1800 Tape & Reel
MJD45H11T4	DPAK	369C	2500 Tape & Reel
MJD45H11T4G	DPAK (Pb−Free)	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

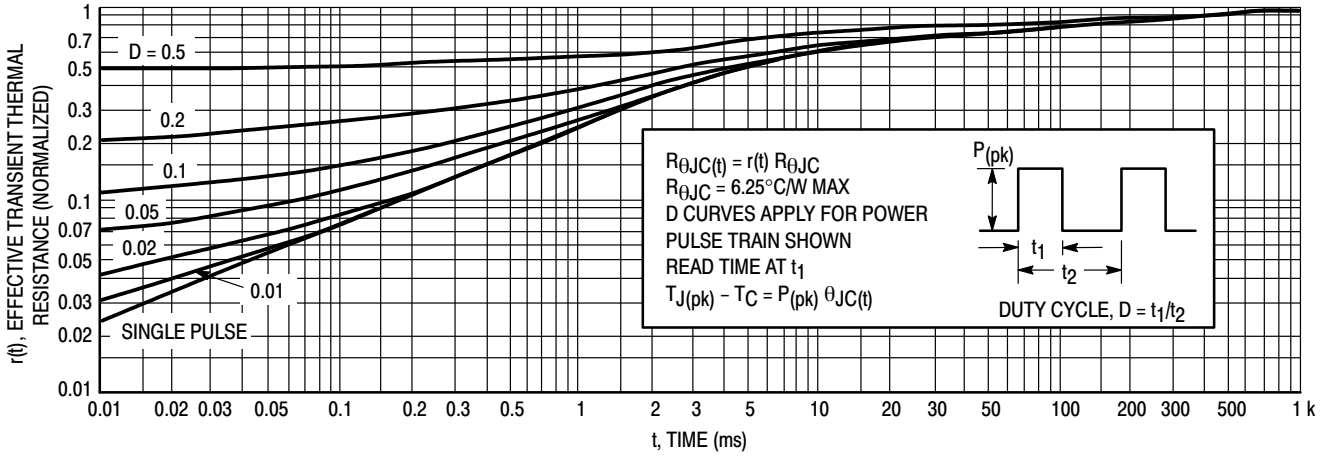


Figure 1. Thermal Response

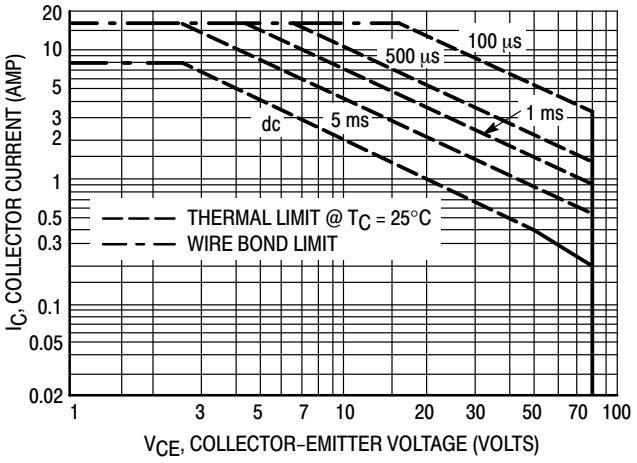


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

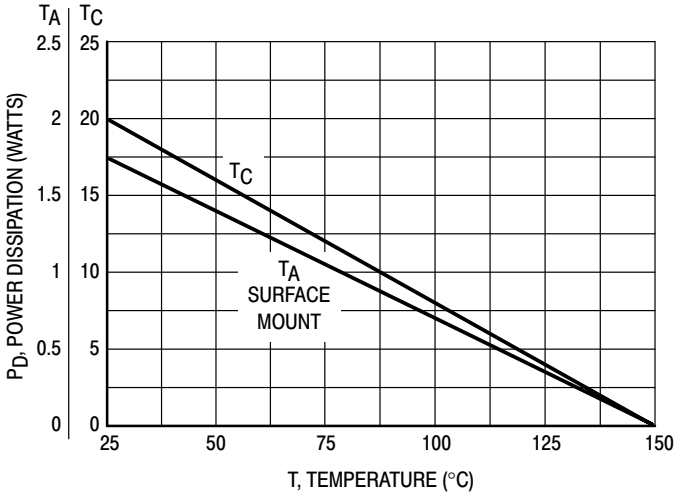


Figure 3. Power Derating

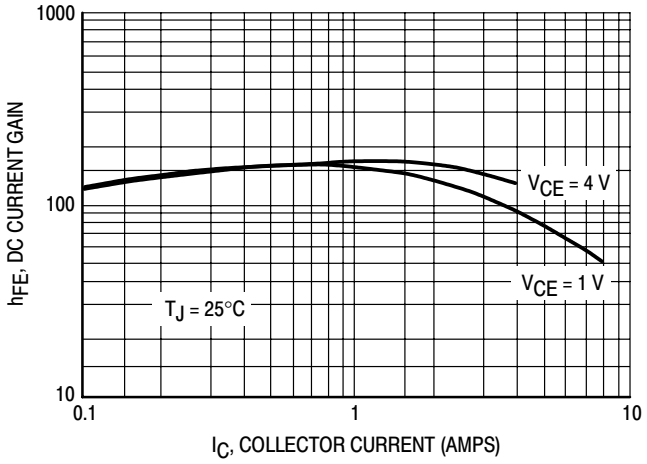


Figure 4. MJD44H11 DC Current Gain

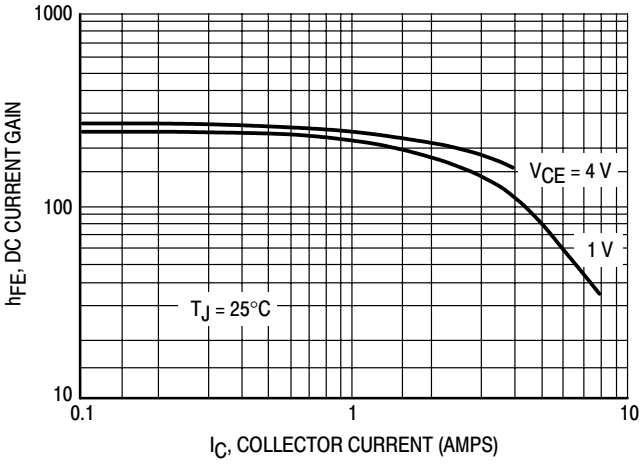


Figure 5. MJD45H11 DC Current Gain

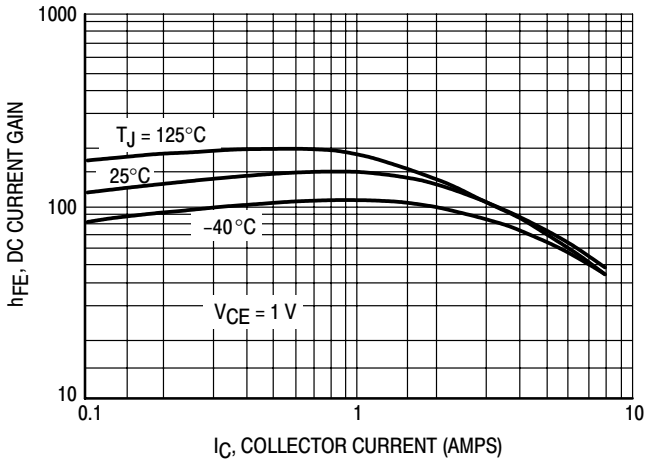


Figure 6. MJD44H11 Current Gain versus Temperature

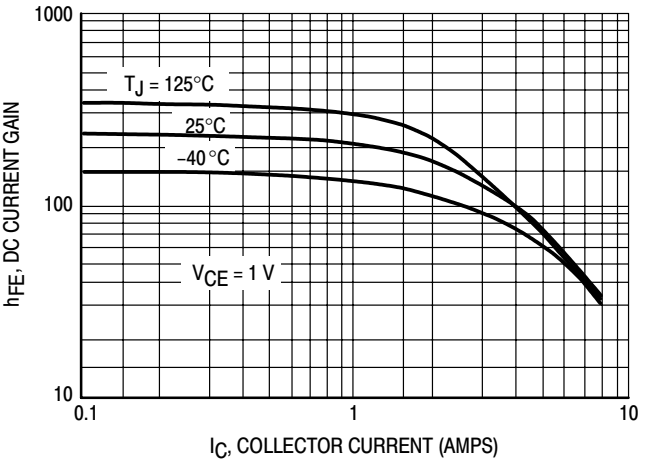


Figure 7. MJD45H11 Current Gain versus Temperature

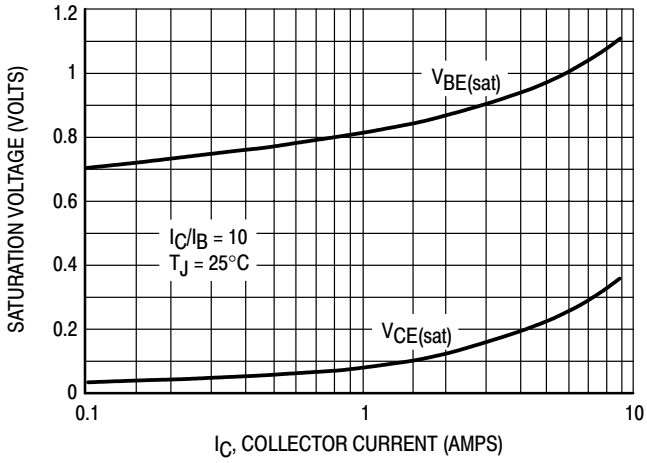


Figure 8. MJD44H11 On−Voltages

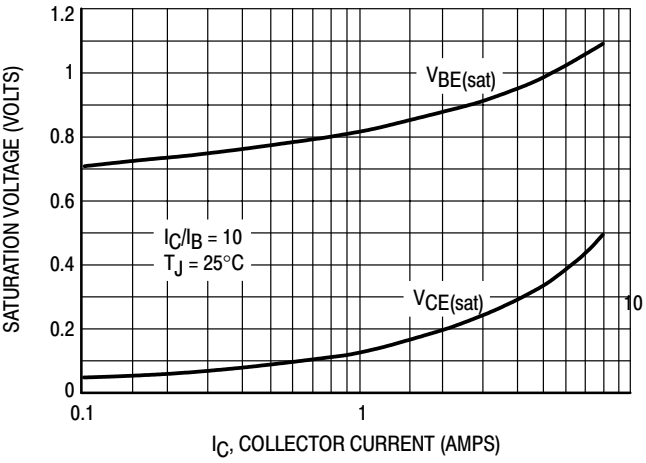


Figure 9. MJD45H11 On−Voltages

MJD47, MJD50

Preferred Device

High Voltage Power Transistors

DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) − $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage MJD47 MJD50	V_{CEO}	 250 400	Vdc
Collector−Base Voltage MJD47 MJD50	V_{CB}	 350 500	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	1 2	Adc
Base Current	I_B	0.6	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.0125	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

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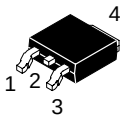
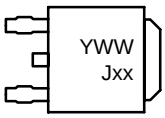
NPN SILICON POWER TRANSISTORS 1 AMPERE 250, 400 VOLTS 15 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week
xx = 47 or 50

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 467 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 11) (I_C = 30 mAdc, I_B = 0)	MJD47 MJD50	$V_{CEO(sus)}$	 250 400	 − −	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJD47 MJD50	I_{CEO}	 − −	 0.2 0.2	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	 MJD47 MJD50	I_{CES}	 − −	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	−	1	mAdc
ON CHARACTERISTICS (Note 11)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 −	−
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	−	1	Vdc
Base−Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2 MHz)		f_T	10	−	MHz
Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	25	−	−

11. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ORDERING INFORMATION

Device	Package	Shipping†
MJD47	369C	75 Units / Rail
MJD47T4	369C	2500 Tape & Reel
MJD50	369C	75 Units / Rail
MJD50T4	369C	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

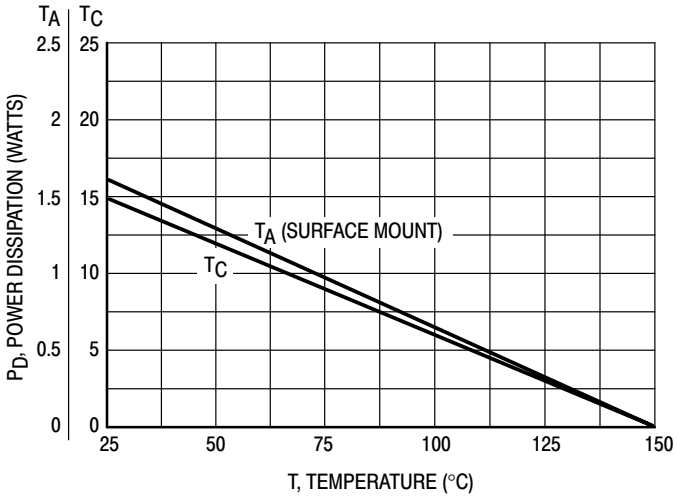


Figure 1. Power Derating

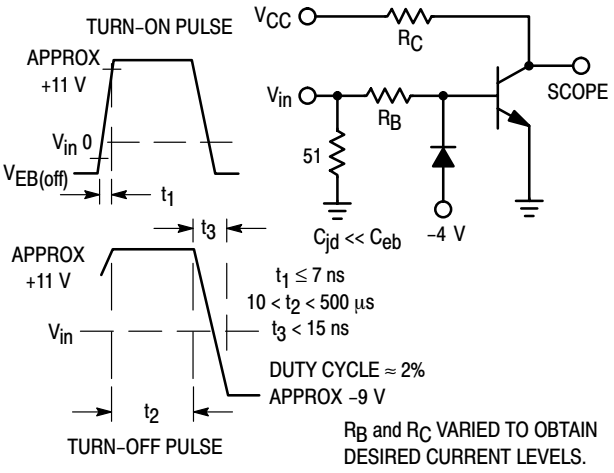


Figure 2. Switching Time Equivalent Circuit

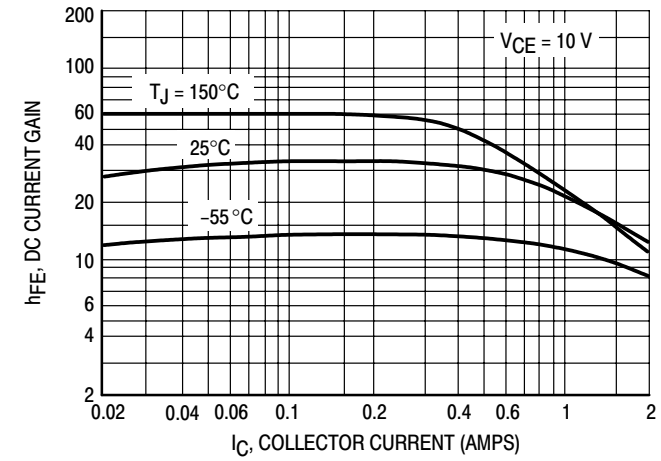


Figure 3. DC Current Gain

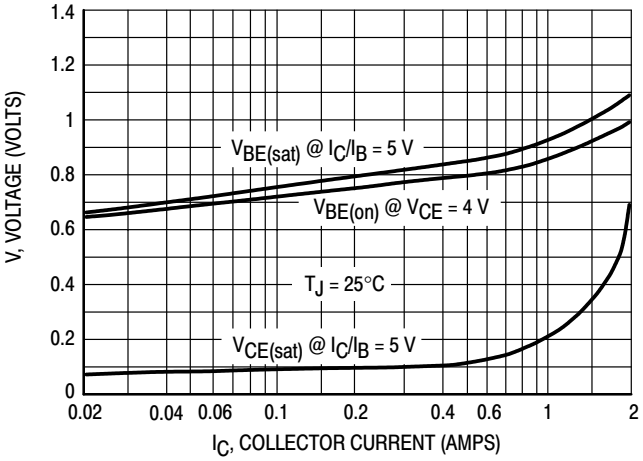


Figure 4. “On” Voltages

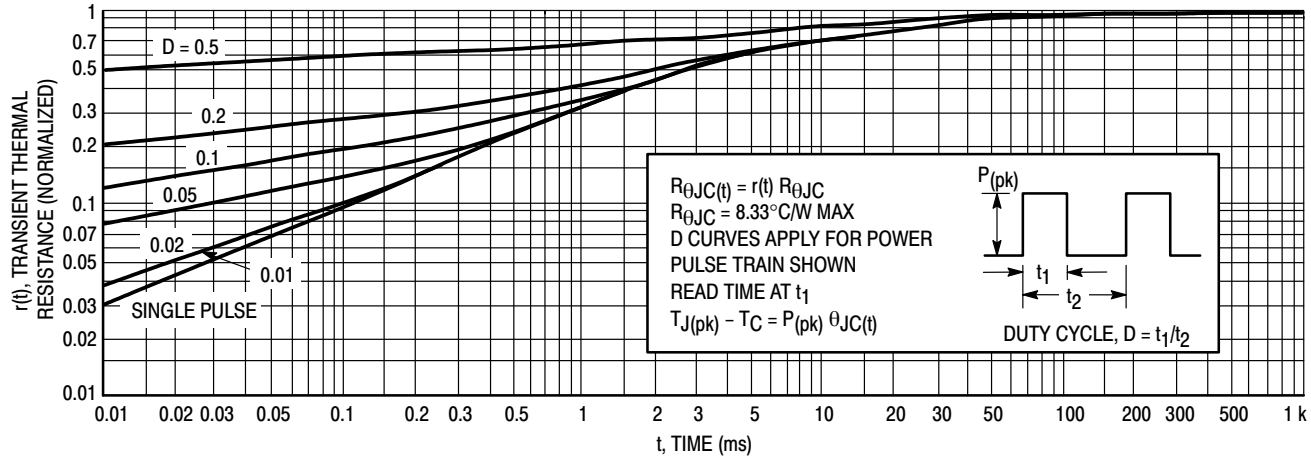


Figure 5. Thermal Response

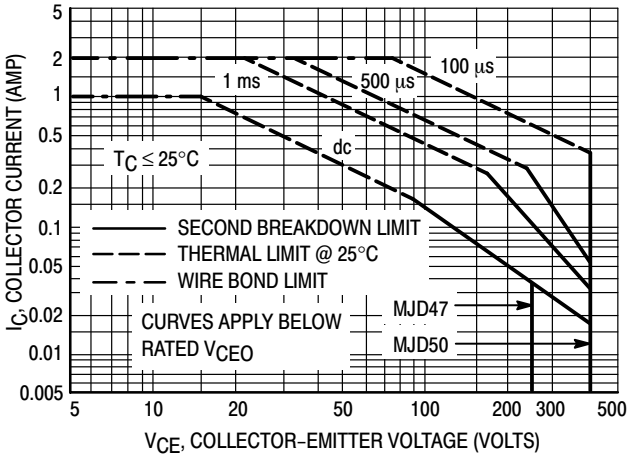


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

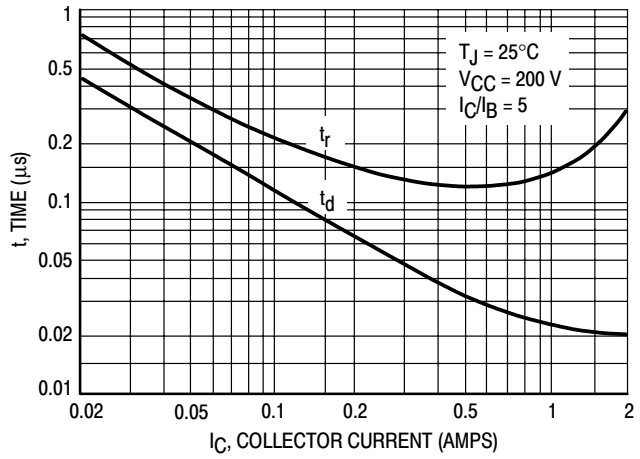


Figure 7. Turn−On Time

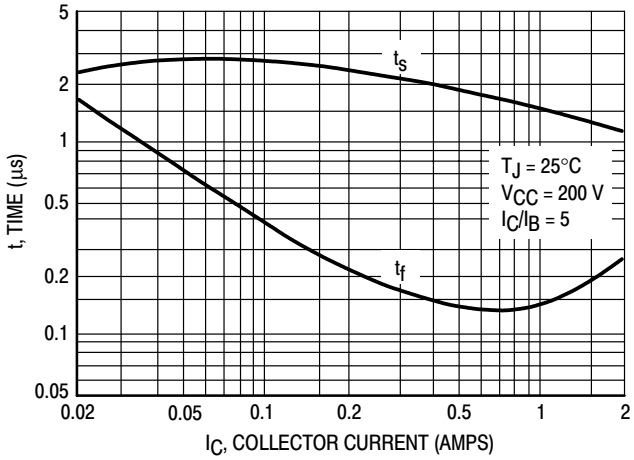


Figure 8. Turn-Off Time

MJD5731

Preferred Device

High Voltage PNP Silicon Power Transistors

Designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

Features

- 350 V (Min) − $V_{CEO(sus)}$
- 1.0 A Rated Collector Current
- PNP Complements to the MJD47 thru MJD50 Series
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	350	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	1.0 3.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.0125	W W/°C
Unclamped Inductive Load Energy (See Figure)	E	20	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering	T_L	260	°C

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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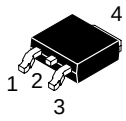
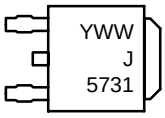
SILICON POWER TRANSISTORS 1.0 AMPERES 350 VOLTS 15 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJD5731T4	DPAK	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 12) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	350	–	Vdc
Collector Cutoff Current (V_{CE} = 250 Vdc, I_B = 0)	I_{CEO}	–	0.1	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	I_{CES}	–	0.01	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	0.5	mAdc
ON CHARACTERISTICS (Note 12)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)	h_{FE}	 30 10	 175 –	–
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)	f_T	10	–	MHz
Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	–	–

12. Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.

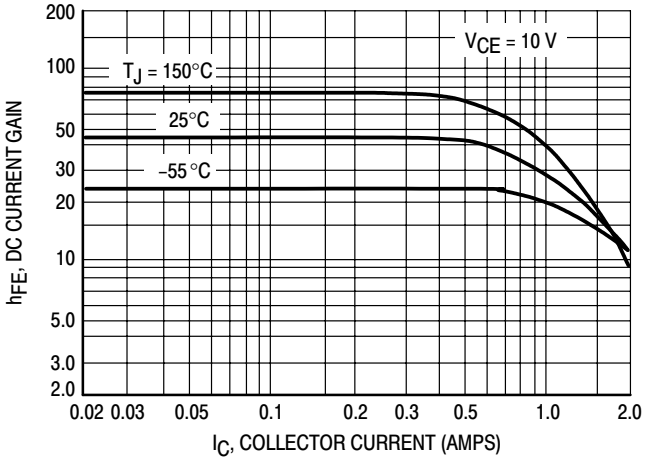


Figure 1. DC Current Gain

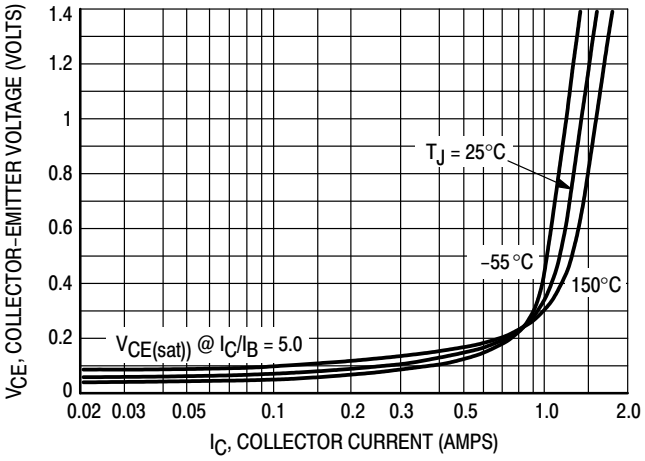


Figure 2. Collector−Emitter Saturation Voltage

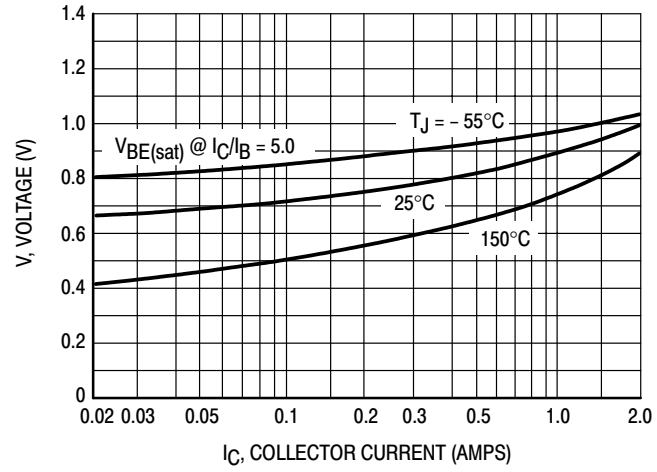


Figure 3. Base−Emitter Voltage

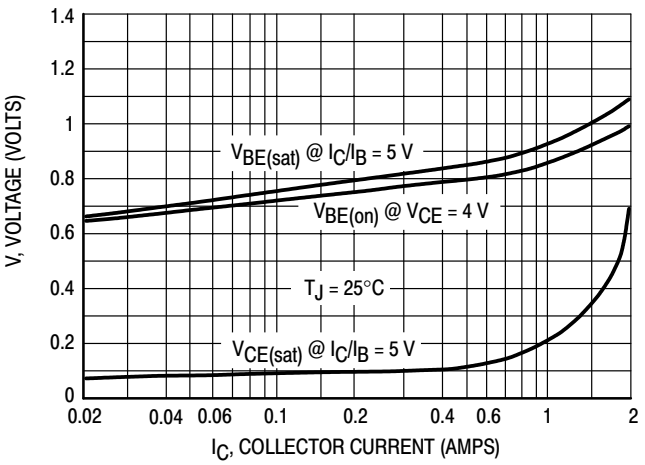


Figure 4. "On" Voltages

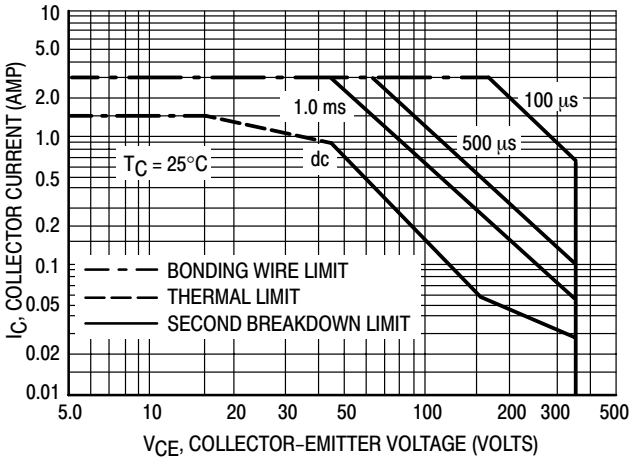


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

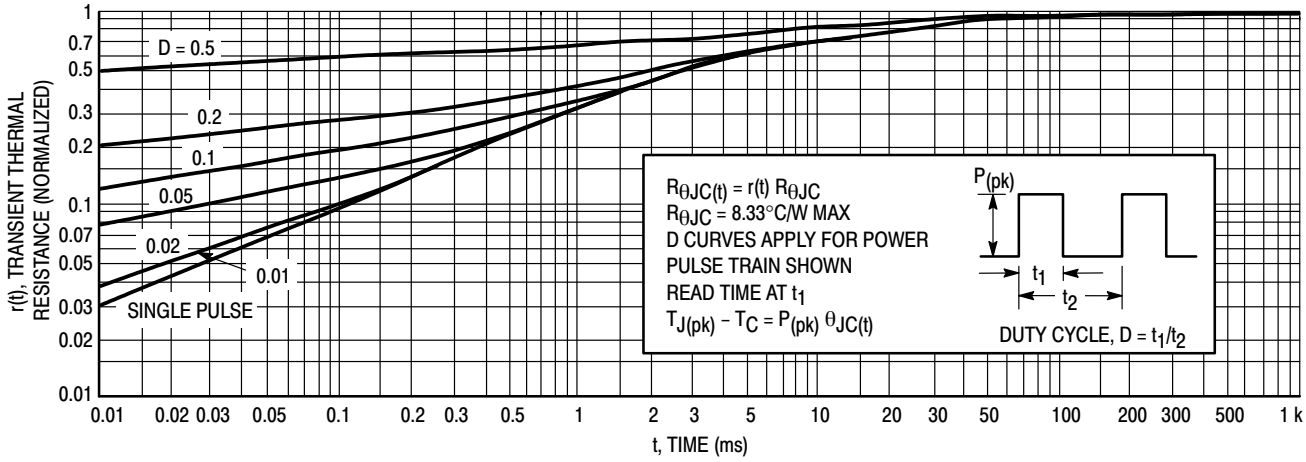


Figure 6. Thermal Response

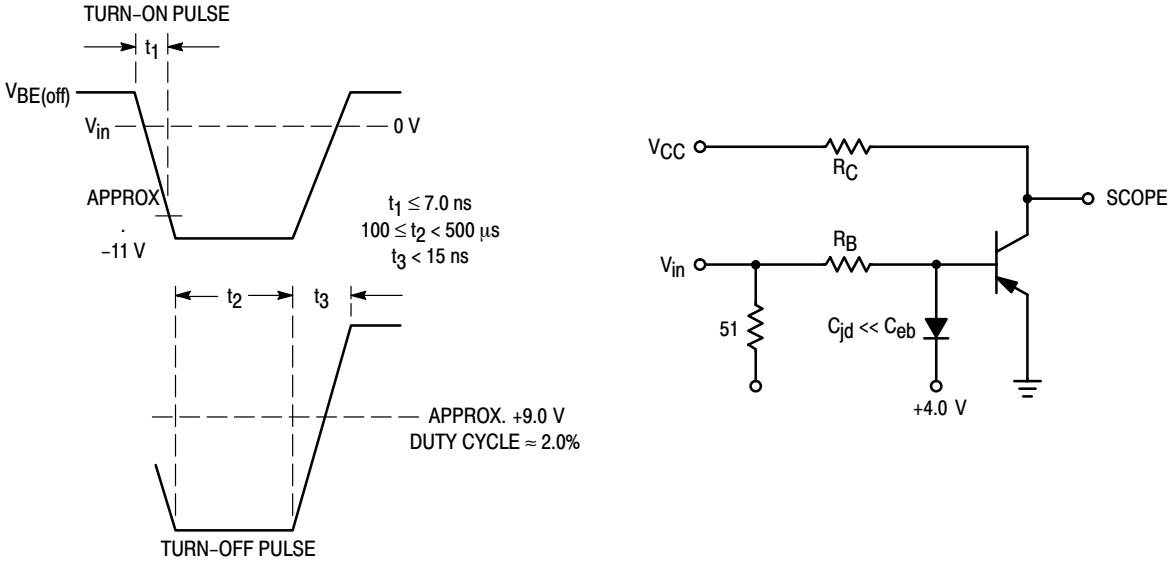


Figure 7. Switching Time Equivalent Circuit

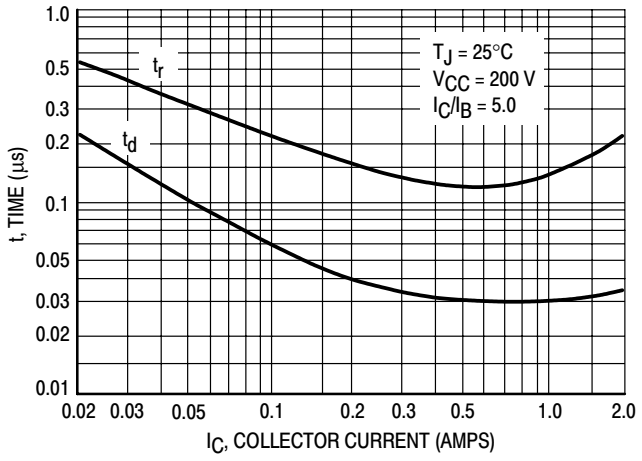


Figure 8. Turn−On Resistive Switching Times

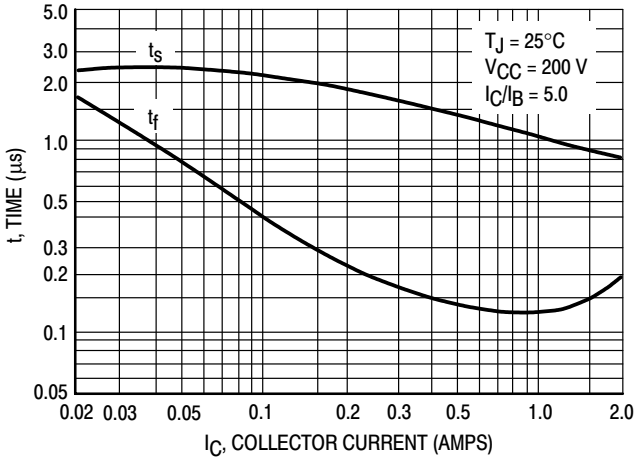
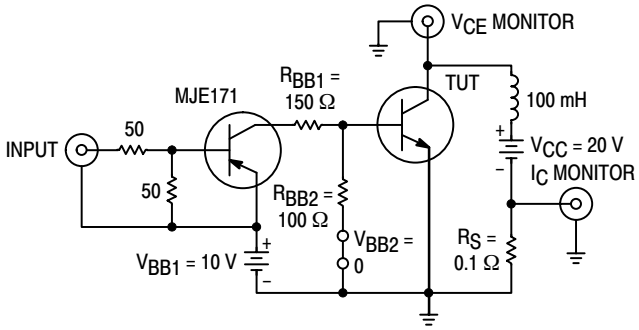


Figure 9. Resistive Turn−Off Switching Times

Test Circuit



Voltage and Current Waveforms

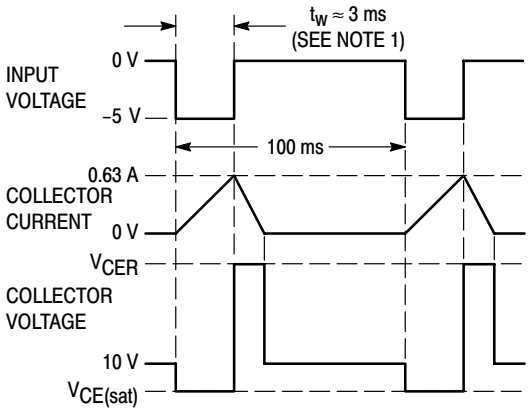


Figure 10. Inductive Load Switching

MJD6039

Darlington Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“−1” Suffix)
- Available on 16 mm Tape and Reel for Automatic Handling (“T4” Suffix)
- Monolithic Construction With Built−in Base−Emitter Shunt Resistors
- High DC Current Gain − h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Collector−Base Voltage	V_{CB}	80	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	4 8	Adc
Base Current	I_B	100	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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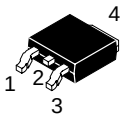
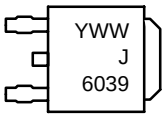
SILICON
POWER TRANSISTORS
4 AMPERES
80 VOLTS
20 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJD6039T4	DPAK	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	−	Vdc
Collector−Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	−	10	μAdc
ON CHARACTERISTICS (Note 13)				
DC Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc) (I_C = 2 Adc, V_{CE} = 4 Vdc)	h_{FE}	 1000 500	 − −	−
Collector−Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc)	$V_{CE(sat)}$	−	2.5	Vdc
Base−Emitter On Voltage (I_C = 2 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	−	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	25	−	−
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	−	100	pF

13. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

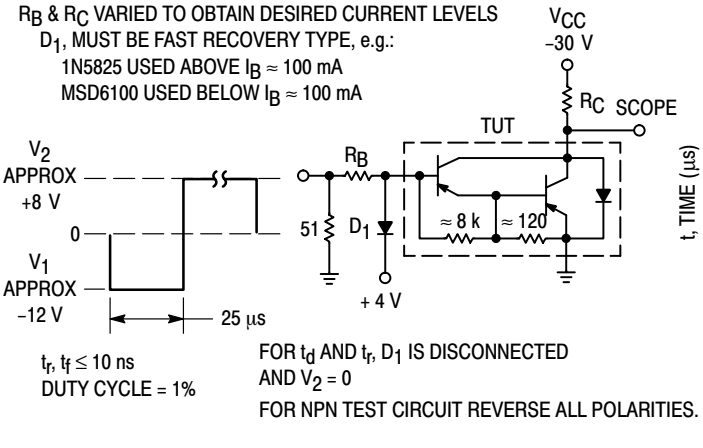


Figure 11. Switching Times Test Circuit

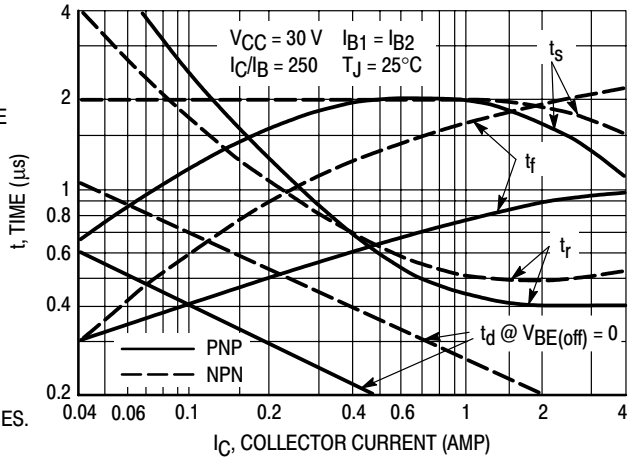


Figure 12. Switching Times

TYPICAL ELECTRICAL CHARACTERISTICS

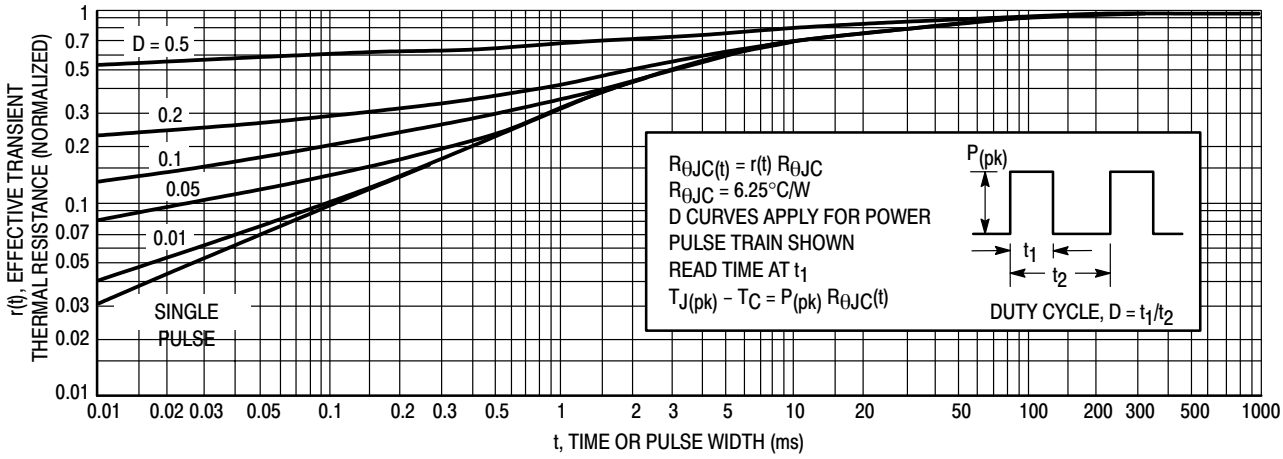


Figure 13. Thermal Response

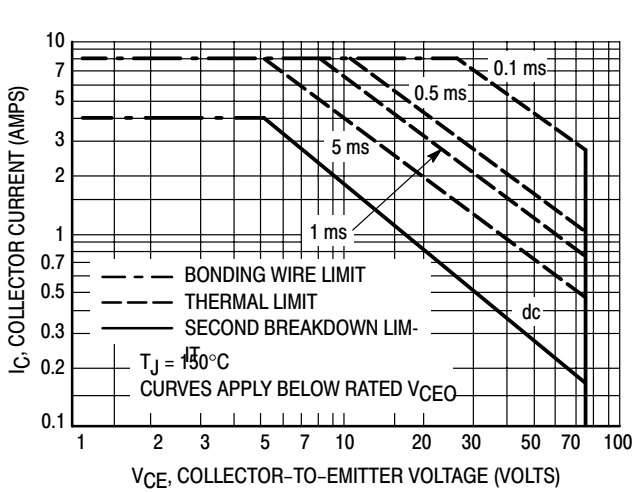


Figure 14. Maximum Rated Forward Biased Safe Operating Area

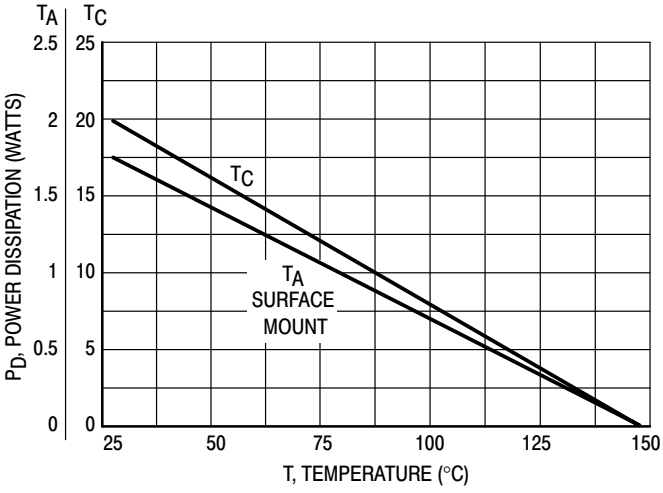


Figure 15. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 16 and 17 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 15. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

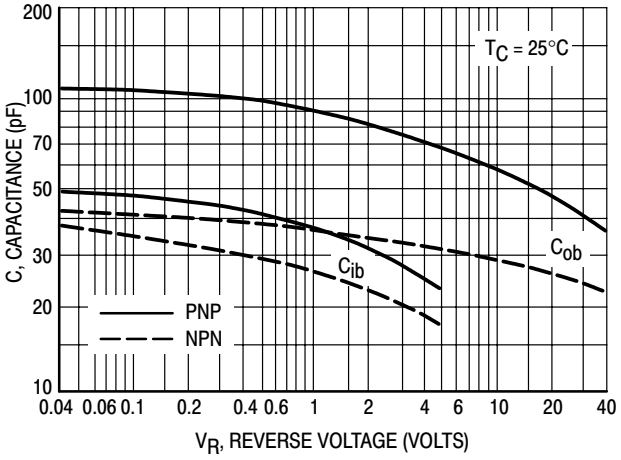


Figure 16. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

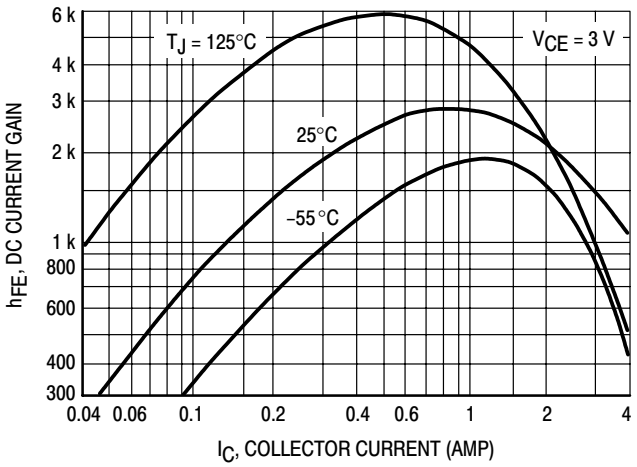


Figure 17. DC Current Gain

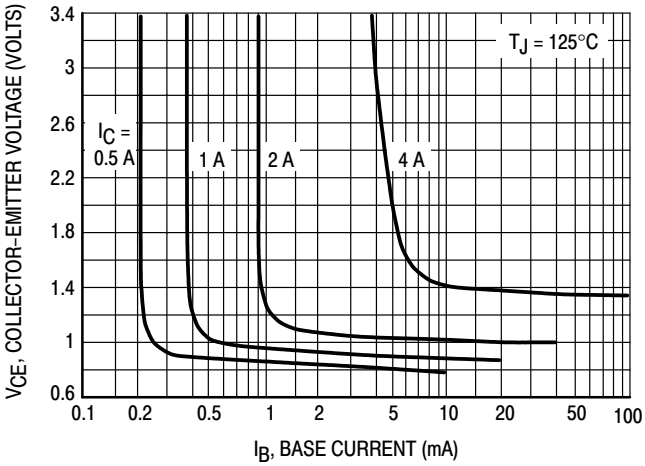


Figure 18. Collector Saturation Region

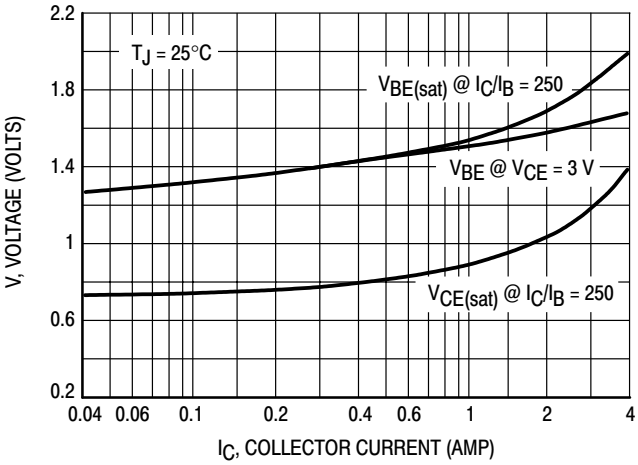


Figure 19. “On” Voltages

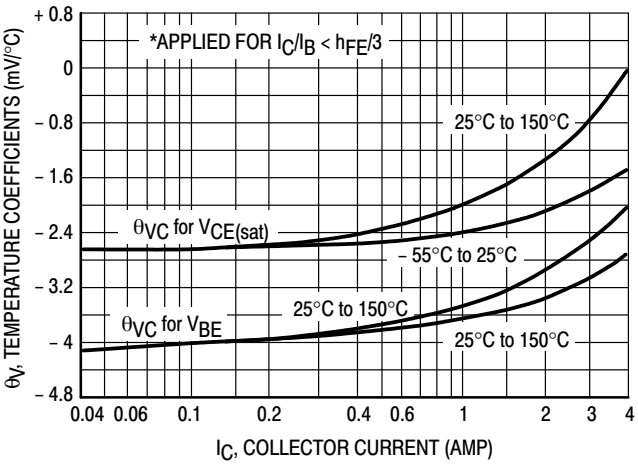


Figure 20. Temperature Coefficients

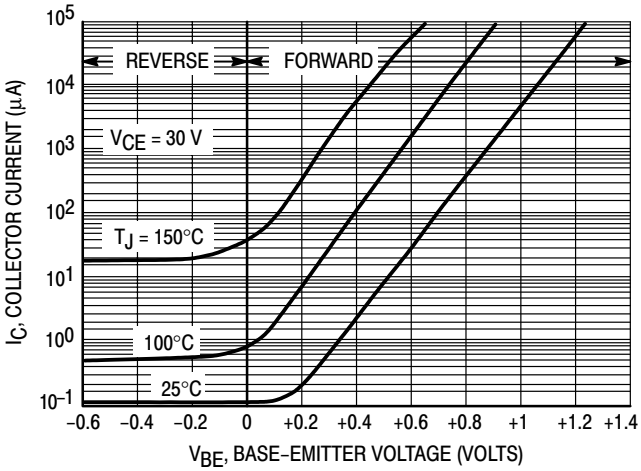


Figure 21. Collector Cut−Off Region

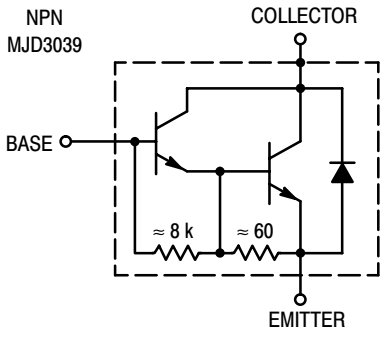


Figure 22. Darlington Schematic

MJE13003

SWITCHMODE™ Series NPN Silicon Power Transistor

These devices are designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C
  t_c @ 1 A, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous − Peak (Note 1.)	I_C I_{CM}	1.5 3	Adc
Base Current − Continuous − Peak (Note 1.)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current − Continuous − Peak (Note 1.)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.4 11.2	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

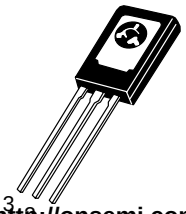
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	°C/W
Maximum Load Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ON Semiconductor®

http://onsemi.com

1.5 AMPERES
NPN SILICON POWER TRANSISTORS
300 AND 400 VOLTS
40 WATTS



http://onsemi.com

TO−225
CASE 77
STYLE 3

MARKING DIAGRAM

Y = Year
WW = Work Week
MJE13003 = Device Code

ORDERING INFORMATION

Device	Package	Shipping
MJE13003	TO−225	500 Units/Box

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2.)						
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	−	−	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	− −	− −	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	−	−	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with bass forward biased		$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 12			
ON CHARACTERISTICS (Note 2.)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc) (I_C = 1 Adc, V_{CE} = 2 Vdc)		h_{FE}	8 5	− −	40 25	−
Collector−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1.5 Adc, I_B = 0.5 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{CE(sat)}$	− − − −	− − − −	0.5 1 3 1	Vdc
Base−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{BE(sat)}$	− − −	− − −	1 1.2 1.1	Vdc
DYNAMIC CHARACTERISTICS						
Current−Gain − Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	10	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	−	21	−	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	−	0.05	0.1	μs
Rise Time		t_r	−	0.5	1	μs
Storage Time		t_s	−	2	4	μs
Fall Time		t_f	−	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	(I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	−	1.7	4	μs
Crossover Time		t_c	−	0.29	0.75	μs
Fall Time		t_{fi}	−	0.15	−	μs

2. Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

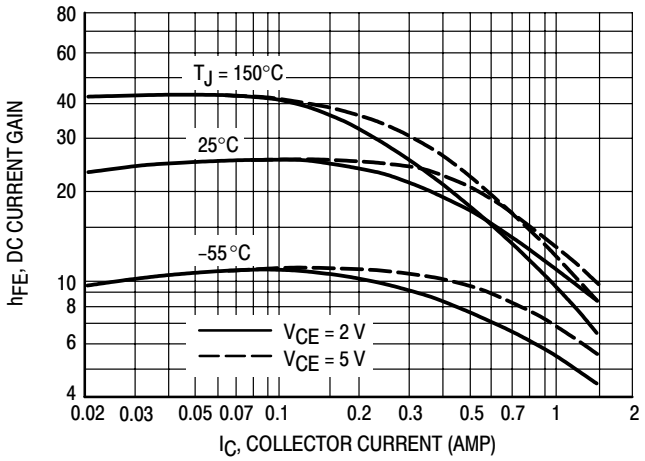


Figure 1. DC Current Gain

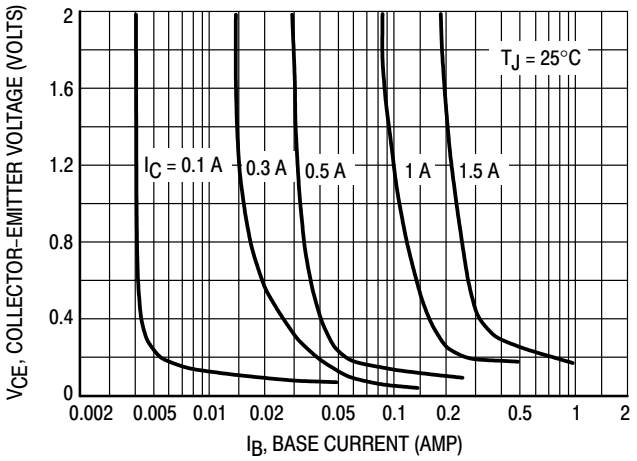


Figure 2. Collector Saturation Region

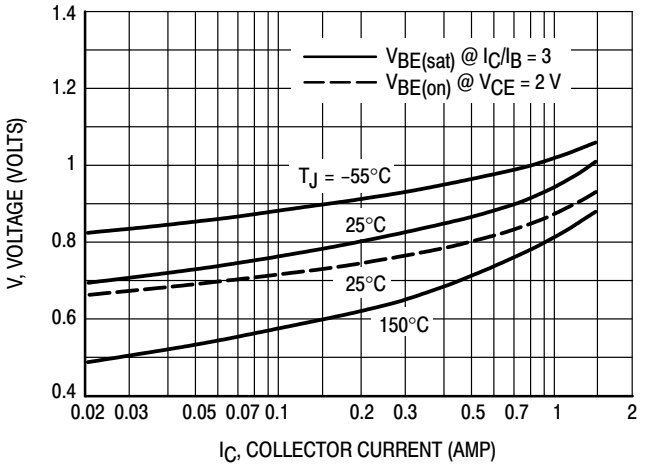


Figure 3. Base−Emitter Voltage

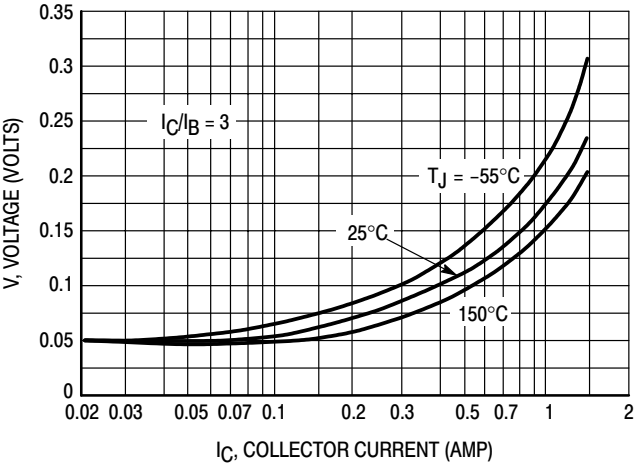


Figure 4. Collector−Emitter Saturation Region

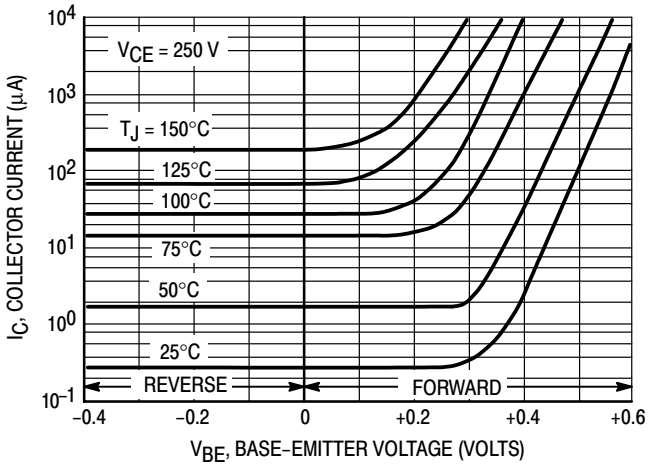


Figure 5. Collector Cutoff Region

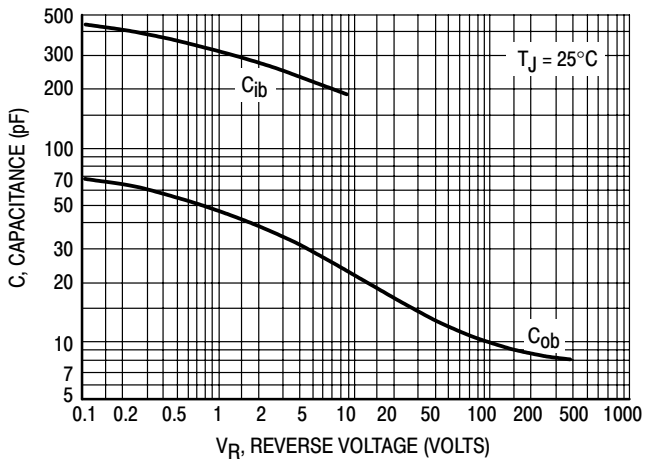
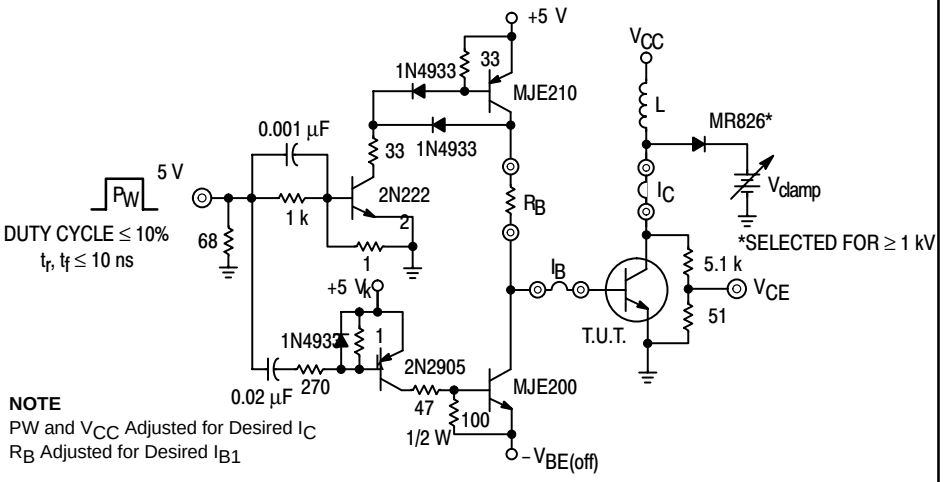


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

<table>
<tr><th colspan="2">REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>TEST CIRCUITS</td><td>


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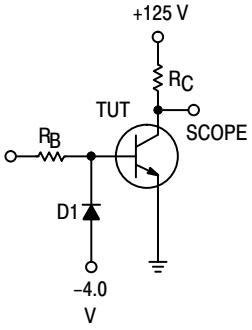
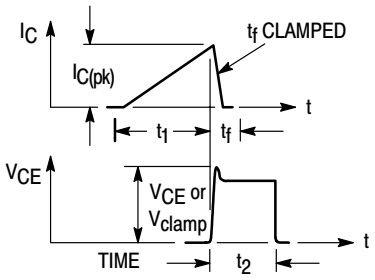
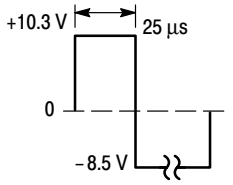


</td></tr>
<tr><td>CIRCUIT VALUES</td><td>Coil Data:
Ferroxcube Core #6656
Full Bobbin (~200 Turns) #20
GAP for 30 mH/2 A
Lcoil = 50 mH
VCC = 20 V
Vclamp = 300 Vdc</td><td>VCC = 125 V
RC = 125 Ω
D1 = 1N5820 or Equiv.
RB = 47 Ω</td></tr>
<tr><td>TEST WAVEFORMS</td><td>
OUTPUT WAVEFORMS


t1 Adjusted to Obtain IC
$t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$
Test Equipment
Scope–Tektronics
475 or Equivalent
</td><td>


tr, tf < 10 ns
Duty Cycle = 1.0%
RB and RC adjusted for desired IB and IC
</td></tr>
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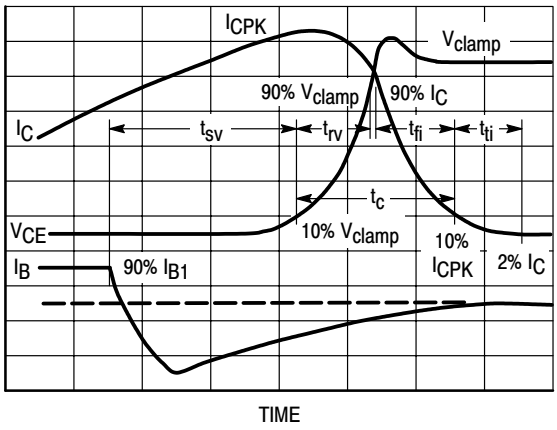


Figure 7. Inductive Switching Measurements

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25 100	1.3 1.6	0.23 0.26	0.30 0.30	0.35 0.40	0.30 0.36
1	25 100	1.5 1.7	0.10 0.13	0.14 0.26	0.05 0.06	0.16 0.29
1.5	25 100	1.8 3	0.07 0.08	0.10 0.22	0.05 0.08	0.16 0.28

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10−90% V_{clamp}

t_{fi} = Current Fall Time, 90−10% I_C

t_{ti} = Current Tail, 10−2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN−222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

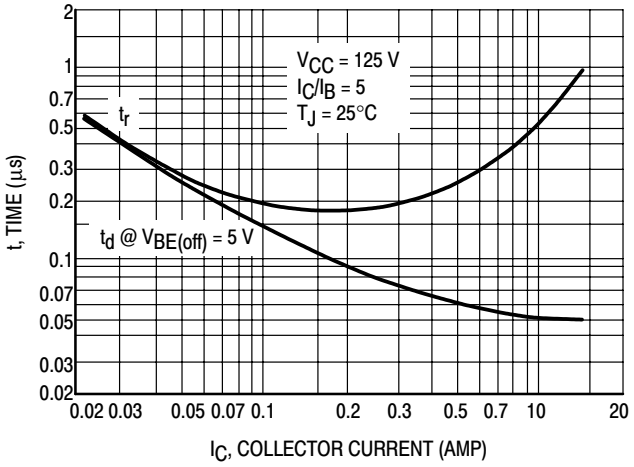


Figure 8. Turn−On Time

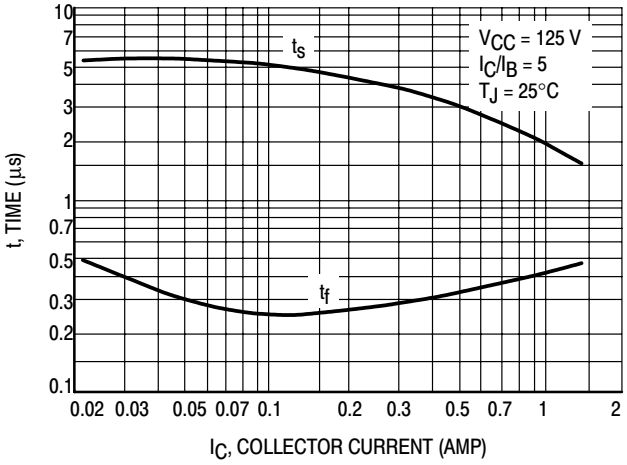


Figure 9. Turn−Off Time

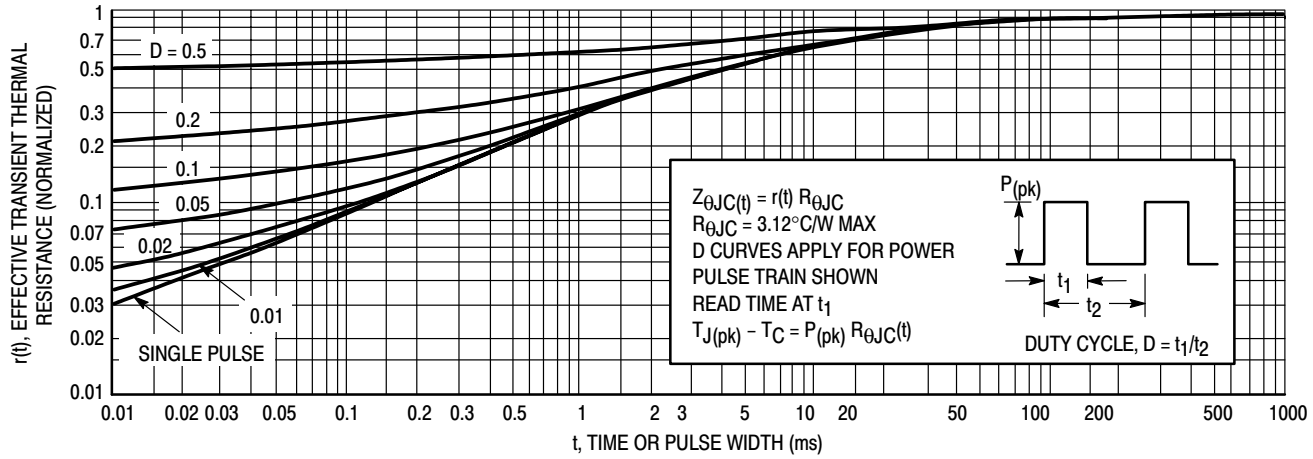


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

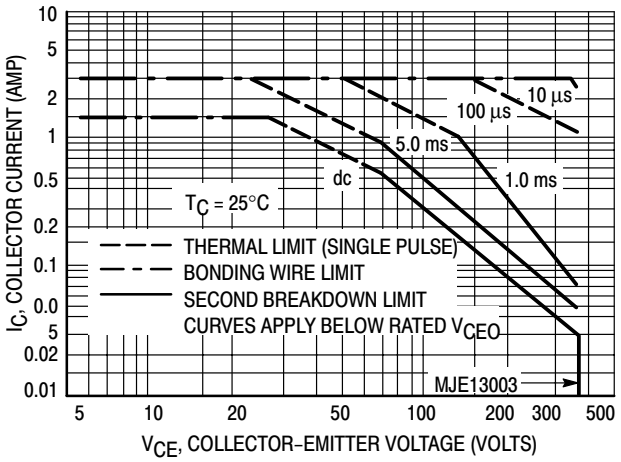


Figure 11. Active Region Safe Operating Area

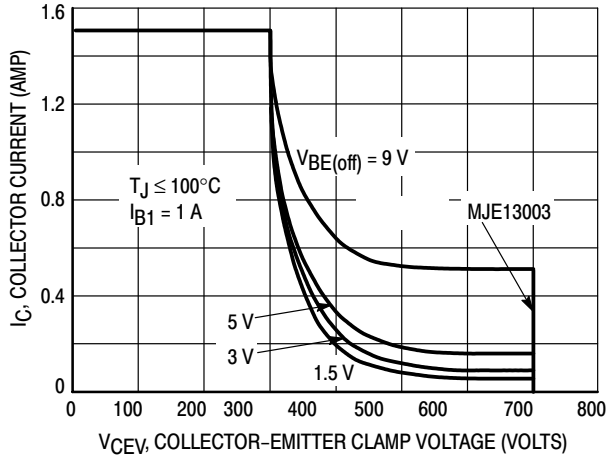


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

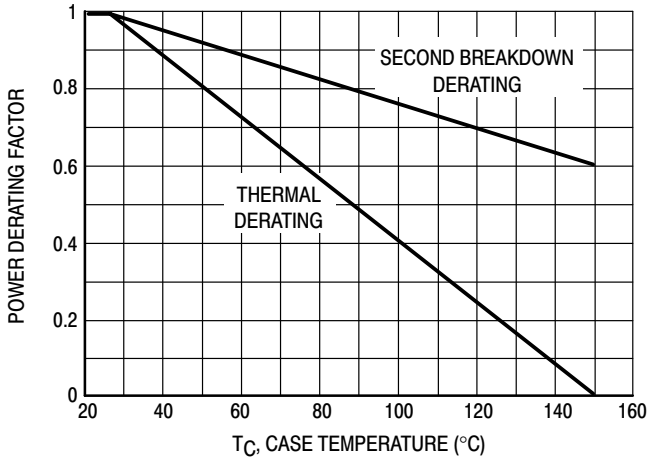


Figure 13. Forward Bias Power Derating

MJE13005*

*ON Semiconductor Preferred Device

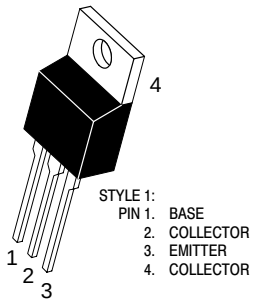
SWITCHMODE™ Series NPN Silicon Power Transistors

These devices are designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

4 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
75 WATTS

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
  t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	6 12	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 600	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 11		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 12		
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)		h_{FE}	 10 8	 — —	 60 40	—
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 4 Adc, I_B = 1 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — — —	 — — — —	 0.5 0.6 1 1	Vdc
Base−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc) (I_C = 2 Adc, I_B = 0.5 Adc) (I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — — —	 — — —	 1.2 1.6 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Current−Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	65	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 2)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 2 A, I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.3	0.7	μs
Storage Time		t_s	—	1.7	4	μs
Fall Time		t_f	—	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	(I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.9	4	μs
Crossover Time		t_c	—	0.32	0.9	μs
Fall Time		t_{fi}	—	0.16	—	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

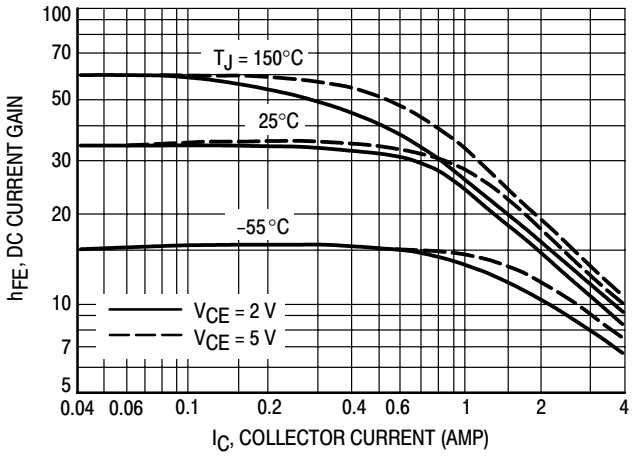


Figure 1. DC Current Gain

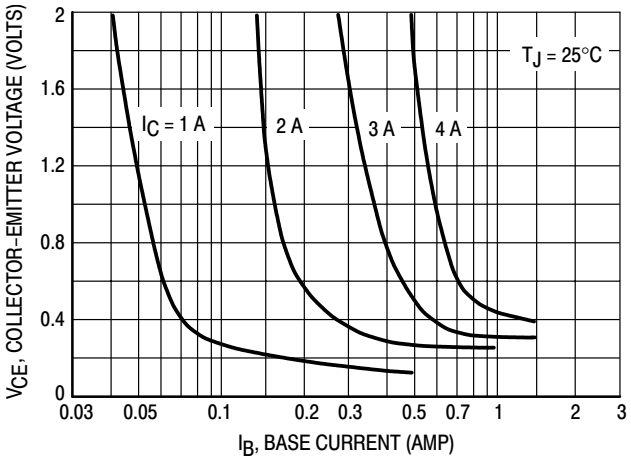


Figure 2. Collector Saturation Region

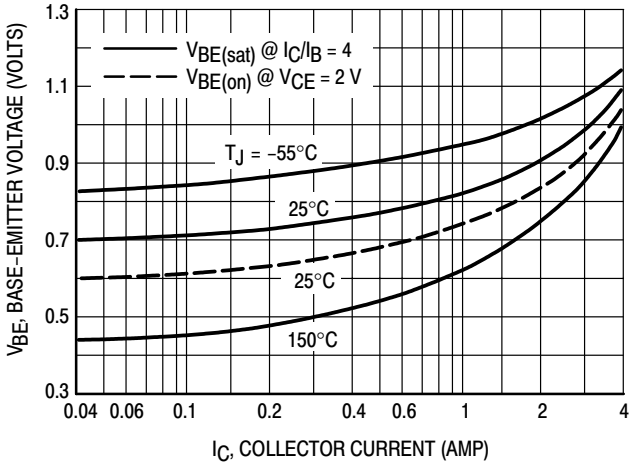


Figure 3. Base−Emitter Voltage

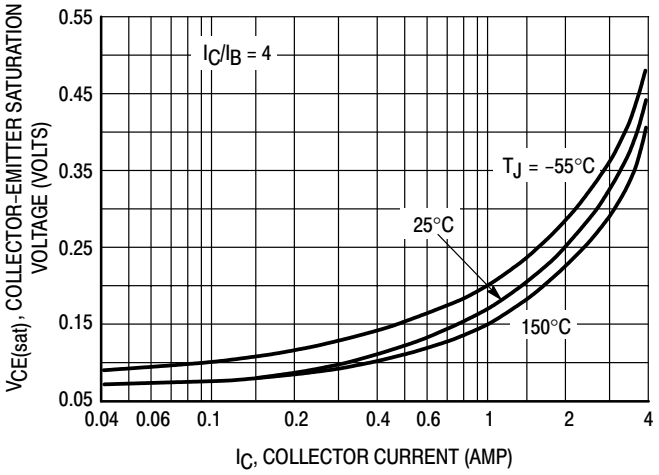


Figure 4. Collector−Emitter Saturation Voltage

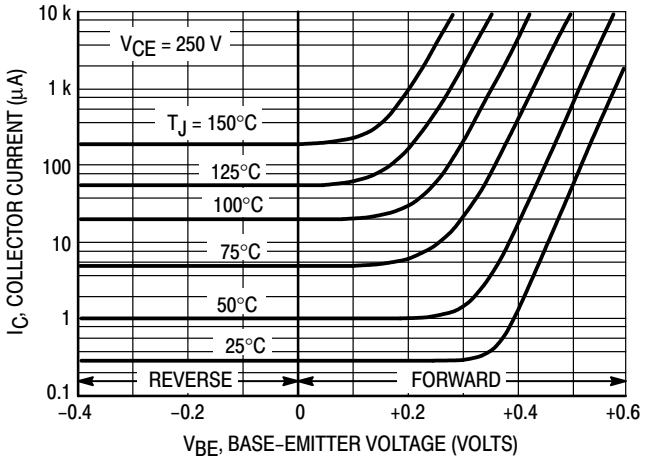


Figure 5. Collector Cutoff Region

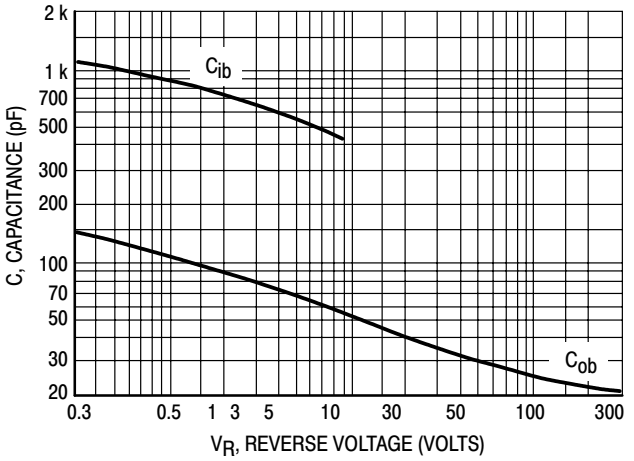


Figure 6. Capacitance

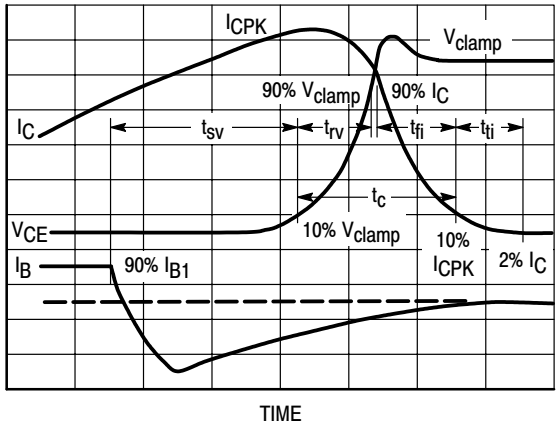


Figure 7. Inductive Switching Measurements

Table 1. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25 100	600 900	70 110	100 240	80 130	180 320
3	25 100	650 950	60 100	140 330	60 100	200 350
4	25 100	550 850	70 110	160 350	100 160	220 390

NOTE: All Data recorded in the inductive Switching Circuit In Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10−90% V_{clamp}

t_{fi} = Current Fall Time, 90−10% I_C

t_{ti} = Current Tail, 10−2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN−222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

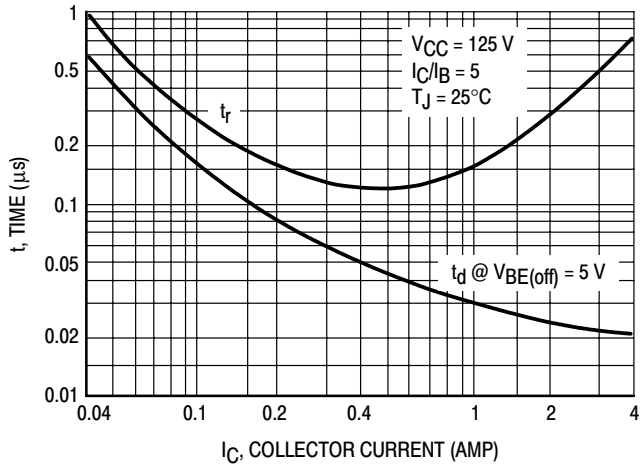


Figure 8. Turn−On Time

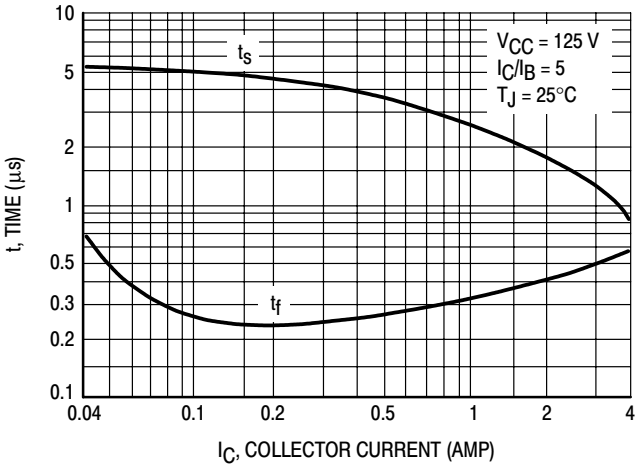
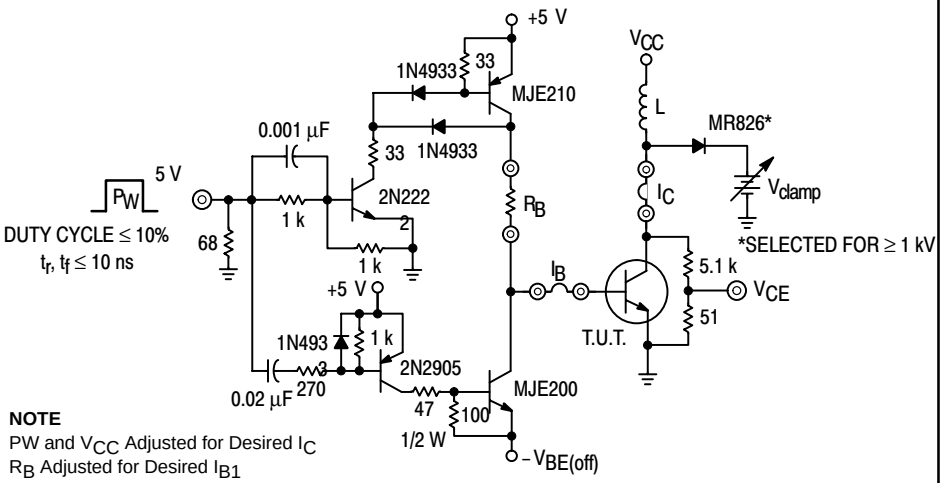
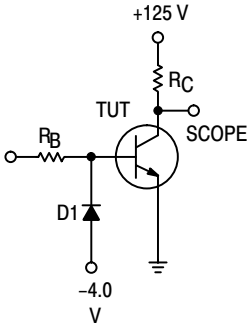
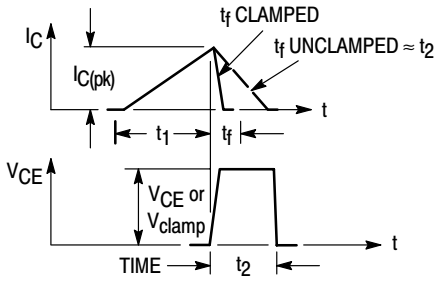
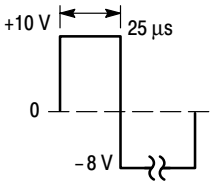


Figure 9. Turn−Off Time

Table 2. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20 A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 62 Ω D1 = 1N5820 or Equiv. R_B = 22 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope−Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

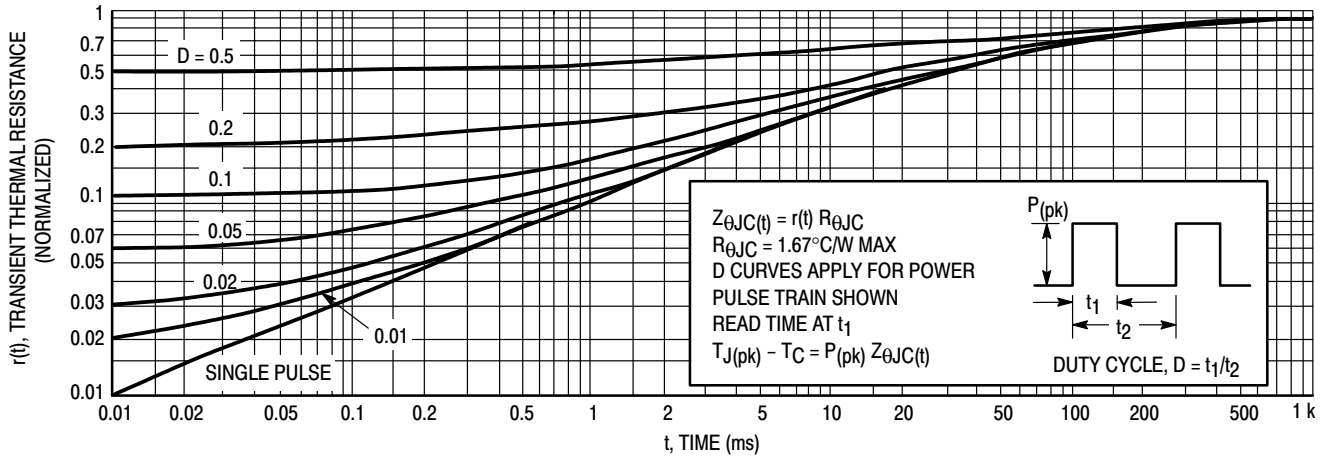


Figure 10. Typical Thermal Response [$Z_{\theta JC}(t)$]

SAFE OPERATING AREA INFORMATION

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

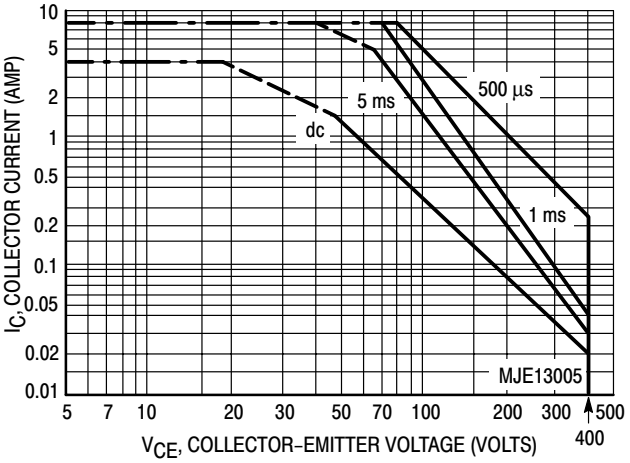


Figure 11. Forward Bias Safe Operating Area

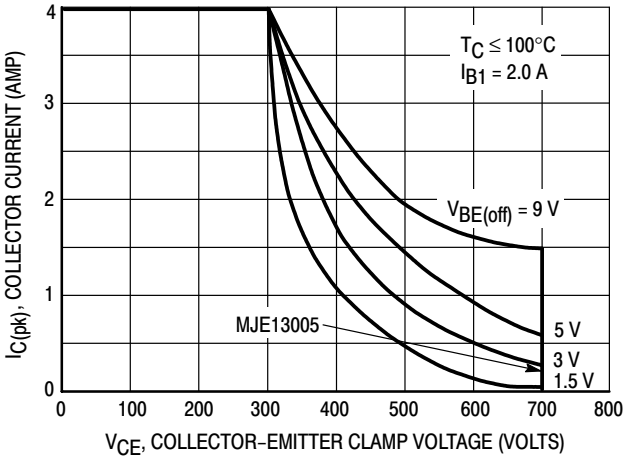


Figure 12. Reverse Bias Switching Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

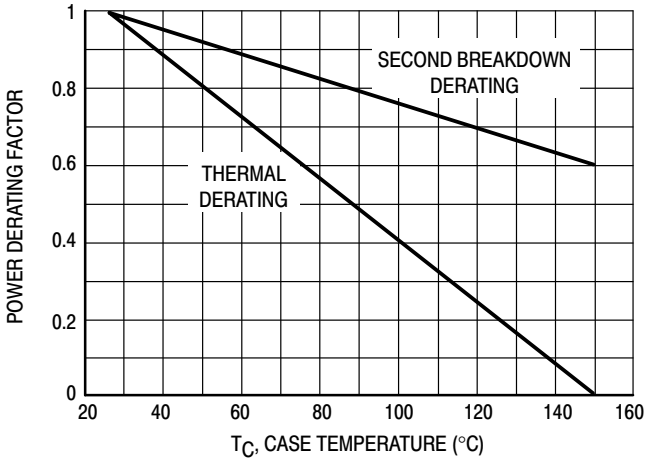


Figure 13. Forward Bias Power Derating

SWITCHMODE™

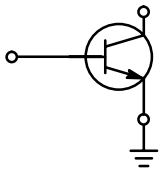
NPN Bipolar Power Transistor For Switching Power Supply Applications

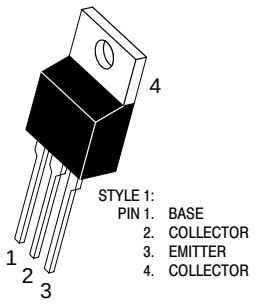
MJE13007

POWER TRANSISTOR
8.0 AMPERES
400 VOLTS
80 WATTS

The MJE13007 is designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Standard TO−220





CASE 221A−09
TO−220AB
MJE13007

MAXIMUM RATINGS

Rating	Symbol	MJE13007	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	− 65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.56 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**							
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current			I_{CES}				mAdc
(V_{CES} = 700 Vdc)				—	—	0.1	
(V_{CES} = 700 Vdc, T_C = 125°C)				—	—	1.0	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)			I_{EBO}	—	—	100	μAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased			—	See Figure 7			
***ON CHARACTERISTICS**							
DC Current Gain			h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)				8.0	—	40	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)				5.0	—	30	
Collector−Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	2.0	
(I_C = 8.0 Adc, I_B = 2.0 Adc)				—	—	3.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	3.0	
Base−Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.2	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	1.5	
DYNAMIC CHARACTERISTICS							
Current−Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)			f_T	4.0	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 125 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 25 μs, Duty Cycle ≤ 1.0%)		t_d	—	0.025	0.1	μs
Rise Time			t_r	—	0.5	1.5	
Storage Time			t_s	—	1.8	3.0	
Fall Time			t_f	—	0.23	0.7	
Inductive Load, Clamped (Table 1)							
Voltage Storage Time	V_{CC} = 15 Vdc, I_C = 5.0 A, V_{clamp} = 300 Vdc	T_C = 25°C	t_{sv}	—	1.2	2.0	μs
		T_C = 100°C		—	1.6	3.0	
Crossover Time	$I_{B(on)}$ = 1.0 A, $I_{B(off)}$ = 2.5 A, L_C = 200 μH	T_C = 25°C	t_c	—	0.15	0.30	μs
		T_C = 100°C		—	0.21	0.50	
Fall Time		T_C = 25°C	t_{fi}	—	0.04	0.12	μs
		T_C = 100°C		—	0.10	0.20	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

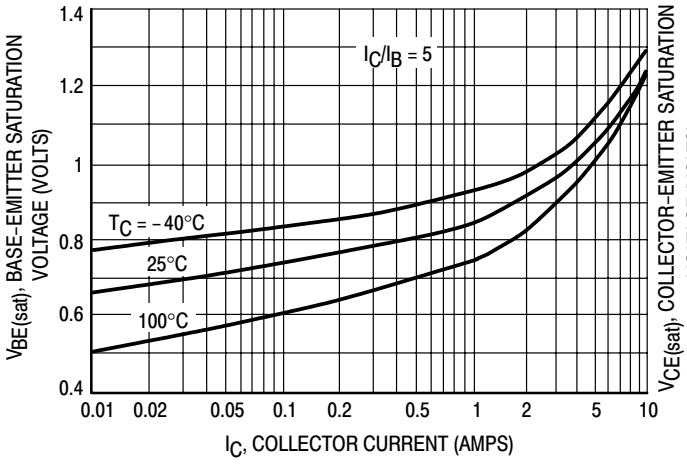


Figure 1. Base−Emitter Saturation Voltage

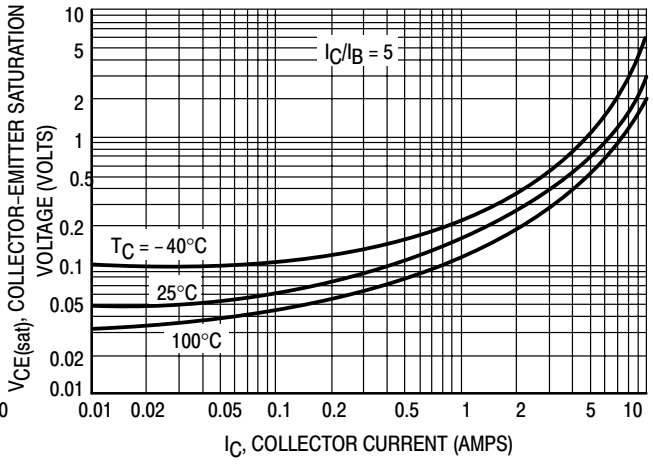


Figure 2. Collector−Emitter Saturation Voltage

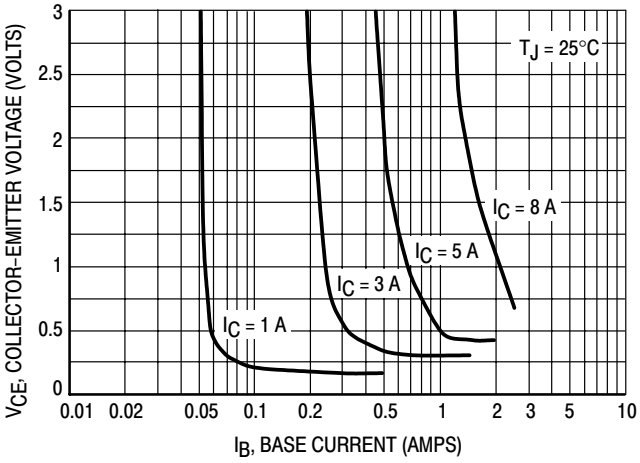


Figure 3. Collector Saturation Region

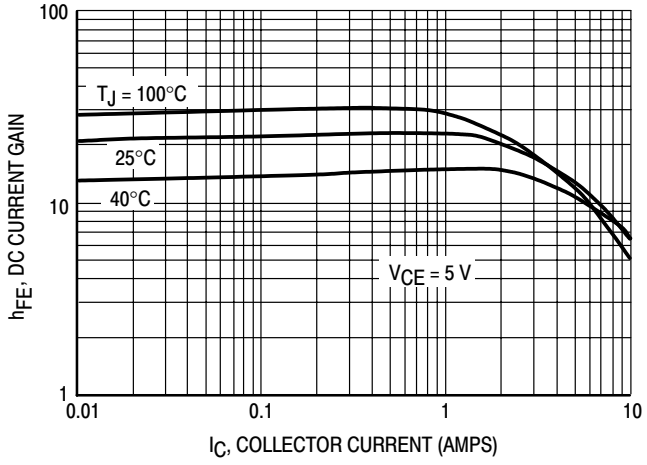


Figure 4. DC Current Gain

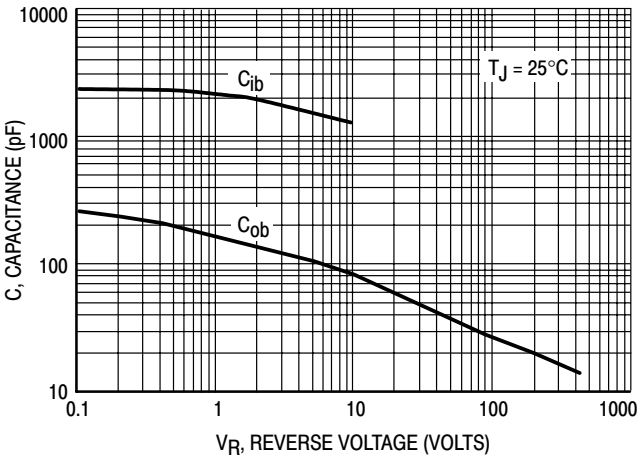


Figure 5. Capacitance

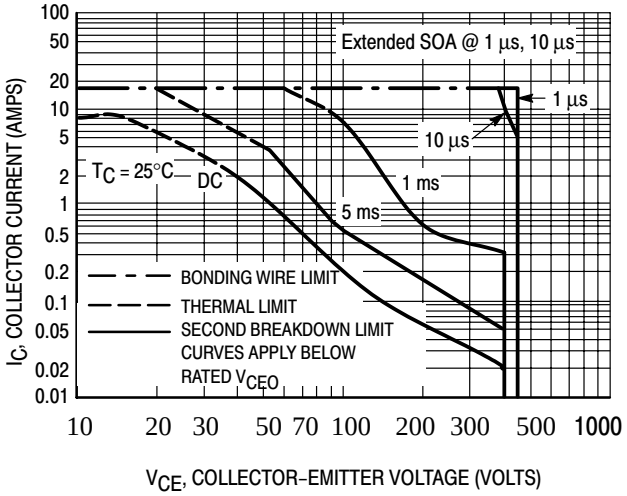


Figure 6. Maximum Forward Bias Safe Operating Area

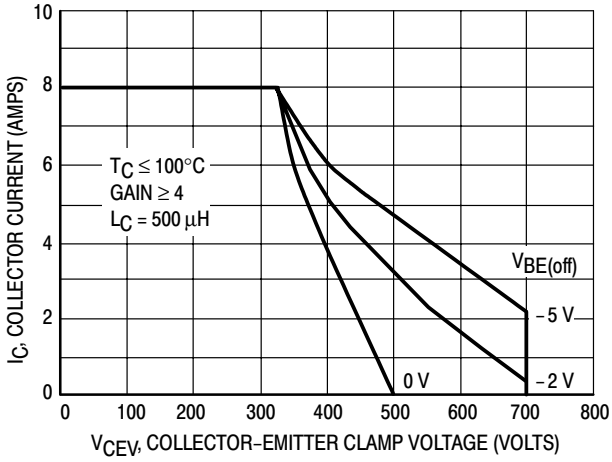


Figure 7. Maximum Reverse Bias Switching Safe Operating Area

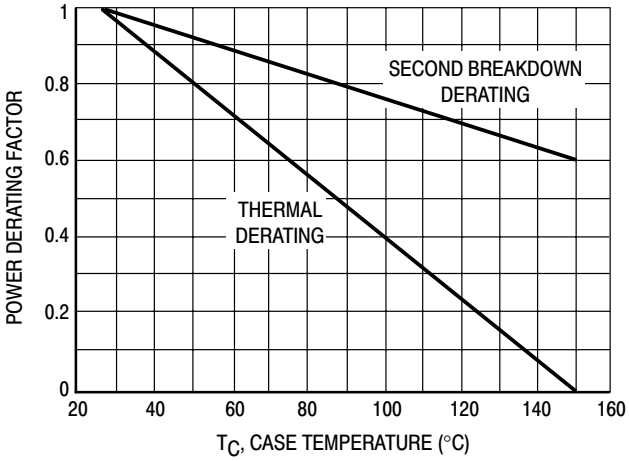


Figure 8. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 8.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 7) is discussed in the applications information section.

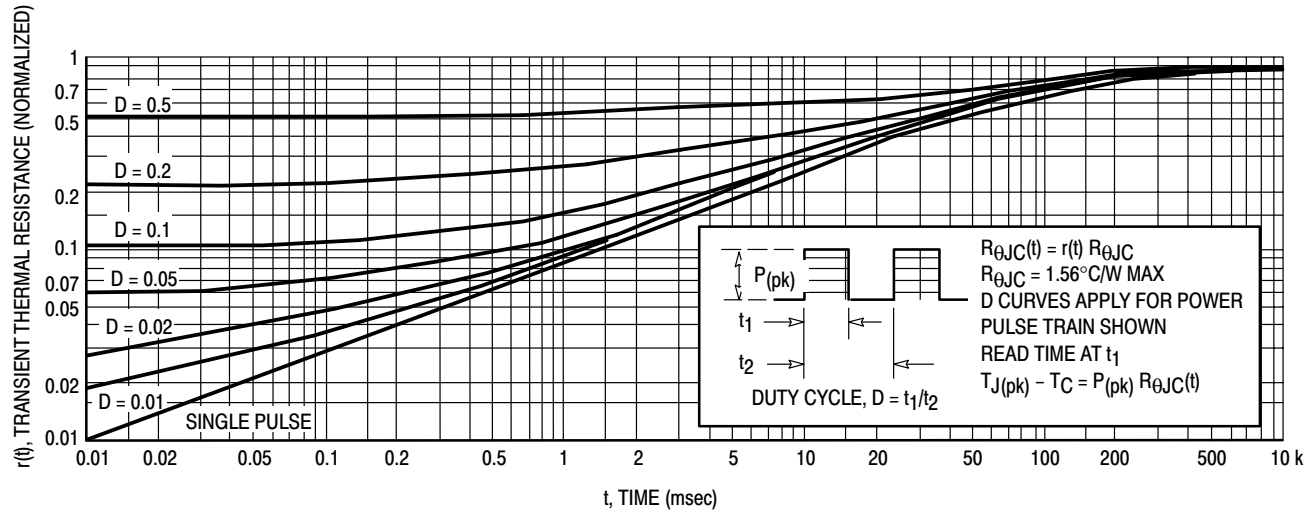


Figure 9. Typical Thermal Response for MJE13007

SPECIFICATION INFORMATION FOR SWITCHMODE APPLICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

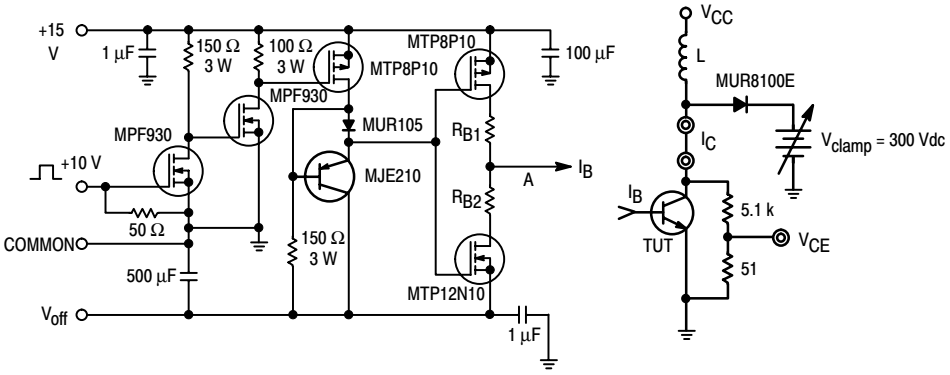
Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

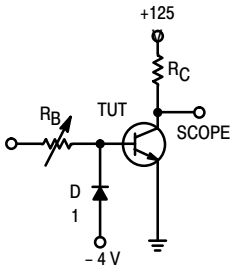
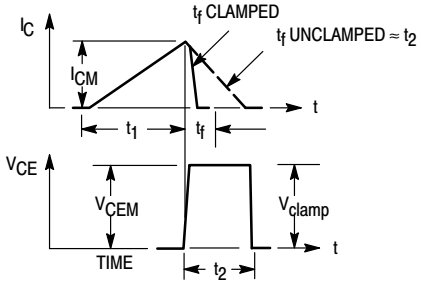
The sustaining or active region voltage requirements in switching applications occur during turn−on and turn−off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn−on and the pulsed forward bias SOA curves (Figure 6) are the proper design limits.

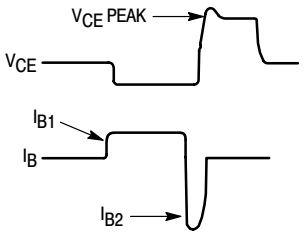
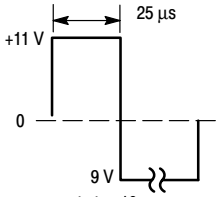
For inductive loads, high voltage and current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 7) which represents voltage−current conditions that can be sustained during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

(1) For detailed information on specific switching applications, see ON Semiconductor Application Note AN719, AN873, AN875, AN951.

Table 1. Test Conditions For Dynamic Performance

<table>
<tr><td>TEST CIRCUITS</td><td>REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING</td><td>RESISTIVE SWITCHING</td></tr>
<tr><td></td><td> 


</td></tr>
<tr><td>CIRCUIT VALUES</td><td><table>
<tr><th>V(BR)CEO(sus)</th><th>Inductive Switching</th><th>RBSOA</th></tr>
<tr><td>L = 10 mH
RB2 = 8
VCC = 20 Volts
IC(pk) = 100 mA</td><td>L = 200 mH
RB2 = 0
VCC = 15 Volts
RB1 selected for desired IB1</td><td>L = 500 mH
RB2 = 0
VCC = 15 Volts
RB1 selected for desired IB1</td></tr>
</table></td><td>VCC = 125 V
RC = 25 Ω
D1 = 1N5820 OR EQUIV.</td></tr>
<tr><td>TEST WAVEFORMS</td><td> 

t1 ADJUSTED TO OBTAIN IC
$t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$
$t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$
TEST EQUIPMENT
SCOPE — TEKTRONIX 475 OR EQUIVALENT</td><td>TYPICAL WAVE-FORMS
 
</td><td> 

tr, tf < 10 ns
DUTY CYCLE = 1.0%
RB AND RC ADJUSTED FOR DESIRED IB AND IC</td></tr>
</table>

VOLTAGE REQUIREMENTS (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn−off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn−on and within the reverse bias SOA curve during turn−off are considered safe, with the following assumptions:

3. The device thermal limitations are not exceeded.
4. The turn−on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 6).
5. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 7).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5.0 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base−emitter junction during turn−off. The reverse biased switching characteristics for inductive loads are shown in Figures 12 and 13 and resistive loads in Figures 10 and 11. Usually the inductive load components will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (see Table 1) providing correlation between test procedures and actual use conditions.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and any coil driver, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10−90% V_{clamp}
t_{fi} = Current Fall Time, 90−10% I_C
t_{ti} = Current Tail, 10−2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn−off waveforms is shown in Figure 12 to aid in the visual identity of these terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222A:

$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$

Typical inductive switching times are shown in Figure 13. In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

SWITCHING PERFORMANCE

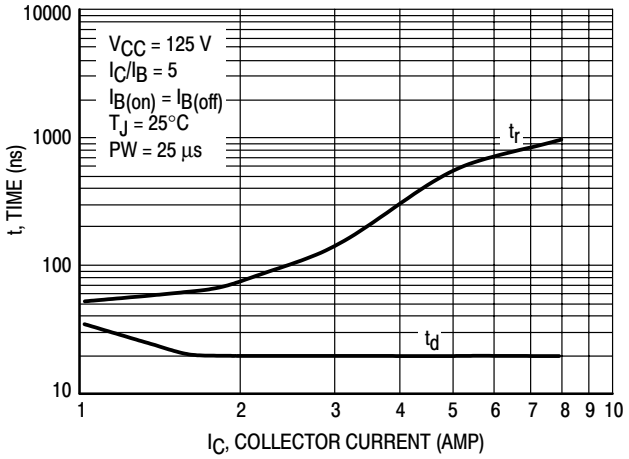


Figure 10. Turn−On Time (Resistive Load)

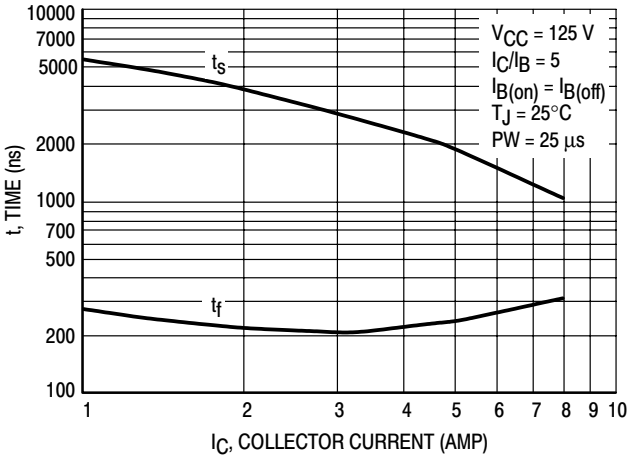


Figure 11. Turn−Off Time (Resistive Load)

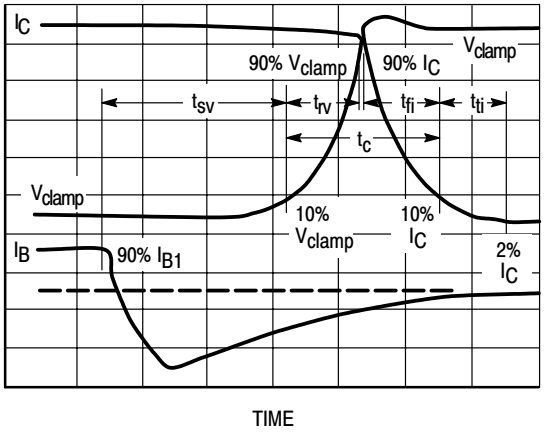


Figure 12. Inductive Switching Measurements

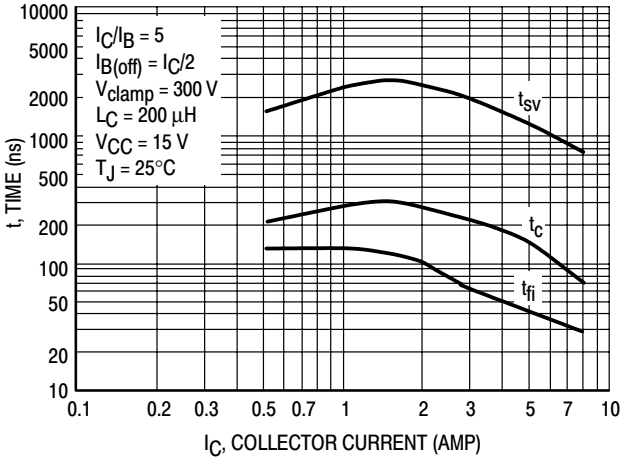
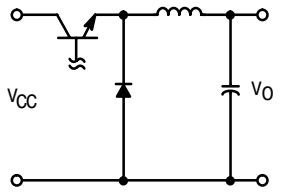
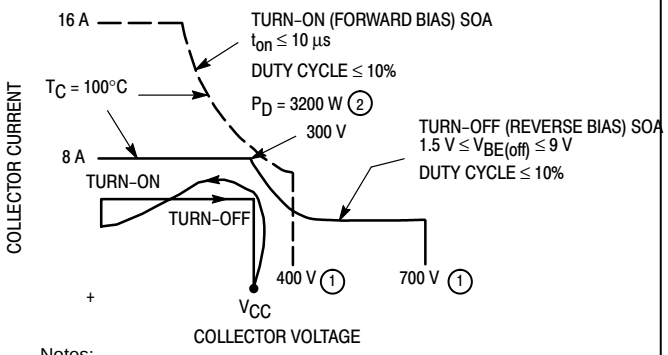
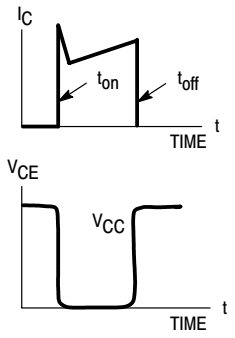
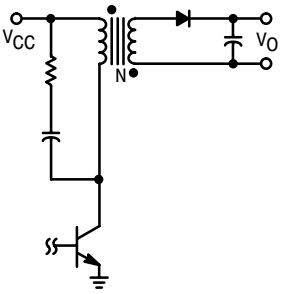
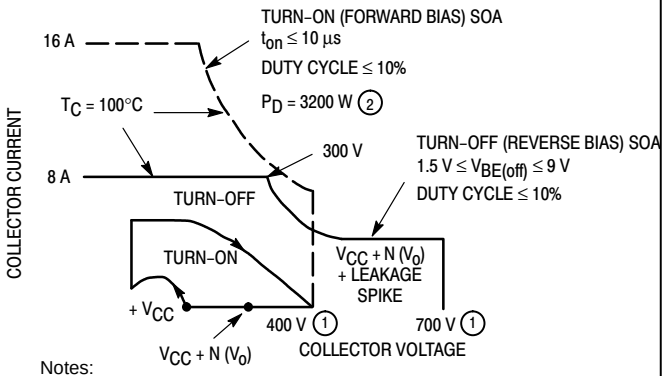
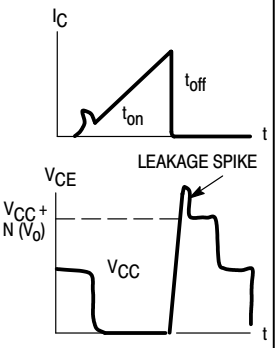
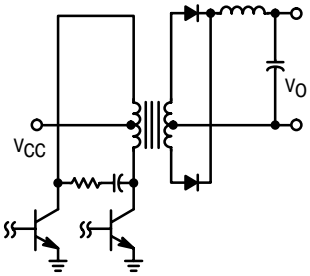
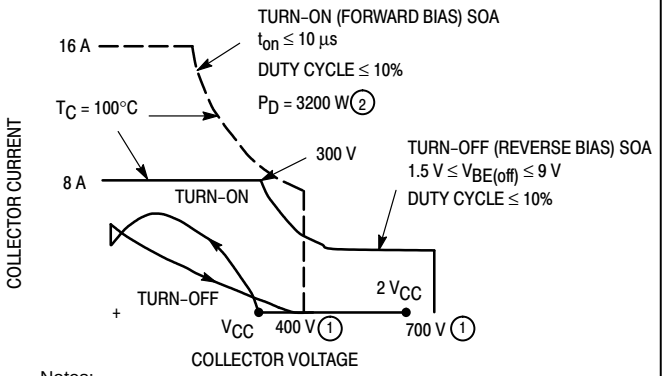
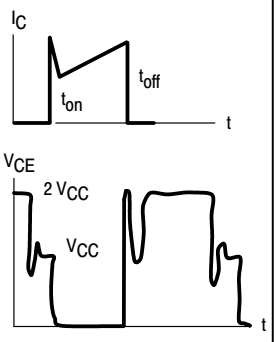
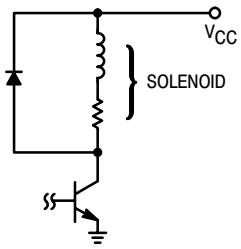
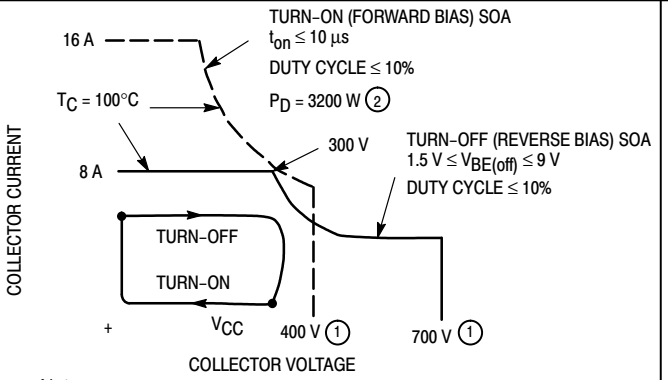
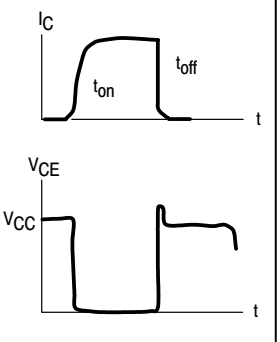


Figure 13. Typical Inductive Switching Times

Table 2. Applications Examples of Switching Circuits

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
B	**FLYBACK INVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
C	**PUSH−PULL INVERTER/CONVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	

MJE13009*

*ON Semiconductor Preferred Device

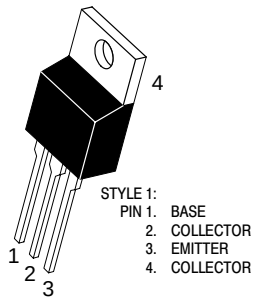
SWITCHMODE™ Series NPN Silicon Power Transistors

The MJE13009 is designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C
  t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

12 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
100 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 800	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased Clamped Inductive SOA with Base Reverse Biased	$I_{S/b}$ —	See Figure 1 See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc)	h_{FE}	8 6	— —	40 30	
Collector−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 8 Adc, I_B = 1.6 Adc) (I_C = 12 Adc, I_B = 3 Adc) (I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — — —	— — — —	1 1.5 3 2	Vdc
Base−Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 8 Adc, I_B = 1.6 Adc) (I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	$V_{BE(sat)}$	— — —	— — —	1.2 1.6 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	180	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 125 Vdc, I_C = 8 A, I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	—	0.06	0.1	μs
Rise Time		t_r	—	0.45	1	μs
Storage Time		t_s	—	1.3	3	μs
Fall Time		t_f	—	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 8 A, V_{clamp} = 300 Vdc, I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.92	2.3	μs
Crossover Time		t_c	—	0.12	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

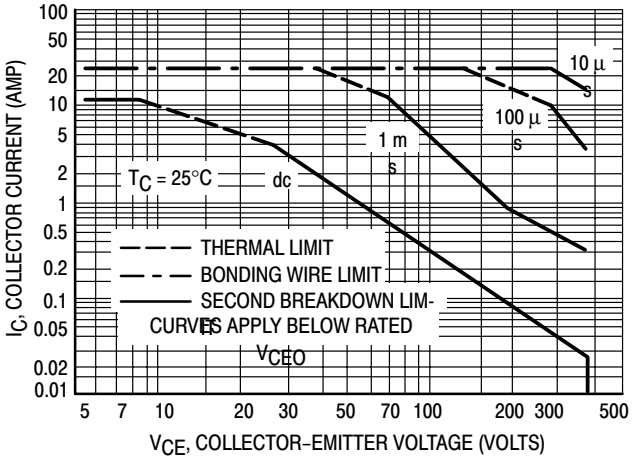


Figure 1. Forward Bias Safe Operating Area

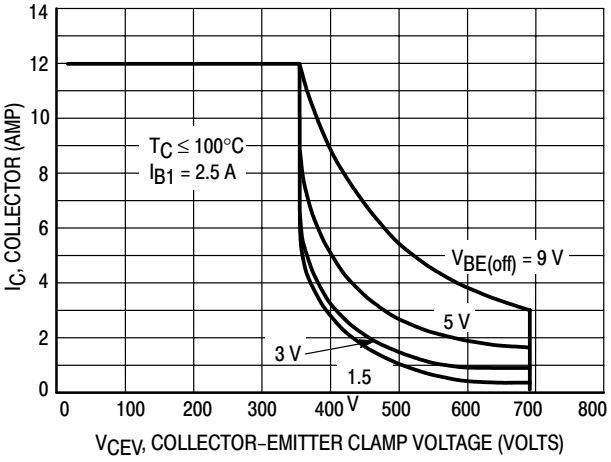


Figure 2. Reverse Bias Switching Safe Operating Area

The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

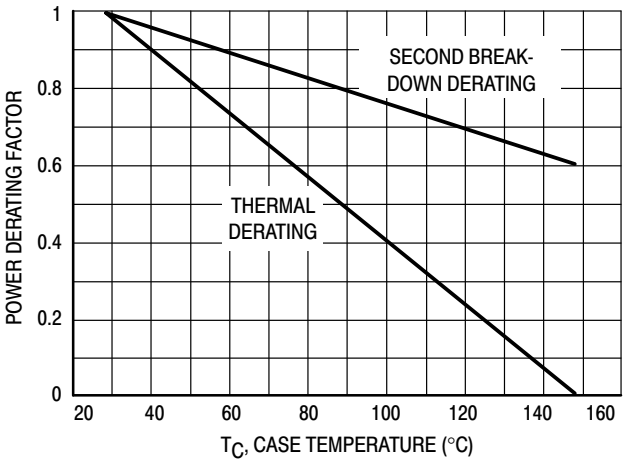


Figure 3. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

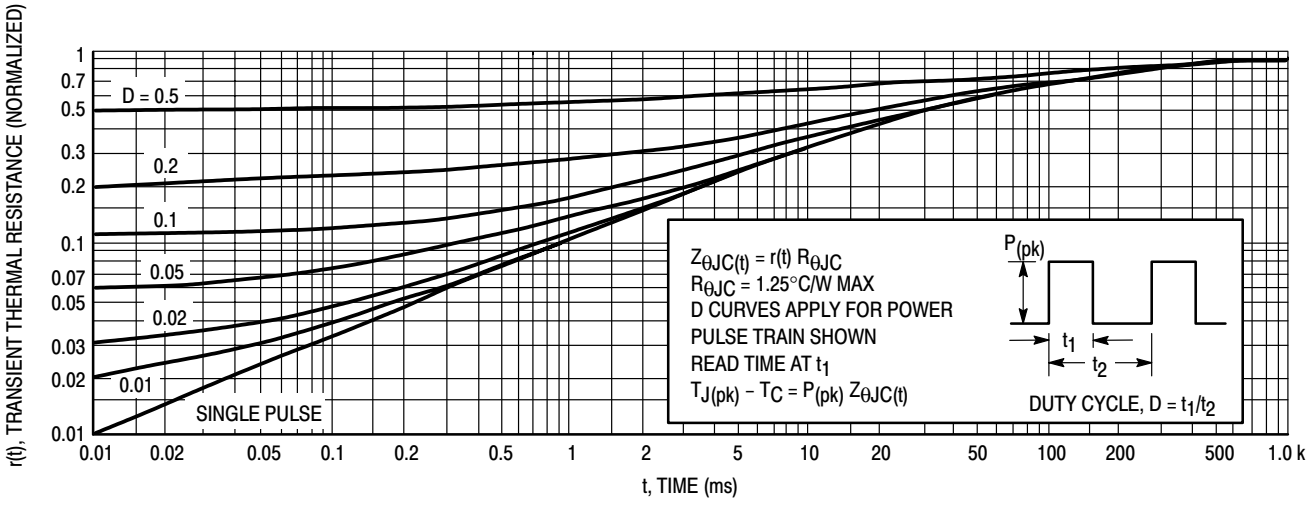


Figure 4. Typical Thermal Response [$Z_{\theta JC}(t)$]

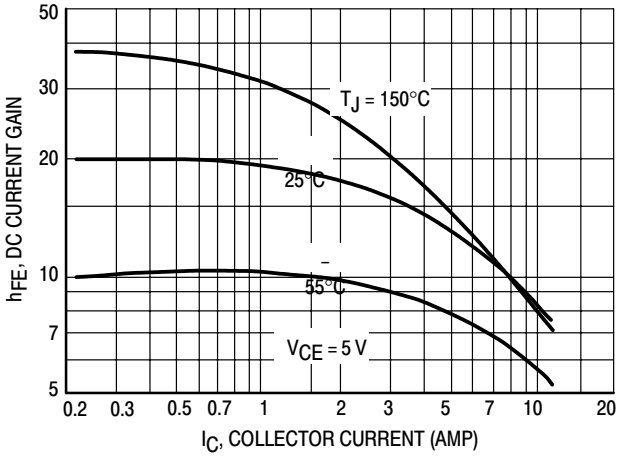


Figure 5. DC Current Gain

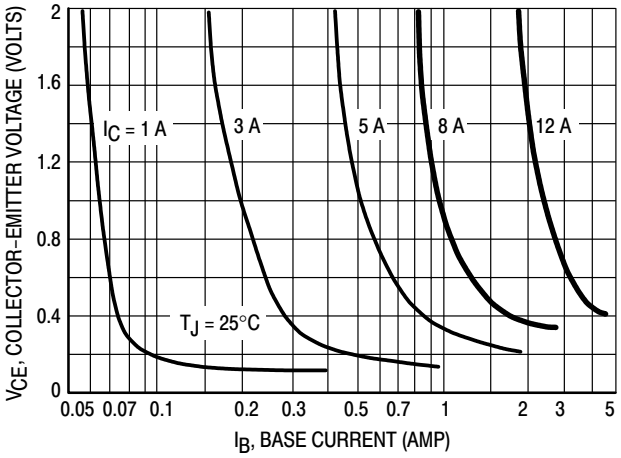


Figure 6. Collector Saturation Region

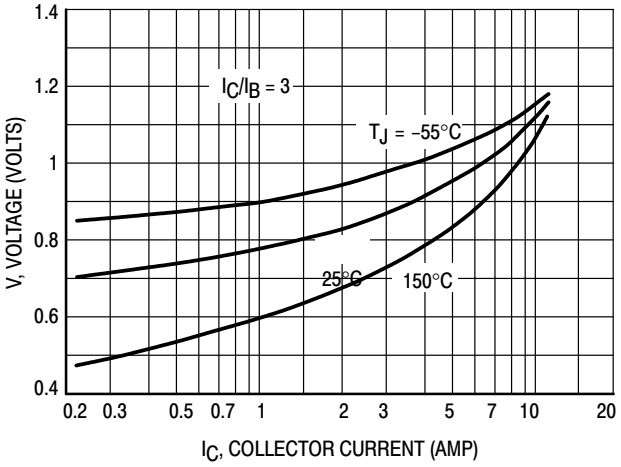


Figure 7. Base−Emitter Saturation Voltage

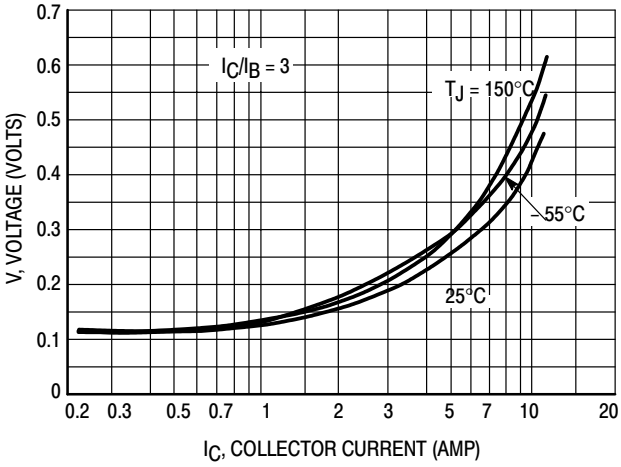


Figure 8. Collector−Emitter Saturation Voltage

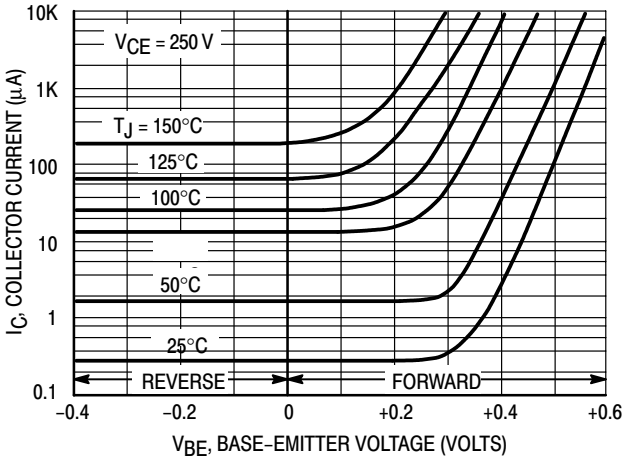


Figure 9. Collector Cutoff Region

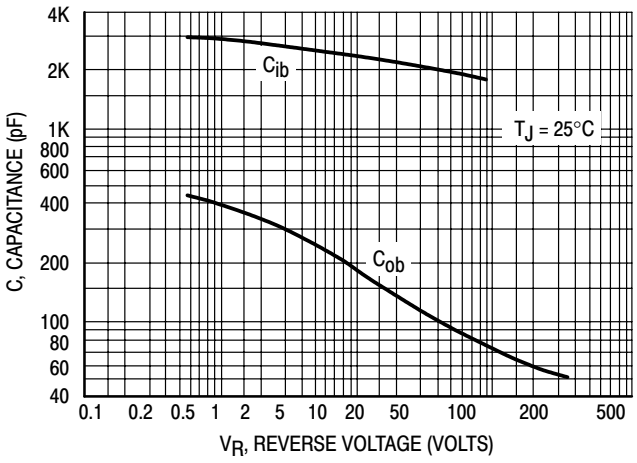
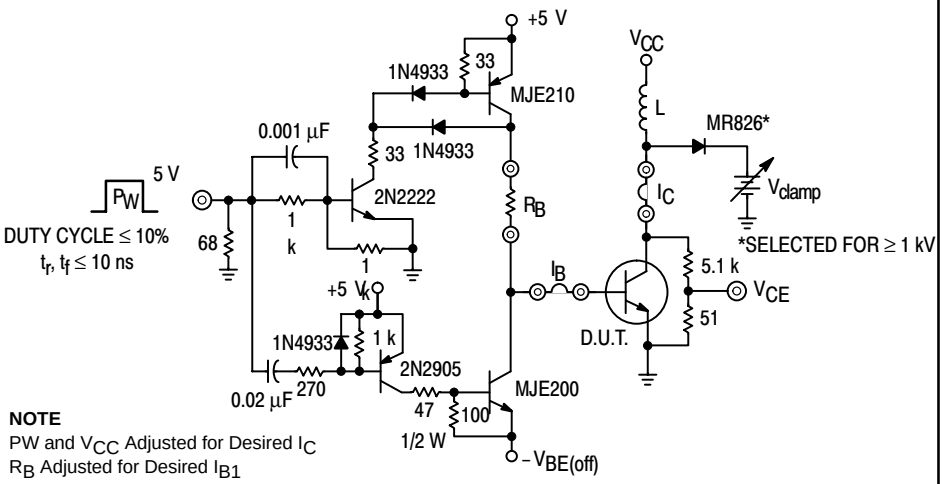
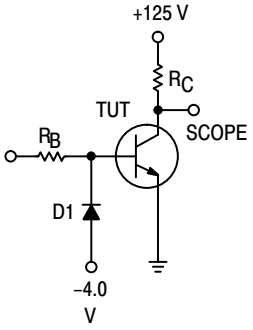
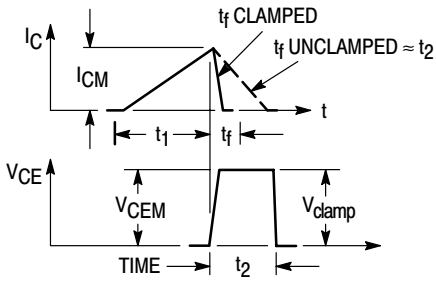
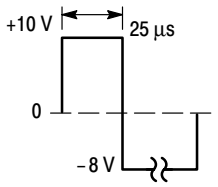


Figure 10. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20 A L_{coil} = 200 µH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15 Ω D1 = 1N5820 or Equiv. R_B = Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope−Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn−on and turn−off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn−on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage−current conditions that can be sustained during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn−off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn−on and within the reverse bias SOA curve during turn−off are considered safe, with the following assumptions:

6. The device thermal limitations are not exceeded.
7. The turn−on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
8. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base−emitter junction during turn−off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

(1) For detailed information on specific switching applications, see ON Semiconductor Application Notes AN−719, AN−767.

RESISTIVE SWITCHING PERFORMANCE

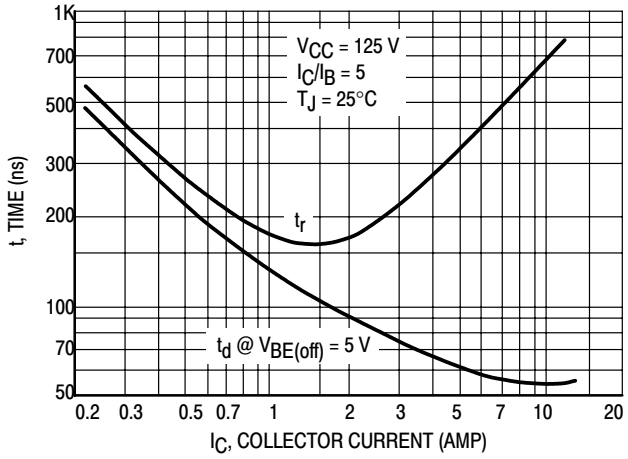


Figure 11. Turn−On Time

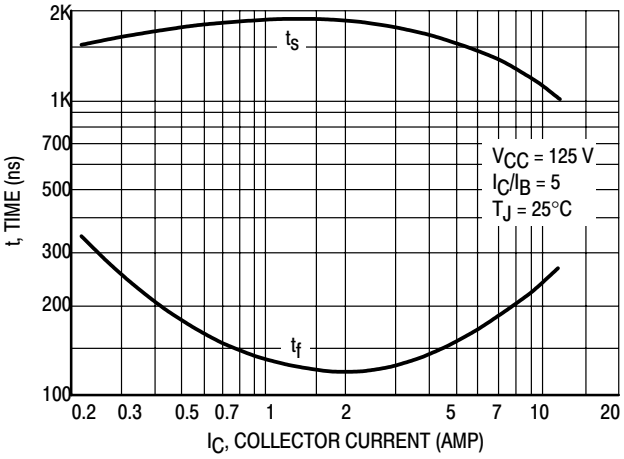


Figure 12. Turn−Off Time

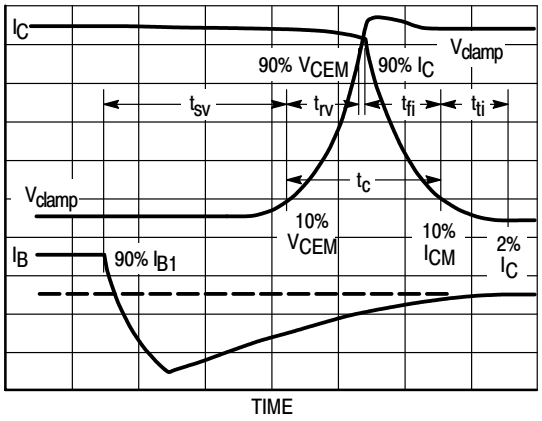


Figure 13. Inductive Switching Measurements

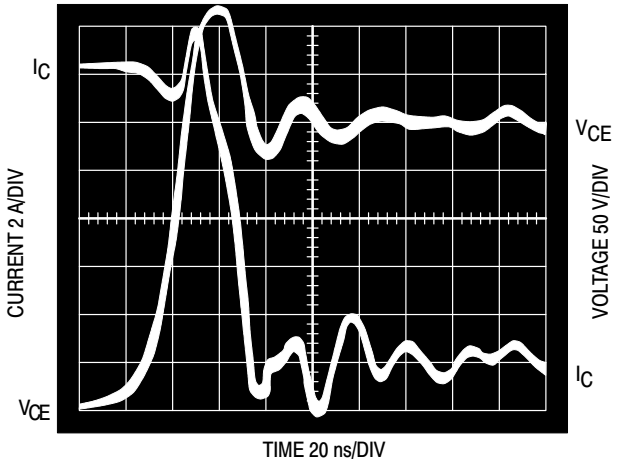


Figure 14. Typical Inductive Switching Waveforms (at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

Table 2. Applications Examples of Switching Circuits

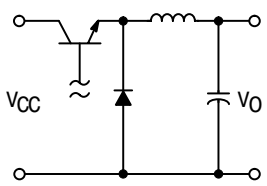
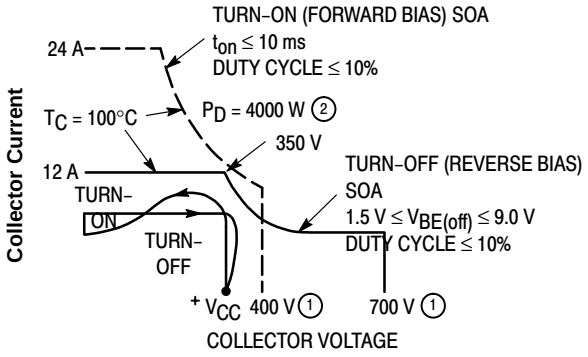
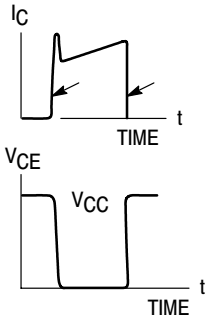
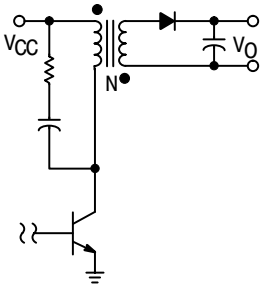
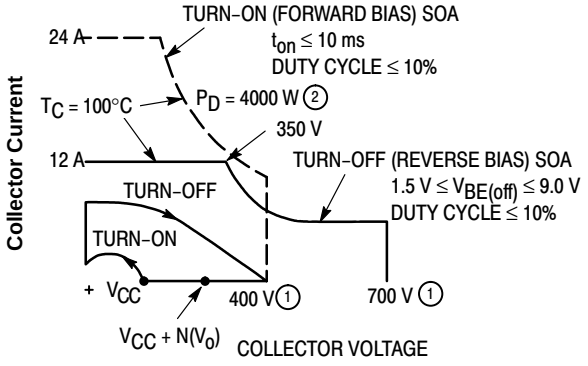
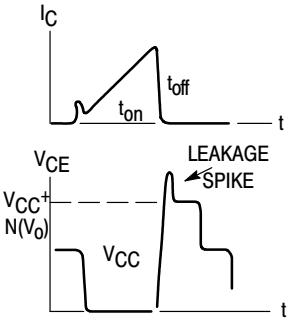
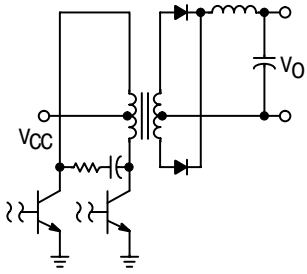
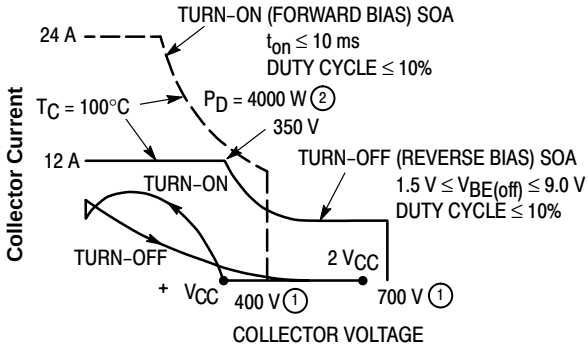
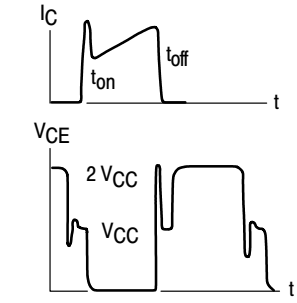
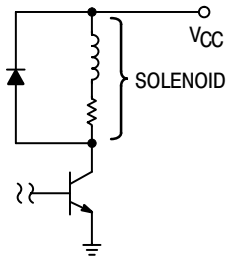
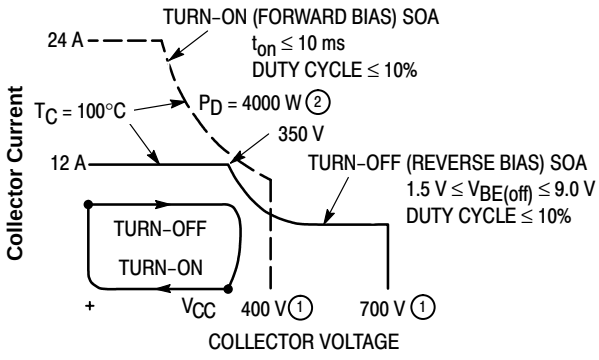
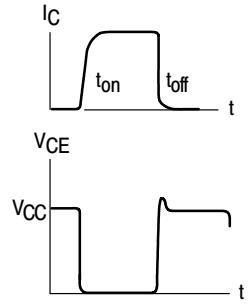
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH–PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

Table 3. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25 100	770 1000	100 230	150 160	200 200	240 320
5	25 100	630 820	72 100	26 55	10 30	100 180
8	25 100	720 920	55 70	27 50	2 8	77 120
12	25 100	640 800	20 32	17 24	2 4	41 54

NOTE: All Data recorded In the Inductive Switching Circuit In Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10−90% V_{CEM}

t_{fi} = Current Fall Time, 90−10% I_{CM}

t_{ti} = Current Tail, 10−2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn−off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN−222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

Complementary Silicon Plastic Power Transistors

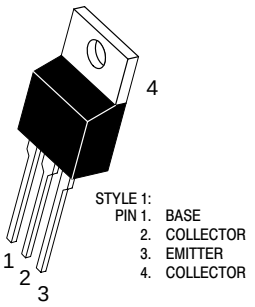
. . . designed for use as high−frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40 (Min) @ I_C = 3.0 Adc
  = 20 (Min) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — MJE15028, MJE15029
  = 150 Vdc (Min) — MJE15030, MJE15031
- High Current Gain — Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO−220AB Compact Package

NPN
MJE15028*
MJE15030*
PNP
MJE15029*
MJE15031*

***ON Semiconductor Preferred Device**

8 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
120−150 VOLTS
50 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector−Emitter Voltage	V_{CEO}	120	150	Vdc
Collector−Base Voltage	V_{CB}	120	150	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak	I_C	8.0 16		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

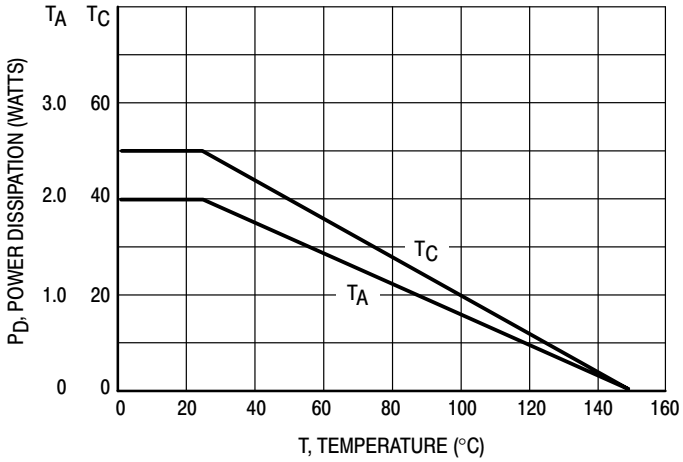


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029		120	—	
	MJE15030, MJE15031		150	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 120 Vdc, I_B = 0)	MJE15028, MJE15029		—	0.1	
(V_{CE} = 150 Vdc, I_B = 0)	MJE15030, MJE15031		—	0.1	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 120 Vdc, I_E = 0)	MJE15028, MJE15029		—	10	
(V_{CB} = 150 Vdc, I_E = 0)	MJE15030, MJE15031		—	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)			40	—	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)			40	—	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			40	—	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	—	
DC Current Gain Linearity (V_{CE} From 2.0 V to 20 V, I_C From 0.1 A to 3 A) (NPN TO PNP)		h_{FE}	**Typ** 2 3		
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.5	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

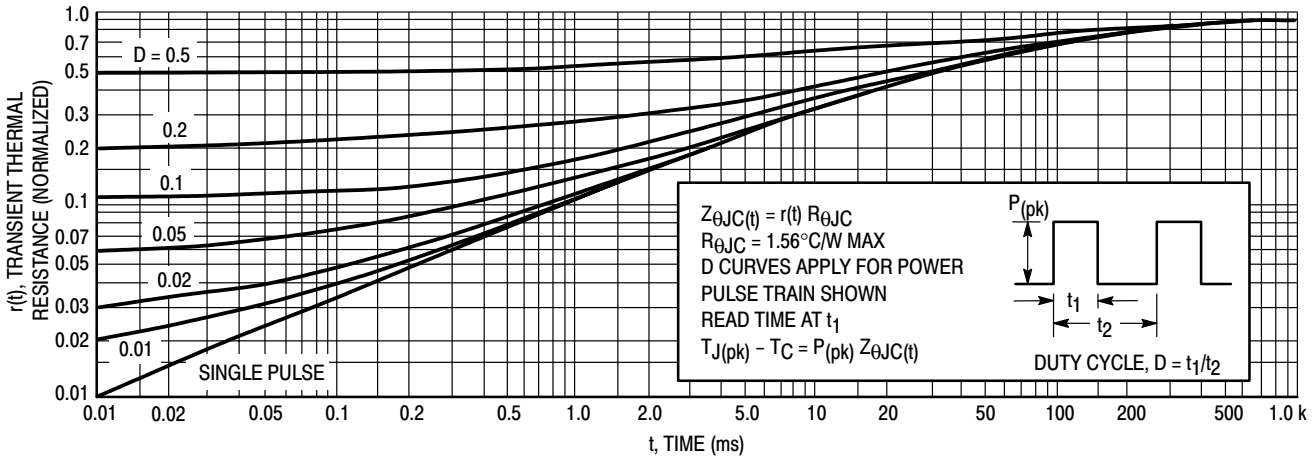


Figure 2. Thermal Response

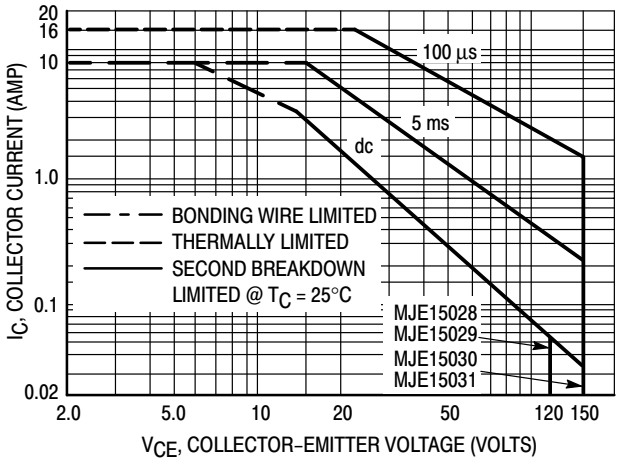


Figure 3. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

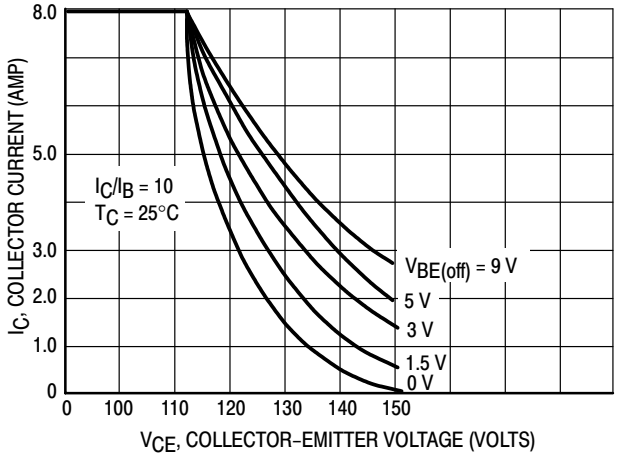


Figure 4. Reverse−Bias Switching Safe Operating Area

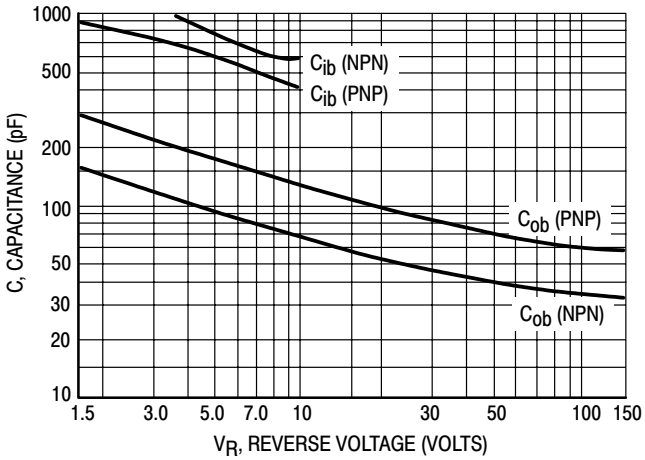


Figure 5. Capacitances

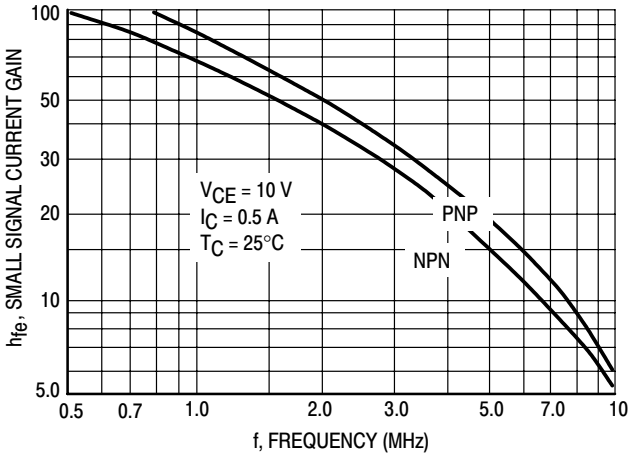


Figure 6. Small−Signal Current Gain

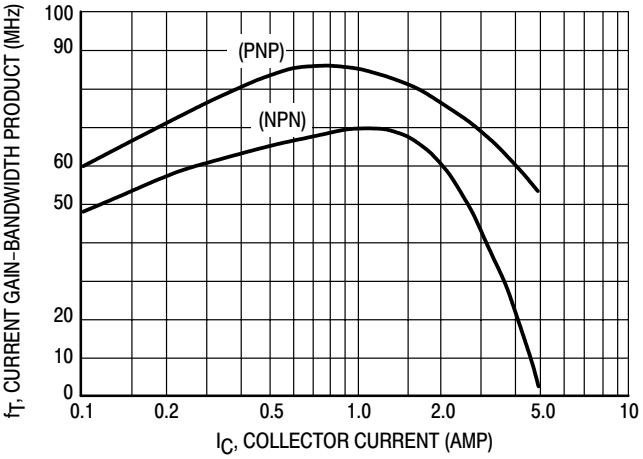
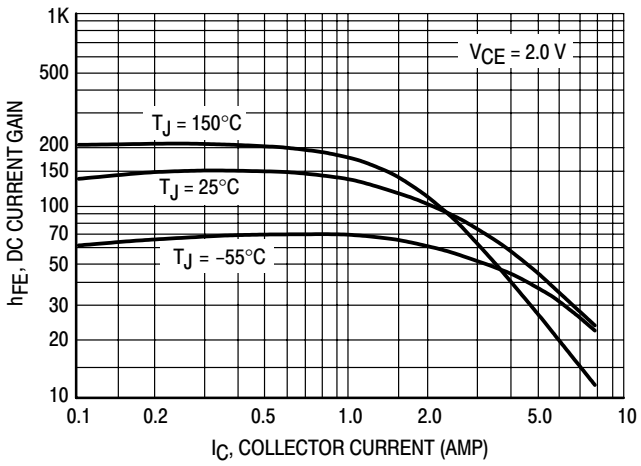


Figure 7. Current Gain−Bandwidth Product

NPN — MJE15028 MJE15030



PNP — MJE15029 MJE15031

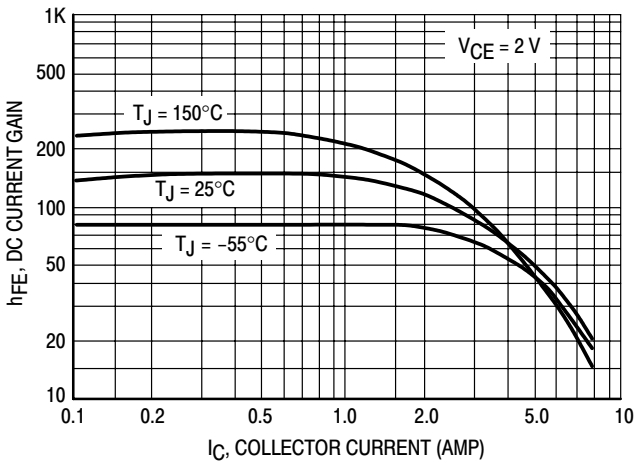
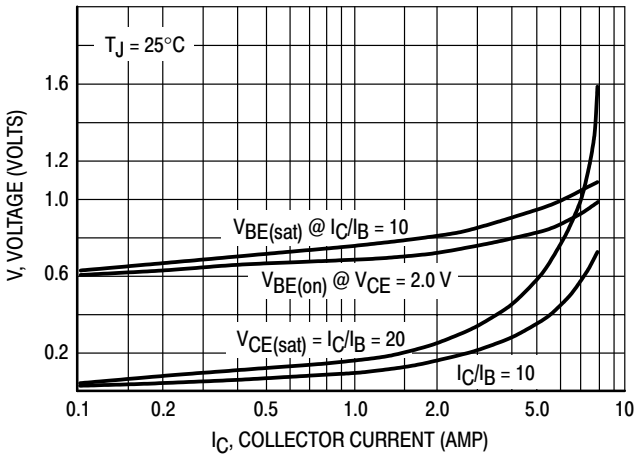


Figure 8. DC Current Gain

NPN



PNP

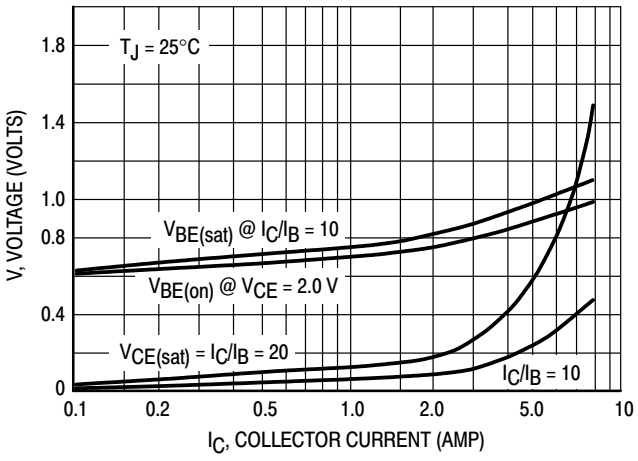


Figure 9. “On” Voltage

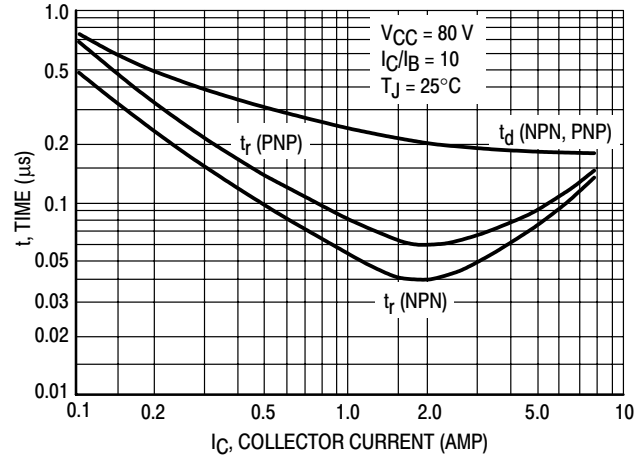


Figure 10. Turn−On Times

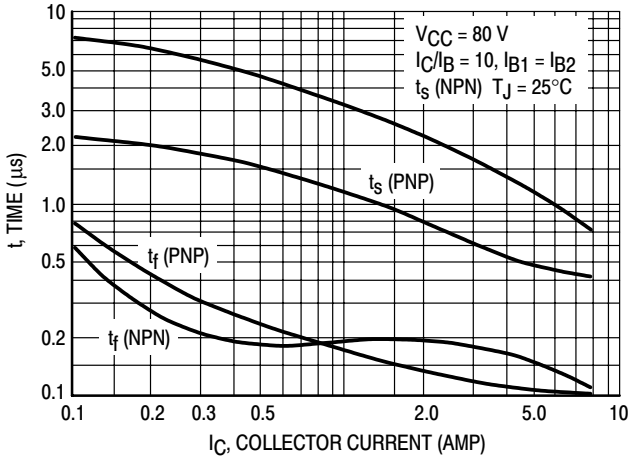


Figure 11. Turn−Off Times

MJE15032 (NPN), MJE15033 (PNP)

Preferred Devices

Complementary Silicon Plastic Power Transistors

Designed for use as high−frequency drivers in audio amplifiers.

- DC Current Gain Specified to 5.0 Amperes
  h_{FE} = 70 (Min) @ I_C = 0.5 Adc
  = 10 (Min) @ I_C = 2.0 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 250 Vdc (Min) − MJE15032, MJE15033
- High Current Gain − Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO−220AB Compact Package
- Epoxy Meets UL94, V0 @ 1/8″
- ESD Ratings: Machine Model C
  Human Body Model 3B

MAXIMUM RATINGS

Rating	Symbol	MJE15032 MJE15033	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CB}	250	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	8.0 16	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

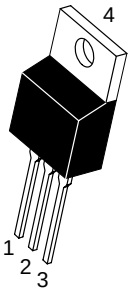
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ON Semiconductor®

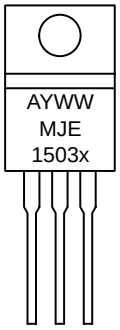
http://onsemi.com

8.0 AMPERES
POWER TRANSISTORS
COMPLEMENTARY SILICON
250 VOLTS
50 WATTS

MARKING DIAGRAM



TO−220
CASE 221A
STYLE 1



MJE1503x = Specific Device Code
x = 2 or 3
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJE15032	TO−220	50 Units/Rail
MJE15033	TO−220	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	−	Vdc
Collector Cutoff Current (V_{CB} = 250 Vdc, I_E = 0)	I_{CBO}	−	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	10	μAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 70 50 10	 − − −	−
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	−	0.5	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	−	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (Note 4) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	30	−	MHz

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. $f_T = |h_{fe}| \bullet f_{test}$.

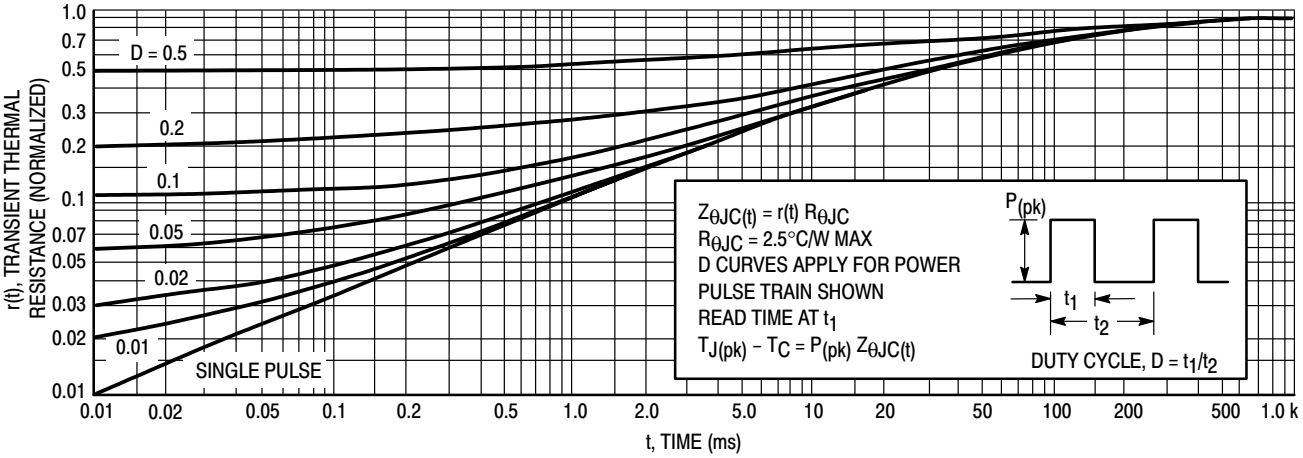


Figure 1. Thermal Response

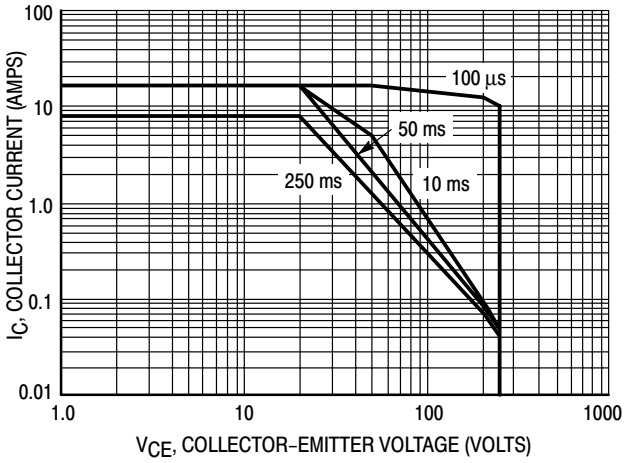


Figure 2. MJE15032 & MJE15033 Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 2 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

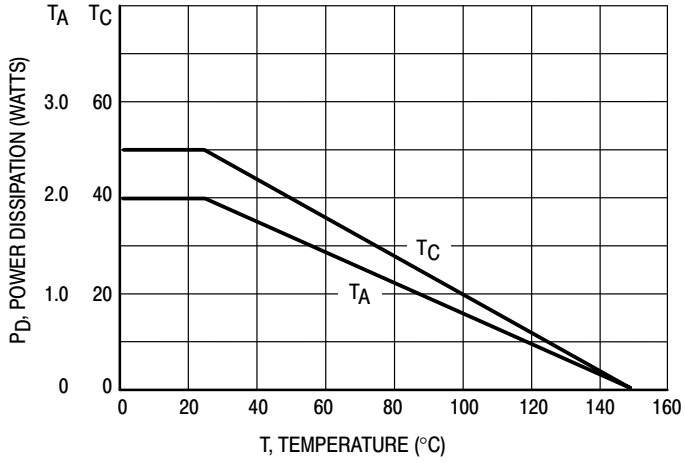


Figure 3. Power Derating

NPN − MJE15032

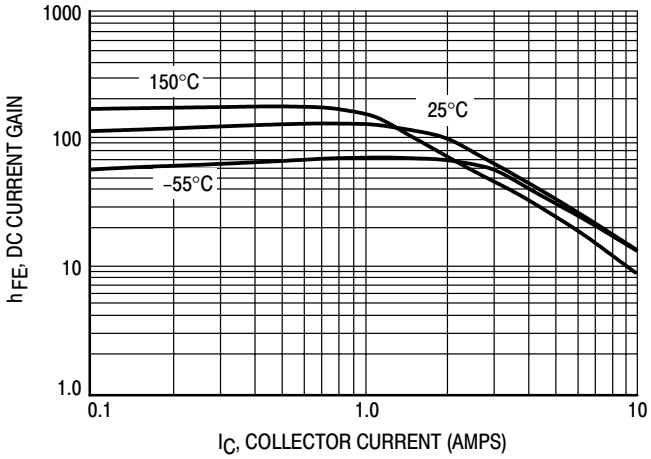


Figure 4. NPN − MJE15032
V_{CE} = 5 V DC Current Gain

PNP − MJE15033

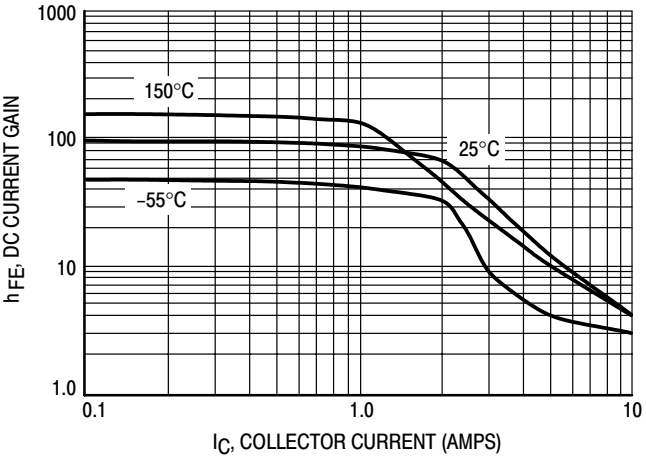


Figure 5. PNP − MJE15033
V_{CE} = 5 V DC Current Gain

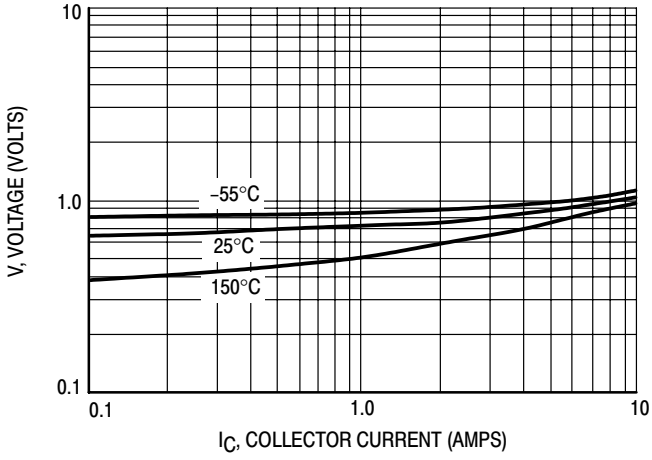


Figure 6. NPN − MJE15032
V_{CE} = 5 V $V_{BE(on)}$ Curve

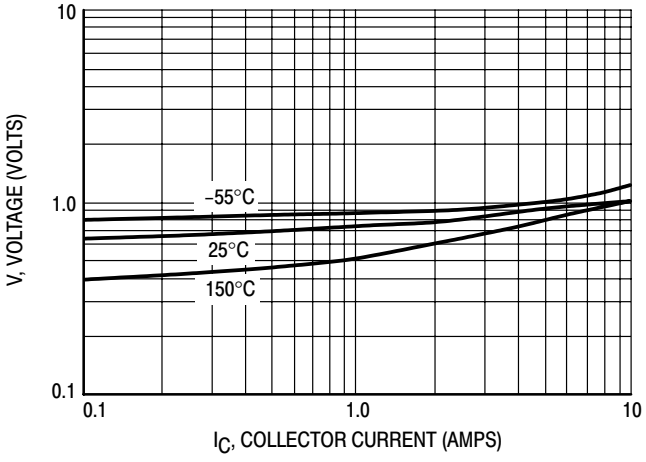


Figure 7. PNP − MJE15033
V_{CE} = 5 V $V_{BE(on)}$ Curve

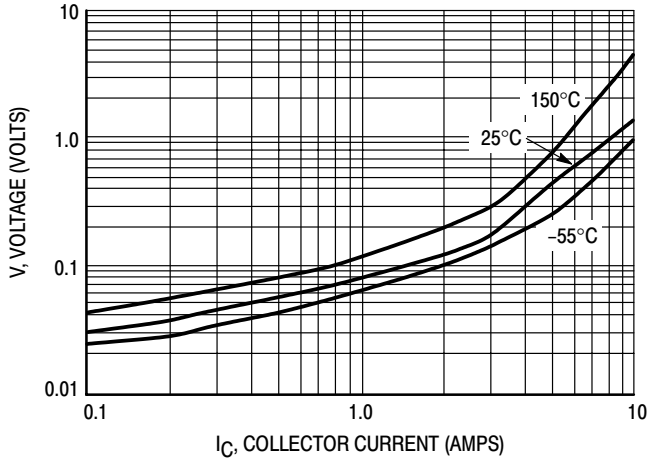


Figure 8. NPN − MJE15032
$V_{CE(sat)}$ I_C/I_B = 10

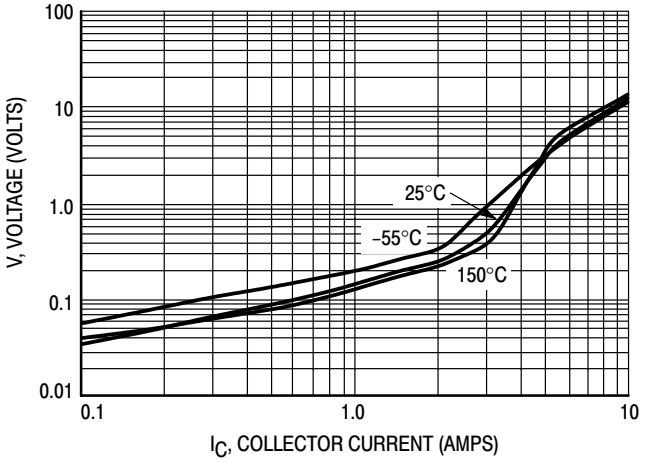


Figure 9. PNP − MJE15033
$V_{CE(sat)}$ I_C/I_B = 10

NPN − MJE15032

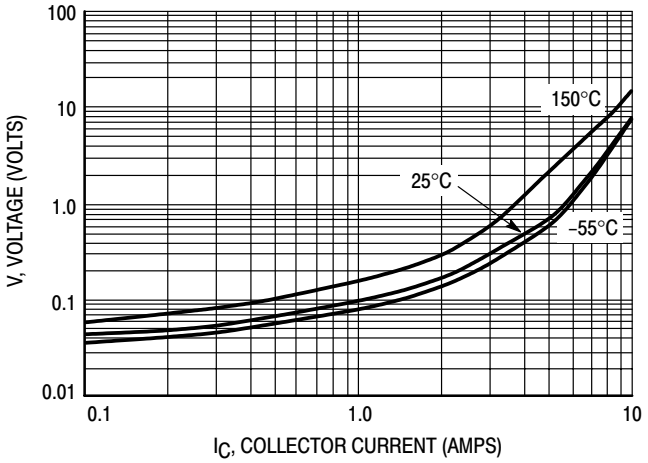


Figure 10. NPN − MJE15032
$V_{CE(sat)}$ I_C/I_B = 20

PNP − MJE15033

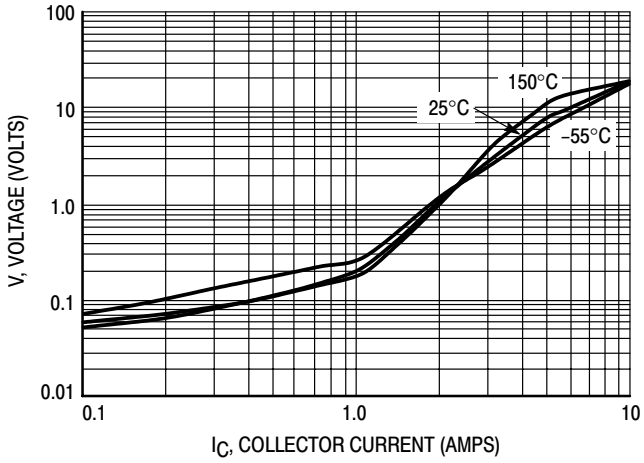


Figure 11. PNP − MJE15033
$V_{CE(sat)}$ I_C/I_B = 20

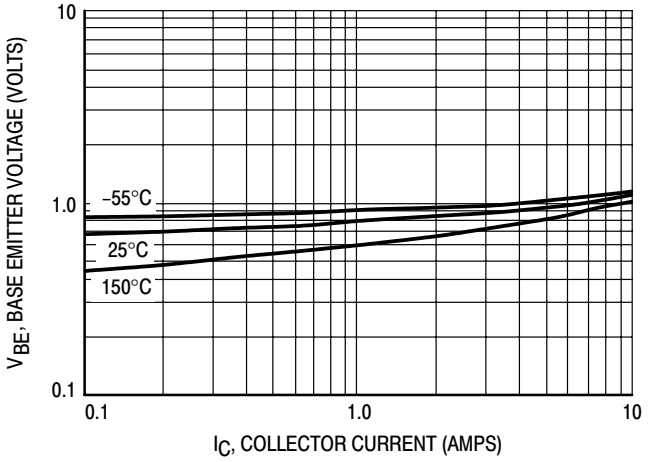


Figure 12. NPN − MJE15032
$V_{BE(sat)}$ I_C/I_B = 10

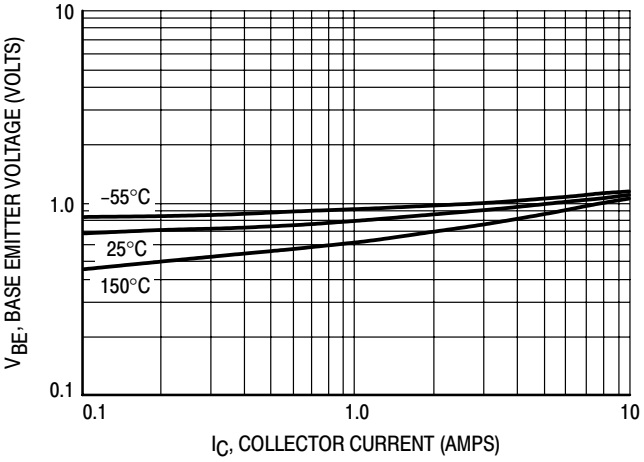


Figure 13. PNP − MJE15033
$V_{BE(sat)}$ I_C/I_B = 10

MJE15034 NPN, MJE15035 PNP

Preferred Device

Complementary Silicon Plastic Power Transistors

TO−220, NPN & PNP Devices

. . . designed for use as high−frequency drivers in audio amplifiers.

- h_{FE} = 100 (Min) @ I_C = 0.5 Adc
  = 10 (Min) @ I_C = 2.0 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 350 Vdc (Min) − MJE15034, MJE15035
- High Current Gain − Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO−220AB Compact Package
- Epoxy meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Machine Model: C
  Human Body Model: 3B

MAXIMUM RATINGS

Rating	Symbol	MJE15034 MJE15035	Unit
Collector−Emitter Voltage	V_{CEO}	350	Vdc
Collector−Base Voltage	V_{CB}	350	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	4.0 8.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

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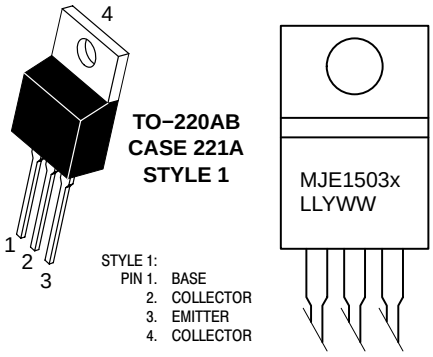
4.0 AMPERES
POWER TRANSISTORS
COMPLEMENTARY
SILICON
350 VOLTS
50 WATTS

MARKING DIAGRAM & PIN ASSIGNMENT



MJE1503x = Device Code
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJE15034	TO−220AB	50 Units/Rail
MJE15035	TO−220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

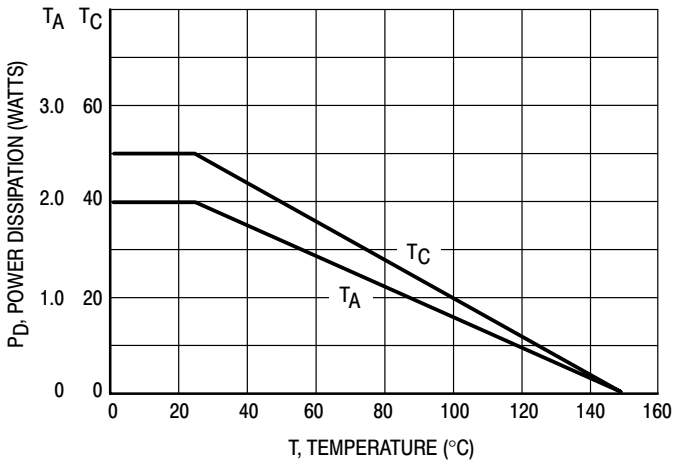


Figure 1. Power Derating

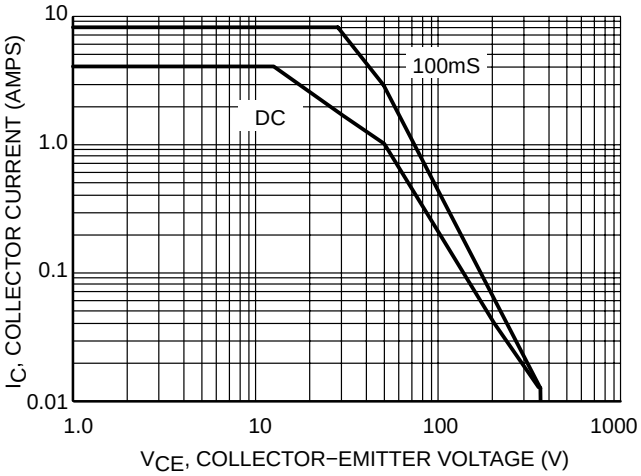


Figure 2. Active Region Safe Operating Area

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1)	(I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	350	−	Vdc
Collector Cutoff Current	(V_{CB} = 350 Vdc, I_E = 0)	I_{CBO}	−	10	μAdc
Emitter Cutoff Current	(V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	10	μAdc
ON CHARACTERISTICS (Note 1)					
DC Current Gain		h_{FE}			−
	(I_C = 0.1 Adc, V_{CE} = 5.0 Vdc)		100	−	
	(I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)		100	−	
	(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		50	−	
	(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)		10	−	
Collector−Emitter Saturation Voltage	(I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	−	0.5	Vdc
Base−Emitter On Voltage	(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	−	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain − Bandwidth Product (Note 2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	30	−	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

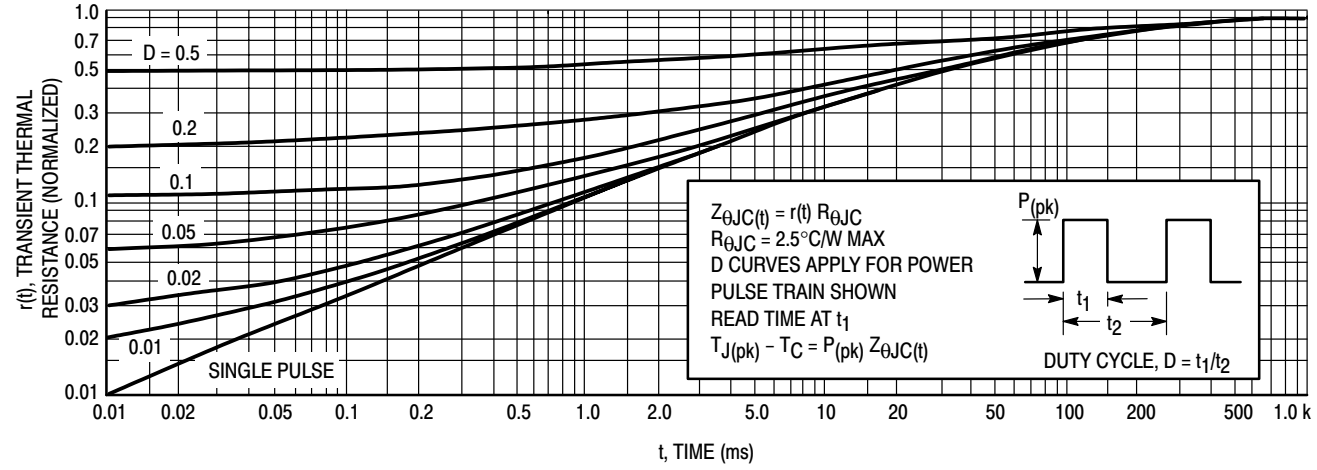


Figure 3. Thermal Response

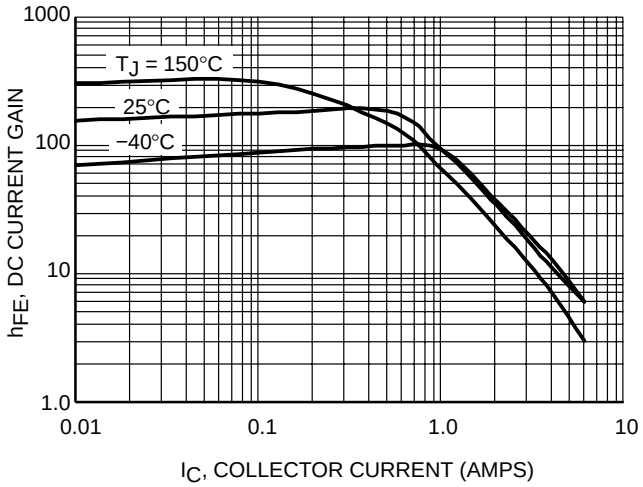


Figure 4. DC Current Gain, V_{CE} = 5.0 V NPN MJE15034

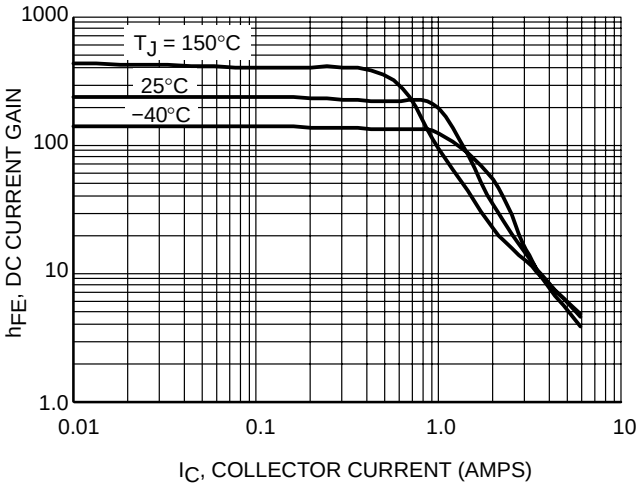


Figure 5. DC Current Gain, V_{CE} = 5.0 V PNP MJE15035

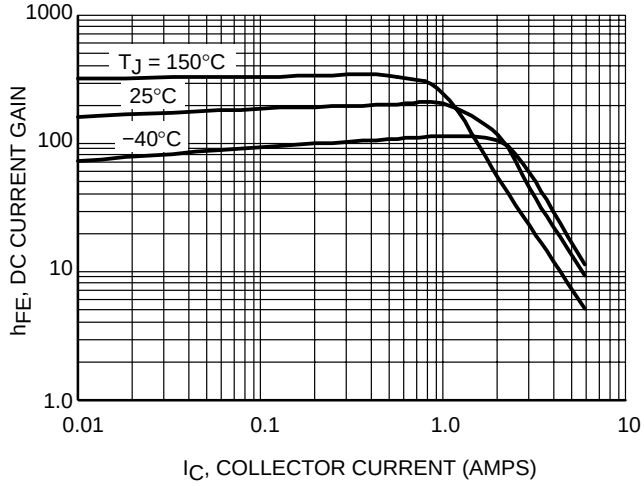


Figure 6. DC Current Gain, V_{CE} = 20 V NPN MJE15034

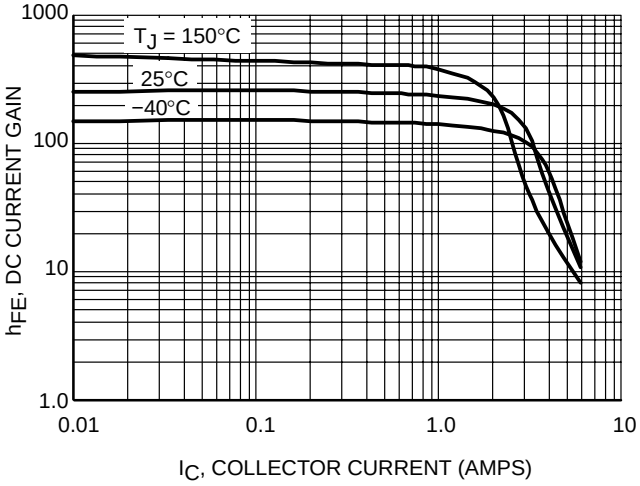


Figure 7. DC Current Gain, V_{CE} = 20 V PNP MJE15035

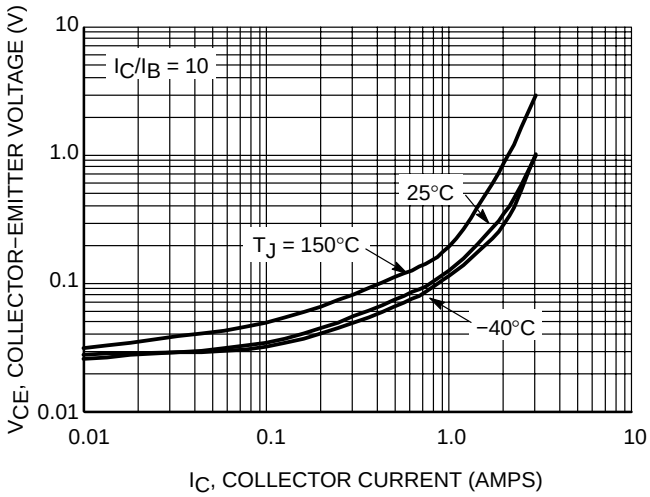


Figure 8. $V_{CE(sat)}$ NPN MJE15034

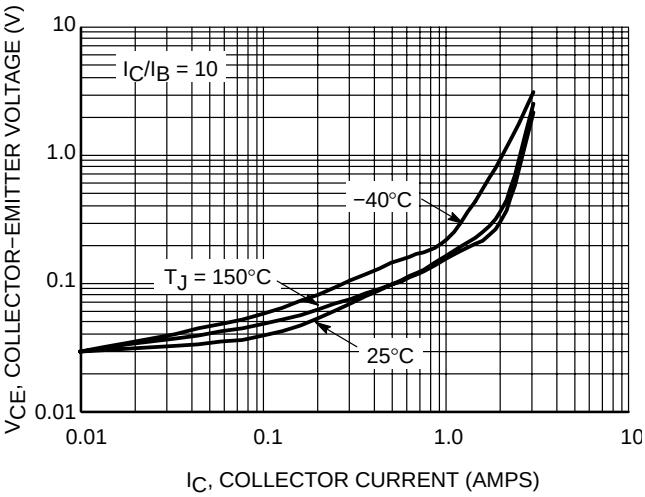


Figure 9. $V_{CE(sat)}$ PNP MJE15035

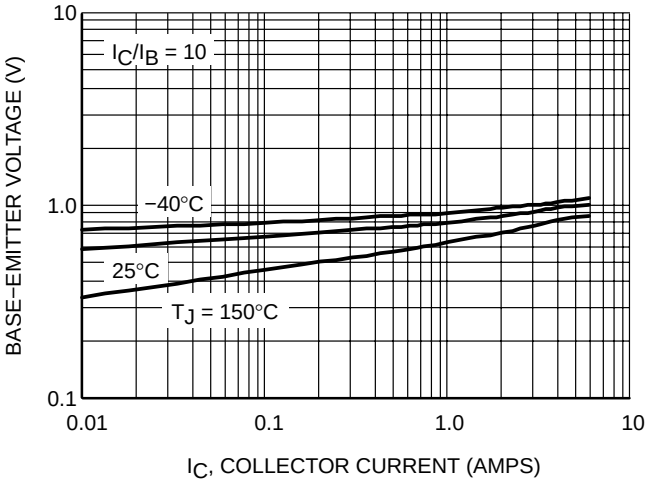


Figure 10. $V_{BE(sat)}$ NPN MJE15034

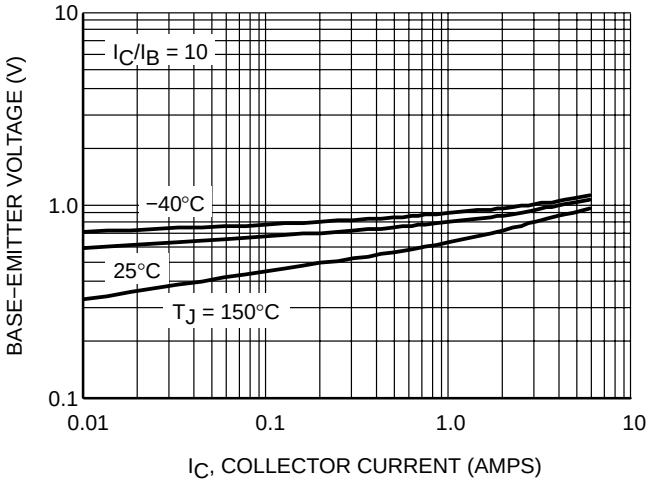


Figure 11. $V_{BE(sat)}$ PNP MJE15035

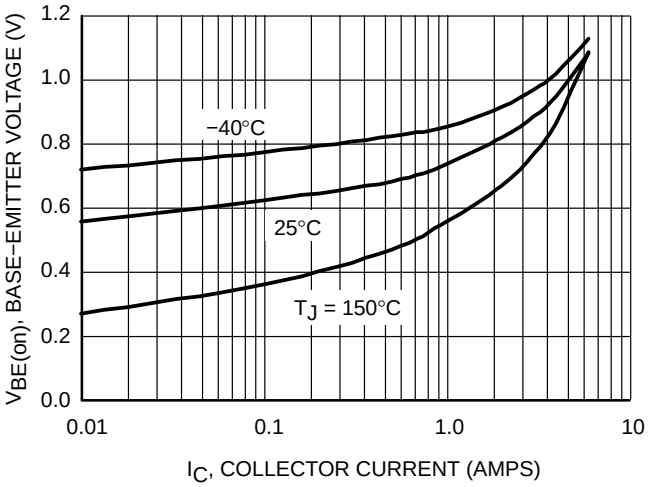


Figure 12. $V_{BE(on)}$ NPN MJE15034

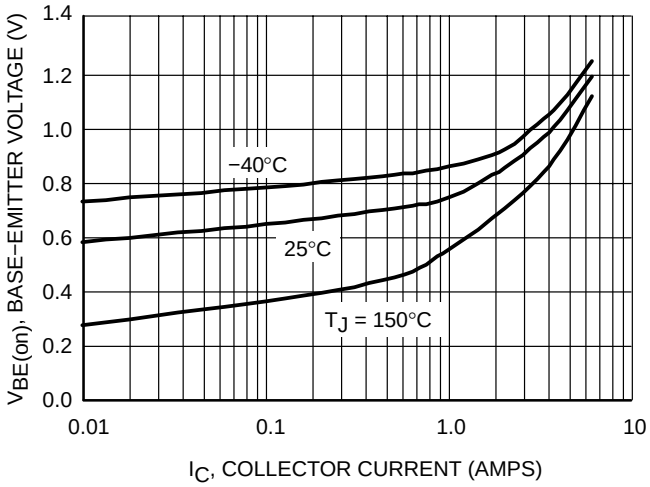


Figure 13. $V_{BE(on)}$ PNP MJE15035

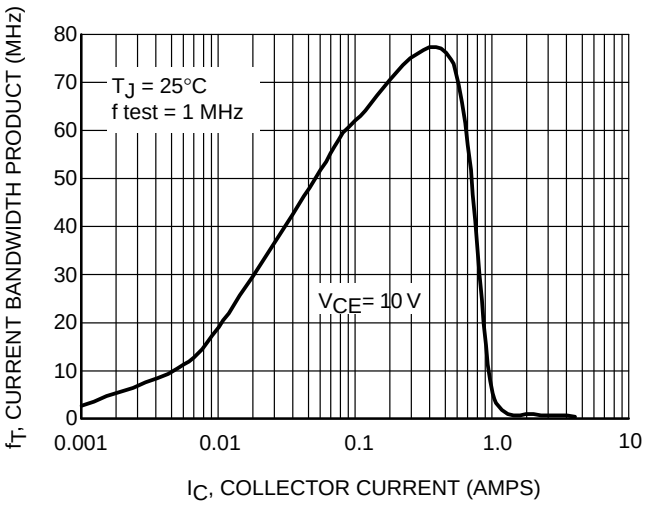


Figure 14. Typical Current Gain Bandwidth Product NPN MJE15034

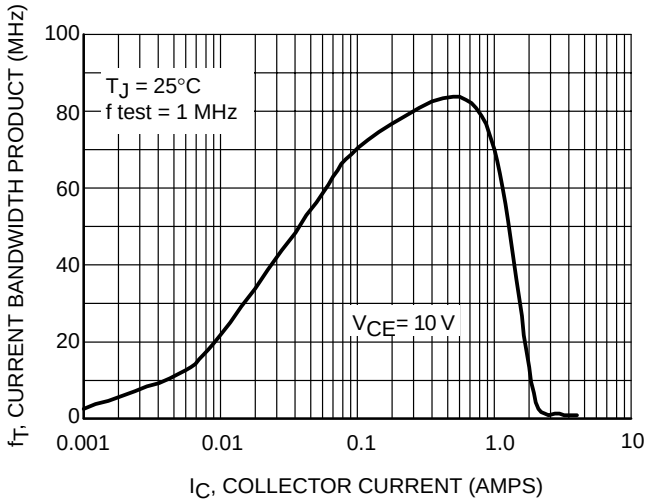


Figure 15. Typical Current Gain Bandwidth Product PNP MJE15035

MJE170, MJE171, MJE172 (PNP), MJE180, MJE181, MJE182 (NPN)

Preferred Device

Complementary Plastic Silicon Power Transistors

The MJE170/180 series is designed for low power audio amplifier and low current, high speed switching applications.

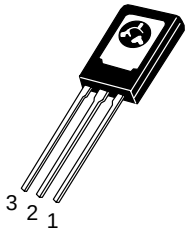
Features

- Pb−Free Package is Available
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 40 Vdc − MJE170, MJE180
  = 60 Vdc − MJE171, MJE181
  = 80 Vdc − MJE172, MJE182
- DC Current Gain −
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current−Gain − Bandwidth Product −
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages −
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Machine Model, C
  Human Body Model, 3B

ON Semiconductor®

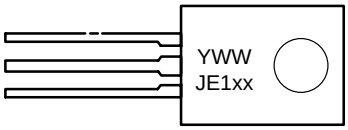
http://onsemi.com

3 AMPERES
POWER TRANSISTORS
COMPLEMENTARY SILICON
40 − 60 − 80 VOLTS
12.5 WATTS



TO−225AA
CASE 77−09
STYLE 1

MARKING DIAGRAM



JE1xx = Specific Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 526 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS

Rating	Symbol	MJE170 MJE180	MJE171 MJE181	MJE172 MJE182	Unit
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Collector−Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter−Base Voltage	V_{EB}	7.0			Vdc
Collector Current − Continuous Peak	I_C	3.0 6.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012			W W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1			W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction−to−Ambient	θ_{JA}	83.4	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
MJE170	TO−225	500 Units / Box
MJE171	TO−225	500 Units / Box
MJE172	TO−225	500 Units / Box
MJE180	TO−225	500 Units / Box
MJE181	TO−225	500 Units / Box
MJE182	TO−225	500 Units / Box
MJE182G	TO−225 (Pb−Free)	500 Units / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

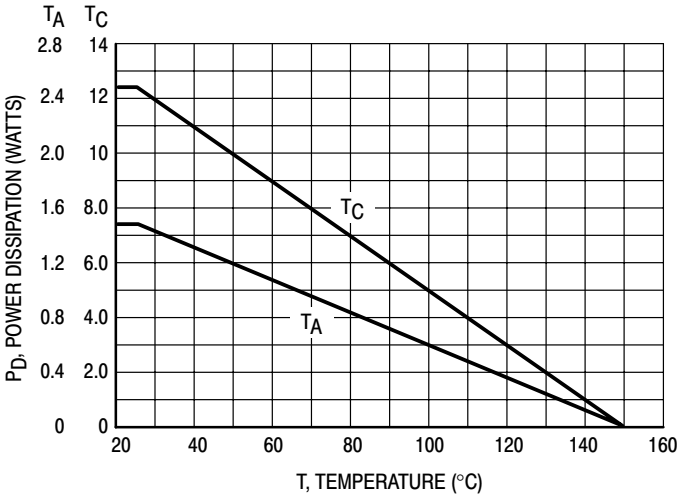


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE170, MJE180 MJE171, MJE181 MJE172, MJE182	$V_{CEO(sus)}$	40 60 80	 − −	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	MJE170, MJE180		−	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		−	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		−	0.1	mAdc
(V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)	MJE170, MJE180				
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		−	0.1	
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		−	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	−	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			−
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	−	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	−	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			−	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			−	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			−	1.7	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			−	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			−	2.0	
Base−Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	−	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 3) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	−	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE171/MJE172		−	60	
	MJE181/MJE182		−	40	

3. $f_T = |h_{fe}| \bullet f_{test}$.

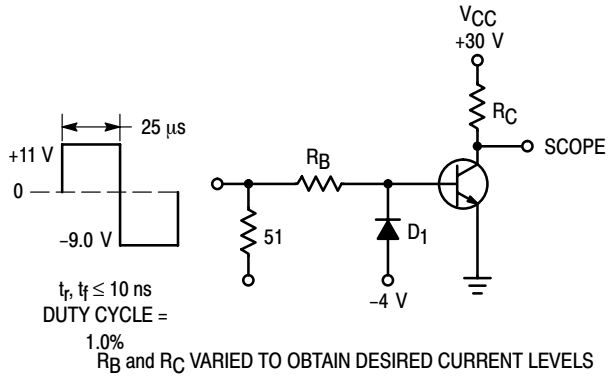


Figure 2. Switching Time Test Circuit

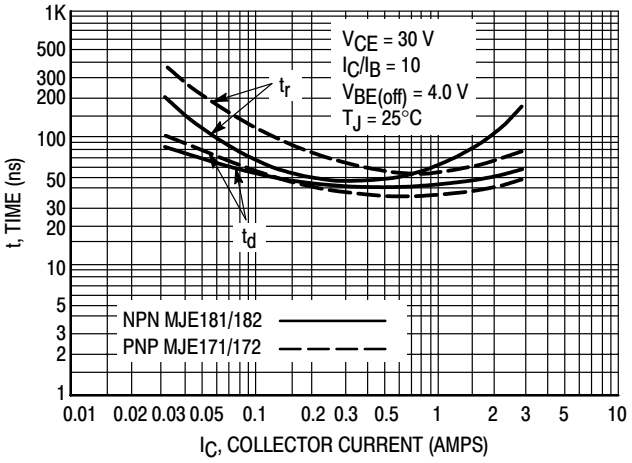


Figure 3. Turn−On Time

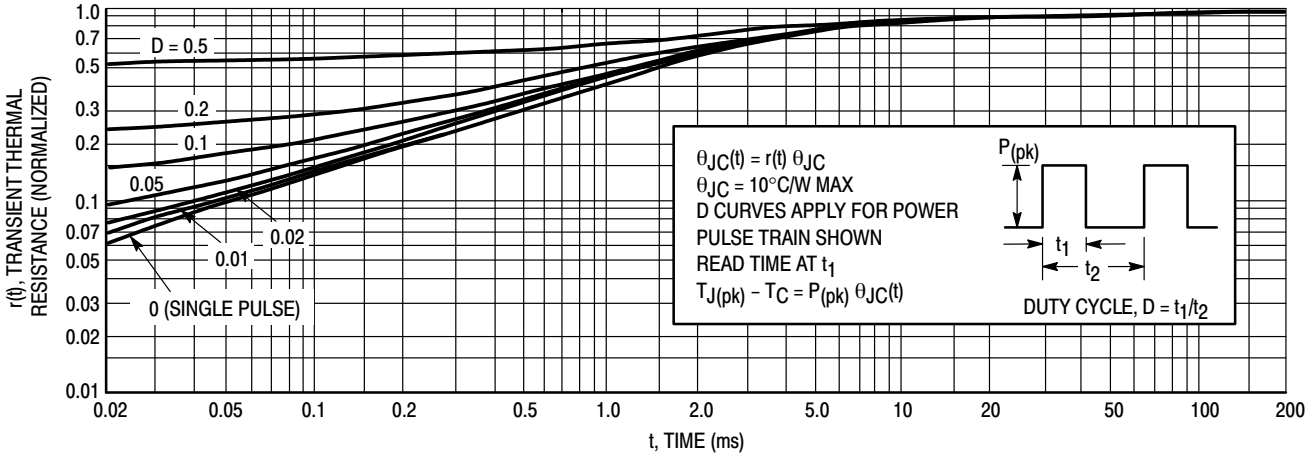


Figure 4. Thermal Response

ACTIVE−REGION SAFE OPERATING AREA

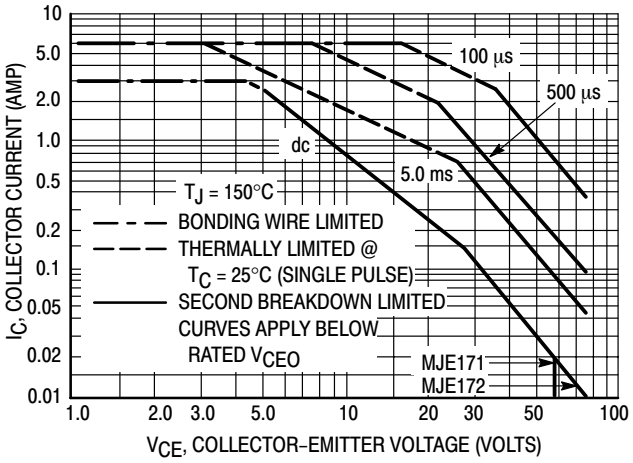


Figure 5. MJE171, MJE172

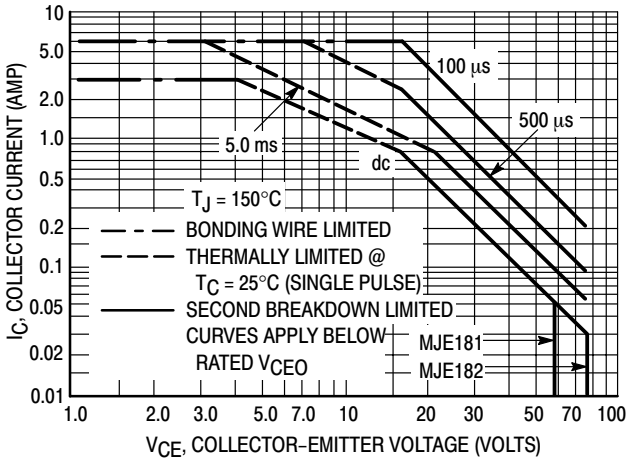


Figure 6. MJE181, MJE182

There are two limitations on the power handling ability of a transistor − average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

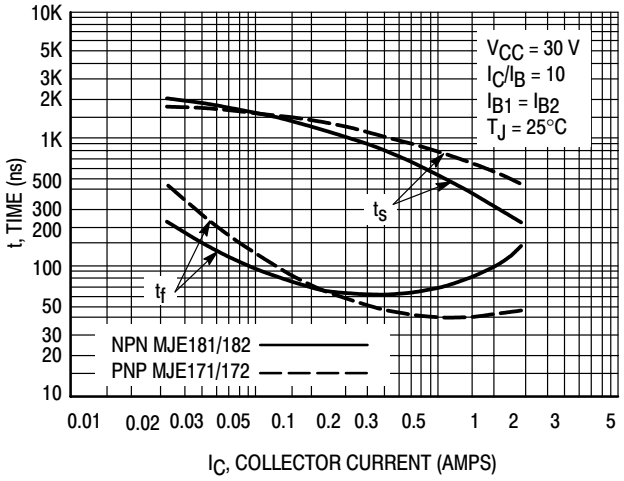


Figure 7. Turn−Off Time

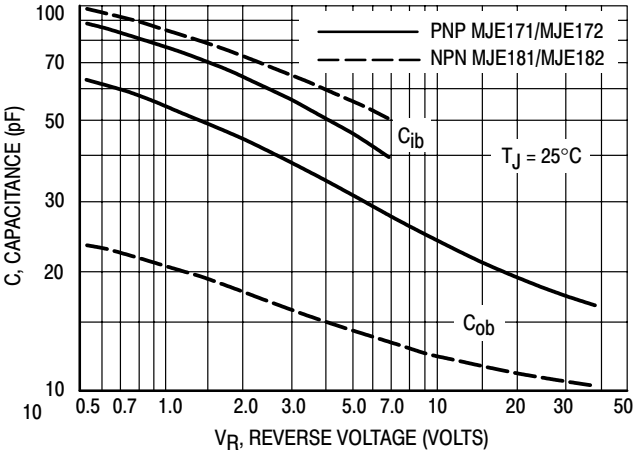


Figure 8. Capacitance

SWITCHMODE™

NPN Bipolar Power Transistor For Switching Power Supply Applications

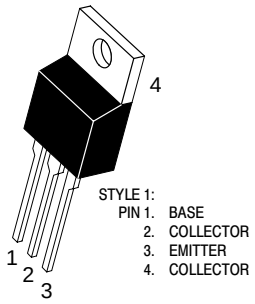
MJE18002*

*ON Semiconductor Preferred Device

POWER TRANSISTOR
2.0 AMPERES
1000 VOLTS
50 WATTS

The MJE18002 have an applications specific state−of−the−art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot−to−Lot
- Standard TO−220



CASE 221A−09
TO−220AB
MJE18002

MAXIMUM RATINGS

Rating	Symbol	MJE18002	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current − Continuous − Peak(1)	I_C I_{CM}	2.0 5.0	Adc
Base Current − Continuous − Peak(1)	I_B I_{BM}	1.0 2.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18002	Unit
Thermal Resistance − Junction to Case − Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	−	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	−	−	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) @ T_C = 125°C	I_{CES}	−	−	100	μAdc
(V_{CE} = 800 V, V_{EB} = 0)		−	−	500	
(V_{CE} = 800 V, V_{EB} = 0) @ T_C = 125°C		−	−	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	−	−	100	μAdc
ON CHARACTERISTICS					
Base−Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	−	0.825	1.1	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)		−	0.92	1.25	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)		−	0.2	0.5	
@ T_C = 125°C		−	0.2	0.5	
(I_C = 1.0 Adc, I_B = 0.2 Adc)		−	0.25	0.5	
@ T_C = 125°C		−	0.3	0.6	
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	−	34	−
@ T_C = 125°C		−	27	−	
(I_C = 0.4 Adc, V_{CE} = 1.0 Vdc)		11	17	−	
@ T_C = 125°C		11	20	−	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		6.0	8.0	−	
@ T_C = 125°C		5.0	8.0	−	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	−	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	−	13	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	−	35	60	pF
Input Capacitance (V_{EB} = 8.0 V)	C_{ib}	−	400	600	pF
Dynamic Saturation: determined 1.0 μs and 3.0 μs after rising I_{B1} reach 0.9 final I_{B1} (see Figure 18)	$V_{CE(dsat)}$				Vdc
I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V; 1.0 μs; @ T_C = 125°C		−	3.5	−	
		−	8.0	−	
I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V; 3.0 μs; @ T_C = 125°C		−	1.5	−	
		−	3.8	−	
I_C = 1.0 A, I_{B1} = 0.2 A, V_{CC} = 300 V; 1.0 μs; @ T_C = 125°C		−	8.0	−	
		−	14	−	
I_C = 1.0 A, I_{B1} = 0.2 A, V_{CC} = 300 V; 3.0 μs; @ T_C = 125°C		−	2.0	−	
		−	7.0	−	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS − continued (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn−On Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 0.2 Adc V_{CC} = 300 V		t_{on}	− −	200 130	300 −	ns
Turn−Off Time		@ T_C = 125°C	t_{off}	− −	1.2 1.5	2.5 −	μs
Turn−On Time	I_C = 1.0 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc V_{CC} = 300 V		t_{on}	− −	85 95	150 −	ns
Turn−Off Time		@ T_C = 125°C	t_{off}	− −	1.7 2.1	2.5 −	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 0.2 Adc		t_{fi}	− −	125 120	200 −	ns
Storage Time		@ T_C = 125°C	t_{si}	− −	0.7 0.8	1.25 −	μs
Crossover Time		@ T_C = 125°C	t_c	− −	110 110	200 −	ns
Fall Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc		t_{fi}	− −	110 120	175 −	ns
Storage Time		@ T_C = 125°C	t_{si}	− −	1.7 2.25	2.75 −	μs
Crossover Time		@ T_C = 125°C	t_c	− −	200 250	300 −	ns
Fall Time	I_C = 0.4 Adc, I_{B1} = 50 mAdc, I_{B2} = 50 mAdc		t_{fi}	− −	140 185	200 −	ns
Storage Time		@ T_C = 125°C	t_{si}	− −	2.2 2.5	3.0 −	μs
Crossover Time		@ T_C = 125°C	t_c	− −	140 220	250 −	ns

TYPICAL STATIC CHARACTERISTICS

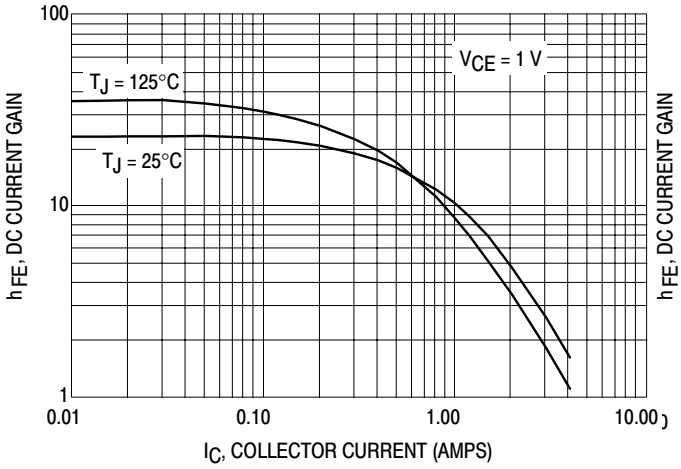


Figure 1. DC Current Gain @ 1 Volt

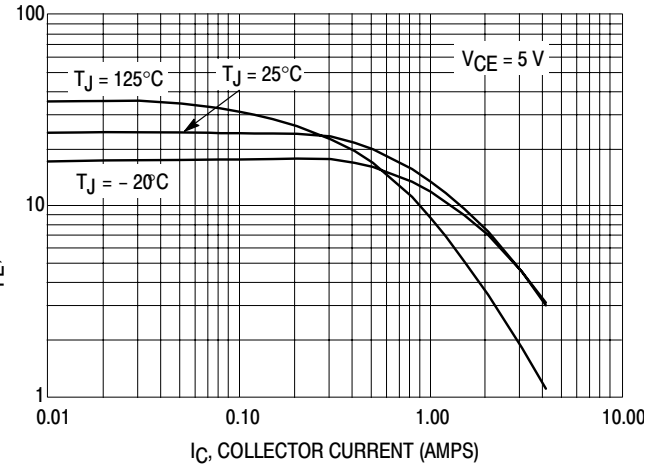


Figure 2. DC Current Gain @ 5 Volts

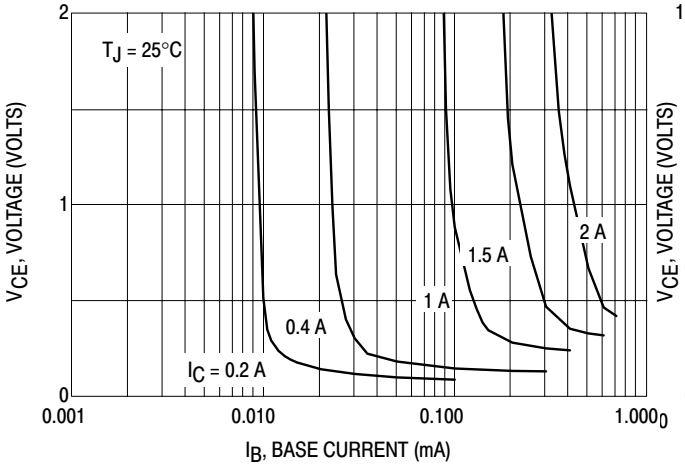


Figure 3. Collector Saturation Region

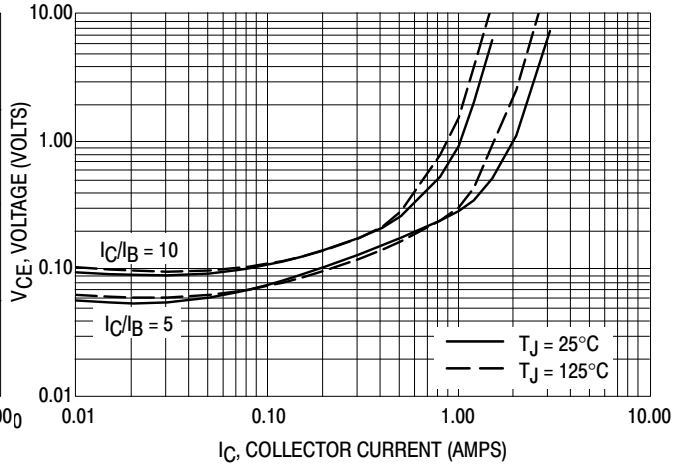


Figure 4. Collector−Emitter Saturation Voltage

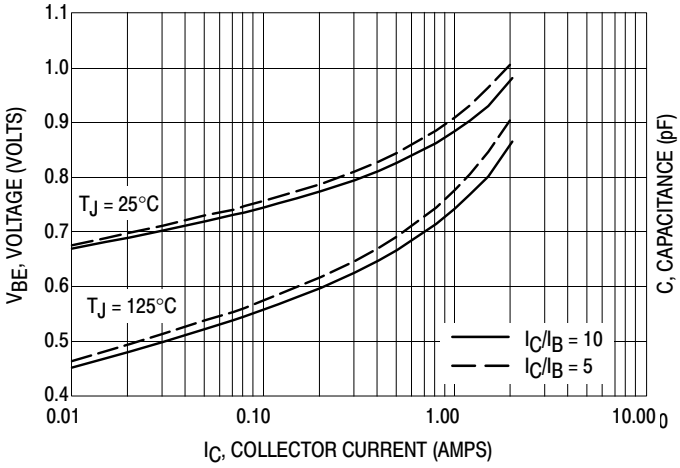


Figure 5. Base−Emitter Saturation Region

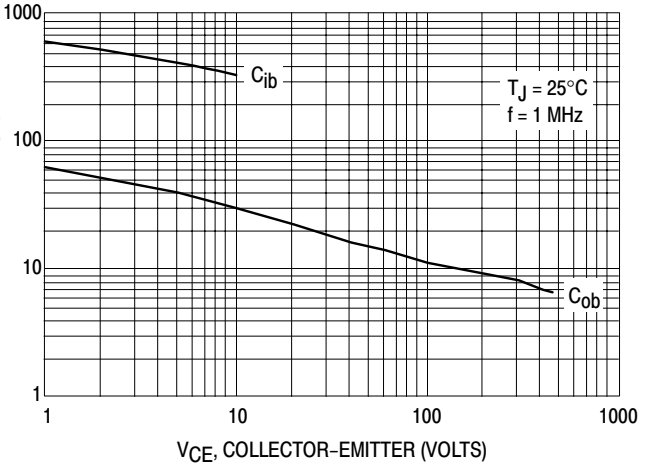


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

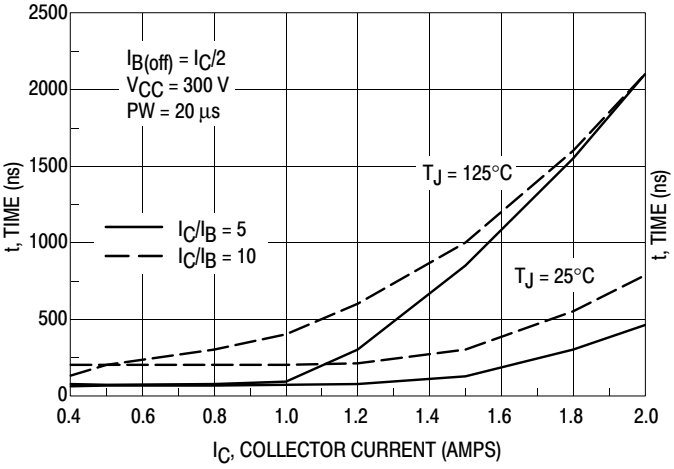


Figure 7. Resistive Switching, t_{on}

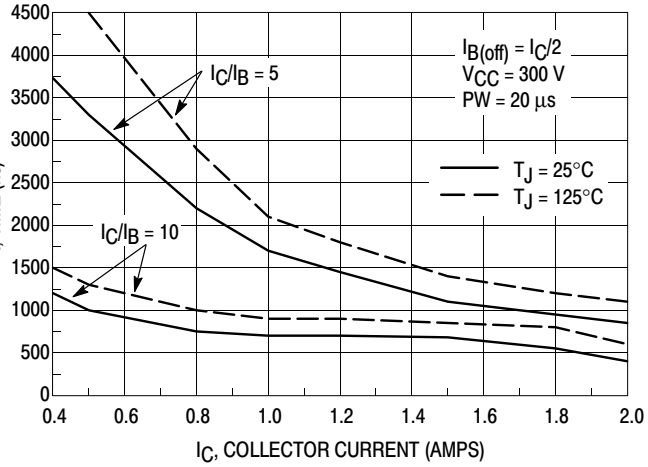


Figure 8. Resistive Switching, t_{off}

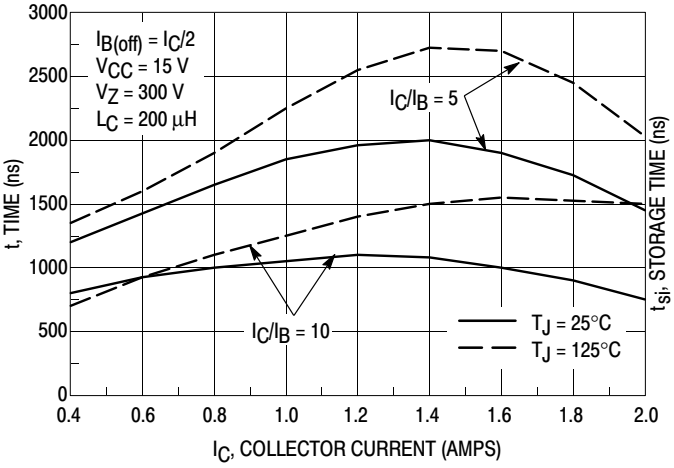


Figure 9. Inductive Storage Time, t_{si}

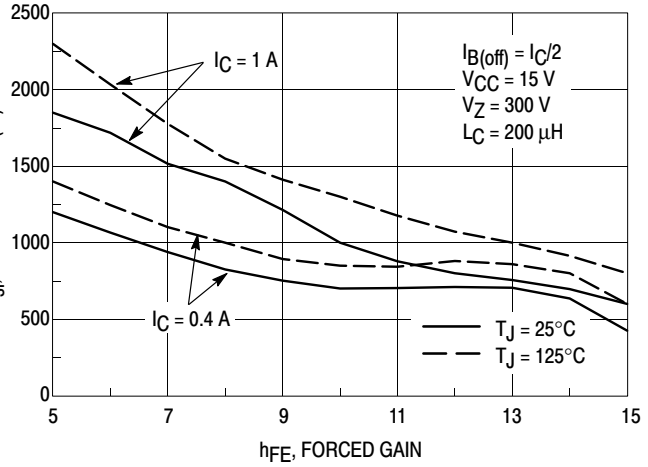


Figure 10. Inductive Storage Time

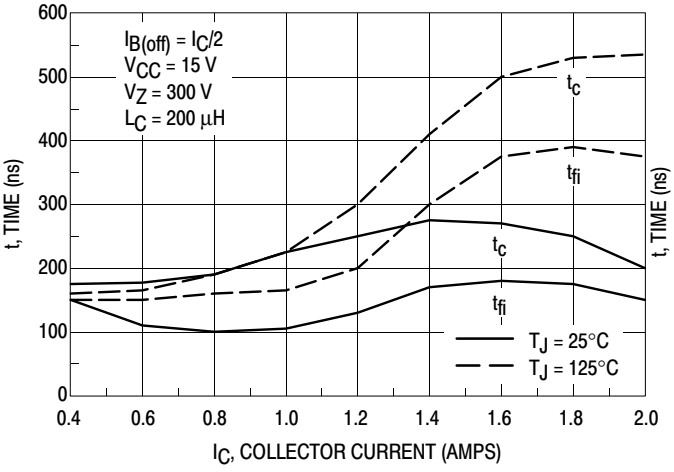


Figure 11. Inductive Switching, t_c and t_{fi}, I_C/I_B = 5

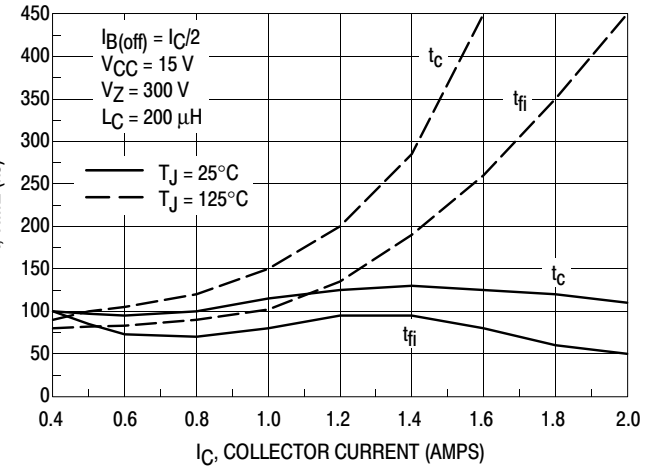


Figure 12. Inductive Switching, t_c and t_{fi}, I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

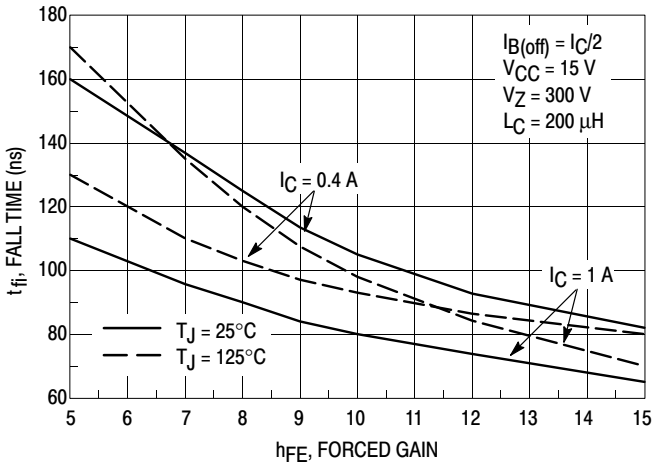


Figure 13. Inductive Fall Time

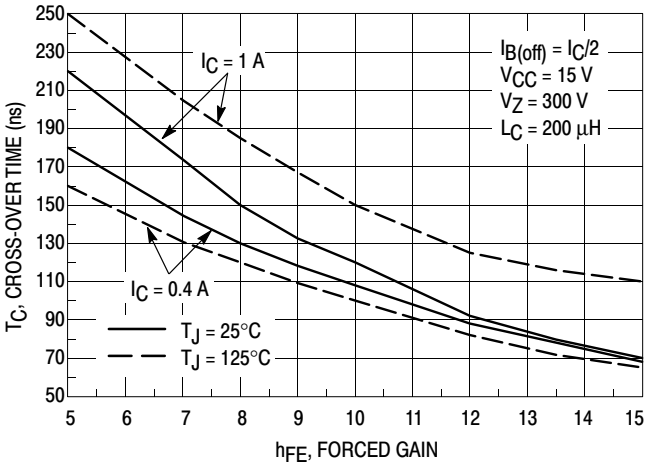


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

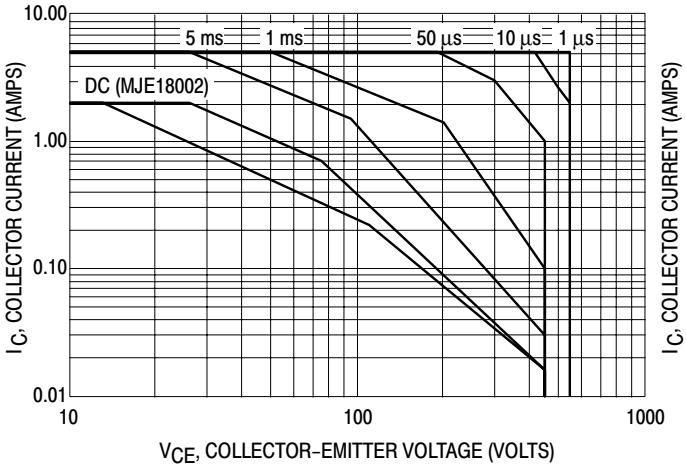


Figure 15. Forward Bias Safe Operating Area

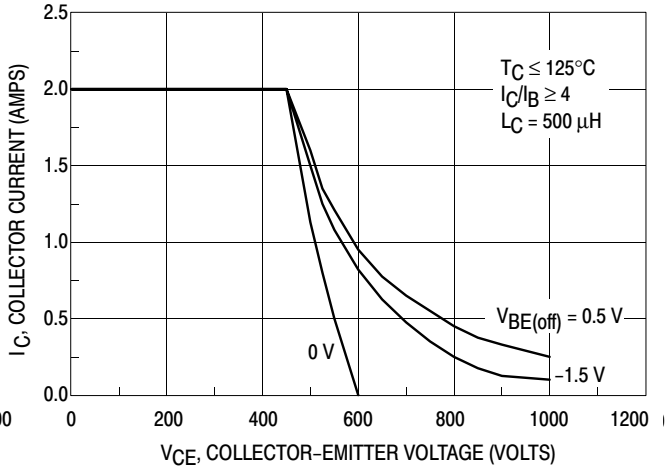


Figure 16. Reverse Bias Switching Safe Operating Area

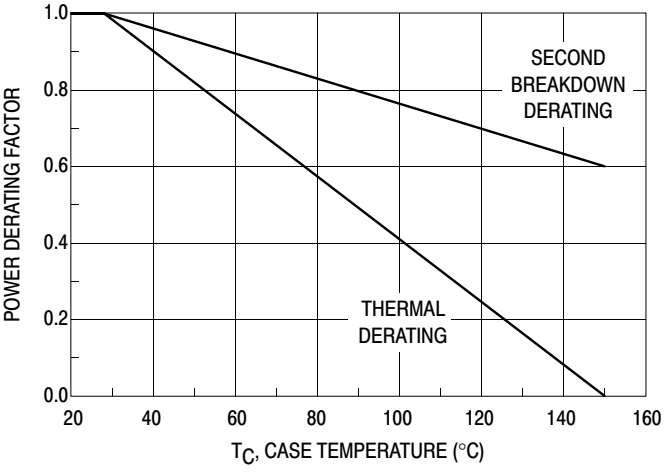


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. T_J(pk) may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

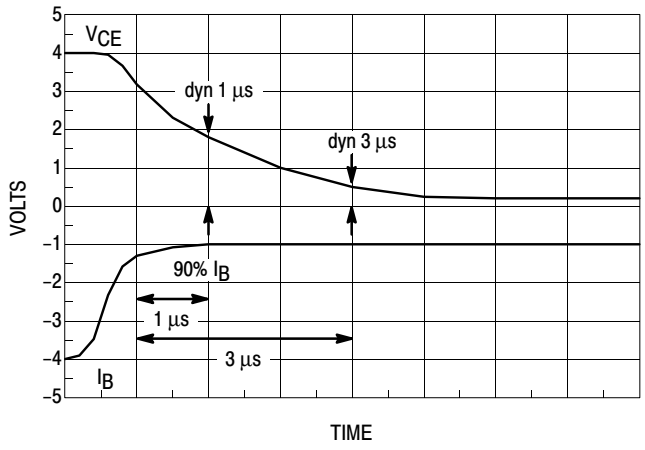


Figure 18. Dynamic Saturation Voltage Measurements

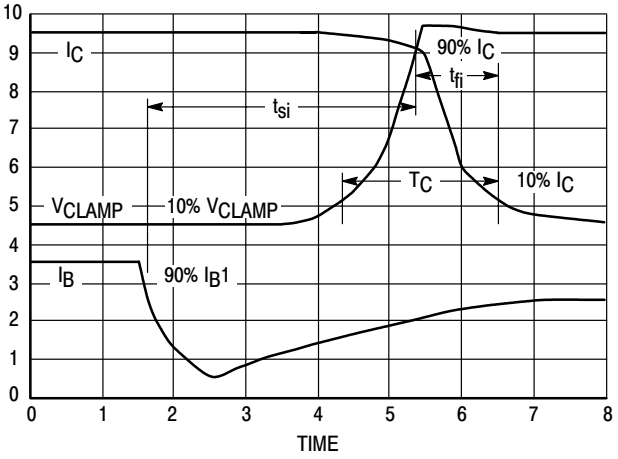
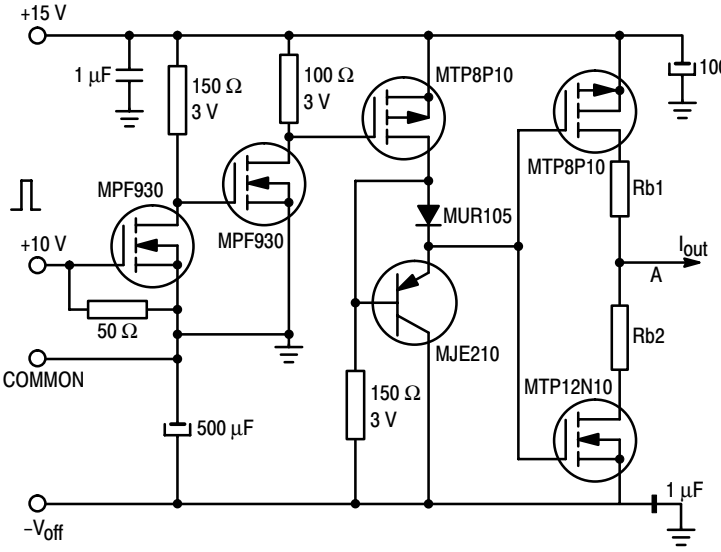
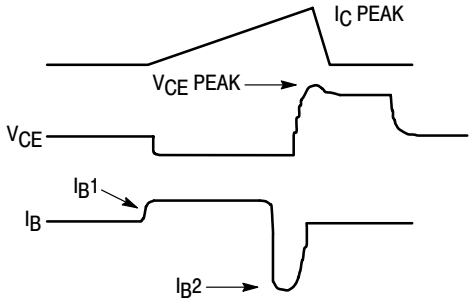


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 μH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

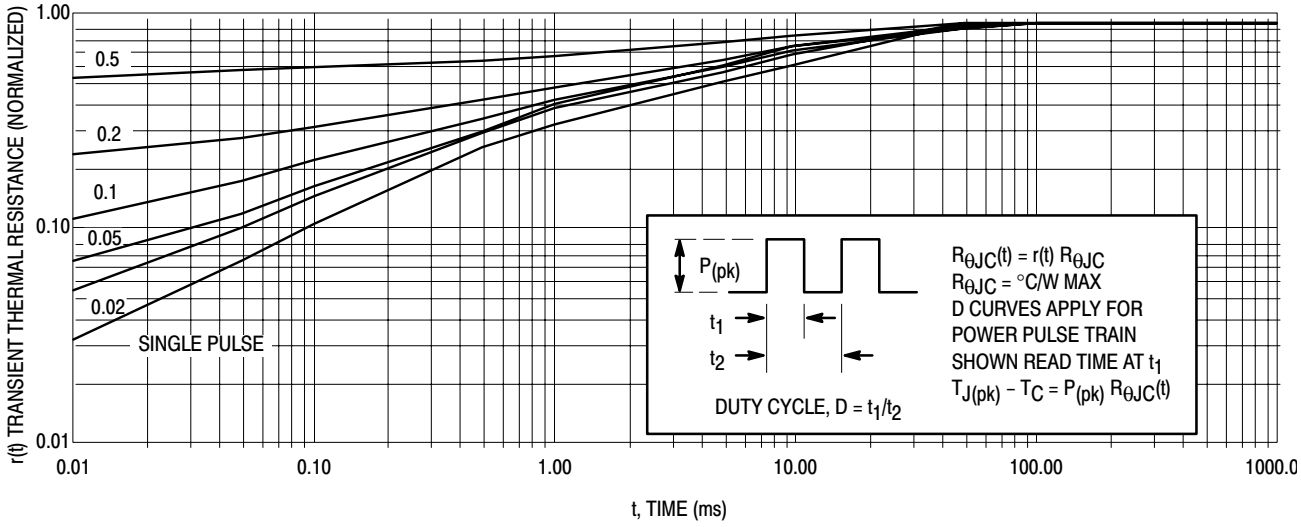


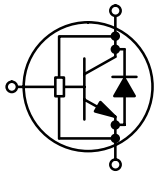
Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18002

MJE18004D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
5 AMPERES
1000 VOLTS
75 WATTS

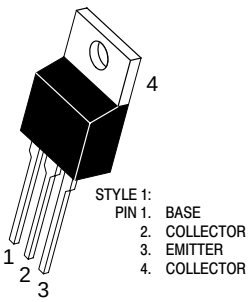
The MJE18004D2 is state−of−art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.



Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector−Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	547		Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	1000	1100		Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter−Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.9 0.8	1 0.9	
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.45 0.75	0.75 1	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.9 1.6	1.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.25 0.28	0.5 0.6	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 10	28 14		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	8 6		
(I_C = 1 Adc, V_{CE} = 2.5 Vdc)	@ T_C = 25°C @ T_C = 125°C		18 14	28 20		
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc I_{B1} = 100 mA V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	9 16		V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		3.1 9		
	I_C = 2 Adc I_{B1} = 0.4 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		11 18		
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C		1.4 8		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 1 Adc)		@ T_C = 25°C @ T_C = 125°C	V_{EC}		0.96 0.72	1.5	V
(I_{EC} = 2 Adc)		@ T_C = 25°C @ T_C = 125°C			1.15 0.8	1.7	
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/μs)		@ T_C = 25°C	t_{fr}		440		ns
(I_F = 1 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
(I_F = 2 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		60	100	pF
Input Capacitance (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			C_{ib}		450	750	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn−on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 1 Adc V_{CC} = 250 Vdc	@ T_C = 25°C	t_{on}		500	750	ns
Turn−off Time		@ T_C = 25°C	t_{off}	1.1		1.4	μs
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		100 150	150	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.6	1.3	μs
Turn−on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		120 500	150	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	1.85	 2.6	2.15	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 2.5 Adc I_{B1} = 500 mAdc I_{B2} = 500 mAdc V_Z = 350 V L_C = 300 μH	@ T_C = 25°C @ T_C = 125°C	t_f		130 300	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.12 2.6	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		355 750	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 400 mAdc I_{B2} = 400 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		95 230	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 2.9	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		300 700	450	ns
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		70 100	90	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.7 1.05	0.9	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		75 160	120	ns

TYPICAL STATIC CHARACTERISTICS

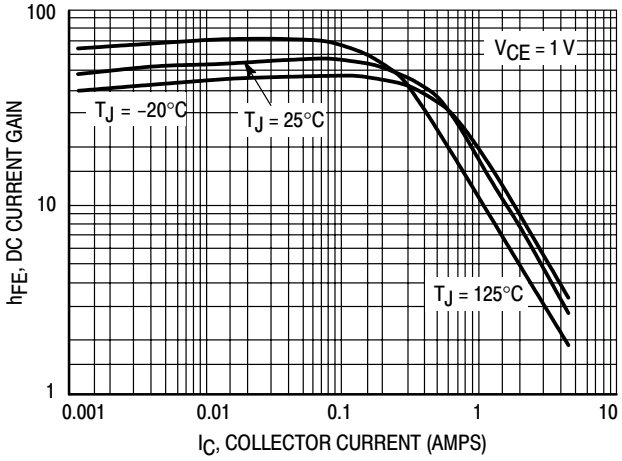


Figure 1. DC Current Gain @ 1 Volt

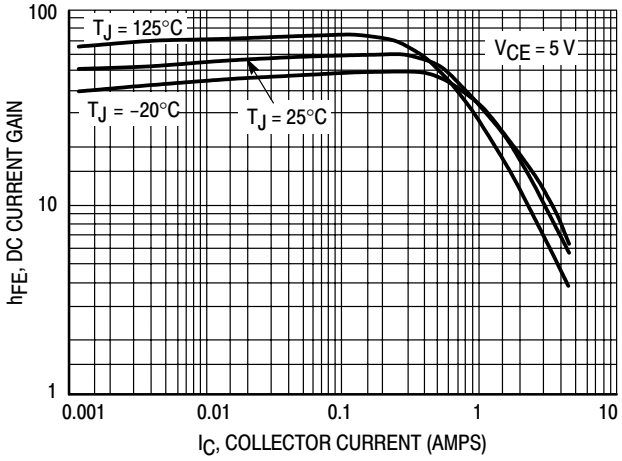


Figure 2. DC Current Gain @ 5 Volt

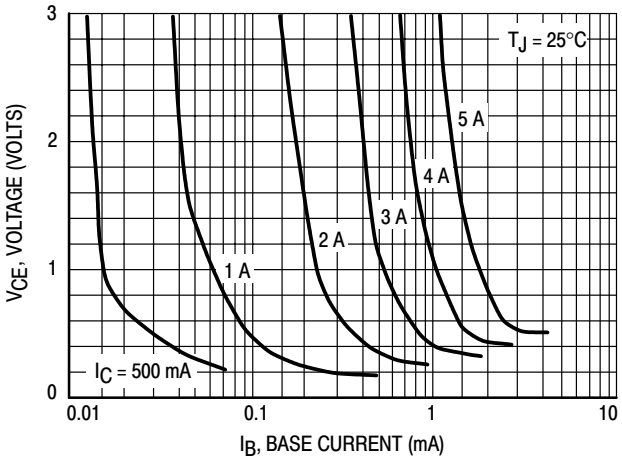


Figure 3. Collector Saturation Region

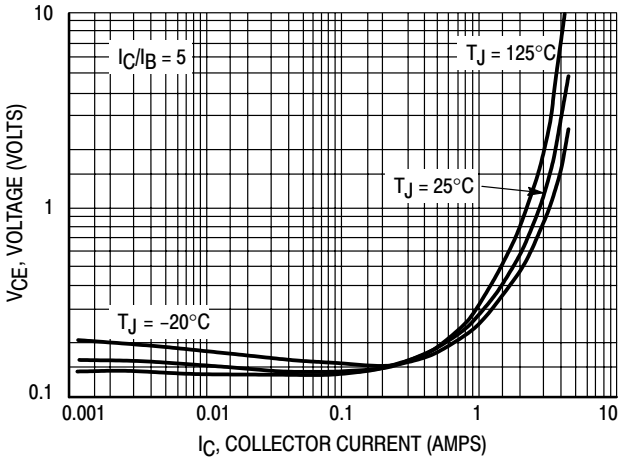


Figure 4. Collector−Emitter Saturation Voltage

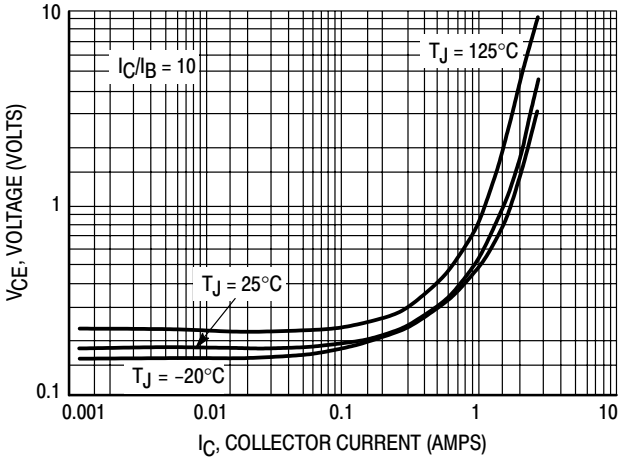


Figure 5. Collector−Emitter Saturation Voltage

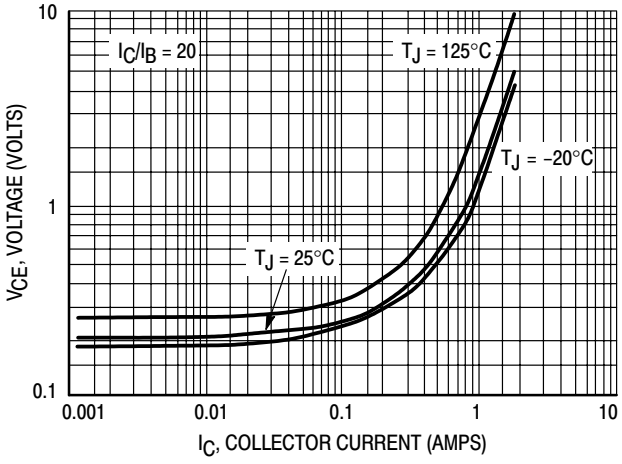


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

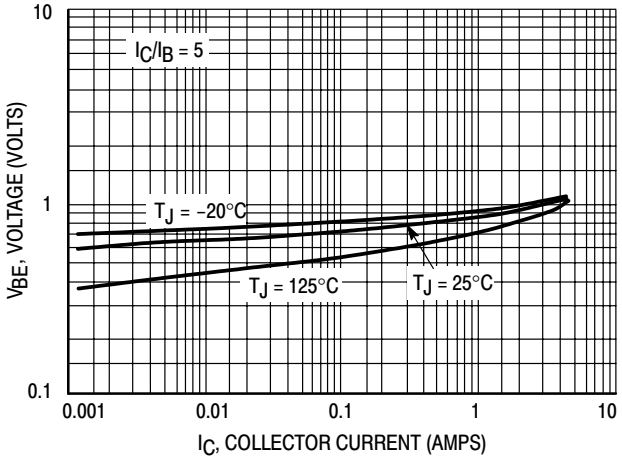


Figure 7. Base−Emitter Saturation Region

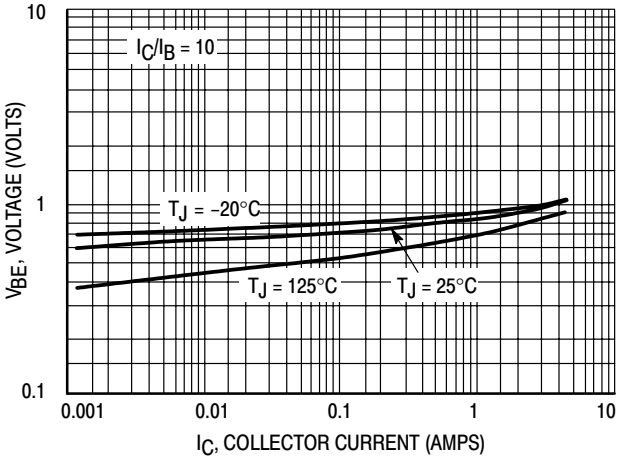


Figure 8. Base−Emitter Saturation Region

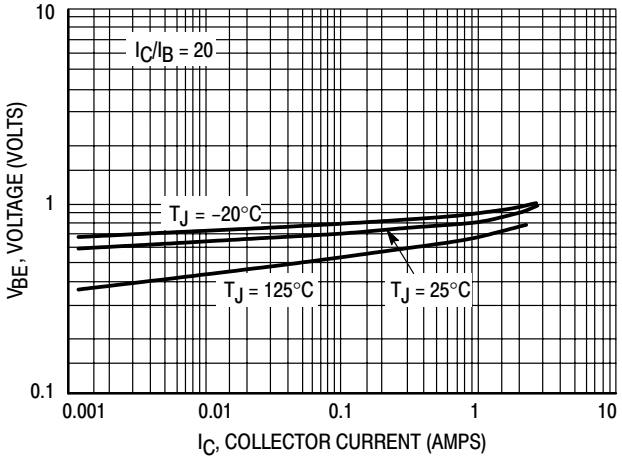


Figure 9. Base−Emitter Saturation Region

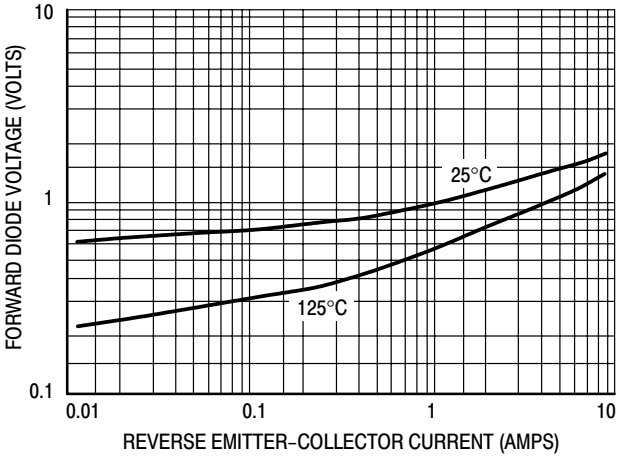


Figure 10. Forward Diode Voltage

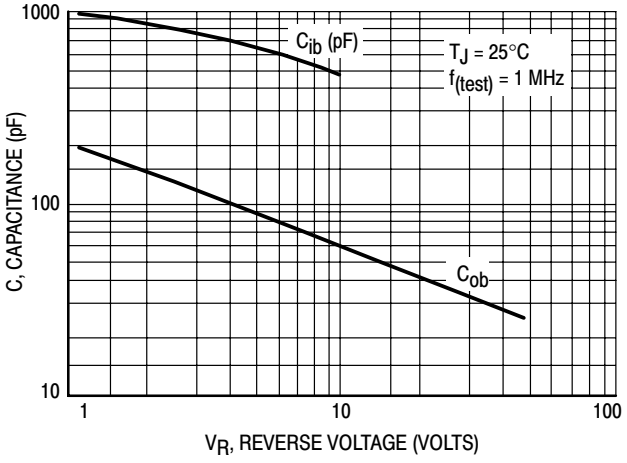


Figure 11. Capacitance

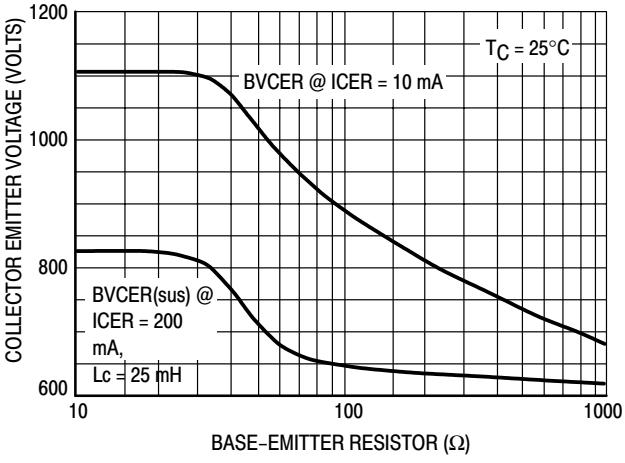


Figure 12. BVCER = f(R_{BE})

TYPICAL SWITCHING CHARACTERISTICS

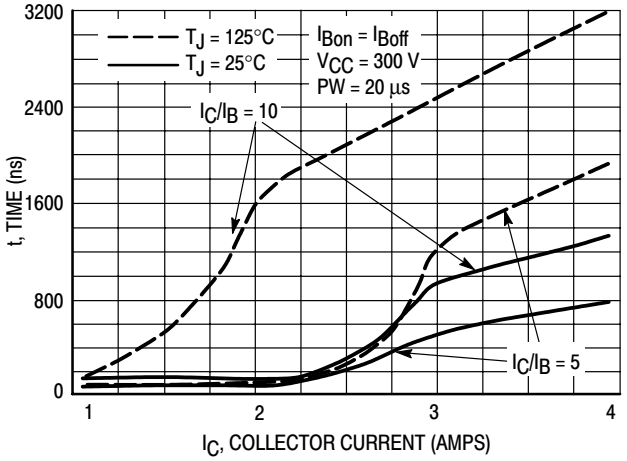


Figure 13. Resistive Switch Time, t_{on}

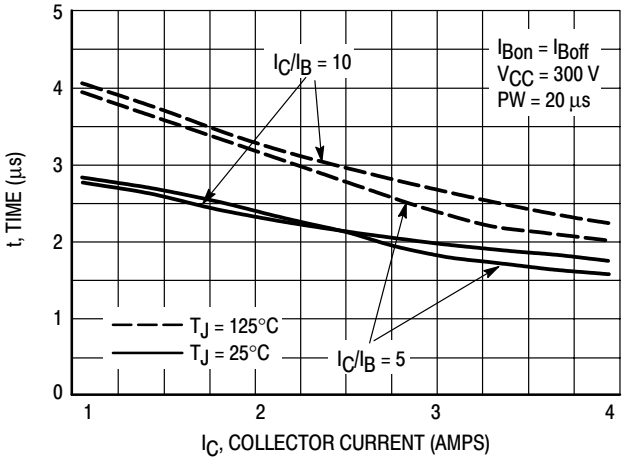


Figure 14. Resistive Switch Time, t_{off}

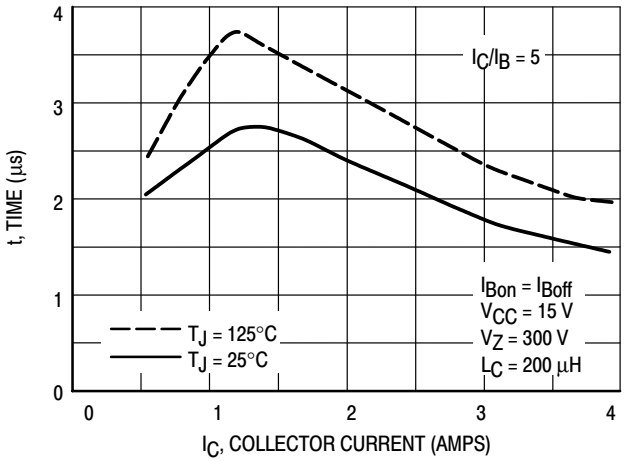


Figure 15. Inductive Storage Time, t_{si} @ I_C/I_B = 5

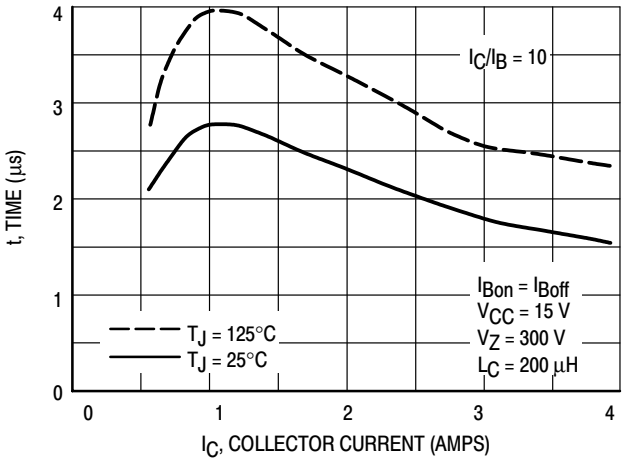


Figure 16. Inductive Storage Time, t_{si} @ I_C/I_B = 10

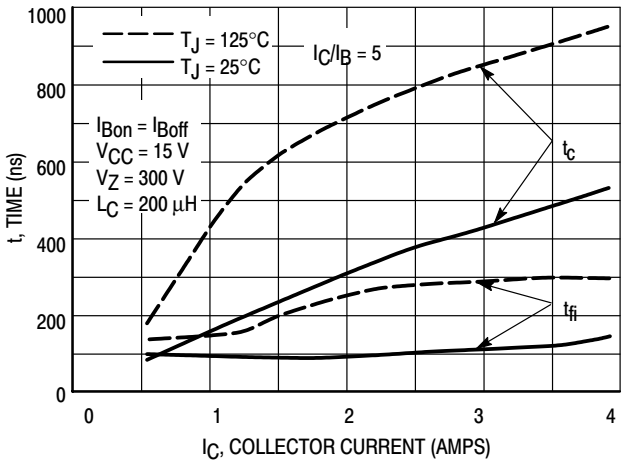


Figure 17. Inductive Switching Time, t_c and t_{fi} @ I_C/I_B = 5

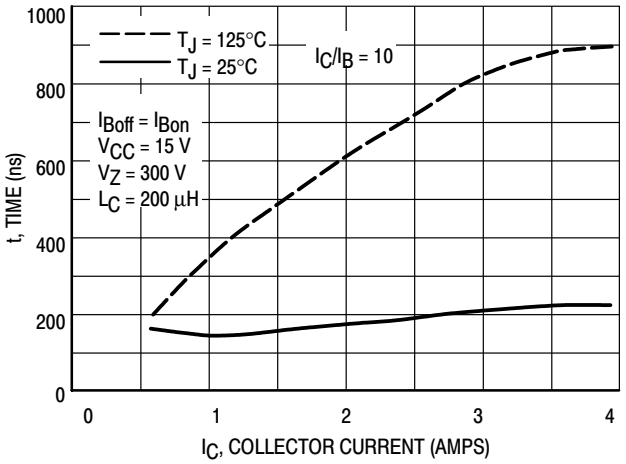


Figure 18. Inductive Switching Time, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

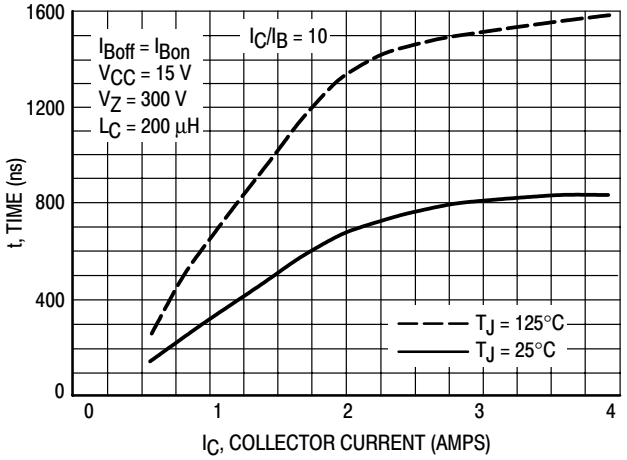


Figure 19. Inductive Switching, t_c @ I_C/I_B = 10

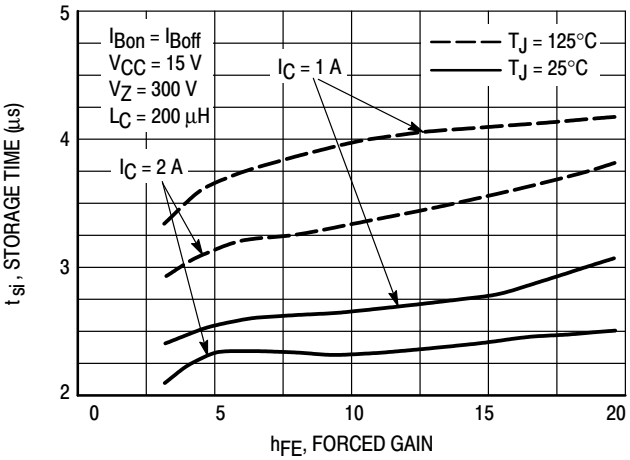


Figure 20. Inductive Storage Time

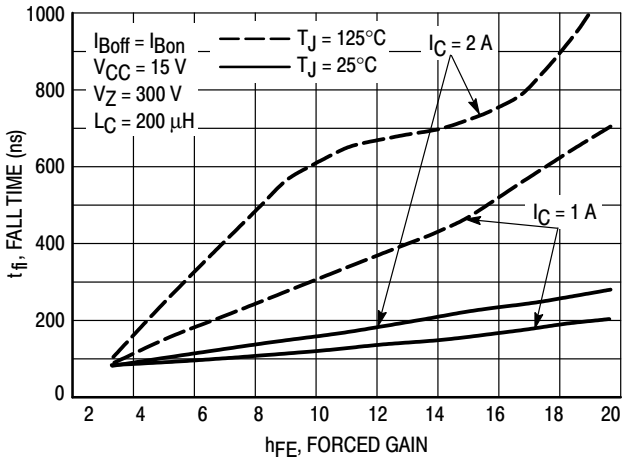


Figure 21. Inductive Fall Time

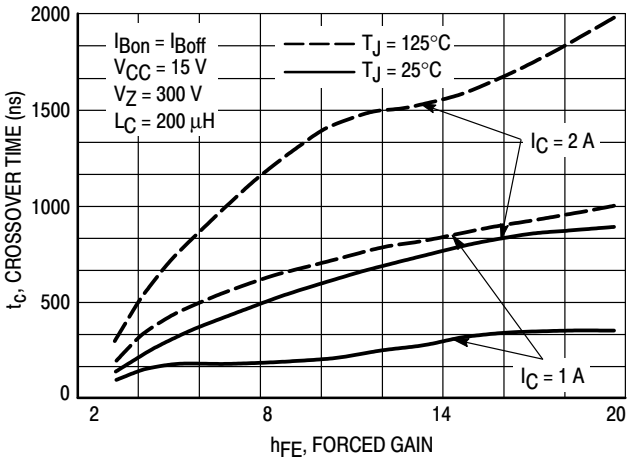


Figure 22. Inductive Crossover Time

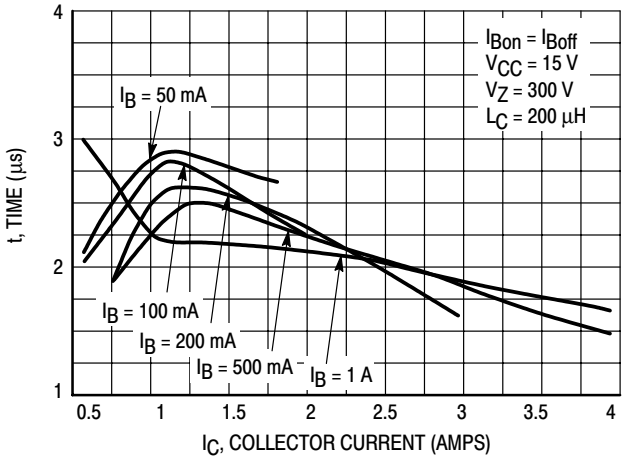


Figure 23. Inductive Storage Time, t_{si}

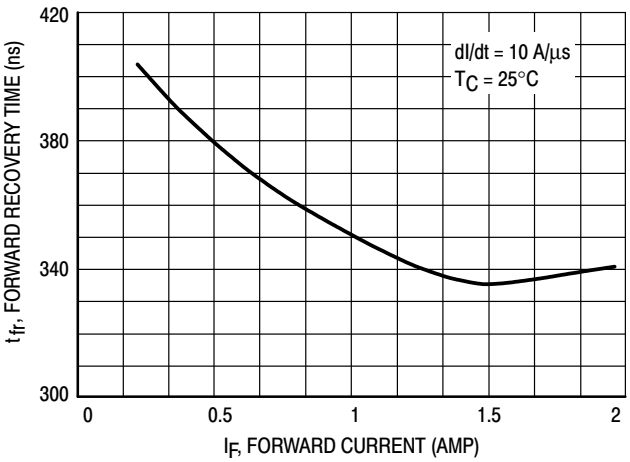


Figure 24. Forward Recovery Time, T_{FR}

TYPICAL SWITCHING CHARACTERISTICS

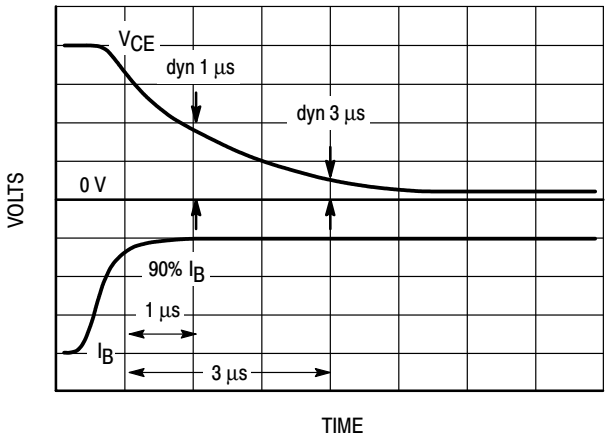


Figure 25. Dynamic Saturation Voltage Measurements

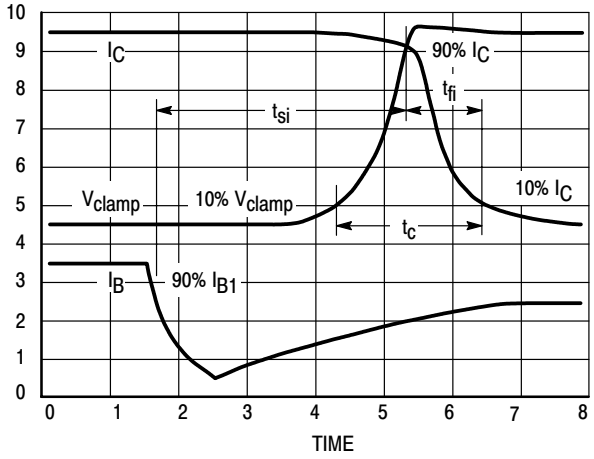


Figure 26. Inductive Switching Measurements

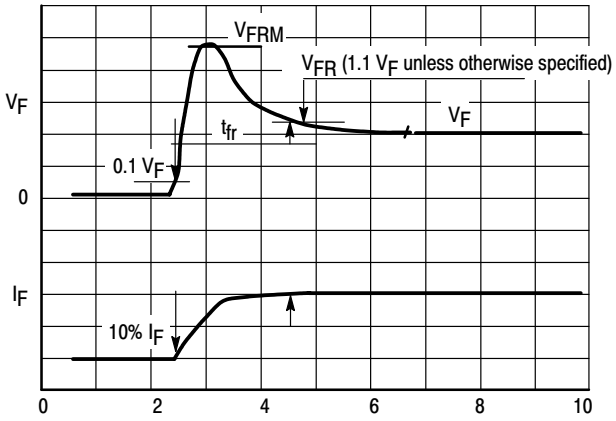
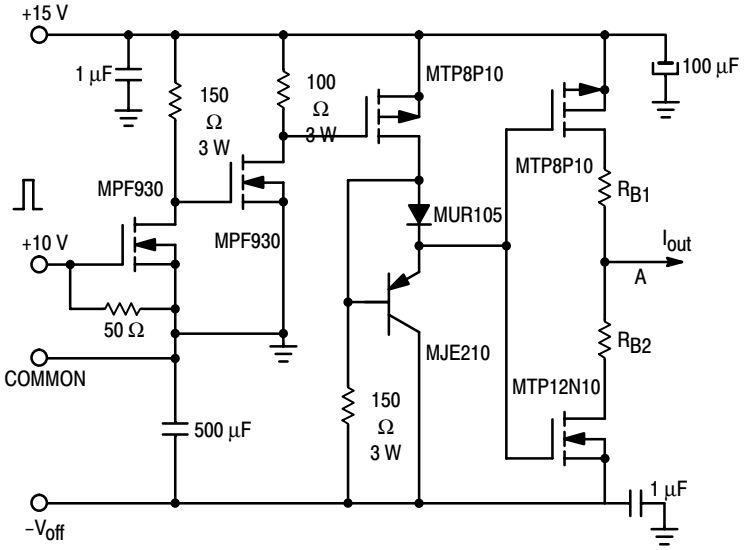
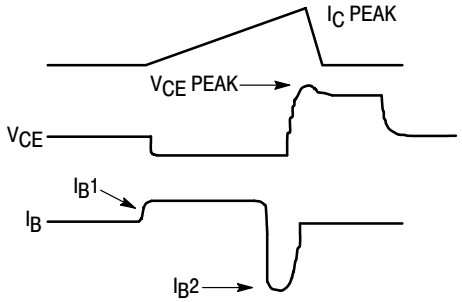


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	RB1 selected for desired Ib1	RB1 selected for desired Ib1

TYPICAL CHARACTERISTICS

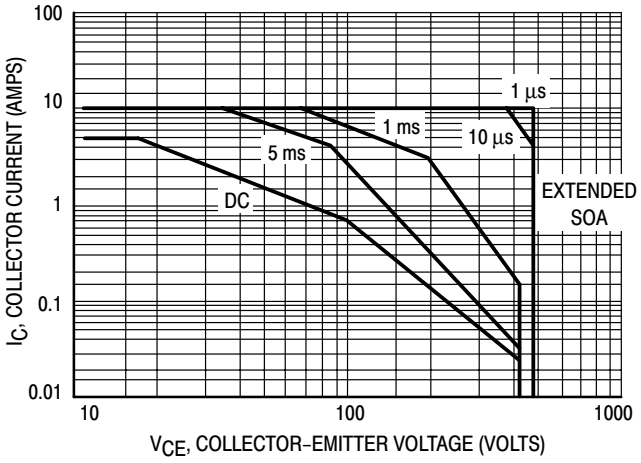


Figure 28. Forward Bias Safe Operating Area

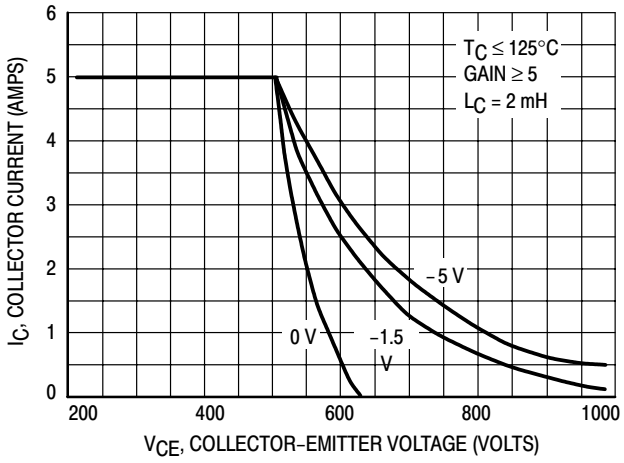


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

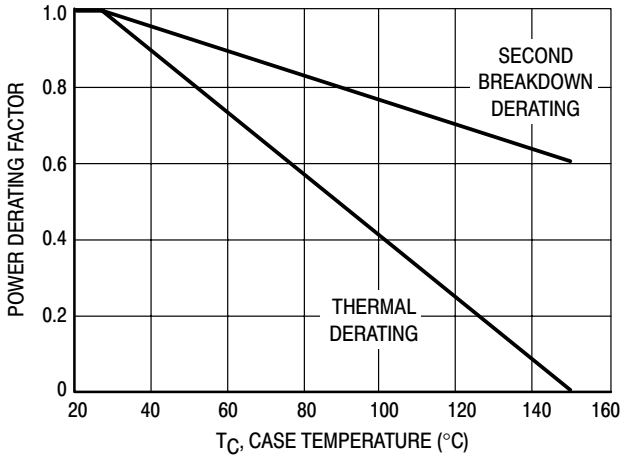


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

T_J(pk) may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse biased. The safe level is specified as a reverse−biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

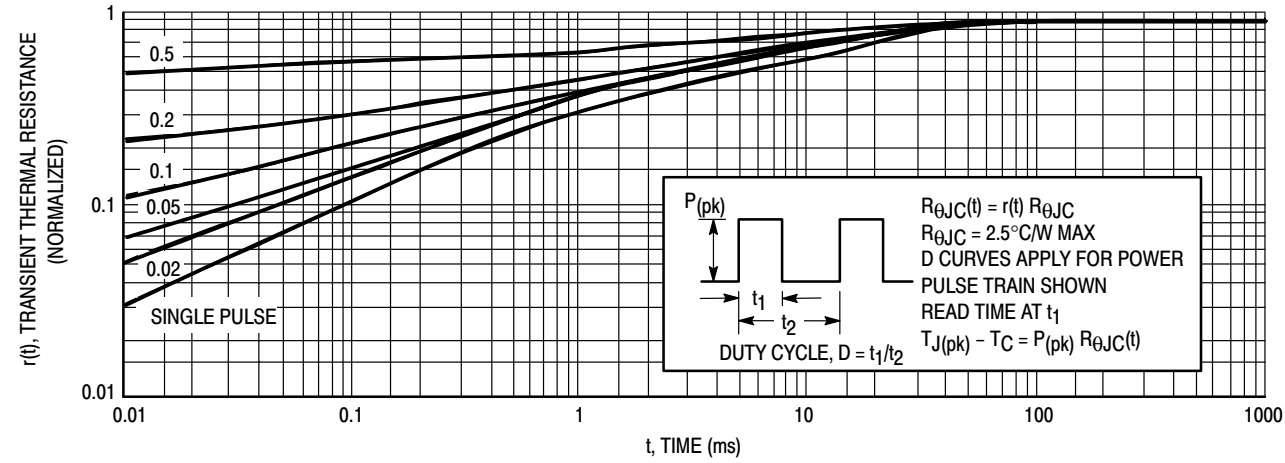


Figure 31. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004D2

MJE18004 *
MJF18004 *

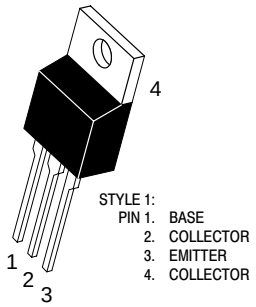
*ON Semiconductor Preferred Device

SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

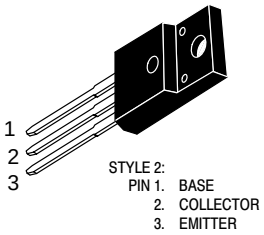
POWER TRANSISTOR
5.0 AMPERES
1000 VOLTS
35 and 75 WATTS

The MJE/MJF18004 have an applications specific state−of−the−art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. This high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Full Characterization at 125°C
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO−220 or Isolated TO−220
- MJF18004, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A−09
TO−220AB
MJE18004



CASE 221D−02
ISOLATED TO−220 TYPE
MJF18004

MAXIMUM RATINGS

Rating	Symbol	MJE18004	MJF18004	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter−Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	2.0 4.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. Test No. 2 Per Fig. 22b < 30%, T_A = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	35 0.28	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18004	MJF18004	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 6
Publication Order Number:
MJE18004/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)				$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)				I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	(T_C = 25°C)			I_{CES}	—	—	100	μAdc
	(T_C = 125°C)				—	—	500	
(V_{CE} = 800 V, V_{EB} = 0)	(T_C = 125°C)				—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)				I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS								
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)				$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)					—	0.92	1.25	
Collector−Emitter Saturation Voltage				$V_{CE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)					—	0.25	0.5	
	(T_C = 125°C)				—	0.29	0.6	
(I_C = 2.0 Adc, I_B = 0.4 Adc)					—	0.3	0.45	
	(T_C = 125°C)				—	0.36	0.8	
(I_C = 2.5 Adc, I_B = 0.5 Adc)					—	0.5	0.75	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 2.5 Vdc)				h_{FE}	12	21	—	—
	(T_C = 125°C)				—	20	—	
(I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)					14	—	34	
	(T_C = 125°C)				—	32	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)					6.0	11	—	
	(T_C = 125°C)				—	7.5	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)					10	22	—	
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	50	65	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	800	1000	pF
Dynamic Saturation Voltage:	(I_C = 1.0 Adc	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	—	6.8	—	Vdc
Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	I_{B1} = 100 mAdc V_{CC} = 300 V)				—	14	—	
		3.0 μs	(T_C = 125°C)		—	2.4	—	
					—	5.6	—	
	(I_C = 2.0 Adc	1.0 μs	(T_C = 125°C)		—	11.3	—	
	I_{B1} = 400 mAdc V_{CC} = 300 V)				—	15.5	—	
		3.0 μs	(T_C = 125°C)		—	1.3	—	
					—	6.1	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%. (continued)

(2) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)						
Turn−On Time	(I_C = 1.0 Adc, I_{B1} = 0.1 Adc, I_{B2} = 0.5 Adc, V_{CC} = 300 V)	t_{on}	— —	210 180	300 —	ns
Turn−Off Time	(T_C = 25°C) (T_C = 125°C)	t_{off}	— —	1.0 1.3	1.7 —	μs
Turn−On Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc, I_{B1} = 1.0 Adc, V_{CC} = 300 V) (T_C = 25°C) (T_C = 125°C)	t_{on}	— —	75 90	110 —	ns
Turn−Off Time	(T_C = 25°C) (T_C = 125°C)	t_{off}	— —	1.5 1.8	2.5 —	μs
Turn−On Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, I_{B2} = 0.5 Adc, V_{CC} = 250 V) (T_C = 25°C) (T_C = 125°C)	t_{on}	— —	450 900	800 1400	ns
Storage Time	(T_C = 25°C) (T_C = 125°C)	t_s	— —	2.0 2.2	3.0 3.5	μs
Fall Time	(T_C = 25°C) (T_C = 125°C)	t_f	— —	275 500	400 800	ns
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)						
Fall Time	(I_C = 1.0 Adc, I_{B1} = 0.1 Adc, I_{B2} = 0.5 Adc) (T_C = 25°C) (T_C = 125°C)	t_{fi}	— —	100 100	150 —	ns
Storage Time	(T_C = 25°C) (T_C = 125°C)	t_{si}	— —	1.1 1.4	1.7 —	μs
Crossover Time	(T_C = 25°C) (T_C = 125°C)	t_c	— —	180 160	250 —	ns
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc, I_{B2} = 1.0 Adc) (T_C = 25°C) (T_C = 125°C)	t_{fi}	— —	90 150	175 —	ns
Storage Time	(T_C = 25°C) (T_C = 125°C)	t_{si}	— —	1.7 2.2	2.5 —	μs
Crossover Time	(T_C = 25°C) (T_C = 125°C)	t_c	— —	180 250	300 —	ns
Fall Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, I_{B2} = 0.5 Adc, $V_{BE(off)}$ = −5.0 Vdc) (T_C = 25°C) (T_C = 125°C)	t_{fi}	— —	70 100	130 175	ns
Storage Time	(T_C = 25°C) (T_C = 125°C)	t_{si}	— —	0.75 1.0	1.0 1.3	μs
Crossover Time	(T_C = 25°C) (T_C = 125°C)	t_c	— —	250 250	350 500	ns

TYPICAL STATIC CHARACTERISTICS

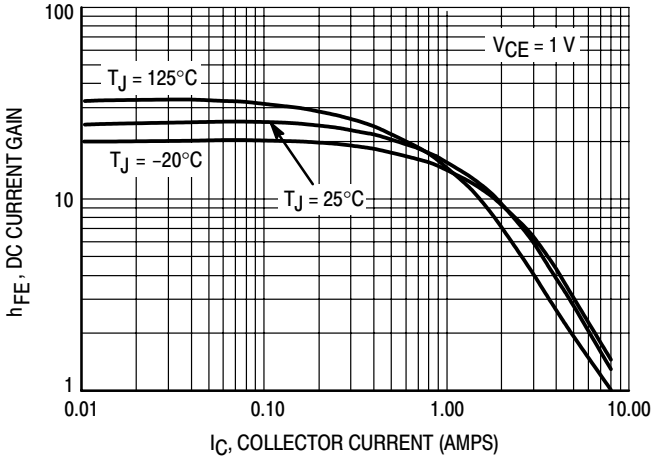


Figure 1. DC Current Gain @ 1 Volt

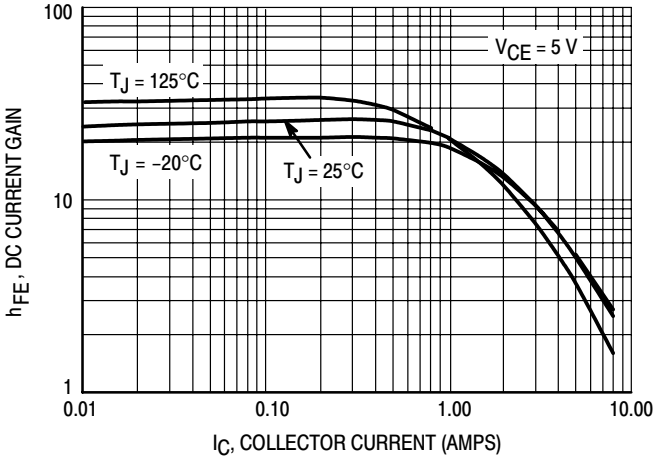


Figure 2. DC Current Gain @ 5 Volts

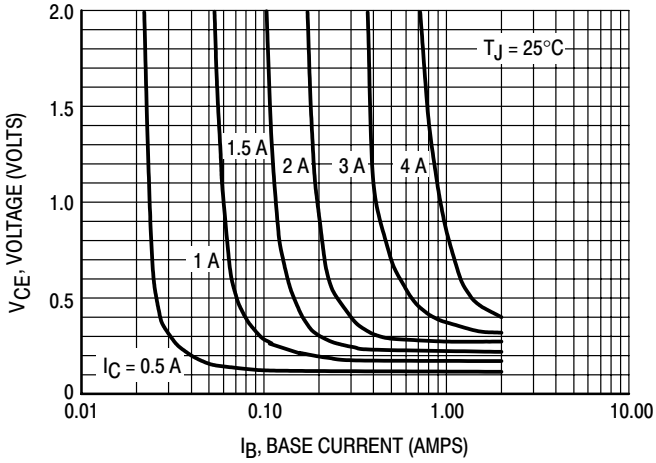


Figure 3. Collector Saturation Region

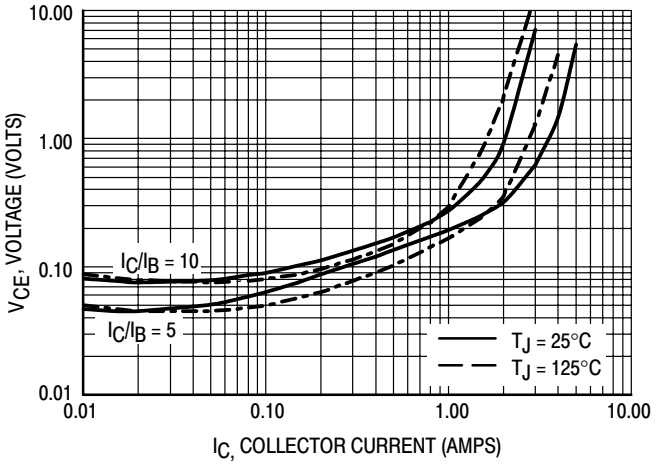


Figure 4. Collector−Emitter Saturation Voltage

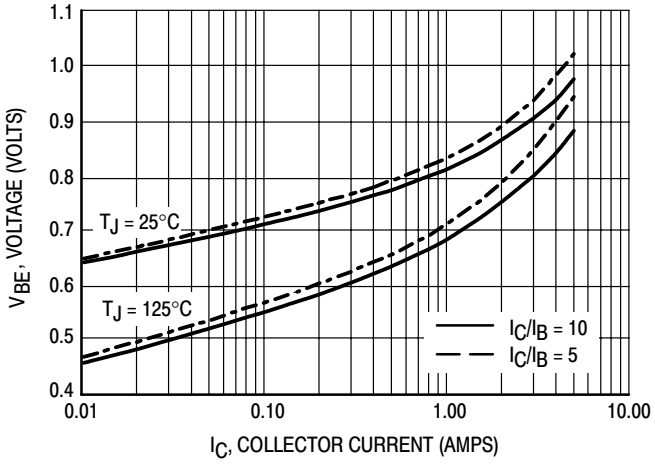


Figure 5. Base−Emitter Saturation Region

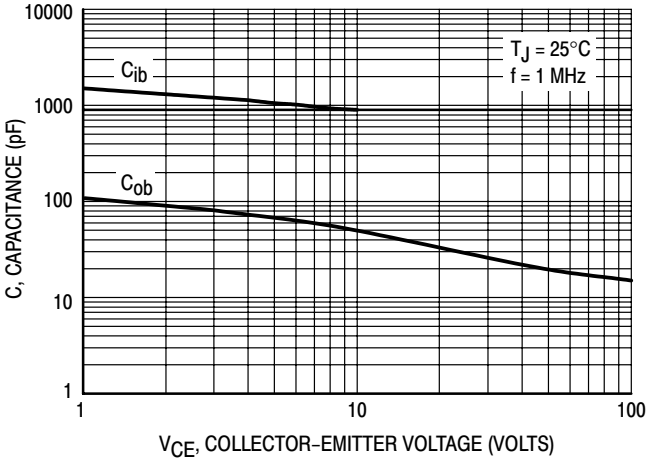


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

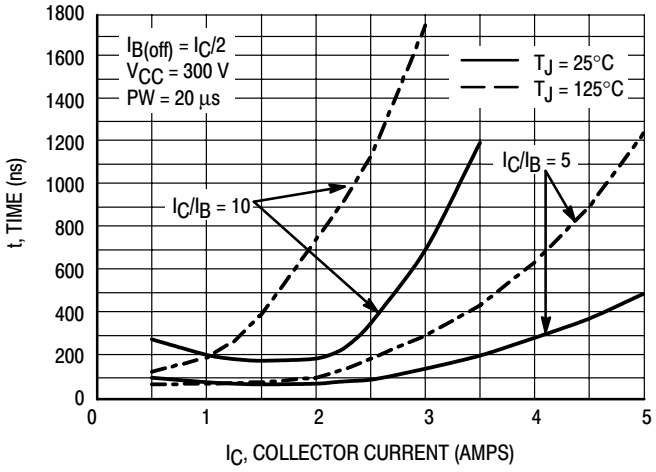


Figure 7. Resistive Switching, t_{on}

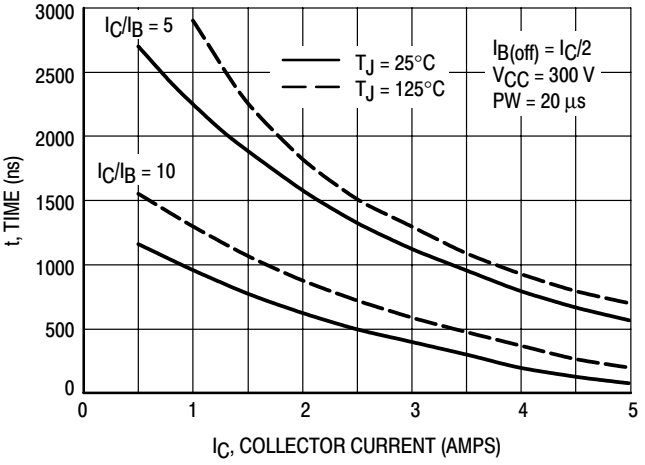


Figure 8. Resistive Switching, t_{off}

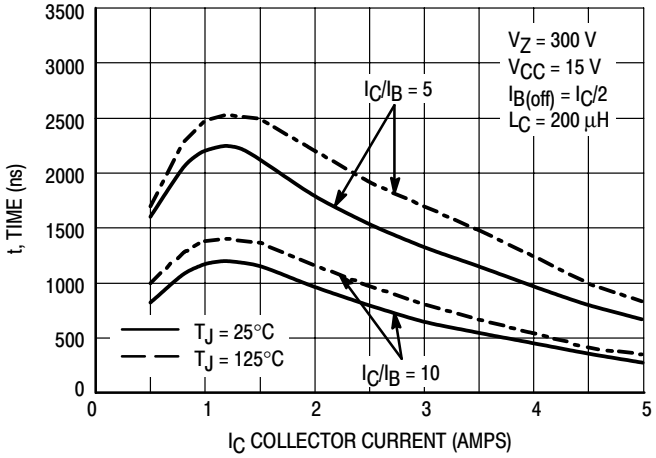


Figure 9. Inductive Storage Time, t_{si}

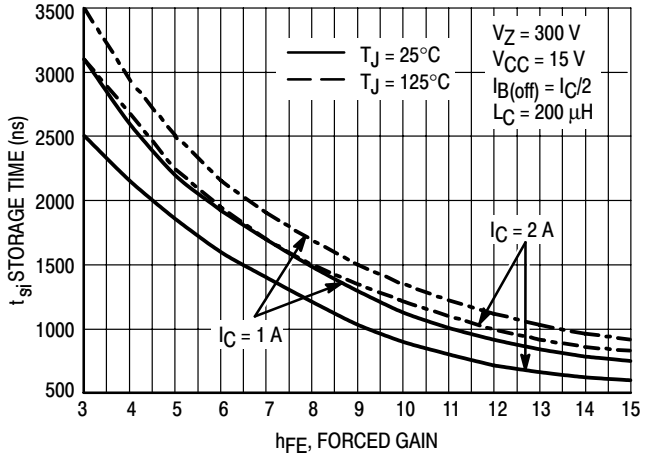


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

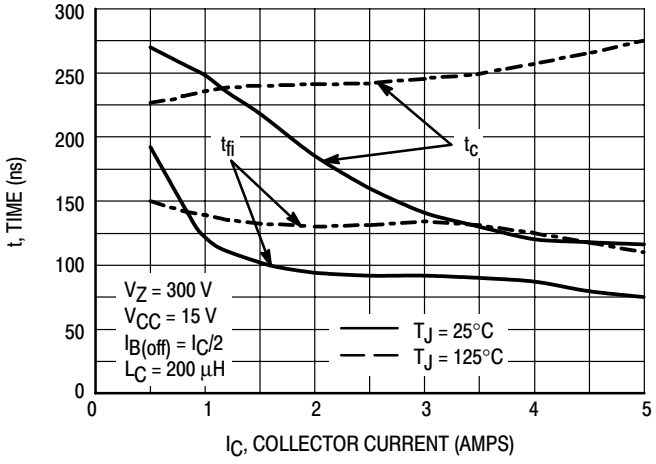


Figure 11. Inductive Switching, t_c and t_{fi}, $I_C/I_B = 5$

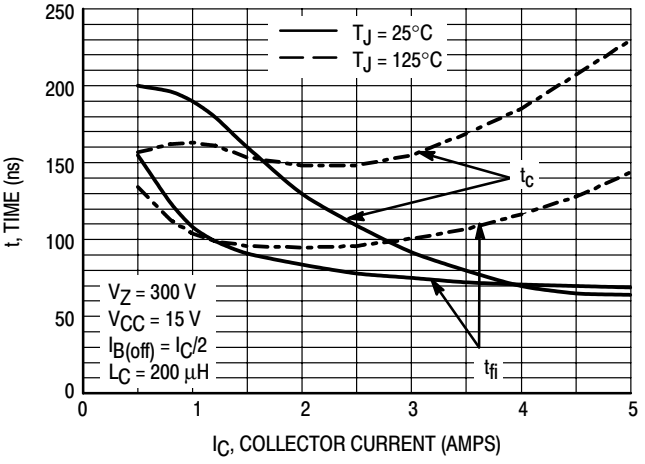


Figure 12. Inductive Switching, t_c and t_{fi}, $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

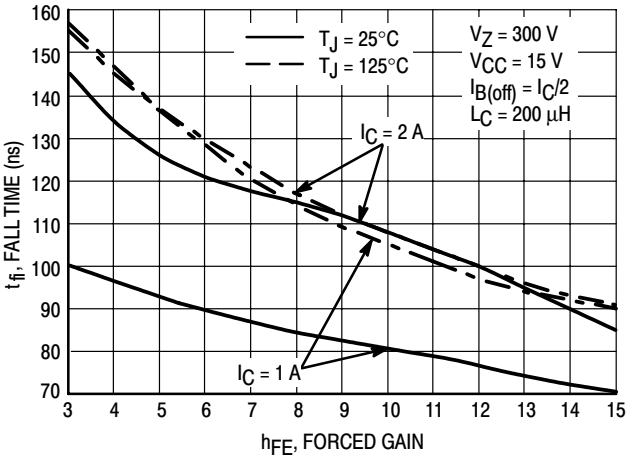


Figure 13. Inductive Fall Time

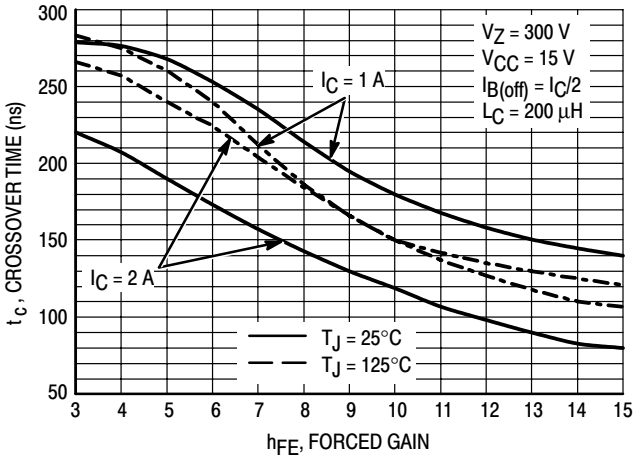


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

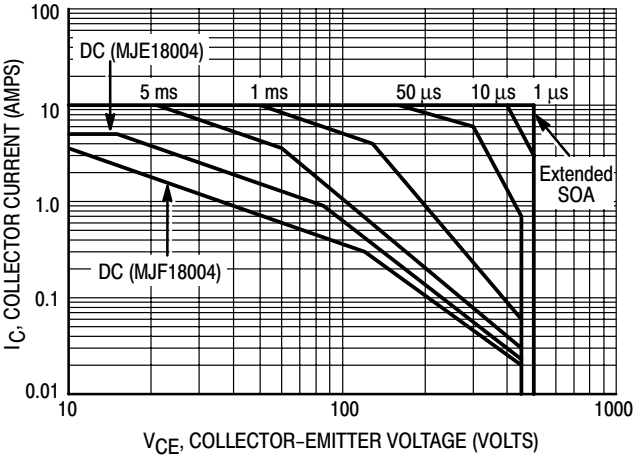


Figure 15. Forward Bias Safe Operating Area

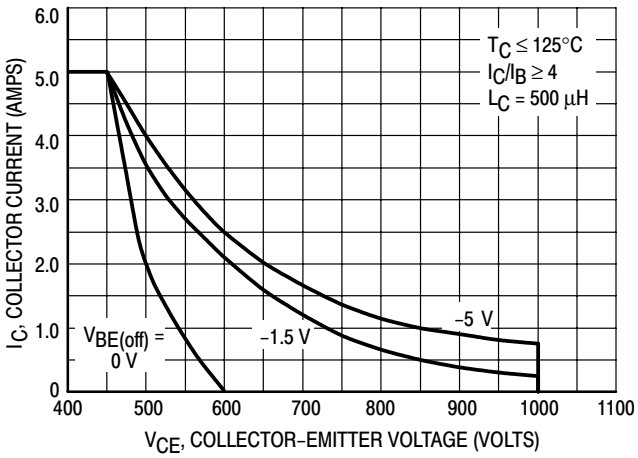


Figure 16. Reverse Bias Safe Operating Area

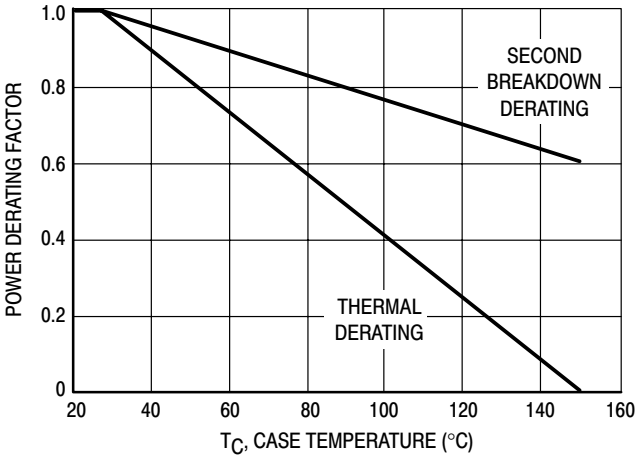


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_J(pk)$ may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse biased. The safe level is specified as a reverse−biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

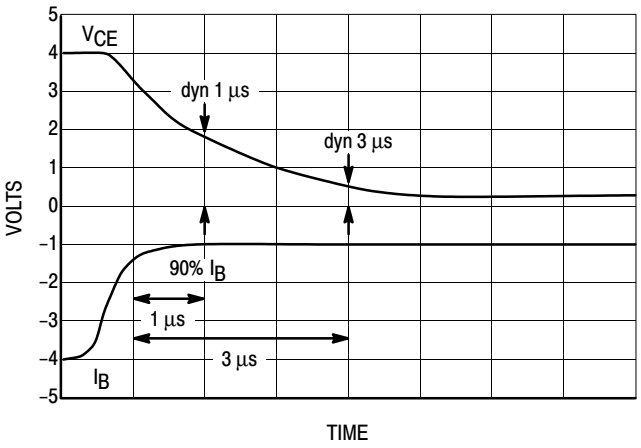


Figure 18. Dynamic Saturation Voltage Measurements

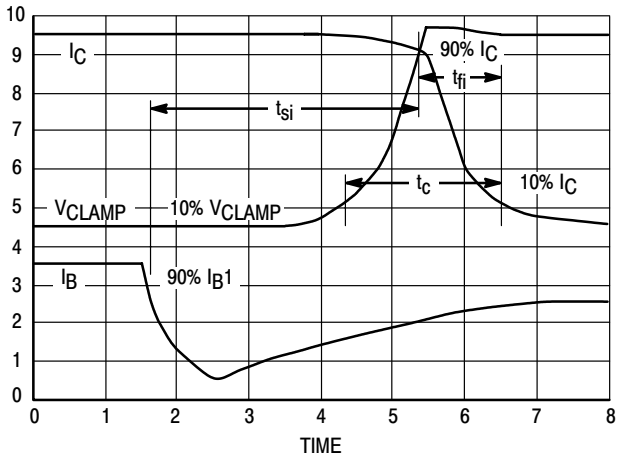
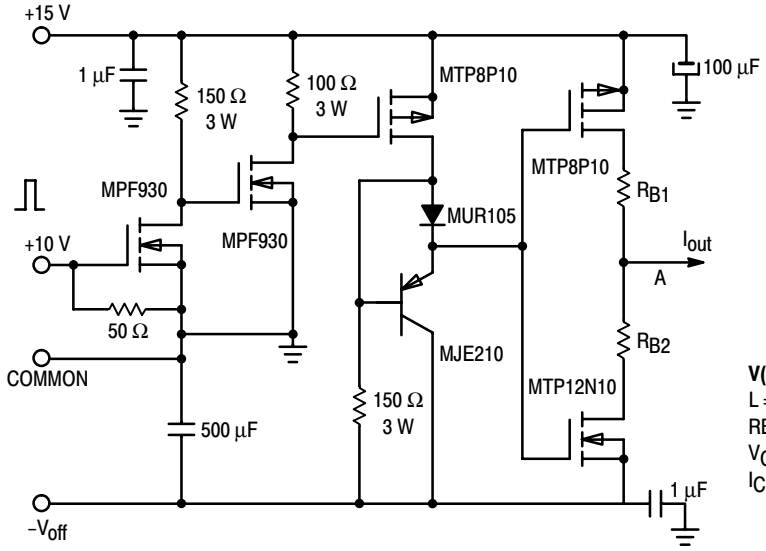
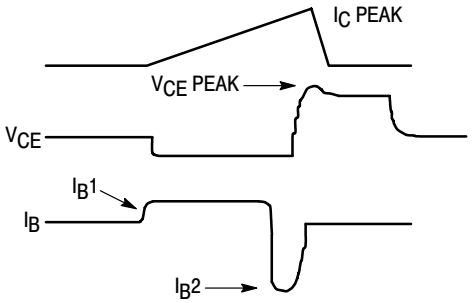


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

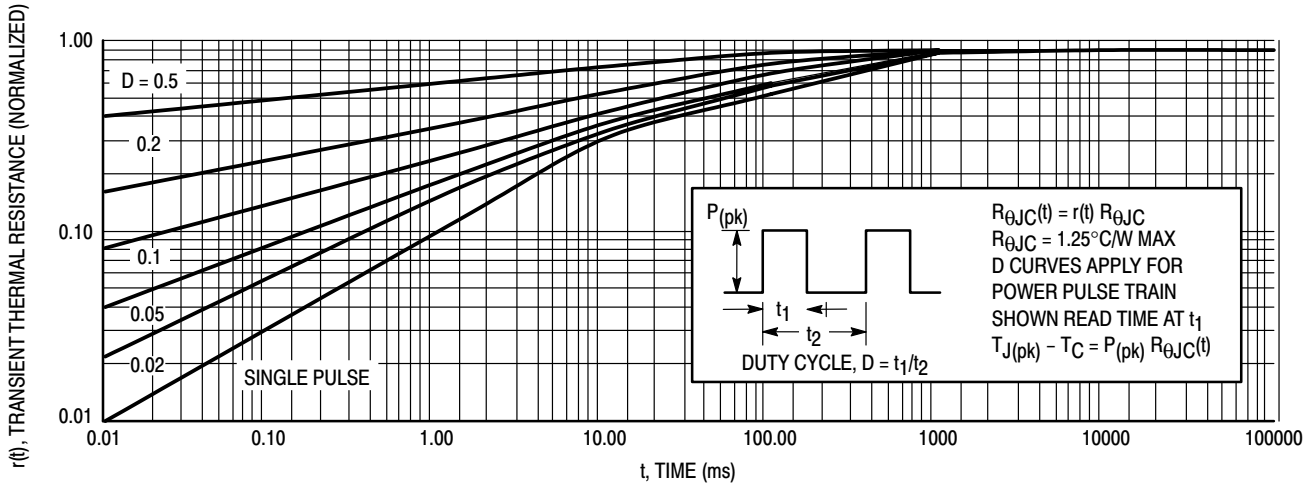


Figure 20. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004

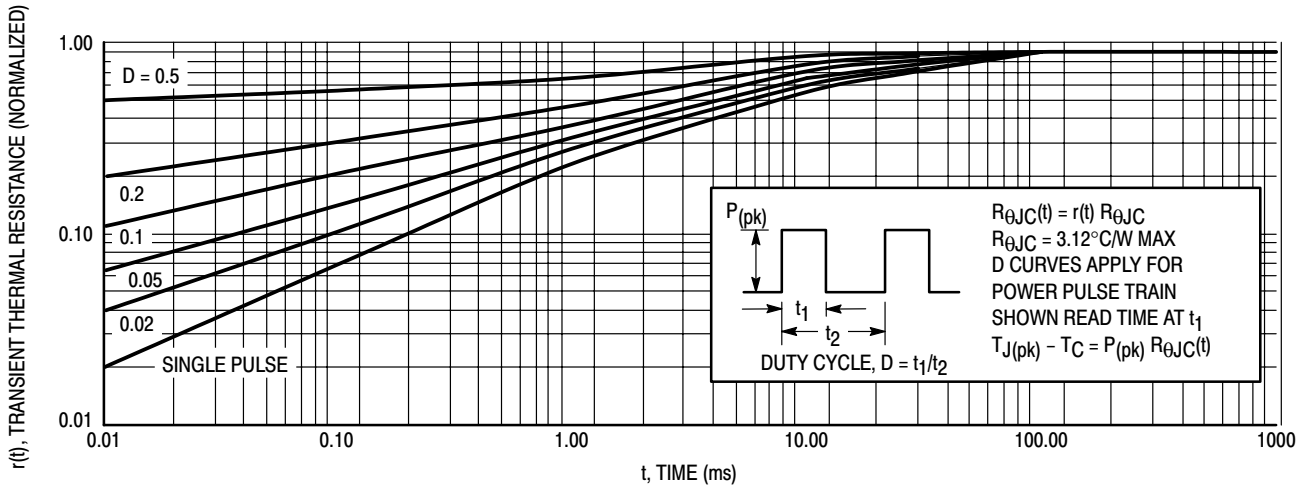


Figure 21. Typical Thermal Response for MJF18004

TEST CONDITIONS FOR ISOLATION TESTS*

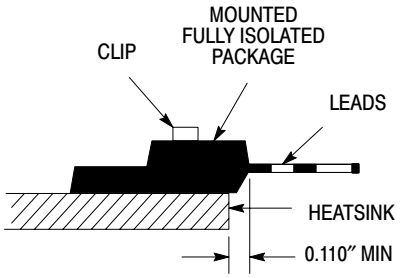


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

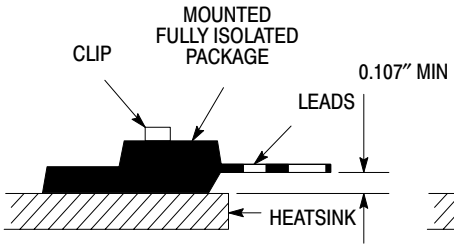


Figure 22b. Clip Mounting Position for Isolation Test Number 2

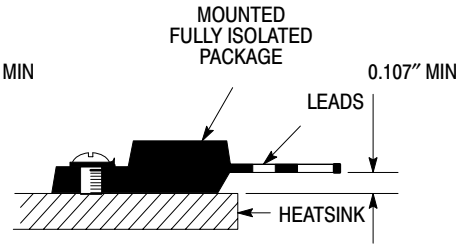


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

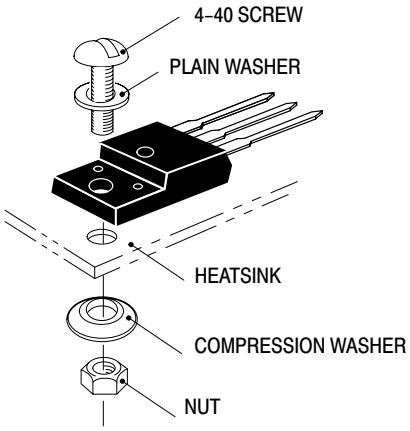


Figure 23a. Screw−Mounted

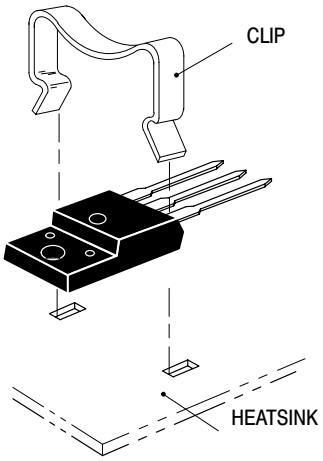


Figure 23b. Clip−Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE18006*

*ON Semiconductor Preferred Device

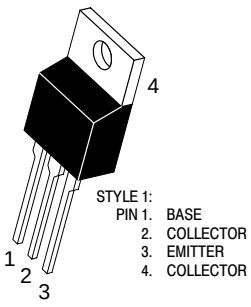
SWITCHMODE™

NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE18006 has an applications specific state−of−the−art die designed for use in 220 V line−operated SWITCHMODE Power supplies and electronic light ballasts. This high voltage/high speed transistor offers the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot−to−Lot
- Standard TO−220

POWER TRANSISTOR
6.0 AMPERES
1000 VOLTS
100 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	MJE18006	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	6.0 15	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0	Adc
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18006	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 5
Publication Order Number:
MJE18006/D

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base−Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)				$V_{BE(sat)}$	— —	0.83 0.94	1.2 1.3	Vdc
Collector−Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)			(T_C = 125°C) (T_C = 125°C)	$V_{CE(sat)}$	— — — —	0.25 0.27 0.35 0.4	0.6 0.65 0.7 0.8	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.3 Adc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)			(T_C = 125°C) (T_C = 125°C) (T_C = 25 to 125°C)	h_{FE}	14 — 6.0 5.0 11 10	— 32 10 8.0 17 22	34 — — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	75	120	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.3 Adc I_{B1} = 130 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	5.5 12	— —	Volts
		3.0 μs	(T_C = 125°C)		— —	3.0 7.0	— —	
	(I_C = 3.0 Adc I_{B1} = 0.6 Adc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	9.5 14.5	— —	
		3.0 μs	(T_C = 125°C)		— —	2.0 7.5	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)								
Turn−On Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	90 100	180 —	ns
Turn−Off Time			(T_C = 125°C)	t_{off}	— —	1.7 2.1	2.5 —	μs
Turn−On Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	200 130	300 —	ns
Turn−Off Time			(T_C = 125°C)	t_{off}	— —	1.2 1.5	2.5 —	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	(I_C = 1.5 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc)		(T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.5 1.9	2.5 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	220 230	350 —	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)		(T_C = 125°C)	t_{fi}	— —	85 120	150 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	2.15 2.75	3.2 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	200 310	300 —	ns

TYPICAL STATIC CHARACTERISTICS

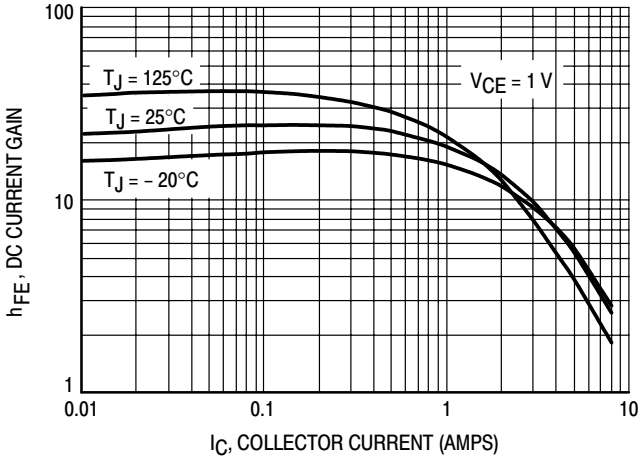


Figure 1. DC Current Gain @ 1 Volt

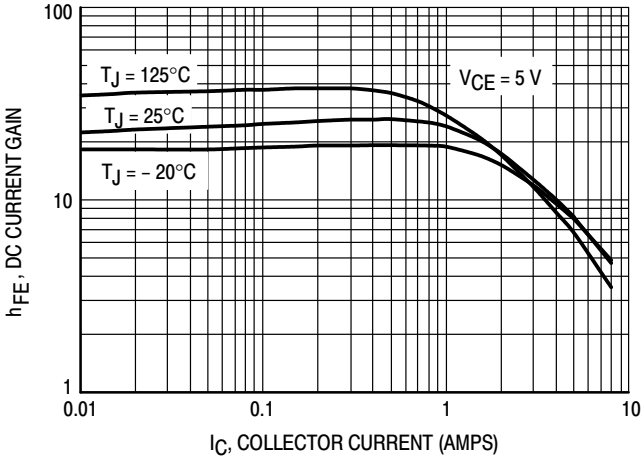


Figure 2. DC Current Gain @ 5 Volts

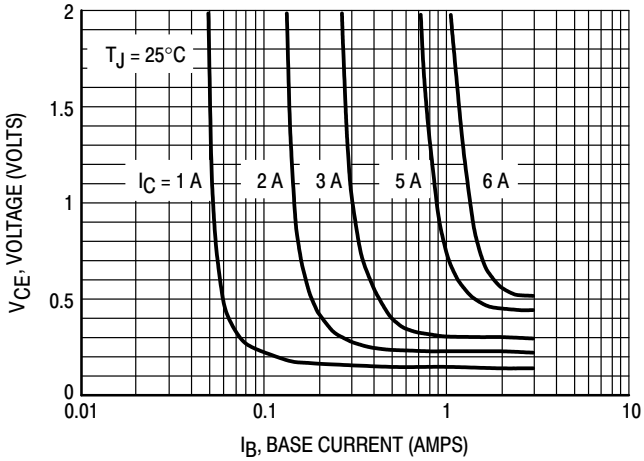


Figure 3. Collector Saturation Region

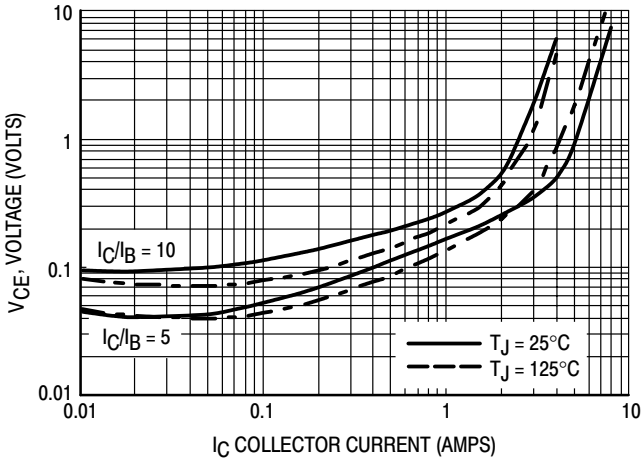


Figure 4. Collector−Emitter Saturation Voltage

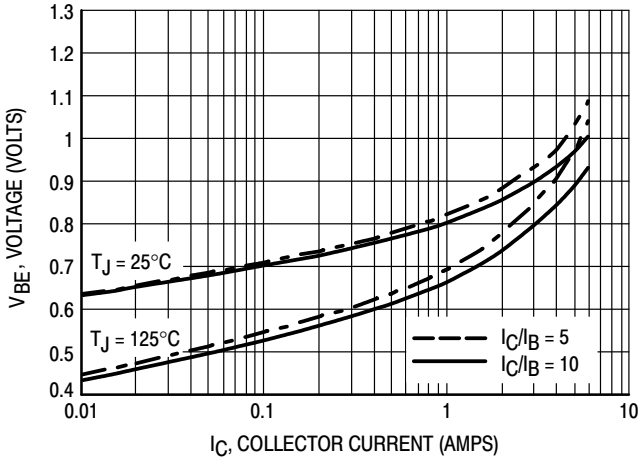


Figure 5. Base−Emitter Saturation Region

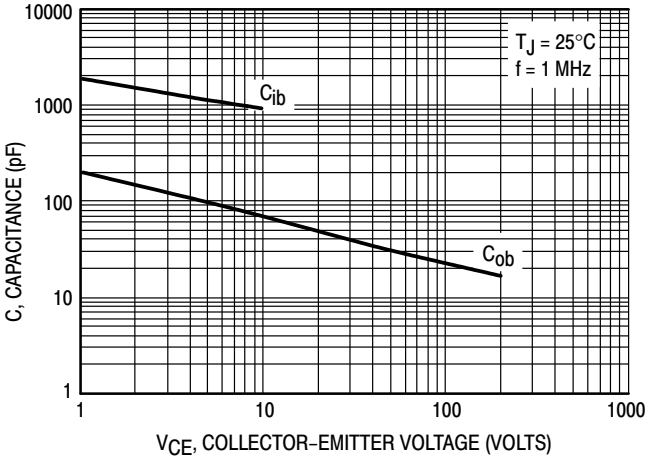


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

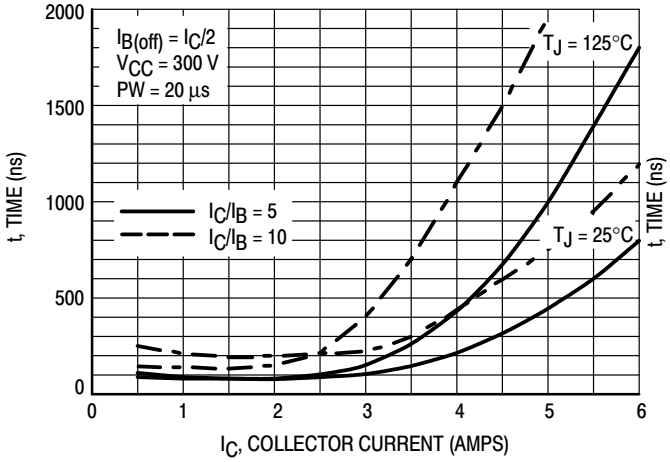


Figure 7. Resistive Switching, t_{on}

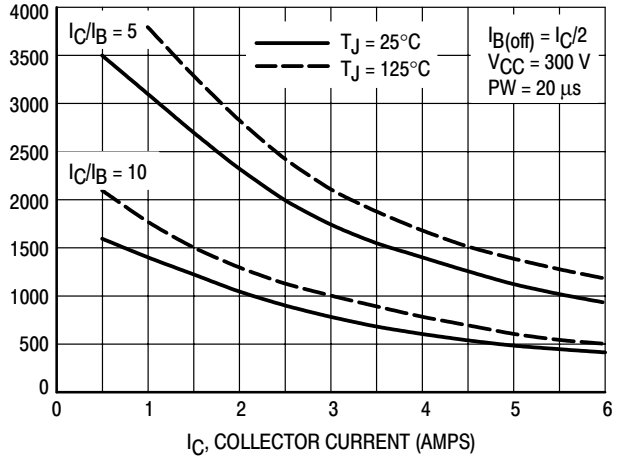


Figure 8. Resistive Switching, t_{off}

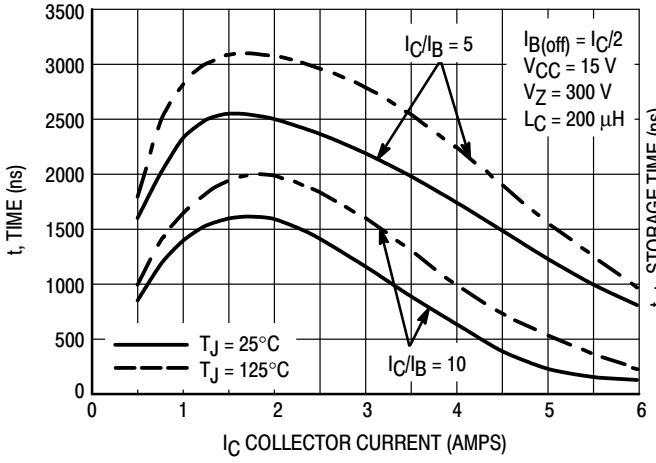


Figure 9. Inductive Storage Time, t_{si}

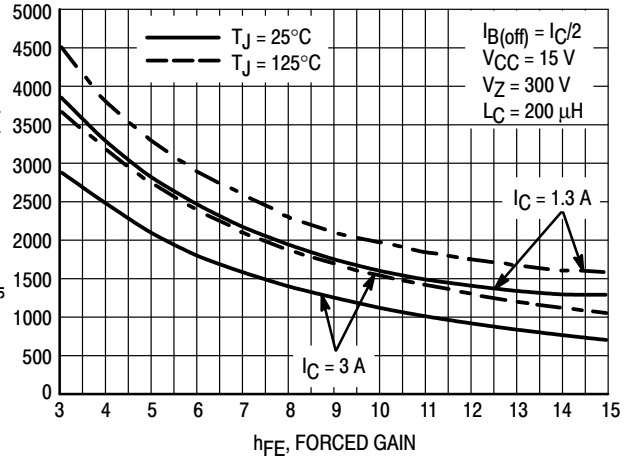


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

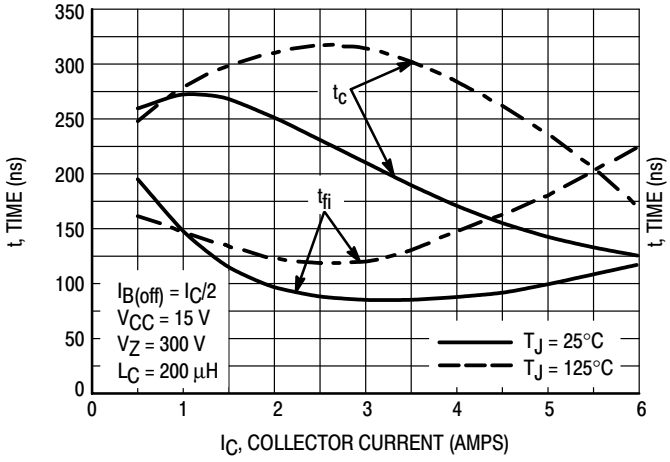


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

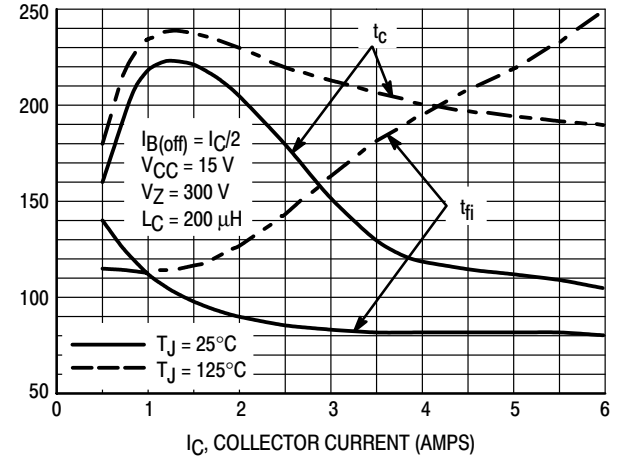


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

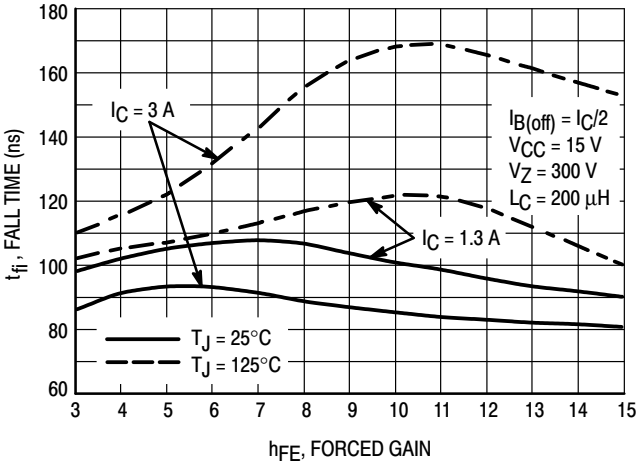


Figure 13. Inductive Fall Time

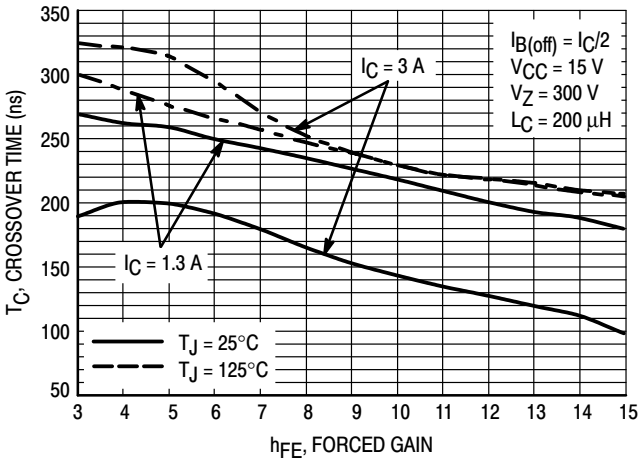


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

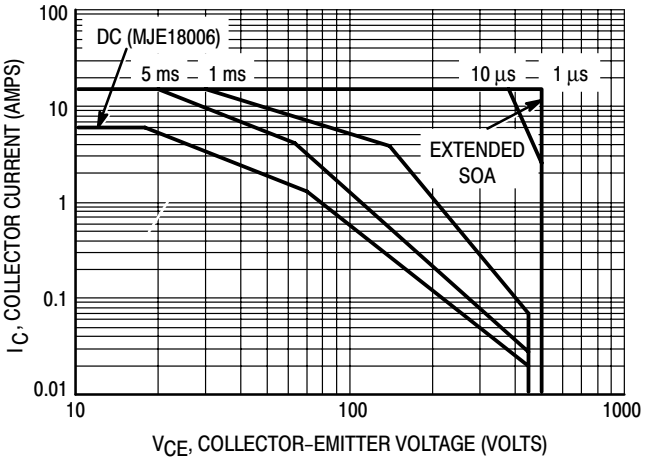


Figure 15. Forward Bias Safe Operating Area

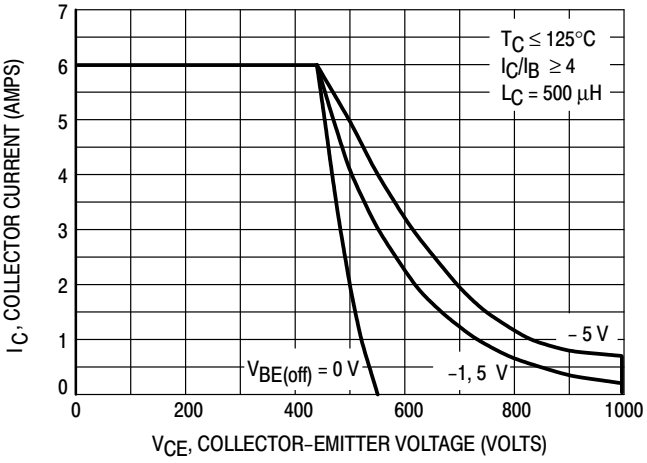


Figure 16. Reverse Bias Switching Safe Operating Area

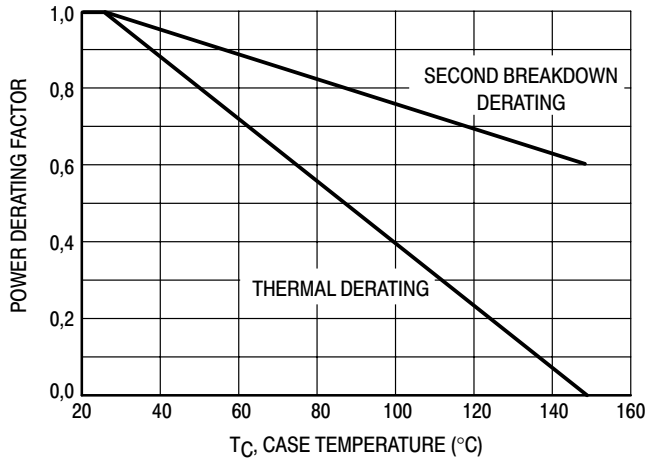


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

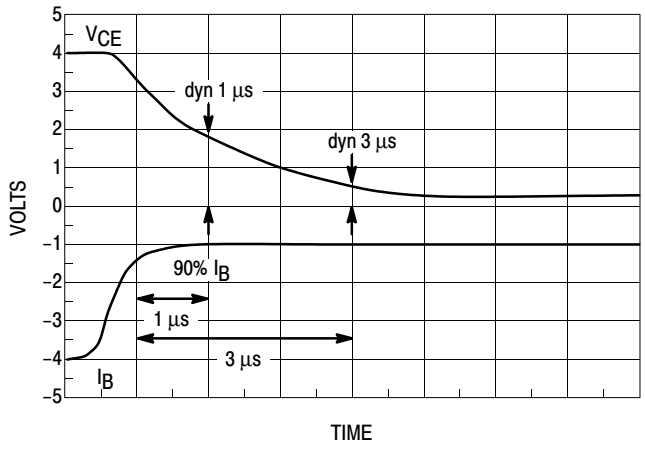


Figure 18. Dynamic Saturation Voltage Measurements

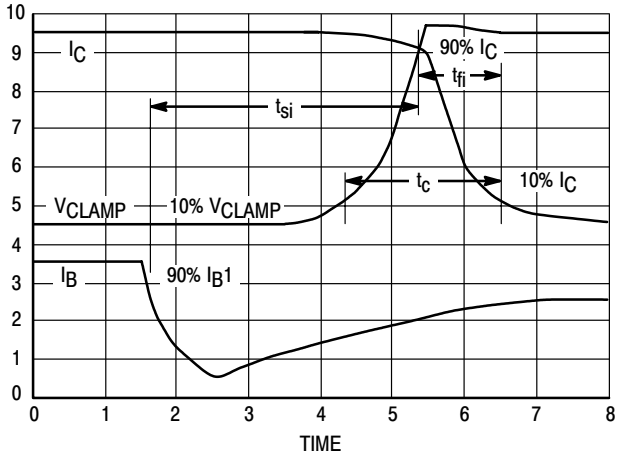
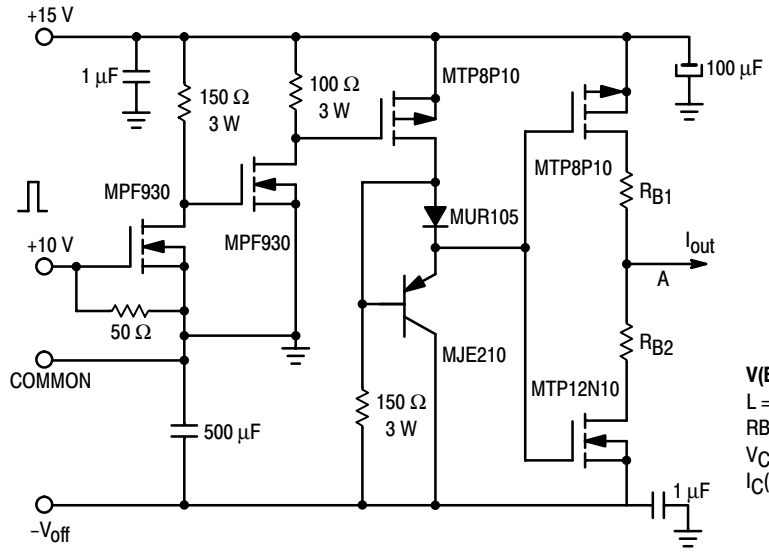
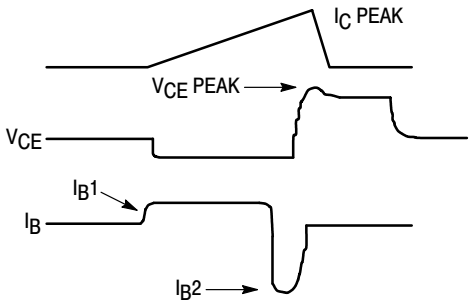


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
$I_{C(pk)}$ = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

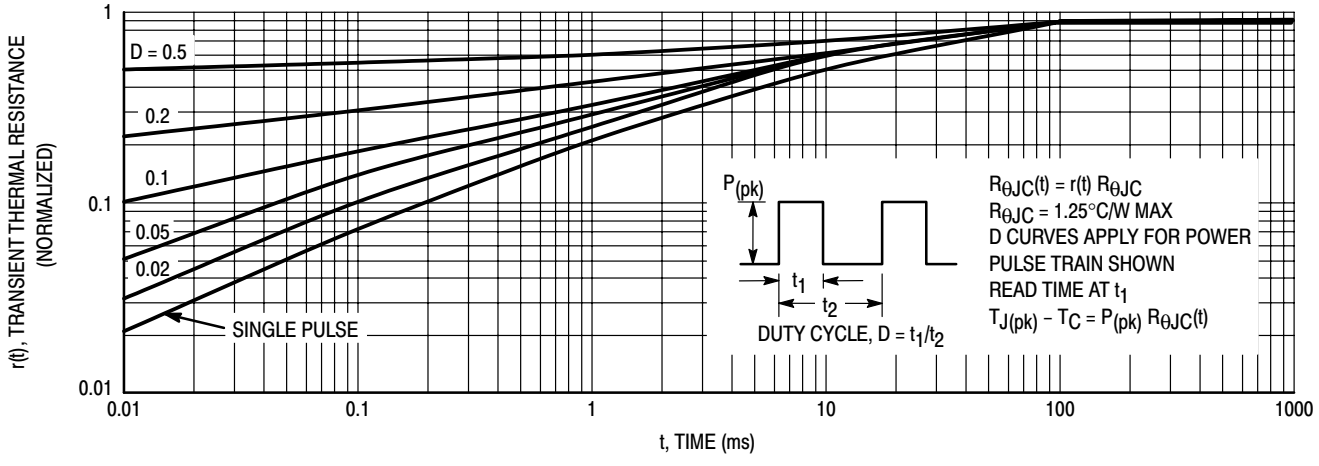


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18006

MJE18008 *
MJF18008 *

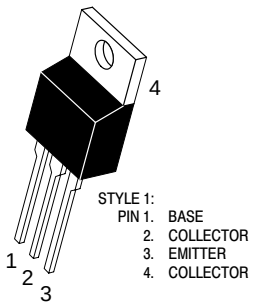
*ON Semiconductor Preferred Device

SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
8.0 AMPERES
1000 VOLTS
45 and 125 WATTS

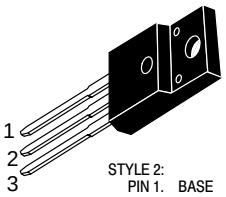
The MJE/MJF18008 have an applications specific state−of−the−art die designed for use in 220 V line−operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - High and Flat DC Current Gain h_{FE}
  - Fast Switching
  - No Coil Required in Base Circuit for Turn−Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot−to−Lot
- Two Package Choices: Standard TO−220 or Isolated TO−220
- MJF18008, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A−09
TO−220AB
MJE18008



STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 221D−02
ISOLATED TO−220 TYPE
UL RECOGNIZED
MJF18008

MAXIMUM RATINGS

Rating	Symbol	MJE18008	MJF18008	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter−Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec,] R.H. < 30%, Test No. 1 Per Fig. 22b T_C = 25°C) Test No. 1 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T^C = 25°C) Derate above 25°C	P_D	125 1.0	45 0.36	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18008	MJF18008	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	2.78 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
ON CHARACTERISTICS					
Base−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.92	1.25	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)		—	0.3	0.6	
(T_C = 125°C)		—	0.3	0.65	
(I_C = 4.5 Adc, I_B = 0.9 Adc)		—	0.35	0.7	
(T_C = 125°C)		—	0.4	0.8	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	—	34	—
(T_C = 125°C)		—	28	—	
(I_C = 4.5 Adc, V_{CE} = 1.0 Vdc)		6.0	9.0	—	
(T_C = 125°C)		5.0	8.0	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		11	15	—	
(T_C = 125°C)		11	16	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	20	—	

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(2) Proper strike and creepage distance must be provided.

(continued)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	100	150	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 2.0 Adc I_{B1} = 200 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	5.5 11.5	— —	Vdc
		3.0 μs	(T_C = 125°C)		— —	3.5 6.5	— —	
	(I_C = 5.0 Adc I_{B1} = 1.0 Adc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	11.5 14.5	— —	
		3.0 μs	(T_C = 125°C)		— —	2.4 9.0	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)								
Turn−On Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	200 190	300 —	ns
Turn−Off Time			(T_C = 125°C)	t_{off}	— —	1.2 1.5	2.5 —	μs
Turn−On Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	100 250	180 —	ns
Turn−Off Time			(T_C = 125°C)	t_{off}	— —	1.6 2.0	2.5 —	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc)		(T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.5 1.9	2.75 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	250 230	350 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc)		(T_C = 125°C)	t_{fi}	— —	85 135	150 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	2.0 2.6	3.2 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	210 250	300 —	ns

TYPICAL STATIC CHARACTERISTICS

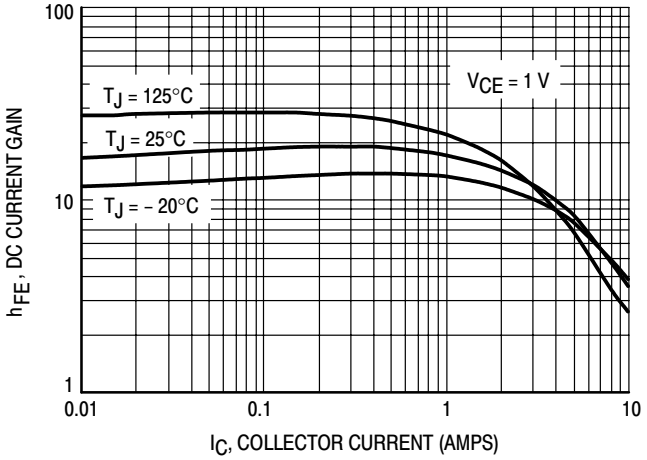


Figure 21. DC Current Gain @ 1 Volt

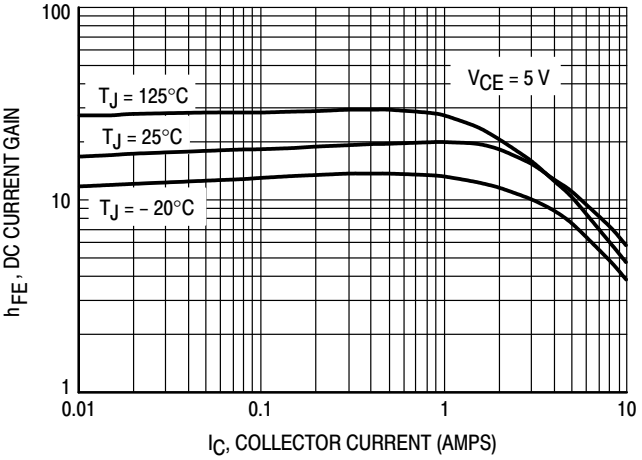


Figure 22. DC Current Gain @ 5 Volts

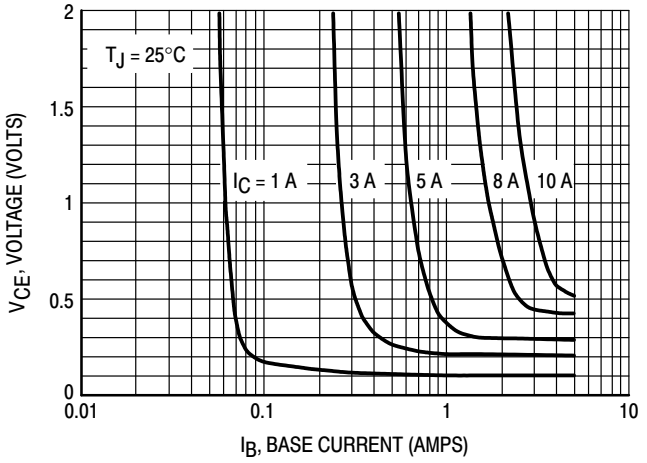


Figure 23. Collector Saturation Region

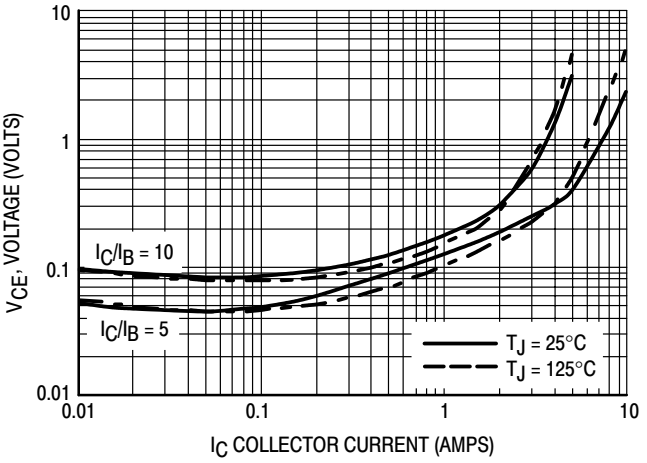


Figure 24. Collector−Emitter Saturation Voltage

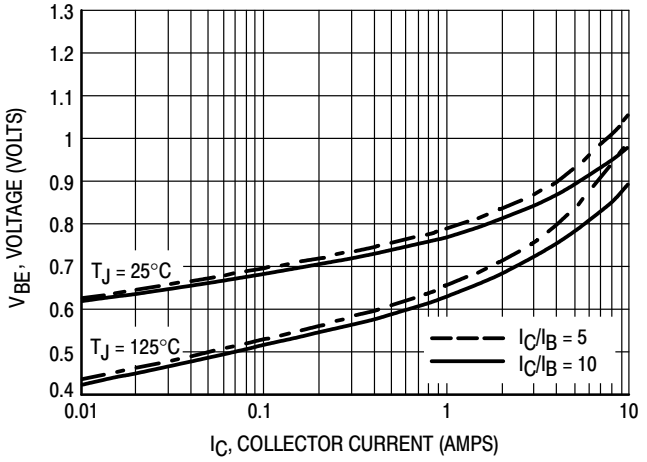


Figure 25. Base−Emitter Saturation Region

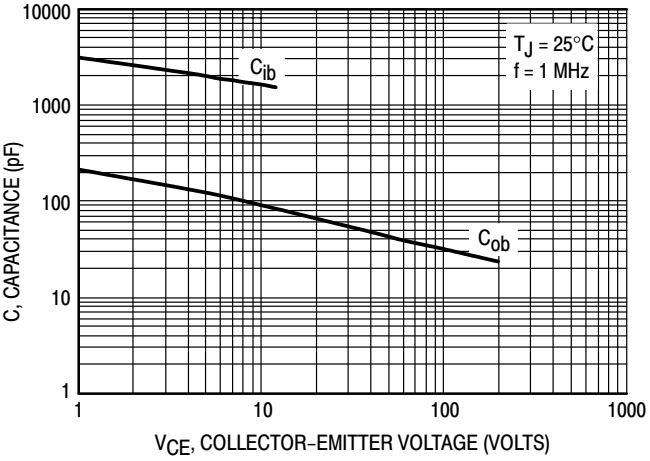


Figure 26. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

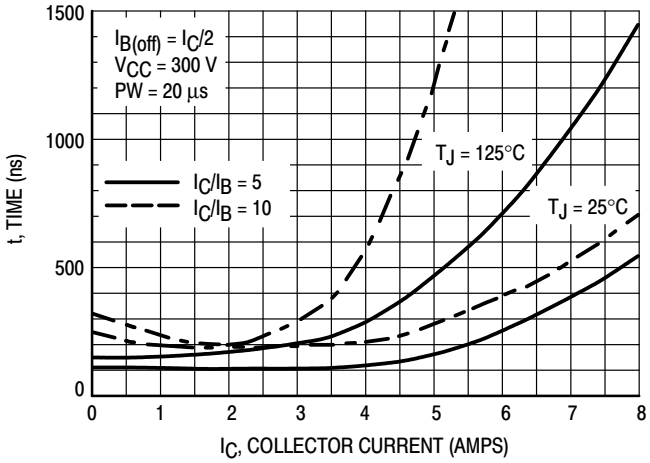


Figure 27. Resistive Switching, t_{on}

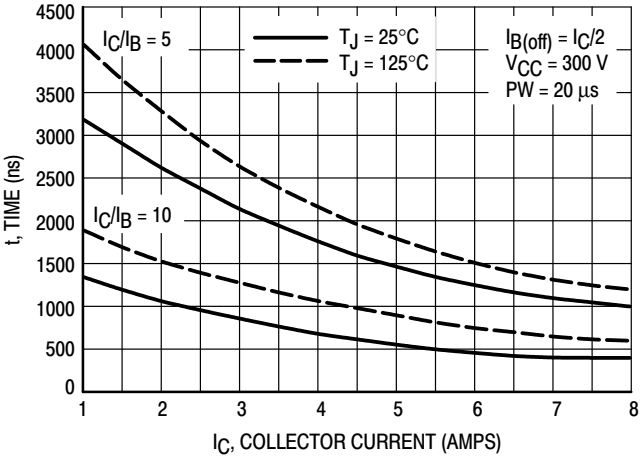


Figure 28. Resistive Switching, t_{off}

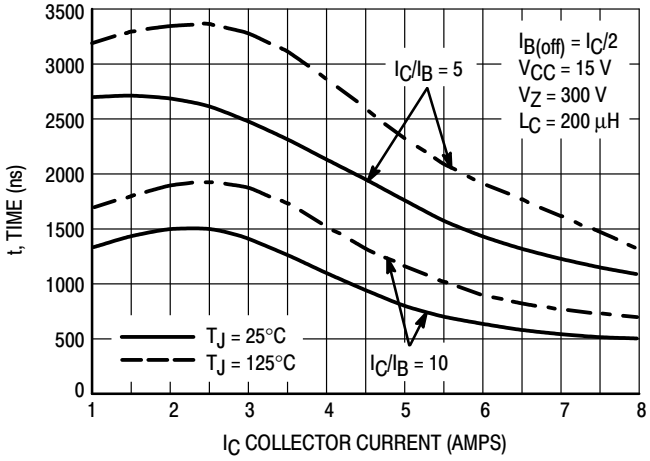


Figure 29. Inductive Storage Time, t_{si}

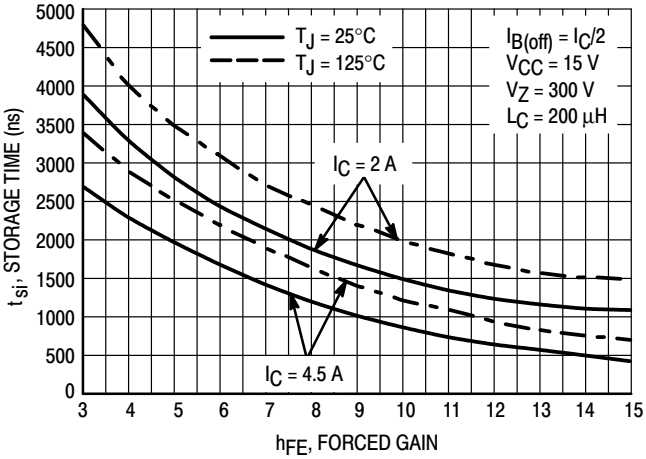


Figure 30. Inductive Storage Time, $t_{si}(h_{FE})$

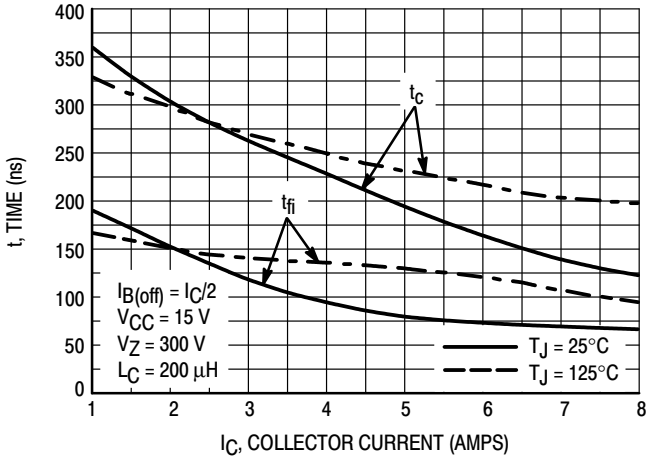


Figure 31. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

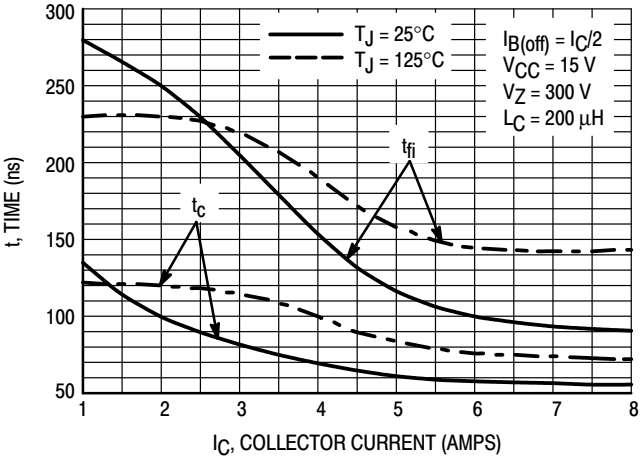


Figure 32. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
(I_{B2} = I_C/2 for all switching)

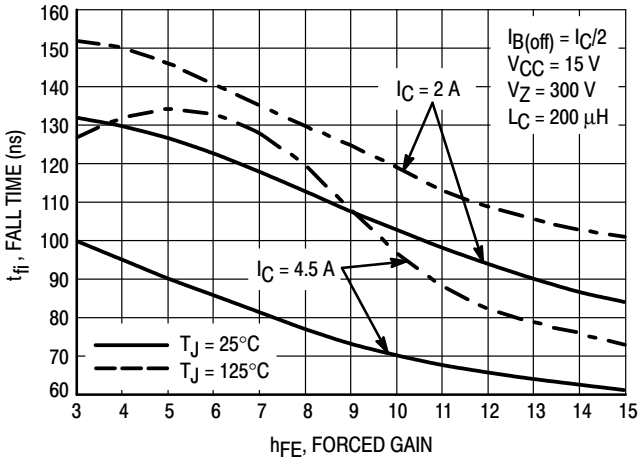


Figure 33. Inductive Fall Time

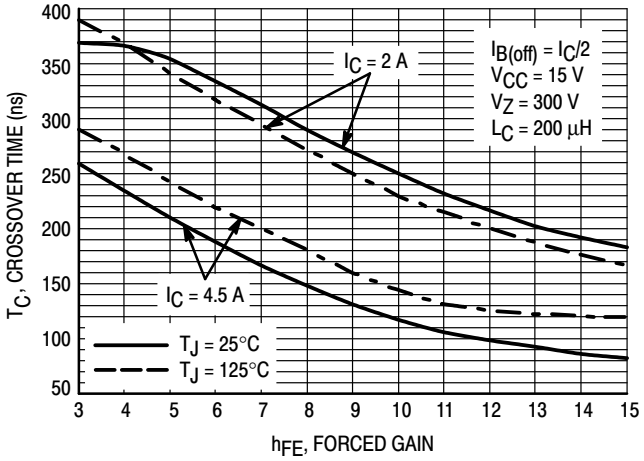


Figure 34. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

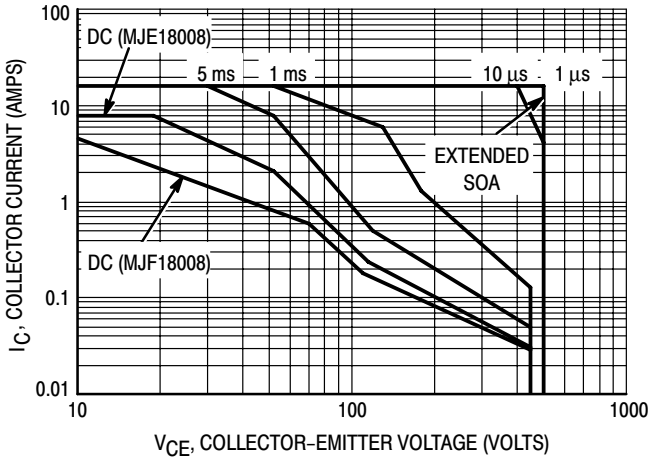


Figure 35. Forward Bias Safe Operating Area

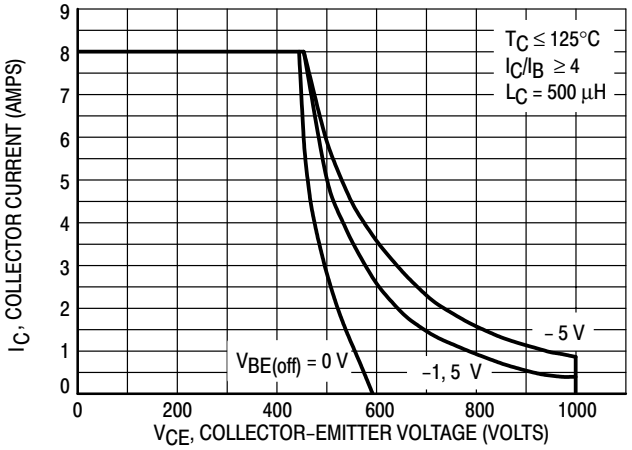


Figure 36. Reverse Bias Switching Safe Operating Area

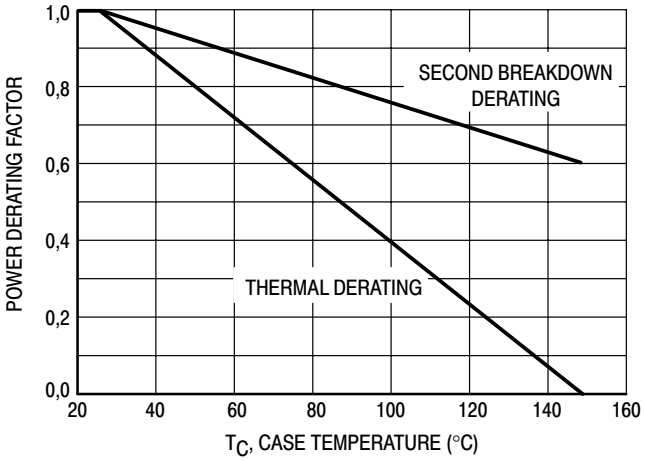


Figure 37. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 35 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 35 may be found at any case temperature by using the appropriate curve on Figure 37. $T_{J(pk)}$ may be calculated from the data in Figure 40 and 41. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse−biased. The safe level is specified as a reverse−biased safe operating area (Figure 36). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

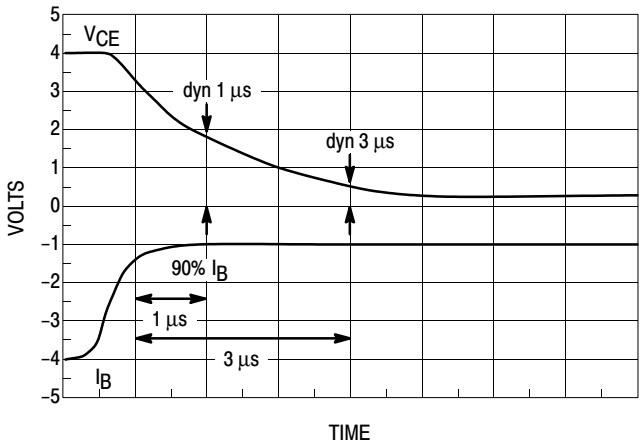


Figure 38. Dynamic Saturation Voltage Measurements

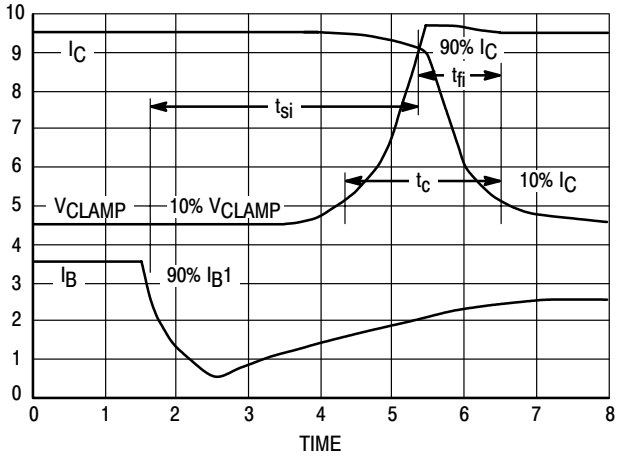
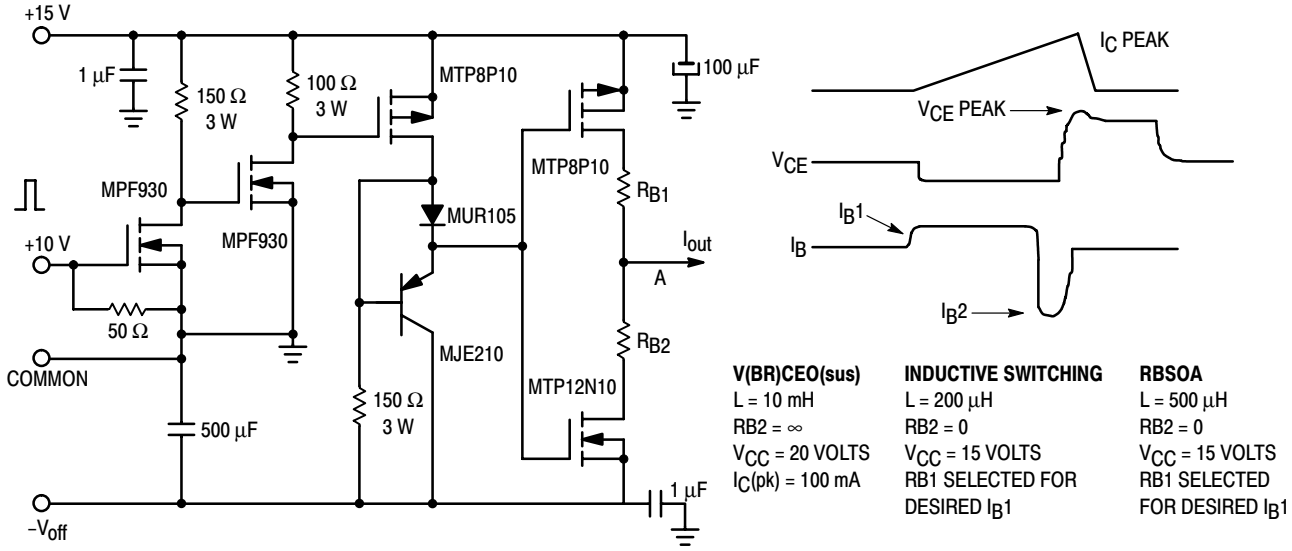


Figure 39. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

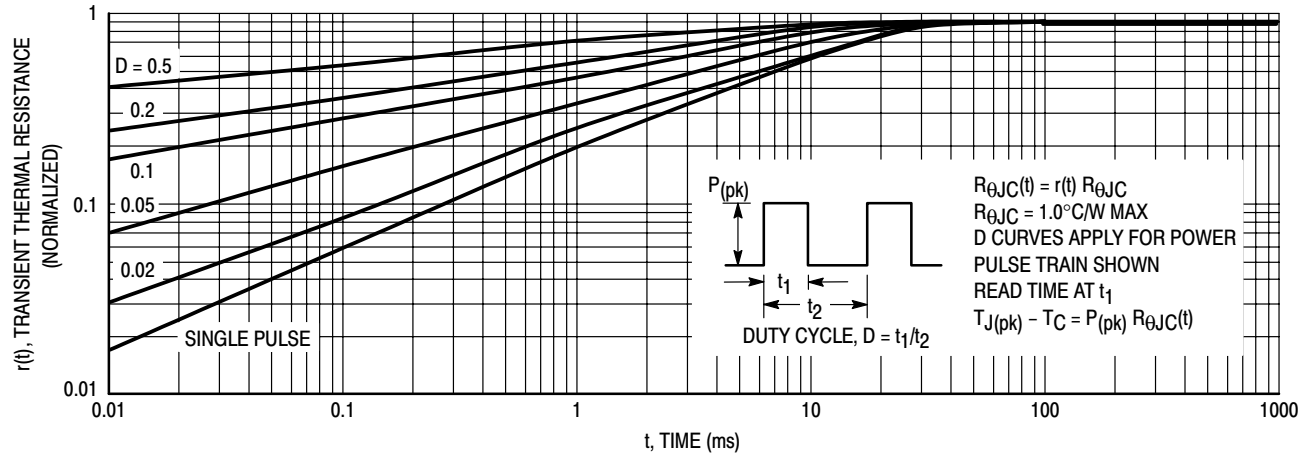


Figure 40. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18008

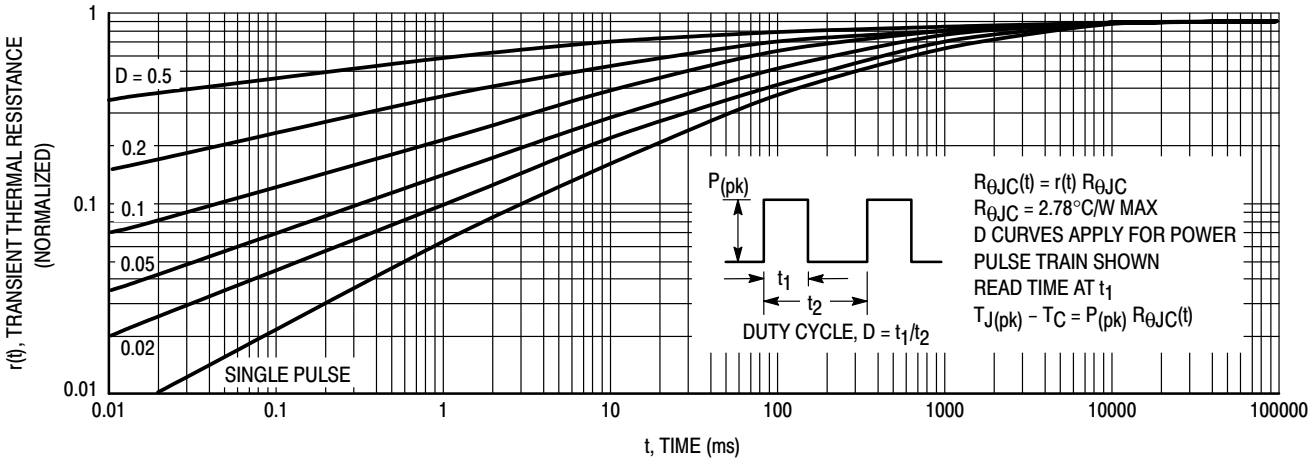


Figure 41. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18008

TEST CONDITIONS FOR ISOLATION TESTS*

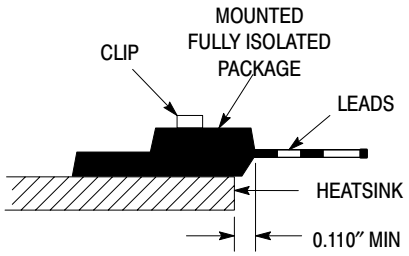


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

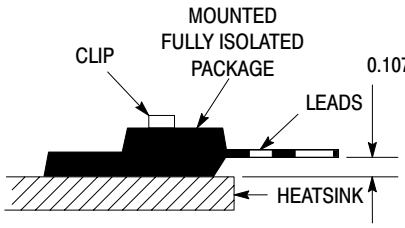


Figure 22b. Clip Mounting Position for Isolation Test Number 2

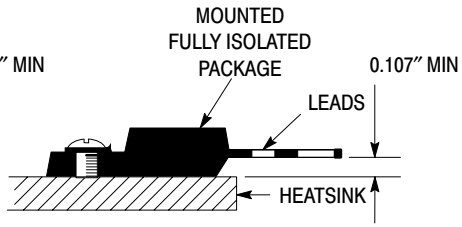


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

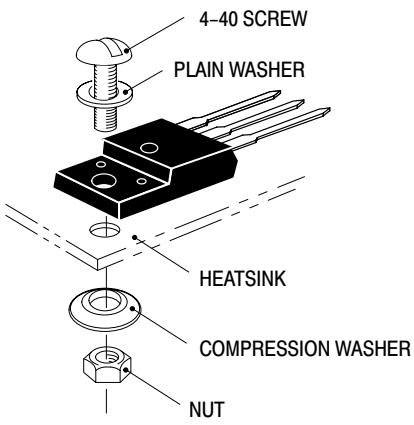


Figure 23a. Screw−Mounted

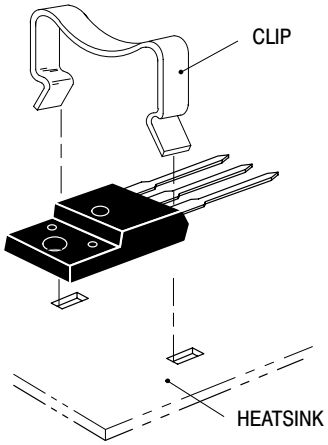


Figure 23b. Clip−Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Silicon Power Plastic Transistors

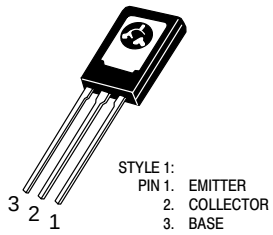
. . . designed for low voltage, low−power, high−gain audio amplifier applications.

- Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current−Gain — Bandwidth Product —
  f_T = 65 MHz (Min) @ I_C
  = 100 mAdc
- Annular Construction for Low Leakage —
  I_{CBO} = 100 nAdc @ Rated V_{CB}

NPN
MJE200*
PNP
MJE210*

*ON Semiconductor Preferred Device

5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
25 VOLTS
15 WATTS



CASE 77−09
TO−225AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Base Voltage	V_{CB}	40	Vdc
Collector−Emitter Voltage	V_{CEO}	25	Vdc
Emitter−Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 10
Publication Order Number:
MJE200/D

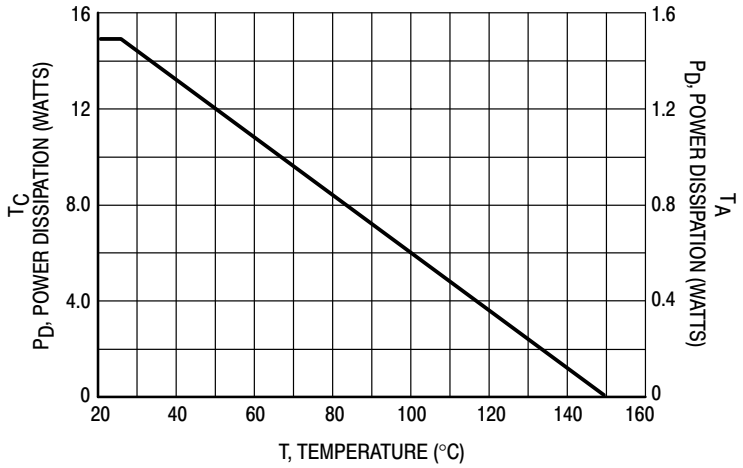


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 — —	 100 100	 nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}	 —	 100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 70 45 10	 — 180 —	—
Collector−Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	 — — —	 0.3 0.75 1.8	Vdc
Base−Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	—	2.5	Vdc
Base−Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200 MJE210	C_{ob}	 — —	 80 120	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

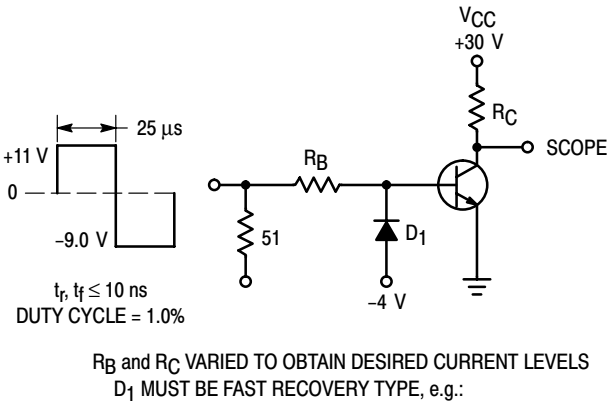


Figure 2. Switching Time Test Circuit

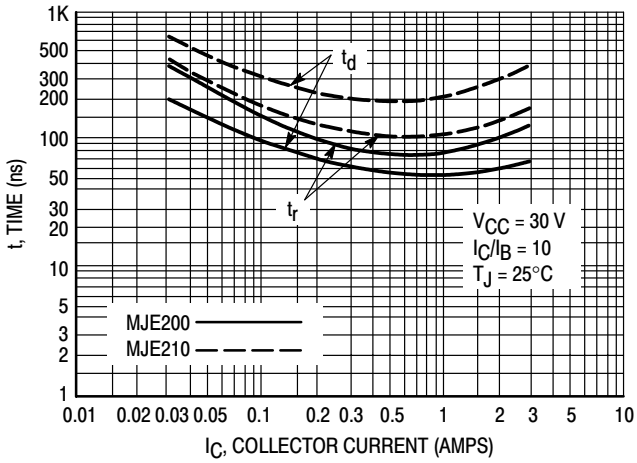


Figure 3. Turn−On Time

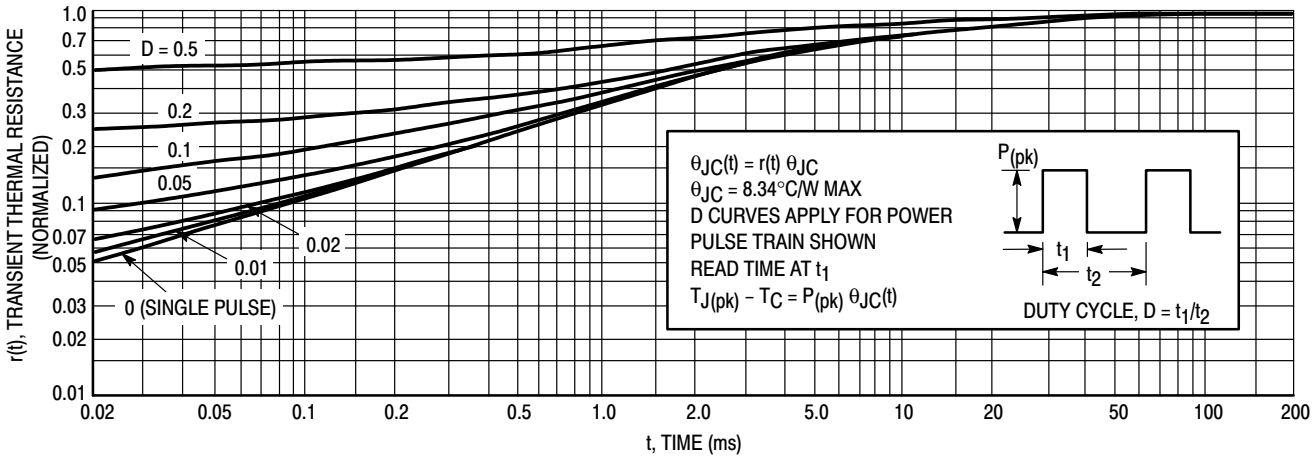


Figure 4. Thermal Response

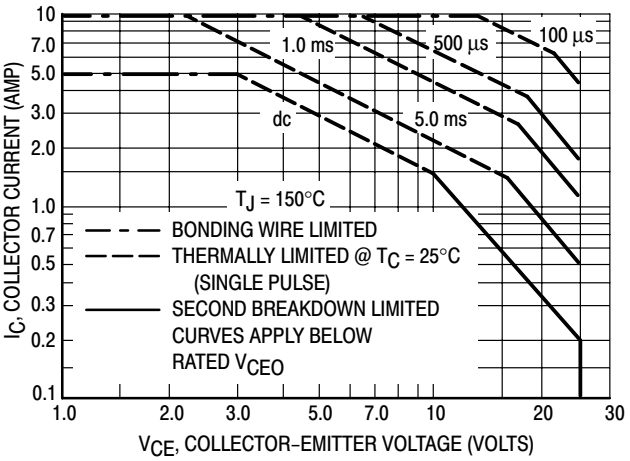


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

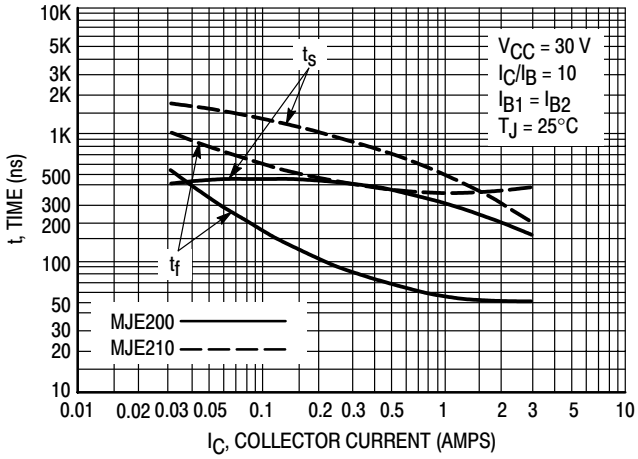


Figure 6. Turn−Off Time

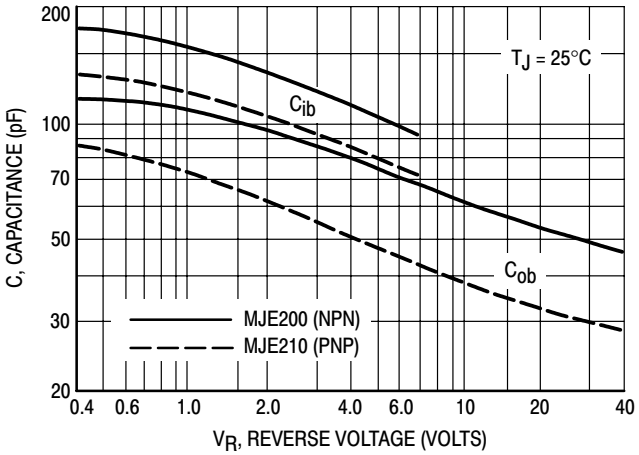
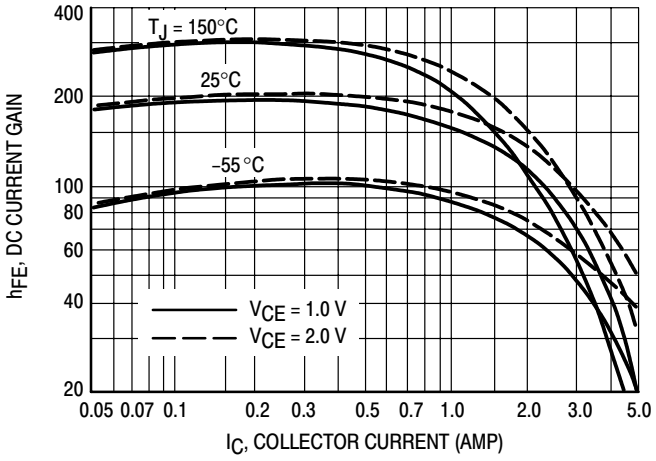


Figure 7. Capacitance

NPN
MJE200



PNP
MJE210

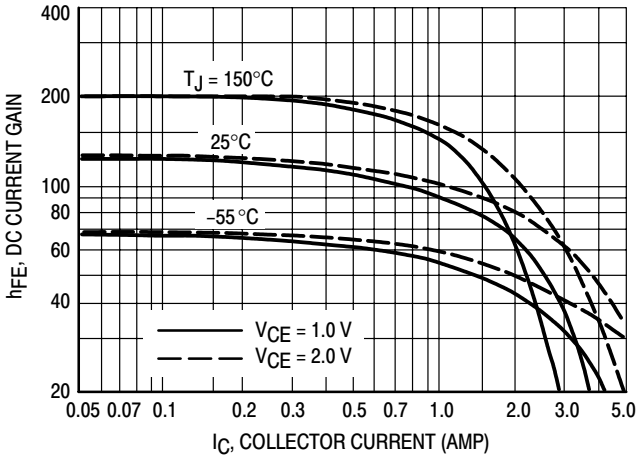
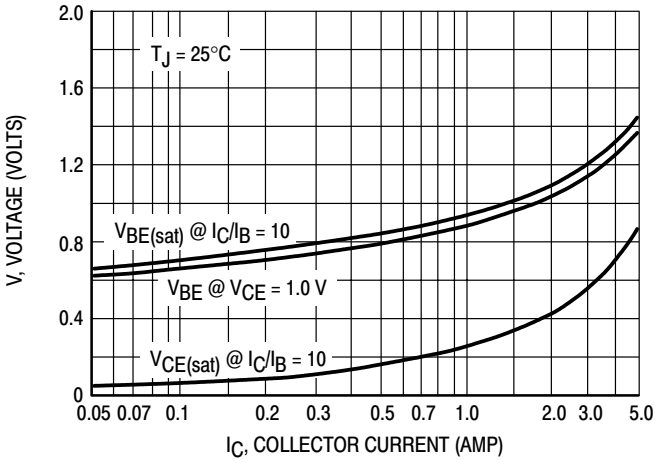


Figure 8. DC Current Gain



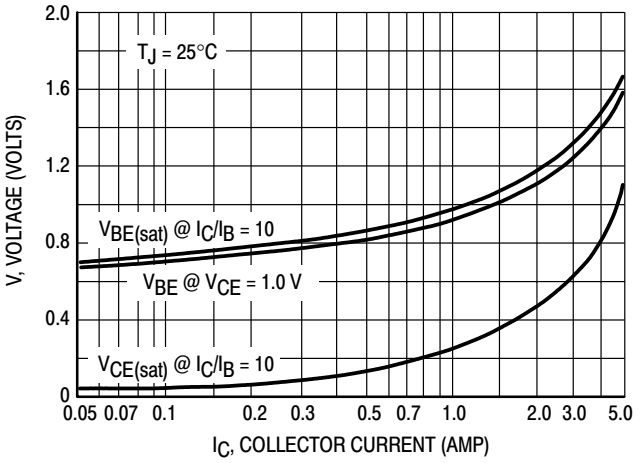
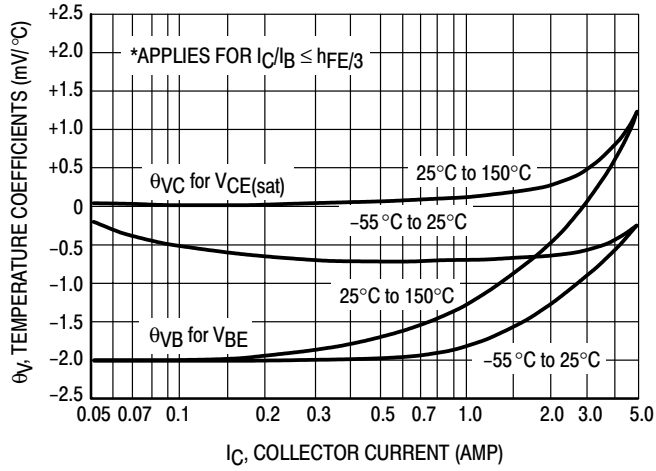


Figure 9. “On” Voltage



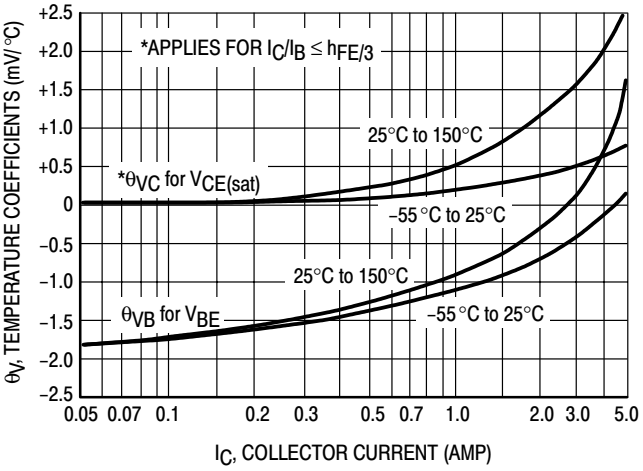


Figure 10. Temperature Coefficients

Complementary Silicon Power Plastic Transistors

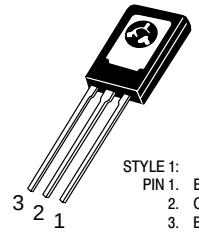
. . . designed for low power audio amplifier and low−current, high−speed switching applications.

- High Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — MJE243, MJE253
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40−200
  = 40−120 — MJE243, MJE253
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages
  I_{CBO} = 100 nAdc (Max) @ Rated V_{CB}

NPN
MJE243*
PNP
MJE253*

*ON Semiconductor Preferred Device

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
100 VOLTS
15 WATTS



CASE 77−09
TO−225AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0	Adc
Base Current	I_B	10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/ac
Total Power Dissipation @ T_A = 25°C Derate @ 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

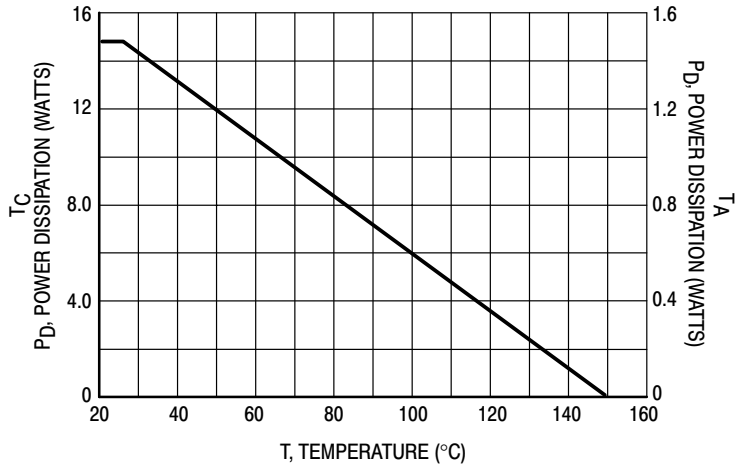
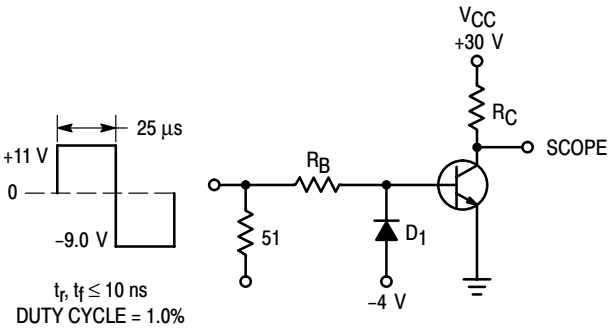


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CE} = 100 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}	— —	0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40 15	180 —	—
Collector−Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	— —	0.3 0.6	Vdc
Base−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	1.8	Vdc
Base−Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	50	pF



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 2. Switching Time Test Circuit

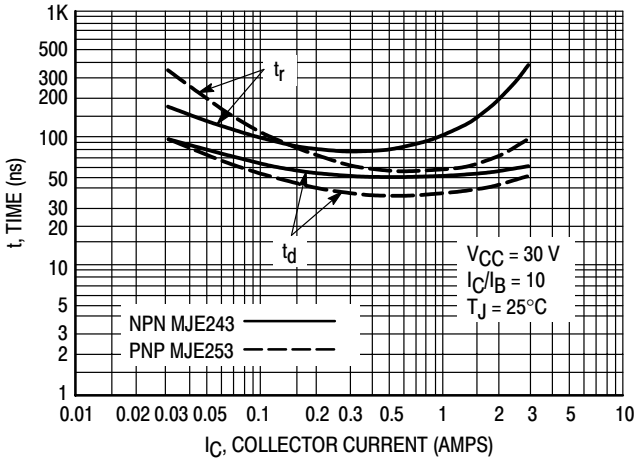


Figure 3. Turn−On Time

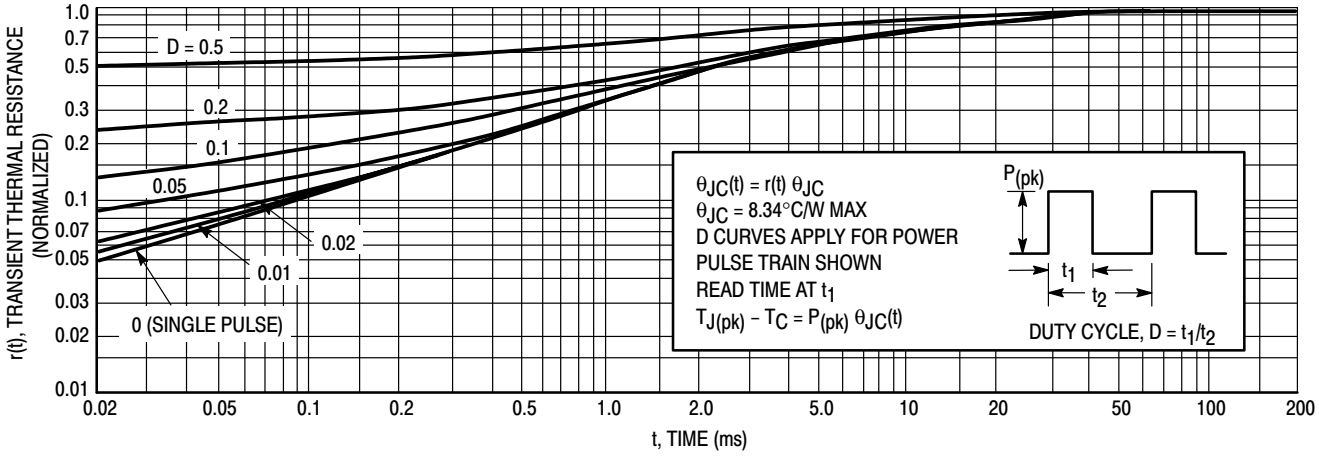


Figure 4. Thermal Response

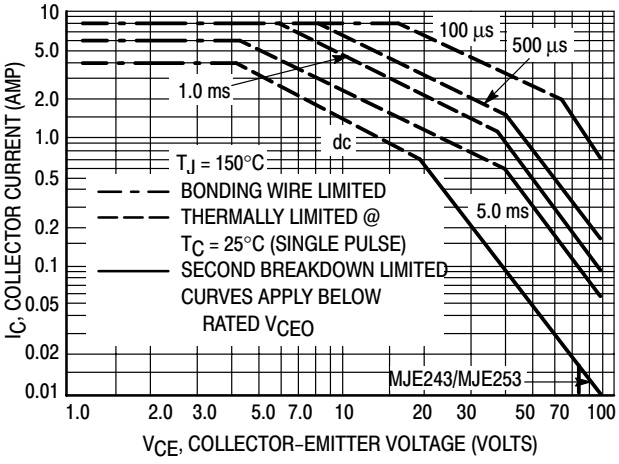


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

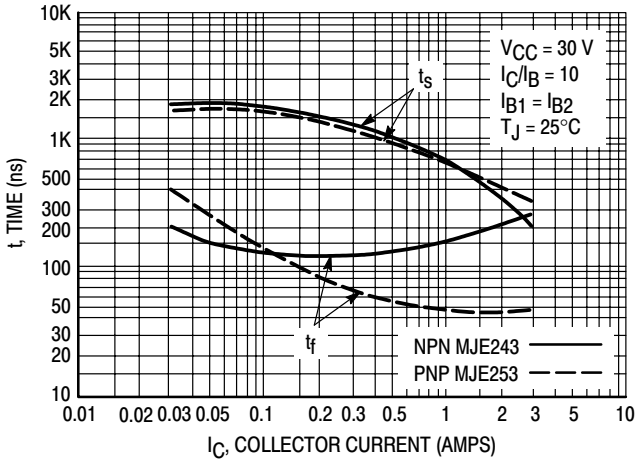


Figure 6. Turn−Off Time

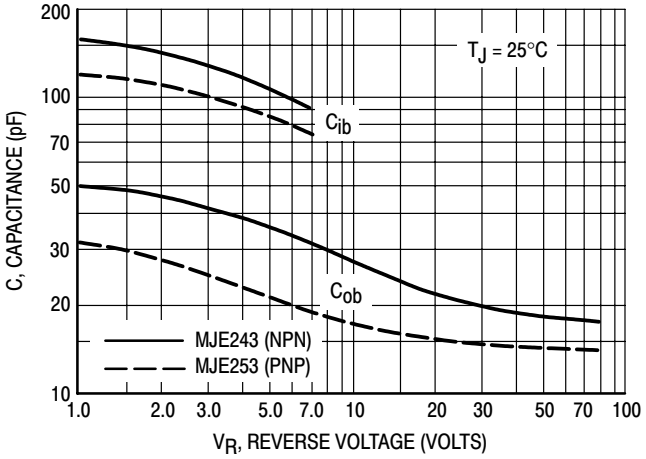
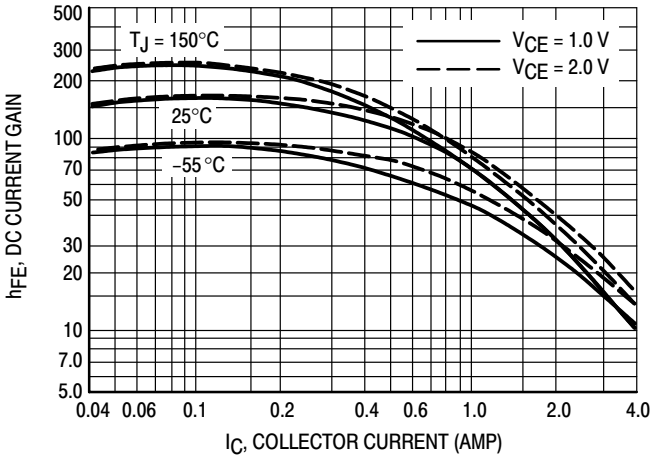


Figure 7. Capacitance

NPN
MJE243



PNP
MJE253

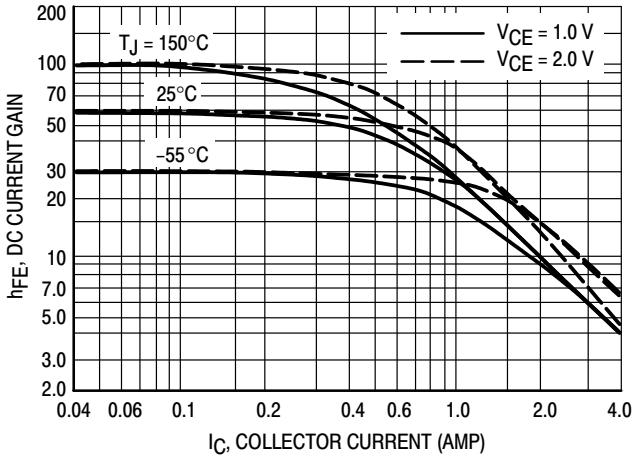
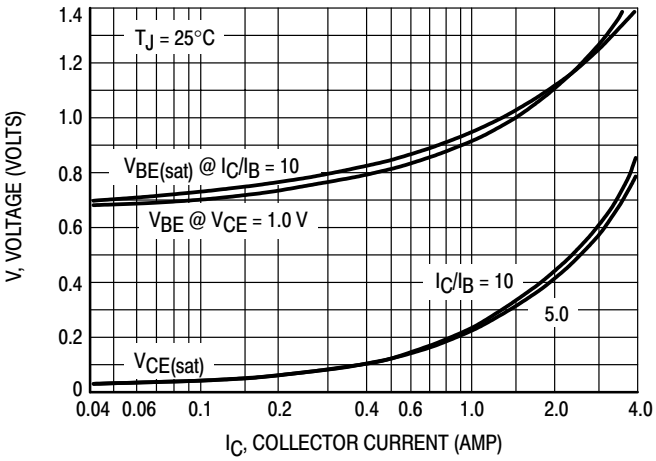


Figure 8. DC Current Gain



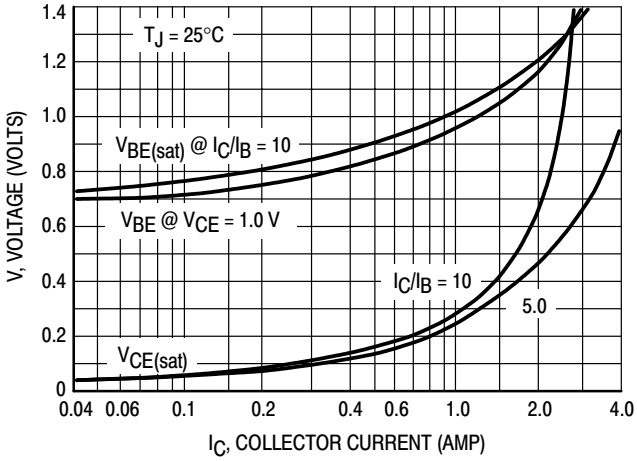
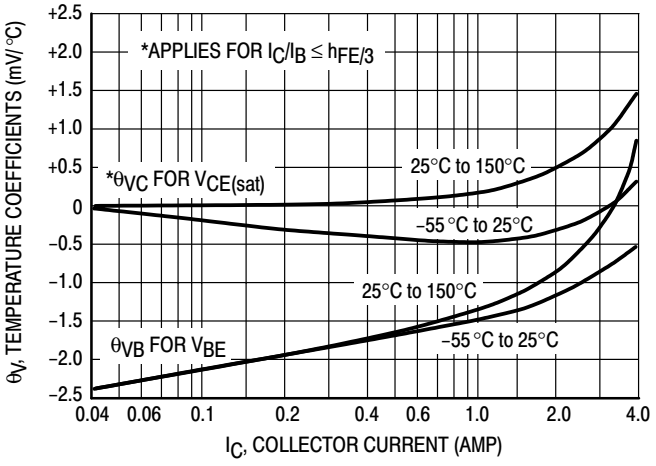


Figure 9. “On” Voltages



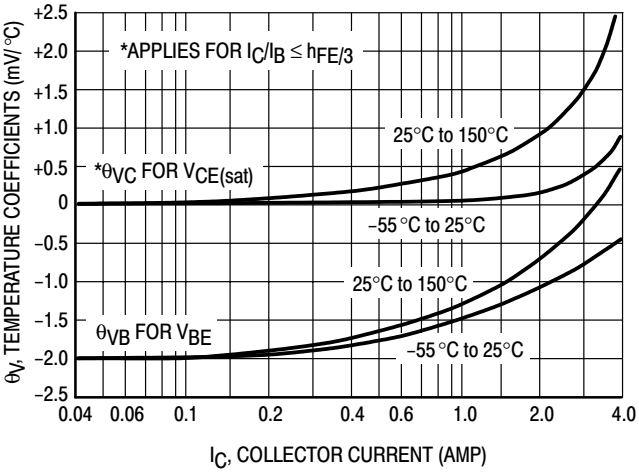


Figure 10. Temperature Coefficients

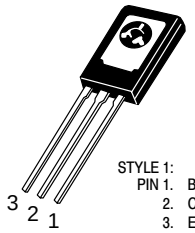
Complementary Silicon Power Transistors

. . . designed specifically for use with the MC3419 Solid−State Subscriber Loop Interface Circuit (SLIC).

- High Safe Operating Area
  $I_{S/B}$ @ 40 V, 1.0 s = 0.375 A — TO−126
- Collector−Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- High DC Current Gain
  h_{FE} @ 120 mA, 10 V = 1500 (Min)

NPN
MJE270
PNP
MJE271

2.0 AMPERE
COMPLEMENTARY
POWER DARLINGTON
TRANSISTORS
100 VOLTS
15 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	2.0 4.0	Adc
Base Current	I_B	0.1	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

April, 2002 − Rev. 4
Publication Order Number:
MJE270/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.3	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, non−repetitive)	$I_{S/b}$	375	—	Adc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 20 mAdc, V_{CE} = 3.0 Vdc) (I_C = 120 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 500 1500	 — —	—
Collector−Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 0.2 mAdc) (I_C = 120 mAdc, I_B = 1.2 mAdc)	$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base−Emitter On Voltage (I_C = 120 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 0.05 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	—	MHz

NOTES:
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \bullet f_{test}$.

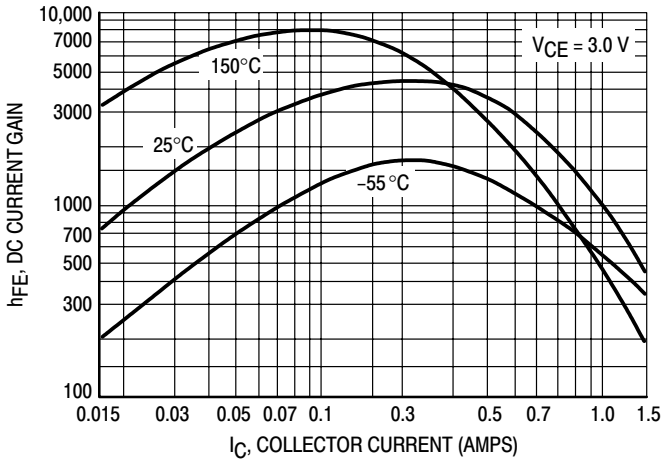


Figure 1. DC Current Gain

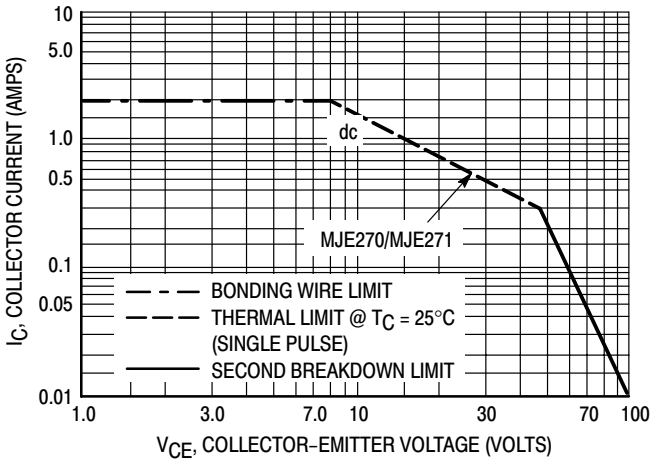


Figure 2. Safe Operating Area

Complementary Silicon Plastic Power Transistors

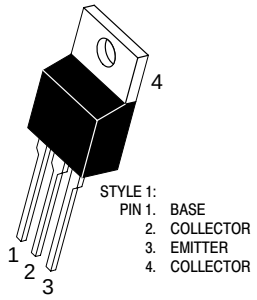
. . . designed for use in general−purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product —
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc

PNP
MJE2955T*
NPN
MJE3055T*

*ON Semiconductor Preferred Device

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60 VOLTS 75 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CB}	70	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C MJE3055T, MJE2955T	P_D†	75 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

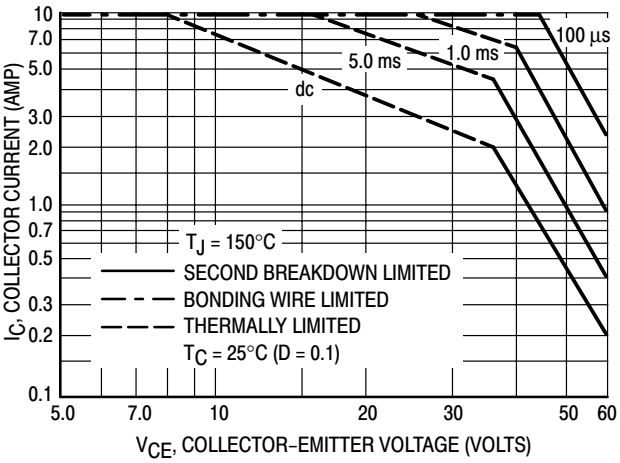


Figure 1. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4 0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 100 —	—
Collector−Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 8.0	Vdc
Base−Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain−Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 20%.

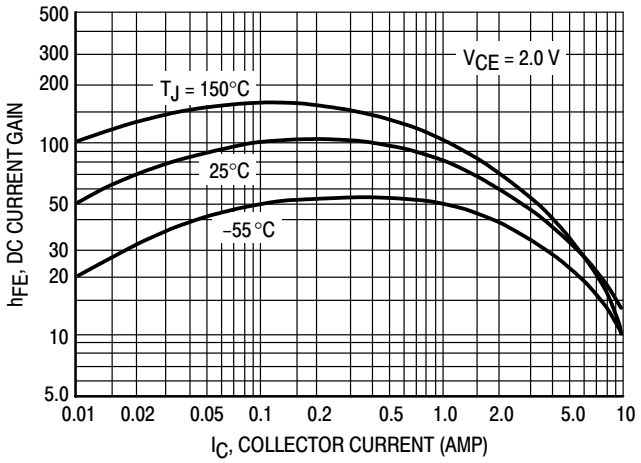


Figure 2. DC Current Gain

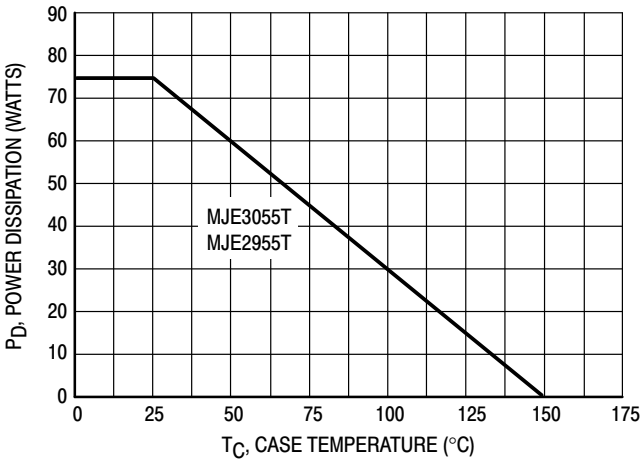
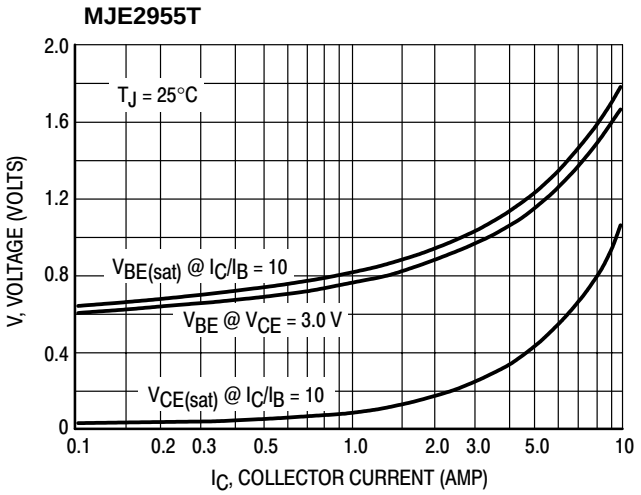


Figure 3. Power Derating



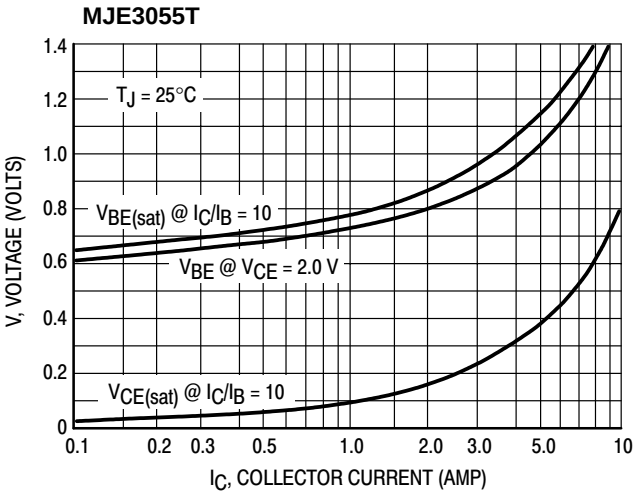


Figure 4. “On” Voltages

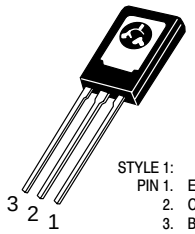
MJE340

Plastic Medium Power NPN Silicon Transistor

. . . useful for high−voltage general purpose applications.

- Suitable for Transformerless, Line−Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
300 VOLTS
20 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Emitter−Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

April, 2002 − Rev. 10
Publication Order Number:
MJE340/D

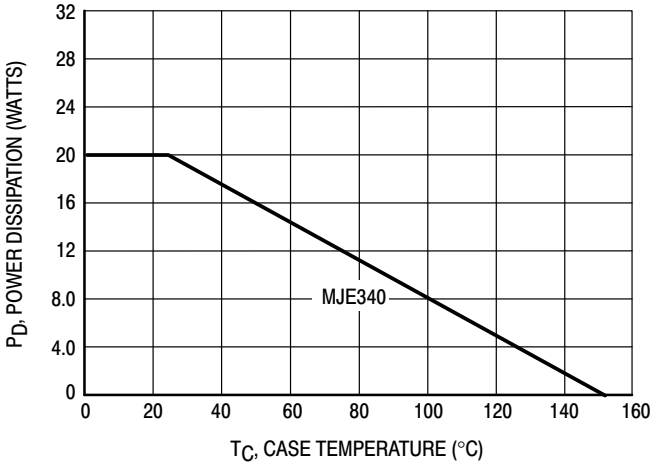


Figure 5. Power Temperature Derating

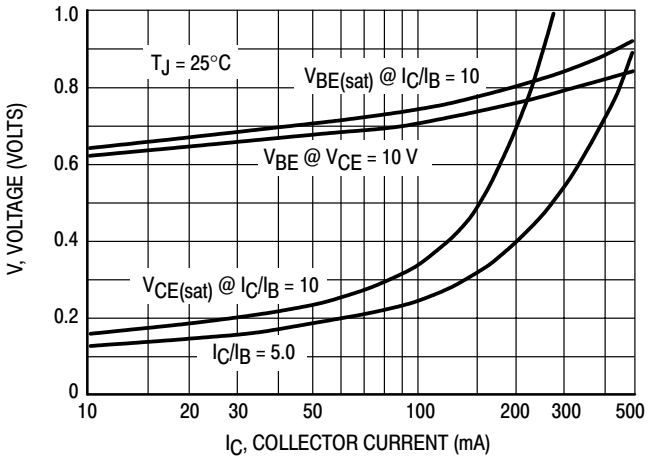


Figure 6. "On" Voltages

ACTIVE−REGION SAFE OPERATING AREA

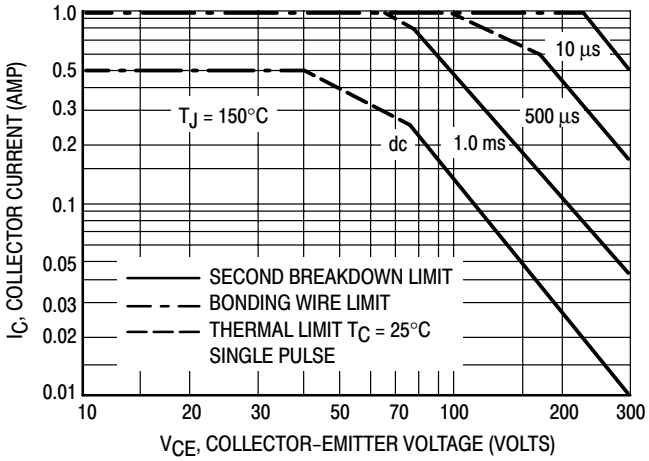


Figure 7. MJE340

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

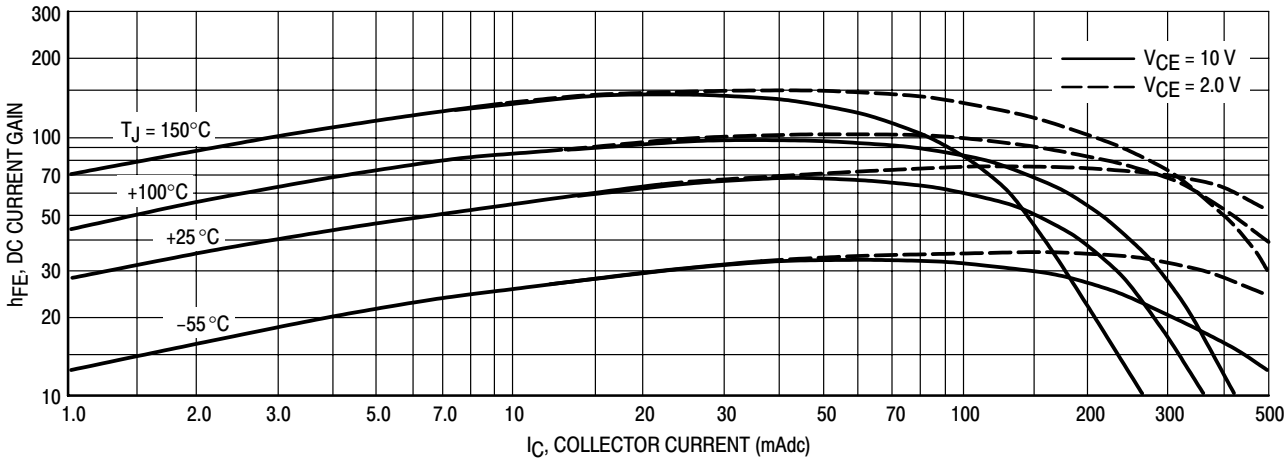


Figure 8. DC Current Gain

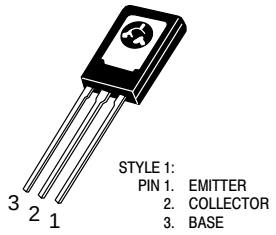
MJE3439

NPN Silicon High-Voltage Power Transistors

. . . designed for use in line−operated equipment requiring high f_T.

- High DC Current Gain
  h_{FE} = 40−160 @ I_C
  = 20 mAdc
- Current Gain Bandwidth Product —
  f_T = 15 MHz (Min) @ I_C
  = 10 mAdc
- Low Output Capacitance
  C_{ob} = 10 pF (Max) @ f
  = 1.0 MHz

0.3 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
15 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	350	Vdc
Collector−Base Voltage	V_{CB}	450	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	0.3	Adc
Base Current	I_B	150	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	°C/W

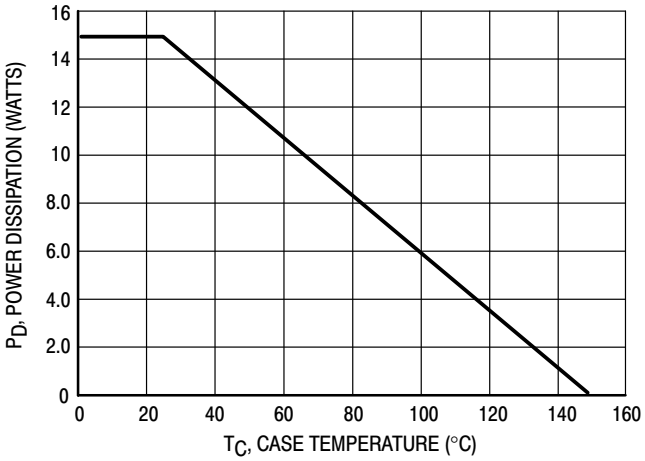


Figure 1. Power−Temperature Derating Curve

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	350	—	Vdc
Collector Cutoff Current (V_{CE} = 300 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	—	500	μAdc
Collector Cutoff Current (V_{CB} = 350 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	20	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc) (I_C = 20 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30 15	— 200	—
Collector−Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)	$V_{CE(sat)}$	—	0.5	Vdc
Base−Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)	$V_{BE(sat)}$	—	1.3	Vdc
Base−Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	0.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)	f_T	15	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	10	pF
Small−Signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	—	—

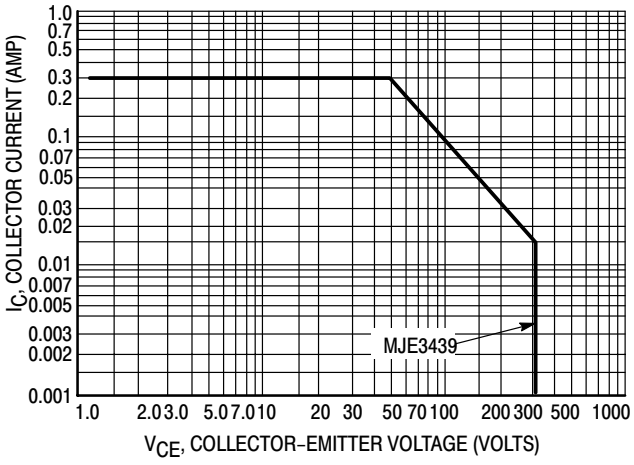


Figure 2. Active−Region Safe Operating Area

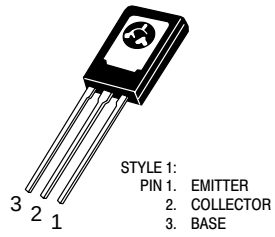
The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power−temperature derating must be observed for both steady state and pulse power conditions.

MJE344

Plastic NPN Silicon Medium-Power Transistor

. . . useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
150−200 VOLTS
20 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	MJE344	Unit
Collector−Emitter Voltage	V_{CEO}	200	Vdc
Collector−Base Voltage	V_{CB}	200	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Base Current	I_B	250	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

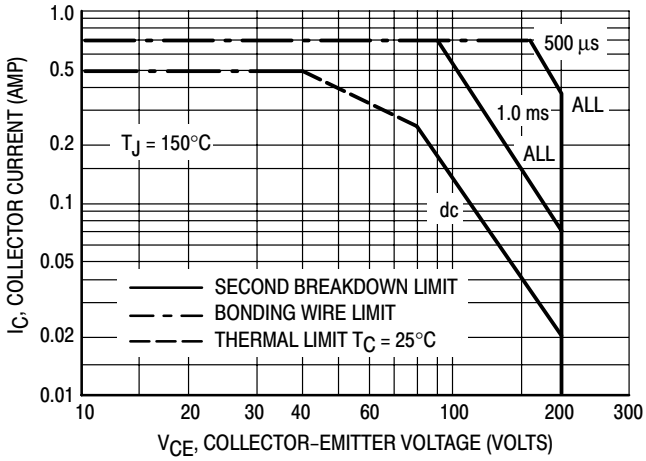


Figure 1. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less then the limitations imposed by second breakdown.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	300	—
Collector−Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	—	1.0	Vdc
Base−Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 10 MHz)	f_T	15	—	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	—	15	pF
Small−Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	—	—

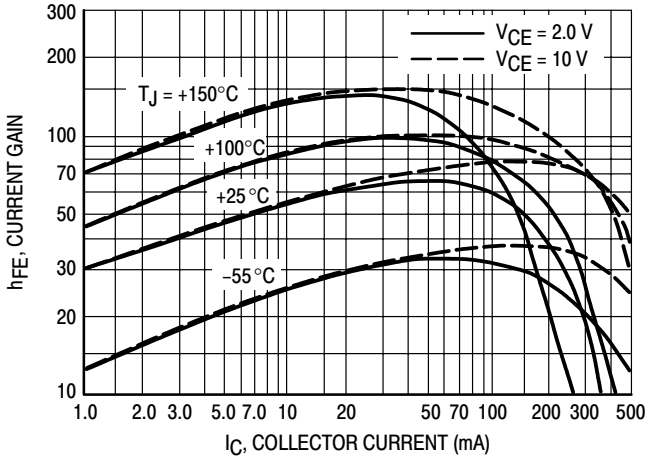


Figure 2. DC Current Gain

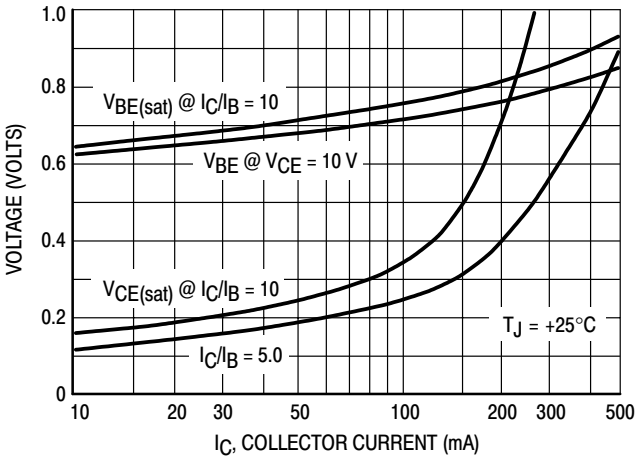


Figure 3. “On” Voltages

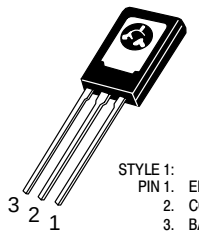
MJE350

Plastic Medium Power PNP Silicon Transistor

. . . designed for use in line−operated applications such as low power, line−operated series pass and switching regulators requiring PNP capability.

- High Collector−Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain —
  h_{FE} = 30−240 @ I_C = 50 mAdc
- Plastic Thermopad Package

0.5 AMPERE
POWER TRANSISTOR
PNP SILICON
300 VOLTS
20 WATTS



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Emitter−Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

April, 2002 − Rev. 12
Publication Order Number:
MJE350/D

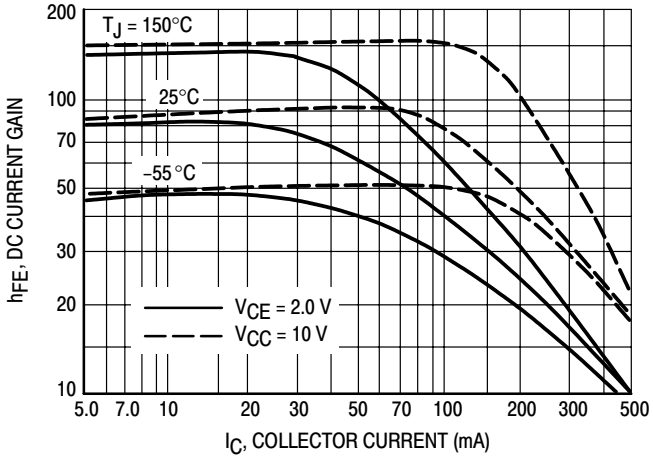


Figure 1. DC Current Gain

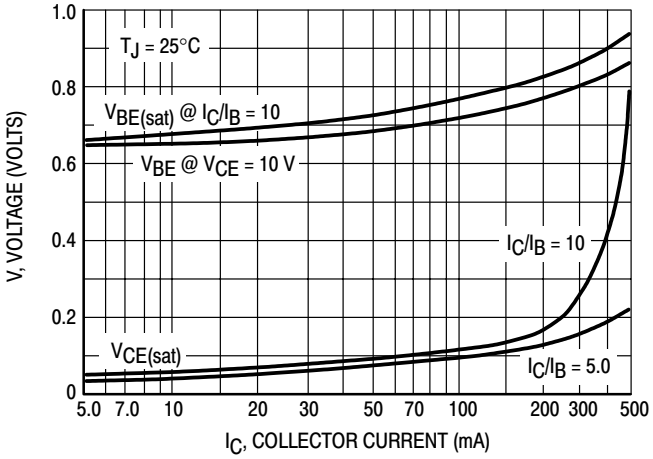


Figure 2. "On" Voltages

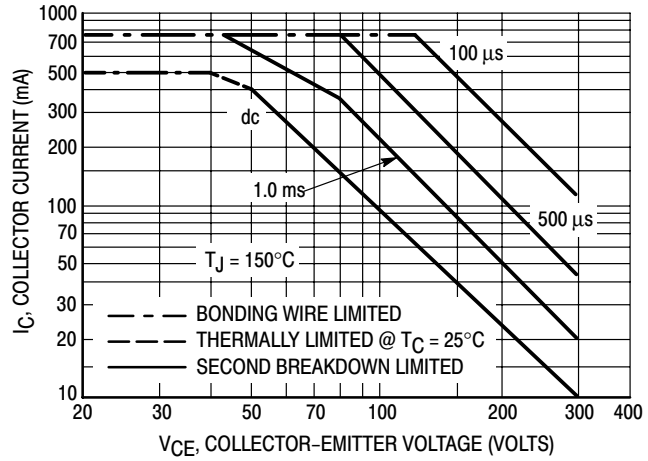


Figure 3. Active−Region Safe Operating Area

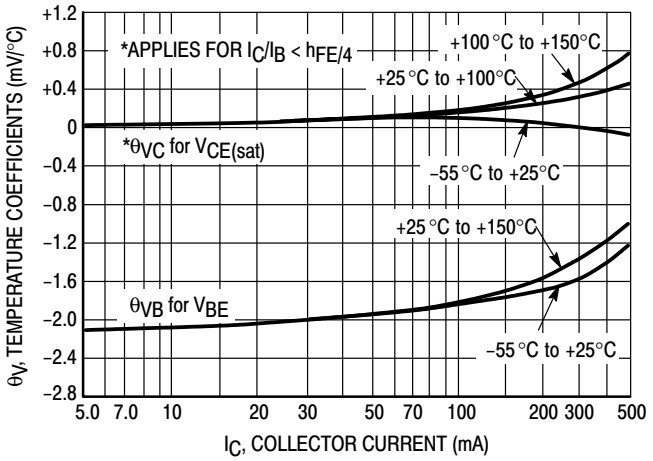


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

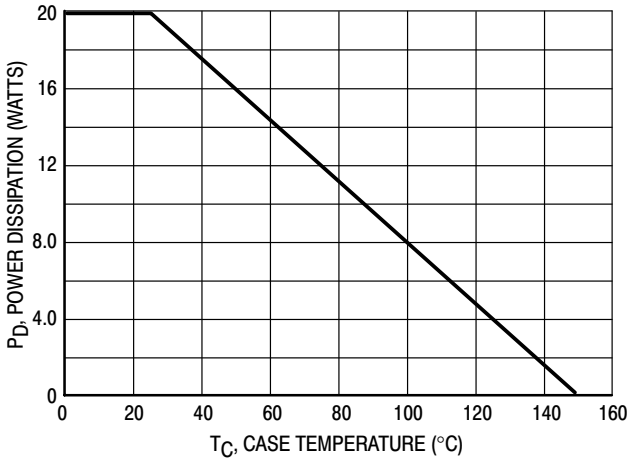


Figure 5. Power Derating

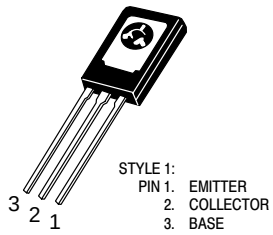
MJE371

Plastic Medium-Power PNP Silicon Transistors

4 AMPERE
POWER TRANSISTOR
PNP SILICON
40 VOLTS
40 WATTS

. . . designed for use in general−purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- MJE371 is Complementary to NPN MJE521



CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CB}	40	Vdc
Emitter−Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector−Base Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter−Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

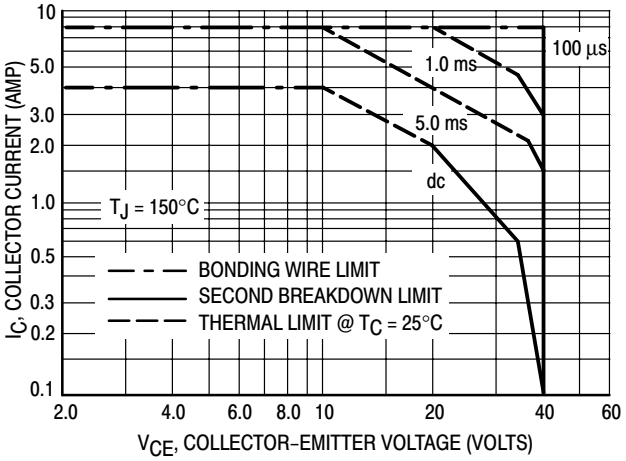


Figure 1. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less then the limitations imposed by second breakdown.

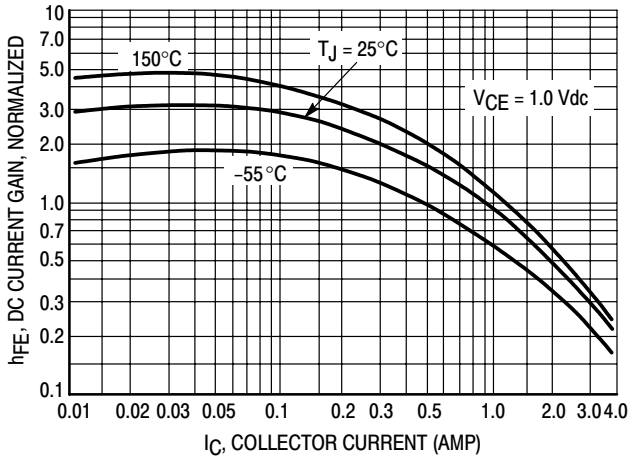


Figure 2. DC Current Gain

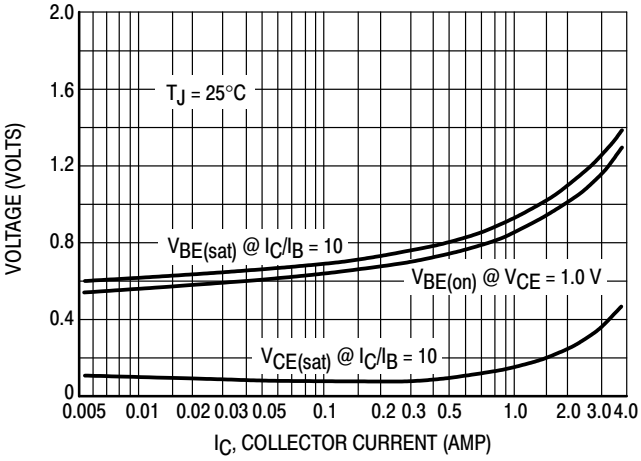


Figure 3. “On” Voltage

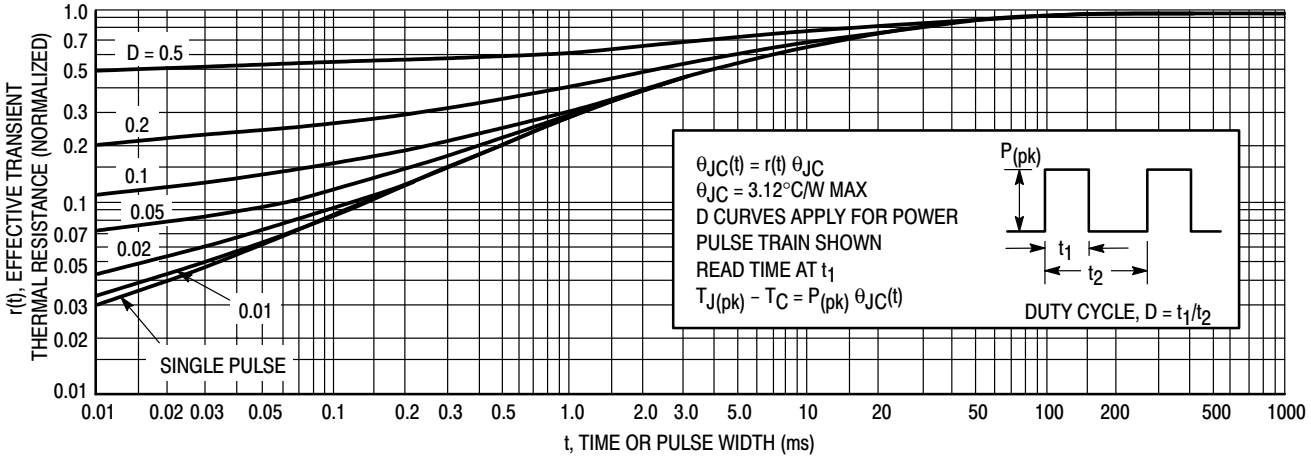


Figure 4. Thermal Response

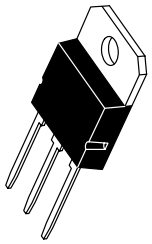
NPN
MJE4343
PNP
MJE4353

High-Voltage — High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector−Emitter Sustaining Voltage —
  NPN PNP
  $V_{CEO(sus)}$ = 160 Vdc — MJE4343 MJE4353
- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 35 (Typ)
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C
  = 8.0 Adc

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
160 VOLTS



CASE 340D−02
TO−218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	160	Vdc
Collector−Base Voltage	V_{CB}	160	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak (1)	I_C	16 20	Adc
Base Current — Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C	P_D	125	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

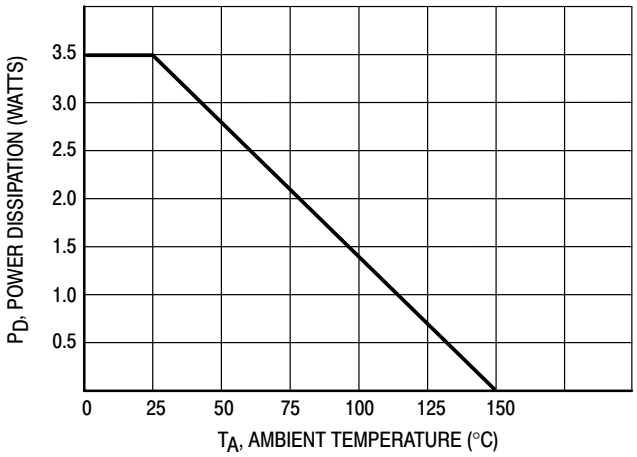


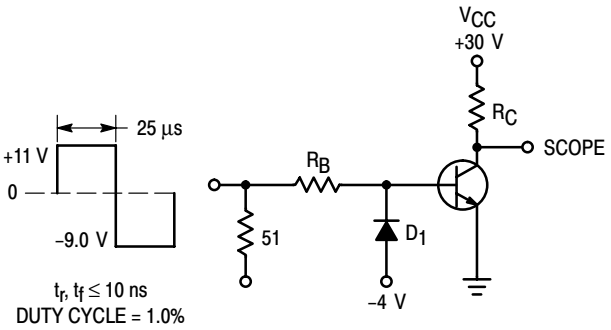
Figure 1. Power Derating
Reference: Ambient Temperature

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	160	—	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CEO}	—	750	μAdc
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	1.0 5.0	mAdc
Collector−Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	—	750	μAdc
Emitter−Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	15 8.0	35 (Typ) 15 (Typ)	—
Collector−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 800 mA) (I_C = 16 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	— —	2.0 3.5	Vdc
Base−Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	—	3.9	Vdc
Base−Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	3.9	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Note: Reverse polarities to test PNP devices.

Figure 2. Switching Times Test Circuit

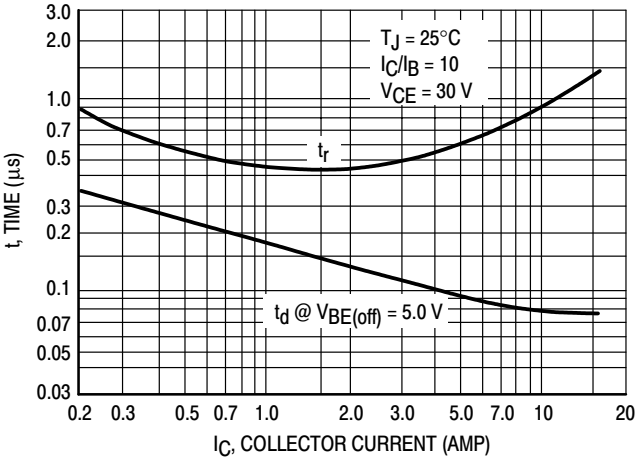


Figure 3. Typical Turn−On Time

TYPICAL CHARACTERISTICS

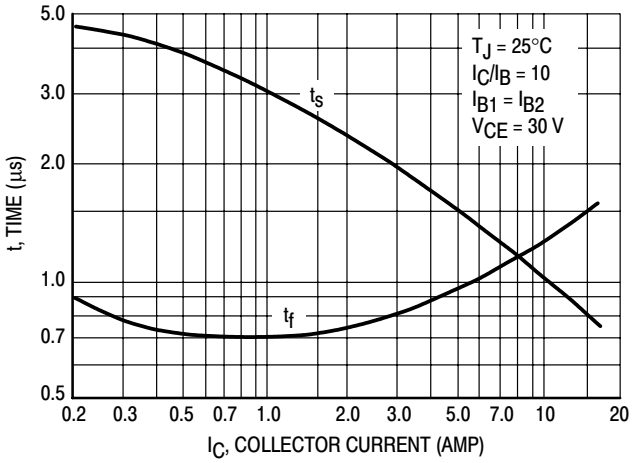


Figure 4. Turn−Off Time

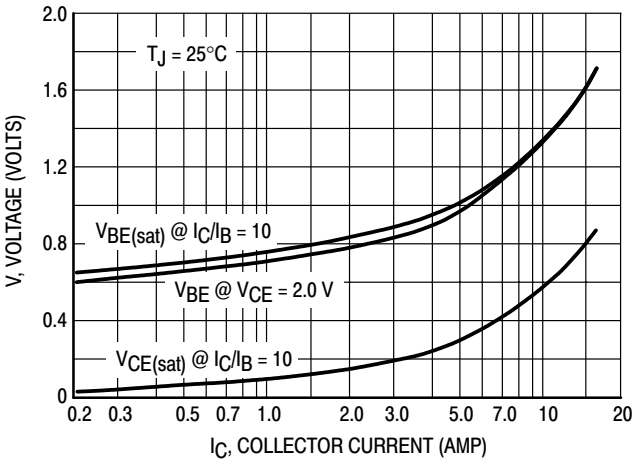


Figure 5. On Voltages

DC CURRENT GAIN

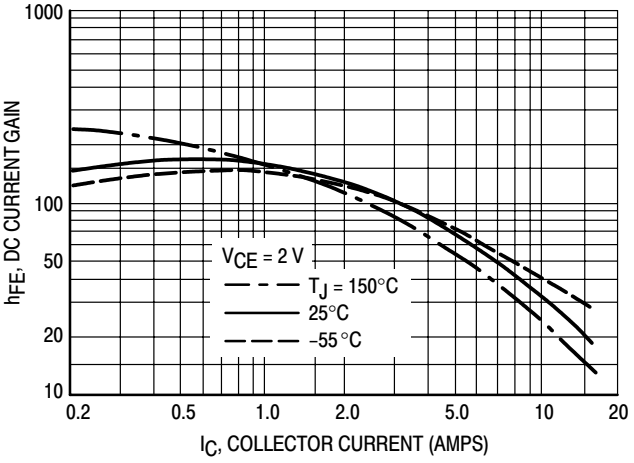


Figure 6. MJE4340 Series (NPN)

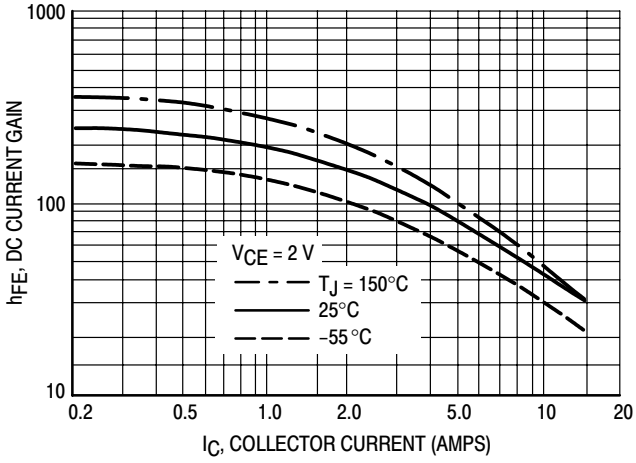


Figure 7. MJE4350 Series (PNP)

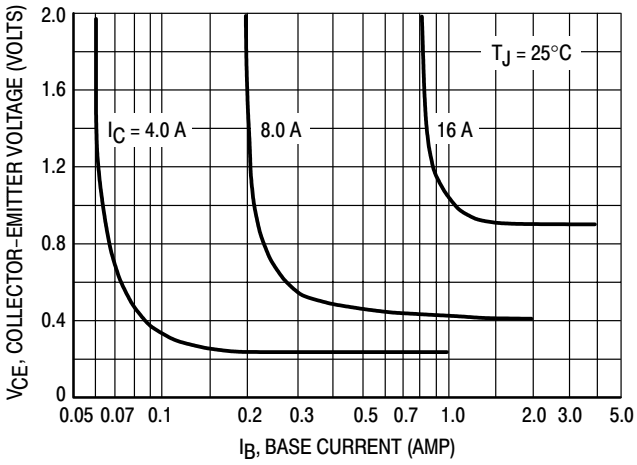


Figure 8. Collector Saturation Region

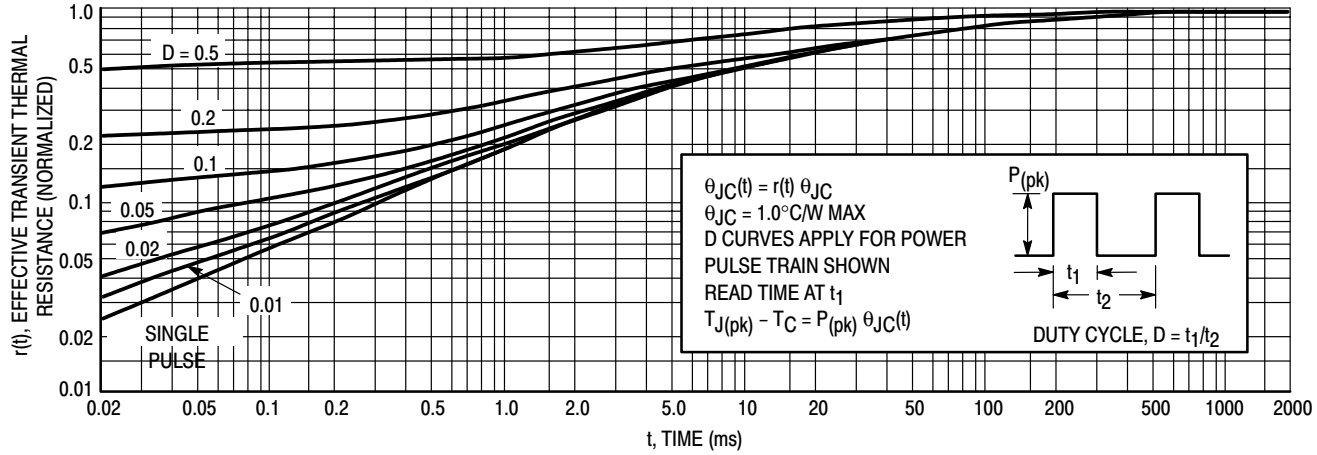


Figure 9. Thermal Response

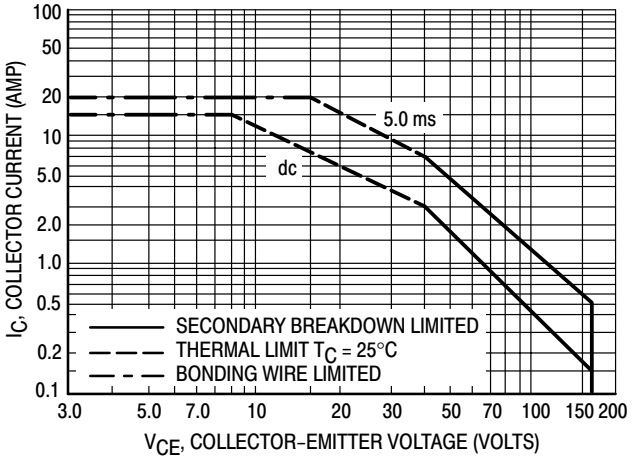


Figure 10. Maximum Forward Bias Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

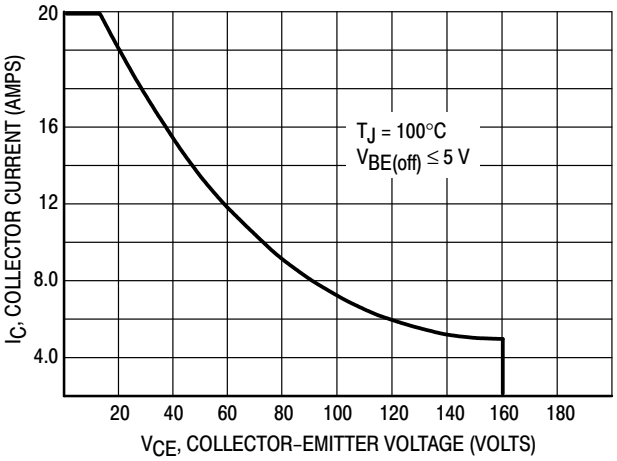


Figure 11. Maximum Reverse Bias Safe Operating Area

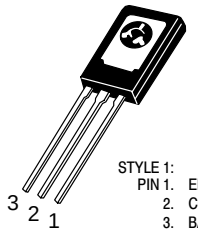
MJE521

Plastic Medium-Power NPN Silicon Transistor

. . . designed for use in general−purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE371

4 AMPERE
POWER TRANSISTOR
NPN SILICON
40 VOLTS
40 WATTS



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 77−09
TO−225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CB}	40	Vdc
Emitter−Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector−Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter−Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

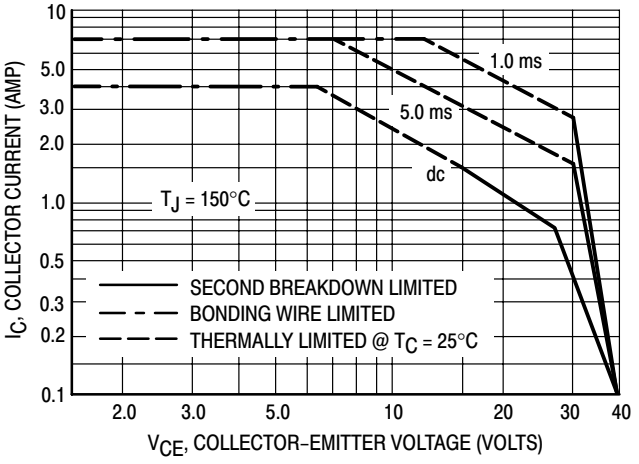


Figure 1. Active−Region Safe Operating Area

The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided (T_{Jpk}) ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

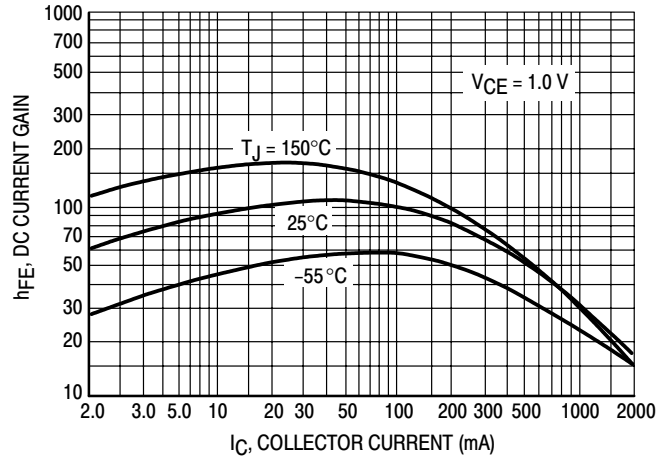


Figure 2. DC Current Gain

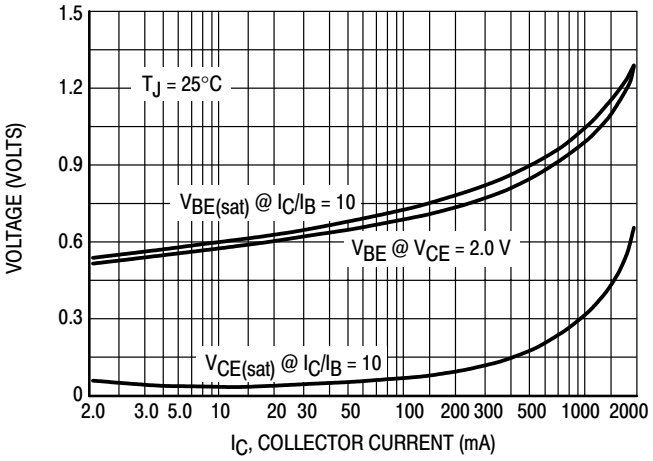


Figure 3. “On” Voltage

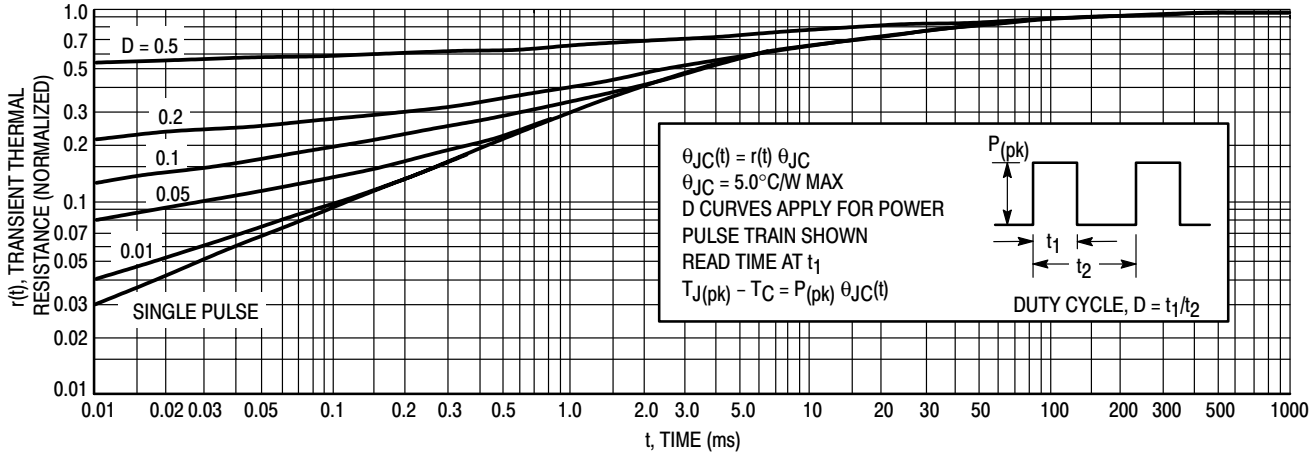


Figure 4. Thermal Response

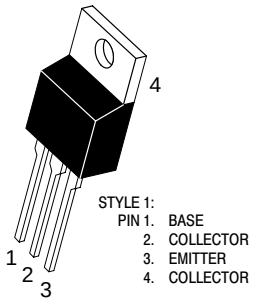
MJE5730
MJE5731
MJE5731A

High Voltage PNP Silicon Power Transistors

. . . designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- 300 V to 400 V (Min) — $V_{CEO(sus)}$
- 1.0 A Rated Collector Current
- Popular TO−220 Plastic Package
- PNP Complements to the TIP47 thru TIP50 Series

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
300−350−400 VOLTS
40 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5730	MJE5731	MJE5731A	Unit
Collector−Emitter Voltage	V_{CEO}	300	350	375	Vdc
Collector−Base Voltage	V_{CB}	300	350	375	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inducting Load Energy (See Figure 10)	E	20			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

April, 2002 − Rev. 4
Publication Order Number:
MJE5730/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJE5730 MJE5731 MJE5731A	$V_{CEO(sus)}$	 300 350 375	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 250 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJE5730 MJE5731 MJE5731A	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 300 Vdc, V_{BE} = 0) (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 400 Vdc, V_{BE} = 0)	 MJE5730 MJE5731 MJE5731A	I_{CES}	 — — —	 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 —	—
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	—	MHz
Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

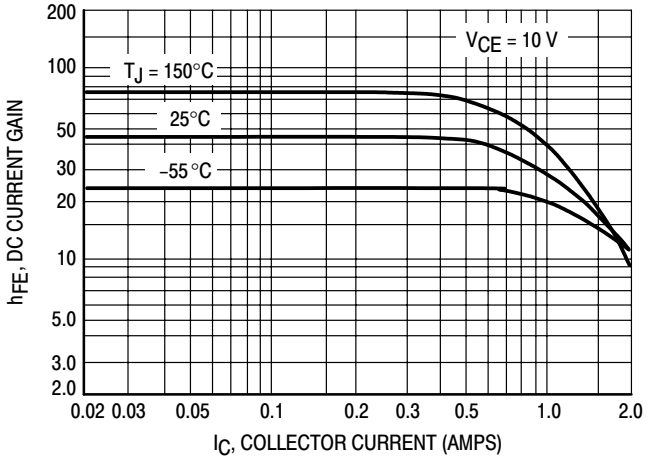


Figure 1. DC Current Gain

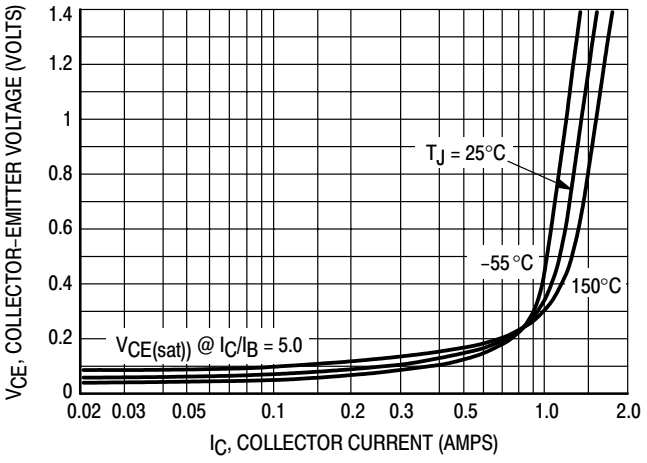


Figure 2. Collector−Emitter Saturation Voltage

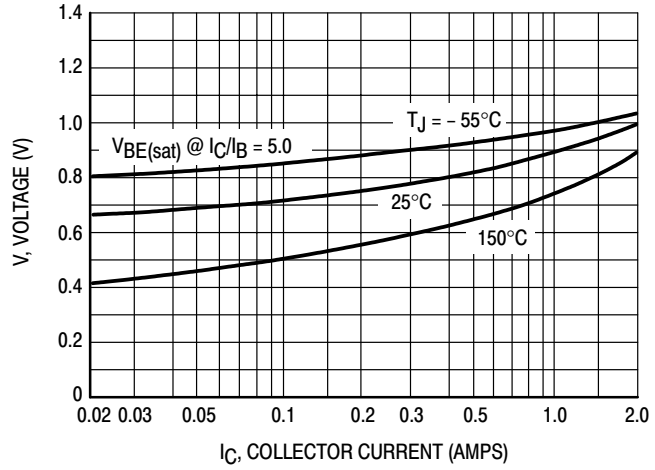


Figure 3. Base−Emitter Voltage

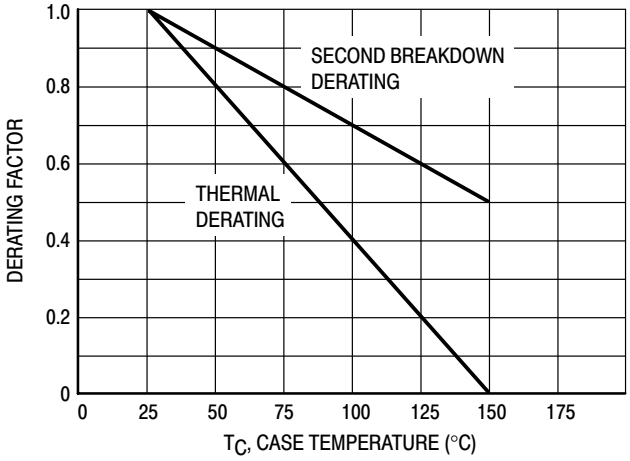


Figure 4. Normalized Power Derating

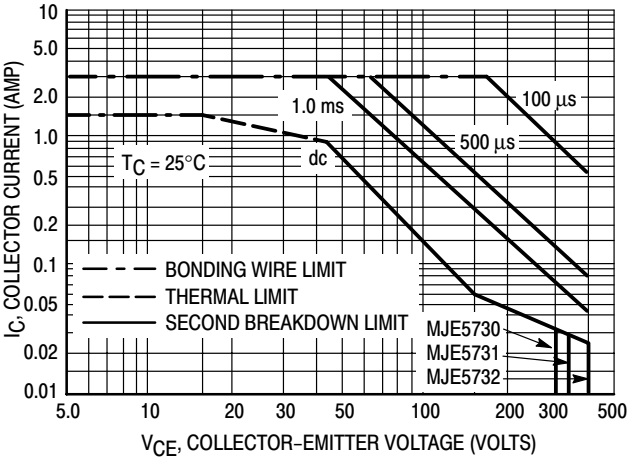


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

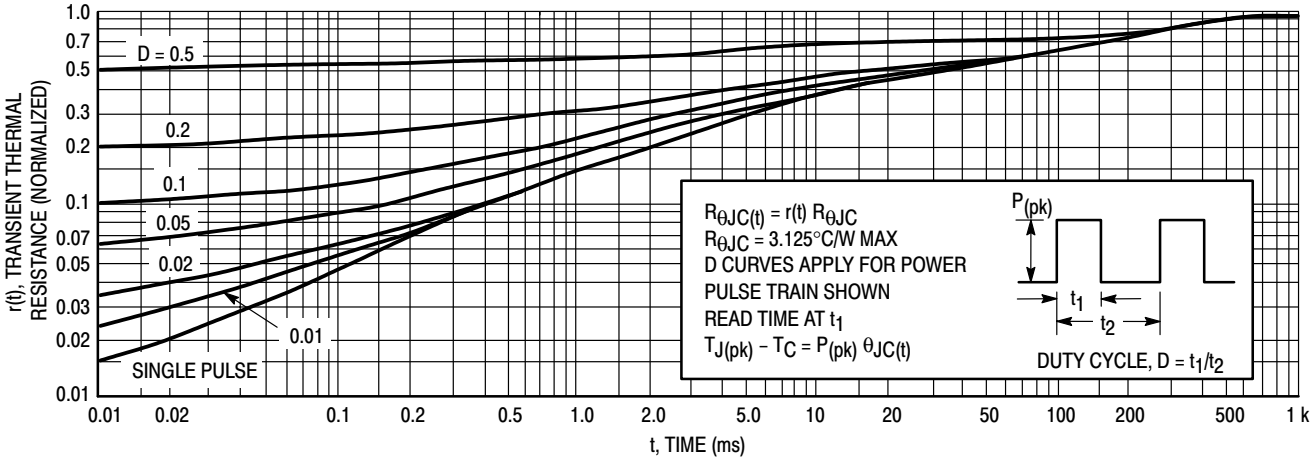


Figure 6. Thermal Response

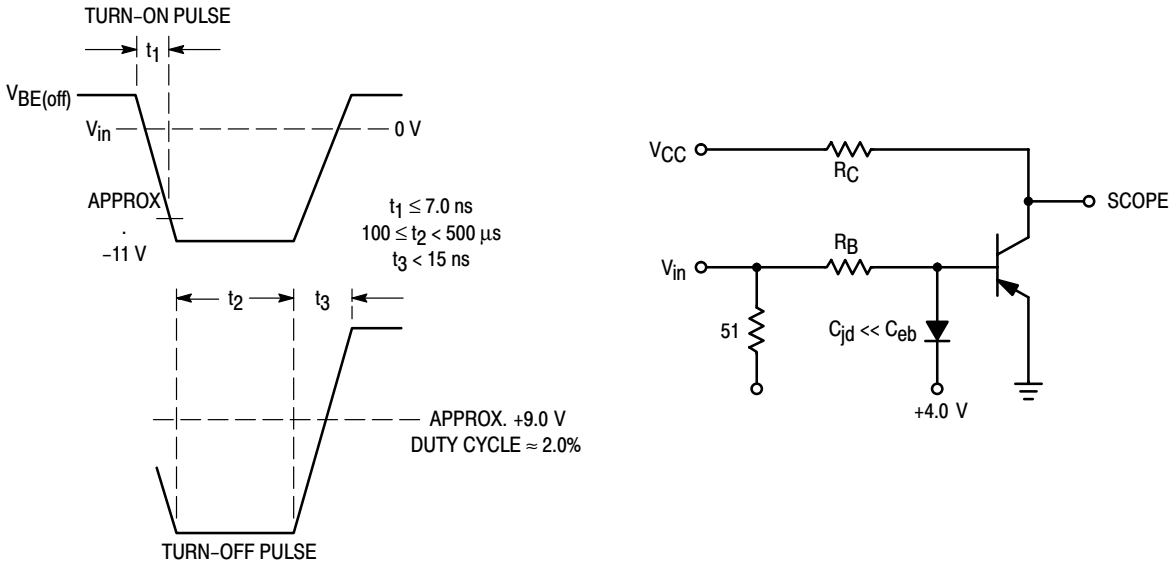


Figure 7. Switching Time Equivalent Circuit

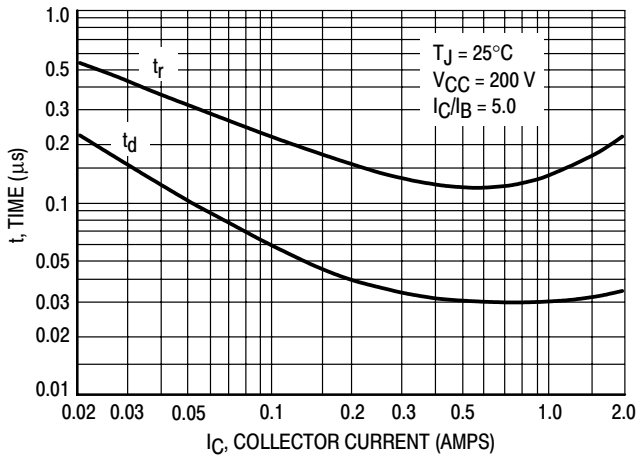


Figure 8. Turn−On Resistive Switching Times

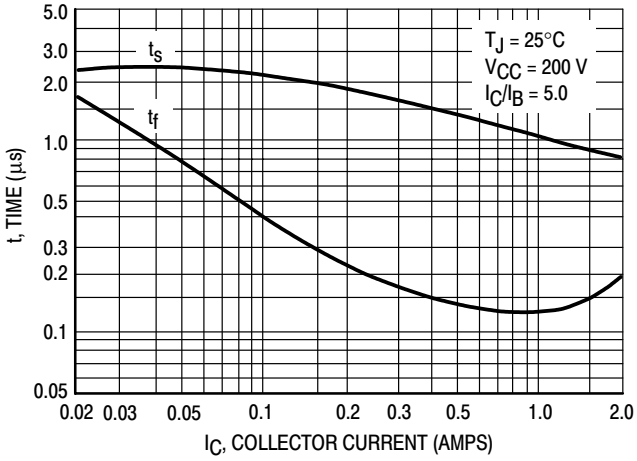
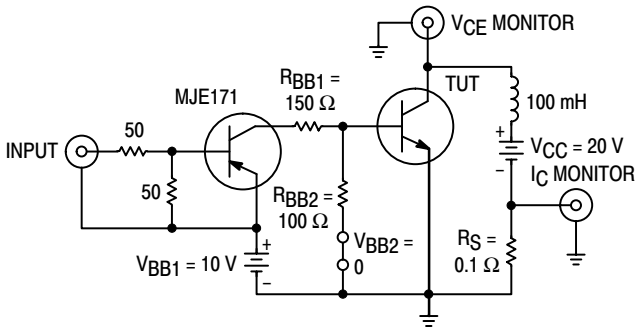


Figure 9. Resistive Turn−Off Switching Times

Test Circuit



Voltage and Current Waveforms

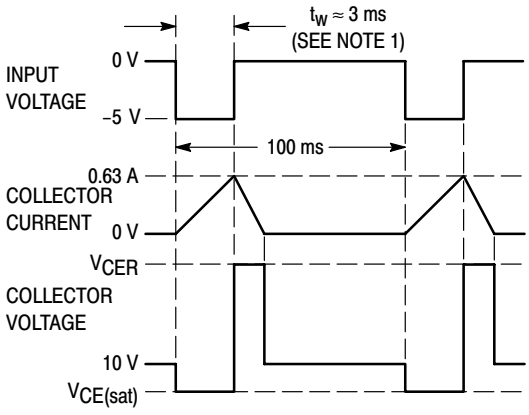


Figure 10. Inductive Load Switching

NPN Silicon Power Darlington Transistors

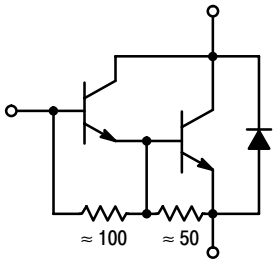
MJE5740
MJE5742*

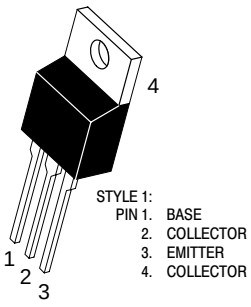
*ON Semiconductor Preferred Device

The MJE5740 and MJE5742 Darlington transistors are designed for high−voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

POWER DARLINGTON TRANSISTORS
8 AMPERES
300, 400 VOLTS
80 WATTS





CASE 221A−06
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5740	MJE5742	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector−Emitter Voltage	V_{CEV}	600	800	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current − Continuous − Peak (1)	I_C I_{CM}	8 16		Adc
Base Current − Continuous − Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2 16		 Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 80 640		 Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle = 10%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 5
Publication Order Number:
MJE5740/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector−Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	MJE5740 MJE5742	$V_{CEO(sus)}$	300 400	− −	− −	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	− −	− −	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	−	−	75	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 7			

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (3)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5 Vdc) (I_C = 4 Adc, V_{CE} = 5 Vdc)		h_{FE}	50 200	100 400	− −	−
Collector−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	− − −	− − −	2 3 2.2	Vdc
Base−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	− − −	− − −	2.5 3.5 2.4	Vdc
Diode Forward Voltage (4) (I_F = 5 Adc)		V_f	−	−	2.5	Vdc
SWITCHING CHARACTERISTICS						
Typical Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, $I_{C(pk)}$ = 6 A I_{B1} = I_{B2} = 0.25 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	−	0.04	−	μs
Rise Time		t_r	−	0.5	−	μs
Storage Time		t_s	−	8	−	μs
Fall Time		t_f	−	2	−	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	($I_{C(pk)}$ = 6 A, $V_{CE(pk)}$ = 250 Vdc I_{B1} = 0.06 A, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	−	4	−	μs
Crossover Time		t_c	−	2	−	μs

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%. (continued)

(3) Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.

(4) The internal Collector−to−Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

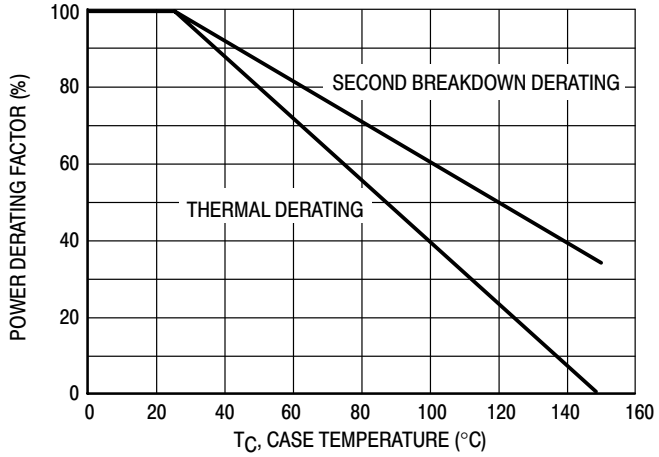


Figure 11. Power Derating

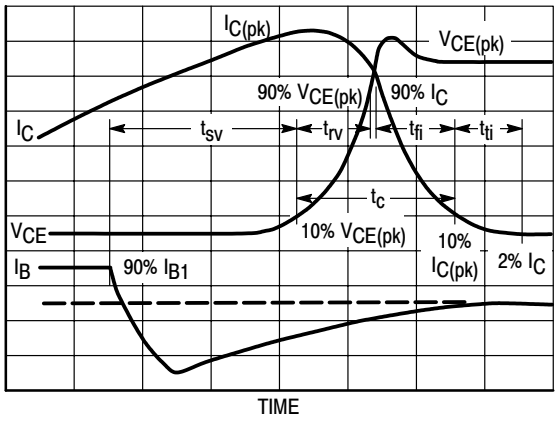


Figure 12. Inductive Switching Measurements

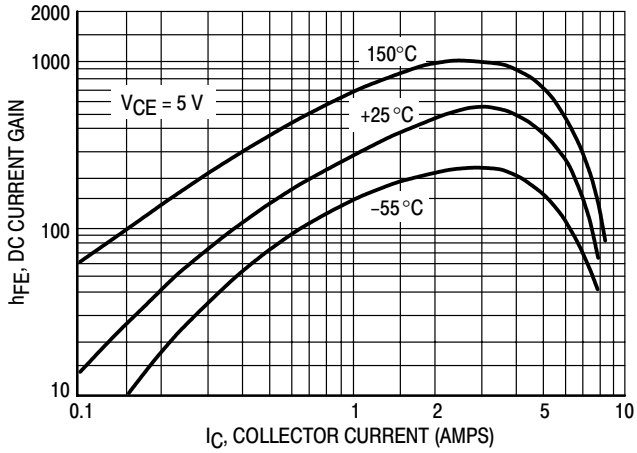


Figure 13. DC Current Gain

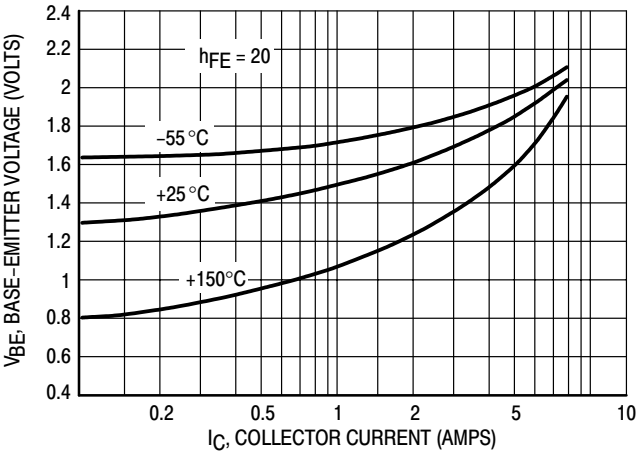
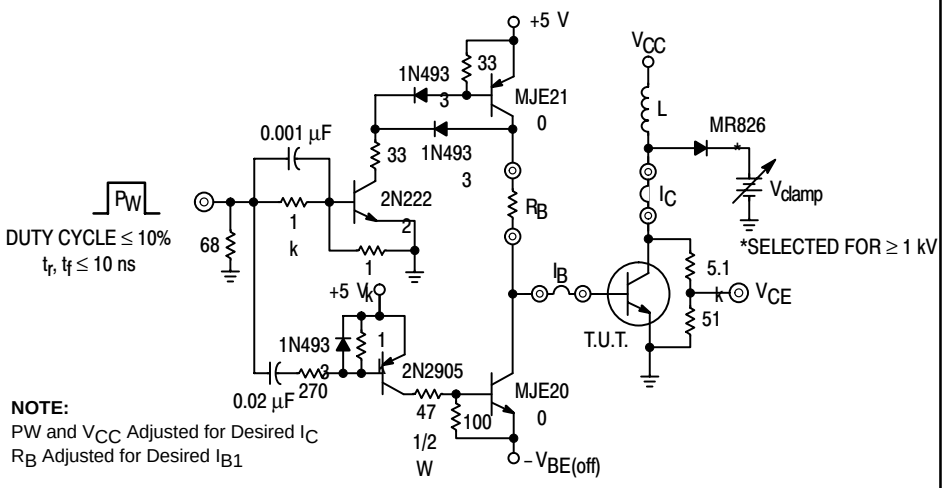
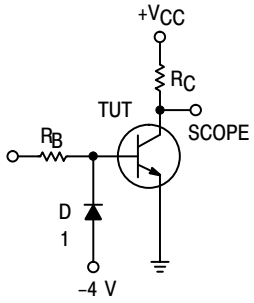
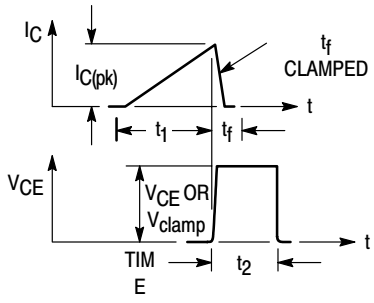
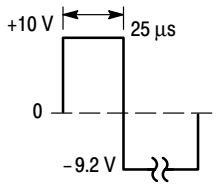


Figure 14. Base−Emitter Voltage

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~16 TURNS) #16 GAP FOR 200 μH/20 A L_{coil} = 200 μH V_{CC} = 30 V $V_{CE(pk)}$ = 250 Vdc $I_{C(pk)}$ = 6 A	V_{CC} = 250 V D1 = 1N5820 OR EQUIV.
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ TEST EQUIPMENT SCOPE–TEKTRONICS 475 OR EQUIVALENT	 t_r, t_f < 10 ns DUTY CYCLE = 1% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

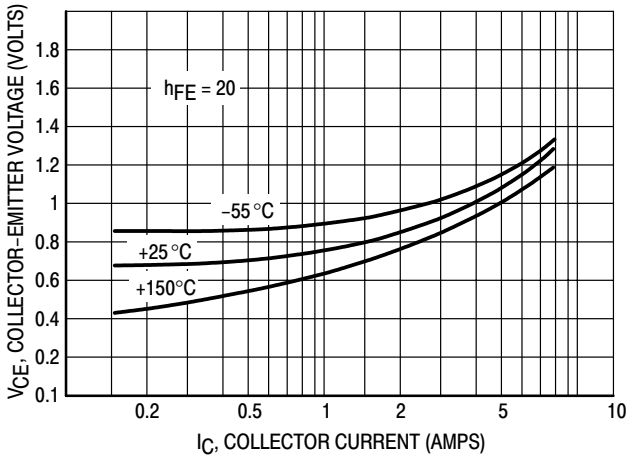


Figure 15. Inductive Switching Measurements

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 11.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

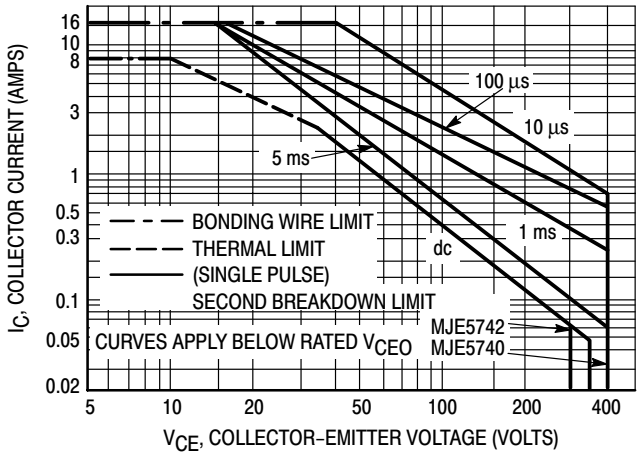


Figure 16. Forward Bias Safe Operating Area

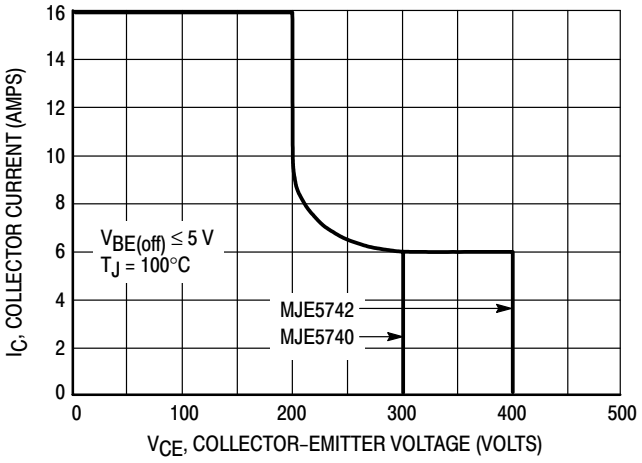


Figure 17. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

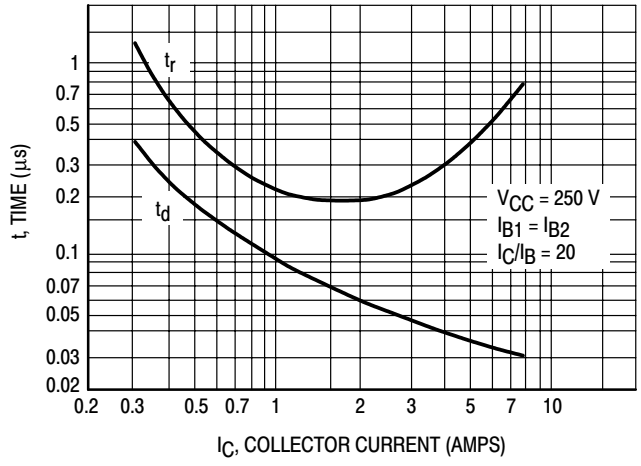


Figure 18. Turn−On Time

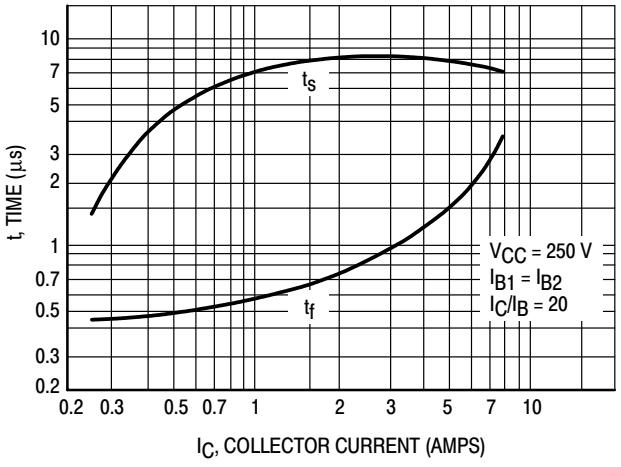


Figure 19. Turn−Off Time

SWITCHMODE™ Series PNP Silicon Power Transistors

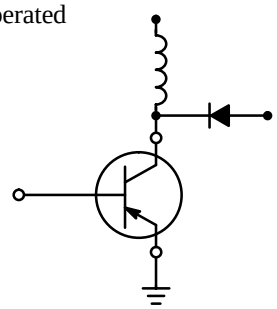
MJE5850
MJE5851*
MJE5852*

*ON Semiconductor Preferred Device

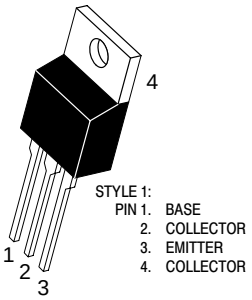
The MJE5850, MJE5851 and the MJE5852 transistors are designed for high−voltage, high−speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated SWITCHMODE applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn−Off Times
100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)
Operating Temperature Range −65 to +150°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



8 AMPERE
PNP SILICON
POWER TRANSISTORS
300, 350, 400 VOLTS
80 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5850	MJE5851	MJE5852	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector−Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 1 6			Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.640			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 3
Publication Order Number:
MJE5850/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE5850 MJE5851 MJE5852	$V_{CEO(sus)}$	300 350 400	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 13			
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc) (I_C = 5.0 Adc, V_{CE} = 5 Vdc)		h_{FE}	 15 5	 — —	 — —	—
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 3.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2.0 5.0 2.5	Vdc
Base−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	270	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.100	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	μs
Fall Time		t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	μs
Crossover Time		t_c	—	0.4	1.5	μs
Fall Time		t_{fi}	—	0.1	—	μs
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.125	—	μs
Fall Time		t_{fi}	—	0.1	—	μs

*Pulse Test: PW = 300 μs. Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

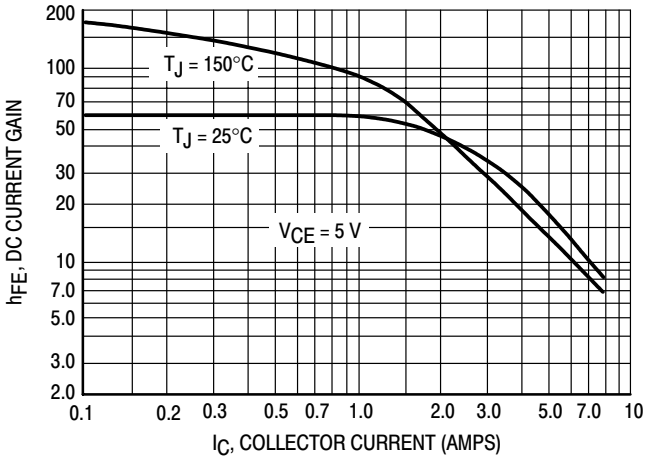


Figure 1. DC Current Gain

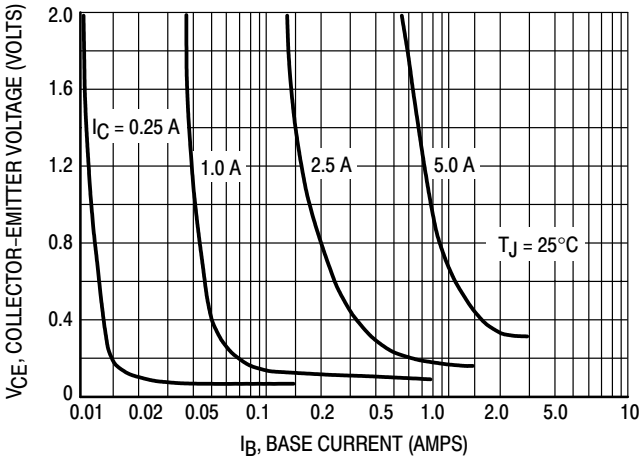


Figure 2. Collector Saturation Region

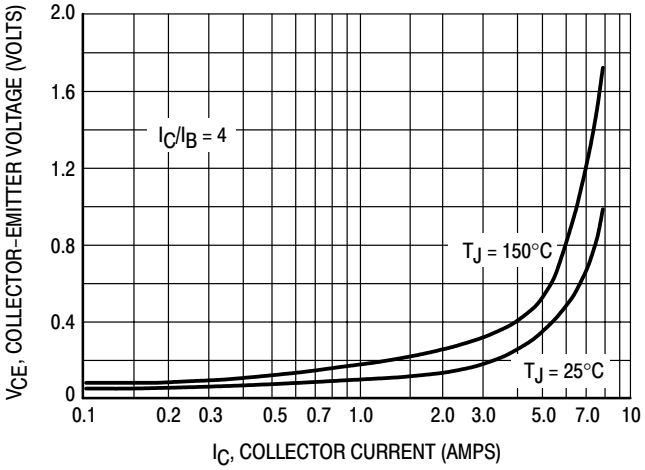


Figure 3. Collector−Emitter Saturation Voltage

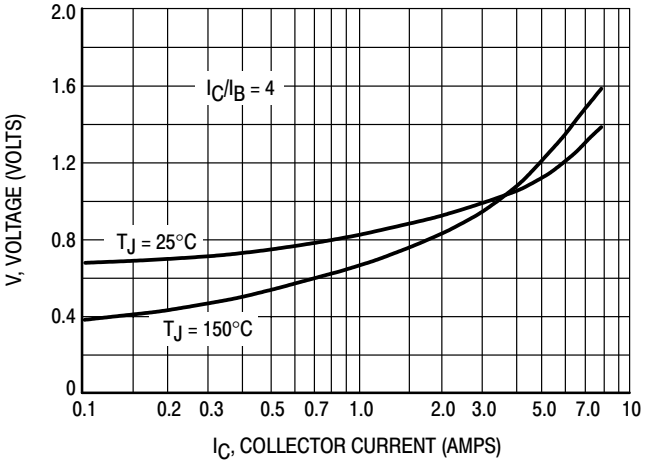


Figure 4. Base−Emitter Voltage

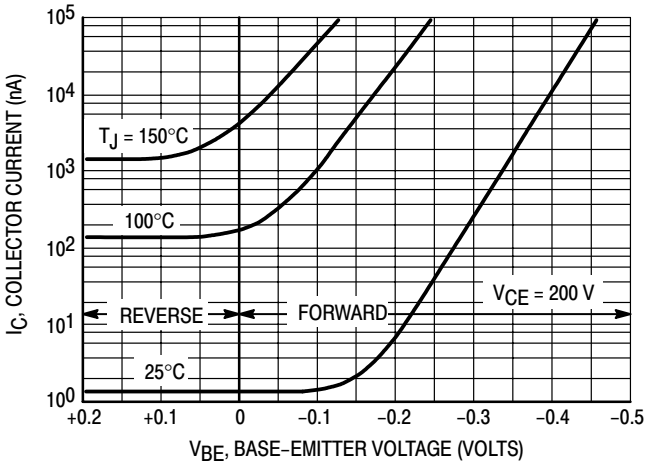


Figure 5. Collector Cutoff Region

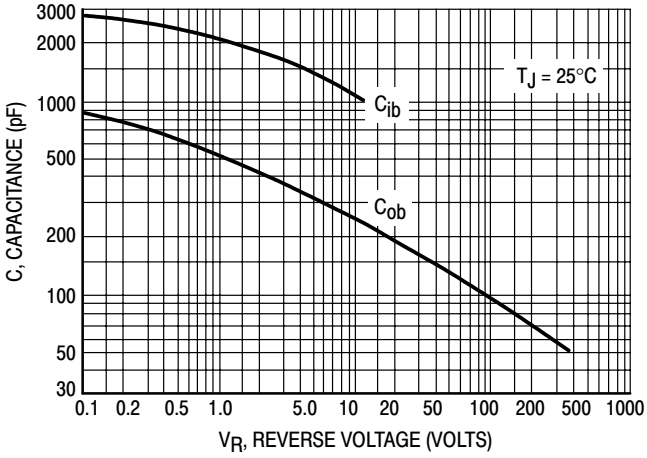


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	−10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	+V, 50 µF, 0.0025 µF, 0.2 µF, 500 Ω 1/2 W, 0.1 µF, MJE15029, 1N4934, INPUT, 0.0033 µF, 1 Ω 2 W, MJE15028, 50 Ω 2 W, −V adjusted to obtain desired I_{B1}, +V adjusted to obtain desired $V_{BE(off)}$	**TURN−ON TIME** I_{B1} adjusted to obtain the forced h_{FE} desired **TURN−OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** TUT, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, IN-PUT, SEE ABOVE FOR DETAILED CONDITIONS, V_{clamp}, V_{CC}, RS = 0.1 Ω **OUTPUT WAVEFORMS** I_C, I_{CM}, t_f, Clamped, t_1, t_f, V_{CE}, V_{CEM}, V_{clamp}, t, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** TUT, 1, 2, R_L, V_{CC}

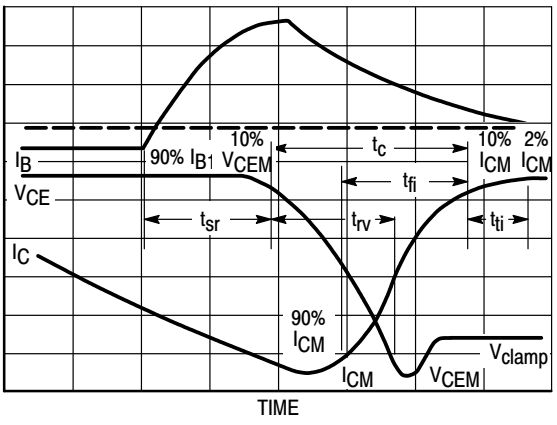


Figure 7. Inductive Switching Measurements

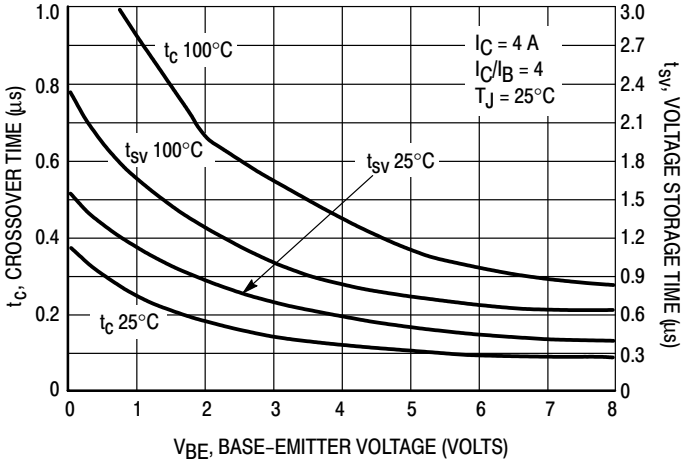


Figure 8. Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10−90% V_{CEM}

t_{fi} = Current Fall Time, 90−10% I_{CM}

t_{ti} = Current Tail, 10−2% I_{CM}

t_c = Crossover Time,10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN−222A:

$P_{SWT} = 1/2\ V_{CC} I_C(t_c) f$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

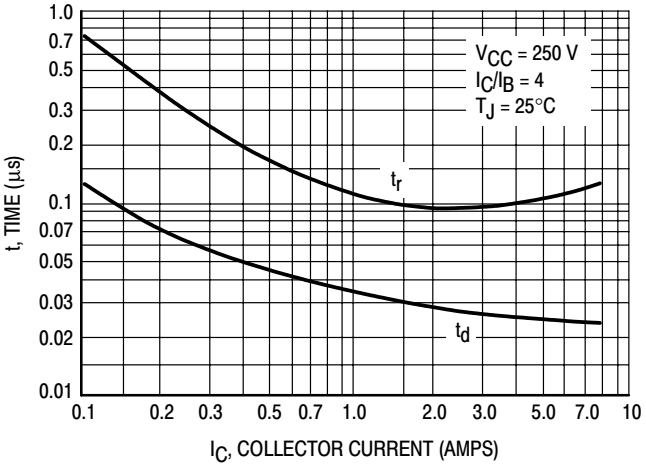


Figure 9. Turn−On Switching Times

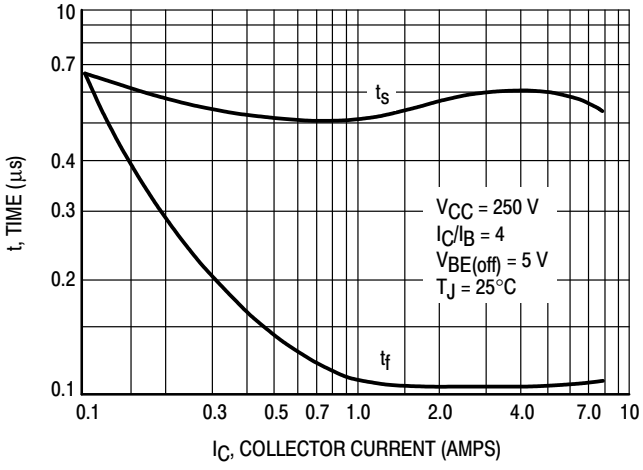


Figure 10. Turn−Off Switching Time

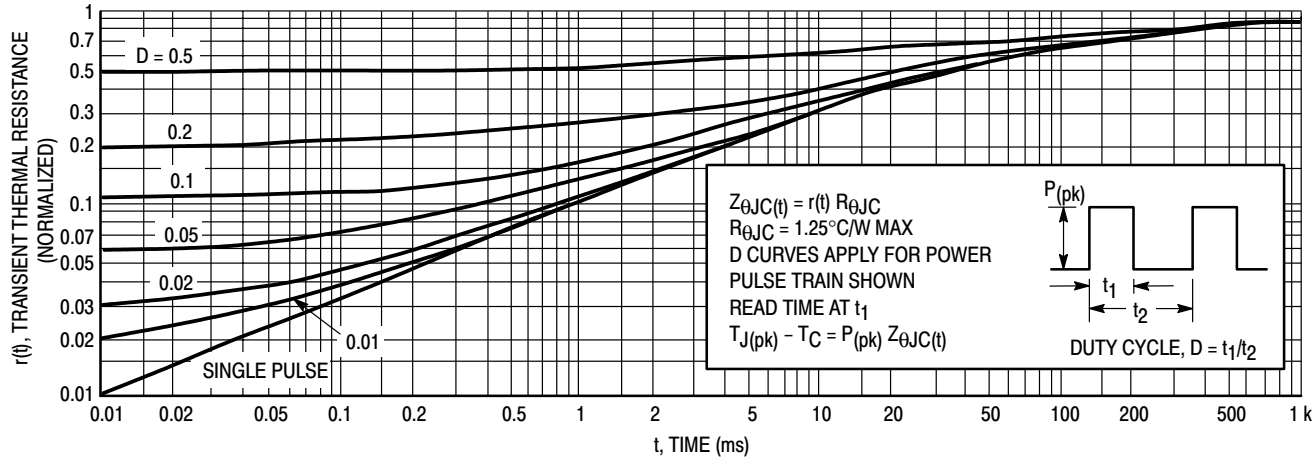


Figure 11. Typical Thermal Response [$Z_{\theta JC}(t)$]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

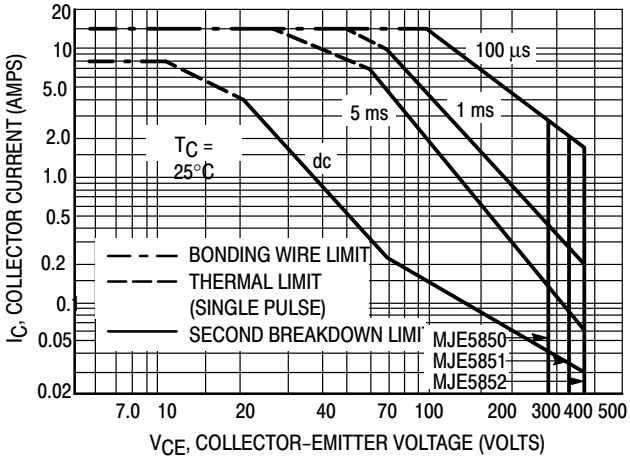


Figure 12. Maximum Forward Bias Safe Operating Area

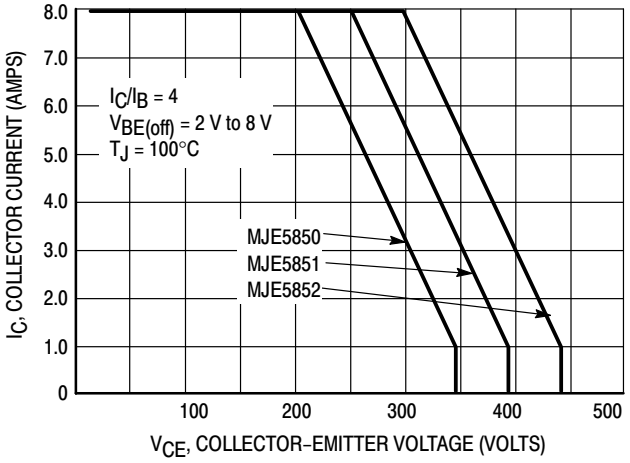


Figure 13. RBSOA, Maximum Reverse Bias Safe Operating Area

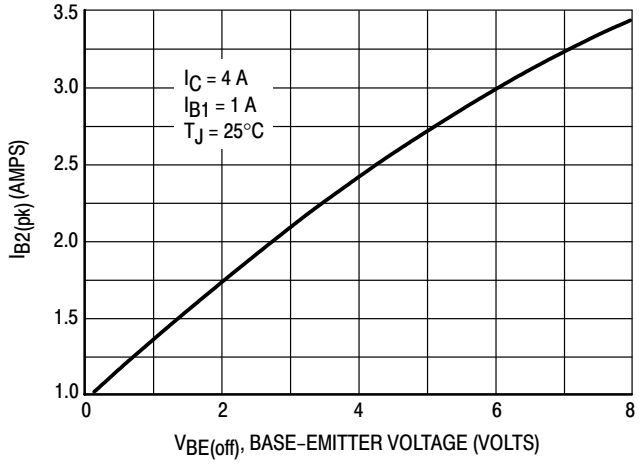


Figure 14. Peak Reverse Base Current

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current condition allowable during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

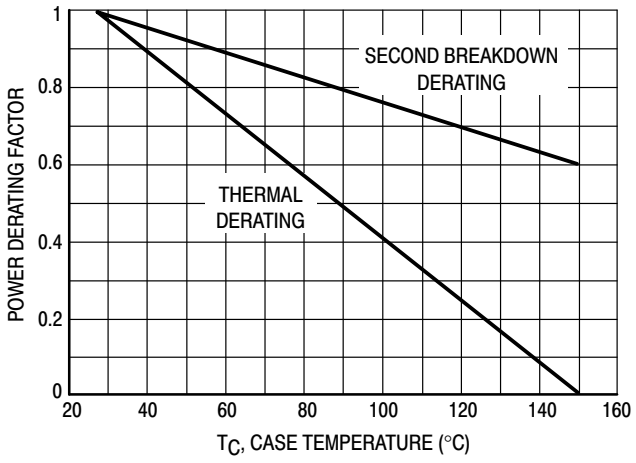


Figure 15. Forward Bias Power Derating

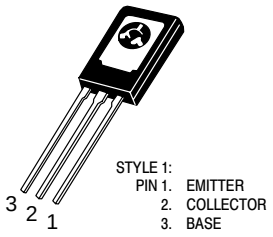
PNP
MJE700
MJE702
MJE703
NPN
MJE800
MJE802
MJE803

Plastic Darlington Complementary Silicon Power Transistors

. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Monolithic Construction with Built−in Base−Emitter Resistors to Limit Leakage Multiplication
- Choice of Packages —
  MJE700 and MJE800 series

4.0 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON 40 WATT 50 WATT



CASE 77−08 TO−225AA TYPE MJE700−703 MJE800−803

MAXIMUM RATINGS

Rating	Symbol	MJE700 MJE800	MJE702 MJE703 MJE802 MJE803	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
		CASE 77		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case CASE 77 TO−220	$R_{\theta JC}$	 3.13 2.50	°C/W

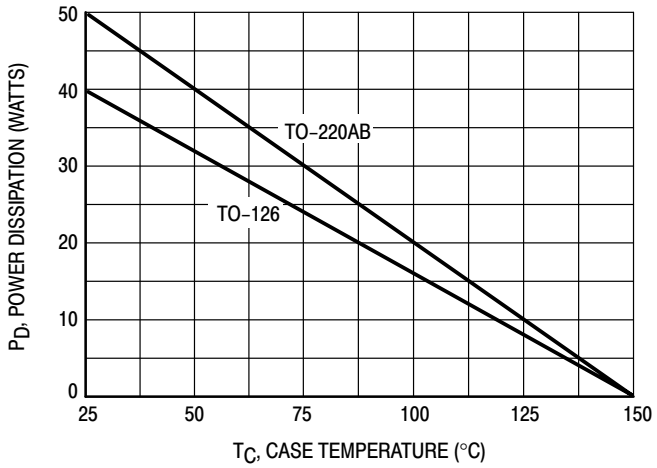


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (1)	MJE700, MJE800	$V_{(BR)CEO}$	60	—	Vdc
(I_C = 50 mAdc, I_B = 0)	MJE702, MJE703, MJE802, MJE803		80	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 60 Vdc, I_B = 0)	MJE700, MJE800		—	100	
(V_{CE} = 80 Vdc, I_B = 0)	MJE702, MJE703, MJE802, MJE803		—	100	
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0)		I_{CBO}	—	100	μAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)			—	500	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700, MJE702, MJE800, MJE802		750	—	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE703, MJE803		750	—	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		100	—	
Collector−Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 30 mAdc)	MJE700, MJE702, MJE800, MJE802		—	2.5	
(I_C = 2.0 Adc, I_B = 40 mAdc)	MJE703, MJE803		—	2.8	
(I_C = 4.0 Adc, I_B = 40 mAdc)	All devices		—	3.0	
Base−Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700, MJE702, MJE800, MJE802		—	2.5	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE703, MJE803		—	2.5	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		—	3.0	
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

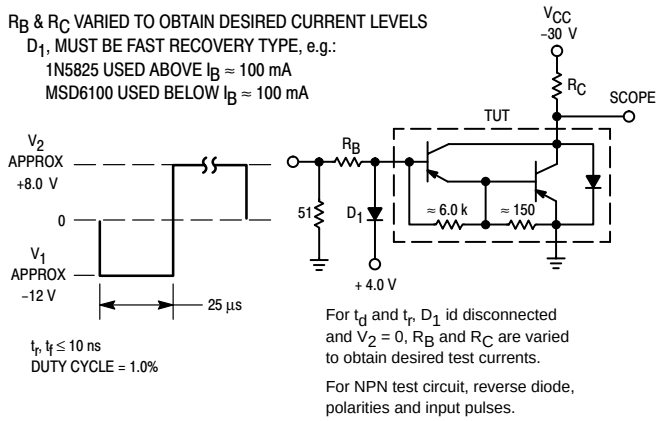


Figure 2. Switching Times Test Circuit

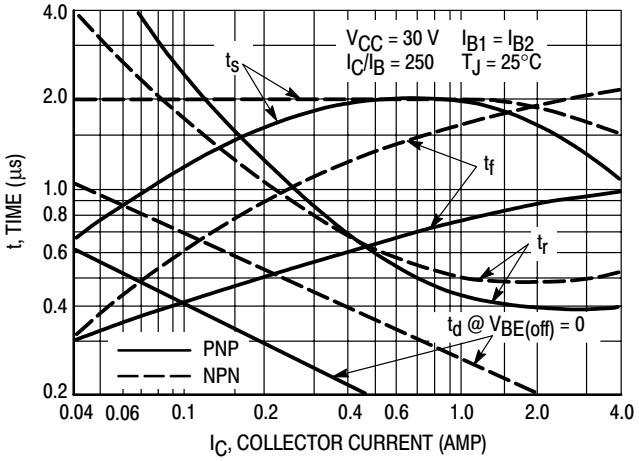


Figure 3. Switching Times

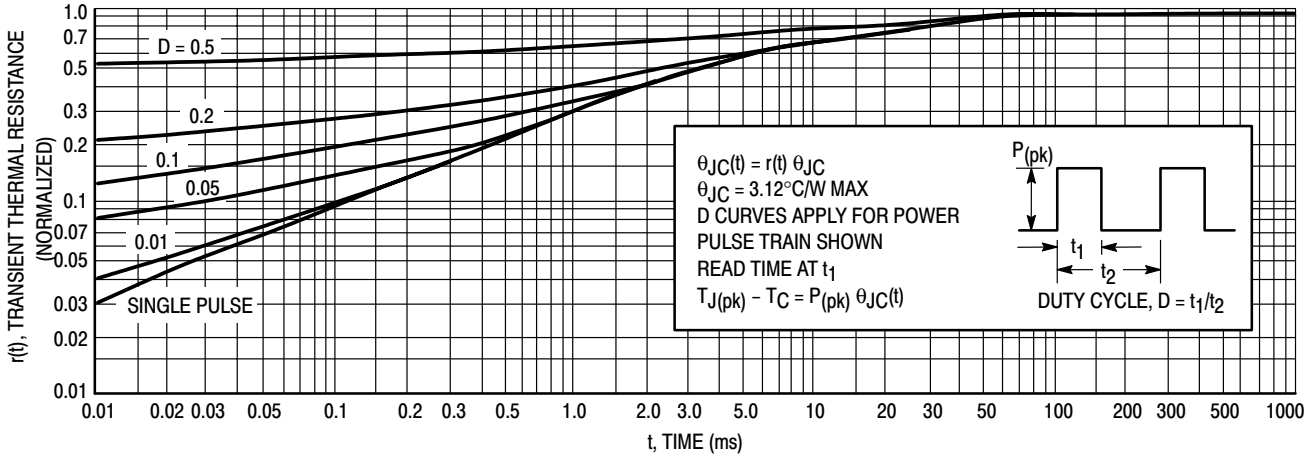


Figure 4. Thermal Response (MJE700, 800 Series)

ACTIVE−REGION SAFE−OPERATING AREA

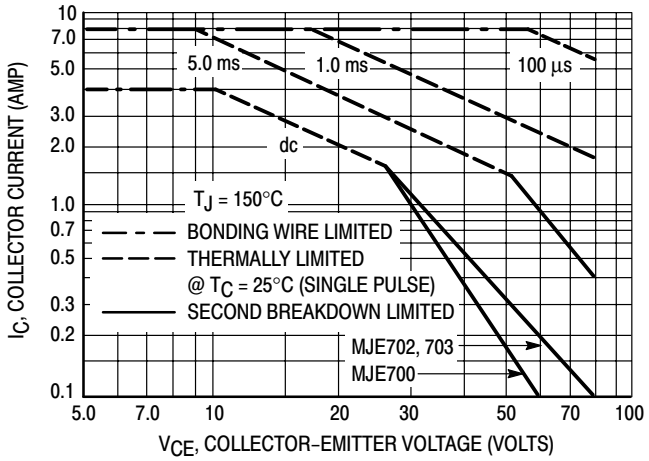


Figure 5. MJE700 Series

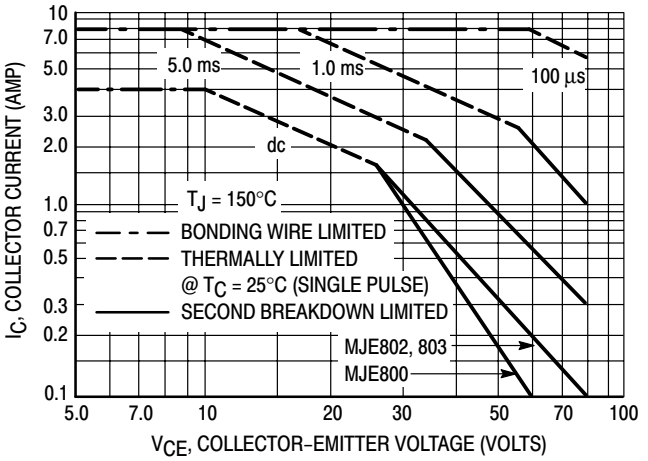
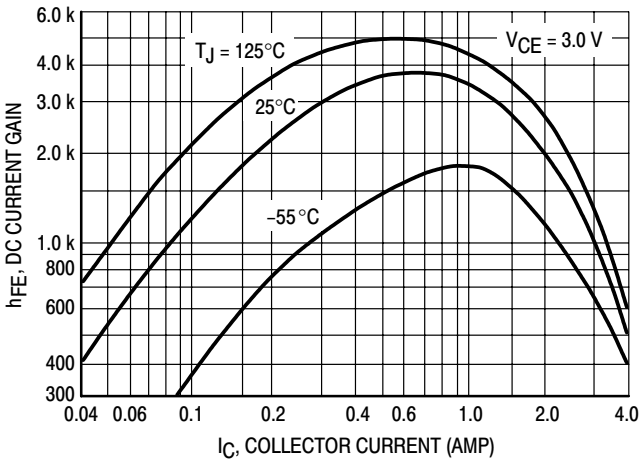


Figure 6. MJE800 Series

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 are based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PNP
MJE700 Series



NPN
MJE800 Series

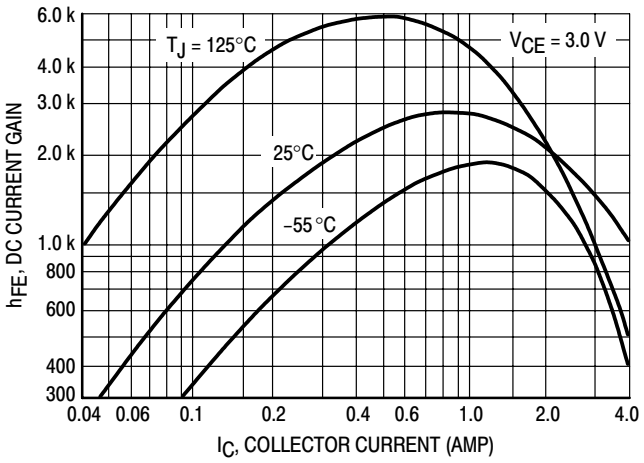
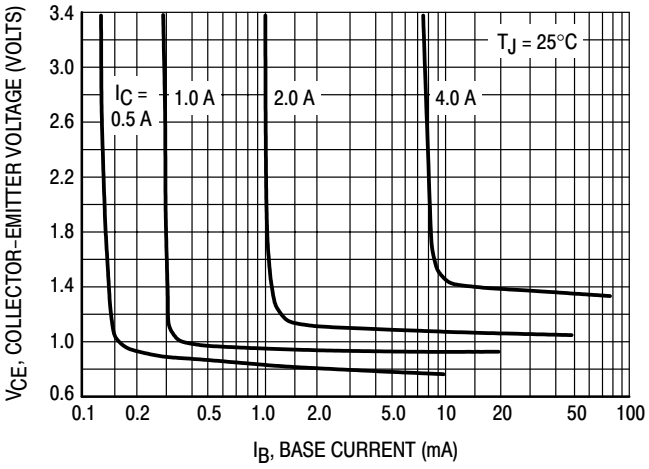


Figure 7. DC Current Gain



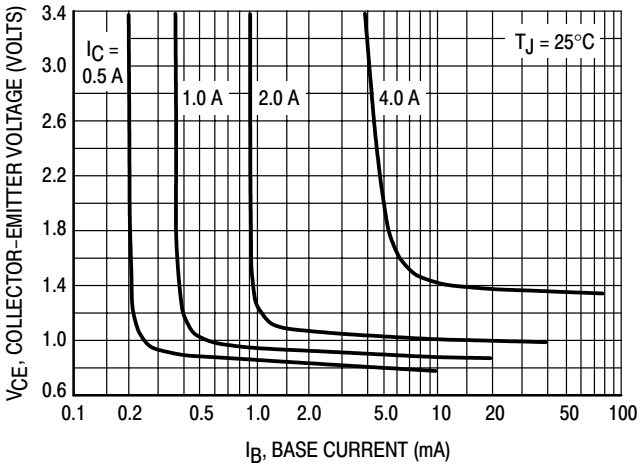
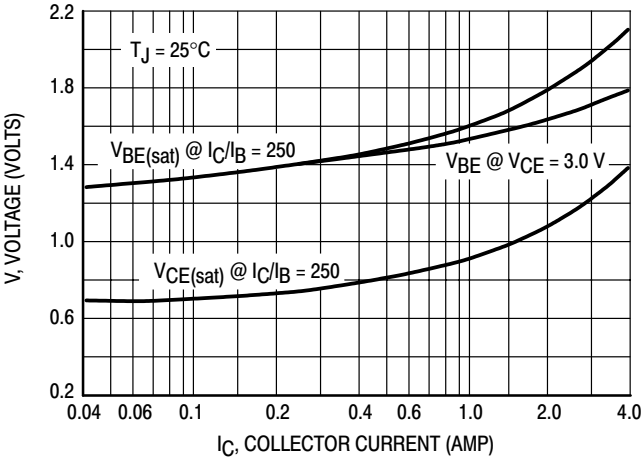


Figure 8. Collector Saturation Region



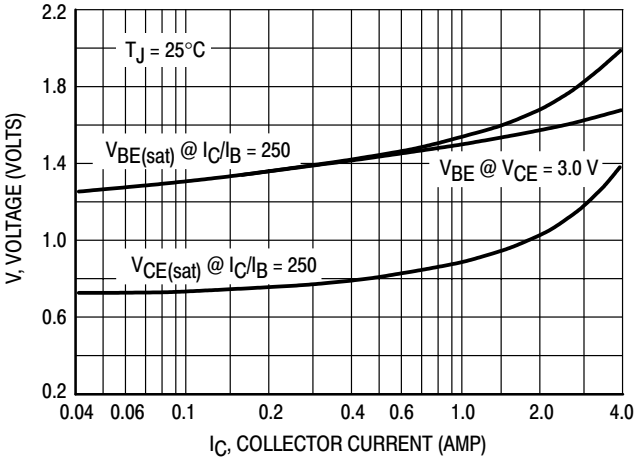


Figure 9. “On” Voltages

Complementary Power Darlingtons

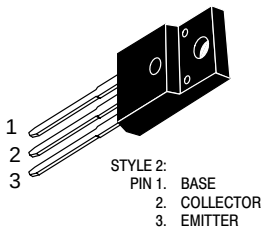
For Isolated Package Applications

NPN
MJF122
PNP
MJF127

COMPLEMENTARY SILICON POWER DARLINGTONS 5 AMPERES 100 VOLTS 30 WATTS

Designed for general−purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP122 and TIP127
- 100 $V_{CEO(sus)}$
- 5 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 2000 (Min) @ I_C = 3 Adc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation



CASE 221D−02
TO−220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage		V_{CEO}	100	Vdc
Collector−Base Voltage		V_{CB}	100	Vdc
Emitter−Base Voltage		V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 14 Test No. 2 Per Fig. 15 Test No. 3 Per Fig. 16	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous Peak		I_C	5 8	Adc
Base Current		I_B	0.12	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	30 0.24	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−65 to +150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.1	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)		I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 3 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 2000	— —	—
Collector−Emitter Saturation Voltage (I_C = 3 Adc, I_B = 12 mAdc) (I_C = 5 Adc, I_B = 20 mAdc)		$V_{CE(sat)}$	— —	2 3.5	Vdc
Base−Emitter On Voltage (I_C = 3 Adc, V_{CE} = 3 Vdc)		$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)		h_{fe}	4	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJF127 MJF122	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

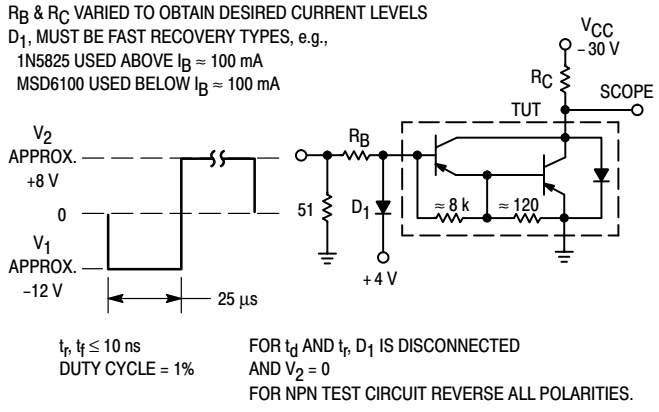


Figure 10. Switching Times Test Circuit

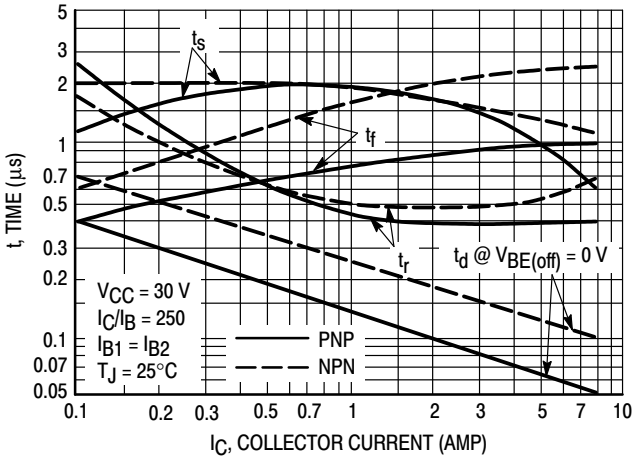


Figure 11. Typical Switching Times

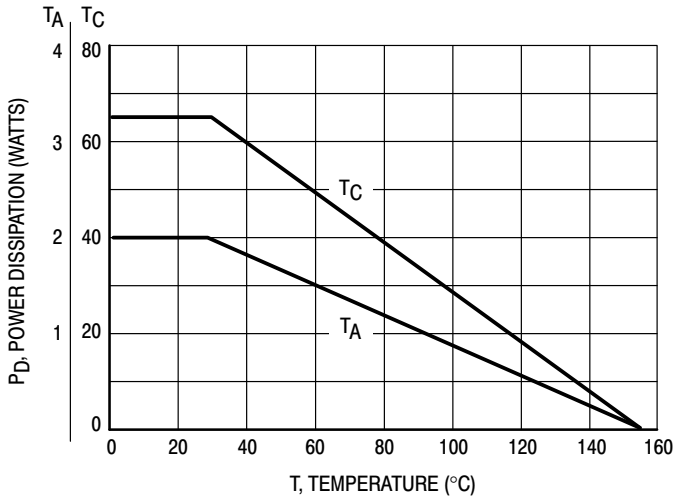


Figure 12. Maximum Power Derating

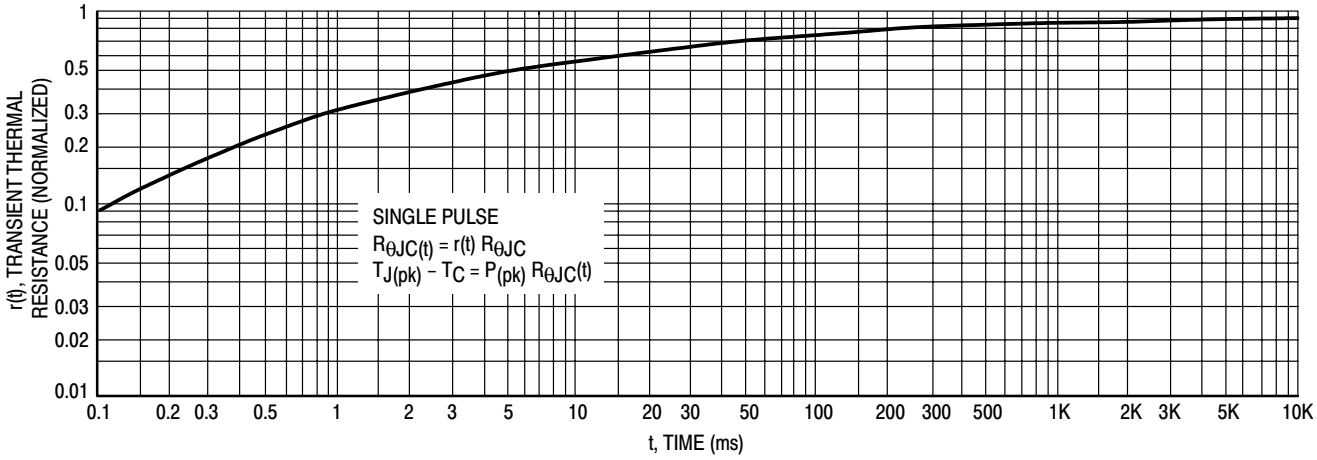


Figure 13. Thermal Response

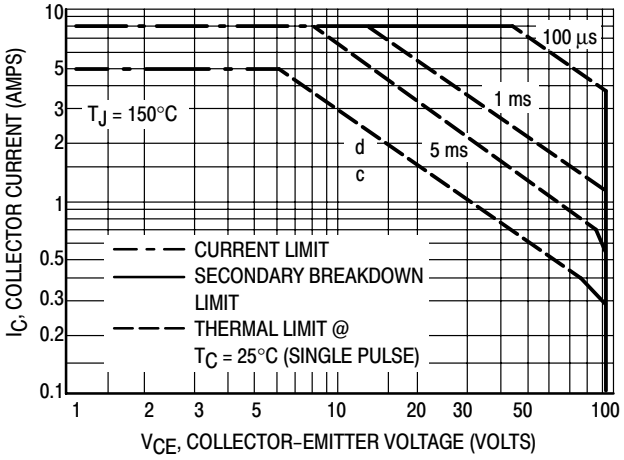


Figure 14. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

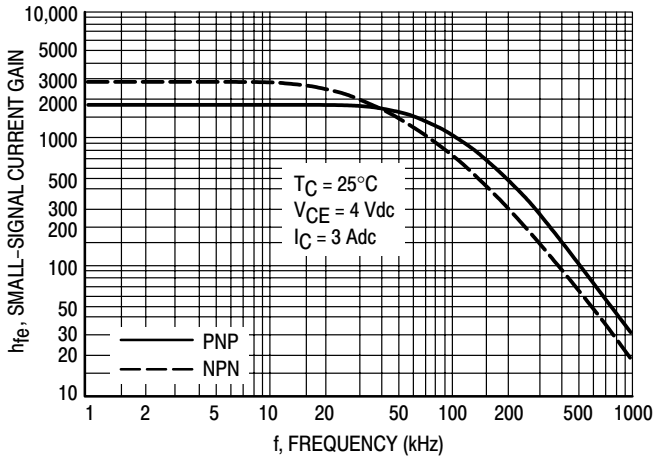


Figure 15. Typical Small−Signal Current Gain

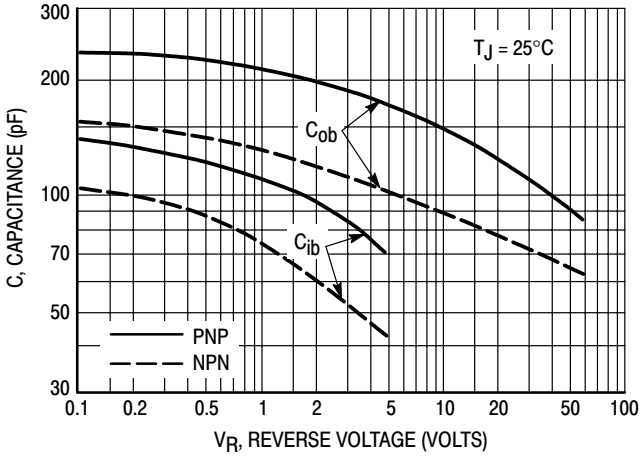
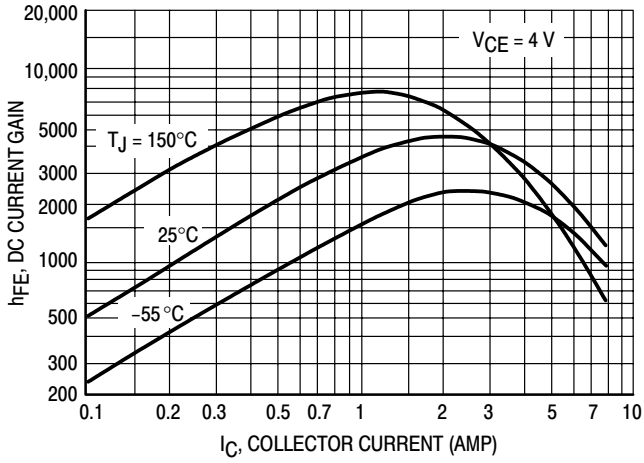


Figure 16. Typical Capacitance

NPN
MJF122



PNP
MJF127

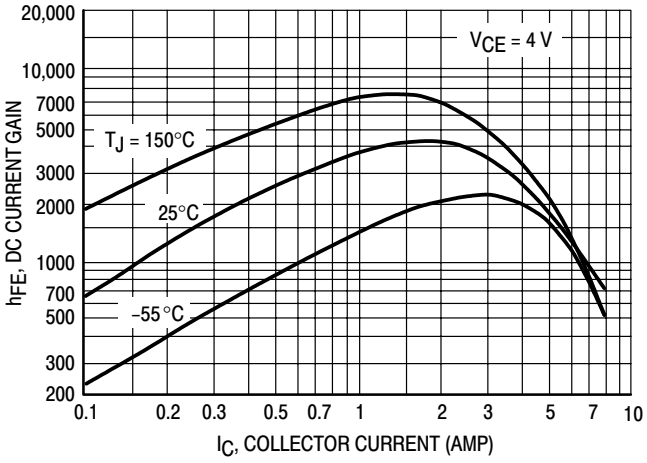
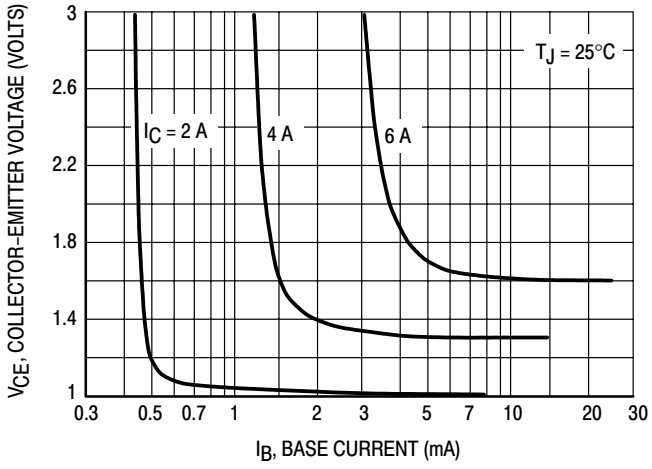


Figure 17. Typical DC Current Gain



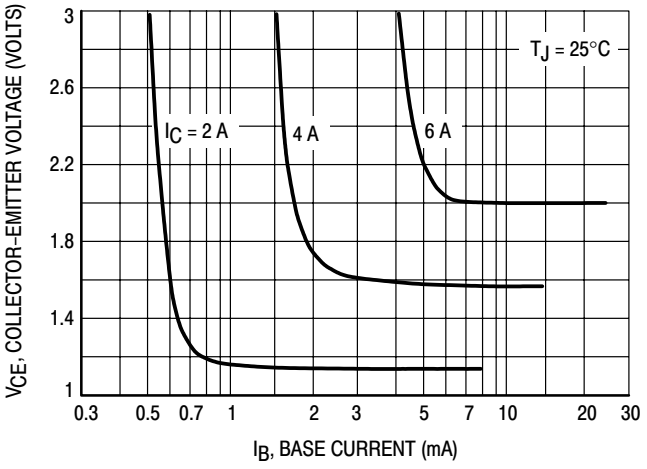
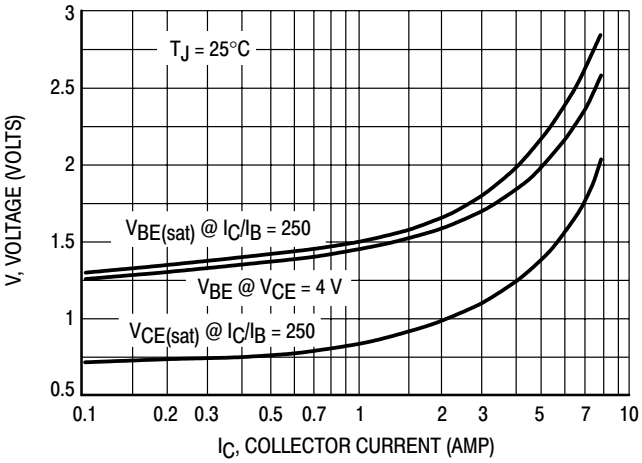


Figure 18. Typical Collector Saturation Region

NPN
MJF122



PNP
MJF127

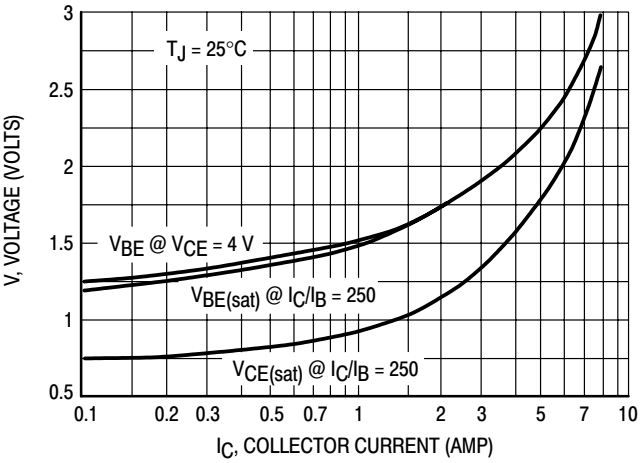
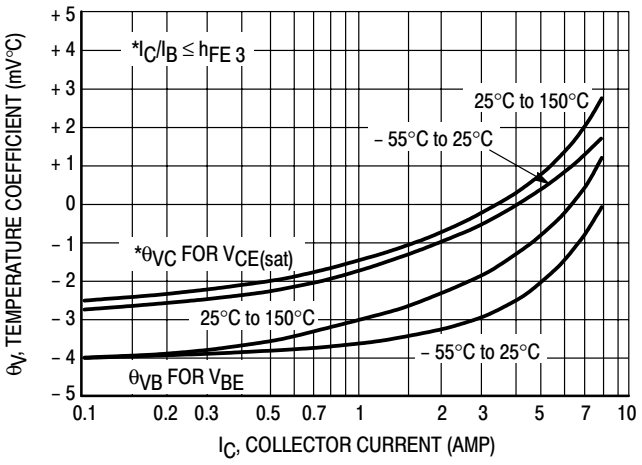


Figure 19. Typical “On” Voltages



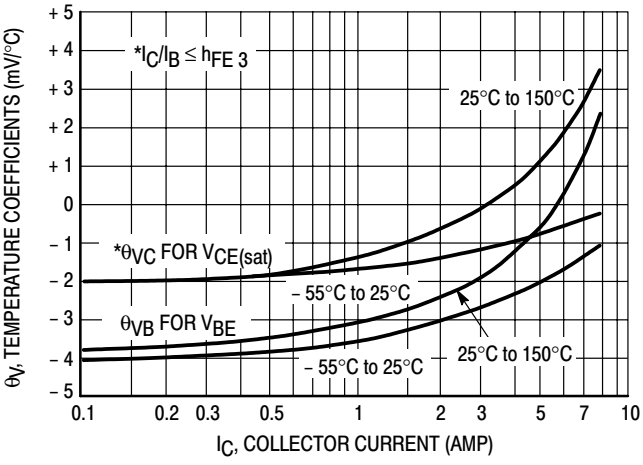
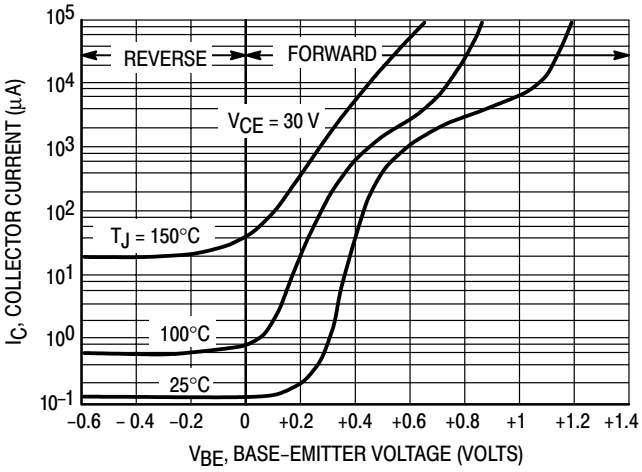


Figure 20. Typical Temperature Coefficients



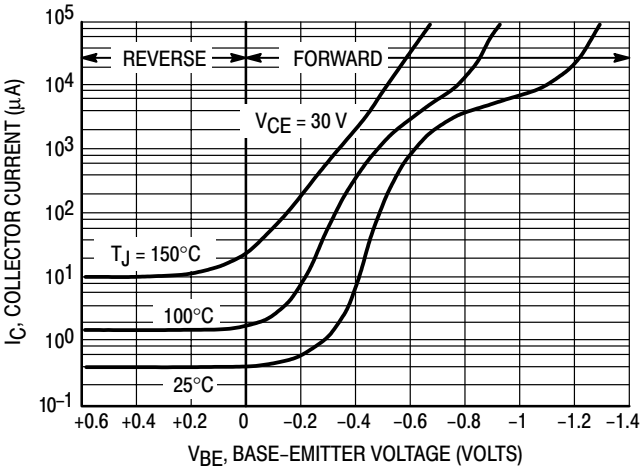
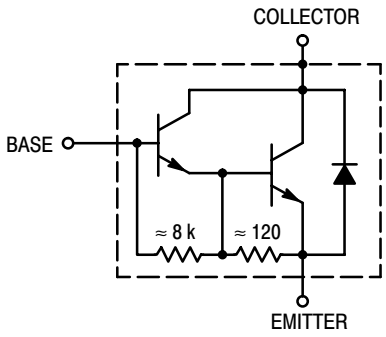


Figure 21. Typical Collector Cut−Off Region

NPN
MJF122



PNP
MJF127

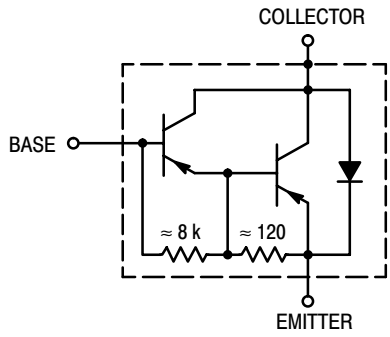


Figure 22. Darlington Schematic

TEST CONDITIONS FOR ISOLATION TESTS*

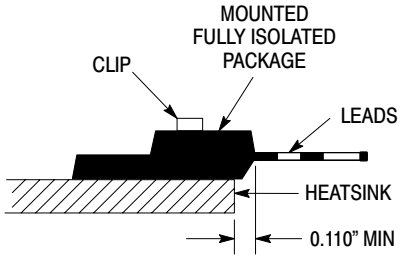


Figure 23. Clip Mounting Position for Isolation Test Number 1

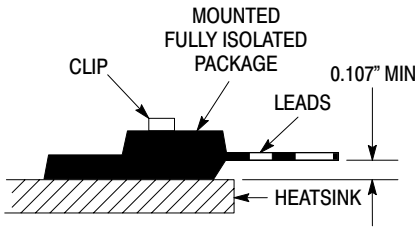


Figure 24. Clip Mounting Position for Isolation Test Number 2

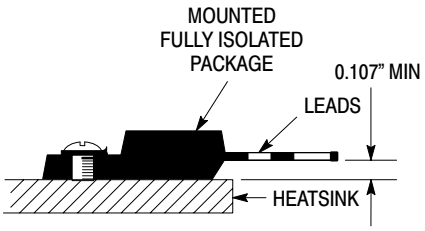


Figure 25. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

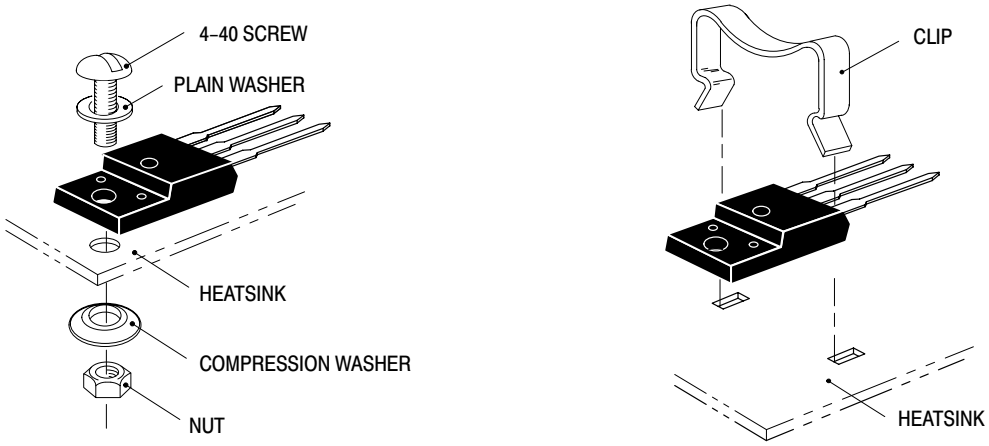


Figure 26. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Transistors

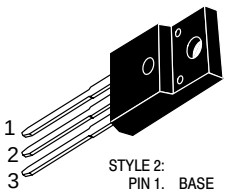
For Isolated Package Applications

NPN
MJF15030
PNP
MJF15031

COMPLEMENTARY SILICON POWER TRANSISTORS
8 AMPERES
150 VOLTS
36 WATTS

Designed for general−purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular MJE15030 and MJE15031
- 150 $V_{CEO(sus)}$
- 8 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain−Bandwidth Product
  f_T = 30 MHz (Min) @ I_C
  = 500 mAdc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation



STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 221D−02
TO−220 TYPE

April, 2002 − Rev. 3
Publication Order Number:
MJF15030/D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	150	Vdc
Collector−Base Voltage	V_{CB}	150	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 11 / Test No. 2 Per Fig. 12 / Test No. 3 Per Fig. 13	V_{ISOL}	4500 / 3500 / 1500	V_{RMS}
Collector Current — Continuous / — Peak	I_C	8 / 16	Adc
Base Current	I_B	2	Adc
Total Power Dissipation* @ T_C = 25°C / Derate above 25°C	P_D	36 / 0.29	Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2 / 0.016	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2 Vdc) / (I_C = 2 Adc, V_{CE} = 2 Vdc) / (I_C = 3 Adc, V_{CE} = 2 Vdc) / (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	40 / 40 / 40 / 20	— / — / — / —	—
DC Current Gain Linearity (V_{CE} from 2 V to 20 V, I_C from 0.1 A to 3 A) (NPN to PNP)	h_{FE}	Typ: 2 / 3		
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base−Emitter On Voltage (I_C = 1 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	1	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain−Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	—	MHz

NOTES:

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

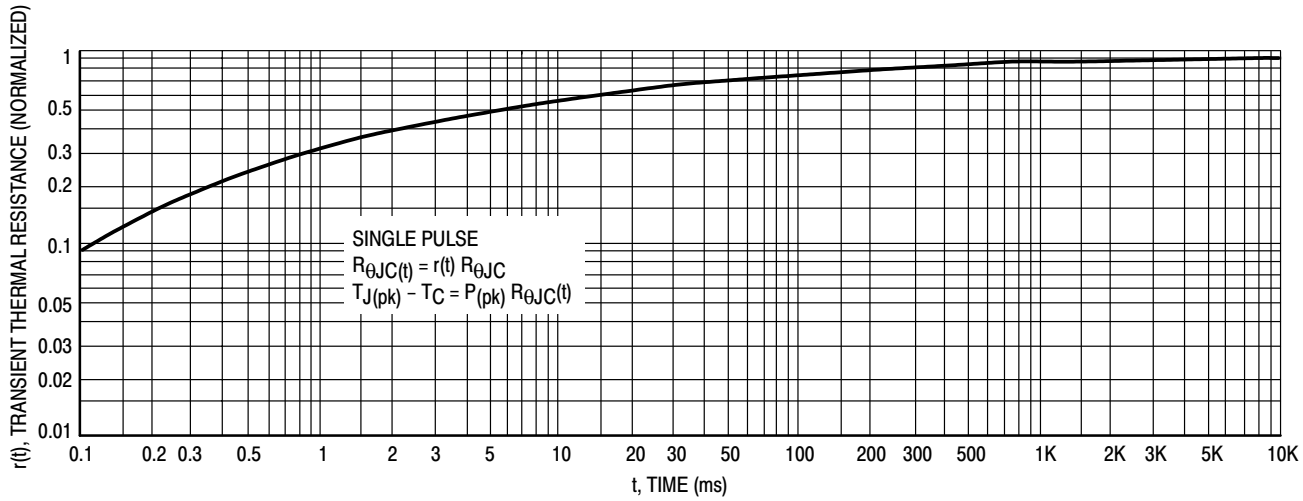


Figure 1. Thermal Response

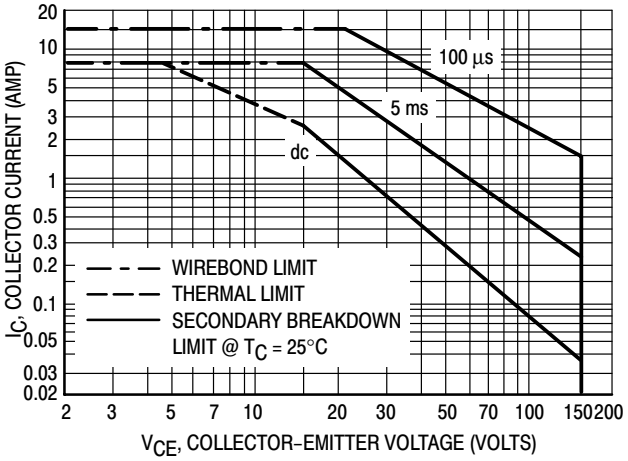


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

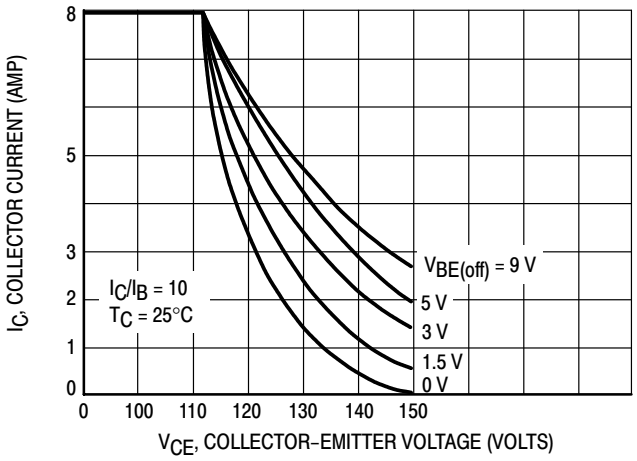


Figure 3. Reverse Bias Switching Safe Operating Area

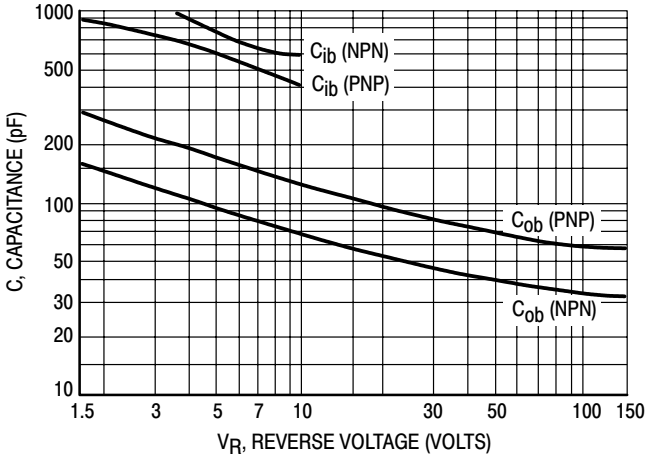


Figure 4. Capacitances

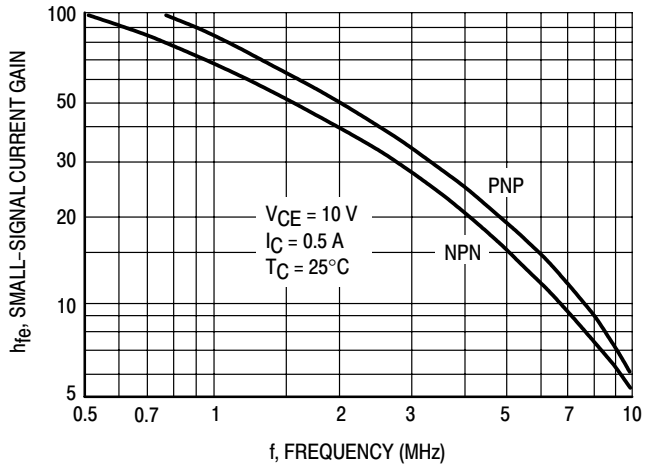


Figure 5. Small−Signal Current Gain

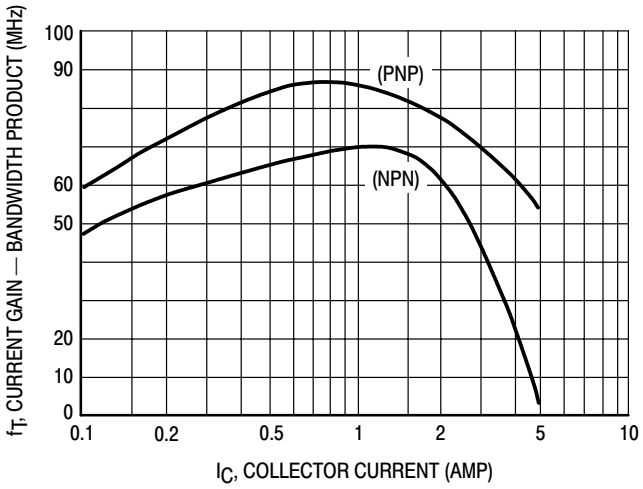


Figure 6. Current Gain — Bandwidth Product

DC CURRENT GAIN

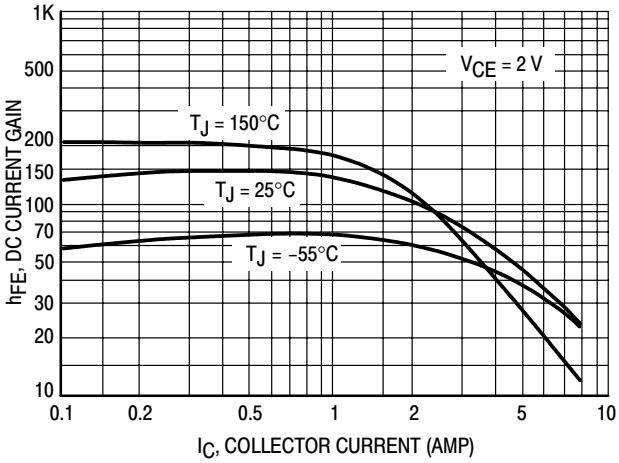


Figure 7a. MJF15030 NPN

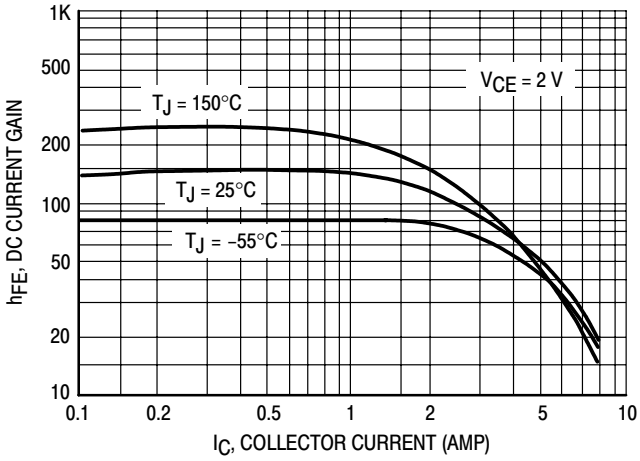


Figure 7b. MJF15031 PNP

“ON” VOLTAGE

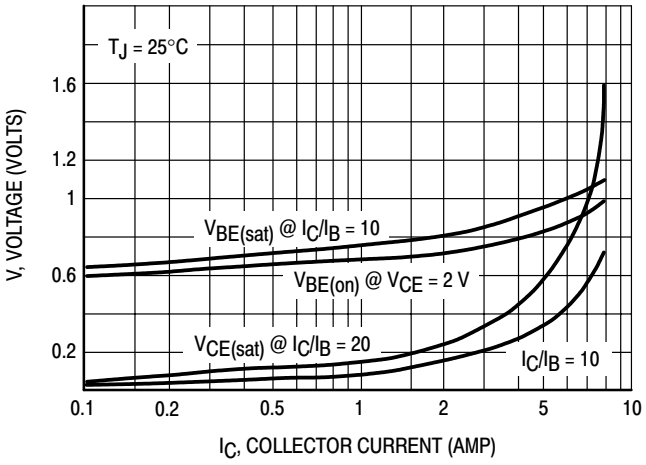


Figure 8a. MJF15030 NPN

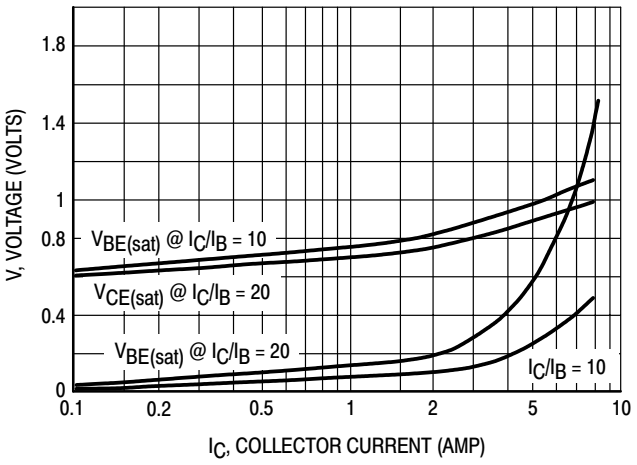


Figure 8b. MJF15031 PNP

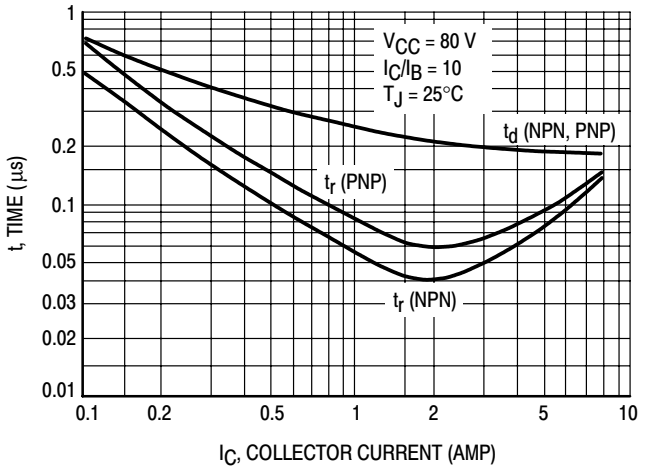


Figure 9. Turn−On Times

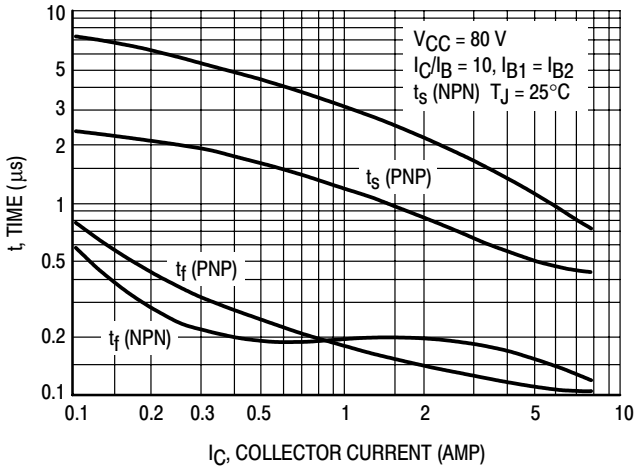


Figure 10. Turn−Off Times

TEST CONDITIONS FOR ISOLATION TESTS*

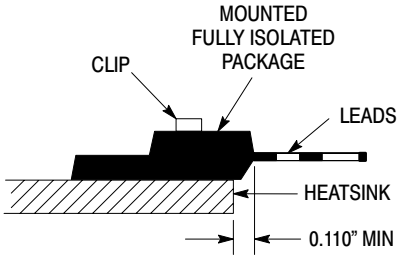


Figure 11. Clip Mounting Position for Isolation Test Number 1

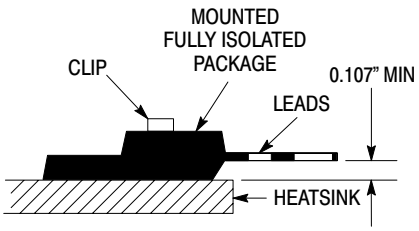


Figure 12. Clip Mounting Position for Isolation Test Number 2

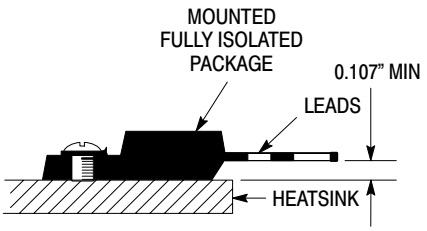


Figure 13. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

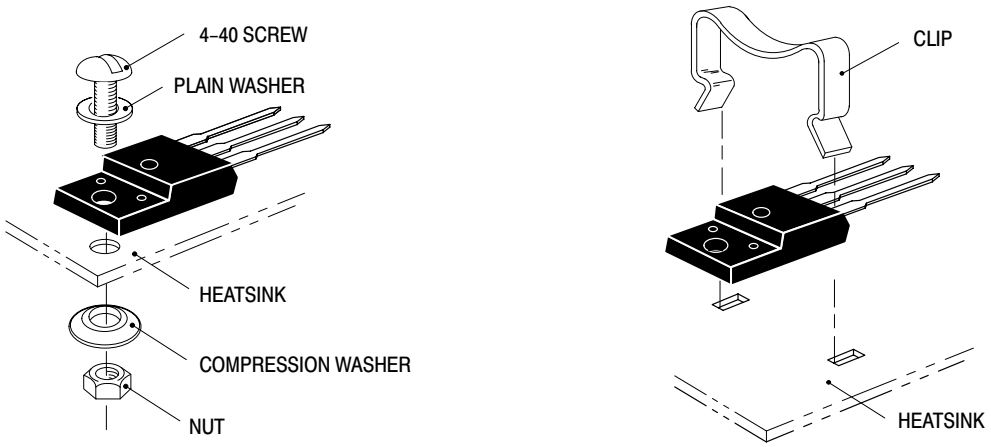


Figure 14. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJF3055 (NPN), MJF2955 (PNP)

Complementary Silicon Power Transistors

Specifically designed for general purpose amplifier and switching applications.

- Isolated Overmold Package (1500 Volts RMS Min)
- Electrically Similar to the Popular MJE3055T and MJE2955T
- Collector−Emitter Sustaining Voltage − $V_{CEO(sus)}$ 90 Volts
- 10 Amperes Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation
- Epoxy Meets UL94, VO at 1/8″
- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	$V_{CEO(sus)}$	90	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	90	Vdc
Base−Emitter Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	10	Adc
Base Current − Continuous	I_B	6.0	Adc
RMS Isolation Voltage (Note 3) Test No. 1 Per Fig. 11 (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 12 T_A = 25°C) Test No. 3 Per Fig. 13	V_{ISOL}	 4500 3500 1500	V_{RMS}
Total Power Dissipation @ T_C = 25°C (Note 2) Derate above 25°C	P_D	30 0.25	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction to Case (Note 2)	$R_{\theta JC}$	4.0	°C/W
Thermal Resistance − Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
2. Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
3. Proper strike and creepage distance must be provided.

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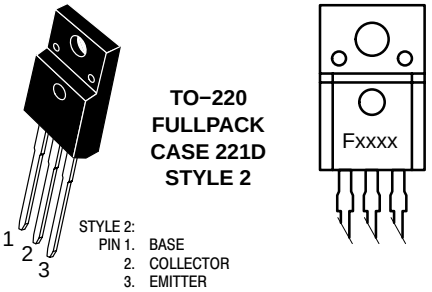
COMPLEMENTARY SILICON POWER TRANSISTORS 10 AMPERES 90 VOLTS 30 WATTS

MARKING DIAGRAM



TO−220 FULLPACK CASE 221D STYLE 2

Fxxxx = Specific Device Code
xxxx = 2955 or 3055

ORDERING INFORMATION

Device	Package	Shipping
MJF2955	TO−220 FULLPACK	50 Units/Rail
MJF3055	TO−220 FULLPACK	50 Units/Rail

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (Note 4)				
Collector−Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	90	−	Vdc
Collector Cutoff Current (V_{CE} = 90 Vdc, V_{BE} = 0)	I_{CES}	−	1.0	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, I_E = 0)	I_{CBO}	−	1.0	μAdc
Emitter−Base Leakage (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	1.0	μAdc
ON CHARACTERISTICS (Note 4)				
DC Current Gain (I_{CE} = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_{CE} = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	100 −	−
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 − −	 1.0 2.5	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{BE} = 4.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain−Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f_{test} = 500 kHz)	f_T	2.0	−	MHz

4. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

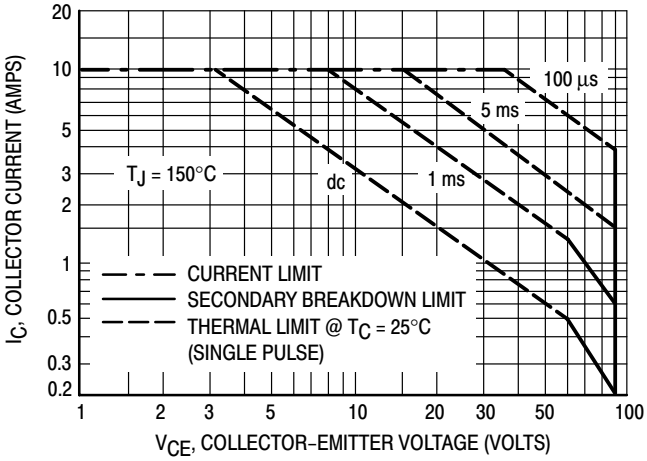


Figure 7. Maximum Forward Bias Safe Operating Area

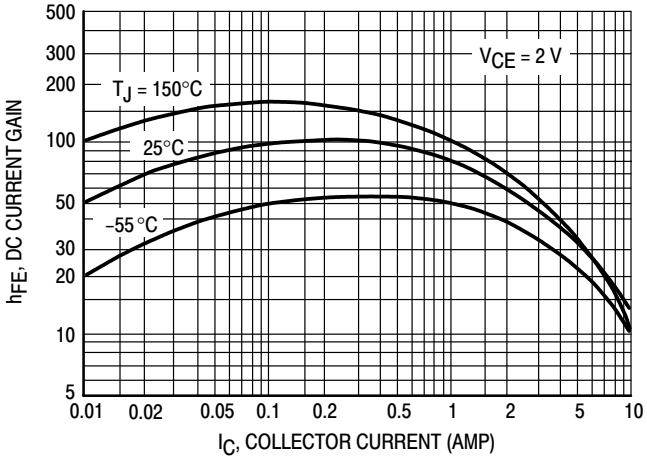
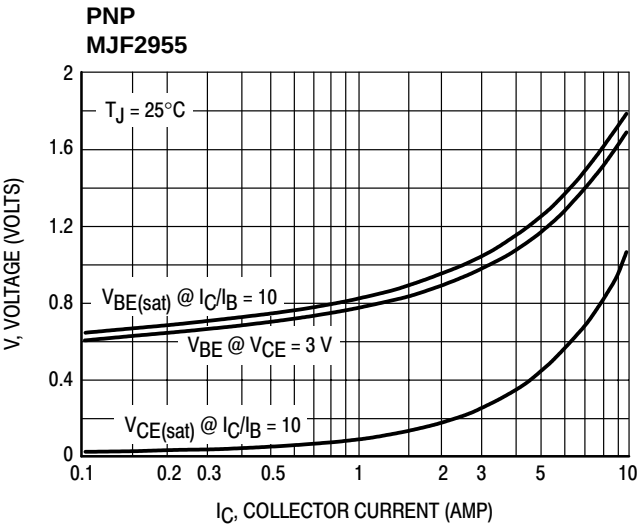


Figure 8. DC Current Gain



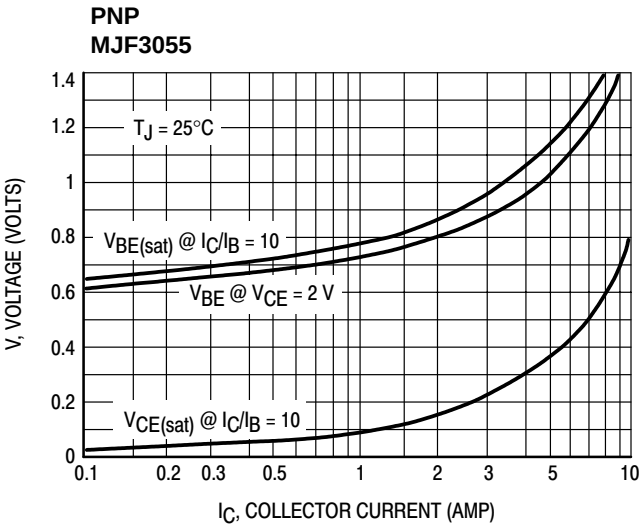


Figure 9. “On” Voltages

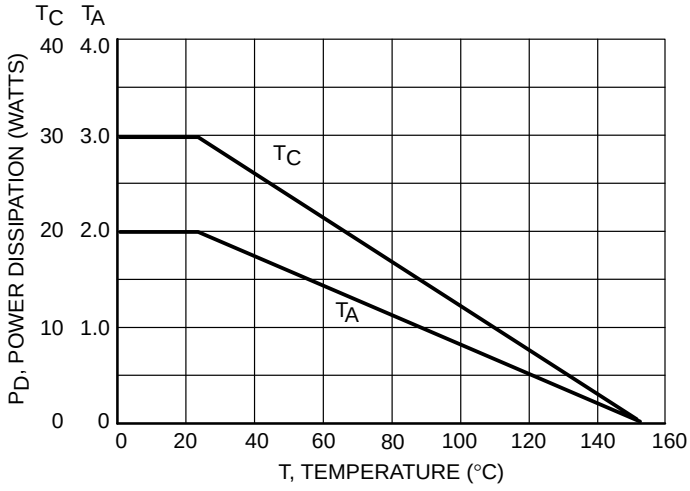


Figure 10. Power Derating

TEST CONDITIONS FOR ISOLATION TESTS*

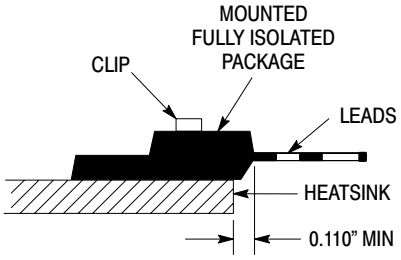


Figure 11. Clip Mounting Position for Isolation Test Number 1

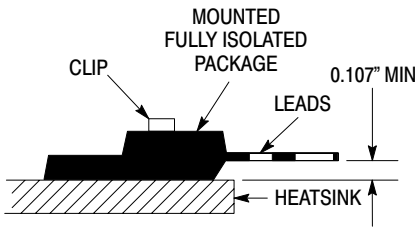


Figure 12. Clip Mounting Position for Isolation Test Number 2

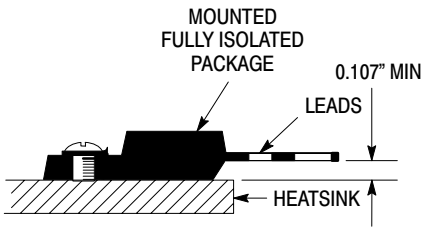


Figure 13. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

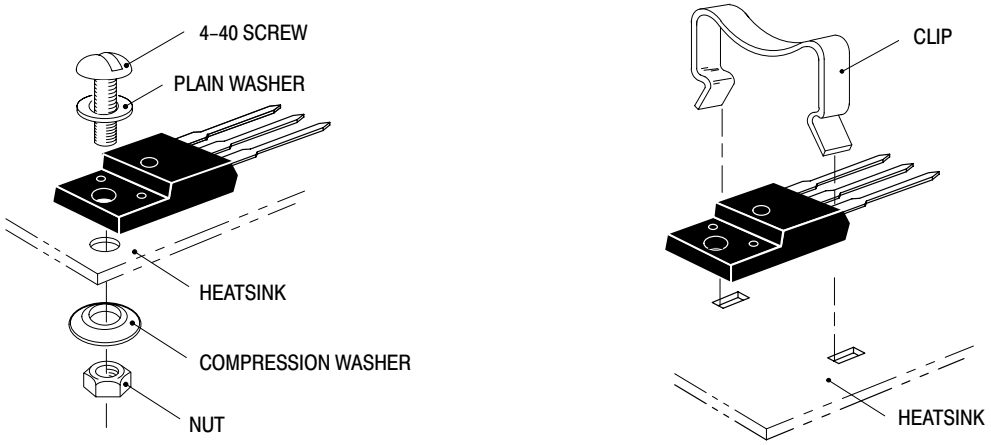


Figure 14. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJF31C* (NPN), MJF32C* (PNP)

*Preferred Devices

Complementary Silicon Plastic Power Transistors for Isolated Package Applications

Designed for use in general purpose amplifier and switching applications.

- Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- High Current Gain − Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

MAXIMUM RATINGS

Rating	Symbol	MJF31C MJF32C	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current Continuous Peak	I_C	 3.0 5.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 28 0.22	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Unclamped Inductive Load Energy (Note 1)	E	32	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

1. I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω..

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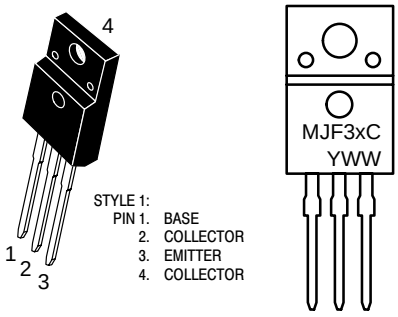
3.0 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 100 VOLTS 28 WATTS



TO−220 FULLPAK
CASE 221D−02

MJF3xC = Specific Device Code
x = 1 or 2
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 648 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

APRIL, 2002 − Rev. 2
Publication Order Number:
MJF31C/D

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.46	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	I_{CEO}	–	0.3	mAdc
Collector Cutoff Current	I_{CES}	–	200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 10	– 50	–
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)	$V_{CE(sat)}$	–	1.2	Vdc
Base−Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	3.0	–	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	–	–

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

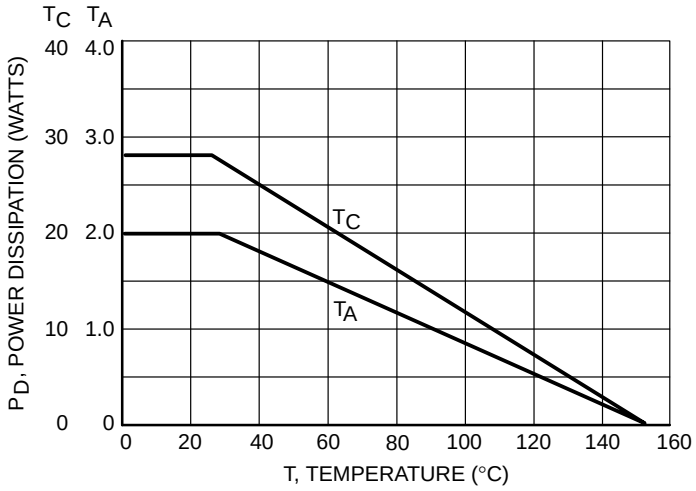


Figure 1. Power Derating

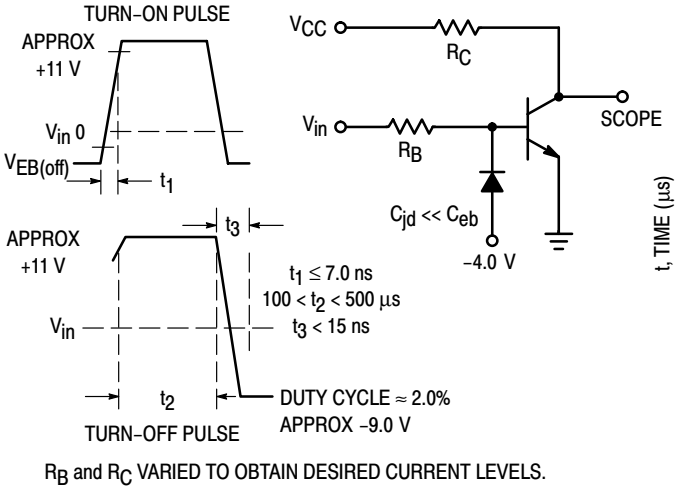


Figure 2. Switching Time Equivalent Circuit

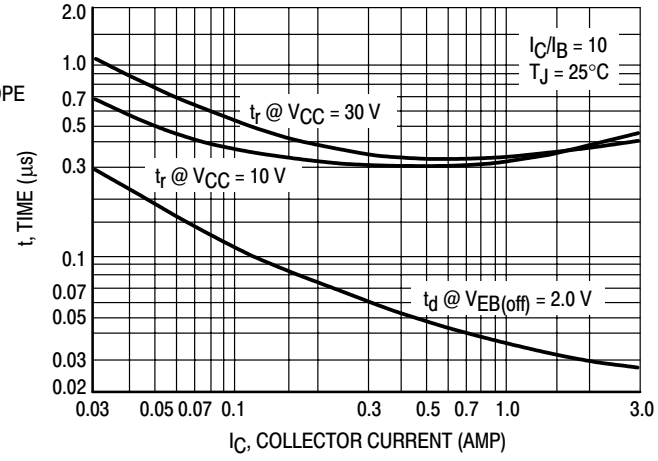


Figure 3. Turn−On Time

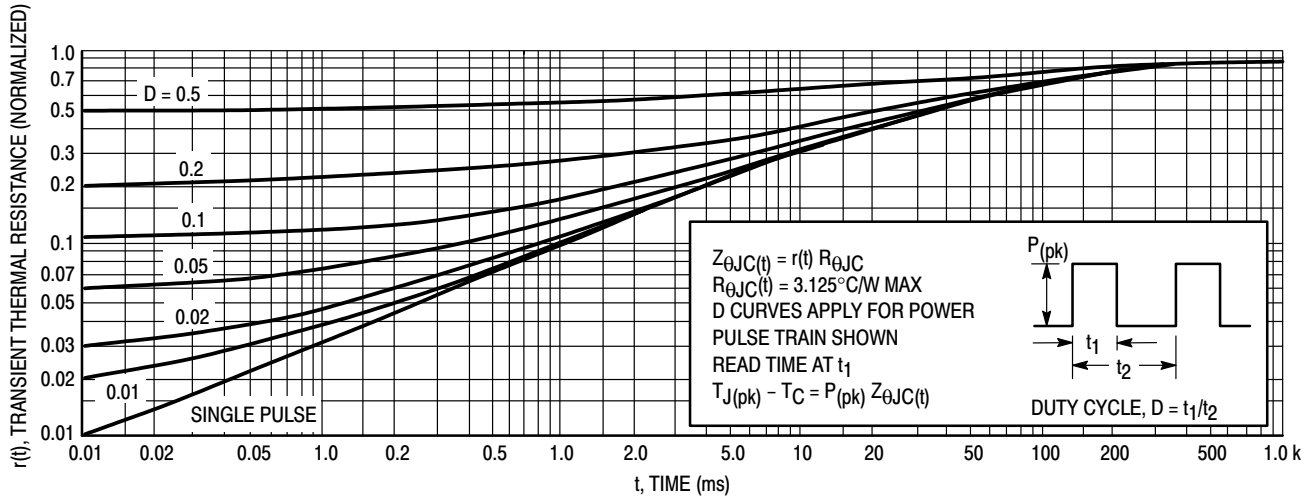


Figure 4. Thermal Response

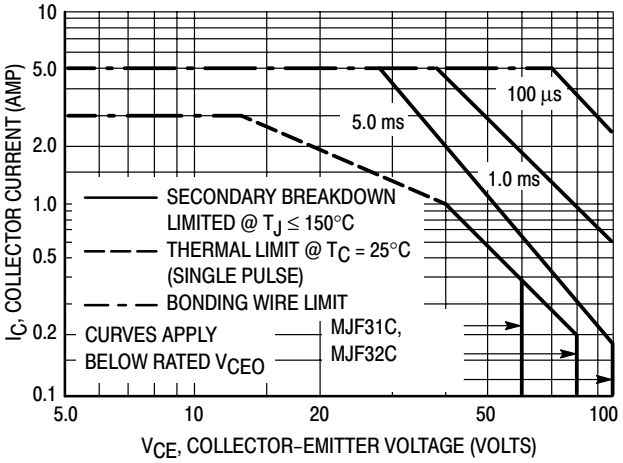


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

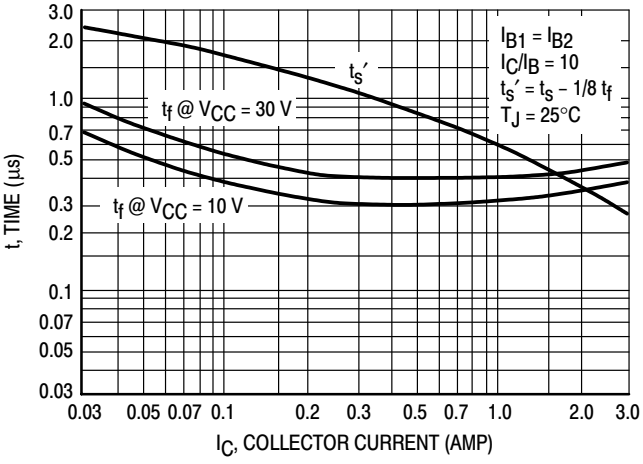


Figure 6. Turn−Off Time

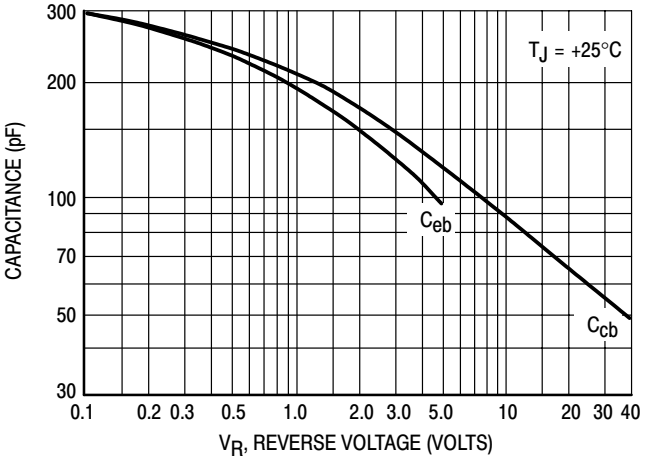


Figure 7. Capacitance

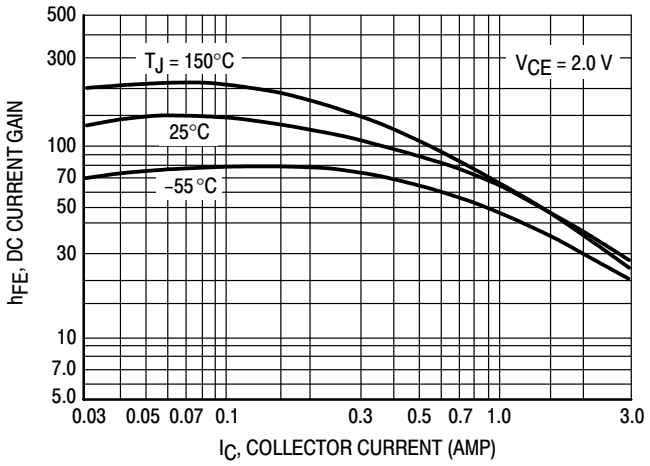


Figure 8. DC Current Gain

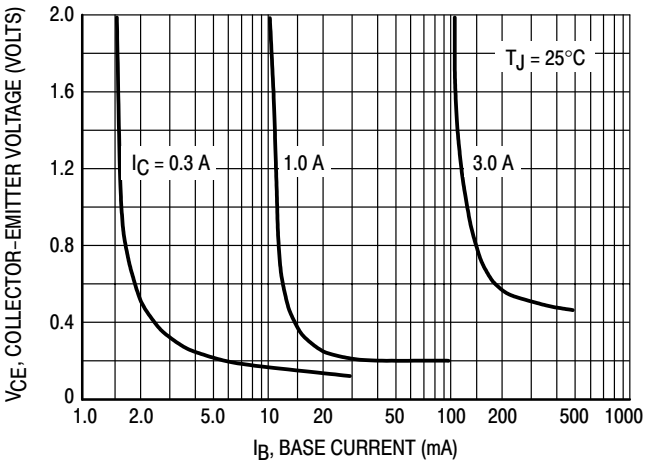


Figure 9. Collector Saturation Region

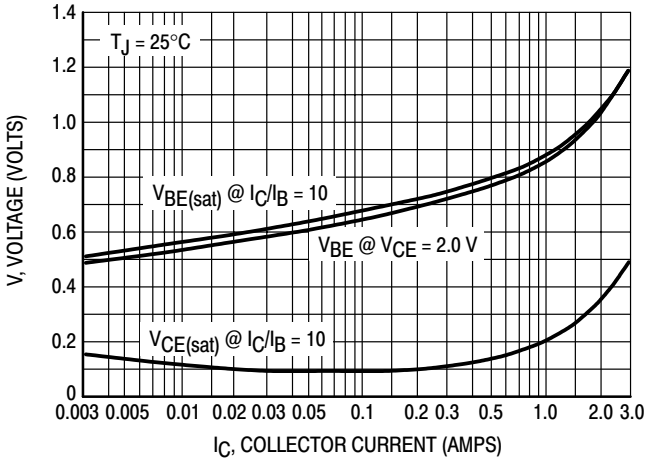


Figure 10. “On” Voltages

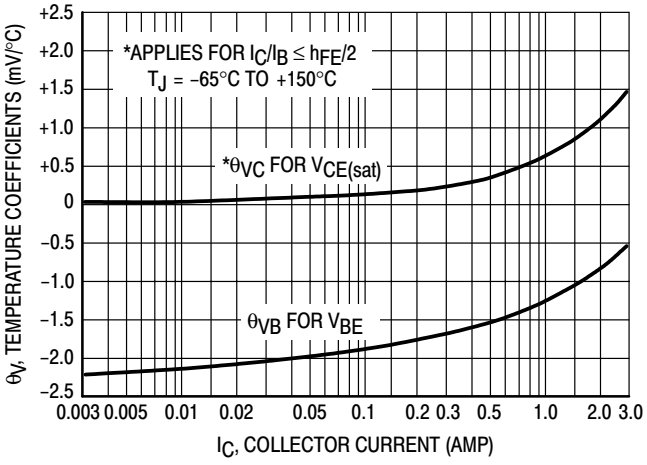


Figure 11. Temperature Coefficients

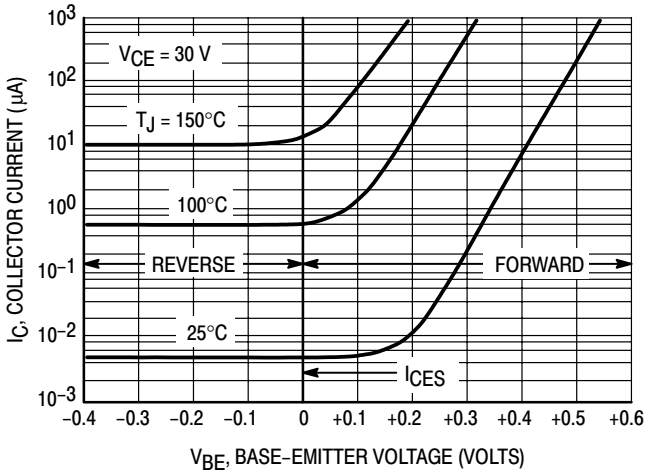


Figure 12. Collector Cut−Off Region

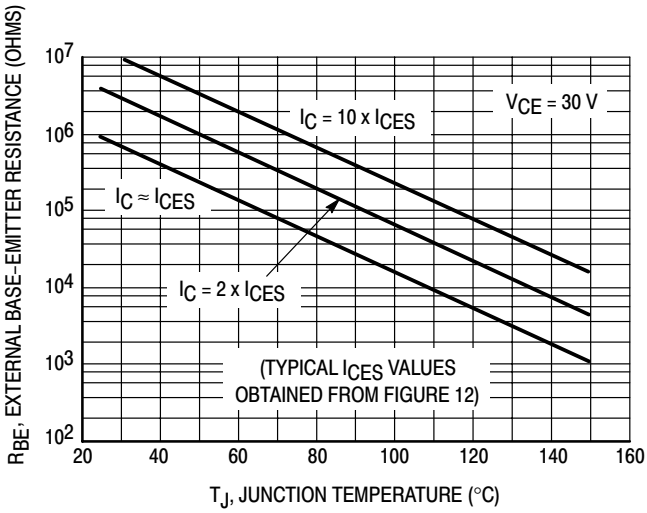


Figure 13. Effects of Base−Emitter Resistance

ORDERING INFORMATION

Device	Package	Shipping
MJF31C	TO−220 FULLPAK	50 Units/Rail
MJF32C	TO−220 FULLPAK	50 Units/Rail

MJF44H11 (NPN), MJF45H11 (PNP)

Preferred Devices

Complementary Power Transistors

For Isolated Package Applications

. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 36 1.67	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

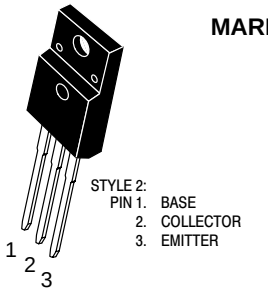
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ON Semiconductor®

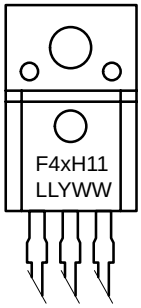
http://onsemi.com

SILICON POWER TRANSISTORS
10 AMPERES
80 VOLTS
36 WATTS



ISOLATED TO−220
CASE 221D
PLASTIC

MARKING DIAGRAM



F4xH11 = Specific Device Code
x = 4 or 5
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF44H11	TO−220	50 Units/Rail
MJF45H11	TO−220	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	−	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	−	−	1.0	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	−	−	10	μA
ON CHARACTERISTICS						
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	−	−	1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	−	−	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	−	−	−
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	−	−	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJF44H11 MJF45H11	C_{cb}	 −	 130	 −	pF
			−	230	−	
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJF44H11 MJF45H11	f_T	 −	 50	 −	MHz
			−	40	−	
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJF44H11 MJF45H11	$t_d + t_r$	 −	 300	 −	ns
			−	135	−	
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJF44H11 MJF45H11	t_s	 −	 500	 −	ns
			−	500	−	
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJF44H11 MJF45H11	t_f	 −	 140	 −	ns
			−	100	−	

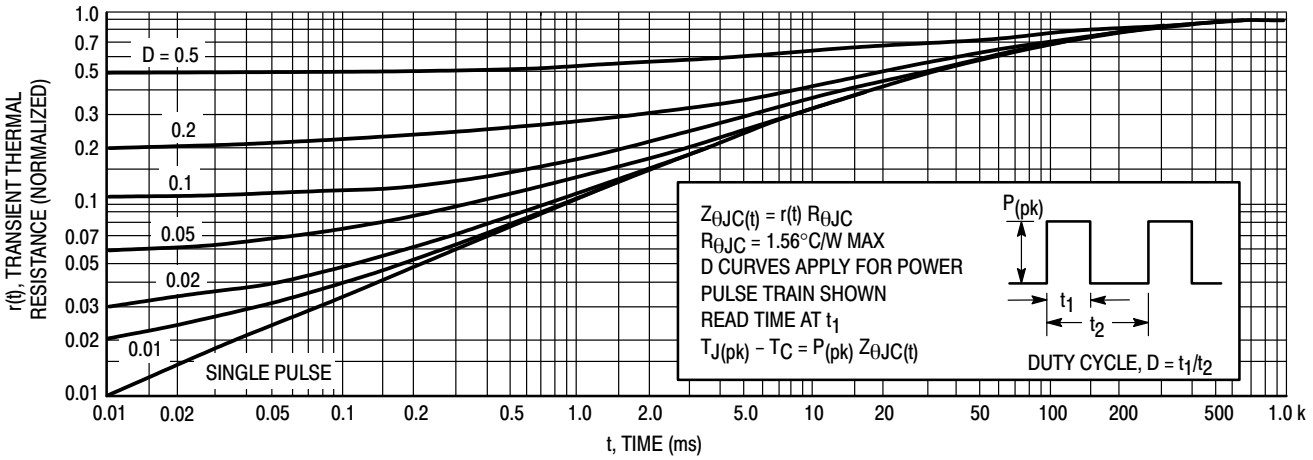


Figure 1. Thermal Response

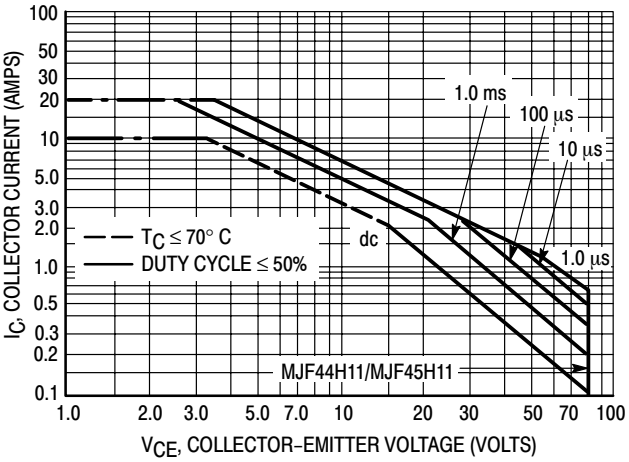


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

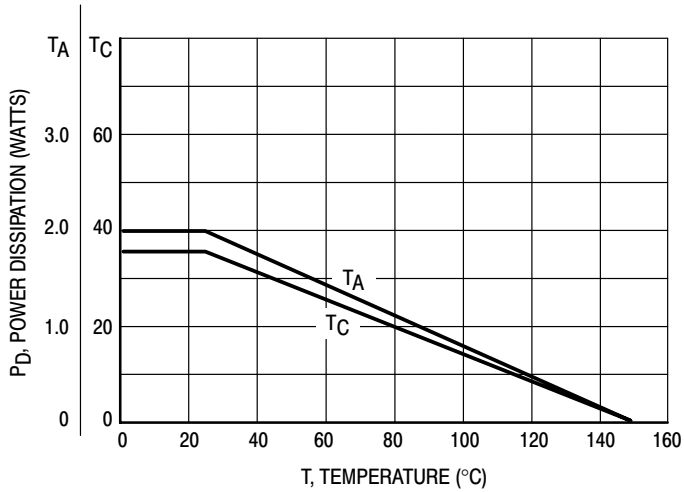


Figure 3. Power Derating

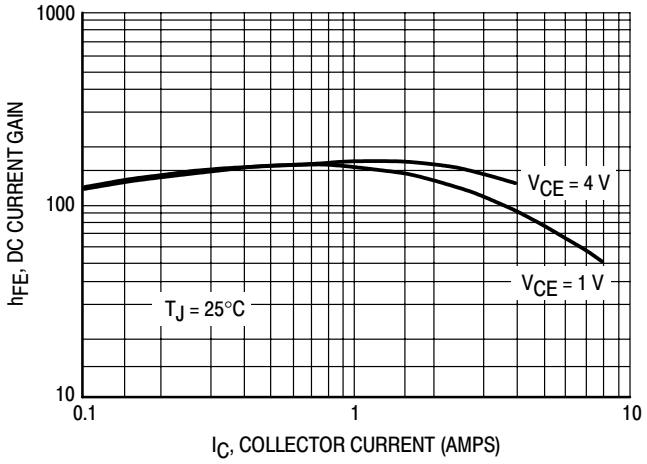


Figure 4. MJF44H11 DC Current Gain

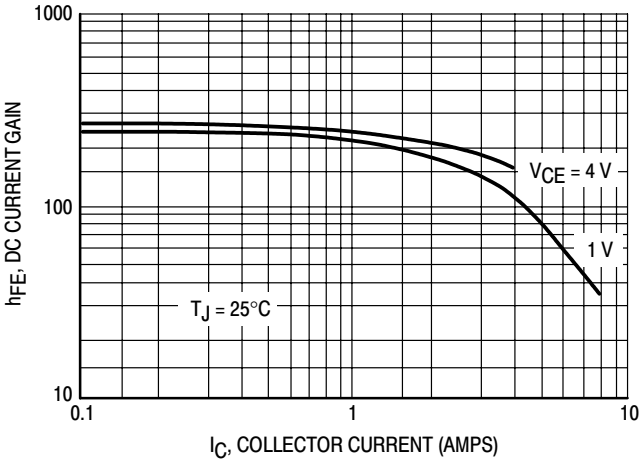


Figure 5. MJF45H11 DC Current Gain

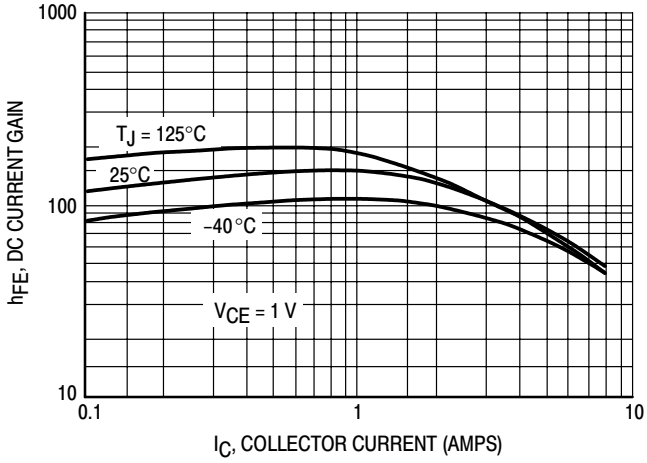


Figure 6. MJF44H11 Current Gain versus Temperature

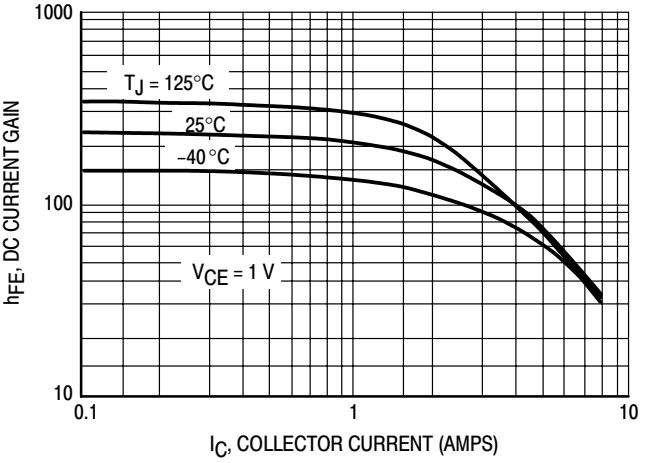


Figure 7. MJF45H11 Current Gain versus Temperature

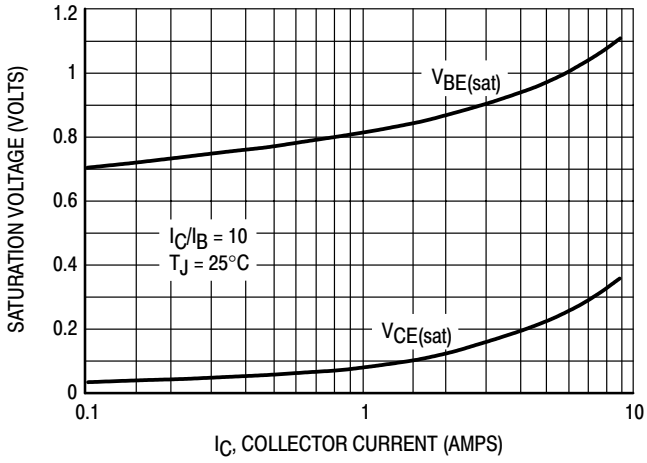


Figure 8. MJF44H11 On−Voltages

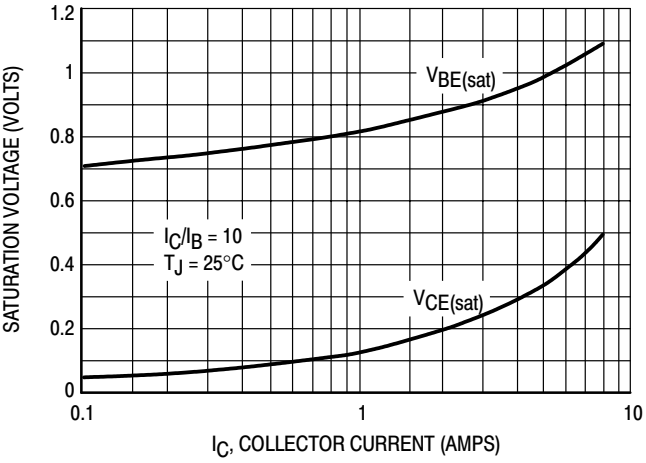


Figure 9. MJF45H11 On−Voltages

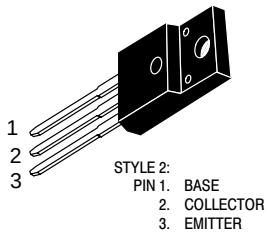
MJF47

High Voltage Power Transistor
Isolated Package Applications

Designed for line operated audio output amplifiers, switching power supply drivers and other switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP47
- 250 $V_{CEO(sus)}$
- 1 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

NPN SILICON
POWER TRANSISTOR
1 AMPERE
250 VOLTS
28 WATTS



CASE 221D−02
TO−220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage		V_{CEO}	250	Vdc
Collector−Base Voltage		V_{CB}	350	Vdc
Emitter−Base Voltage		V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 10 Test No. 2 Per Fig. 11 Test No. 3 Per Fig. 12	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous Peak		I_C	1 2	Adc
Base Current		I_B	0.6	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	28 0.23	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.4	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
(1) Proper strike and creepage distance must be provided.

April, 2002 − Rev. 3
Publication Order Number:
MJF47/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	0.2	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	I_{CES}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	1	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)	h_{FE}	30 10	150 —	—
Collector−Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base−Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} 10 Vdc, f = 2 MHz)	f_T	10	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

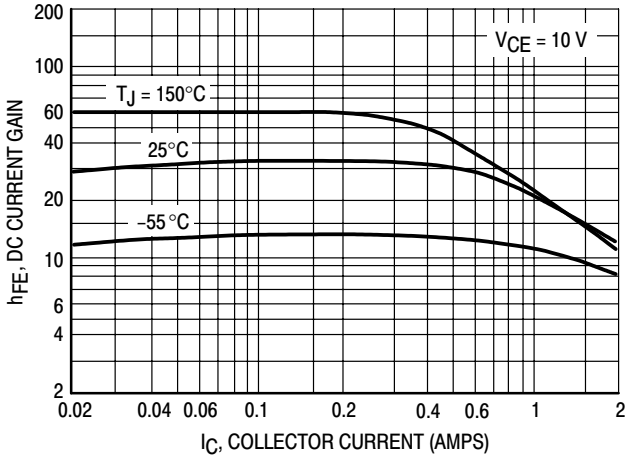


Figure 1. DC Current Gain

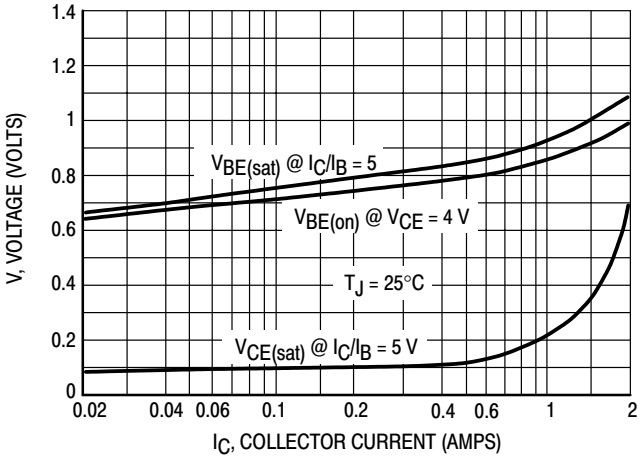


Figure 2. “On” Voltages

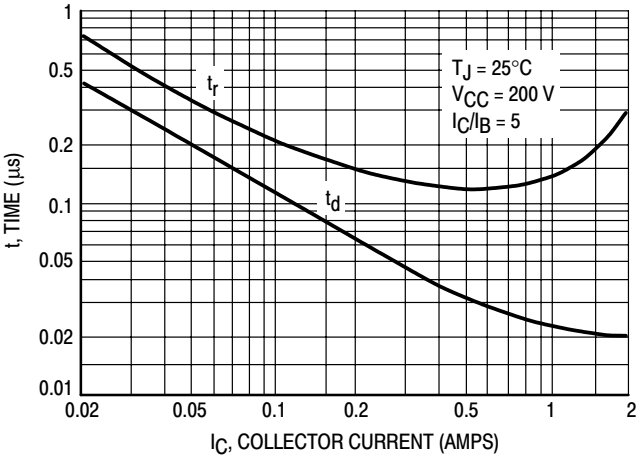


Figure 3. Turn−On Time

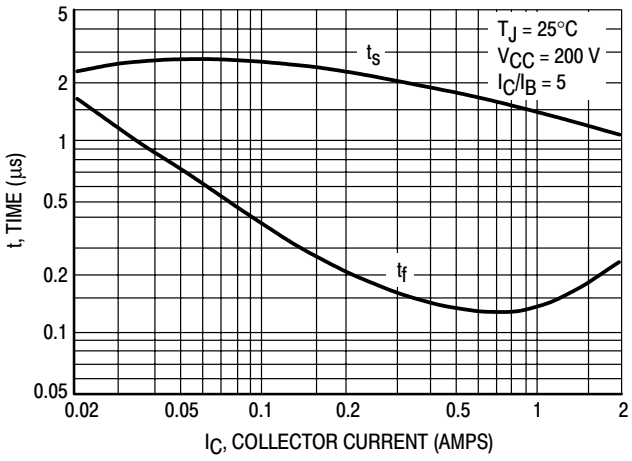


Figure 4. Turn−Off Time

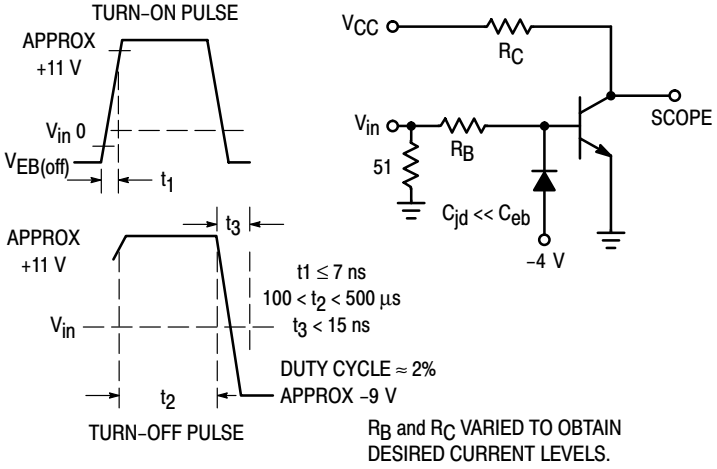


Figure 5. Switching Time Equivalent Circuit

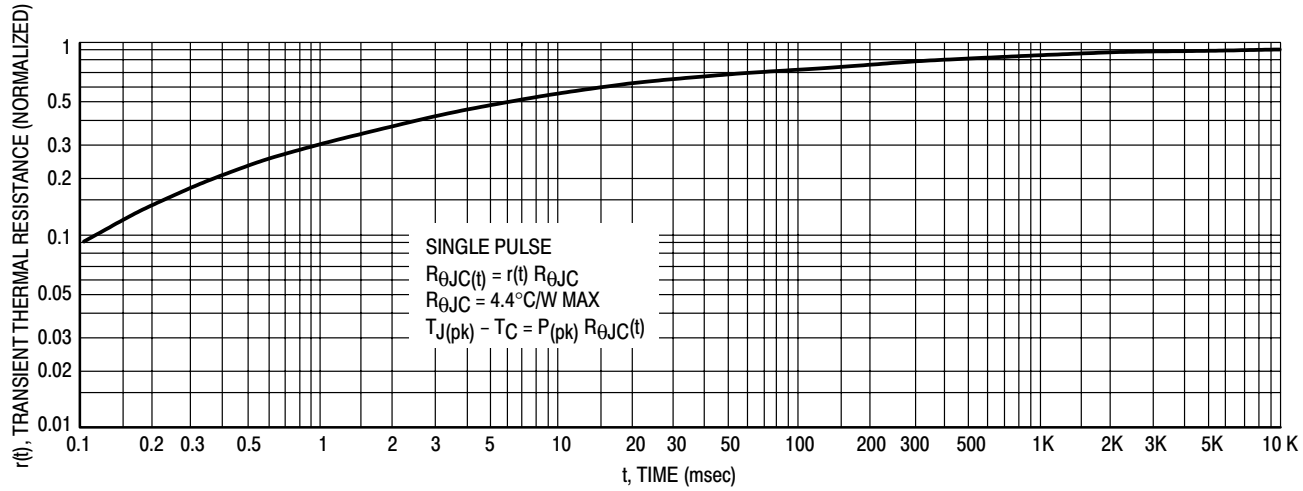


Figure 6. Thermal Response

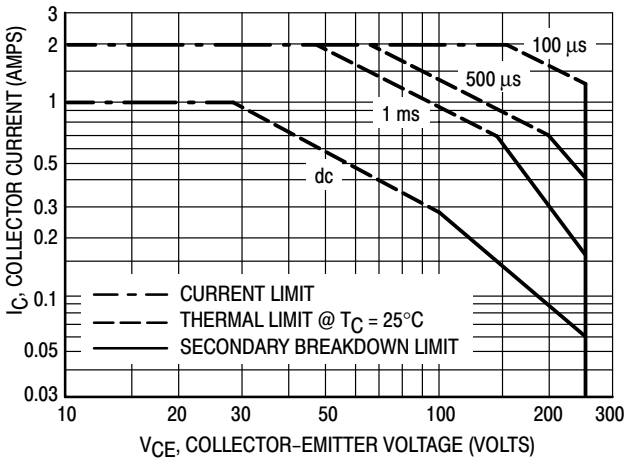


Figure 7. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

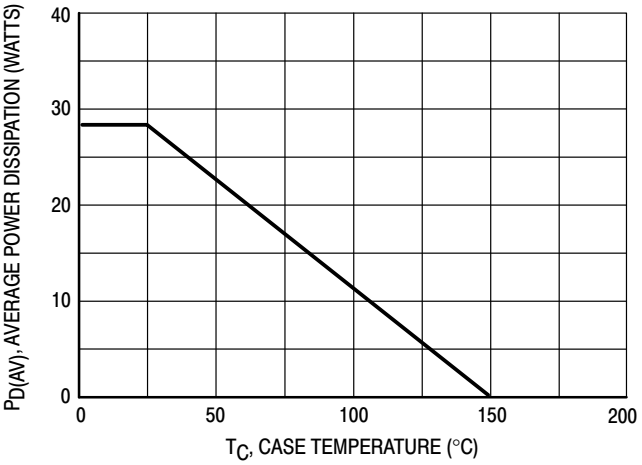


Figure 8. Power Derating

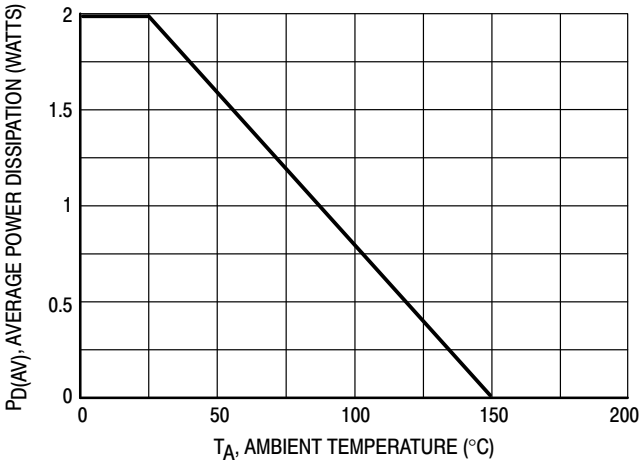


Figure 9. Power Derating

TEST CONDITIONS FOR ISOLATION TESTS*

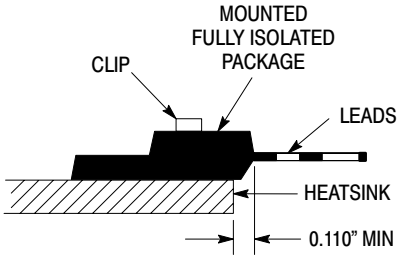


Figure 10. Clip Mounting Position for Isolation Test Number 1

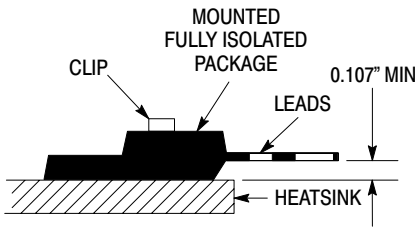


Figure 11. Clip Mounting Position for Isolation Test Number 2

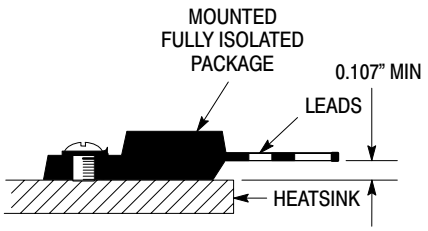


Figure 12. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

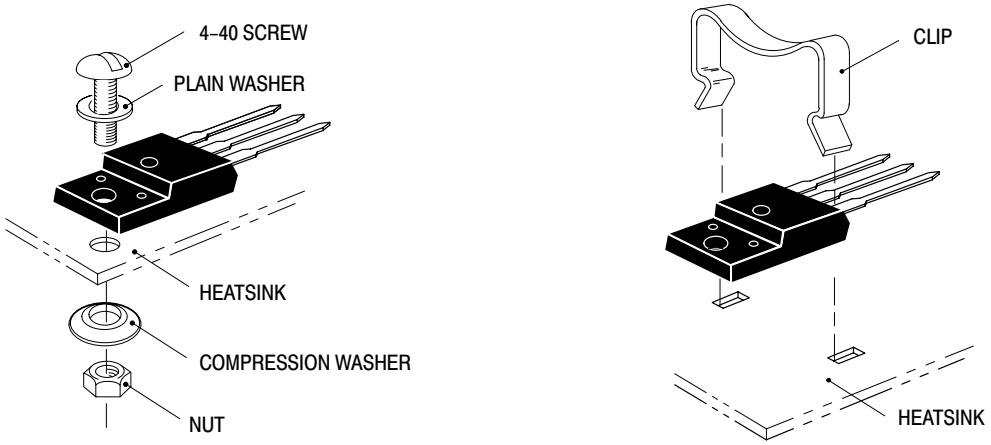


Figure 13. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Darlingtons

For Isolated Package Applications

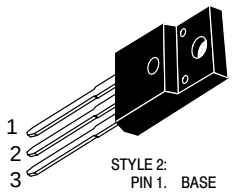
NPN
MJF6388*
PNP
MJF6668*

*ON Semiconductor Preferred Devices

COMPLEMENTARY SILICON POWER DARLINGTONS 10 AMPERES 100 VOLTS 40 WATTS

Designed for general−purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Isolated Overmold Package, TO−220 Type
- Electrically Similar to the Popular 2N6388, 2N6668, TIP102 and TIP107
- 100 $V_{CEO(sus)}$
- 10 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 1000 (Min) @ I_C = 5.0 Adc
- High Isolation Voltage (up to 4500 VRMS)
- Case 221D is UL Recognized at 3500 VRMS: File #E69369



STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 221D−02
UL RECOGNIZED

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage		V_{CEO}	100	Vdc
Collector−Base Voltage		V_{CB}	100	Vdc
Emitter−Base Voltage		V_{EB}	5.0	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Figure 14 Test No. 2 Per Figure 15 Test No. 3 Per Figure 16	V_{ISOL}	4500 3500 1500	V
Collector Current — Continuous — Peak(2)		I_C	10 15	Adc
Base Current		I_B	1.0	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	40 0.31	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

(1) Proper strike and creepage distance must be provided.
(2) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

*Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied and a mounting torque of 6 to 8 in▪lbs.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

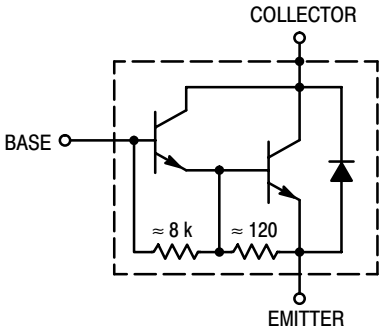
April, 2002 − Rev. 6
Publication Order Number:
MJF6388/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	— —	10 3.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	3000 1000 200 100	15000 — — —	—
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc) (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 8.0 Adc, I_B = 80 mAdc) (I_C = 10 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	— — — —	2.0 2.0 2.5 3.0	Vdc
Base−Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	— —	2.8 4.5	Vdc
Base−Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz) MJF6388 MJF6668	C_{ob}	—	200 300	pF
Insulation Capacitance (Collector−to−External Heatsink)	C_{c-hs}	—	3.0 Typ	pF
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	1000	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

NPN
MJF6388



PNP
MJF6668

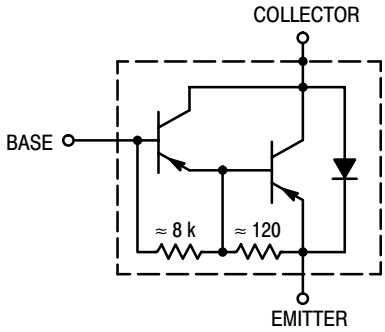


Figure 1. Darlington Schematic

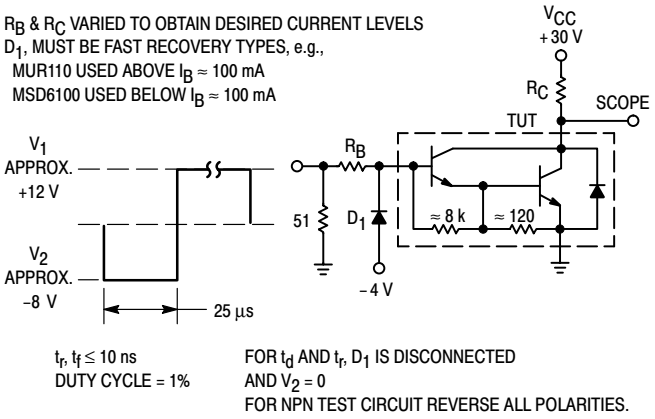


Figure 2. Switching Times Test Circuit

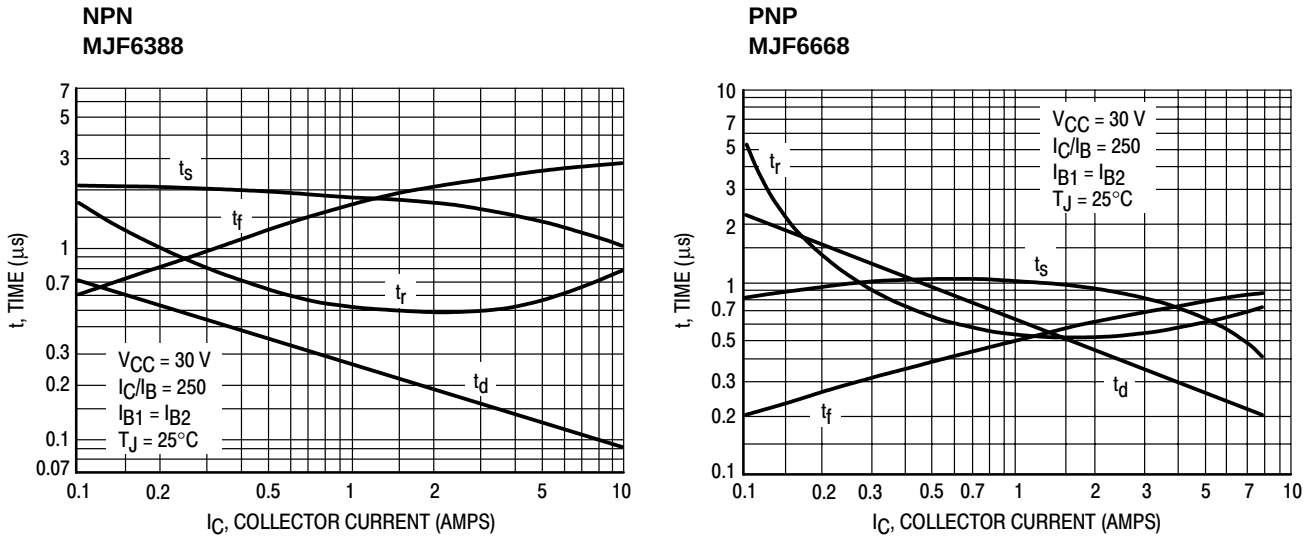


Figure 3. Typical Switching Times

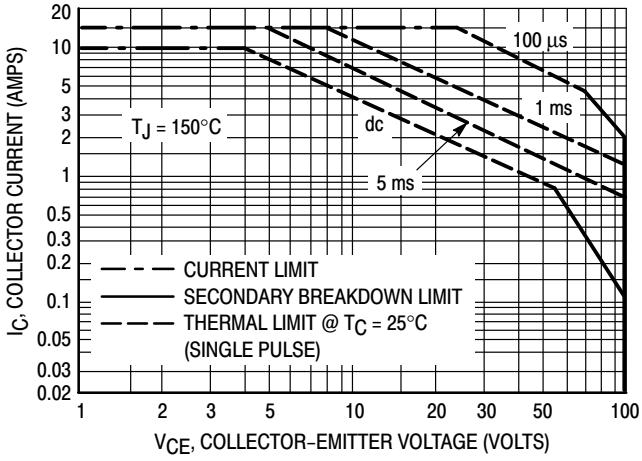


Figure 4. Maximum Forward Bias Safe Operating Area

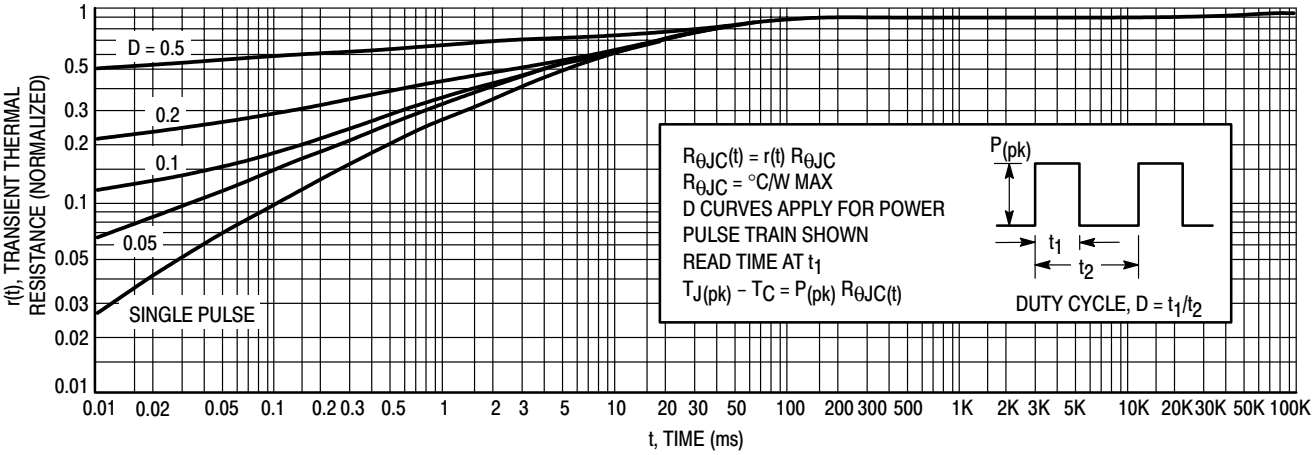


Figure 5. Thermal Response

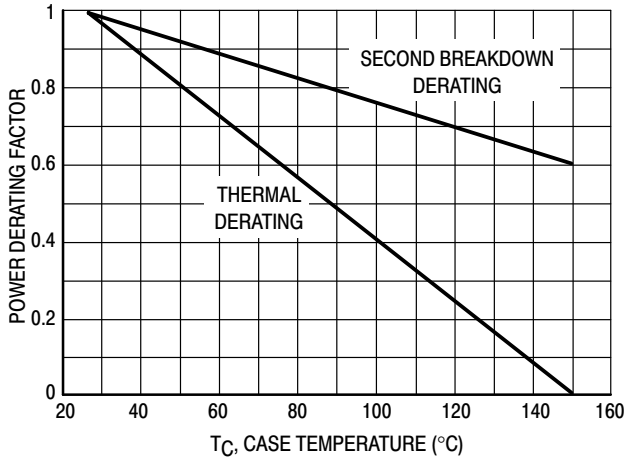


Figure 6. Maximum Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = l50°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

NPN
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PNP
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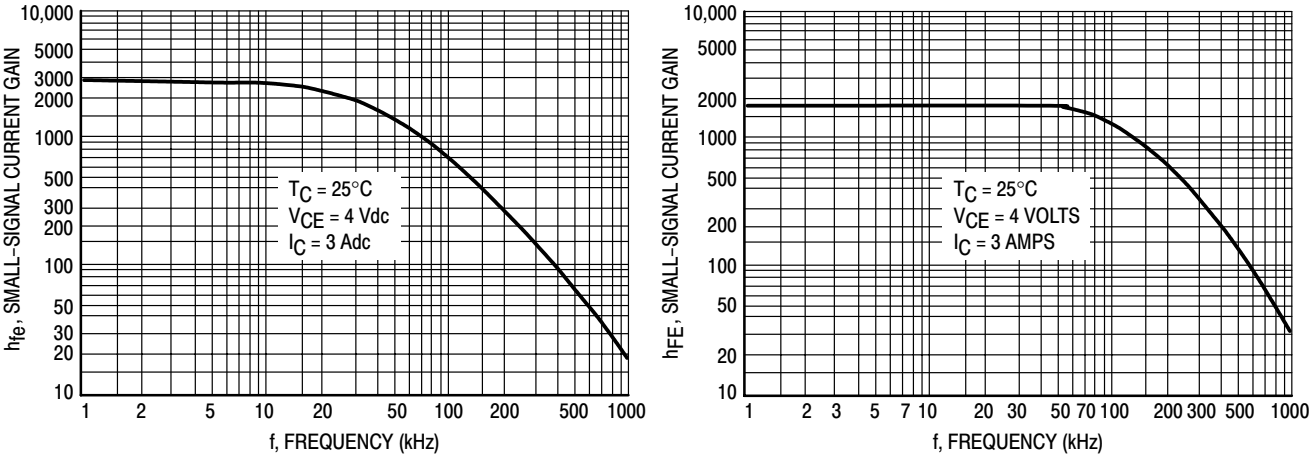
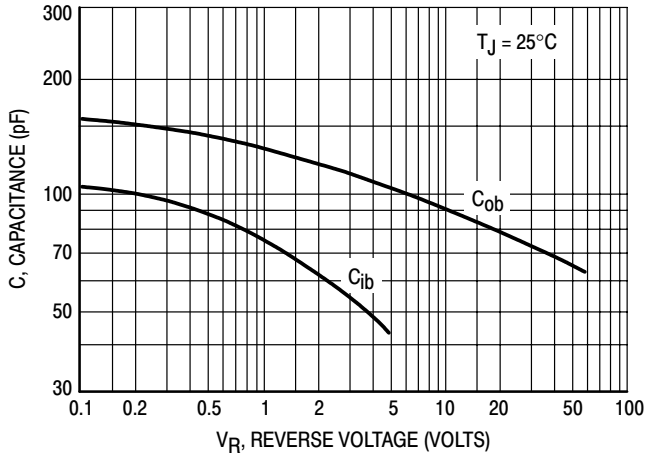


Figure 7. Typical Small−Signal Current Gain

NPN
MJF6388



PNP
MJF6668

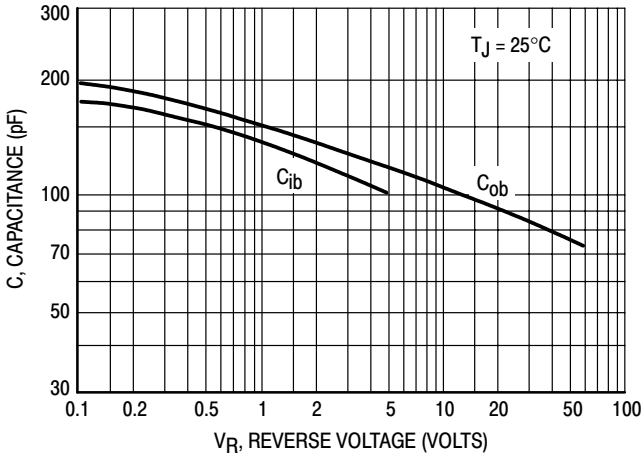
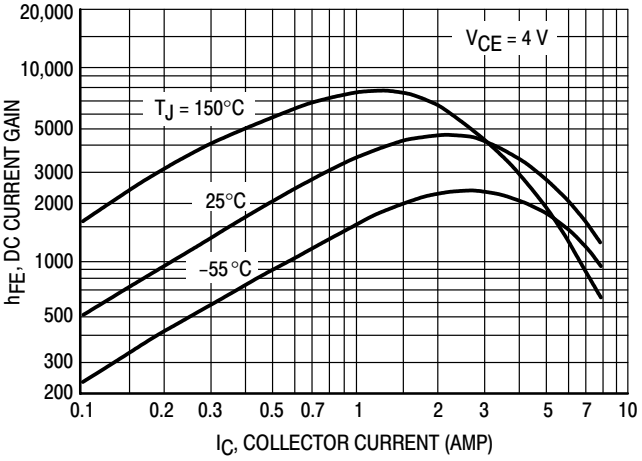


Figure 8. Typical Capacitance



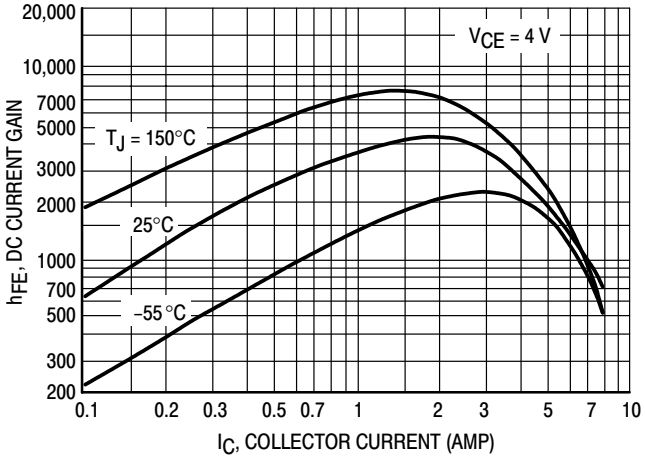
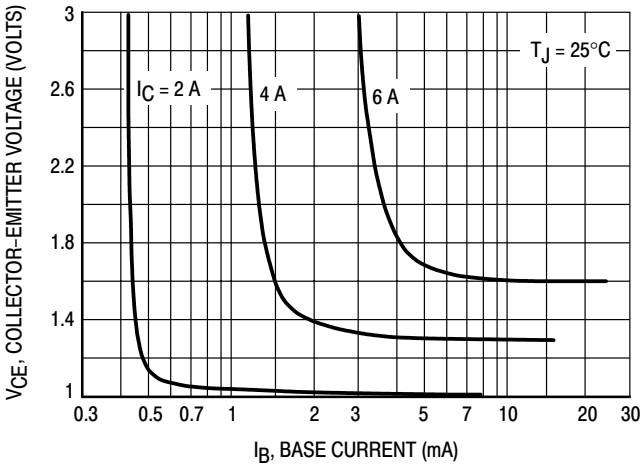


Figure 9. Typical DC Current Gain



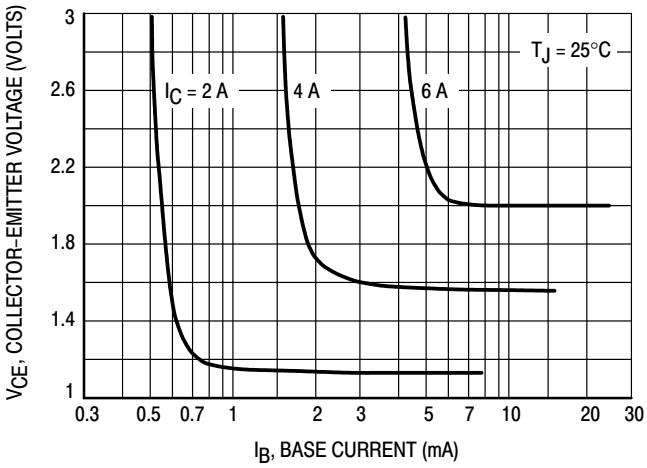


Figure 10. Typical Collector Saturation Region

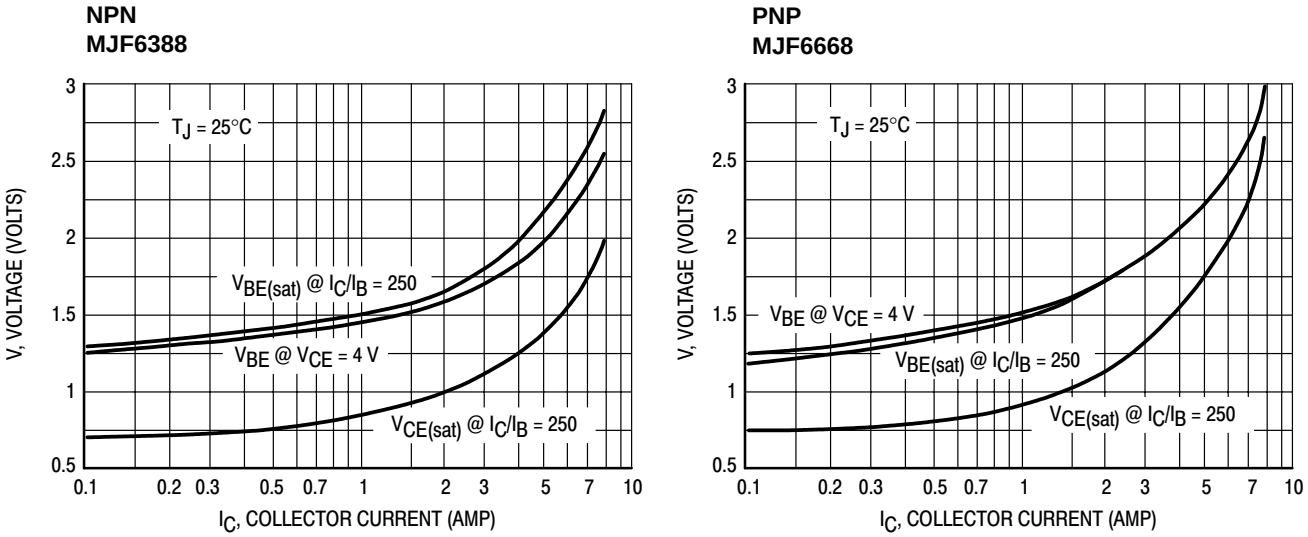


Figure 11. Typical “On” Voltages

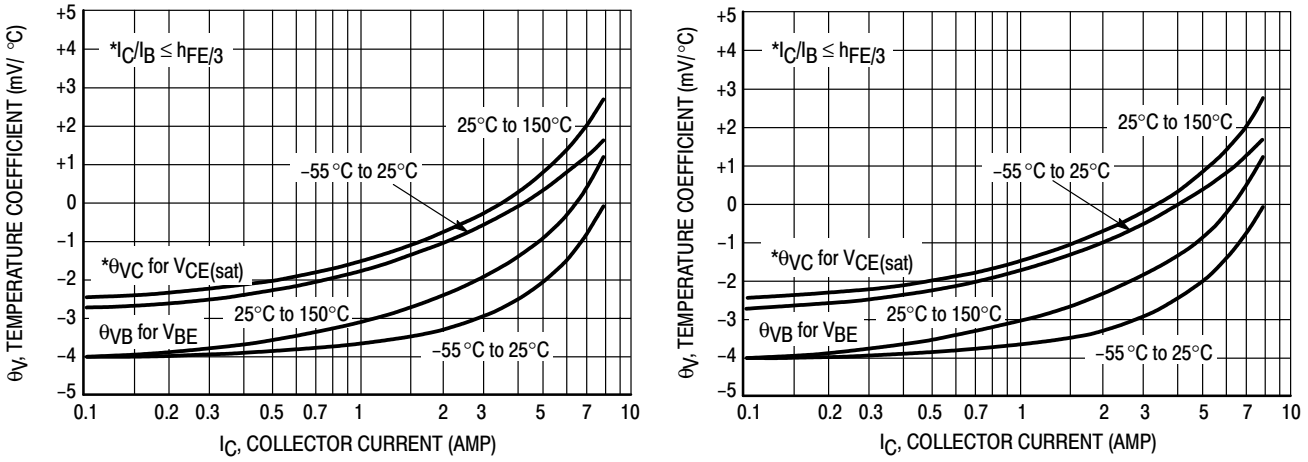


Figure 12. Typical Temperature Coefficients

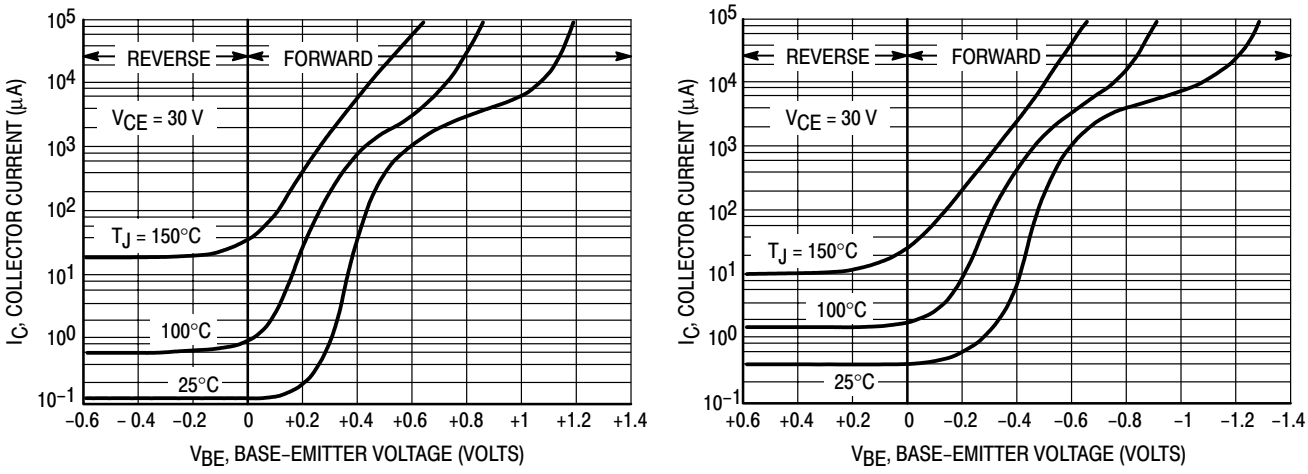


Figure 13. Typical Collector Cut−Off Region

TEST CONDITIONS FOR ISOLATION TESTS*

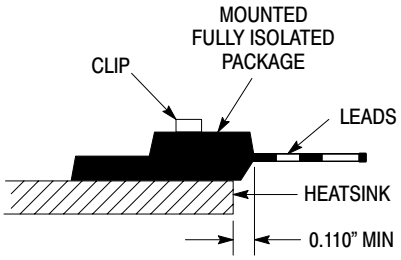


Figure 14. Clip Mounting Position for Isolation Test Number 1

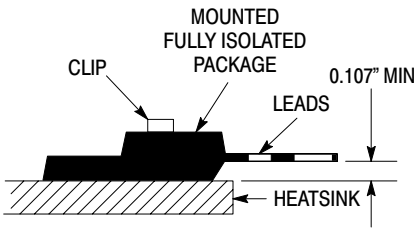


Figure 15. Clip Mounting Position for Isolation Test Number 2

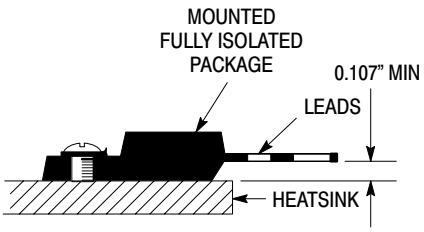


Figure 16. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

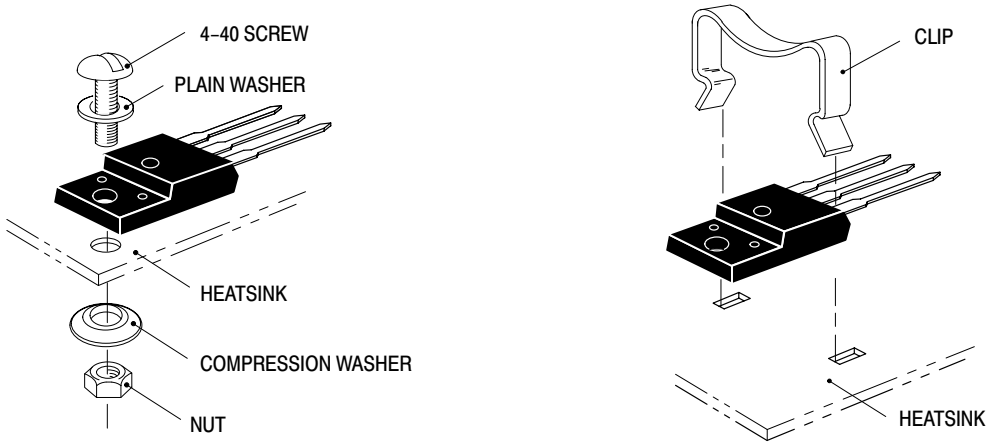


Figure 17. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Darlington Silicon Power Transistors

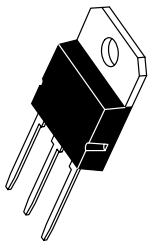
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc —
  h_{FE} = 400 Min (All Types)
- Collector−Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJH11018, 17
  = 200 Vdc (Min) — MJH11020, 19
  = 250 Vdc (Min) — MJH11022, 21
- Low Collector−Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.2 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction

PNP
MJH11017*
MJH11019*
MJH11021*
NPN
MJH11018*
MJH11020*
MJH11022*

*ON Semiconductor Preferred Device

15 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 150, 200, 250 VOLTS 150 WATTS



CASE 340D−02

MAXIMUM RATINGS

Rating	Symbol	MJH 11018 11017	MJH 11020 11019	MJH 11022 11021	Unit
Collector−Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector−Base Voltage	V_{CB}	150	200	250	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous — Peak (1)	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	150 1.2			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance. Junction to Case	$R_{\theta JC}$	0.83	°C/W

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

January, 2002 − Rev. 4
Publication Order Number:
MJH11017/D

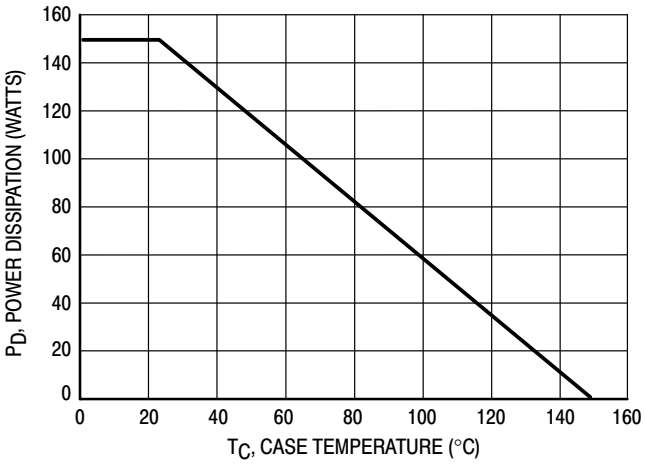


Figure 1. Power Derating

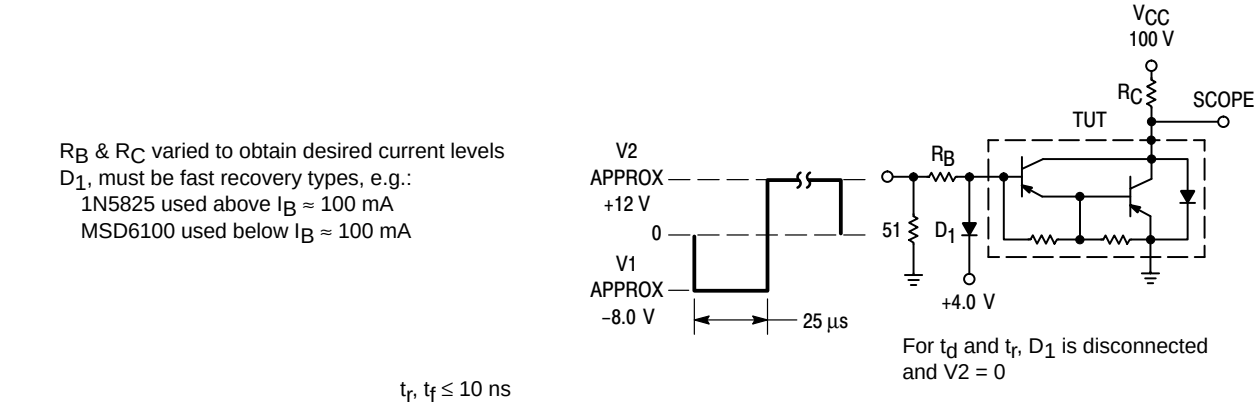
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	$V_{CEO(sus)}$	 150 200 250	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0) (V_{CE} = 100 Vdc, I_B = 0) (V_{CE} = 125 Vdc, I_B = 0)	 MJH11017, MJH11018 MJH11019, MJH11020 MJH11021, MJH11022	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		I_{CEV}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	400 100	15,000 —	—
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)		$V_{CE(sat)}$	— —	2.5 4.0	Vdc
Base−Emitter On Voltage (I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base−Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	3.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH11018, MJH11020, MJH11022 MJH11017, MJH11019, MJH11021	C_{ob}	— —	400 600	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	μs
Storage Time		t_s	4.4	2.7	μs
Fall Time		t_f	2.5	2.5	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.



R_B & R_C varied to obtain desired current levels
D_1, must be fast recovery types, e.g.:
1N5825 used above $I_B \approx 100$ mA
MSD6100 used below $I_B \approx 100$ mA

For t_d and t_r, D_1 is disconnected and V2 = 0

t_r, $t_f \leq 10$ ns
Duty Cycle = 1.0%

For NPN test circuit, reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

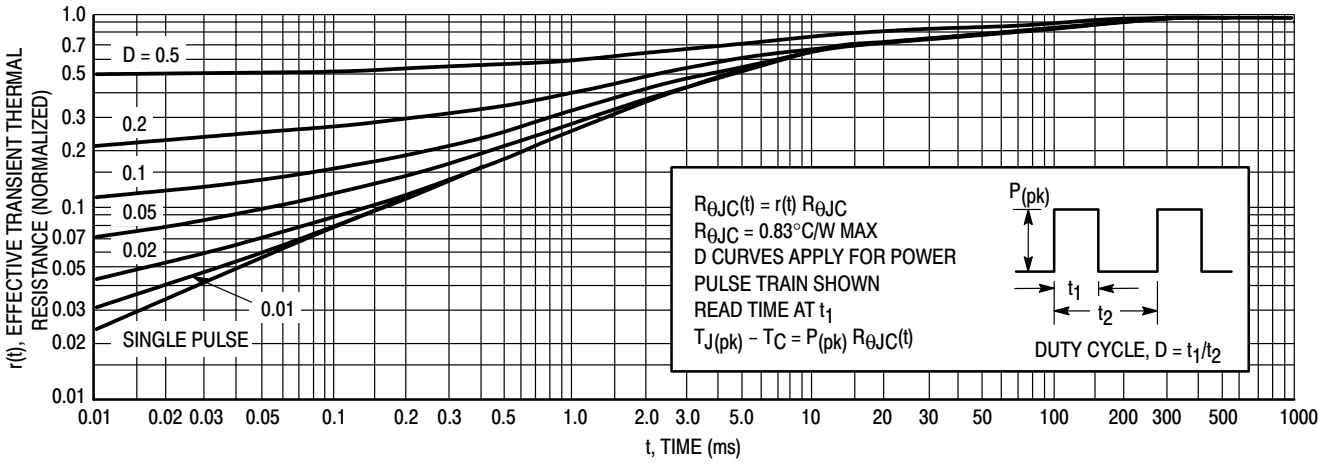


Figure 3. Thermal Response

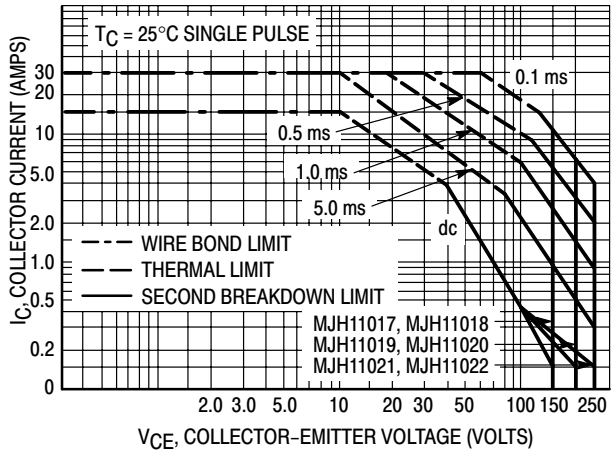


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

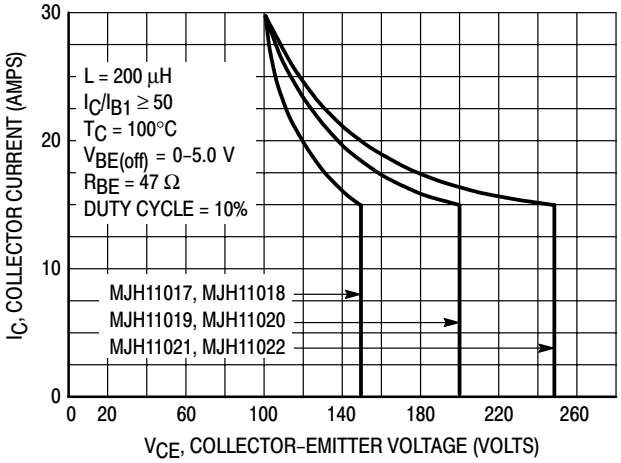


Figure 5. Maximum Rated Reverse Bias Safe Operating Area (RBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

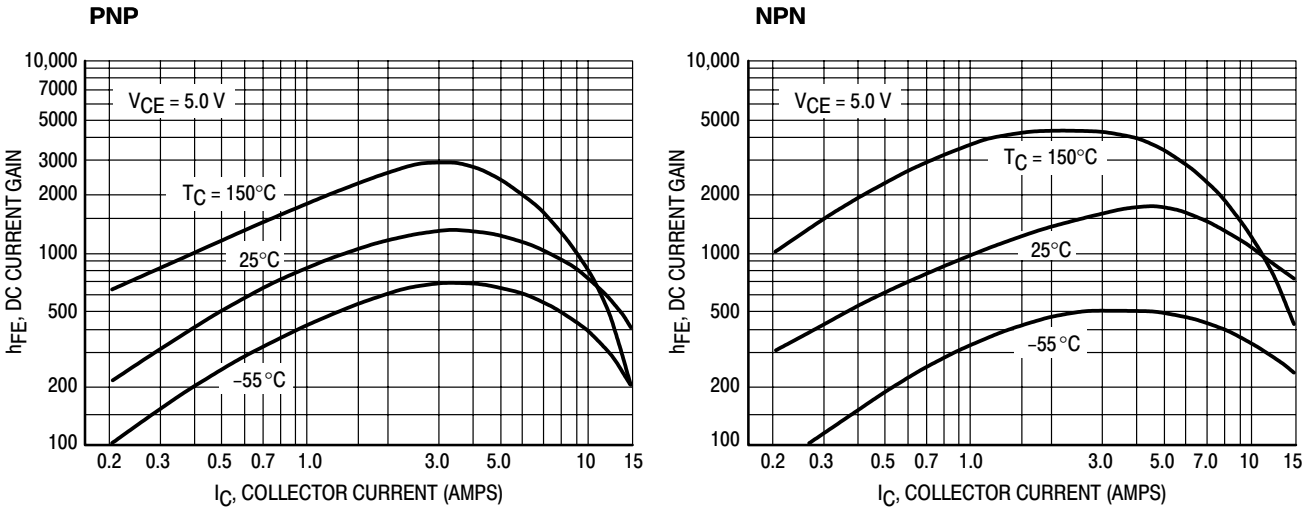


Figure 6. DC Current Gain

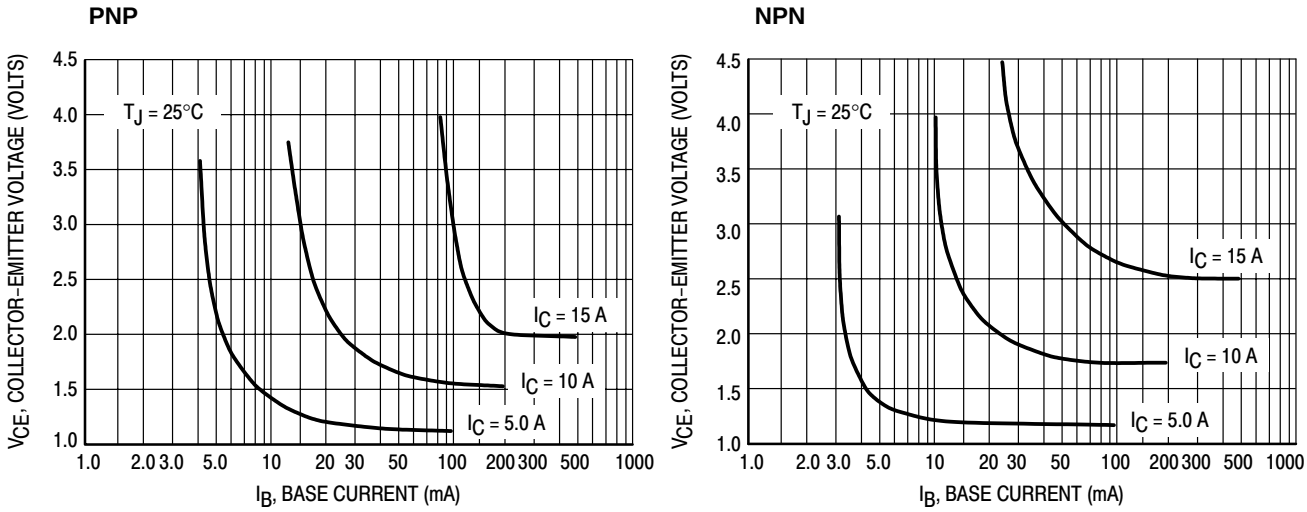


Figure 7. Collector Saturation Region

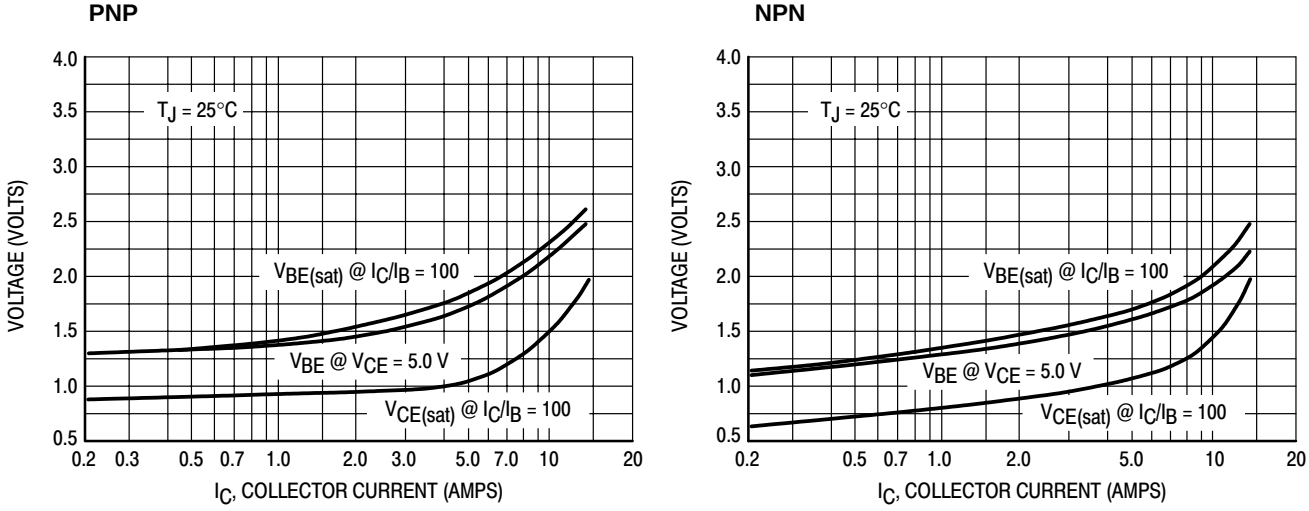


Figure 8. “On” Voltages

PNP **NPN**

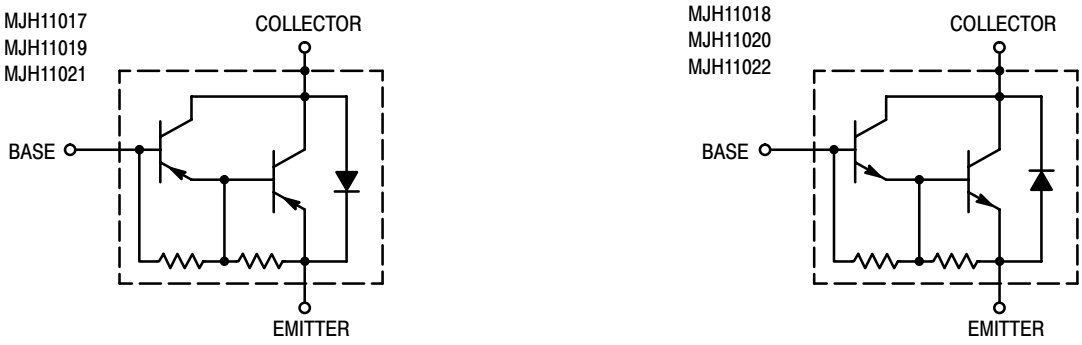


Figure 9. Darlington Schematic

Darlington Complementary Silicon Power Transistors

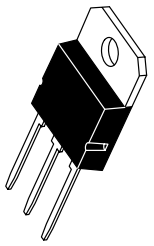
. . . designed for general−purpose amplifier and low−speed switching motor control applications.

- Similar to the Popular NPN 2N6284 and the PNP 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built−in Collector−Emitter Diode

NPN
MJH6284
PNP
MJH6287

ON Semiconductor Preferred Devices

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
100 VOLTS
160 WATTS



CASE 340D−02

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	100	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak	I_C	20 40	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 160 1.28	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	°C/W

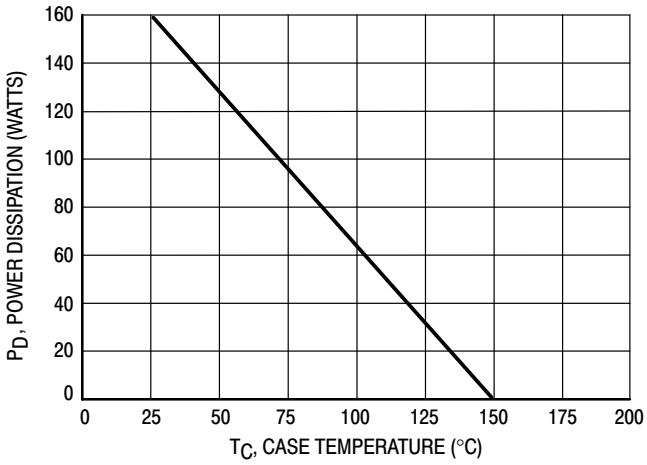


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

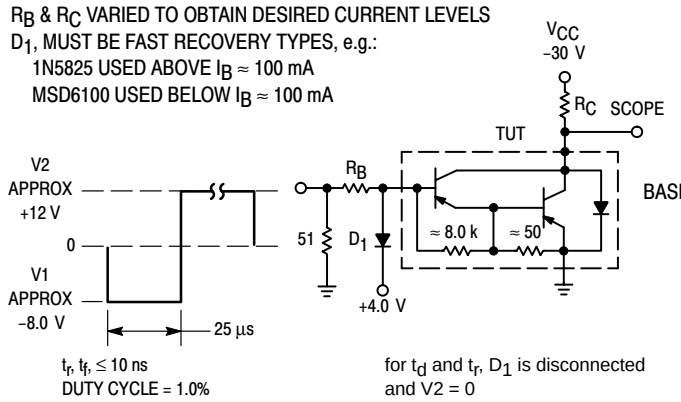
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	750 100	18,000 —	—
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)	$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
Base−Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	4.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJH6284 MJH6287	C_{ob}	— —	400 600	pF
Small−Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)	h_{fe}	300	—	—

SWITCHING CHARACTERISTICS

Resistive Load		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	V_{CC} = 30 Vdc, I_C = 10 Adc I_{B1} = I_{B2} = 100 mA Duty Cycle = 1.0%	t_d	0.1	0.1	μs
Rise Time		t_r	0.3	0.3	
Storage Time		t_s	1.0	1.0	
Fall Time		t_f	3.5	2.0	

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

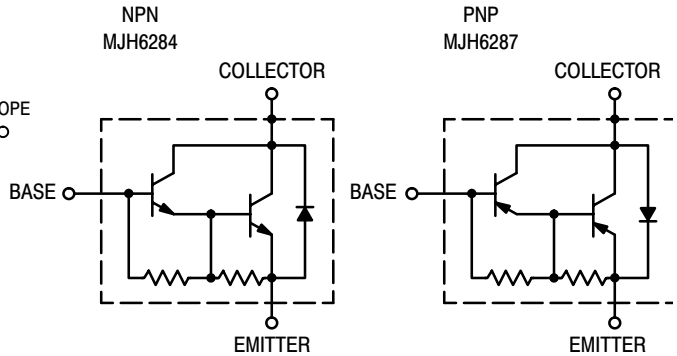


Figure 3. Darlington Schematic

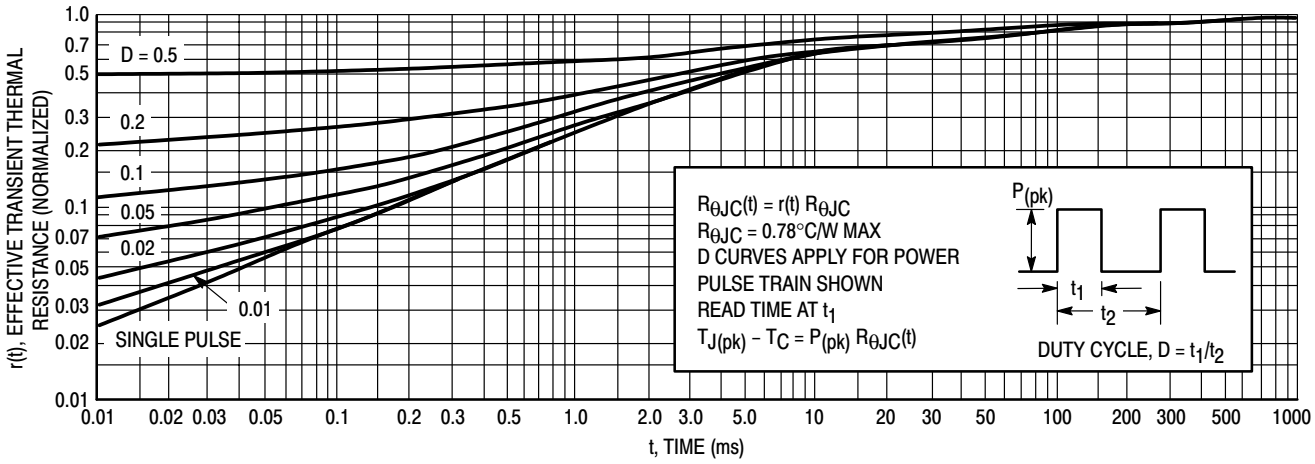


Figure 4. Thermal Response

FBSOA, FORWARD BIAS SAFE OPERATING AREA

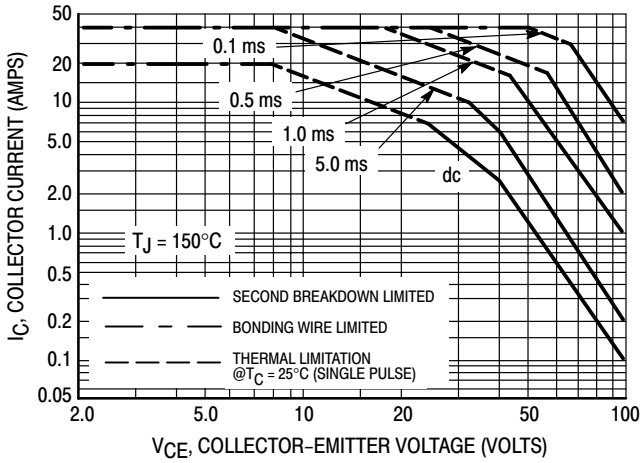


Figure 5. MJH6284, MJH6287

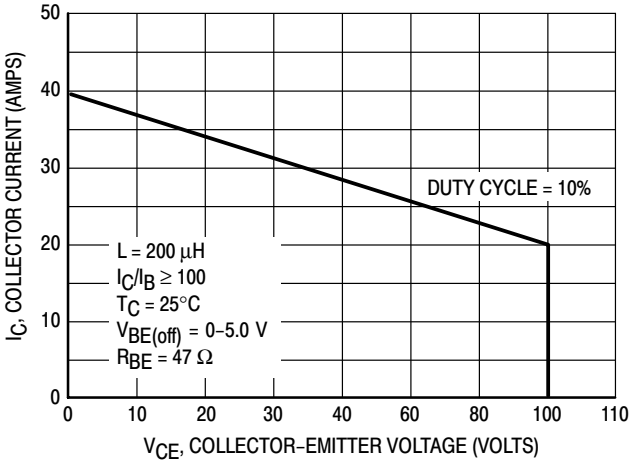


Figure 6. Maximum RBSOA, Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

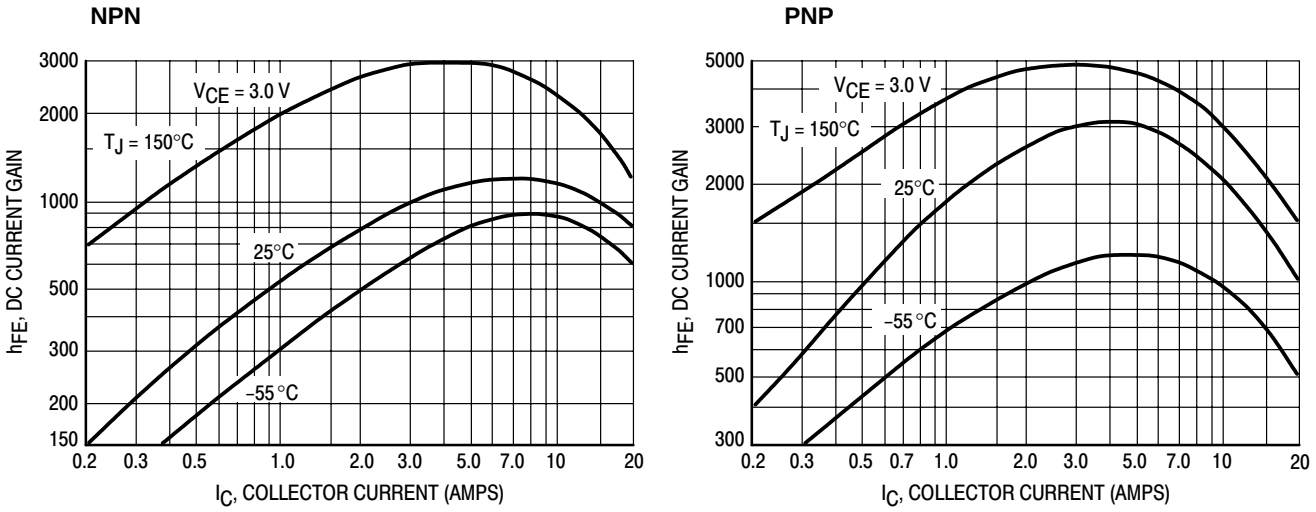


Figure 7. DC Current Gain

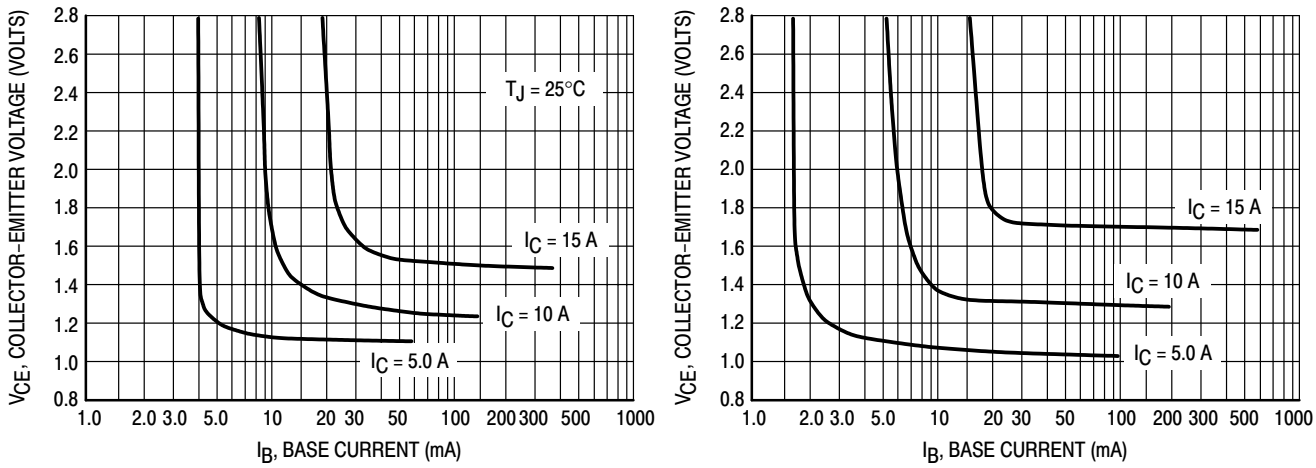


Figure 8. Collector Saturation Region

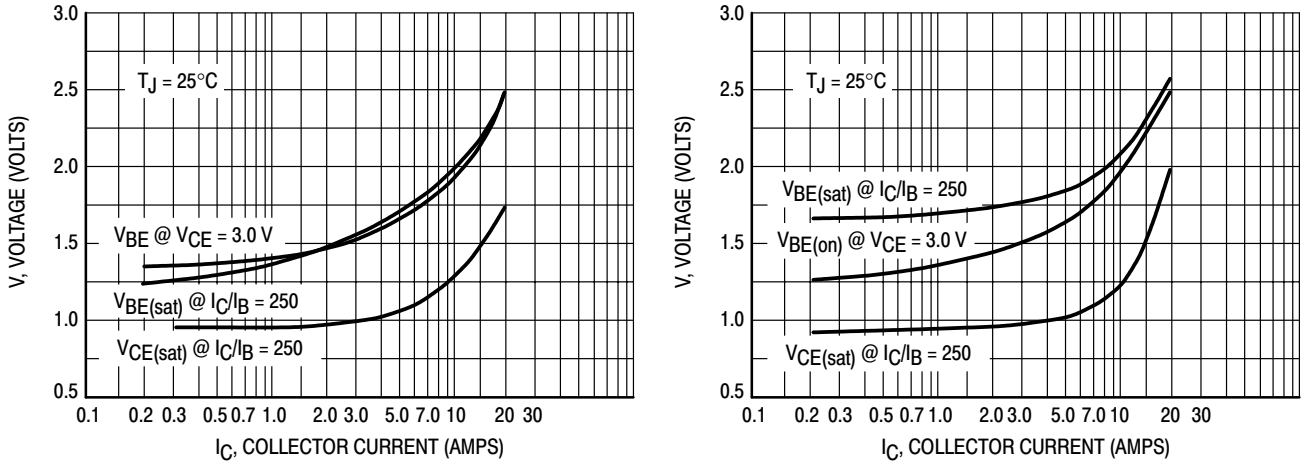


Figure 9. “On” Voltages

PNP
MJL21193*
NPN
MJL21194*

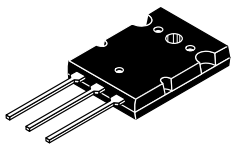
*ON Semiconductor Preferred Device

Silicon Power Transistors

The MJL21193 and MJL21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain − h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



CASE 340G−02 TO−3PBL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current − Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2002 − Rev. 3
Publication Order Number:
MJL21193/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS						
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)		I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non−repetitive)			4.0	—	—	
(V_{CE} = 80 Vdc, t = 1 s (non−repetitive)			2.25	—	—	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				
(I_C = 8 Adc, V_{CE} = 5 Vdc)			25	—	75	
(I_C = 16 Adc, I_B = 5 Adc)			8	—	—	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)		$V_{BE(on)}$	—	—	2.2	Vdc
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			—	—	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)			—	—	4	
DYNAMIC CHARACTERISTICS						
Total Harmonic Distortion at the Output		T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS}	h_{FE} unmatched		—	0.8	—	
(Matched pair h_{FE} = 50 @ 5 A/5 V)	h_{FE} matched		—	0.08	—	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJL21193

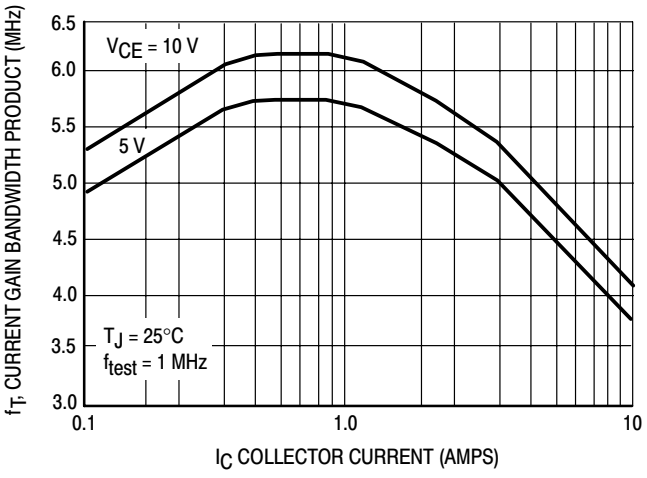


Figure 1. Typical Current Gain Bandwidth Product

NPN MJL21194

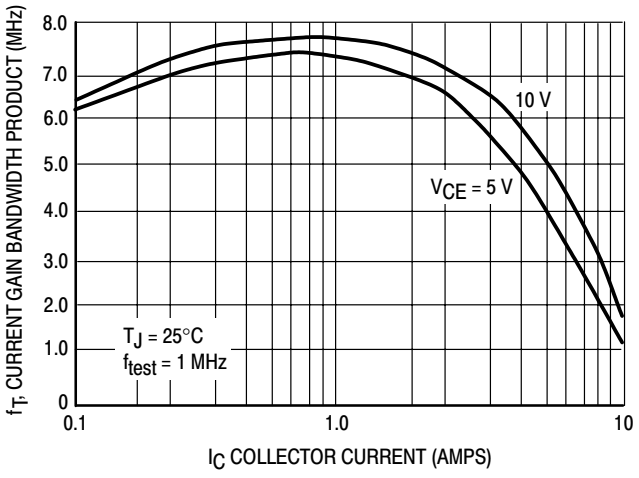


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJL21193

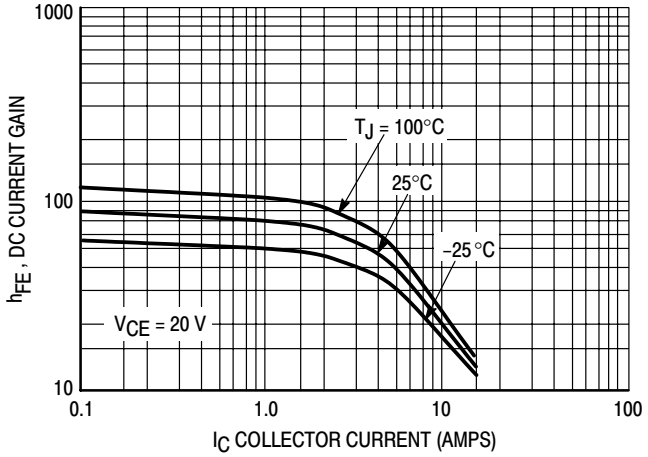


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJL21194

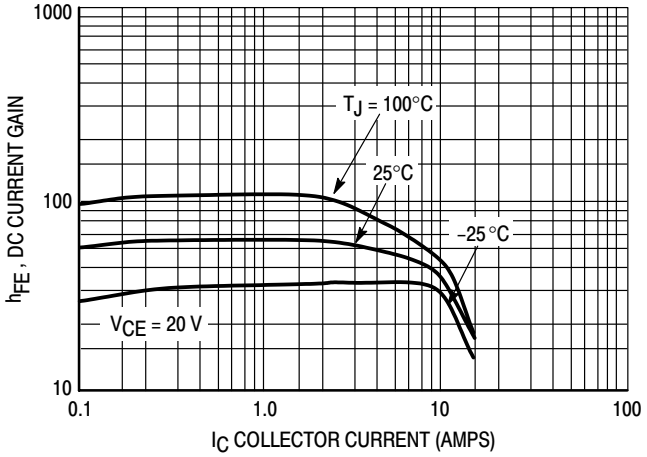


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJL21193

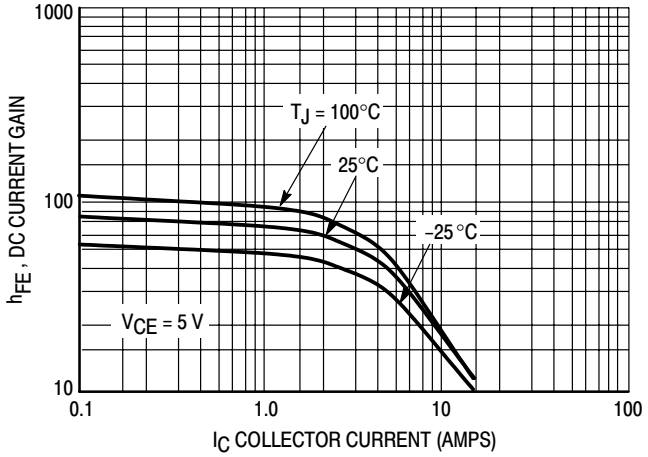


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJL21194

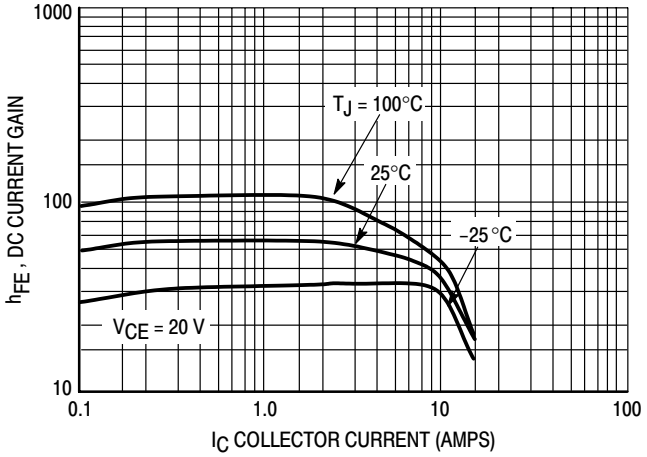
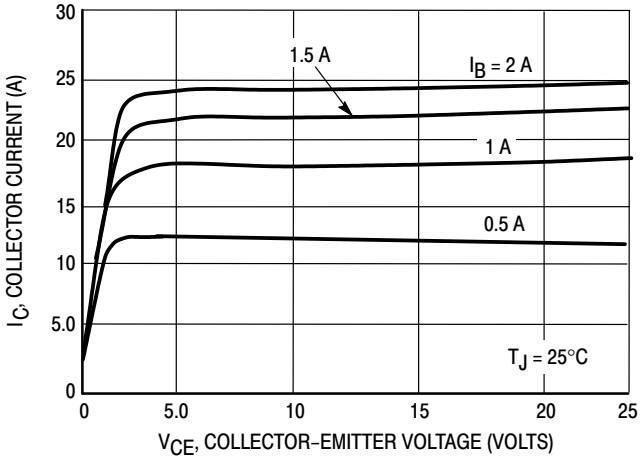
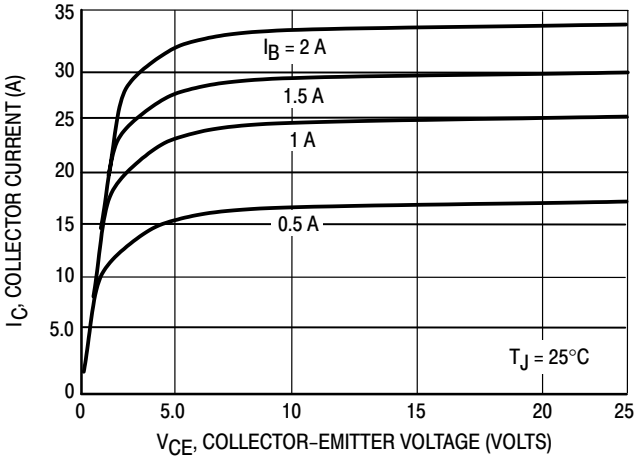


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJL21193



NPN MJL21194



TYPICAL CHARACTERISTICS

PNP MJL21193

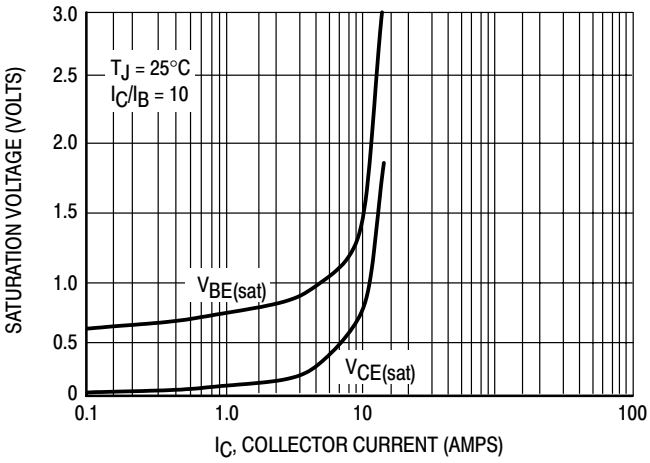


Figure 9. Typical Saturation Voltages

NPN MJL21194

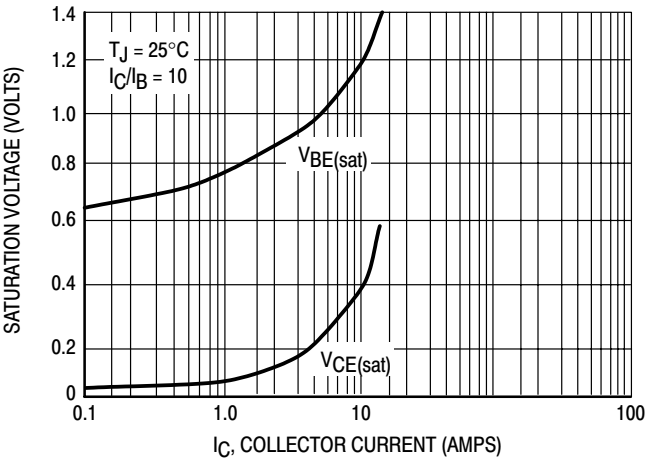


Figure 10. Typical Saturation Voltages

PNP MJL21193

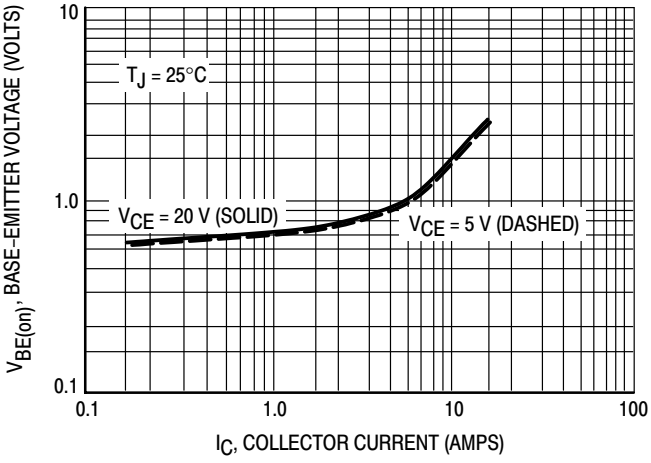


Figure 11. Typical Base−Emitter Voltage

NPN MJL21194

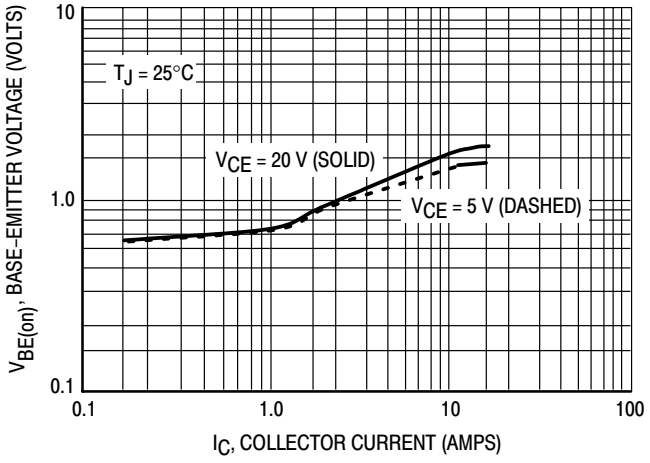


Figure 12. Typical Base−Emitter Voltage

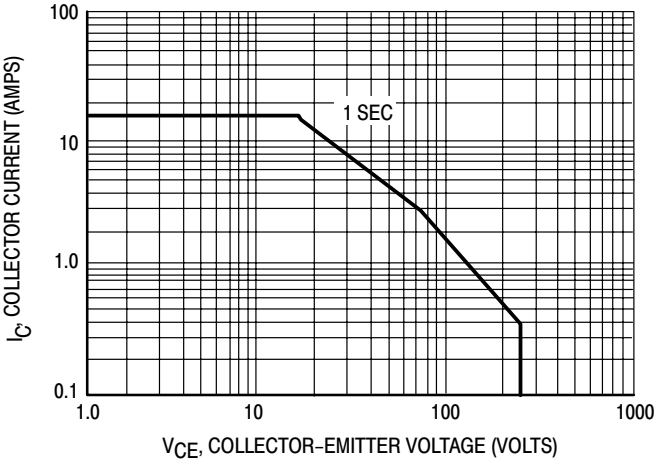


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

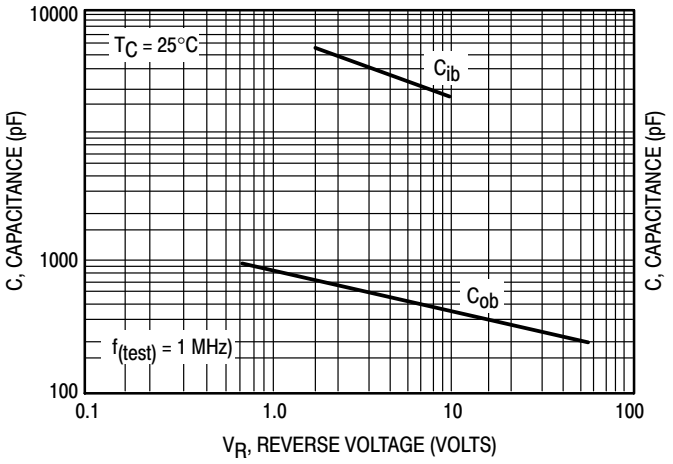


Figure 14. MJL21193 Typical Capacitance

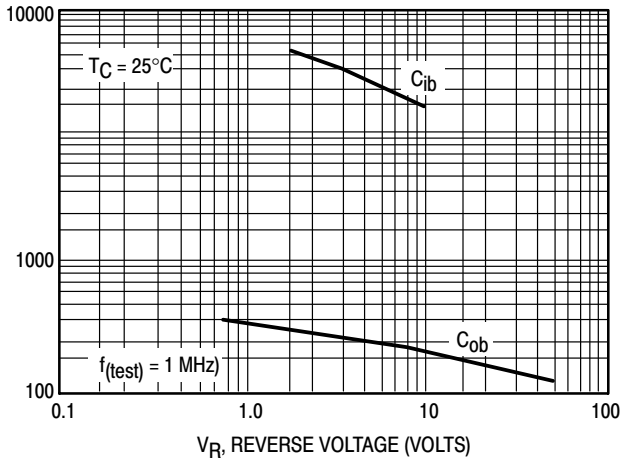


Figure 15. MJL21194 Typical Capacitance

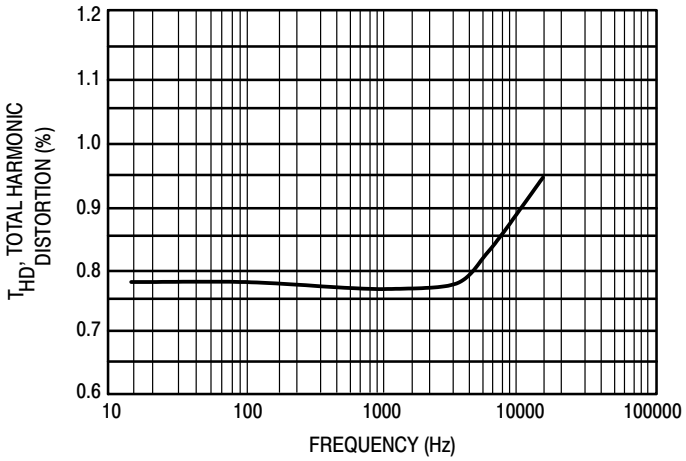


Figure 16. Typical Total Harmonic Distortion

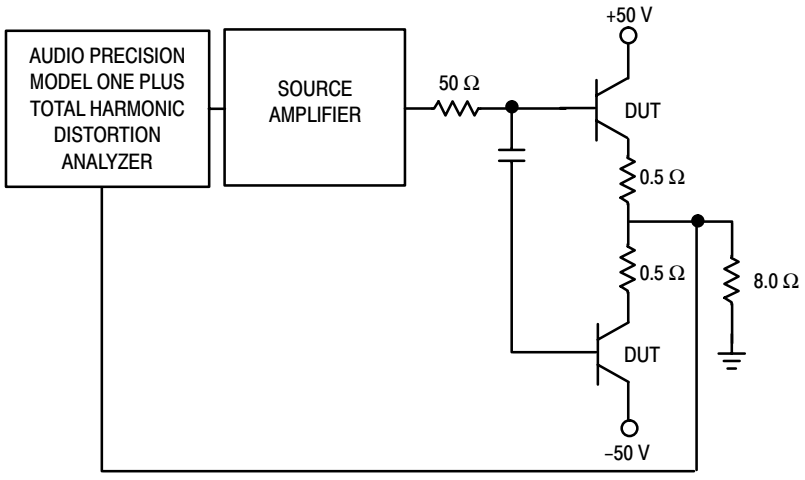


Figure 17. Total Harmonic Distortion Test Circuit

PNP
MJL21195*
NPN
MJL21196*

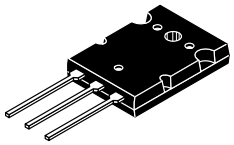
*ON Semiconductor Preferred Device

Silicon Power Transistors

The MJL21195 and MJL21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain − h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.50 A, 80 V, 1 Second

16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



CASE 340G−02 TO−3PBL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current − Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2002 − Rev. 2
Publication Order Number:
MJL21195/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive)) (V_{CE} = 80 Vdc, t = 1 s (non−repetitive))	$I_{S/b}$	 4.0 2.25	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, I_B = 5 Adc)	h_{FE}	 25 8	 — —	 100 —	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 — —	 1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 — —	 0.8 0.08	 — —	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJL21195

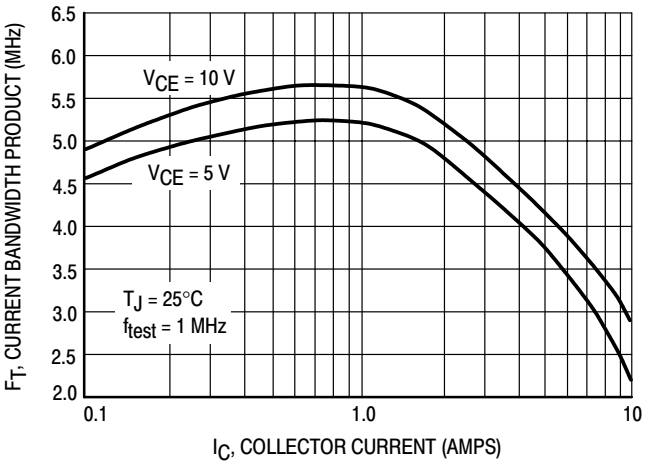


Figure 1. Typical Current Gain Bandwidth Product

NPN MJL21196

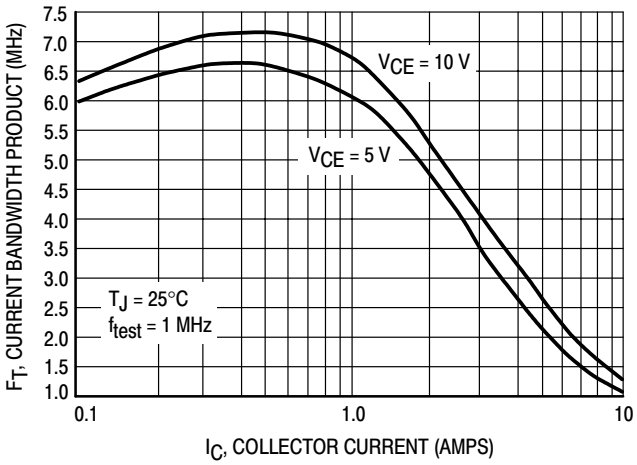


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJL21195

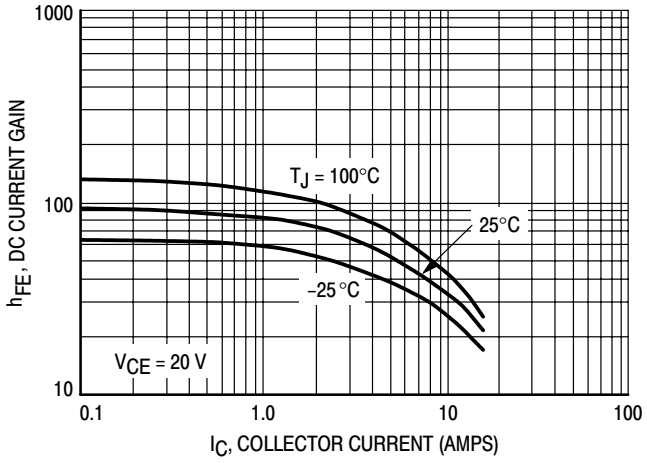


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJL21196

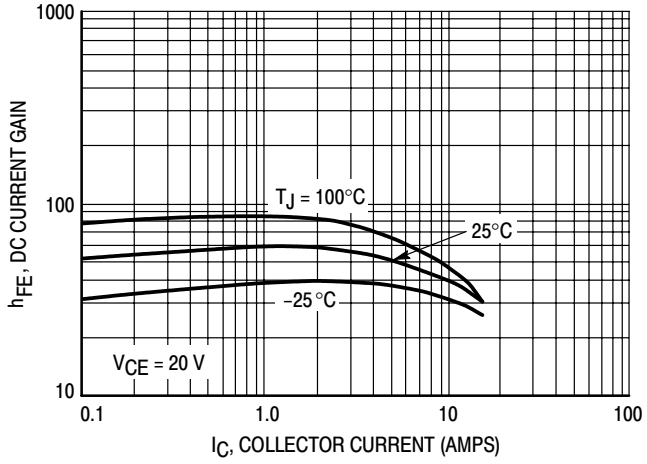


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJL21195

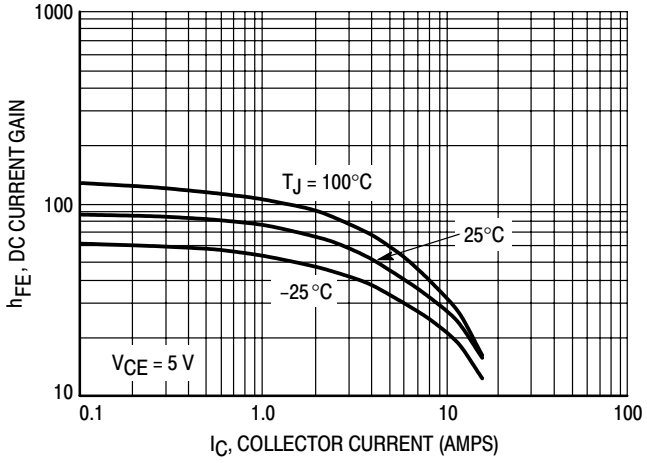


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJL21196

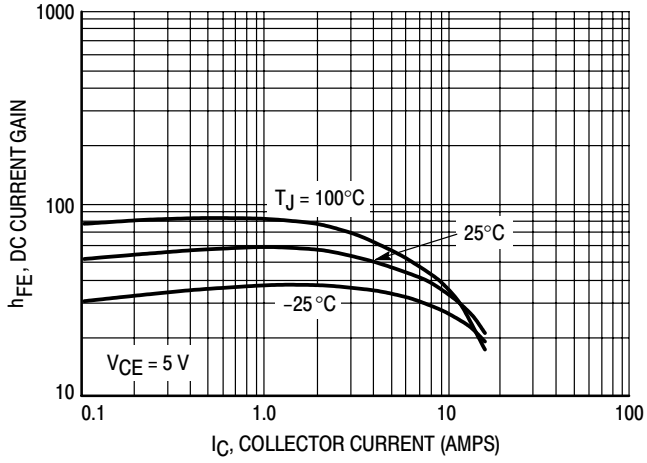


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJL21195

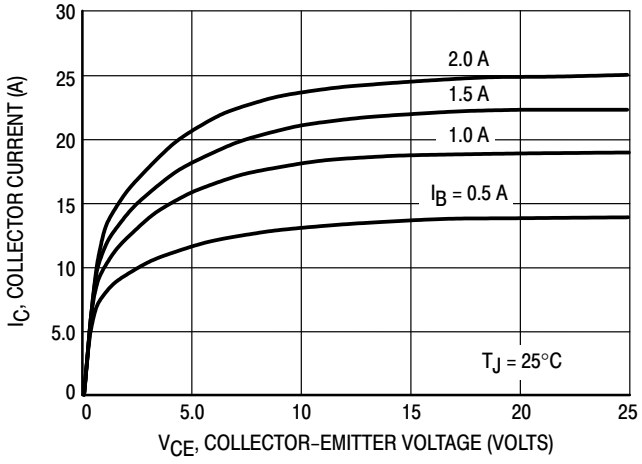


Figure 7. Typical Output Characteristics

NPN MJL21196

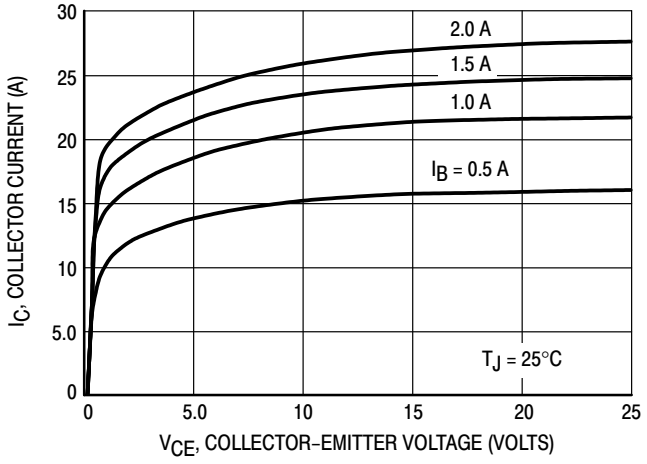


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJL21195

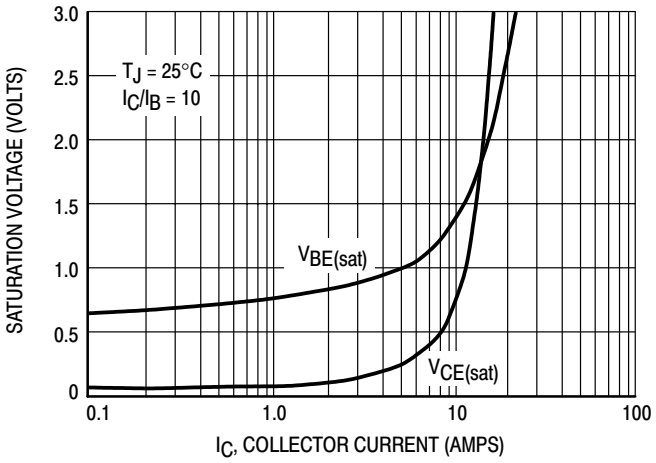


Figure 9. Typical Saturation Voltages

NPN MJL21196

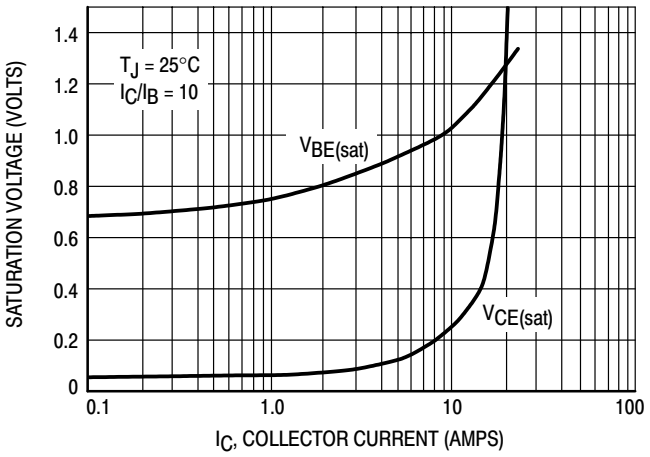


Figure 10. Typical Saturation Voltages

PNP MJL21195

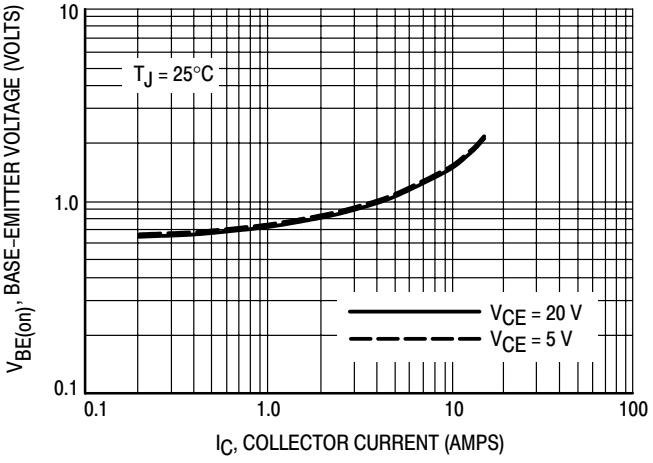


Figure 11. Typical Base−Emitter Voltage

NPN MJL21196

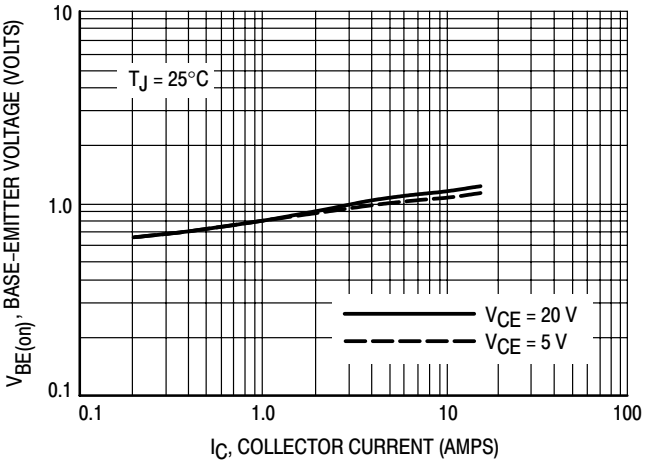


Figure 12. Typical Base−Emitter Voltage

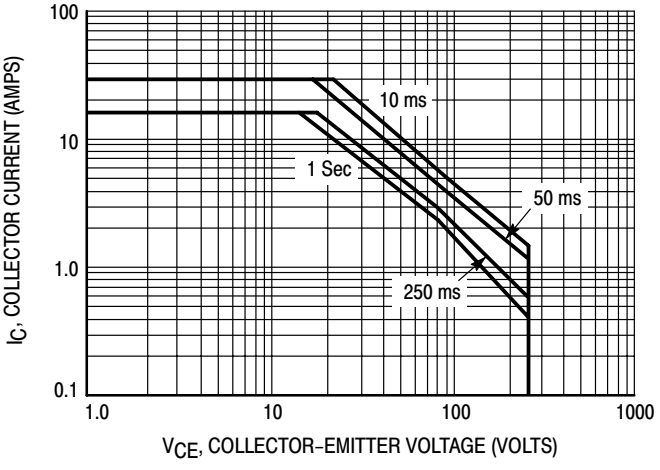


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

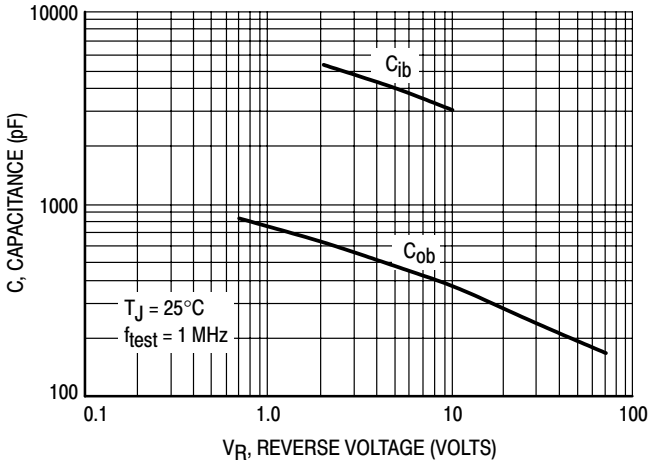


Figure 14. MJL21195 Typical Capacitance

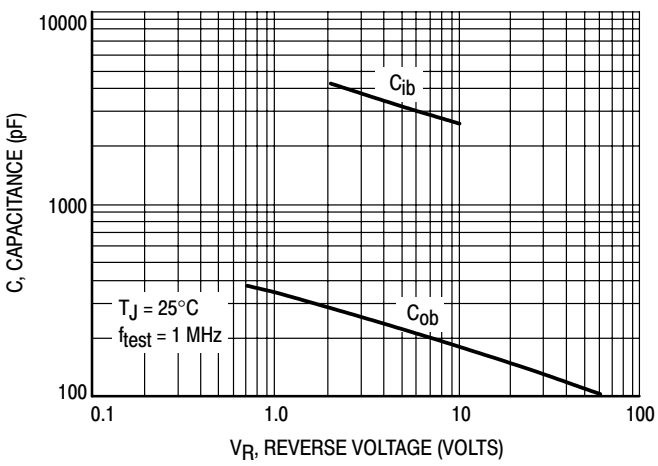


Figure 15. MJL21196 Typical Capacitance

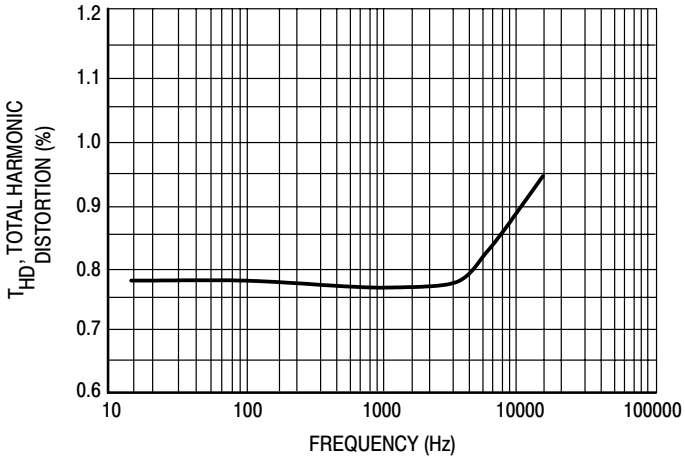


Figure 16. Typical Total Harmonic Distortion

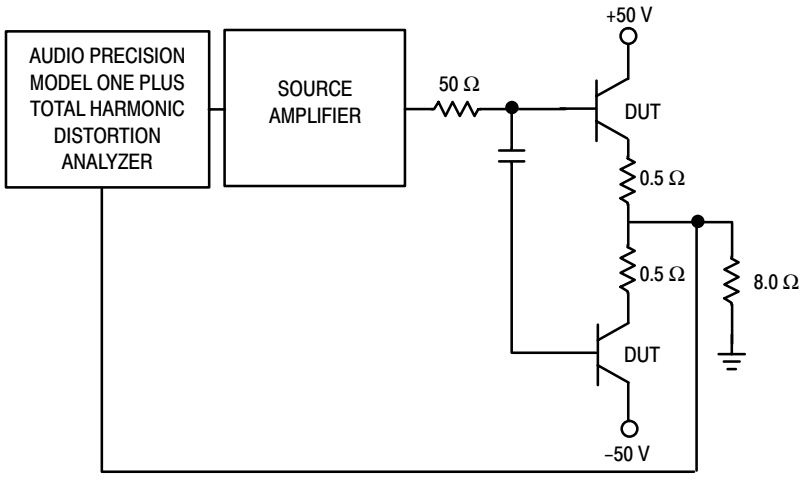


Figure 17. Total Harmonic Distortion Test Circuit

MJL31193 (PNP)
MJL31194 (NPN)

Preferred Devices

Product Preview

Complementary PNP-NPN Silicon Power Transistors

The MJL31193 and MJL31194 are PowerBase™ transistors that are specifically designed for high power audio output.

Features

- High DC Current Gain − h_{FE} = 25 Min @ I_C = 10 A
- Excellent Gain Linearity
- Low Harmonic Distortion
- Ultra High Safe Operation Area

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous − Peak (Note 3)	I_C	20 40	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.84	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.50	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

3. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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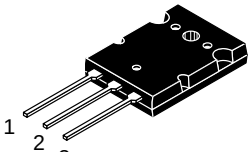
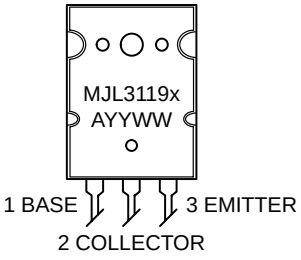
http://onsemi.com

20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 250 WATTS



TO−264
CASE 340G
STYLE 2

MARKING DIAGRAM



x = 3 or 4
A = Location Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJL31193	TO−264	30 Units/Rail
MJL31194	TO−264	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0 Adc)	I_{CEO}	−	−	100	μAdc
Emitter Cutoff Current (V_{CE} = 5.0 Vdc, I_C = 0 Adc)	I_{EBO}	−	−	10	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	−	−	50	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 20 Adc, I_B = 5.0 Adc)	h_{FE}	 25 10	 − −	 75 −	
Base−Emitter On Voltage (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	−	−	1.8	Vdc
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	−	−	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 − −	 0.8 0.08	 − −	%
Current Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	−	−	700	pF

TYPICAL CHARACTERISTICS

PNP MJL31193

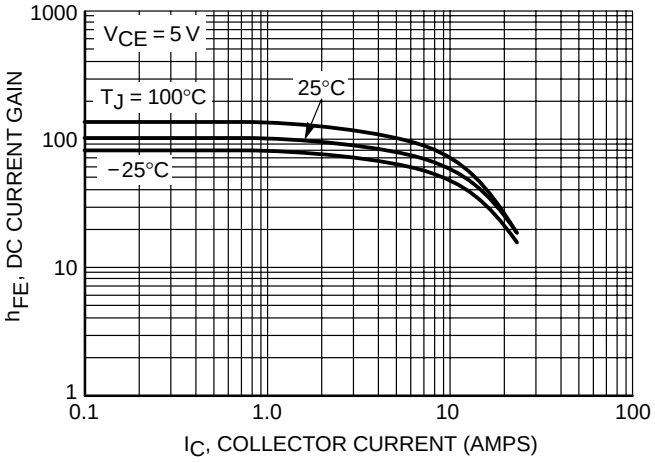


Figure 1. DC Current Gain, V_{CE} = 5 V

NPN MJL31194

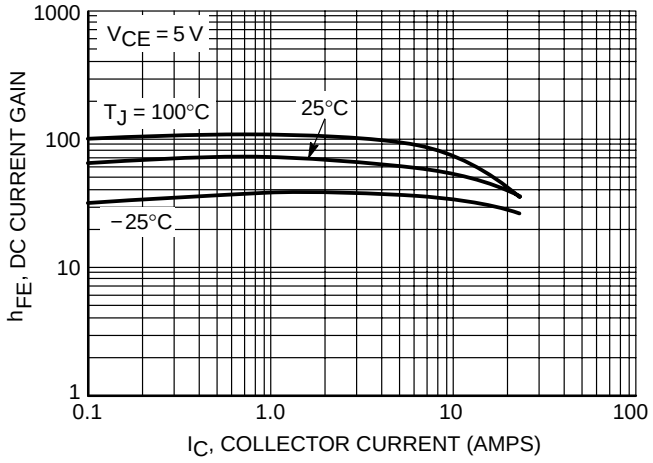


Figure 2. DC Current Gain, V_{CE} = 5 V

PNP MJL31193

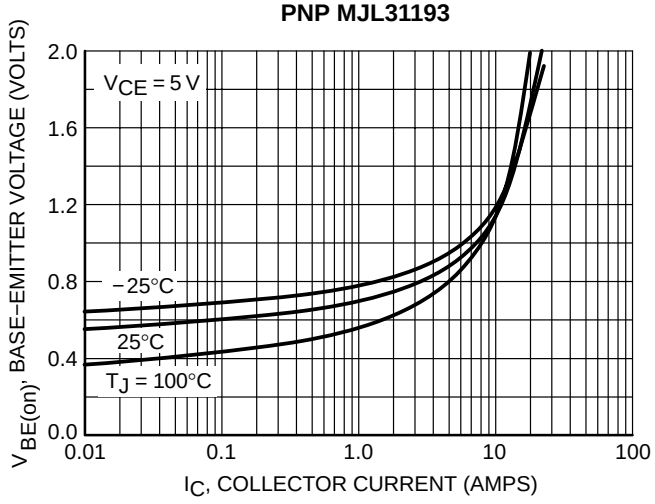


Figure 3. Typical Base−Emitter Voltage

NPN MJL31194

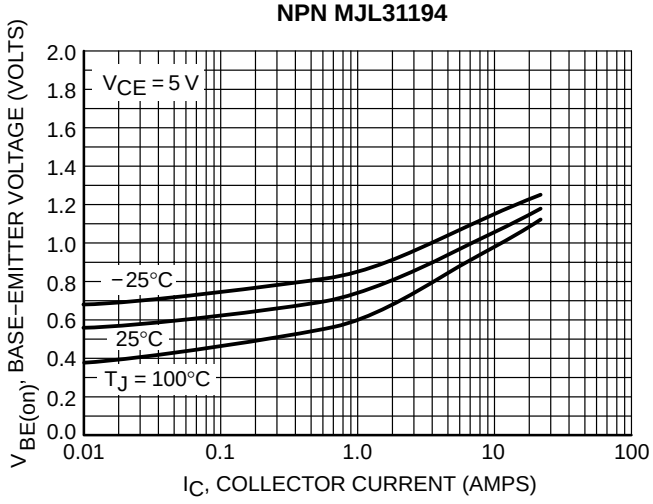


Figure 4. Typical Base−Emitter Voltage

PNP MJL31193

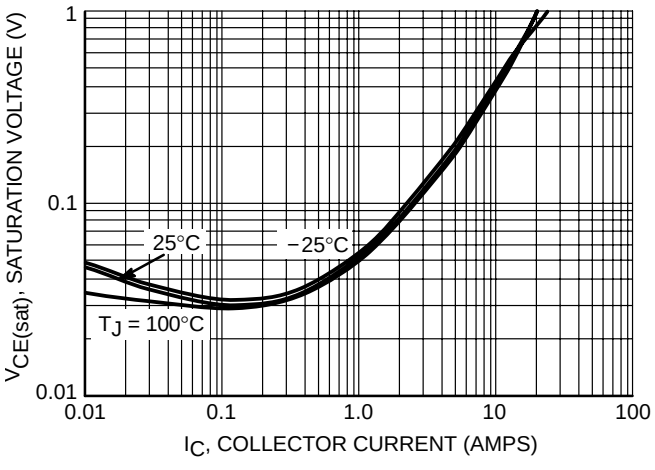


Figure 5. Typical Saturation Voltages

NPN MJL31194

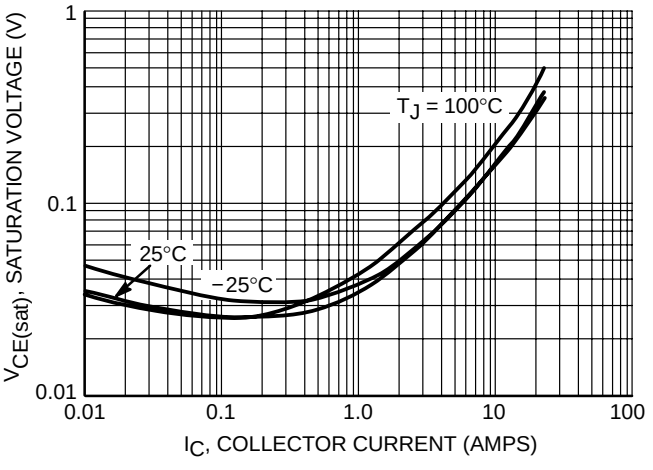


Figure 6. Typical Saturation Voltages

TYPICAL CHARACTERISTICS

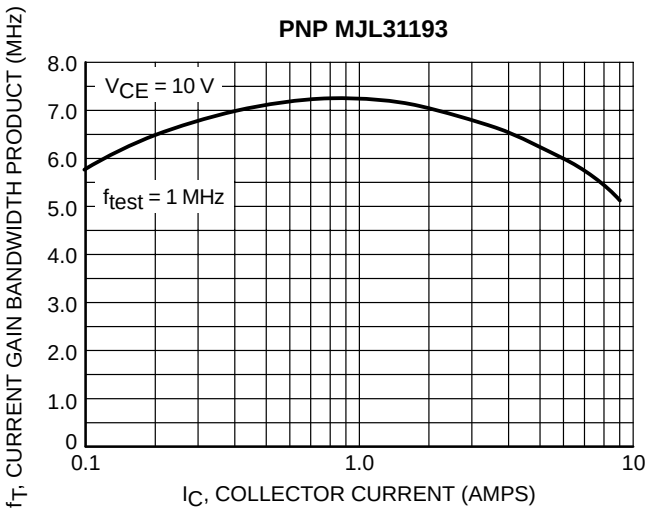


Figure 7. Typical Current Gain Bandwidth Product

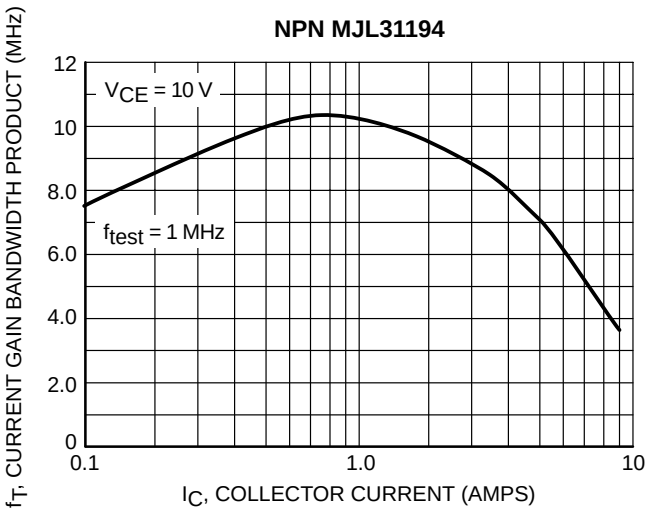


Figure 8. Typical Current Gain Bandwidth Product

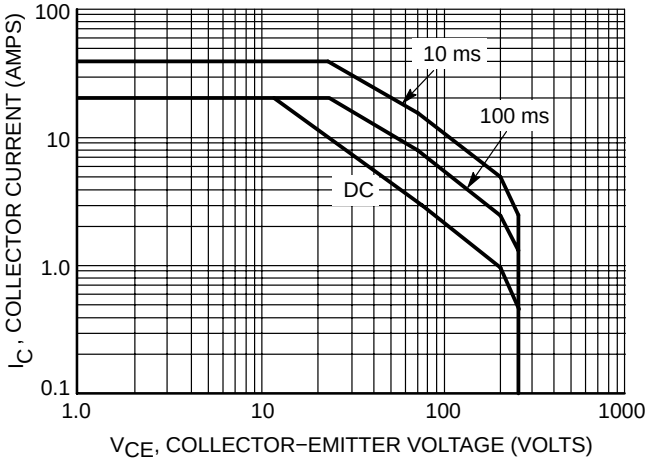


Figure 9. Safe Operating Area

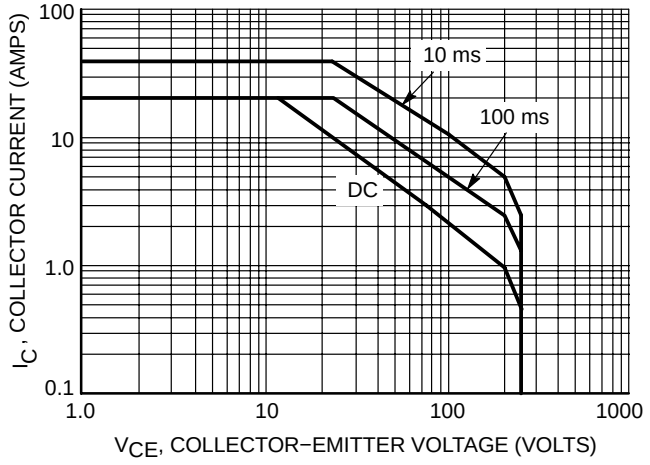


Figure 10. Safe Operating Area

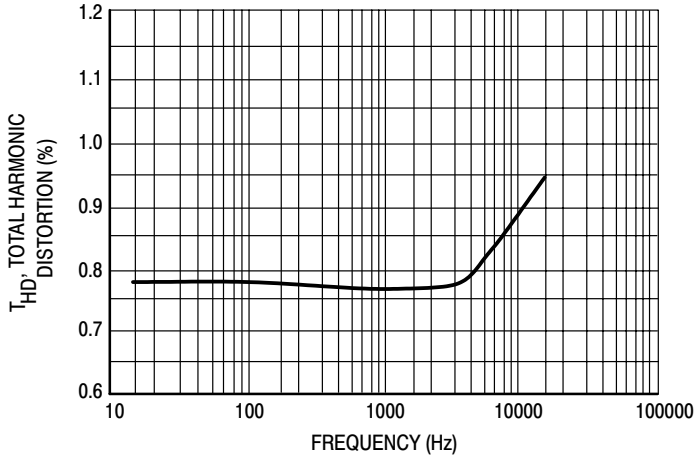


Figure 11. Typical Total Harmonic Distortion

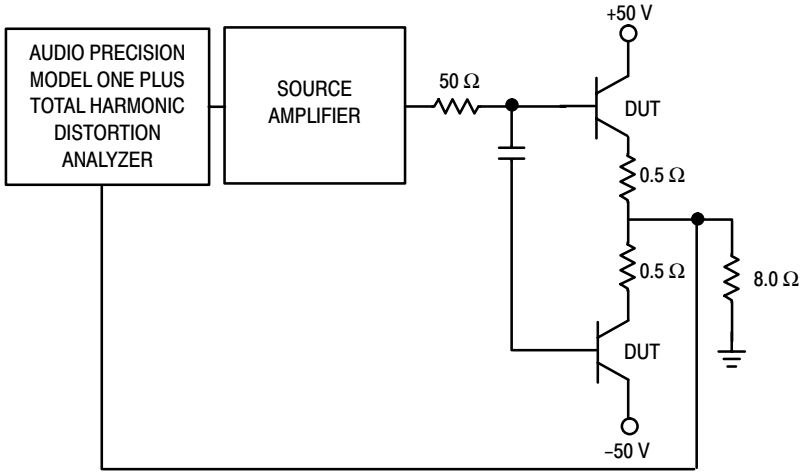


Figure 12. Total Harmonic Distortion Test Circuit

MJL3281A (NPN)
MJL1302A (PNP)

Preferred Devices

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJL3281A and MJL1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  Gain Linearity from 100 mA to 7 A
  High Gain − 60 to 175
  h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area − 1 A/100 V @ 1 Second
- High f_T − 30 MHz Typical
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	230	Vdc
Collector−Base Voltage	V_{CBO}	230	Vdc
Emitter−Base Voltage	V_{EBO}	7	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	230	Vdc
Collector Current − Continuous − Peak (Note 4)	I_C	15 25	Adc
Base Current − Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.7	°C/W

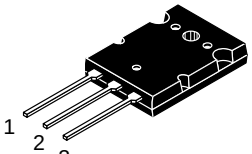
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

4. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

ON Semiconductor®

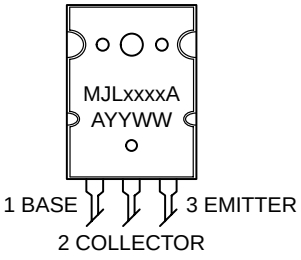
http://onsemi.com

15 AMPERES
COMPLEMENTARY
SILICON POWER
TRANSISTORS
230 VOLTS
200 WATTS



TO−264
CASE 340G
STYLE 2

MARKING DIAGRAM



xxxx = 3281 or 1302
A = Location Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJL3281A	TO−247	30 Units/Rail
MJL1302A	TO−247	30 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	230	−	−	Vdc
Emitter−Base Voltage (I_E = 100 μAdc, I_C = 0)	V_{EBO}	7	−	−	Vdc
Collector Cutoff Current (V_{CB} = 230 Vdc, I_E = 0)	I_{CBO}	−	−	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	−	−	5	μAdc
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}	−	−	25	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive) (V_{CE} = 100 Vdc, t = 1 s (non−repetitive)	$I_{S/b}$	 4 1	 − −	 − −	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc) (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 7 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	 60 60 60 60 60 45 12	 125 − − − 115 − 35	 175 175 175 175 175 − −	
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	−	−	3	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	−	30	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	−	600	pF

TYPICAL CHARACTERISTICS

PNP MJL1302A

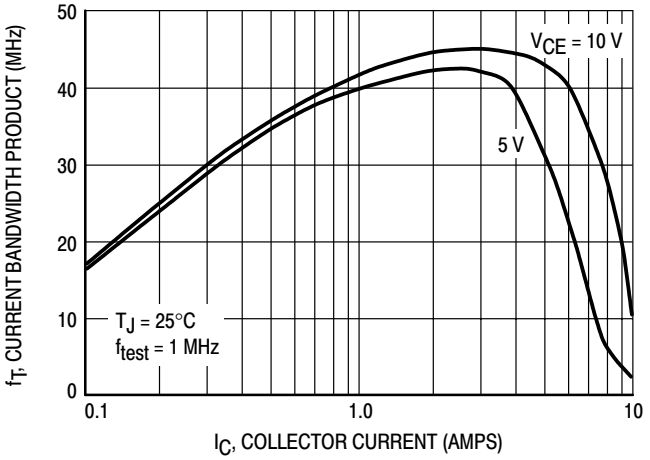


Figure 13. Typical Current Gain Bandwidth Product

NPN MJL3281A

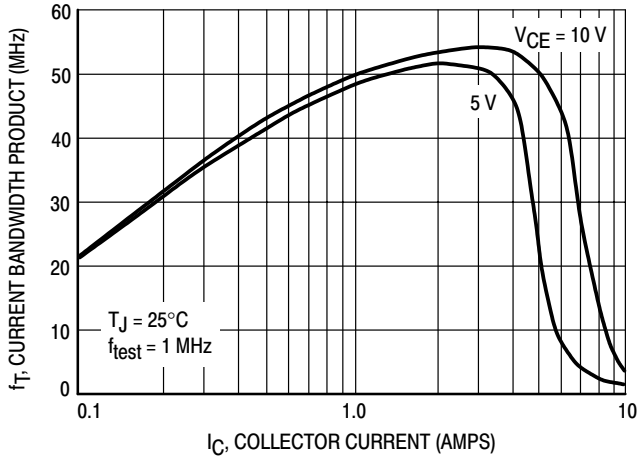


Figure 14. Typical Current Gain Bandwidth Product

PNP MJL1302A

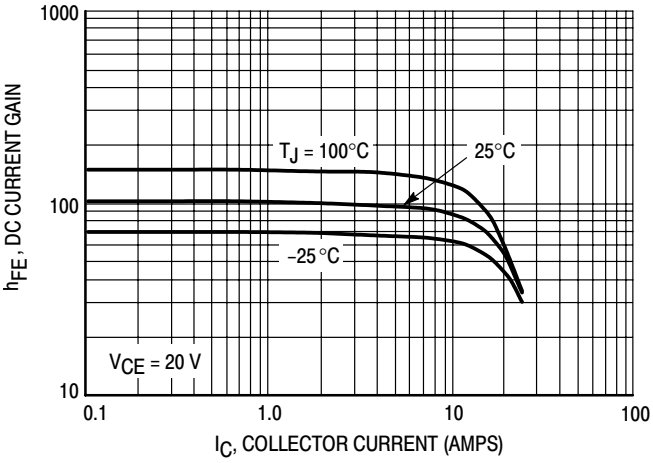


Figure 15. DC Current Gain, V_{CE} = 20 V

NPN MJL3281A

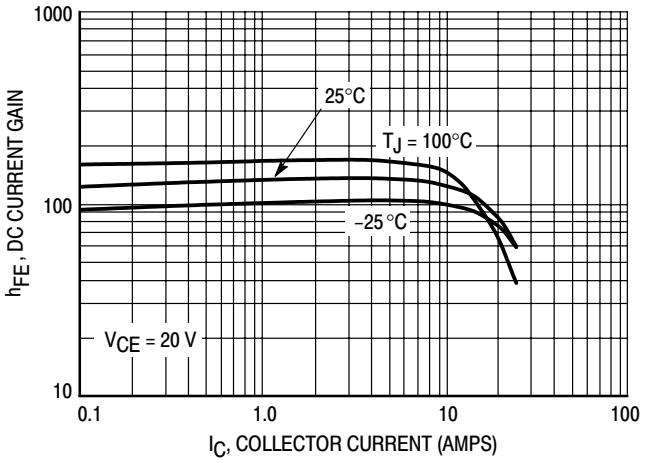


Figure 16. DC Current Gain, V_{CE} = 20 V

PNP MJL1302A

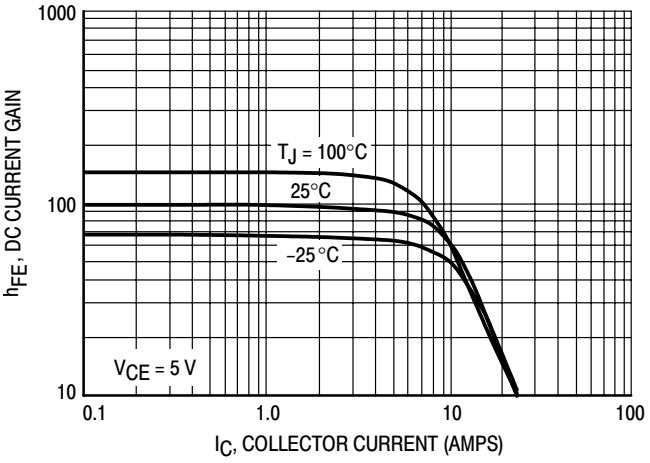


Figure 17. DC Current Gain, V_{CE} = 5 V

NPN MJL3281A

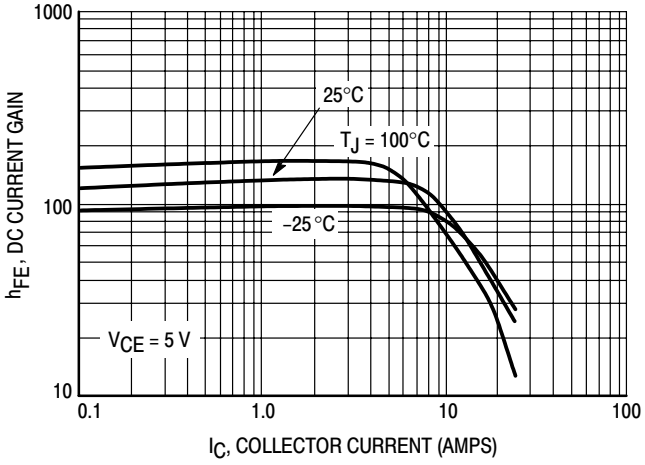


Figure 18. DC Current Gain, V_{CE} = 5 V

TYPICAL CHARACTERISTICS

PNP MJL1302A

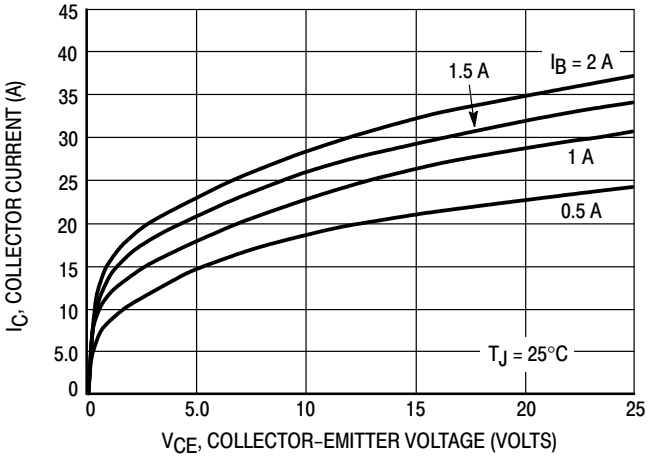


Figure 19. Typical Output Characteristics

NPN MJL3281A

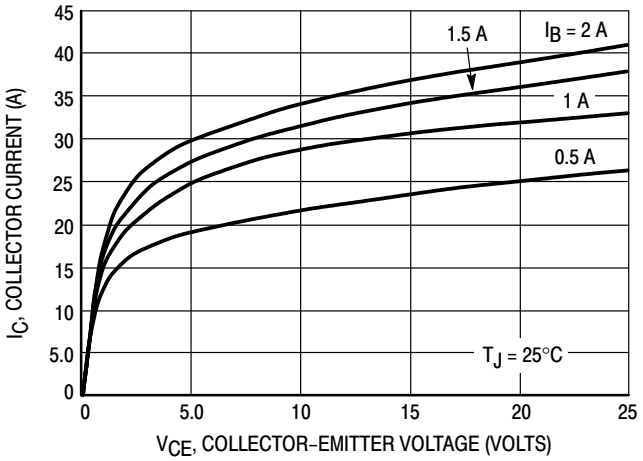


Figure 20. Typical Output Characteristics

PNP MJL1302A

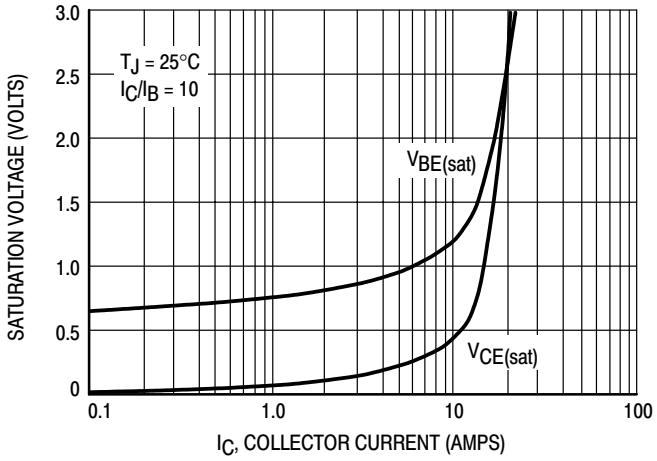


Figure 21. Typical Saturation Voltages

NPN MJL3281A

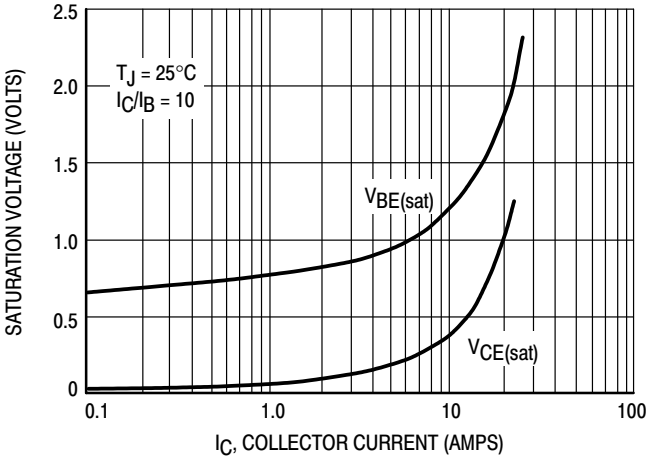


Figure 22. Typical Saturation Voltages

PNP MJL1302A

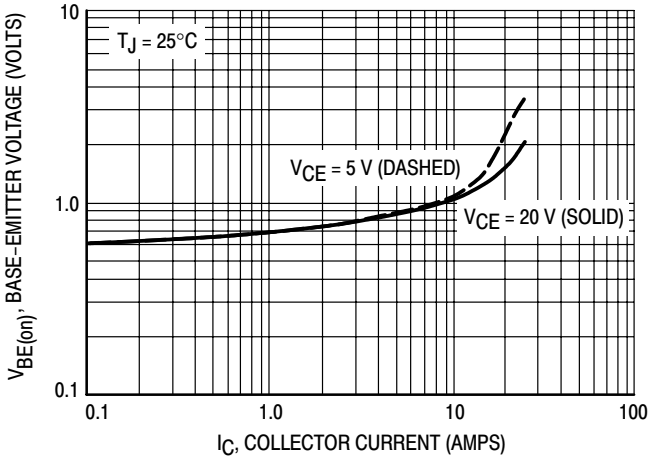


Figure 23. Typical Base−Emitter Voltage

NPN MJL3281A

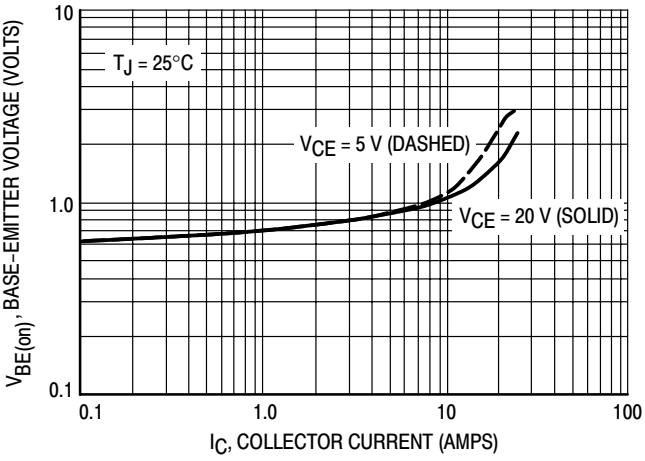


Figure 24. Typical Base−Emitter Voltage

TYPICAL CHARACTERISTICS

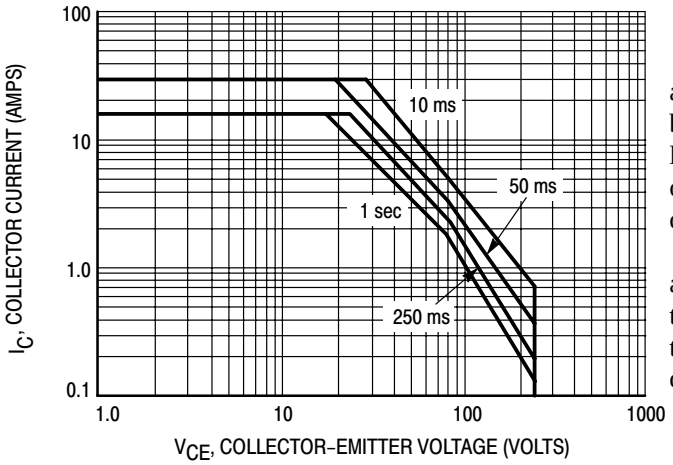


Figure 25. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 25 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

PNP MJL1302A

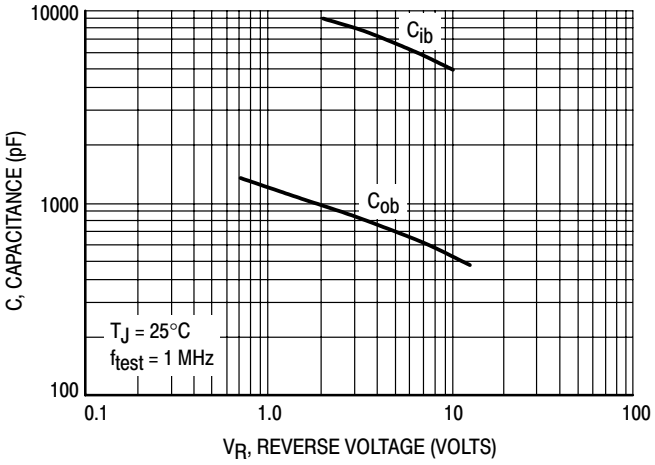


Figure 26. MJL1302A Typical Capacitance

NPN MJL3281A

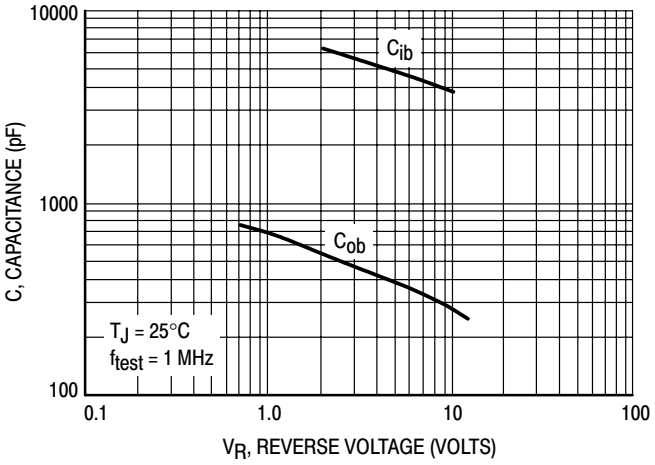


Figure 27. MJL3281A Typical Capacitance

MJL4281A (NPN)
MJL4302A (PNP)

Preferred Device

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJL4281A and MJL4302A are PowerBase™ power transistors for high power audio.

- 350 V Collector−Emitter Sustaining Voltage
- Gain Complementary:
  - Gain Linearity from 100 mA to 5 A
  - High Gain − 80 to 240
  - h_{FE} = 50 (min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area − 1.0 A/100 V @ 1 Second
- High f_T

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	350	Vdc
Collector−Base Voltage	V_{CBO}	350	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	350	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	15 30	Adc
Base Current − Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	230 1.84	Watts °C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.54	°C/W

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

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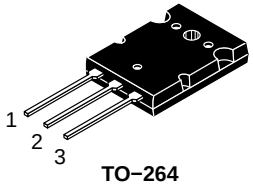
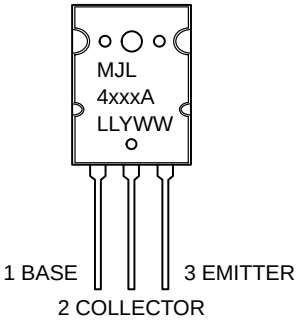
15 AMPERES
COMPLEMENTARY
SILICON POWER
TRANSISTORS
350 VOLTS
230 WATTS



TO−264
CASE 340G
STYLE 2

MARKING DIAGRAM



MJL4xxxA = Device Code
xxx = 281 OR 302
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJL4281A	TO−264	25 Units/Rail
MJL4302A	TO−264	25 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	$V_{CE(sus)}$	350		Vdc
Collector Cut−off Current (V_{CE} = 200 V, I_B = 0)	I_{CEO}		100	μAdc
Collector Cutoff Current (V_{CB} = 350 Vdc, I_E = 0)	I_{CBO}	−	50	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1.0 s (non−repetitive)) (V_{CE} = 100 Vdc, t = 1.0 s (non−repetitive))	$I_{S/b}$	 4.5 1.0	 − −	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 80 80 80 80 50 10	 250 250 250 250 − −	−
Collector−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)	$V_{CE(sat)}$	−	1.0	Vdc
Emitter−Base Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 A)	$V_{BE(sat)}$	−	1.4	Vdc
Base−Emitter ON Voltage (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	35	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	−	600	pF

TYPICAL CHARACTERISTICS

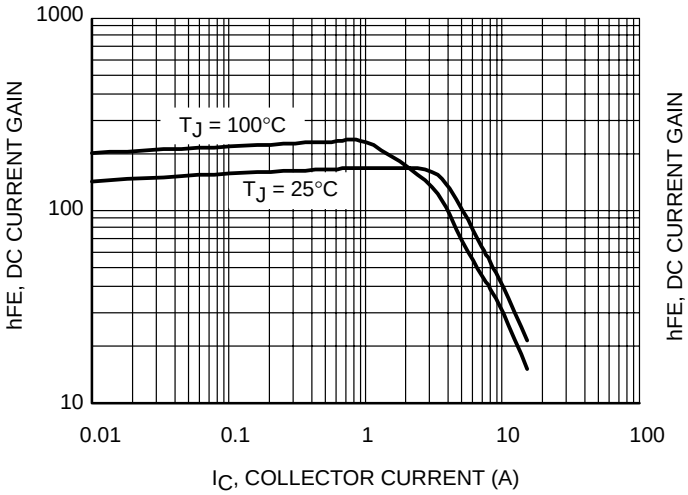


Figure 28. DC Current Gain, V_{CE} = 5 V, NPN MJL4281A

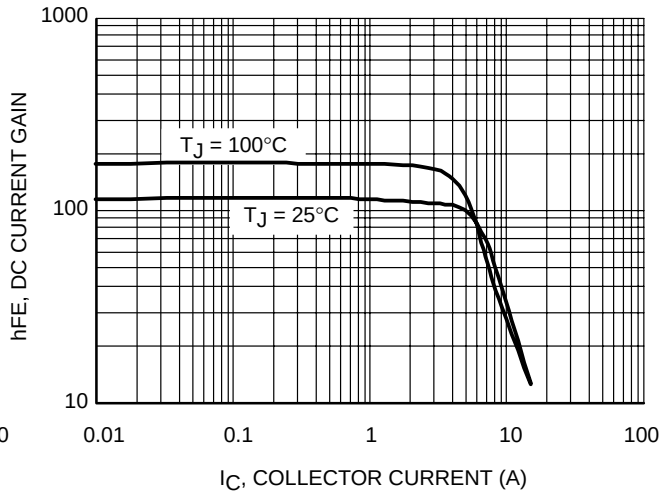


Figure 29. DC Current Gain, V_{CE} = 5 V, PNP MJL4302A

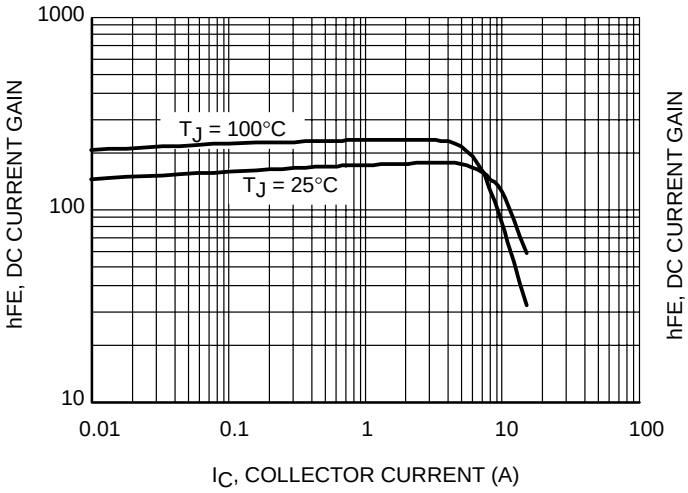


Figure 30. DC Current Gain, V_{CE} = 20 V, NPN MJL4281A

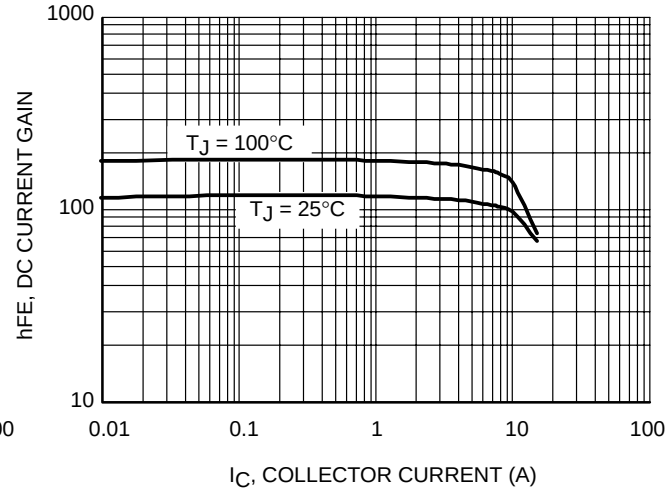


Figure 31. DC Current Gain, V_{CE} = 20 V, PNP MJL4302A

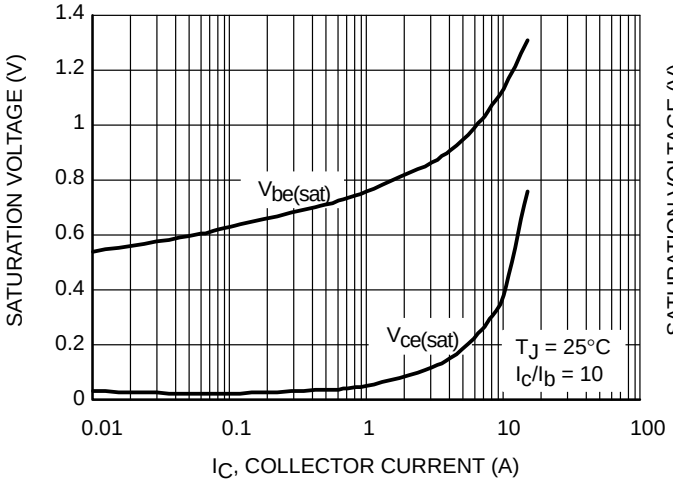


Figure 32. Typical Saturation Voltage, NPN MJL4281A

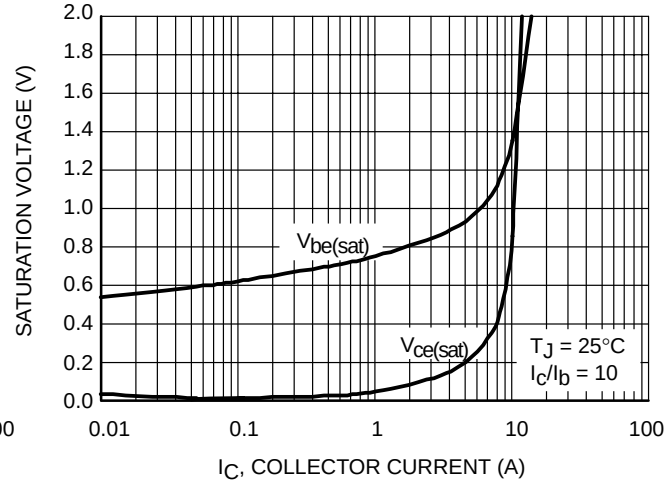


Figure 33. Typical Saturation Voltage, PNP MJL4302A

TYPICAL CHARACTERISTICS

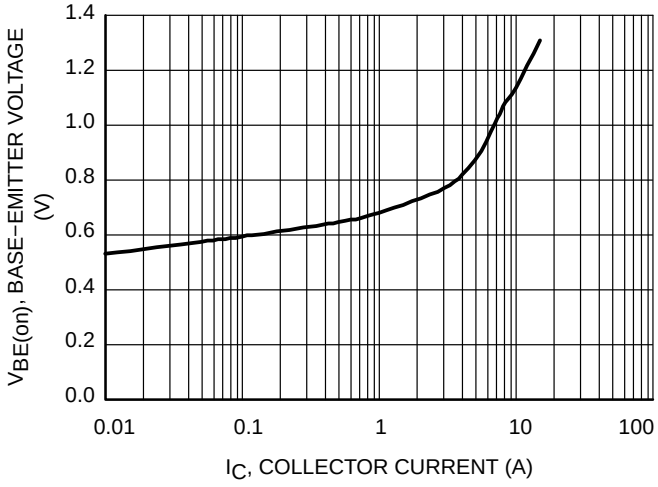


Figure 34. Typical Base−Emitter Voltages, NPN MJL4281A

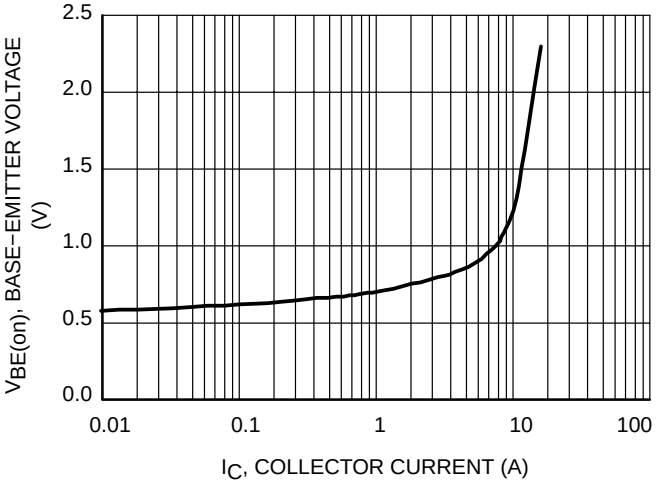


Figure 35. Typical Base−Emitter Voltages, PNP MJL4302A

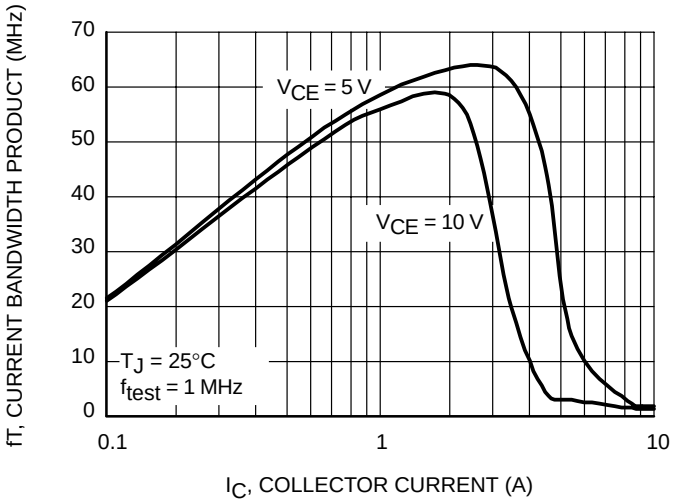


Figure 36. Typical Current Gain Bandwidth Product, NPN MJL4281A

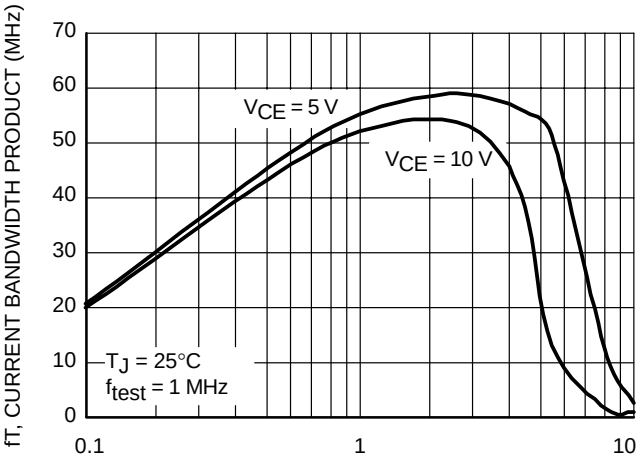


Figure 37. Typical Current Gain Bandwidth Product, PNP MJL4302A

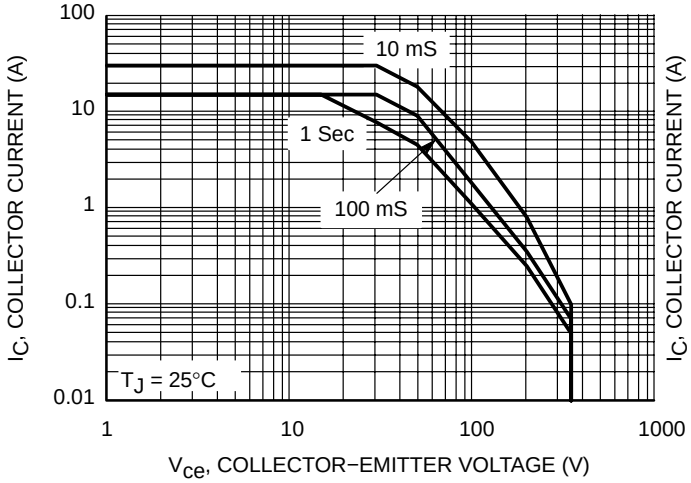


Figure 38. Active Region Safe Operating Area, NPN MJL4281A

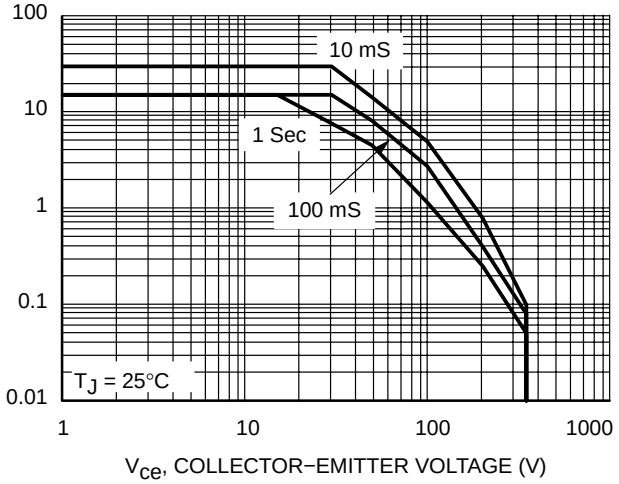


Figure 39. Active Region Safe Operating Area, PNP MJL4302A

MJW0281A (NPN)
MJW0302A (PNP)

Preferred Devices

Advance Information

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJW0281A and MJW0302A are PowerBase™ power transistors for high power audio.

- Designed for 100 W Audio Frequency Applications
- Gain Complementary:
  Gain Linearity from 100 mA to 5.0 A
- Low Harmonic Distortion
- Ultra High Safe Operation Area
- High f_T − 30 MHz (min)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	230	Vdc
Collector−Base Voltage	V_{CBO}	230	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	230	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	15 30	Adc
Base Current − Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.83	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

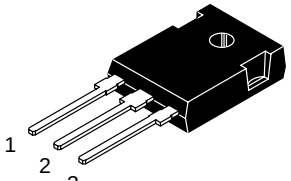
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle < 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor®

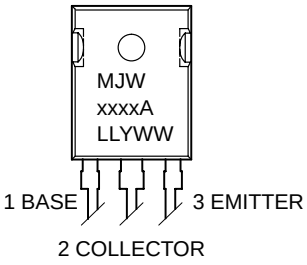
http://onsemi.com

15 AMPERES
COMPLEMENTARY
SILICON POWER
TRANSISTORS
230 VOLTS
150 WATTS



TO−247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJWxxxxA = Device Code
xxxx = 0281 OR 0302
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW0281A	TO−247	30 Units/Rail
MJW0302A	TO−247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	230	−	Vdc
Collector Cutoff Current (V_{CB} = 230 Vdc, I_E = 0)	I_{CBO}	−	50	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	μAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			−
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)		60	180	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		60	180	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)		60	180	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)		60	180	
(I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)		40	−	
Collector−Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	−	1.0	Vdc
Base−Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	−	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	30	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	−	400	pF

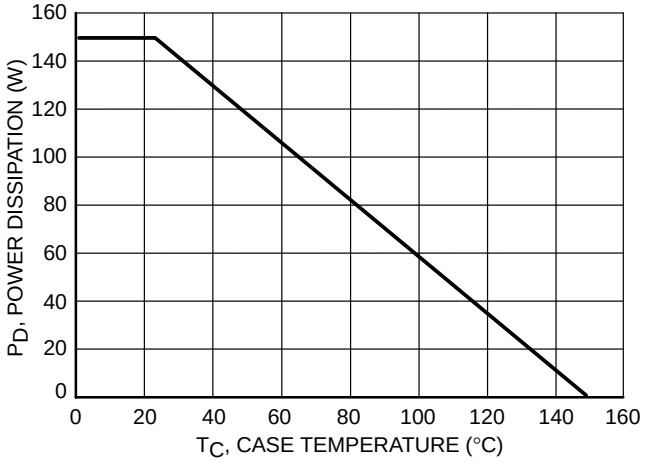


Figure 1. Power Derating

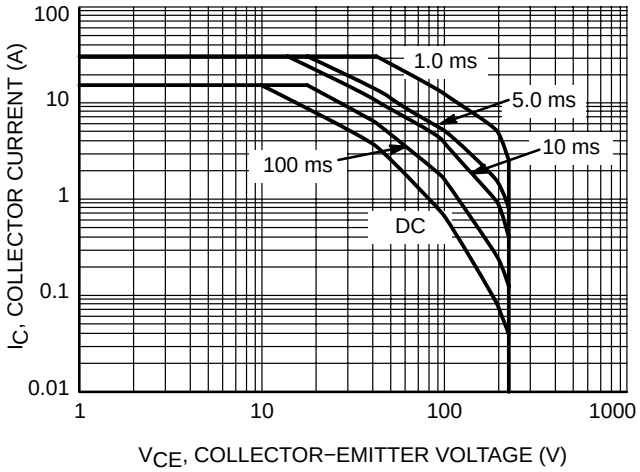


Figure 2. Safe Operating Area

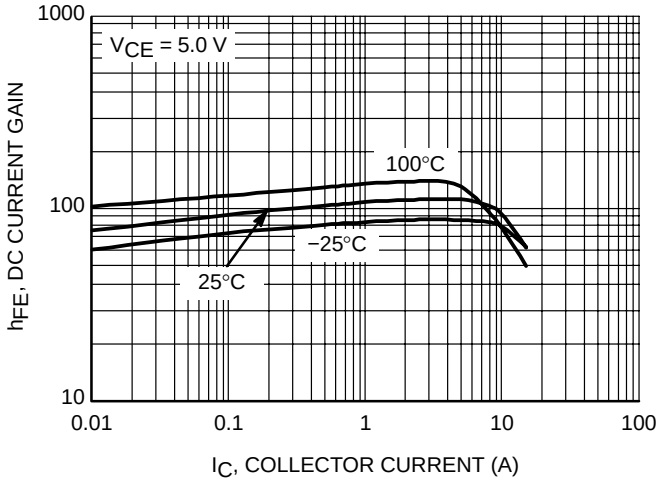


Figure 3. DC Current Gain

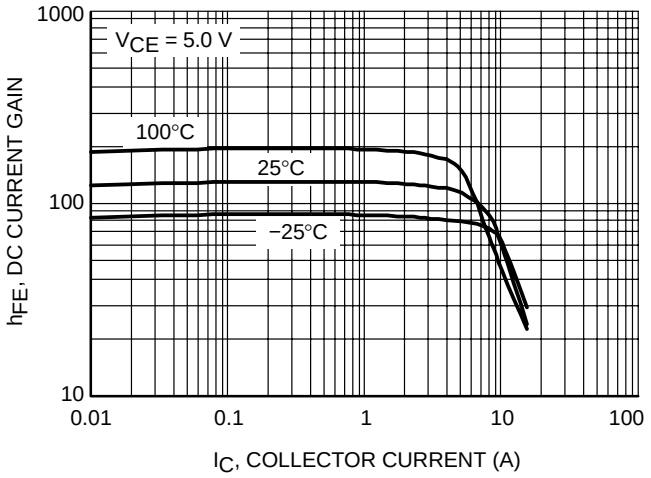


Figure 4. DC Current Gain

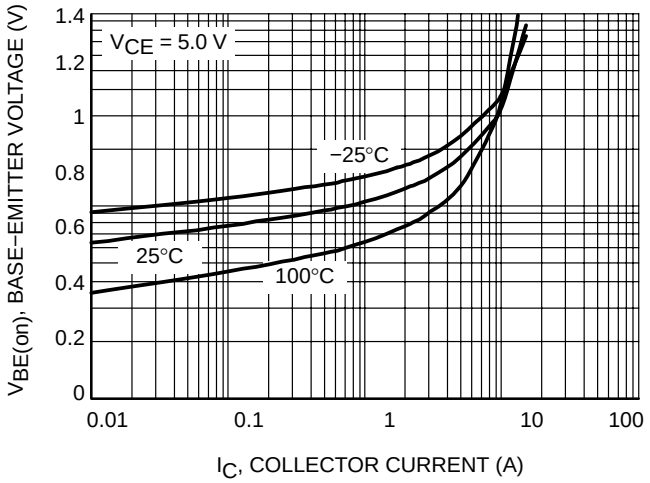


Figure 5. Typical Base−Emitter Voltage

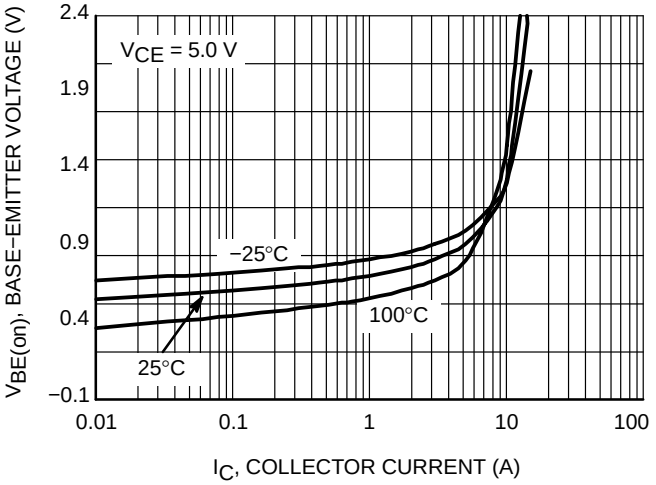


Figure 6. Typical Base−Emitter Voltage

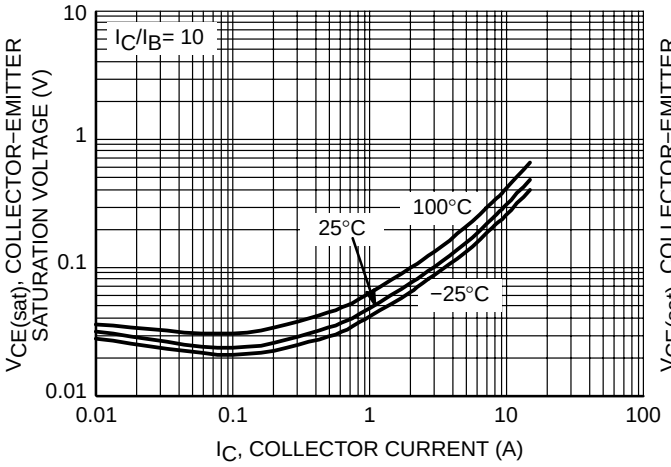


Figure 7. Typical Saturation Voltage

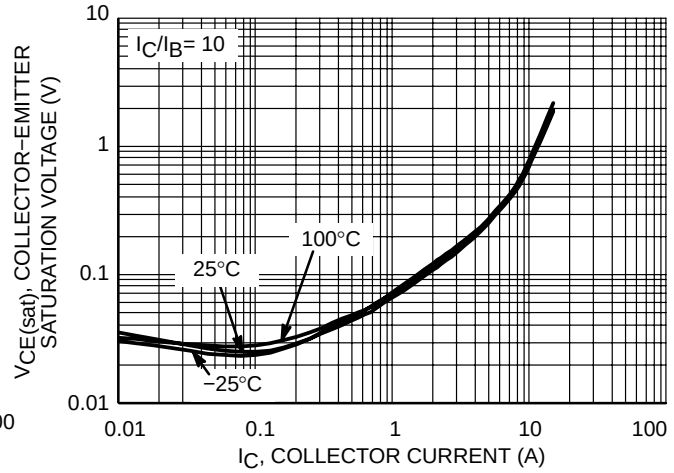


Figure 8. Typical Saturation Voltage

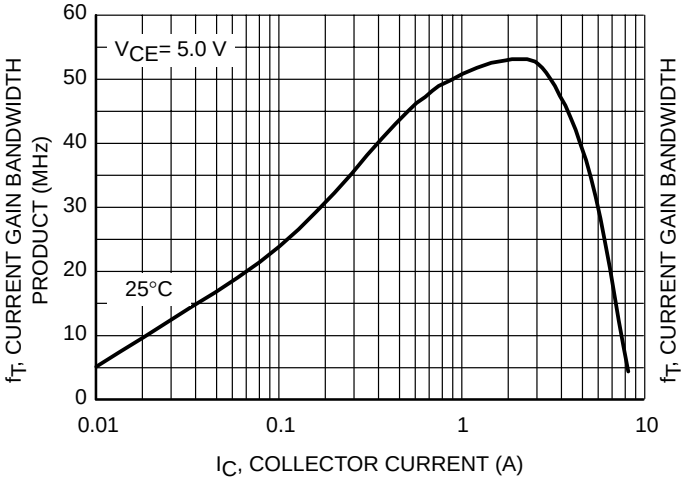


Figure 9. Typical Current Gain Bandwidth Product

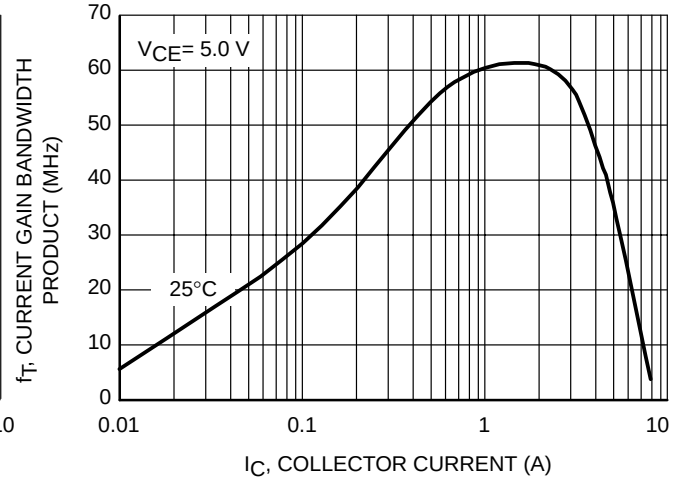


Figure 10. Typical Current Gain Bandwidth Product

MJW18020

Preferred Devices

NPN Silicon Power Transistors High Voltage Planar

The MJW18020 planar High Voltage Power Transistor is specifically Designed for motor control applications, high power supplies and UPS's for which the high reproducibility of DC and Switching parameters minimizes the dead time in bridge configurations.

Mains features include:

- High and Excellent Gain Linearity
- Fast and Very Tight Switching Times Parameters t_{si} and t_{fi}
- Very Stable Leakage Current due to the Planar Structure
- High Reliability

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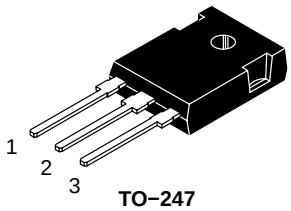
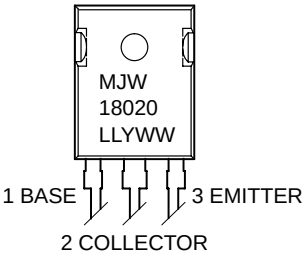
30 AMPERES
1000 VOLTS BV_{CES}
450 VOLTS BV_{CEO}
250 WATTS



TO−247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW18020= Device Code
LL = Location Code
Y = Year
WW = Work Week

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Base Breakdown Voltage	V_{CES}	1000	Vdc
Collector−Base Voltage	V_{CBO}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	9.0	Vdc
Collector Current − Continuous − Peak (Note 1.)	I_C	30 45	Adc
Base Current − Continuous − Peak (Note 1.)	I_B	6.0 10	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

2. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

ORDERING INFORMATION

Device	Package	Shipping
MJW18020	TO−247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	450	−	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	−	−	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	−	−	100	μAdc
(T_C = 125°C)		−	−	500	
Emitter Cutoff Current (V_{CE} = 9 Vdc, I_C = 0)	I_{EBO}	−	−	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3 Adc, V_{CE} = 5 Vdc)	h_{FE}	14		34	
(T_C = 125°C)		−	30	−	
(I_C = 10 Adc V_{CE} = 2 Vdc)		8	16		
(T_C = 125°C)		5	14	−	
(I_C = 20 Adc V_{CE} = 2 Vdc)		5.5	9	−	
(T_C = 125°C)		4	7	−	
(I_C = 10 mAdc V_{CE} = 5 Vdc)		14	25	−	
Base−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc)	$V_{BE(sat)}$	−	0.97	1.25	Vdc
(I_C = 20 Adc, I_B = 4 Adc)			1.15	1.5	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)		−	0.2	0.6	
(T_C = 125°C)		−	0.3	−	
(I_C = 20 Adc, I_B = 4 Adc)		−	0.5	1.5	
(T_C = 125°C)		−	0.9	2.0	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	−	13	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	300	500	pF
Input Capacitance (V_{EB} = 8.0)	C_{ib}	−	7000	9000	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. = 10%, Pulse Width = 70 μs)					
Turn−On Time (I_C = 10 Adc, I_{B1} = I_{B2} = 2 Adc, Vcc = 125 V)	t_{On}	−	540	750	ns
Storage Time	t_s	−	4.75	6	μs
Fall Time	t_f	−	380	500	ns
Turn−Off Time	t_{Off}	−	5.2	6.5	μs
Turn−On Time (I_C= 20 Adc, I_{B1} = I_{B2} = 4 Adc, Vcc = 125 V)	t_{On}	−	965	1200	ns
Storage Time	t_s	−	2.9	3.5	μs
Fall Time	t_f	−	350	500	ns
Turn−Off Time	t_{Off}	−	3.25	4	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp}= 300 V , Vcc = 15 V, L = 200 μH)					
Fall Time (I_C = 10 Adc, I_{B1} = I_{B2} = 2 Adc)	t_{fi}	−	142	250	ns
Storage Time	t_{si}	−	4.75	6	μs
Crossover Time	t_c	−	320	500	ns
Fall Time (I_C = 20 Adc, I_{B1} = I_{B2} = 4 Adc)	t_{fi}	−	350	500	ns
Storage Time	t_{si}	−	3.0	3.5	μs
Crossover Time	t_c	−	500	750	ns

TYPICAL CHARACTERISTICS

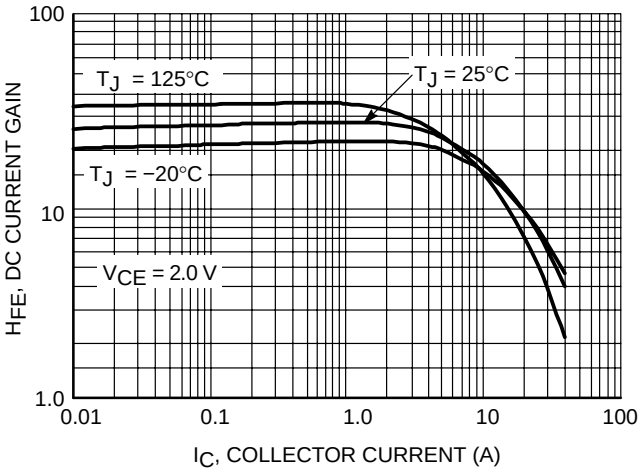


Figure 11. DC Current Gain, V_{CE} = 2.0 V

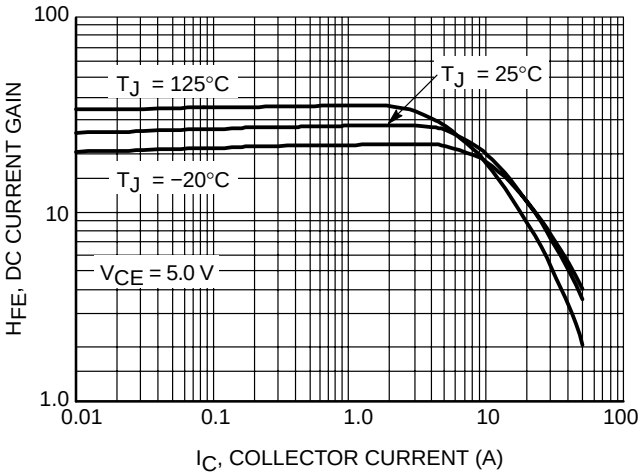


Figure 12. DC Current Gain, V_{CE} = 5.0 V

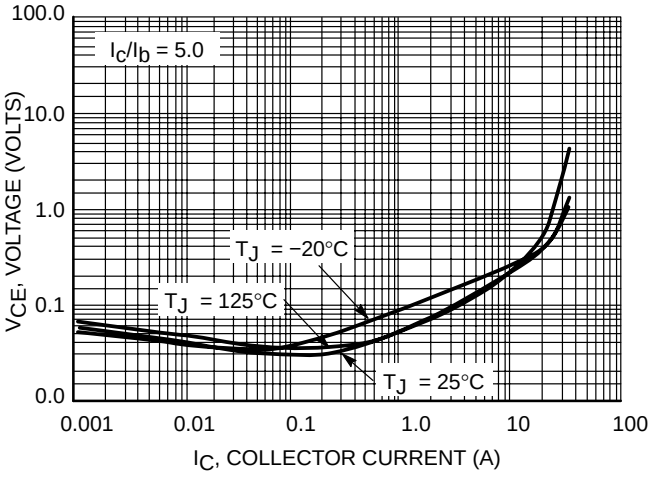


Figure 13. Typical Collector−Emitter Saturation Voltage, I_C/I_B = 5.0

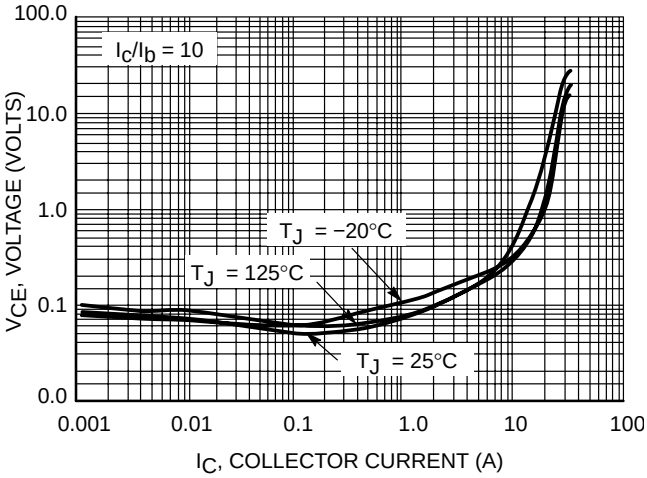


Figure 14. Typical Collector−Emitter Saturation Voltage, I_C/I_B = 10

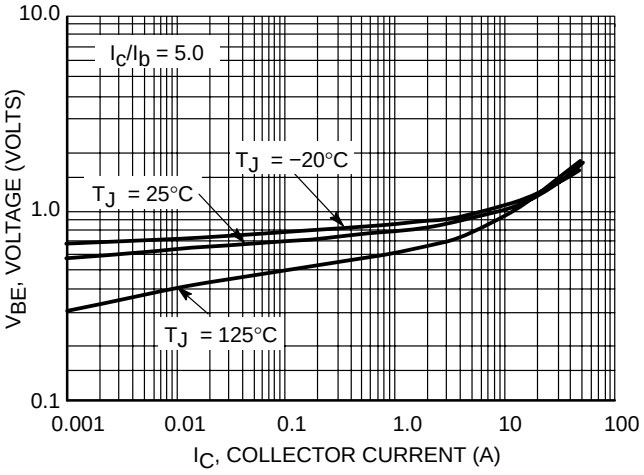


Figure 15. Typical Base−Emitter Saturation Voltage, I_C/I_B = 5.0

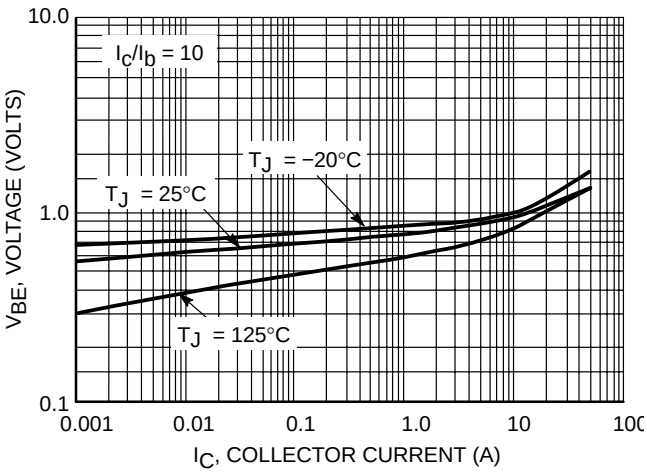


Figure 16. Typical Base−Emitter Saturation Voltage, I_C/I_B = 10

TYPICAL CHARACTERISTICS

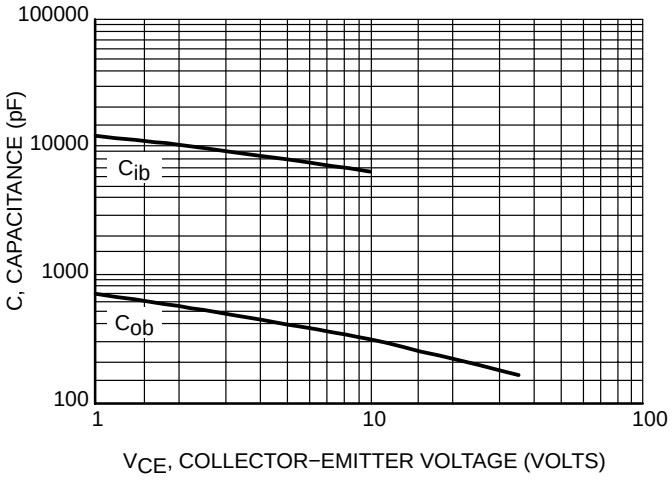


Figure 17. Typical Capacitance

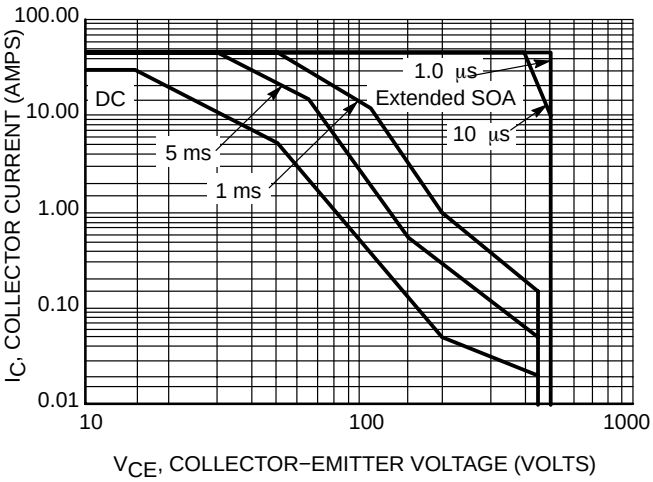


Figure 18. Forward Bias Safe Operating Area

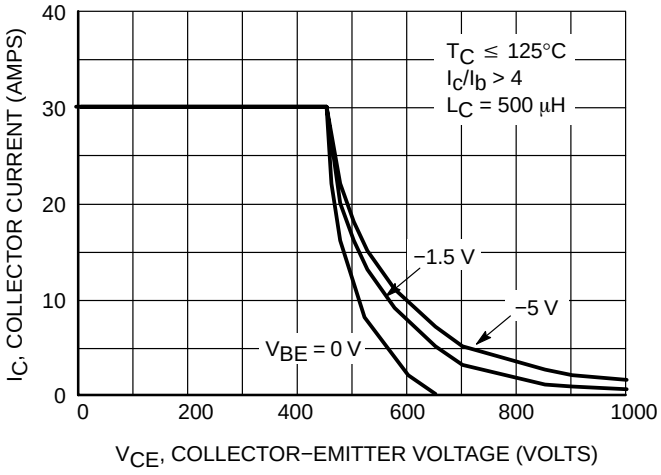


Figure 19. Reverse Bias Safe Operating Area

Complementary Silicon Plastic Power Transistors

Specifically designed for power audio output, or high power drivers in audio amplifiers.

- DC Current Gain Specified up to 8.0 Amperes at Temperature
- All On Characteristics at Temperature
- High SOA: 20 A, 18 V, 100 ms
- TO−247AE Package

NPN
MJW21192
PNP
MJW21191

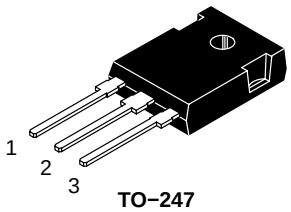
8.0 AMPERES
POWER TRANSISTORS
COMPLEMENTARY SILICON
150 VOLTS
125 WATTS

MAXIMUM RATINGS

Rating	Symbol	MJW21191 MJW21192	Unit
Collector−Emitter Voltage	V_{CEO}	150	Vdc
Collector−Base Voltage	V_{CB}	150	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	8.0 16	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.65	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

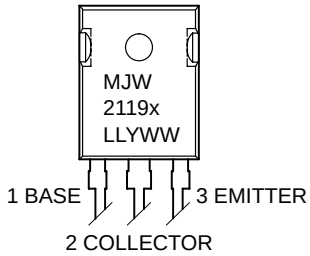
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	°C/W



TO−247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW2119x = Device Code
x = 1 or 2
LL = Location Code
Y = Year
WW = Work Week

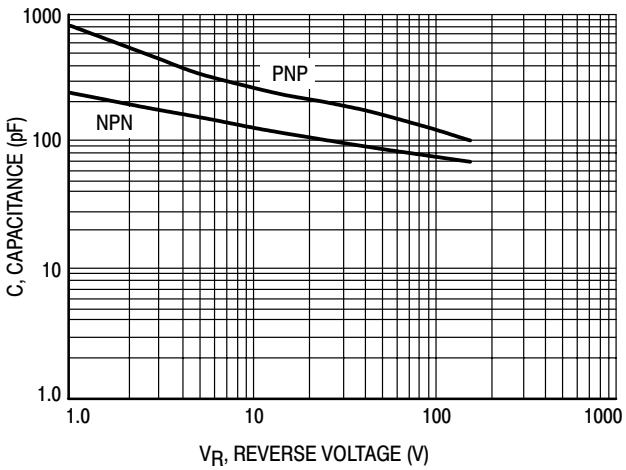


Figure 1. Typical Capacitance @ 25°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current (V_{CB} = 250 Vdc, I_E = 0)	I_{CES}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	15 5.0	— —	— 100
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 8.0 Adc, I_B = 1.6 Adc)	$V_{CE(sat)}$	— —	1.0 2.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

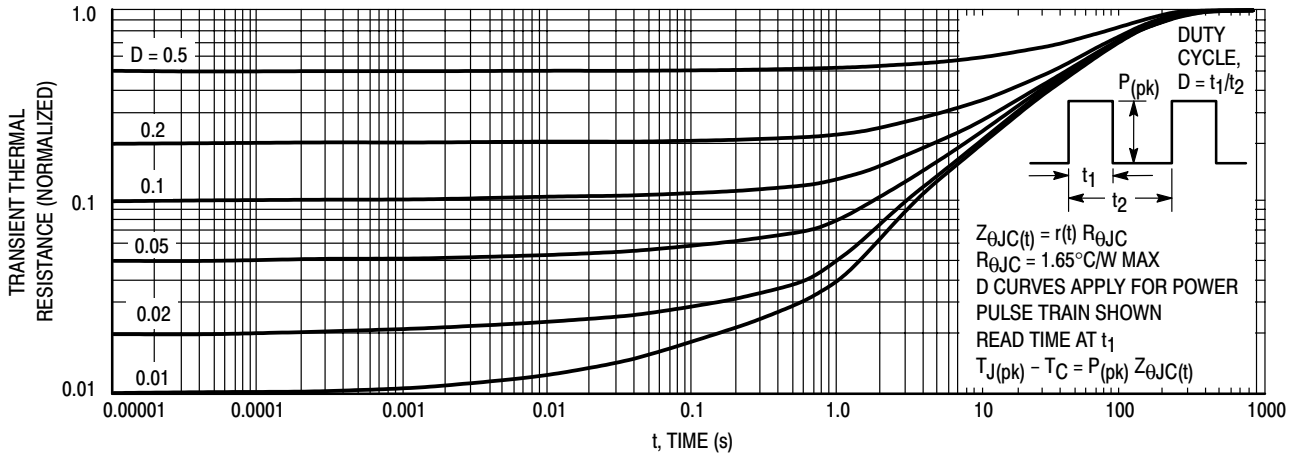


Figure 2. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN — MJW21192

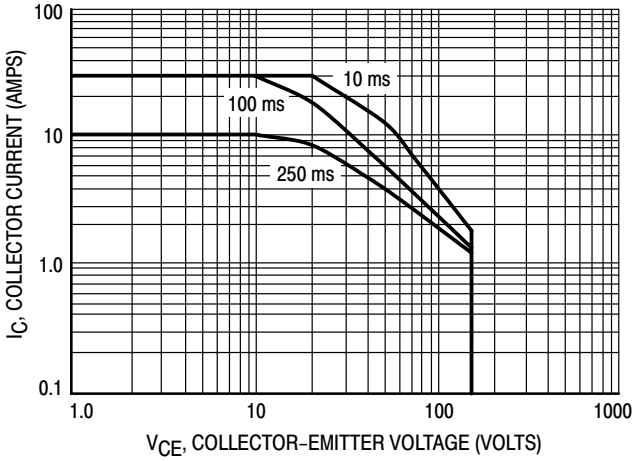


Figure 3. NPN — MJW21192 Safe Operating Area

PNP — MJW21191

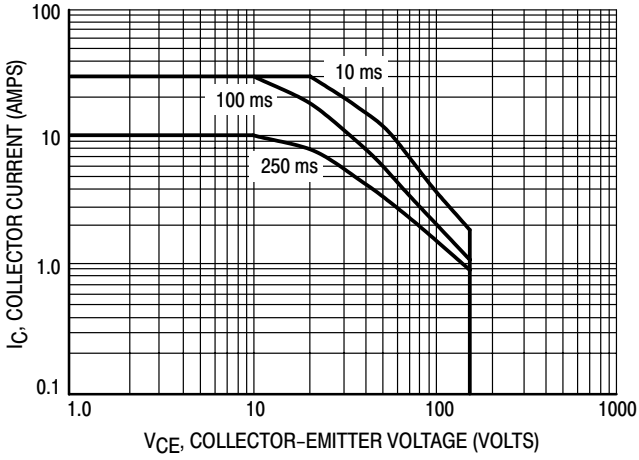


Figure 4. PNP — MJW21191 Safe Operating Area

TYPICAL CHARACTERISTICS

NPN — MJW21192

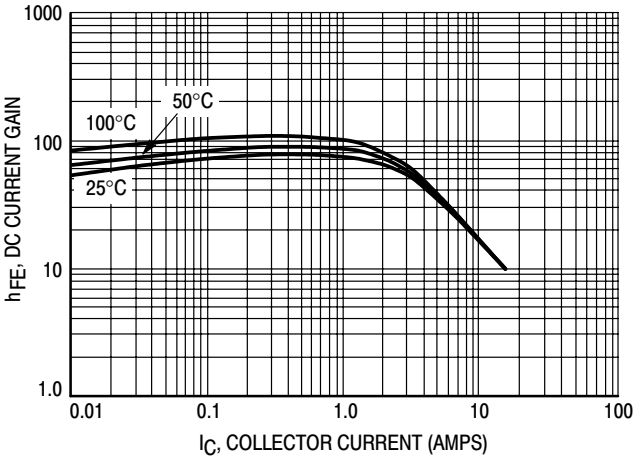


Figure 5. NPN — MJW21192 V_{CE} = 2.0 V DC Current Gain

PNP — MJW21191

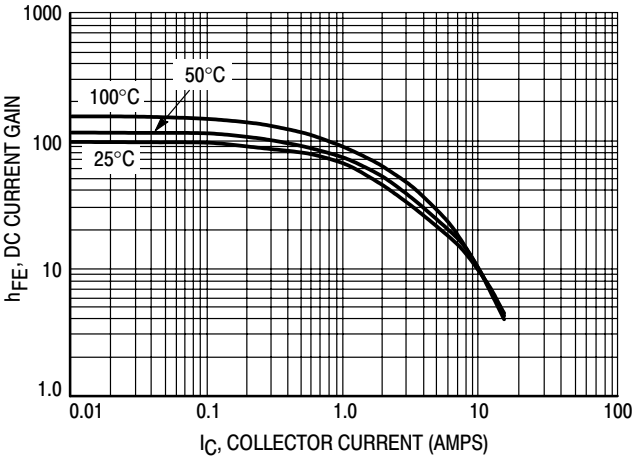


Figure 6. PNP — MJW21191 V_{CE} = 2.0 V DC Current Gain

NPN — MJW21192

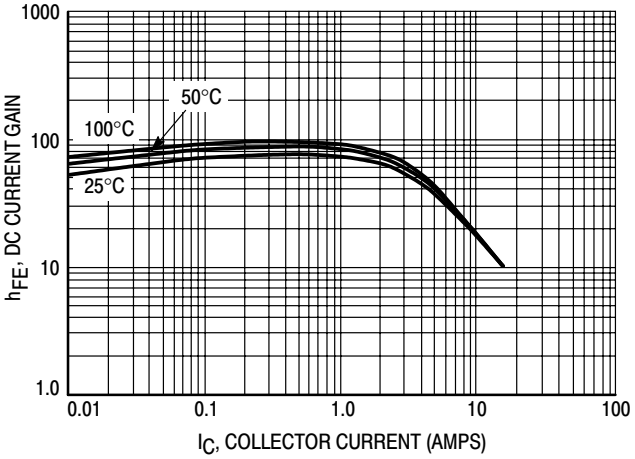


Figure 7. NPN — MJW21192
V_{CE} = 5.0 V DC Current Gain

PNP — MJW21191

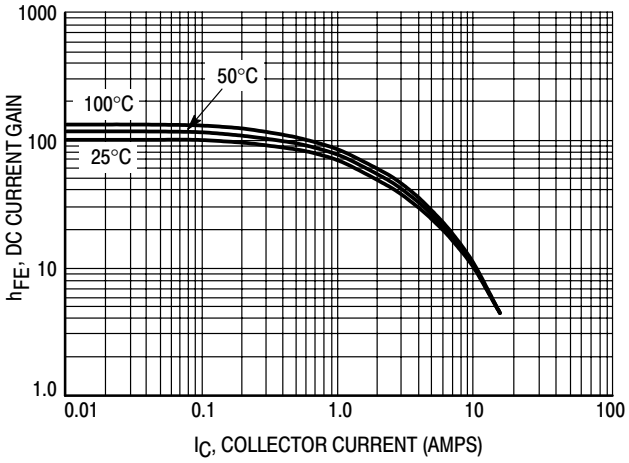


Figure 8. PNP — MJW21191
V_{CE} = 5.0 V DC Current Gain

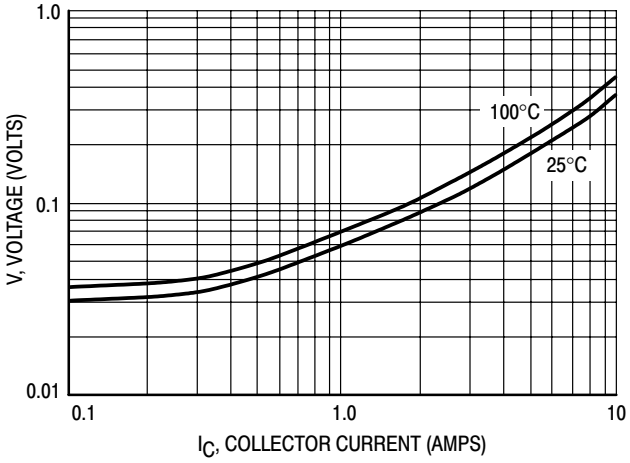


Figure 9. NPN — MJW21192
$V_{CE(sat)}$ I_C/I_B = 5.0

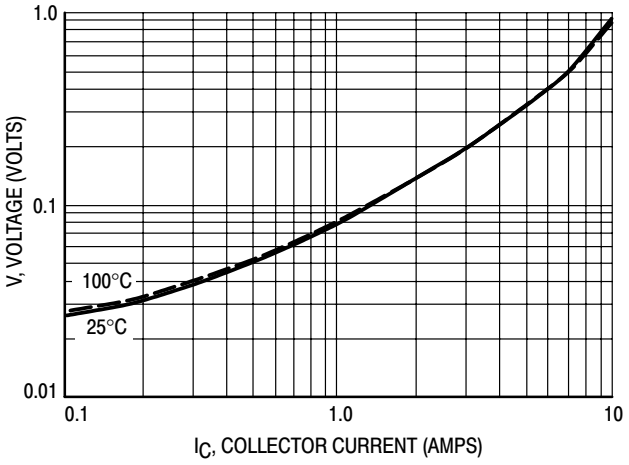


Figure 10. PNP — MJW21191
$V_{CE(sat)}$ I_C/I_B = 5.0

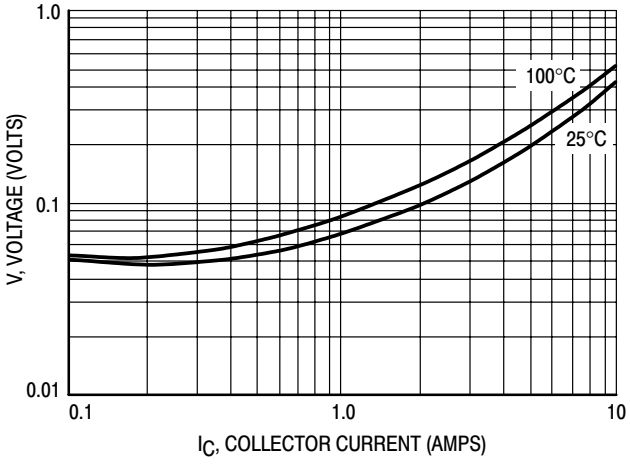


Figure 11. NPN — MJW21192
$V_{CE(sat)}$ I_C/I_B = 10

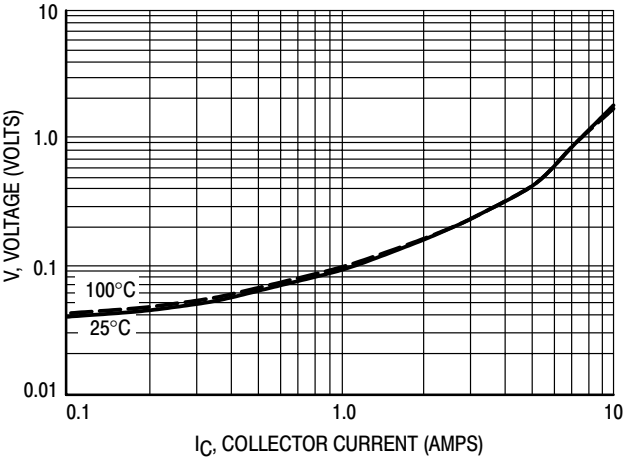


Figure 12. PNP — MJW21191
$V_{CE(sat)}$ I_C/I_B = 10

NPN — MJW21192

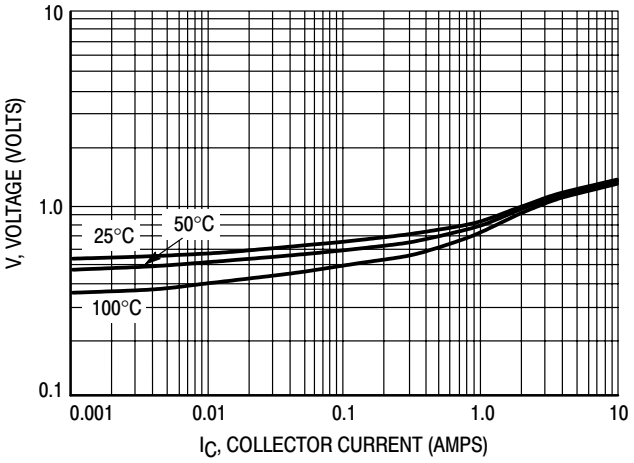


Figure 13. NPN — MJW21192
V_{CE} = 2.0 V $V_{BE(on)}$ Curve

PNP — MJW21191

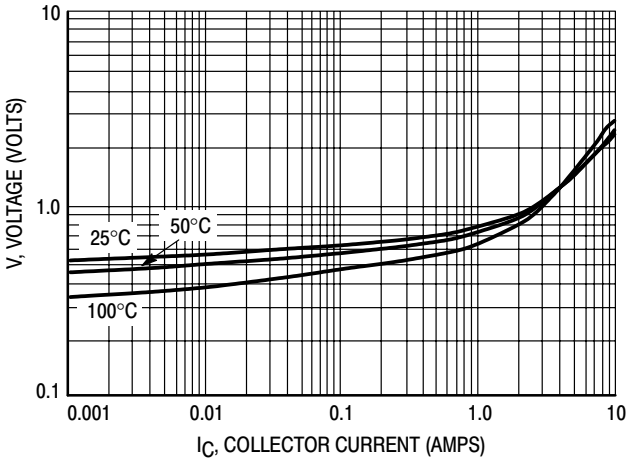


Figure 14. PNP — MJW21191
V_{CE} = 2.0 V $V_{BE(on)}$ Curve

MJW21193 (PNP)
MJW21194 (NPN)

Preferred Devices

Silicon Power Transistors

The MJW21193 and MJW21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain −
  h_{FE} = 20 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	16 30	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

ON Semiconductor™

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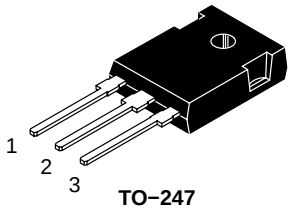
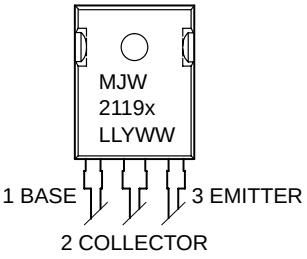
16 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



TO−247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW2119x = Device Code
x = 3 or 4
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW21193	TO−247	30 Units/Rail
MJW21194	TO−247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)		I_{CEO}	−	−	100	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)		I_{EBO}	−	−	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEX}	−	−	100	μAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non−repetitive)			4.0	−	−	
(V_{CE} = 80 Vdc, t = 1 s (non−repetitive)			2.25	−	−	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				
(I_C = 8 Adc, V_{CE} = 5 Vdc)			20	−	60	
(I_C = 16 Adc, I_B = 5 Adc)			8	−	−	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)		$V_{BE(on)}$	−	−	2.2	Vdc
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			−	−	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)			−	−	4	
DYNAMIC CHARACTERISTICS						
Total Harmonic Distortion at the Output		T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS}	h_{FE} unmatched		−	0.8	−	
(Matched pair h_{FE} = 50 @ 5 A/5 V)	h_{FE} matched		−	0.08	−	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	−	−	500	pF

PNP MJW21193

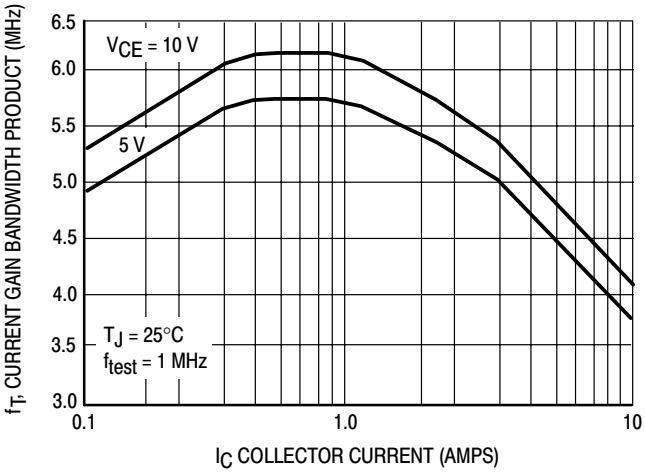


Figure 1. Typical Current Gain Bandwidth Product

NPN MJW21194

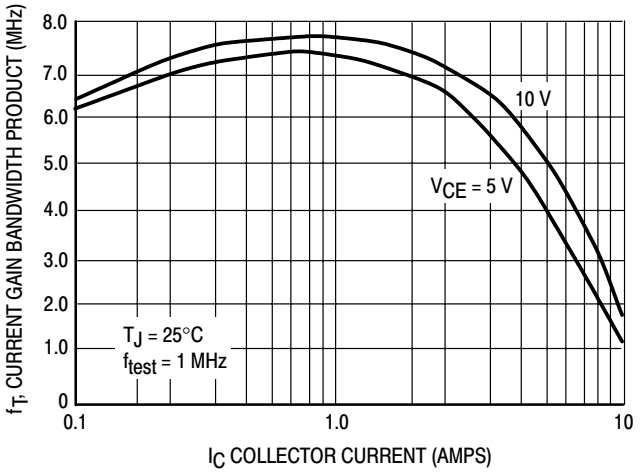


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW21193

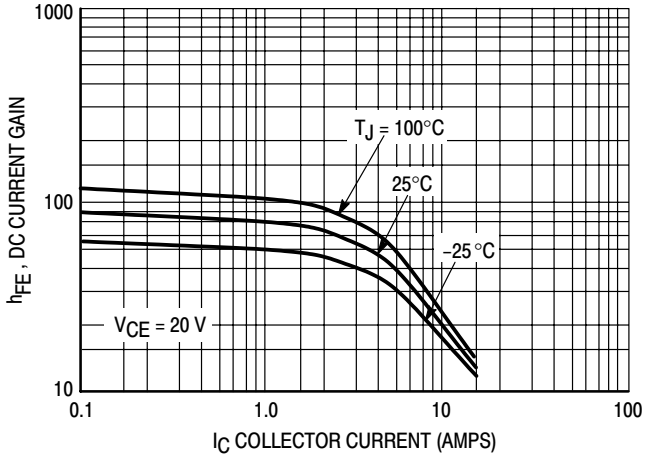


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJW21194

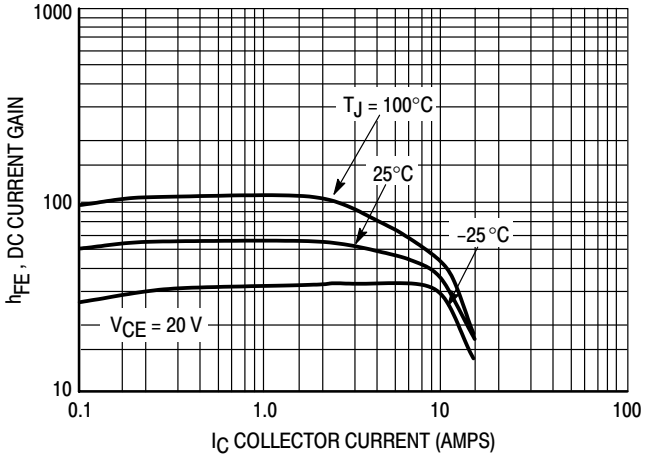


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJW21193

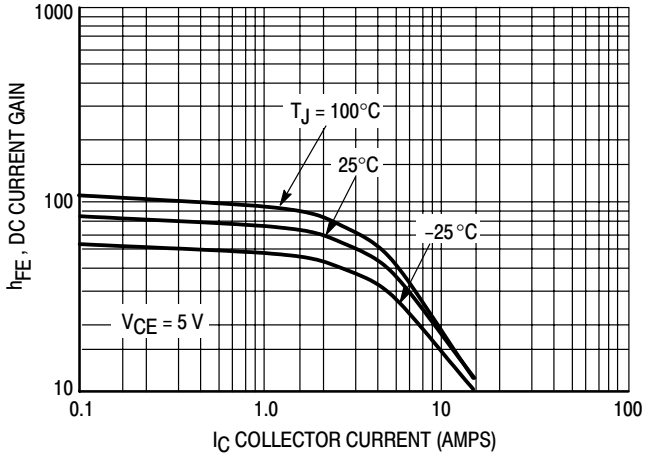


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJW21194

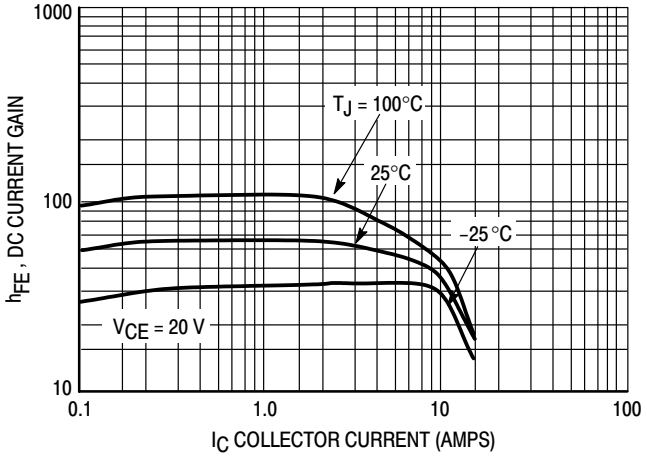


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJW21193

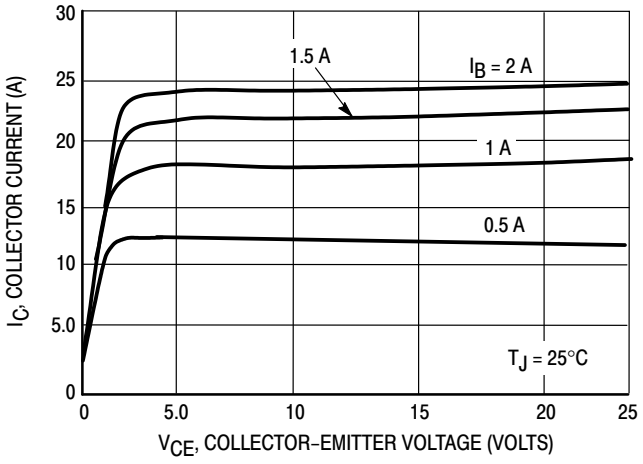


Figure 7. Typical Output Characteristics

NPN MJW21194

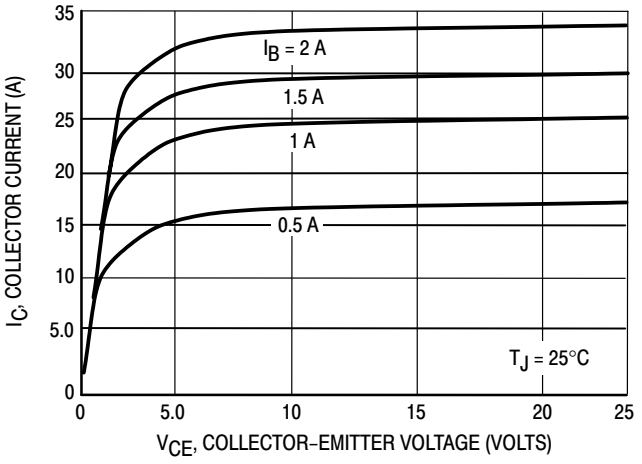


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW21193

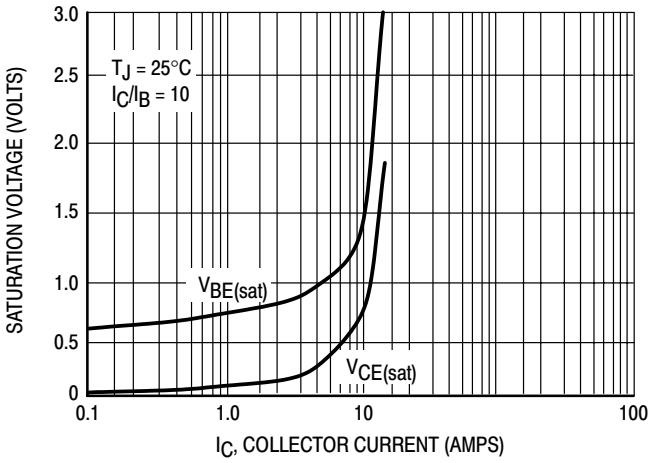


Figure 9. Typical Saturation Voltages

NPN MJW21194

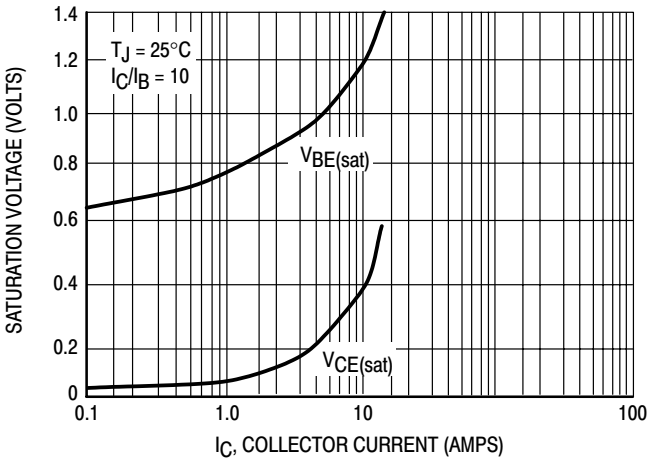


Figure 10. Typical Saturation Voltages

PNP MJW21193

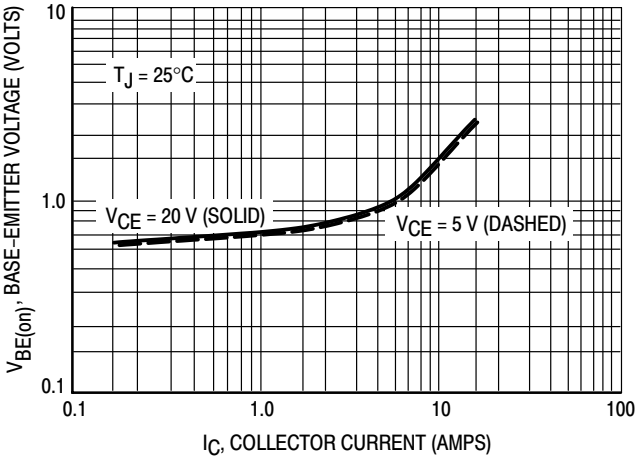


Figure 11. Typical Base−Emitter Voltage

NPN MJW21194

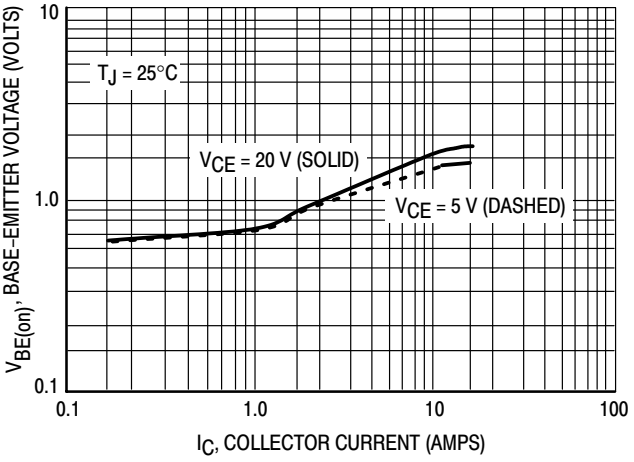


Figure 12. Typical Base−Emitter Voltage

PNP MJW21193

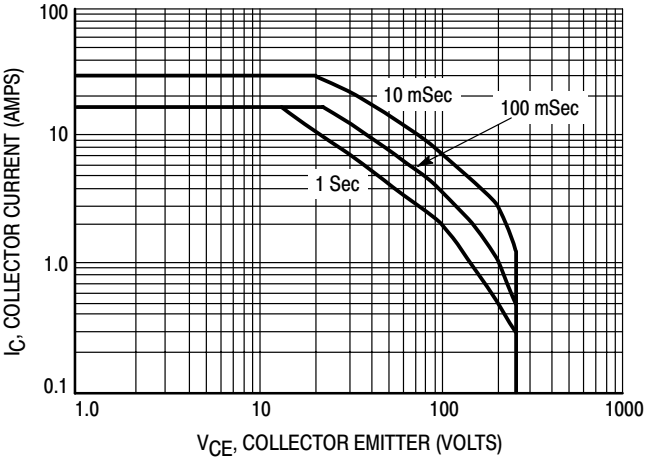


Figure 13. Active Region Safe Operating Area

NPN MJW21194

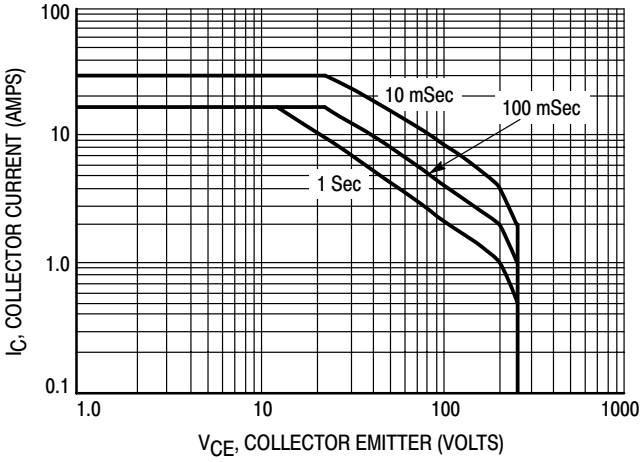


Figure 14. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

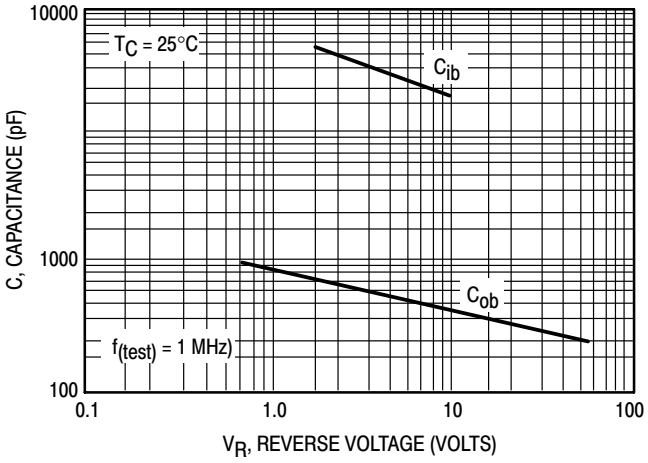


Figure 15. MJW21193 Typical Capacitance

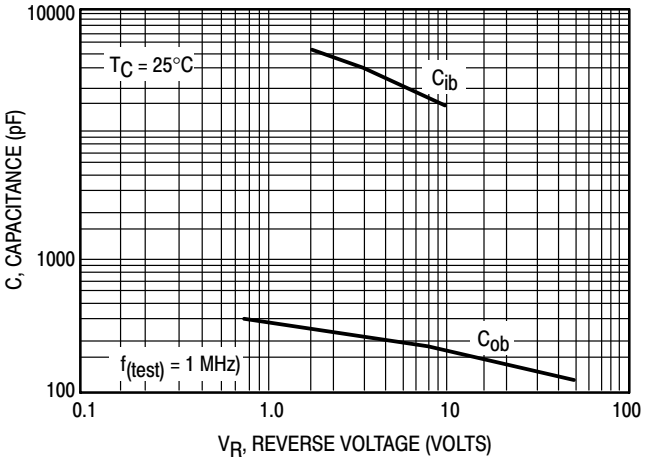


Figure 16. MJW21194 Typical Capacitance

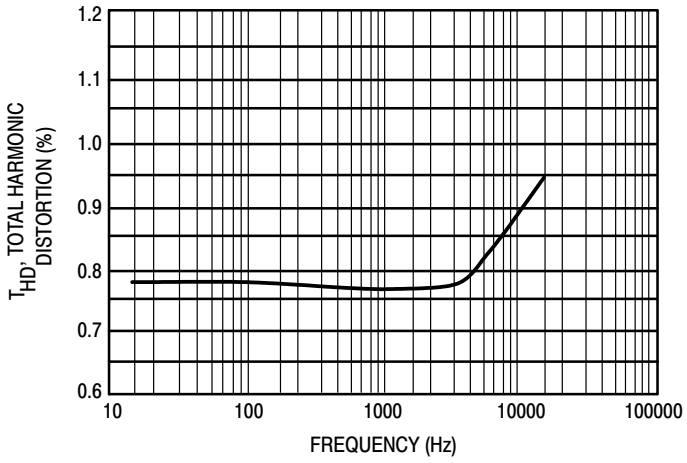


Figure 17. Typical Total Harmonic Distortion

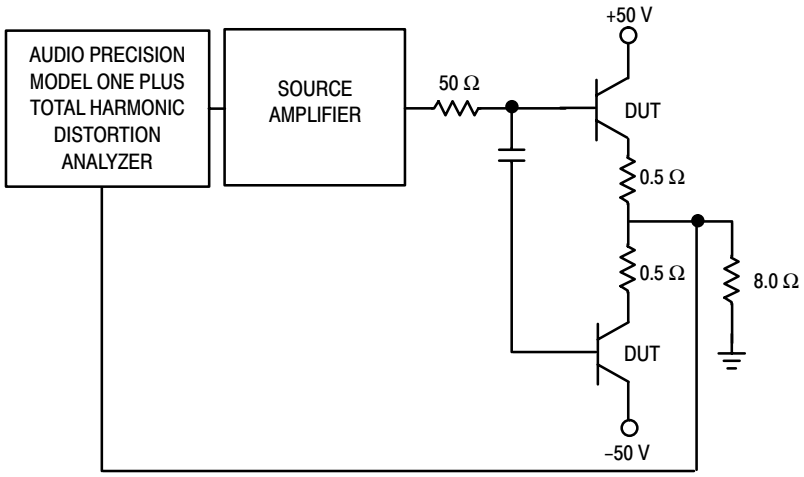


Figure 18. Total Harmonic Distortion Test Circuit

MJW21195 (PNP)
MJW21196 (NPN)

Preferred Devices

Silicon Power Transistors

The MJW21195 and MJW21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain − h_{FE} = 20 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	16 30	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

ON Semiconductor™

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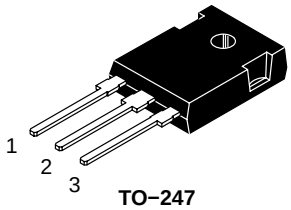
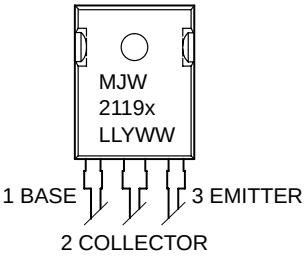
16 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



TO−247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJW2119x = Device Code
x = 5 or 6
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW21195	TO−247	30 Units/Rail
MJW21196	TO−247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	−	−	100	μAdc

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	−	−	50	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	−	−	50	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive)) (V_{CE} = 80 Vdc, t = 1 s (non−repetitive))	$I_{S/b}$	 4.0 2.25	 − −	 − −	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, I_B = 5 Adc)	h_{FE}	 20 8	 − −	 80 −	
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	−	−	2.0	Vdc
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 − −	 − −	 1.0 3	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 − −	 0.8 0.08	 − −	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	−	500	pF

PNP MJW21195

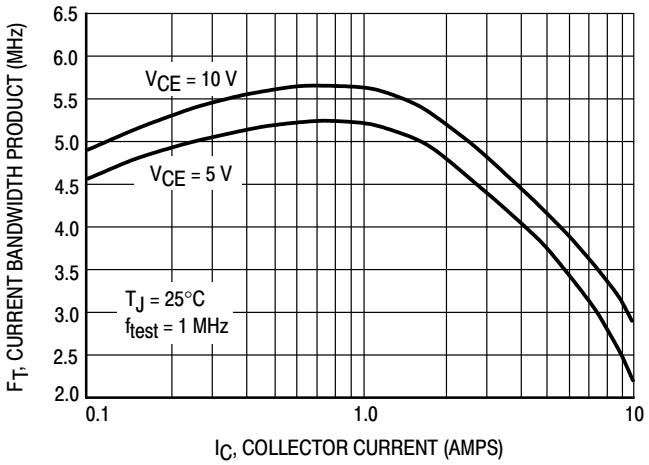


Figure 1. Typical Current Gain Bandwidth Product

NPN MJW21196

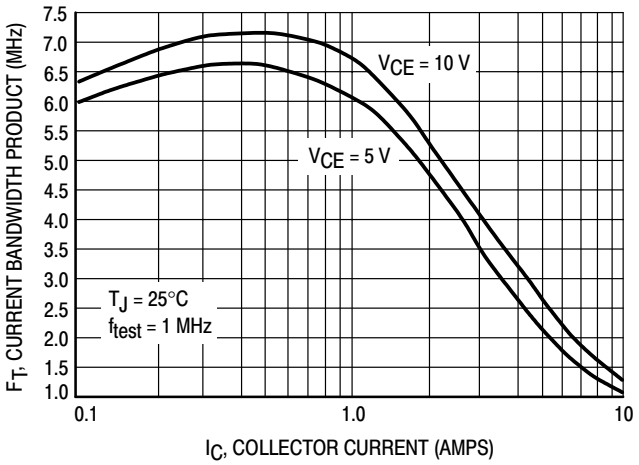


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW21195

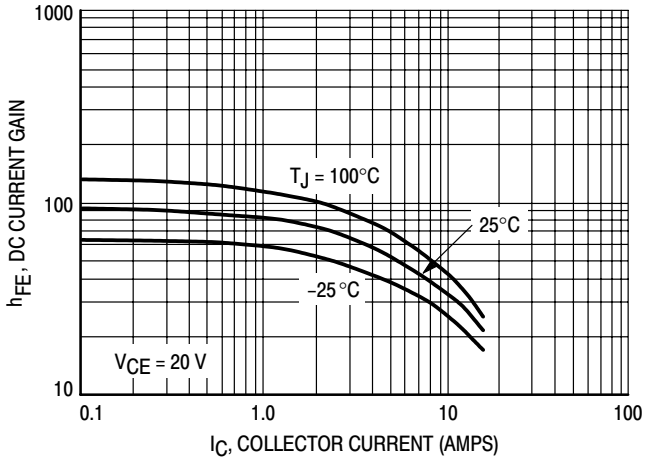


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJW21196

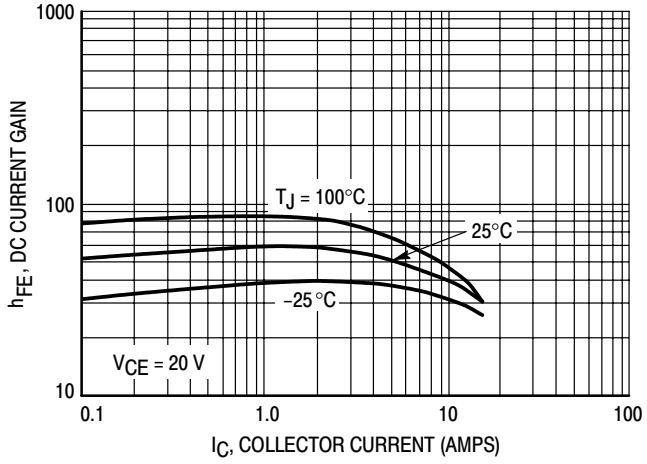


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJW21195

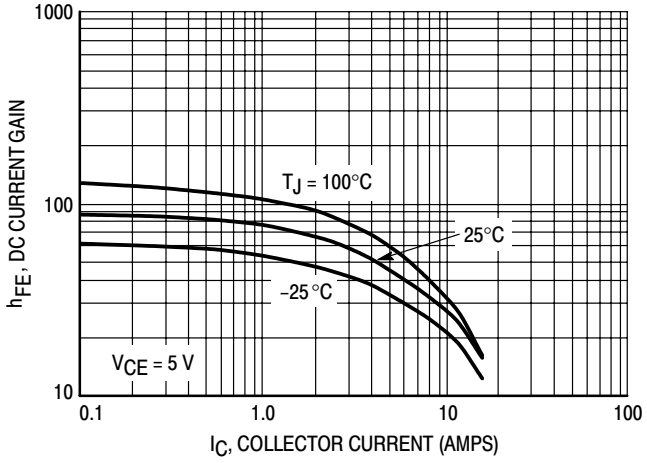


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJW21196

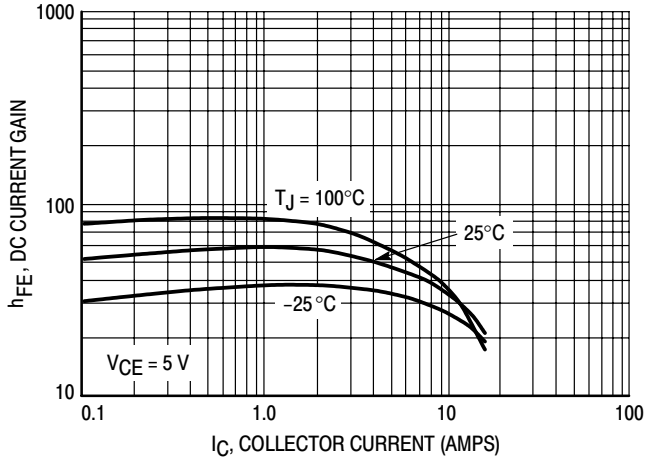


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJW21195

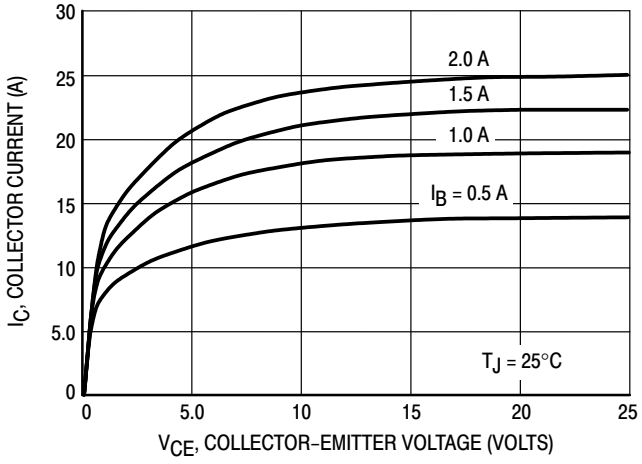


Figure 7. Typical Output Characteristics

NPN MJW21196

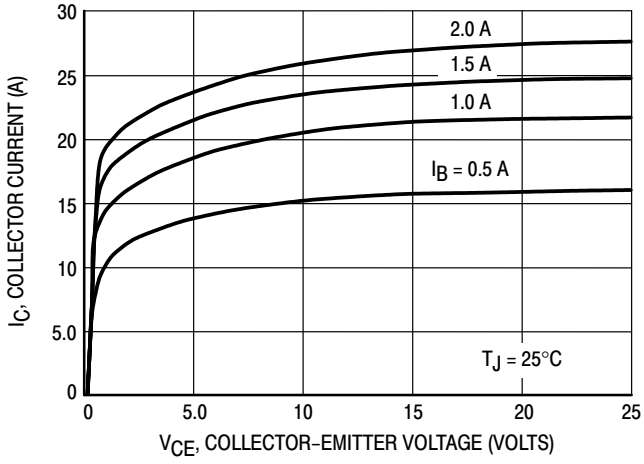


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW21195

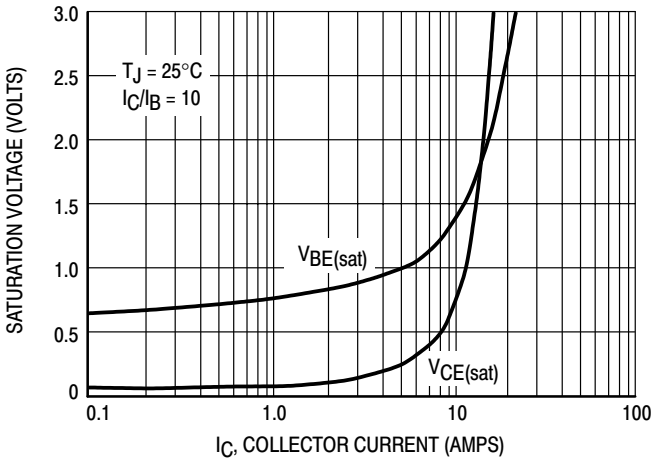


Figure 9. Typical Saturation Voltages

NPN MJW21196

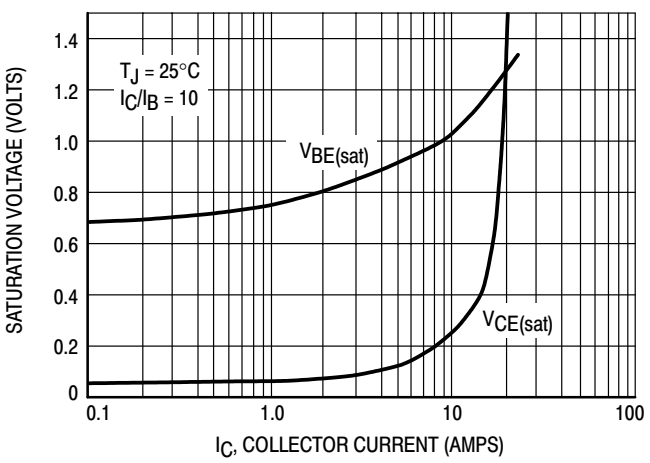


Figure 10. Typical Saturation Voltages

PNP MJW21195

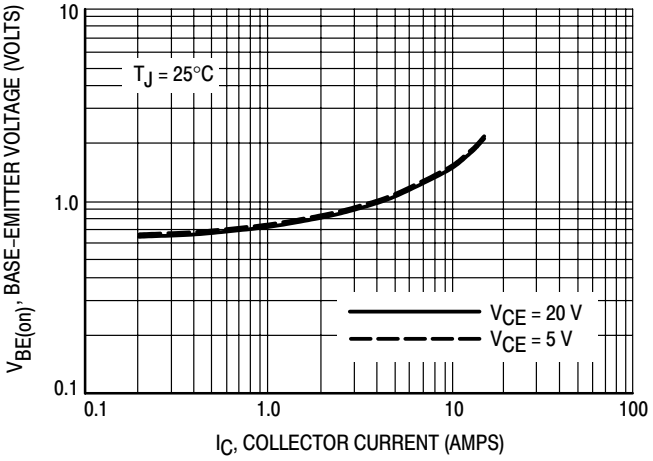


Figure 11. Typical Base−Emitter Voltage

NPN MJW21196

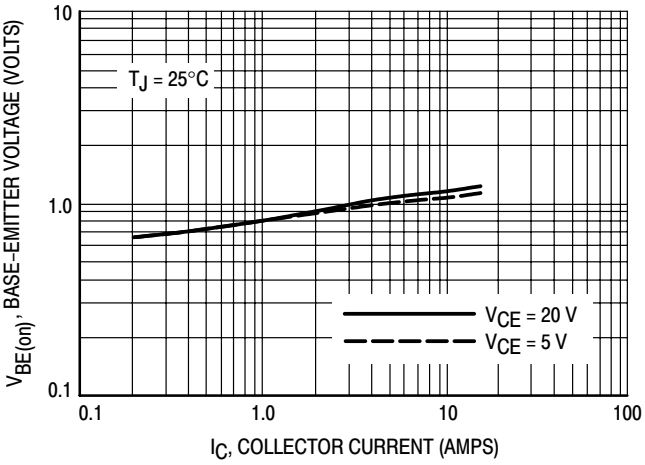


Figure 12. Typical Base−Emitter Voltage

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

PNP MJW21195

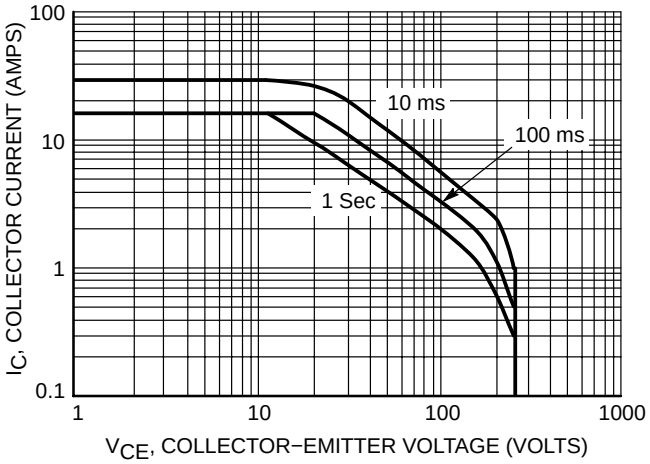


Figure 13. Active Region Safe Operating Area

NPN MJW21196

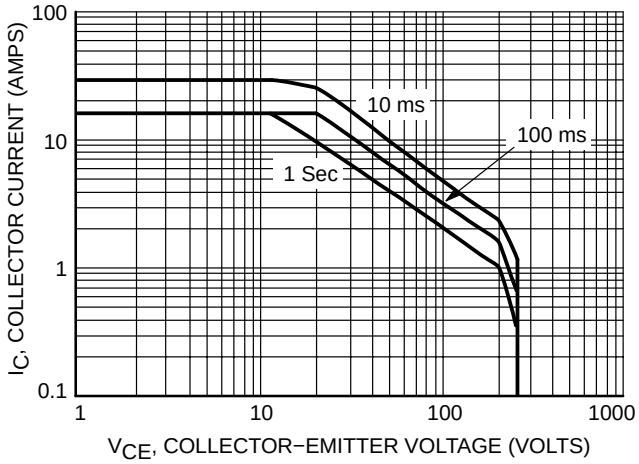


Figure 14. Active Region Safe Operating Area

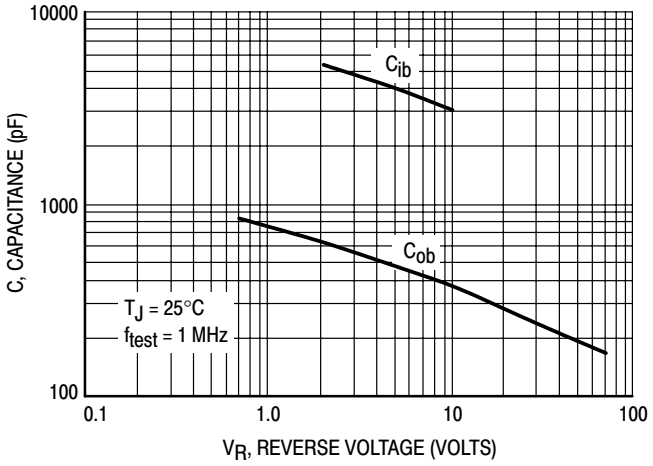


Figure 15. MJW21195 Typical Capacitance

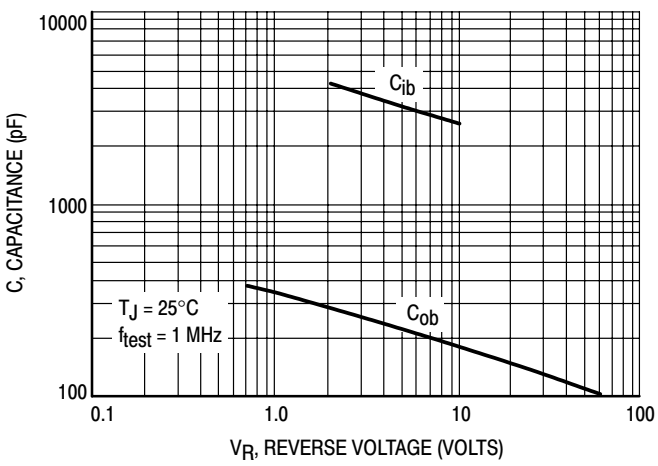


Figure 16. MJW21196 Typical Capacitance

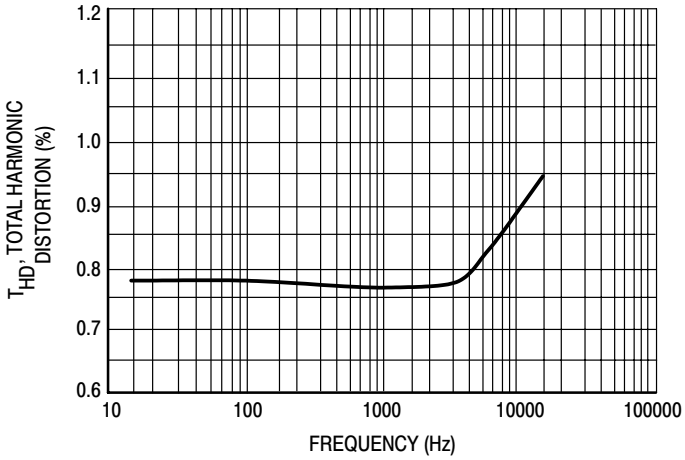


Figure 17. Typical Total Harmonic Distortion

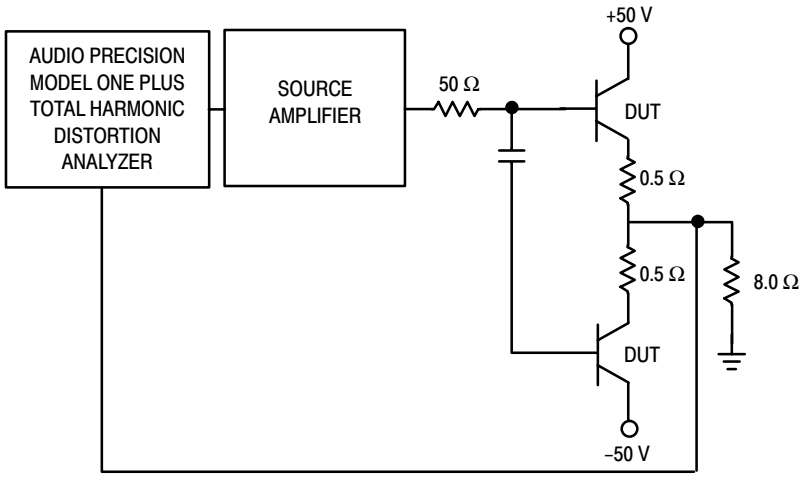


Figure 18. Total Harmonic Distortion Test Circuit

MJW3281A (NPN)
MJW1302A (PNP)

Preferred Devices

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJW3281A and MJW1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  Gain Linearity from 100 mA to 7 A
  h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area − 1 A/100 V @ 1 Second
- High f_T − 30 MHz Typical

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	230	Vdc
Collector−Base Voltage	V_{CBO}	230	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	230	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	15 25	Adc
Base Current − Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	°C/W

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

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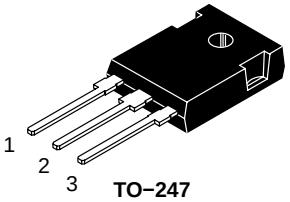
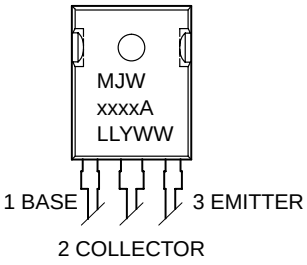
15 AMPERES
COMPLEMENTARY
SILICON POWER
TRANSISTORS
230 VOLTS
200 WATTS



TO−247
CASE 340K
STYLE 3

MARKING DIAGRAM



MJWxxxxA = Device Code
xxxx = 3281 OR 1302
LL = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJW3281A	TO−247	30 Units/Rail
MJW1302A	TO−247	30 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	230	–	–	Vdc
Collector Cutoff Current (V_{CB} = 230 Vdc, I_E = 0)	I_{CBO}	–	–	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	5	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive) (V_{CE} = 100 Vdc, t = 1 s (non−repetitive)	$I_{S/b}$	4 1	– –	– –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc) (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 7 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	 50 50 50 50 50 45 12	 125 – – – 115 – 35	 200 200 200 200 200 – –	–
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	–	0.4	2	Vdc
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	–	–	2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	–	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	–	600	pF

PNP MJW1302A

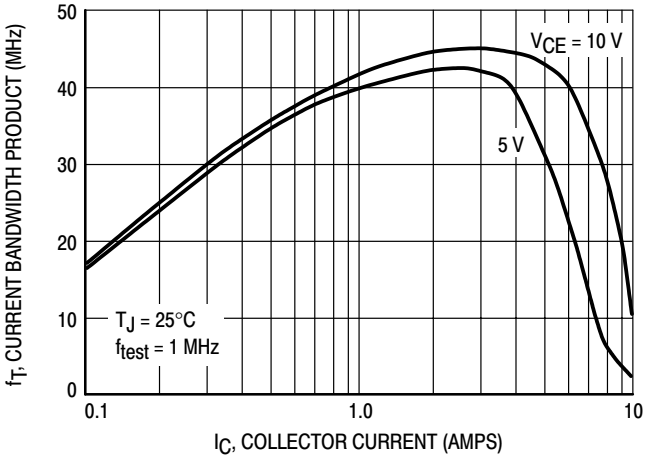


Figure 19. Typical Current Gain Bandwidth Product

NPN MJW3281A

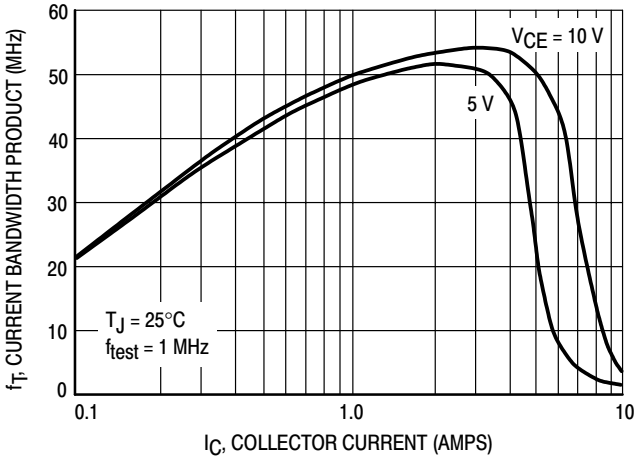


Figure 20. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJW1302A

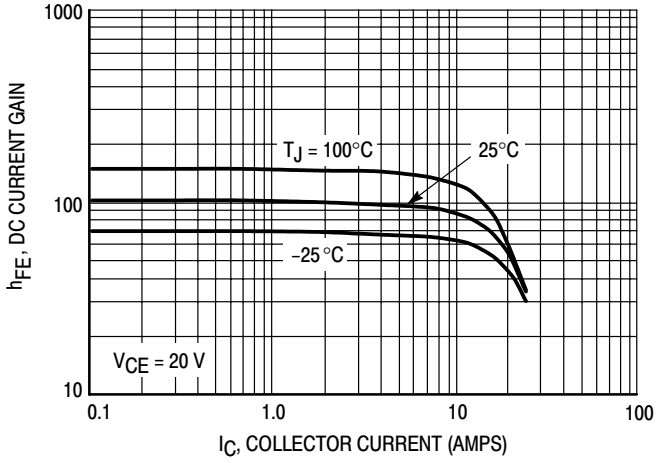


Figure 21. DC Current Gain, V_{CE} = 20 V

NPN MJW3281A

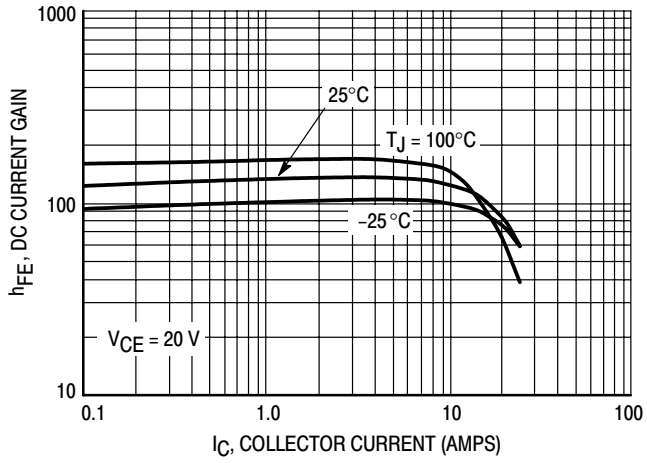


Figure 22. DC Current Gain, V_{CE} = 20 V

PNP MJW1302A

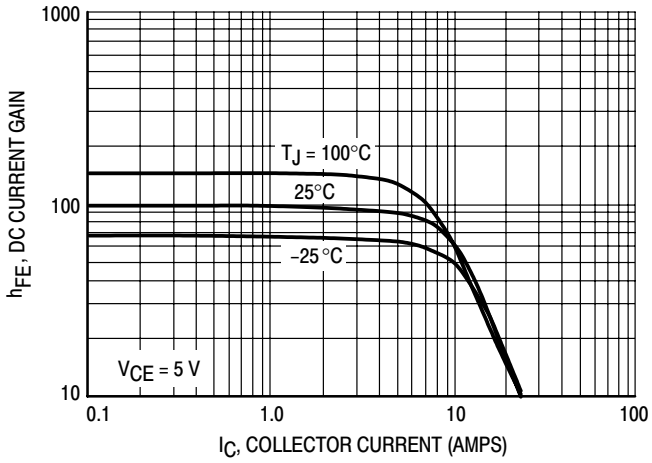


Figure 23. DC Current Gain, V_{CE} = 5 V

NPN MJW3281A

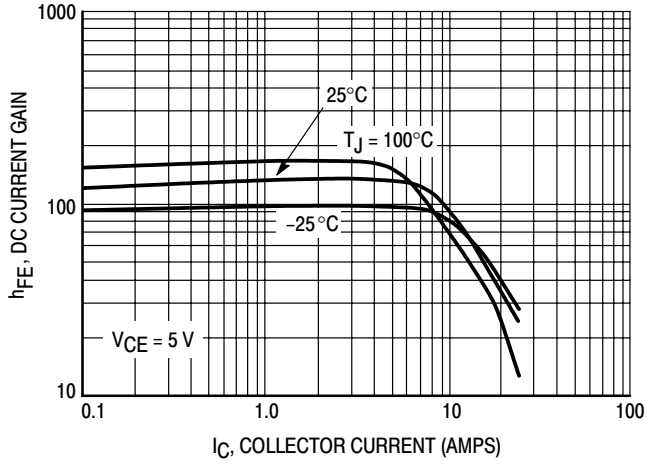


Figure 24. DC Current Gain, V_{CE} = 5 V

PNP MJW1302A

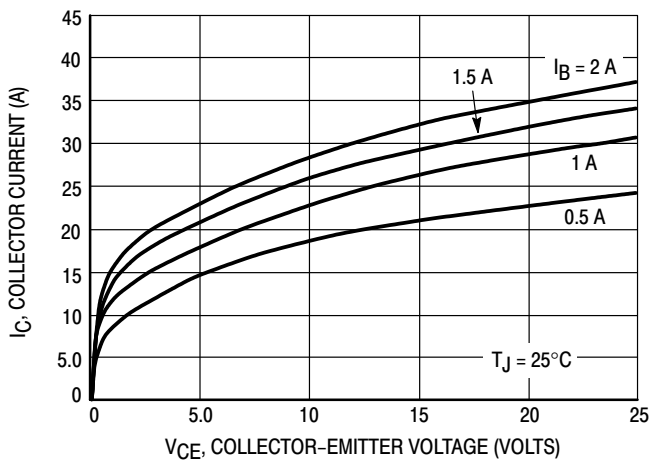


Figure 25. Typical Output Characteristics

NPN MJW3281A

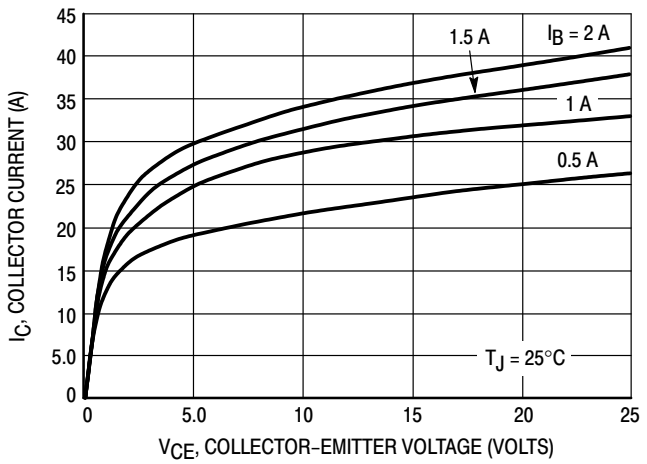


Figure 26. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJW1302A

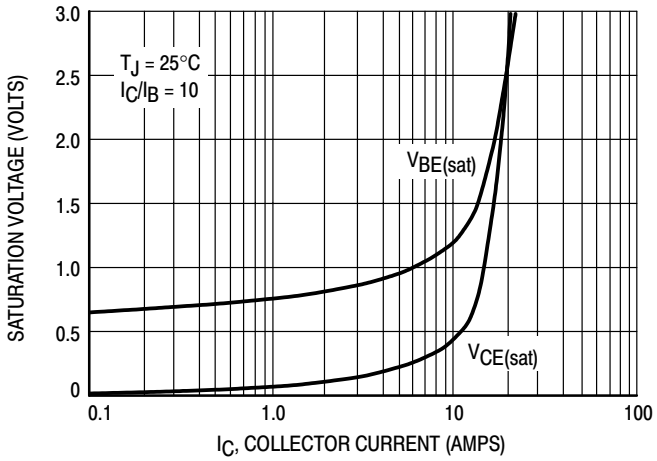


Figure 27. Typical Saturation Voltages

NPN MJW3281A

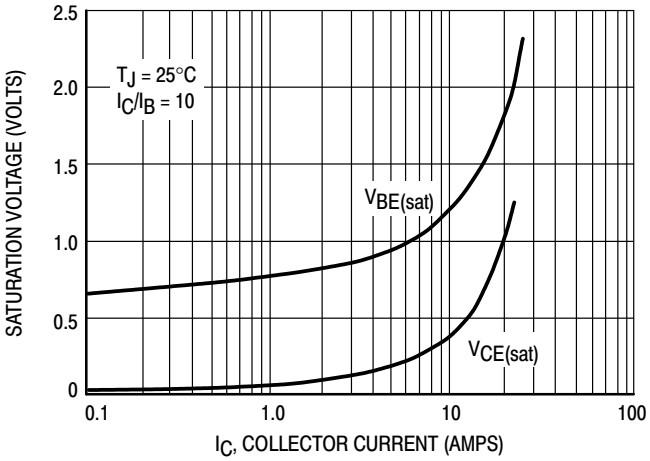


Figure 28. Typical Saturation Voltages

PNP MJW1302A

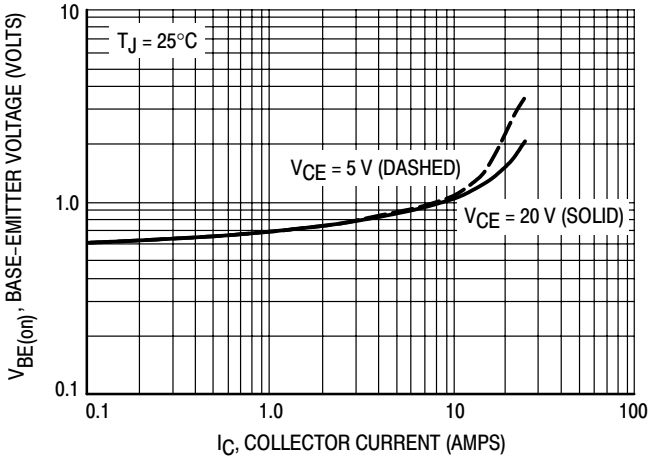


Figure 29. Typical Base−Emitter Voltage

NPN MJW3281A

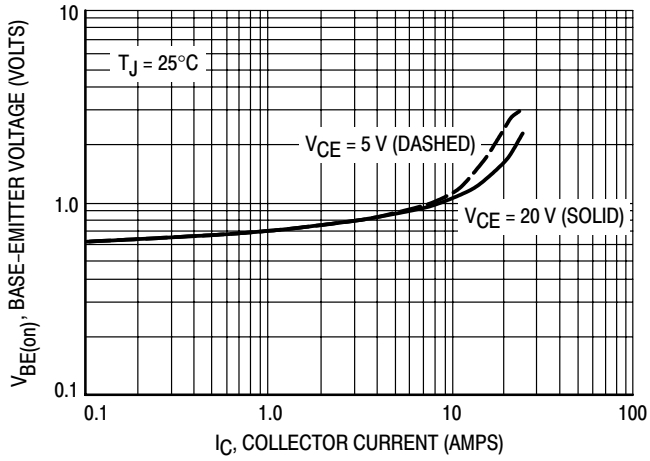


Figure 30. Typical Base−Emitter Voltage

PNP MJW1302A

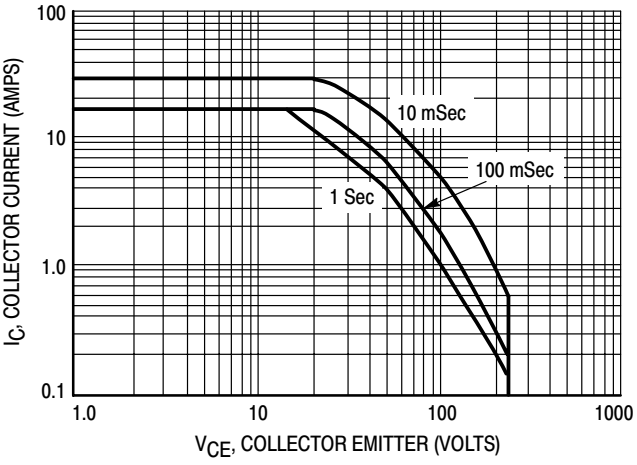


Figure 31. Active Region Safe Operating Area

NPN MJW3281A

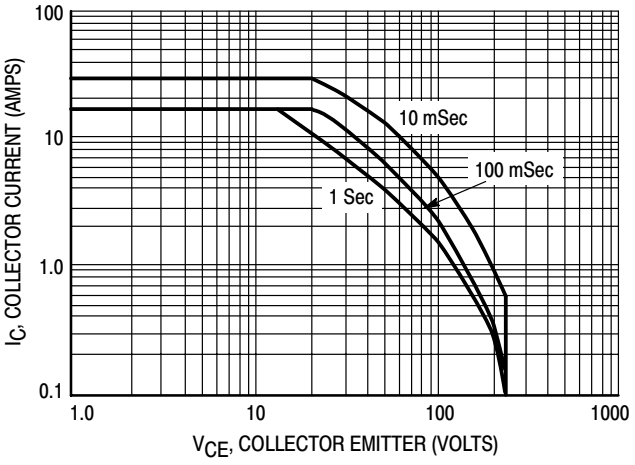


Figure 32. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 31 and 32 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

PNP MJW1302A

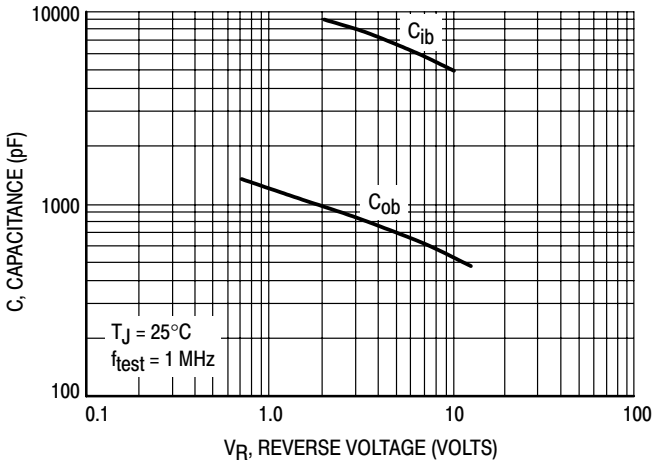


Figure 33. MJW1302A Typical Capacitance

NPN MJW3281A

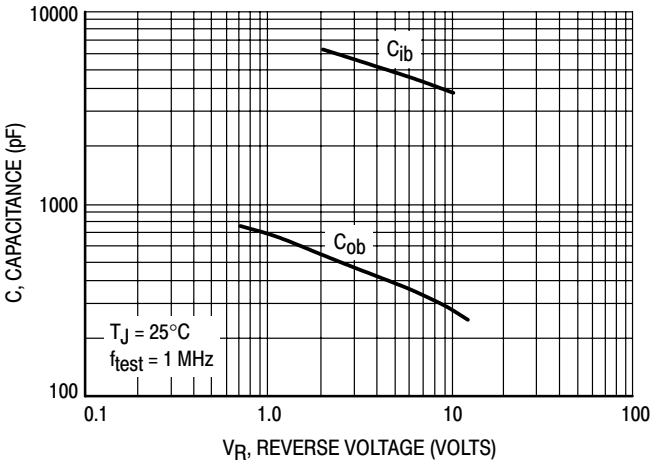


Figure 34. MJW3281A Typical Capacitance

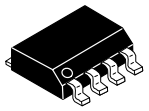
MMDJ3N03BJT

ON Semiconductor Preferred Device

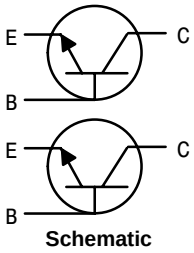
Plastic Power Transistors
SO−8 for Surface Mount Applications

DUAL BIPOLAR
POWER TRANSISTOR
NPN SILICON
30 VOLTS
3 AMPERES

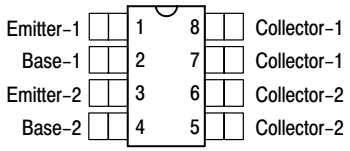
- Collector −Emitter Sustaining Voltage — $V_{CEO(sus)}$
  = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE}= 85 (Min) @ I_C = 0.8 Adc
  = 60 (Min) @ I_C = 3.0 Adc
- Low Collector −Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.18 Vdc (Max) @ I_C = 1.2 Adc
  = 0.45 Vdc (Max) @ I_C = 3.0 Adc
- Miniature SO−8 Surface Mount Package − Saves Board Space



CASE 751−07, Style 16
(SO−8)



Schematic



Top View
Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Base Voltage	V_{CB}	45	Vdc
Collector−Emitter Voltage	V_{CEO}	30	Vdc
Emitter−Base Voltage	V_{EB}	±6.0	Vdc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Base Current — Continuous	I_B	1.0	Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction to Ambient on 1″ sq. (645 sq. mm) Collector pad on FR−4 board material with one die operating. Thermal Resistance − Junction to Ambient on 0.012″ sq. (7.6 sq. mm) Collector pad on FR−4 board material with one die operating.	$R_{\theta JA}$	 100 185	°C/W
Total Power Dissipation @ T_A = 25°C mounted on 1″ sq. (645 sq. mm) Collector pad on FR−4 board material with one die operating. Derate above 25°C	P_D	 1.25 10	 Watts mW/°C
Maximum Temperature for Soldering	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter−Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω) (V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)	I_{CER}	— —	— —	20 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS(1)					
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc) (I_C = 1.2 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	— — —	0.105 — —	0.15 0.18 0.45	Vdc
Base−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base−Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.2 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	85 80 60	195 — —	— — —	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	85	135	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	200	—	pF
Current−Gain — Bandwidth Product(2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, F_{test} = 1.0 MHz)	f_T	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{FE}| \cdot f_{test}$

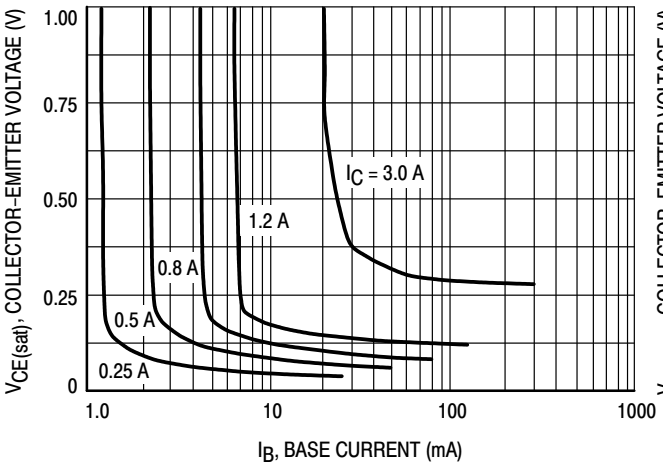


Figure 1. Collector Saturation Region

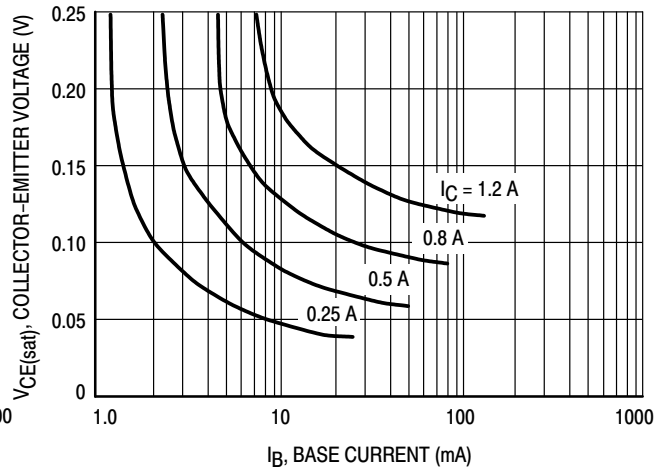


Figure 2. Collector Saturation Region

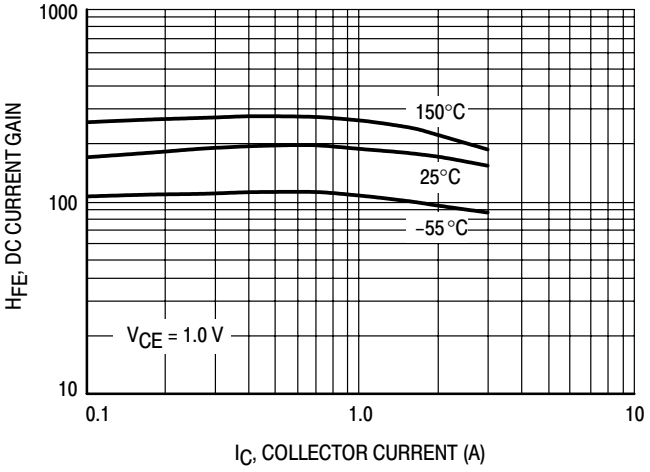


Figure 3. DC Current Gain

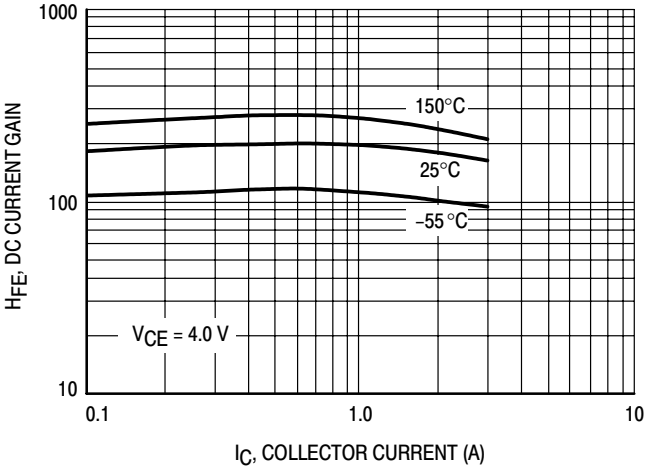


Figure 4. DC Current Gain

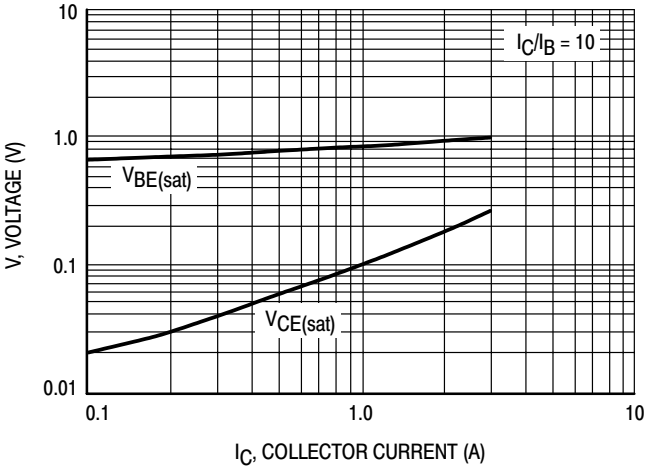


Figure 5. “On” Voltages

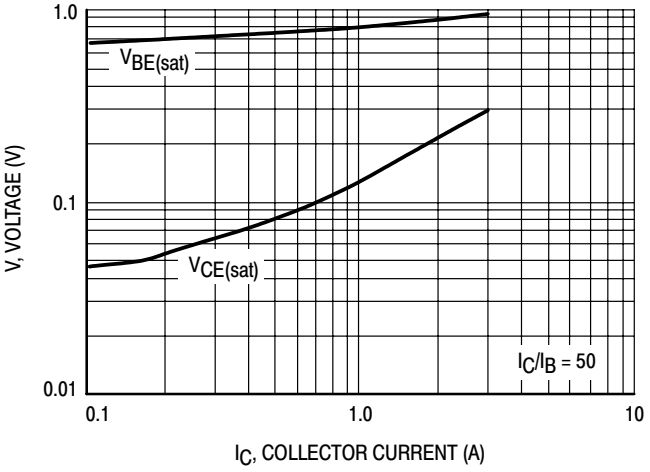


Figure 6. “On” Voltages

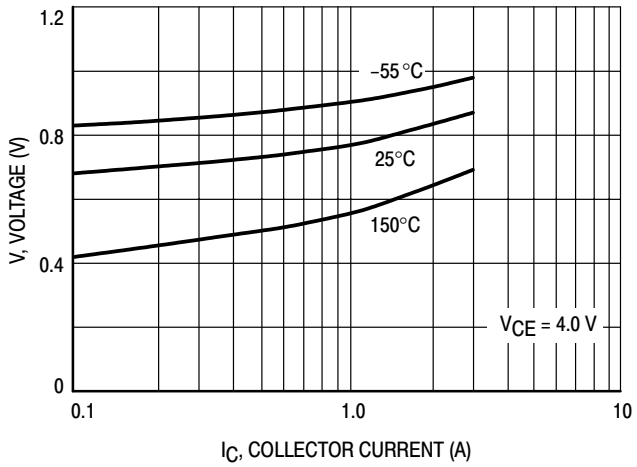


Figure 7. $V_{BE(on)}$ Voltage

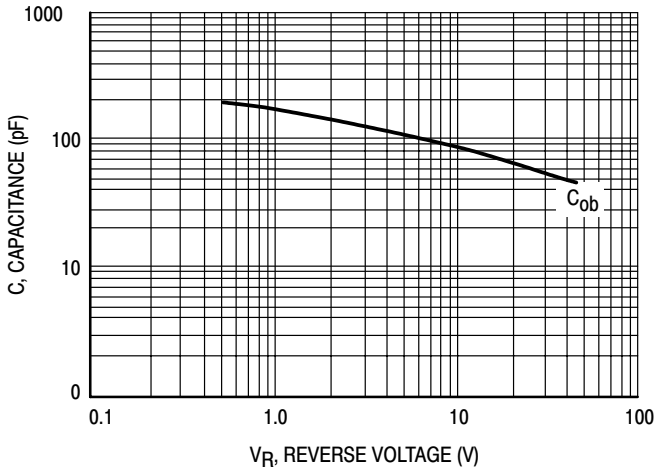


Figure 8. Capacitance

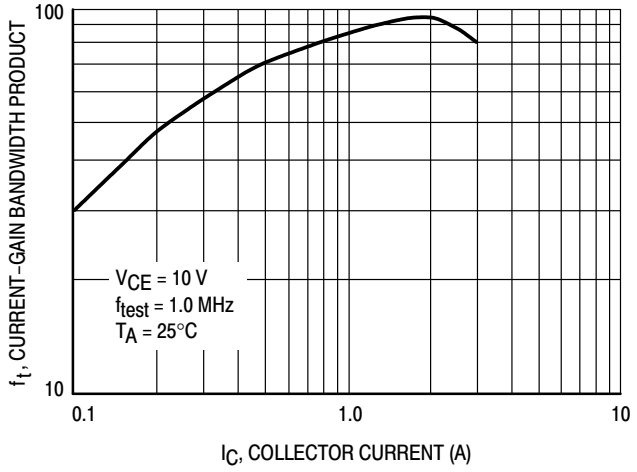


Figure 9. Current−Gain Bandwidth Product

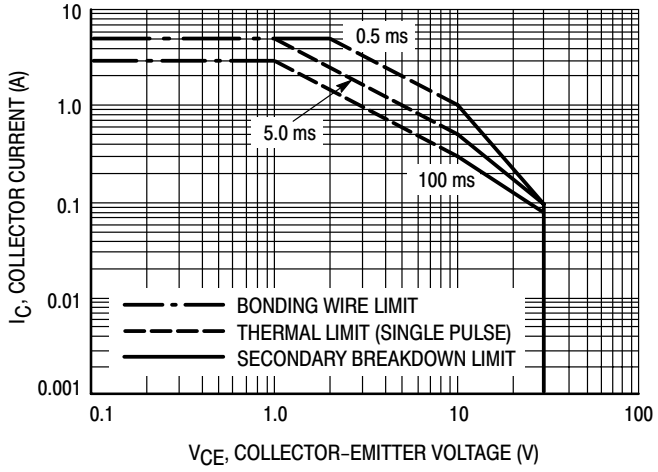


Figure 10. Active Region Safe Operating Area

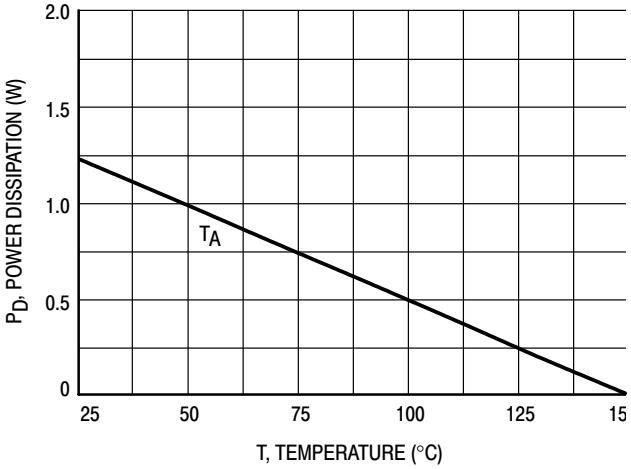


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

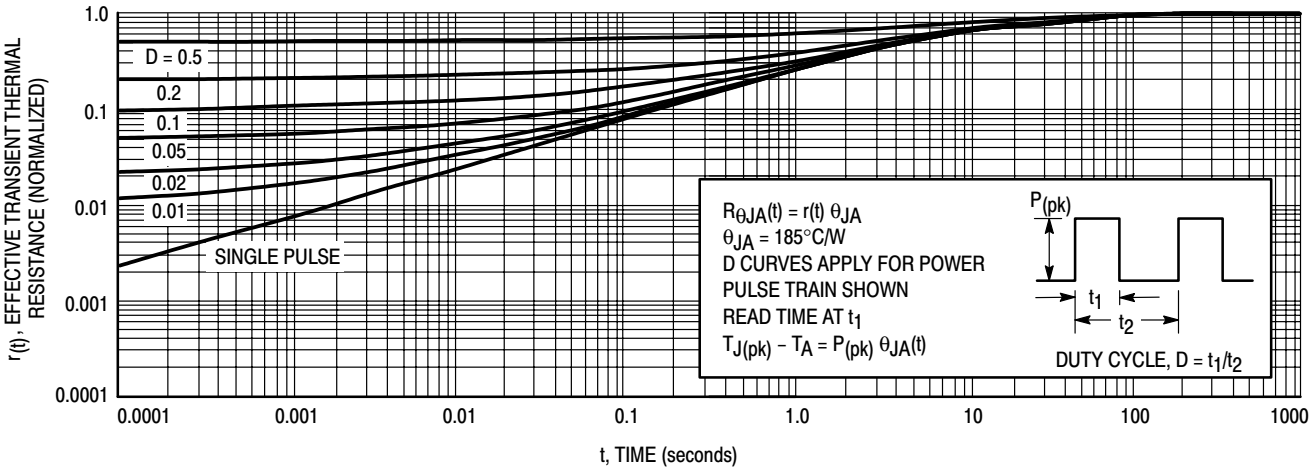


Figure 12. Thermal Response

MMJT350T1

Bipolar Power Transistors

PNP Silicon

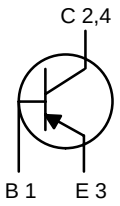
. . . designed for use in line−operated applications such as low power, line−operated series pass and switching regulators requiring PNP capability.

- High Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain −
  h_{FE} = 30−240 @ I_C = 50 mAdc
- Epoxy Meets UL94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; > 8000 V
  Machine Model, C; > 400 V

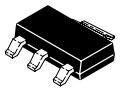
ON Semiconductor®

http://onsemi.com

0.5 AMPERE
POWER TRANSISTOR
PNP SILICON
300 VOLTS
2.75 WATTS

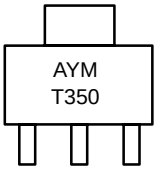


Schematic

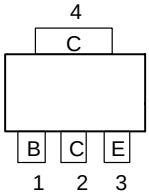


SOT−223
CASE 318E
Style 1

MARKING DIAGRAM



T350	= Specific Device Code
A	= Assembly Location
Y	= Last Digit of Year
M	= Month Code



Top View Pinout

ORDERING INFORMATION

Device	Package	Shipping
MMJT350T1	SOT−223	1000 / Tape & Reel

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Collector−Base Voltage	V_{CB}	300	Vdc
Emitter−Base Voltage	V_{EB}	3.0	Vdc
Collector Current − Continuous − Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	P_D	2.75 22 1.40 0.65	W mW/°C W W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction to Case − Junction−to−Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material − Junction−to−Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	45 85 190	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0 Adc)	$V_{CEO(SUS)}$	300	−	Vdc
Collector−Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	I_{CBO}	−	100	μAdc
Emitter Cut−off Current (V_{BE} = 5.0 Vdc)	I_{EBO}	−	100	μAdc
ON CHARACTERISTICS (Note)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 30 20	 240 −	−

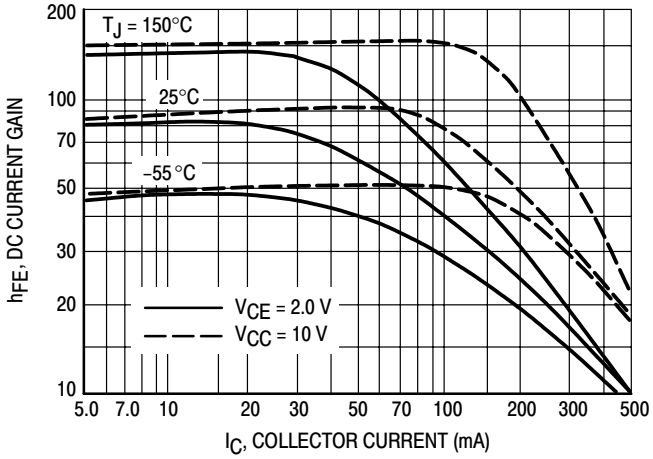


Figure 1. DC Current Gain

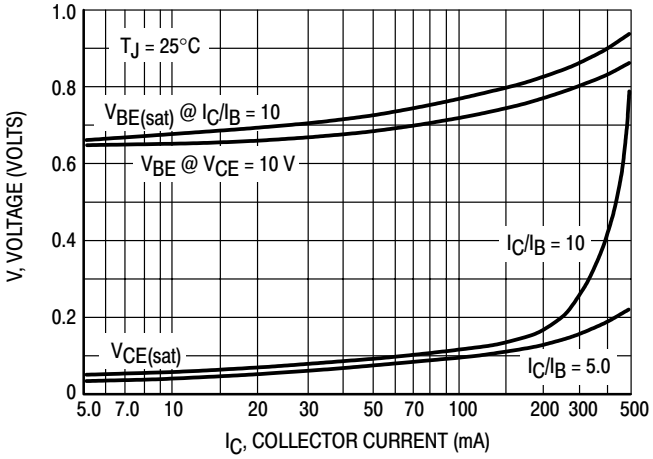


Figure 2. "On" Voltages

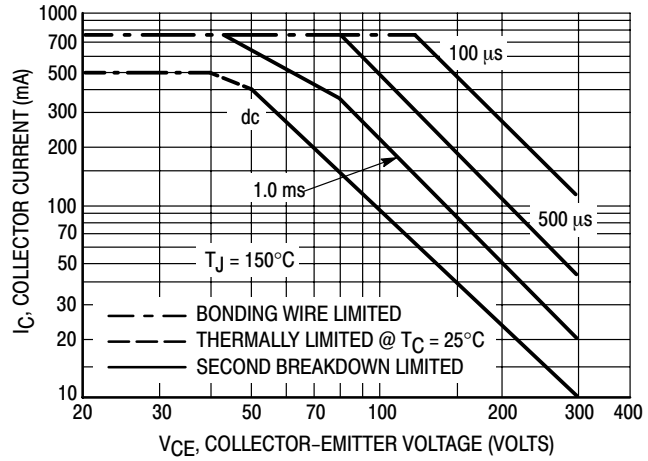


Figure 3. Active−Region Safe Operating Area

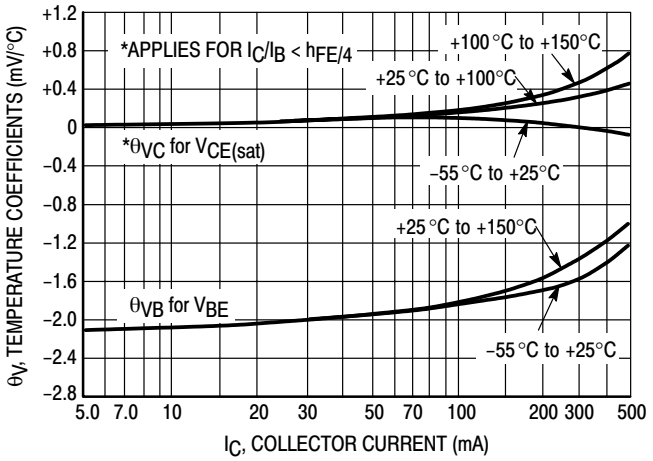


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

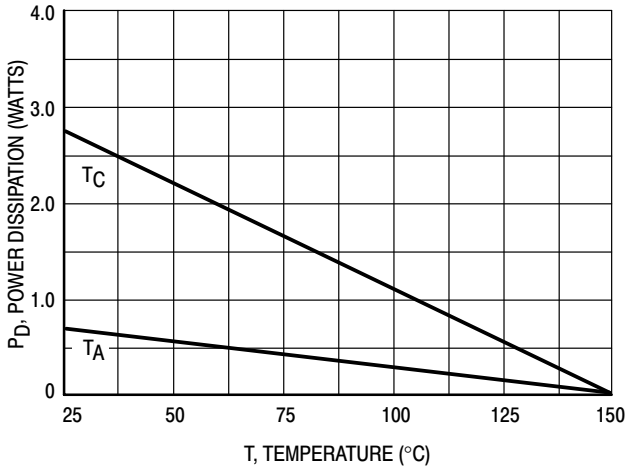


Figure 5. Power Derating

MMJT9410

Preferred Device

Bipolar Power Transistors

NPN Silicon

- Collector −Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain −
  h_{FE} = 85 (Min) @ I_C = 0.8 Adc
  = 60 (Min) @ I_C = 3.0 Adc
- Low Collector −Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.2 Vdc (Max) @ I_C = 1.2 Adc
  = 0.45 Vdc (Max) @ I_C = 3.0 Adc
- SOT−223 Surface Mount Packaging
- Epoxy Meets UL94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; > 8000 V
  Machine Model, C; > 400 V

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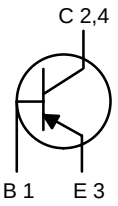
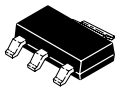
POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.2 VOLTS

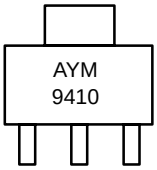


Schematic

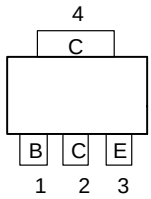


SOT−223
CASE 318E
Style 1

MARKING DIAGRAM



9410	= Specific Device Code
A	= Assembly Location
Y	= Last Digit of Year
M	= Month Code



Top View Pinout

ORDERING INFORMATION

Device	Package	Shipping
MMJT9410T1	SOT−223	1000 / Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	30	Vdc
Collector−Base Voltage	V_{CB}	45	Vdc
Emitter−Base Voltage	V_{EB}	6.0	Vdc
Base Current − Continuous	I_B	1.0	Adc
Collector Current − Continuous − Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	P_D	3.0 24 1.7 0.75	Watts mW/°C Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction to Case − Junction to Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material − Junction to Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 75 165	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	−	−	Vdc
Emitter−Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	−	−	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω) (V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)	I_{CER}	− −	− −	20 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	−	−	10	μAdc
ON CHARACTERISTICS (Note 1)					
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc) (I_C = 1.2 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	− − −	0.105 0.150 −	0.150 0.200 0.450	Vdc
Base−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	−	−	1.25	Vdc
Base−Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	−	−	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.2 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	85 80 60	200 − −	− − −	−
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	−	85	135	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	−	200	−	pF
Current−Gain − Bandwidth Product (Note 2) (I_C = 500 mA, V_{CE} = 10 Vdc, F_{test} = 1.0 MHz)	f_T	−	72	−	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{FE}| \bullet f_{test}$

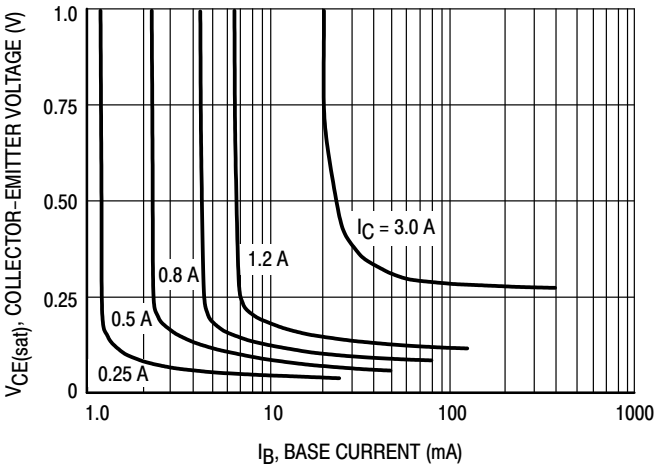


Figure 1. Collector Saturation Region

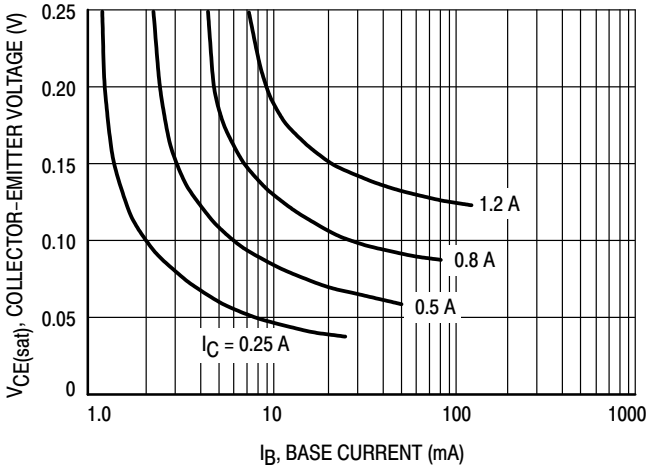


Figure 2. Collector Saturation Region

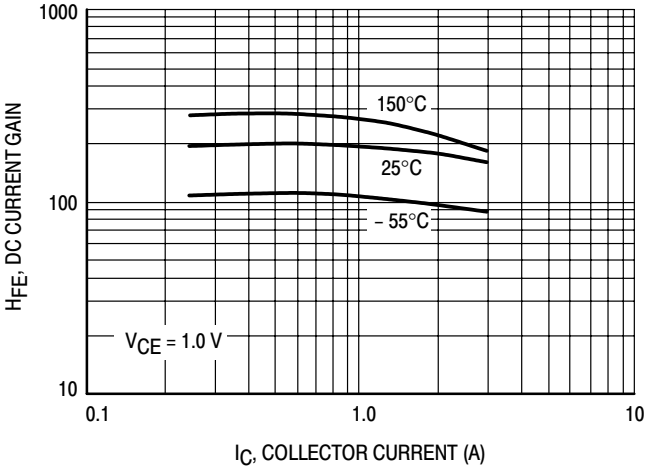


Figure 3. DC Current Gain

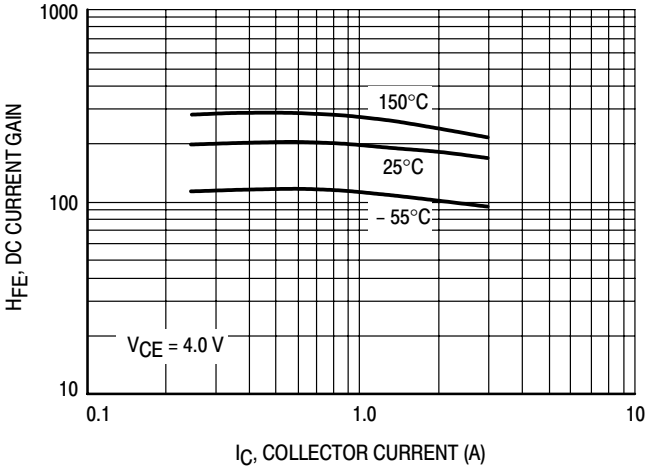


Figure 4. DC Current Gain

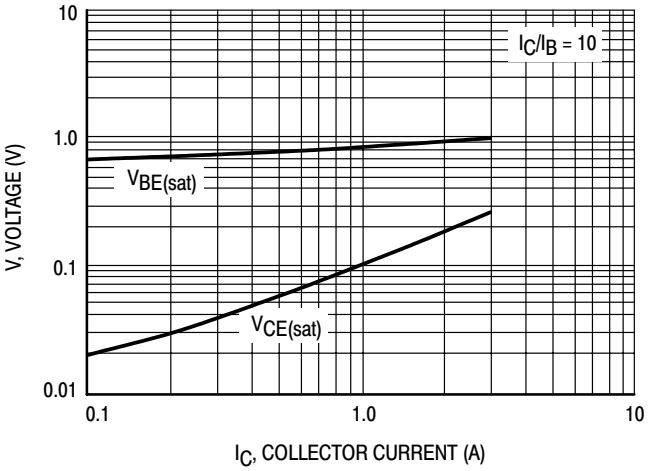


Figure 5. “On” Voltages

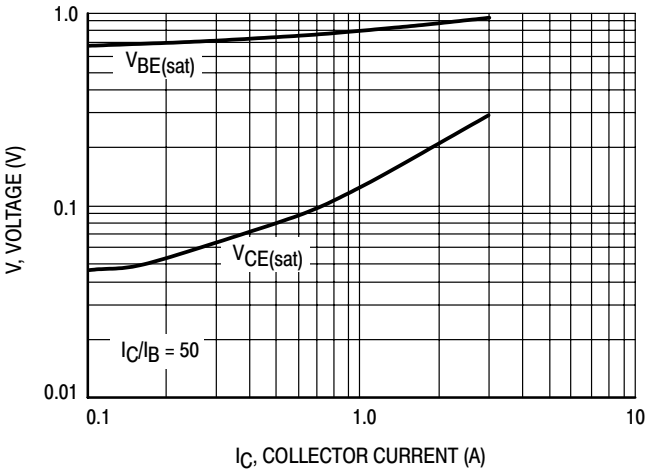


Figure 6. “On” Voltages

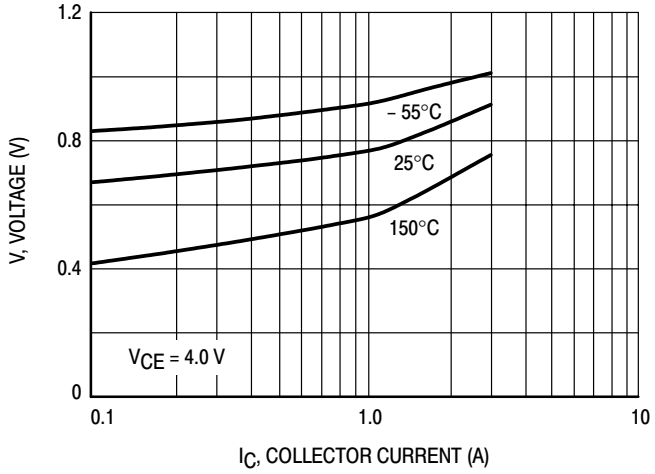


Figure 7. $V_{BE(on)}$ Voltage

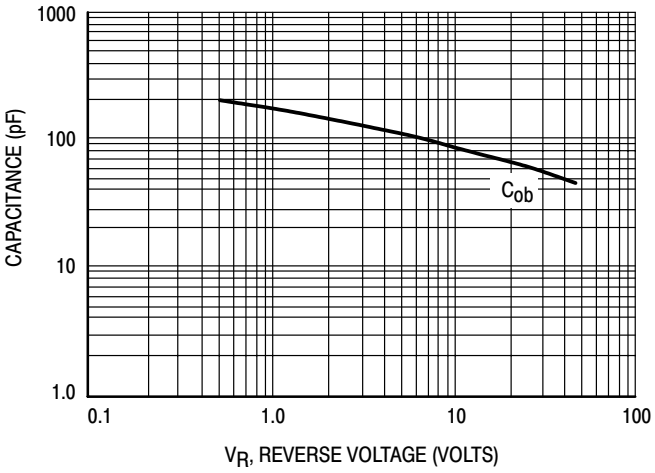


Figure 8. Capacitance

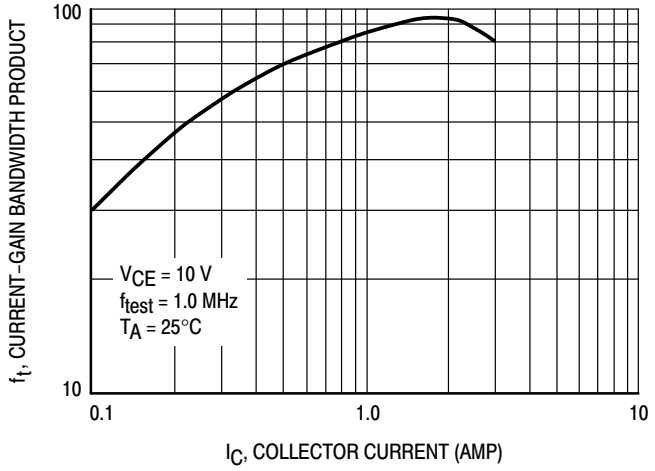


Figure 9. Current−Gain Bandwidth Product

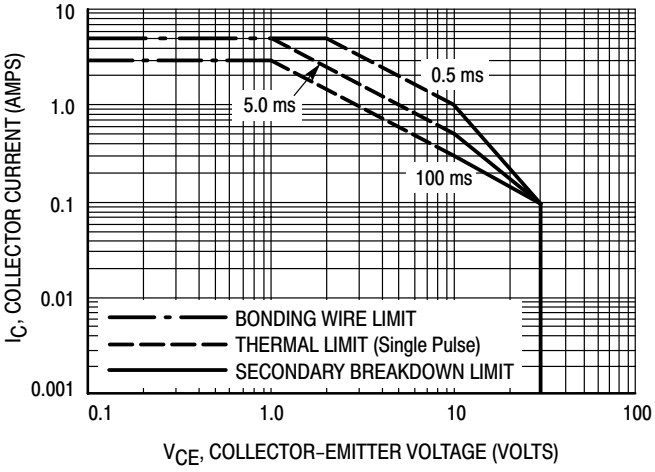


Figure 10. Active Region Safe Operating Area

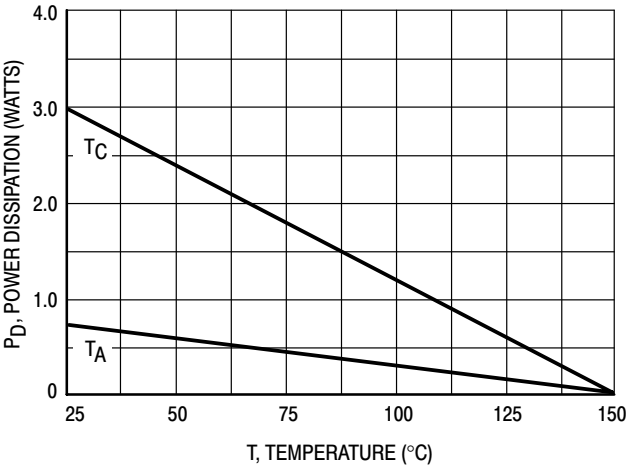


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

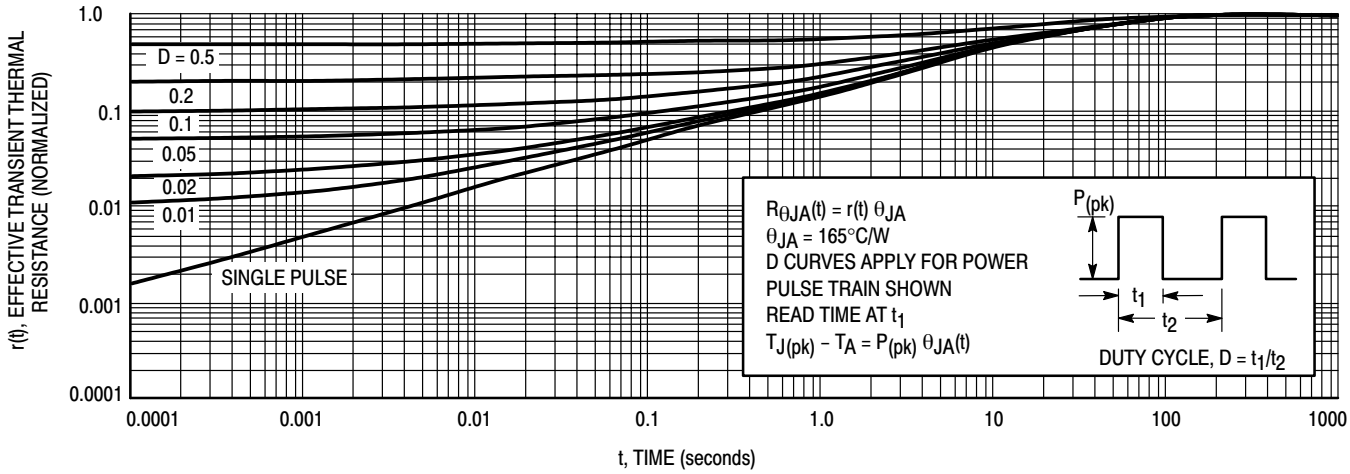


Figure 12. Thermal Response

MMJT9435

Preferred Device

Bipolar Power Transistors

PNP Silicon

Features

- Pb−Free Packages are Available
- Collector −Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain −
  h_{FE} = 125 (Min) @ I_C = 0.8 Adc
  = 90 (Min) @ I_C = 3.0 Adc
- Low Collector −Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.275 Vdc (Max) @ I_C = 1.2 Adc
  = 0.55 Vdc (Max) @ I_C = 3.0 Adc
- SOT−223 Surface Mount Packaging
- Epoxy Meets UL 94, V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; > 8000 V
  Machine Model, C; > 400 V

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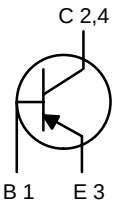
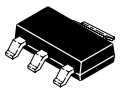
POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.275 VOLTS

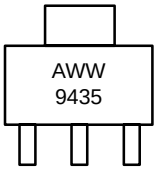


Schematic

MARKING DIAGRAM

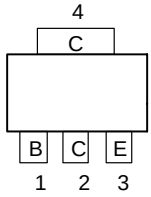


SOT−223
CASE 318E
STYLE 1



9435 = Specific Device Code
A = Assembly Location
WW = Work Week

PIN ASSIGNMENT



Top View Pinout

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 745 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	30	Vdc
Collector−Base Voltage	V_{CB}	45	Vdc
Emitter−Base Voltage	V_{EB}	6.0	Vdc
Base Current − Continuous	I_B	1.0	Adc
Collector Current − Continuous − Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	P_D	3.0 24 1.56 0.72	W mW/°C W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case − Junction−to−Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material − Junction−to−Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 80 174	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

ORDERING INFORMATION

Device	Package	Shipping†
MMJT9435T1	SOT−223	1000 / Tape & Reel
MMJT9435T1G	SOT−223 (Pb−Free)	1000 / Tape & Reel
MMJT9435T3	SOT−223	4000 / Tape & Reel
MMJT9435T3G	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	–	–	Vdc
Emitter−Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω) (V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)	I_{CER}	– –	– –	20 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	–	–	10	μAdc
ON CHARACTERISTICS (Note 3)					
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc) (I_C = 1.2 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	– – –	0.155 – –	0.210 0.275 0.550	Vdc
Base−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	–	–	1.25	Vdc
Base−Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	–	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.2 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	125 110 90	220 – –	– – –	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	–	100	150	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	–	135	–	pF
Current−Gain − Bandwidth Product (Note 4) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T	–	110	–	MHz

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. $f_T = |h_{FE}| \bullet f_{test}$

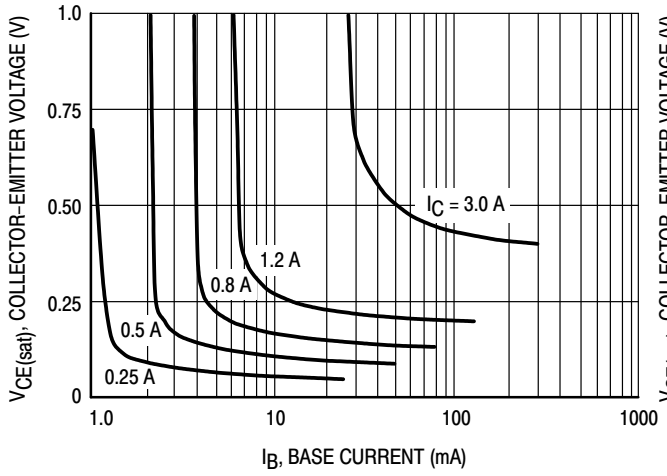


Figure 1. Collector Saturation Region

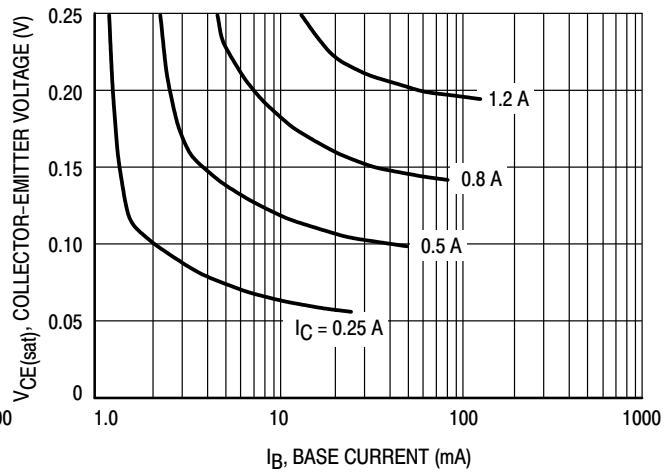


Figure 2. Collector Saturation Region

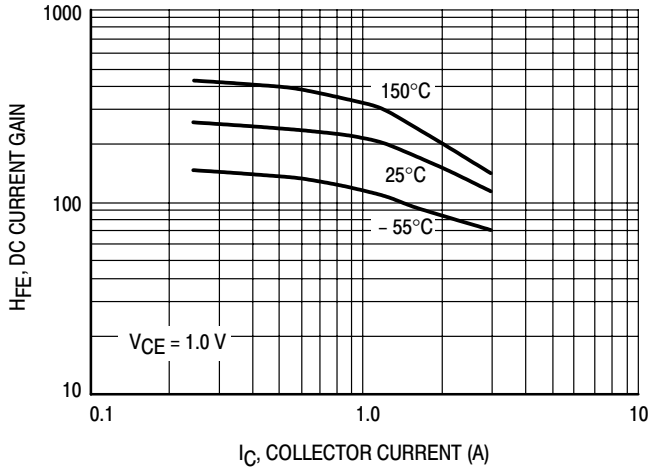


Figure 3. DC Current Gain

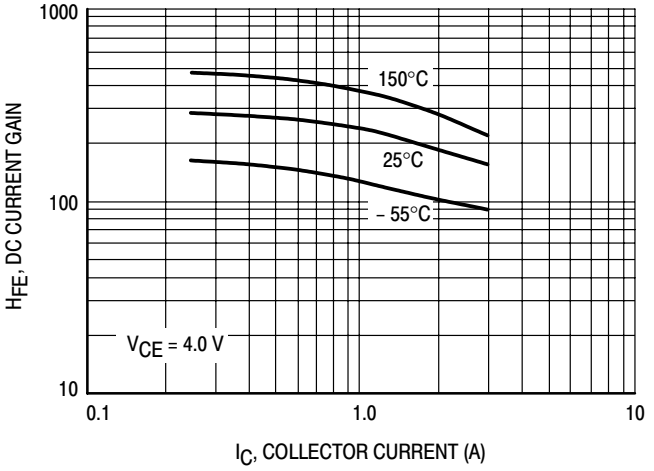


Figure 4. DC Current Gain

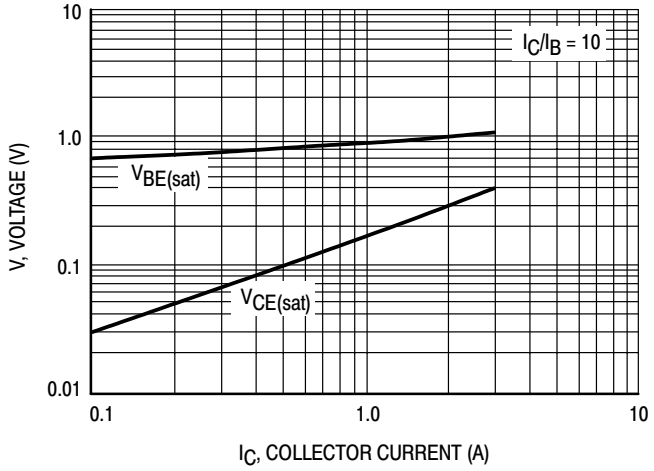


Figure 5. “On” Voltages

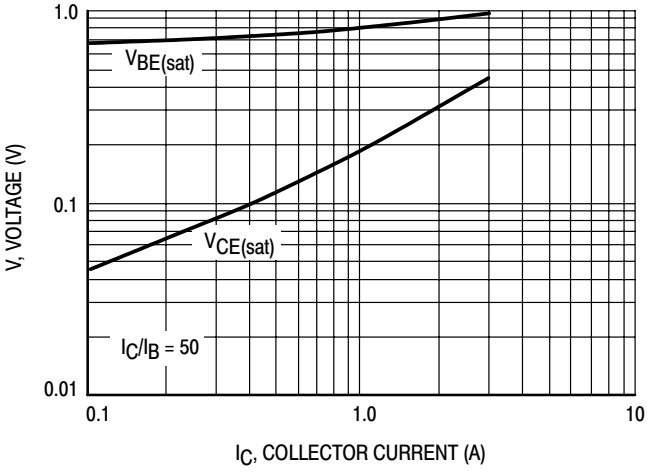


Figure 6. “On” Voltages

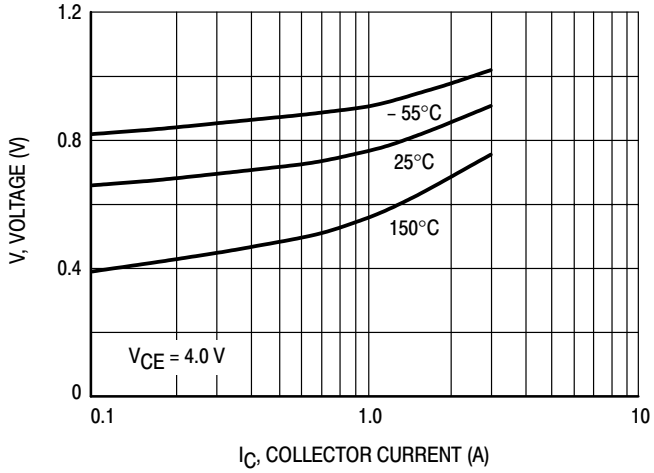


Figure 7. $V_{BE(on)}$ Voltage

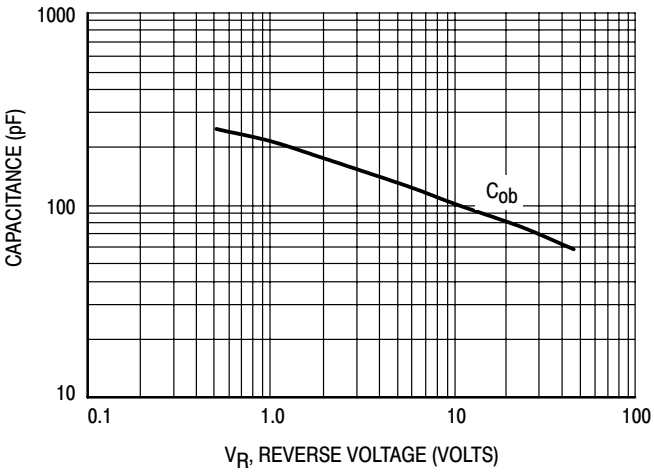


Figure 8. Output Capacitance

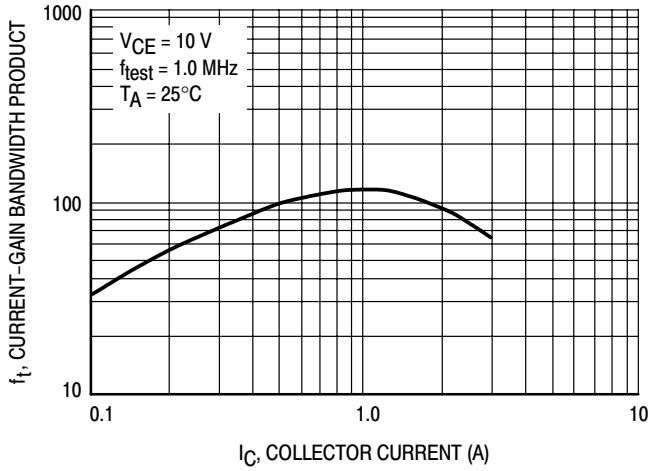


Figure 9. Current−Gain Bandwidth Product

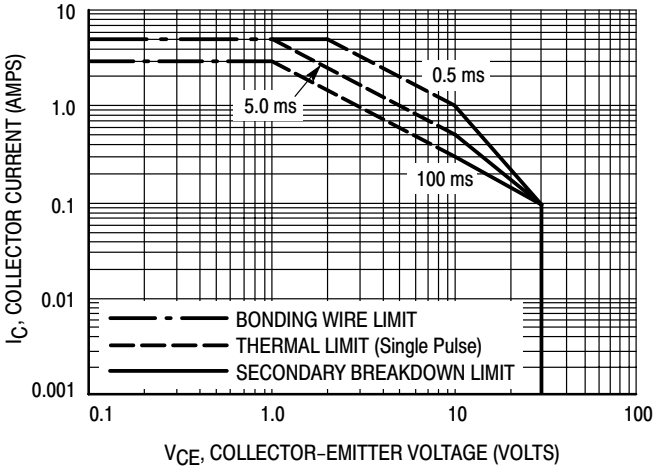


Figure 10. Active Region Safe Operating Area

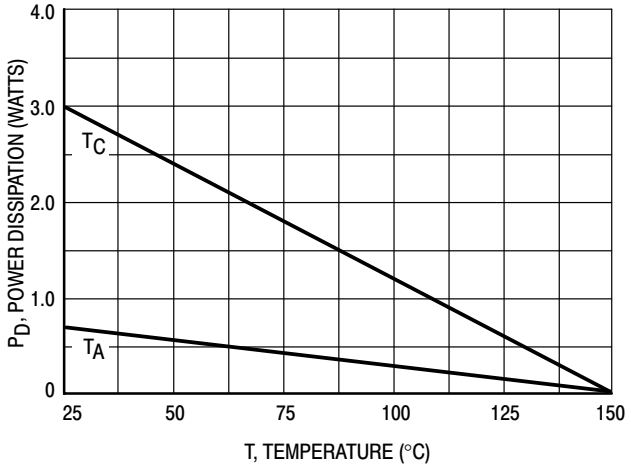


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

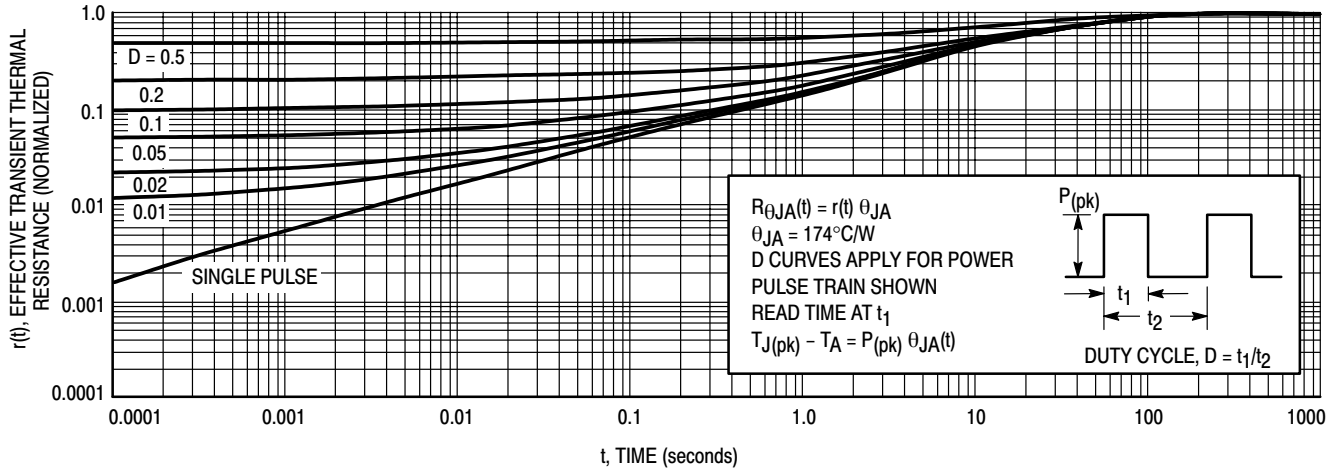


Figure 12. Thermal Response

NJD2873T4

Plastic Power Transistors

NPN Silicon DPAK For Surface Mount Applications

Designed for high−gain audio amplifier applications.

Features

- Pb−Free Package is Available
- High DC Current Gain −
  h_{FE} = 120 (Min) @ I_C = 500 mA
  = 40 (Min) @ I_C = 2 A
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 1 A
- High Current−Gain − Bandwidth Product −
  f_T = 65 MHz (Min) @ I_C = 100 mA
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Base Voltage	V_{CB}	50	Vdc
Collector−Emitter Voltage	V_{CEO}	50	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current Continuous Peak	I_C	2 3	Adc
Base Current	I_B	0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	W W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Case Junction−to−Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

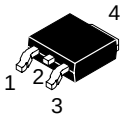
*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ON Semiconductor®

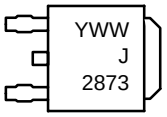
http://onsemi.com

SILICON
POWER TRANSISTORS
2 AMPERES
50 VOLTS
12.5 WATTS

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NJD2873T4	DPAK	2500 Units / Reel
NJD2873T4G	DPAK (Pb−Free)	2500 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	50	−	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	−	100	nAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 1) (I_C = 0.5 A, V_{CE} = 2 V) (I_C = 2 Adc, V_{CE} = 2 Vdc)	h_{FE}	120 40	360 −	−
Collector−Emitter Saturation Voltage (Note 1) (I_C = 1 A, I_B = 0.05 A)	$V_{CE(sat)}$	−	0.3	Vdc
Base−Emitter Saturation Voltage (Note 1) (I_C = 1 A, I_B = 0.05 Adc)	$V_{BE(sat)}$	−	1.2	Vdc
Base−Emitter On Voltage (Note 1) (I_C = 1 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	−	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	−	80	pF

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

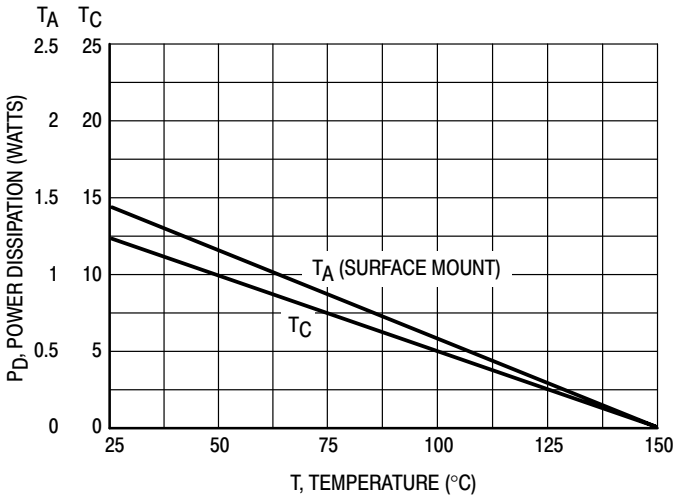


Figure 13. Power Derating

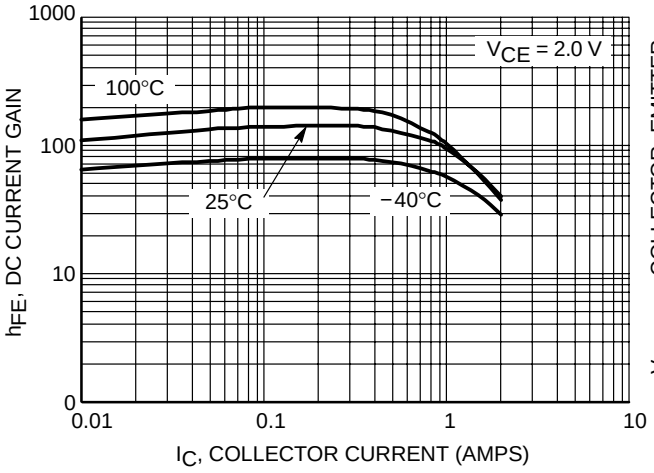


Figure 14. DC Current Gain

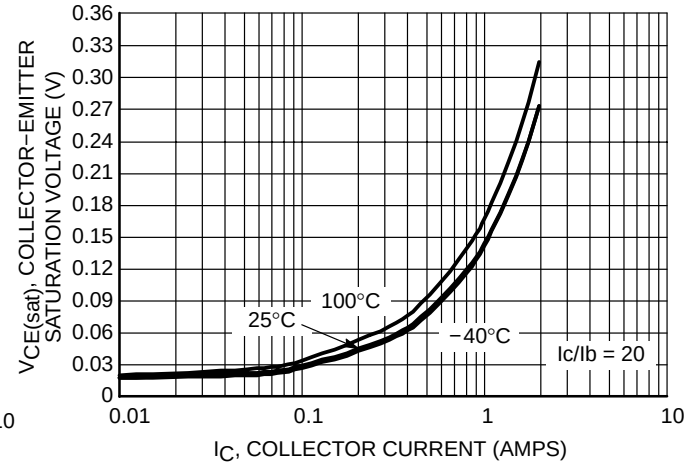


Figure 15. Collector−Emitter Saturation Voltage

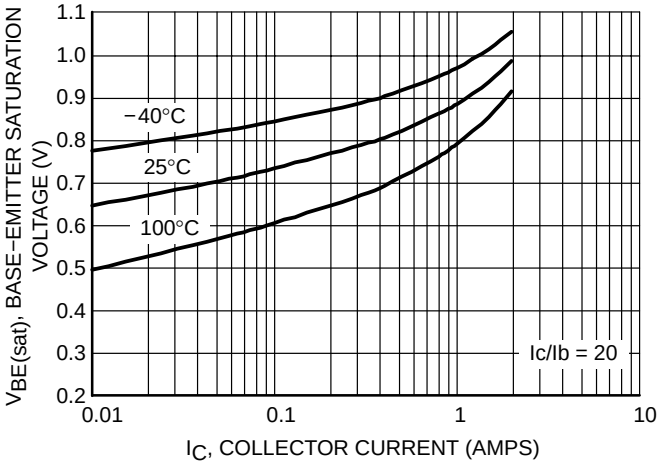


Figure 16. Base−Emitter Saturation Voltage

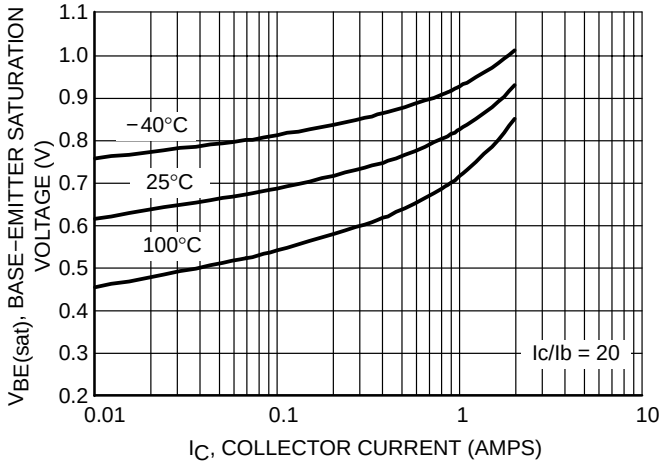


Figure 17. Base−Emitter Saturation Voltage

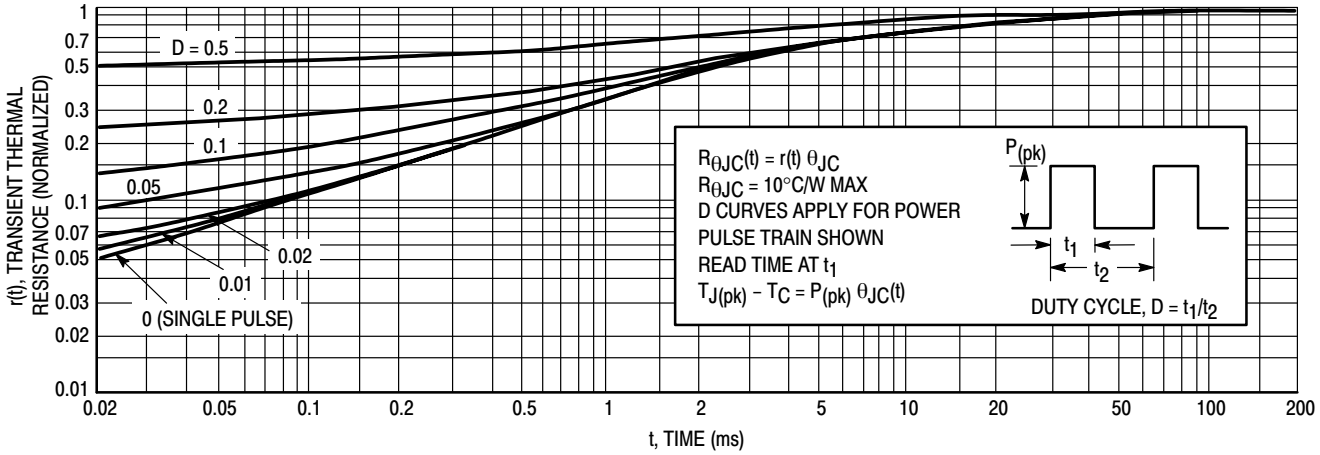


Figure 18. Thermal Response

Plastic Medium-Power Complementary Silicon Transistors

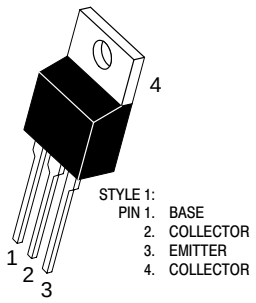
. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP100, TIP105
  = 80 Vdc (Min) — TIP101, TIP106
  = 100 Vdc (Min) — TIP102, TIP107
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built−in Base−Emitter Shunt Resistors
- TO−220AB Compact Package

NPN
TIP100
TIP101*
TIP102*
PNP
TIP105
TIP106*
TIP107*

*ON Semiconductor Preferred Device

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60−80−100 VOLTS
80 WATTS



CASE 221A−09
TO−220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 15			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64			Watts W/°C
Unclamped Inductive Load Energy (1)	E	30			mJ
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 10
Publication Order Number:
TIP100/D

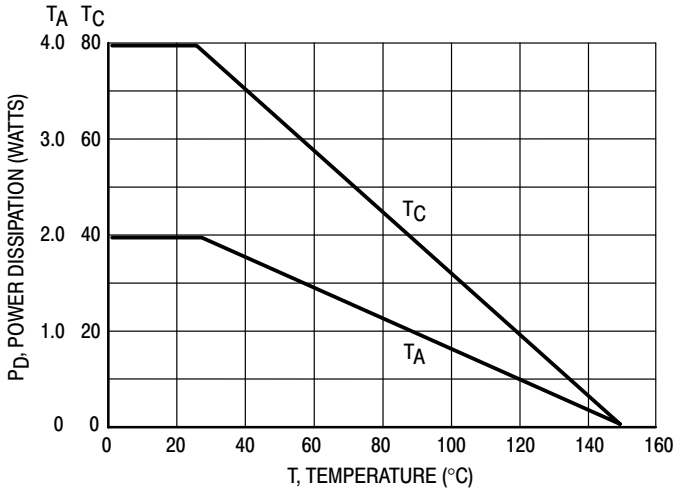


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP100, TIP105		60	—	
	TIP101, TIP106		80	—	
	TIP102, TIP107		100	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP100, TIP105		—	50	
(V_{CE} = 40 Vdc, I_B = 0)	TIP101, TIP106		—	50	
(V_{CE} = 50 Vdc, I_B = 0)	TIP102, TIP107		—	50	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP100, TIP105		—	50	
(V_{CB} = 80 Vdc, I_E = 0)	TIP101, TIP106		—	50	
(V_{CB} = 100 Vdc, I_E = 0)	TIP102, TIP107		—	50	
Emitter Cutoff Current		I_{EBO}	—	8.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)			200	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 6.0 mAdc)			—	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			—	2.5	
Base−Emitter On Voltage		$V_{BE(on)}$	—	2.8	Vdc
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain		h_{fe}	4.0	—	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					—
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107		—	300	
	TIP100, TIP101, TIP102		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

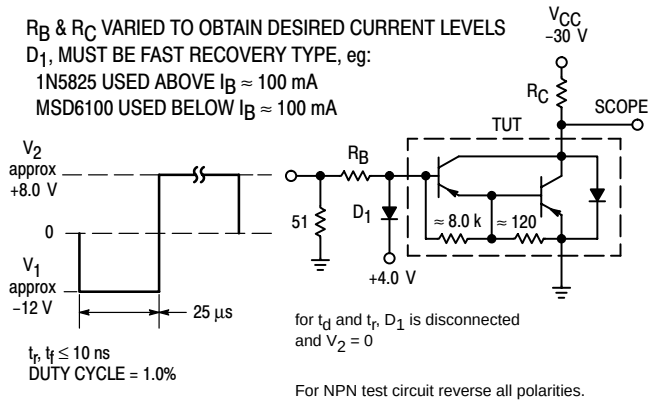


Figure 2. Switching Times Test Circuit

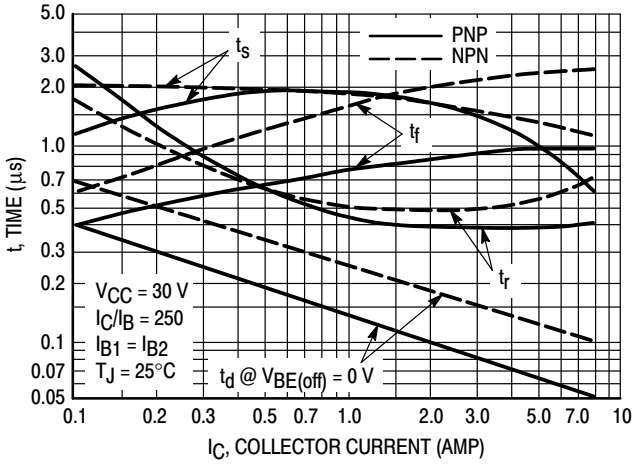


Figure 3. Switching Times

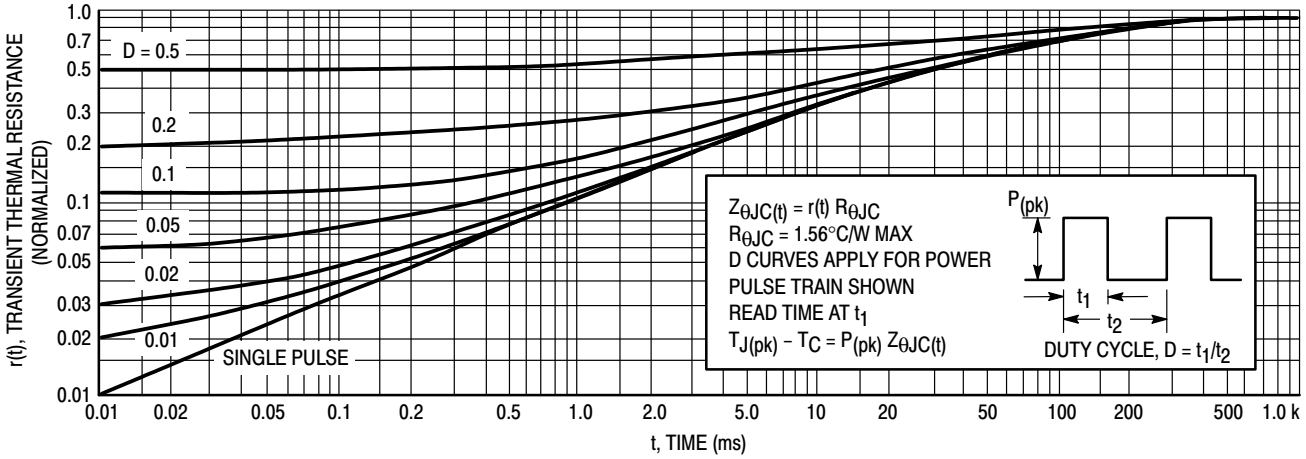


Figure 4. Thermal Response

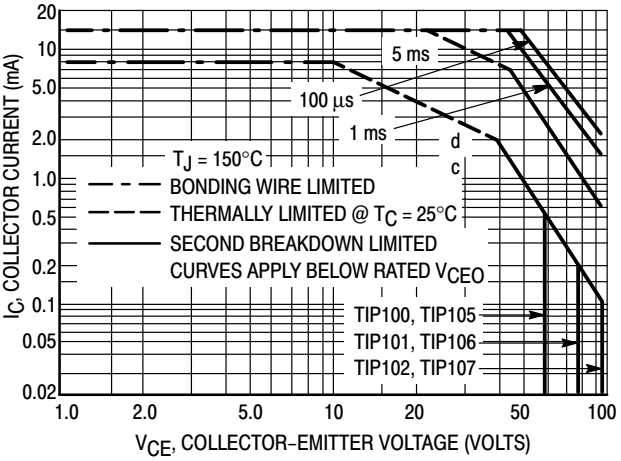


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

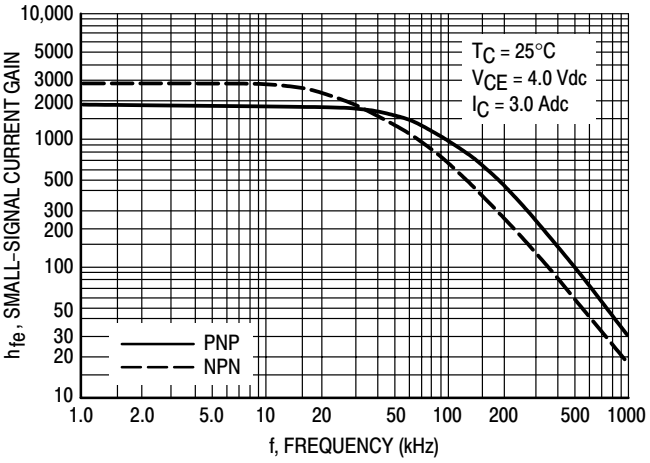


Figure 6. Small−Signal Current Gain

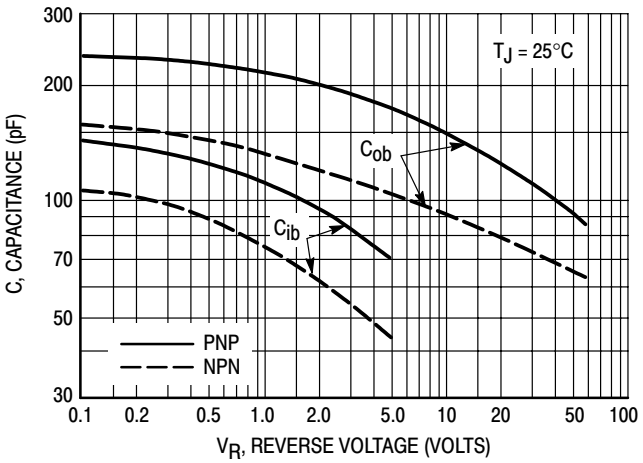
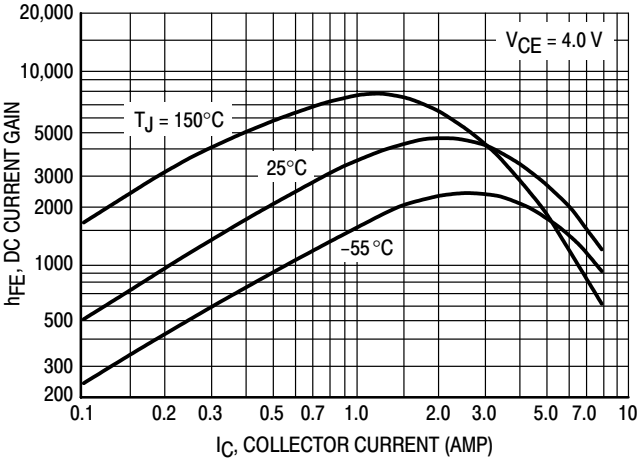


Figure 7. Capacitance

NPN
TIP100, TIP101, TIP102



PNP
TIP105, TIP106, TIP107

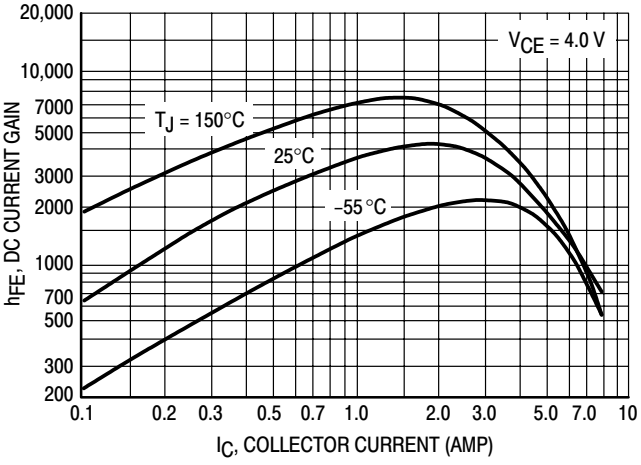
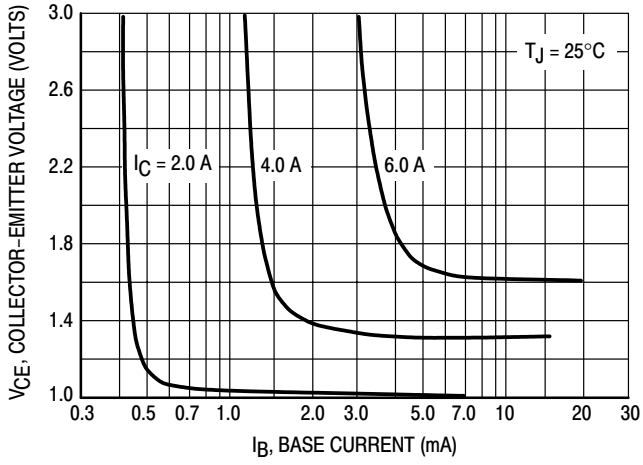


Figure 8. DC Current Gain



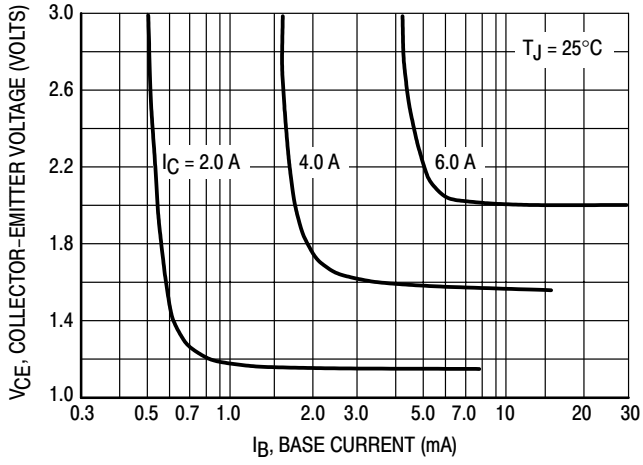
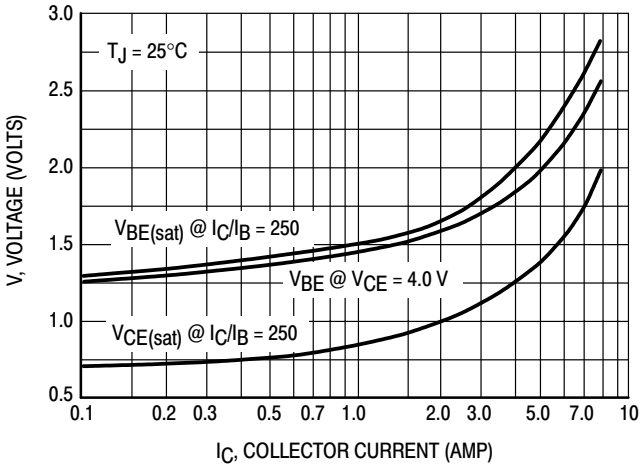


Figure 9. Collector Saturation Region



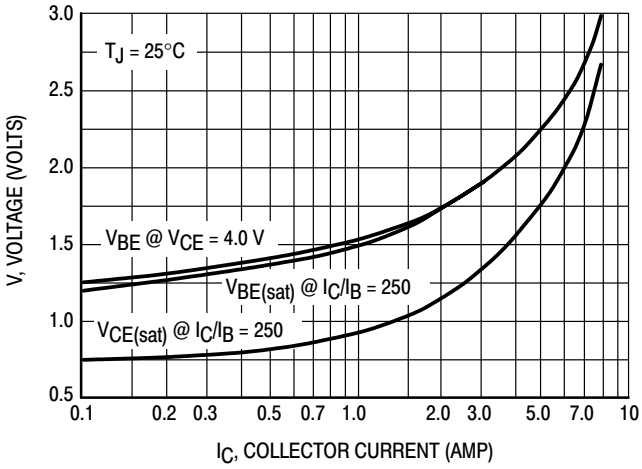


Figure 10. “On” Voltages

Plastic Medium-Power Complementary Silicon Transistors

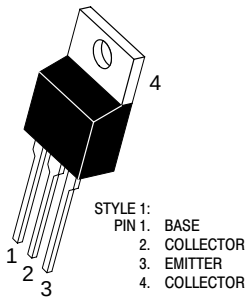
. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C
  = 1.0 Adc
- Collector−Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP110, TIP115
  = 80 Vdc (Min) — TIP111, TIP116
  = 100 Vdc (Min) — TIP112, TIP117
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C
  = 2.0 Adc
- Monolithic Construction with Built−in Base−Emitter Shunt Resistors
- TO−220AB Compact Package

NPN
TIP110
TIP111*
TIP112*
PNP
TIP115
TIP116*
TIP117*

***ON Semiconductor Preferred Device**

DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60−80−100 VOLTS
50 WATTS



CASE 221A−09
TO−220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	2.0 4.0			Adc
Base Current	I_B	50			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy — Figure 13	E	25			mJ
Operating and Storage Junction	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

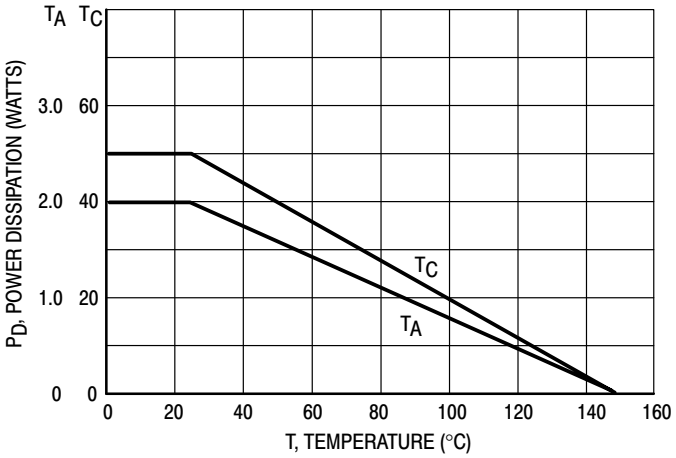


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP110, TIP115 TIP111, TIP116 TIP112 ,TIP117	I_{CEO}	 — — —	 2.0 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	I_{CBO}	 — — —	 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 1000 500	 — —	—
Collector−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		$V_{CE(sat)}$	—	2.5	Vdc
Base−Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		h_{fe}	25	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 TIP115, TIP116, TIP117 TIP110, TIP111, TIP112	C_{ob}	 — —	 200 100	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

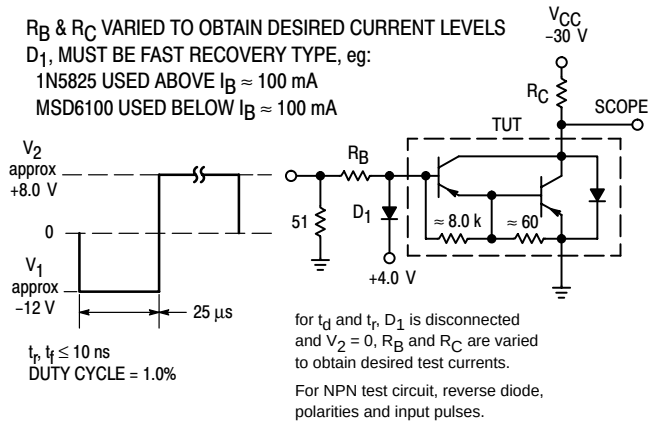


Figure 2. Switching Times Test Circuit

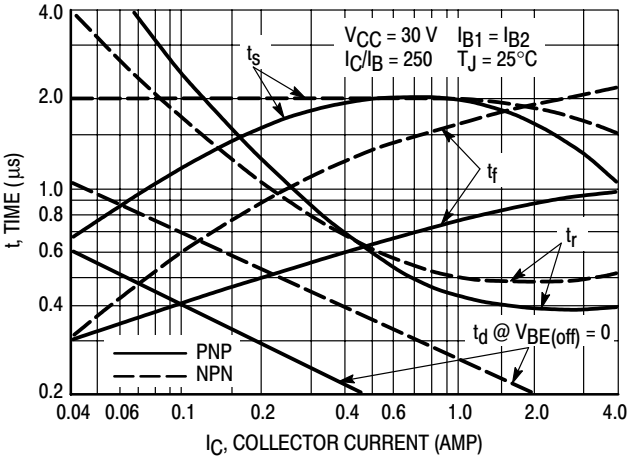


Figure 3. Switching Times

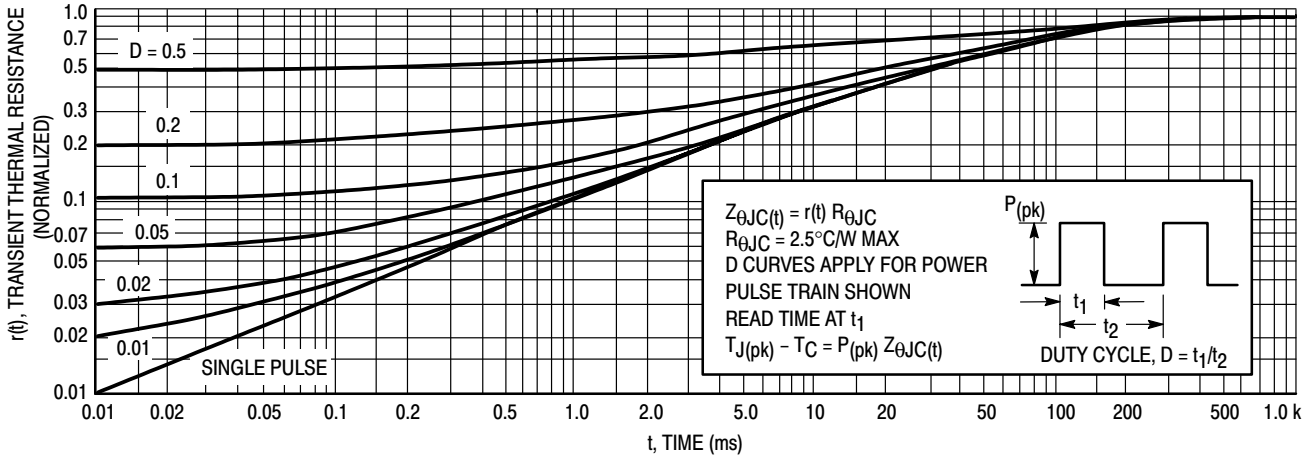


Figure 4. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

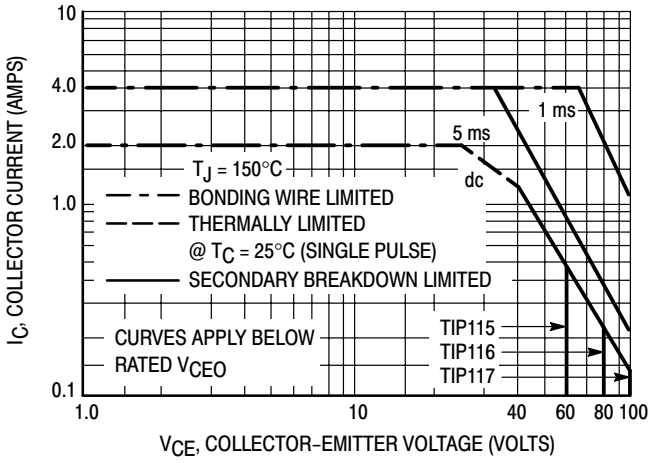


Figure 5. TIP115, 116, 117

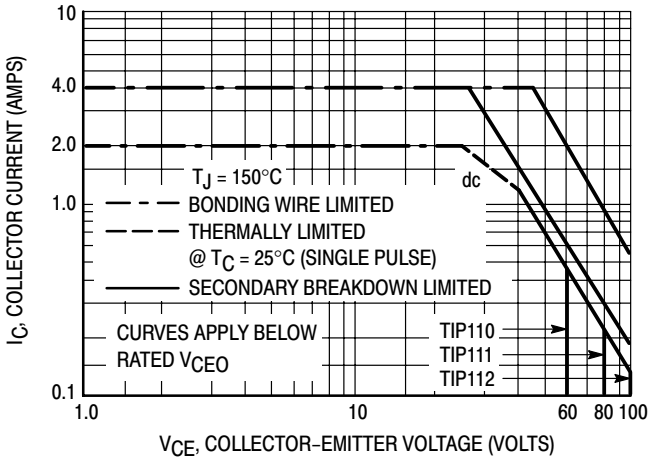


Figure 6. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

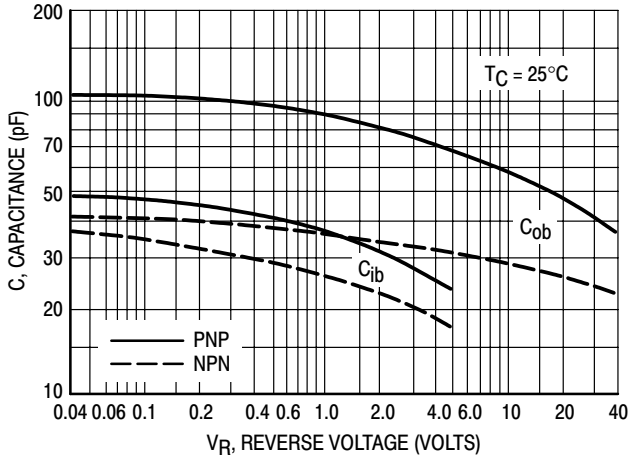
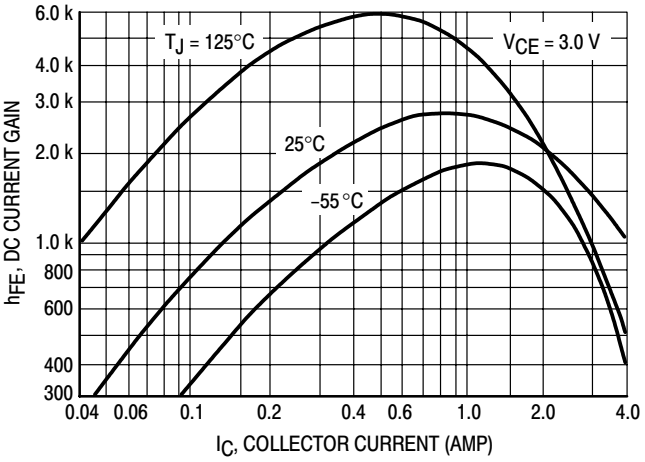


Figure 7. Capacitance

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

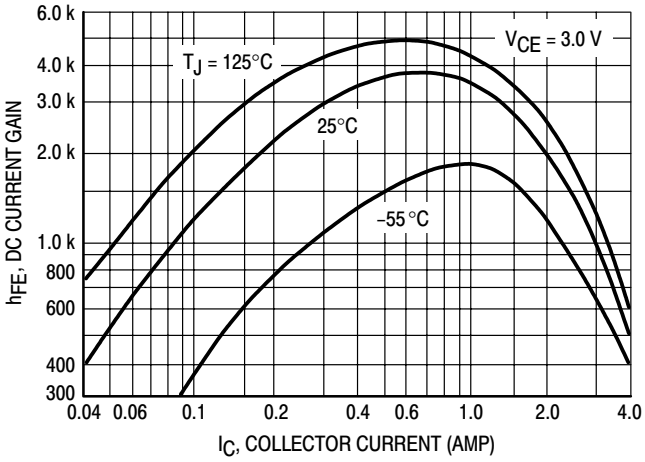
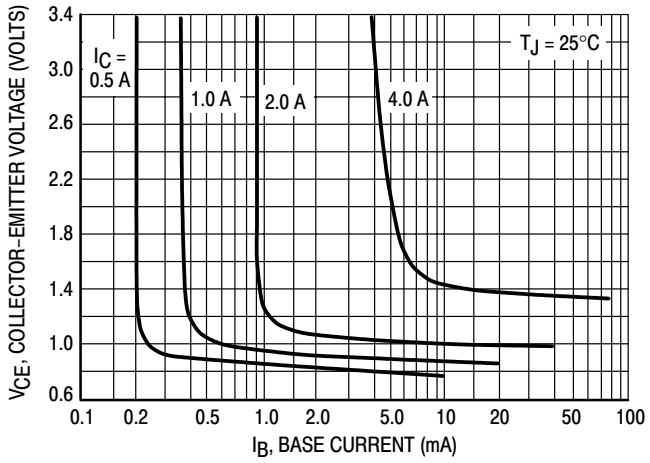


Figure 8. DC Current Gain



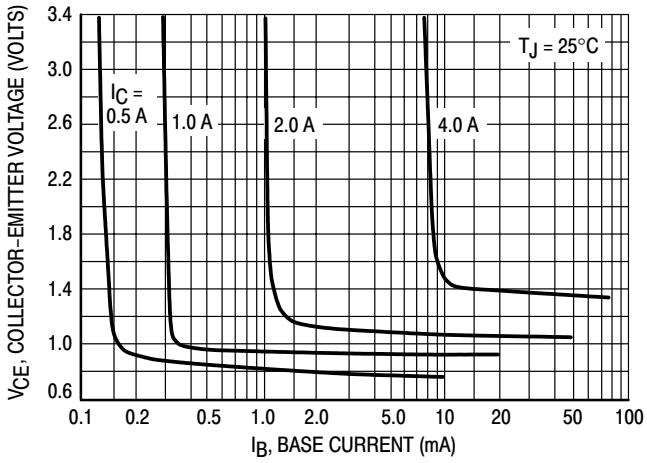
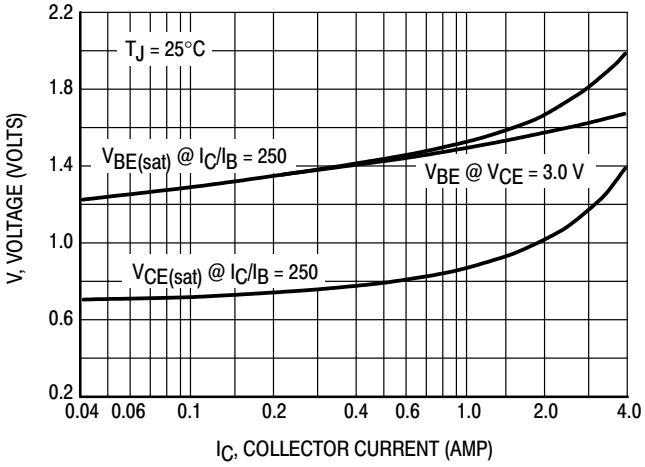


Figure 9. Collector Saturation Region



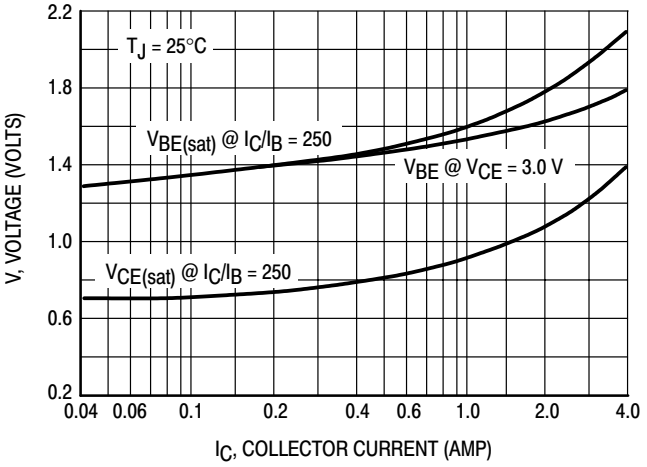
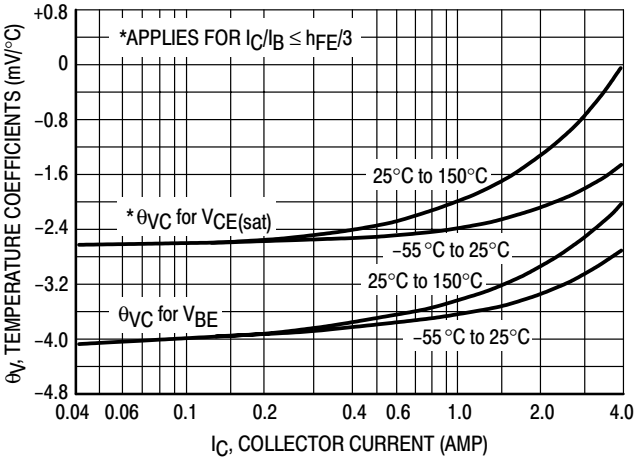


Figure 10. “On” Voltages

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

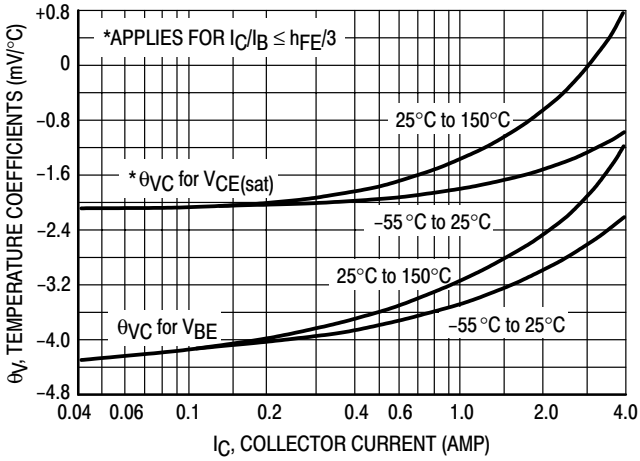
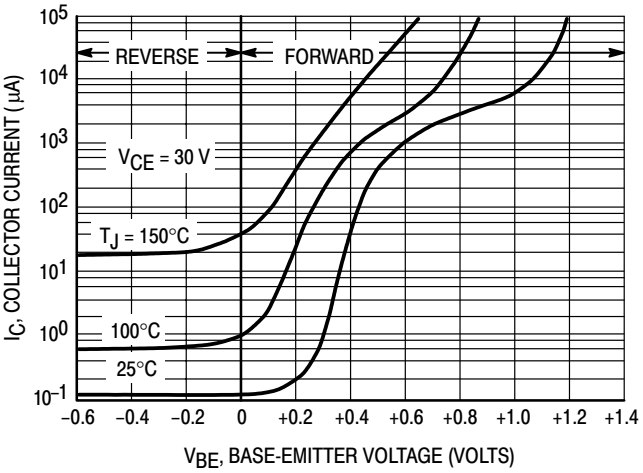


Figure 11. Temperature Coefficients



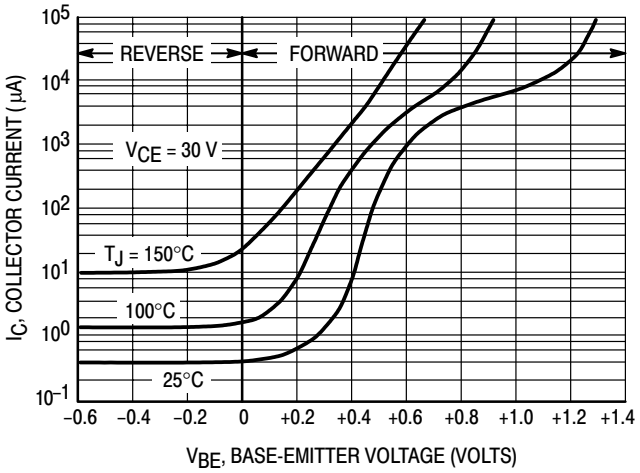
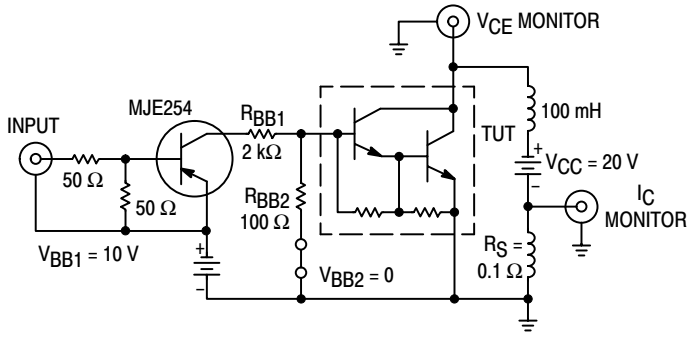


Figure 12. Collector Cut-Off Region

TEST CIRCUIT



Note A: Input pulse width is increased until I_{CM} = 0.71 A,
NPN test shown; for PNP test
reverse all polarity and use MJE224 driver.

VOLTAGE AND CURRENT WAVEFORMS

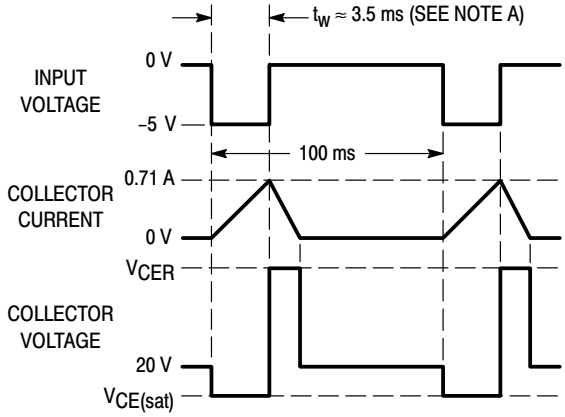


Figure 13. Inductive Load Switching

Plastic Medium-Power Complementary Silicon Transistors

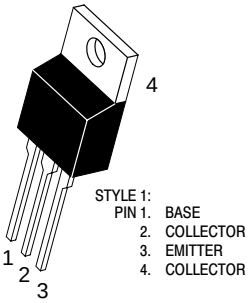
. . . designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP120, TIP125
  = 80 Vdc (Min) — TIP121, TIP126
  = 100 Vdc (Min) — TIP122, TIP127
- Low Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package

NPN
TIP120*
TIP121*
TIP122*
PNP
TIP125*
TIP126*
TIP127*

*ON Semiconductor Preferred Device

DARLINGTON
5 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60−80−100 VOLTS
65 WATTS



CASE 221A−09
TO−220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	5.0 8.0			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

April, 2002 − Rev. 5
Publication Order Number:
TIP120/D

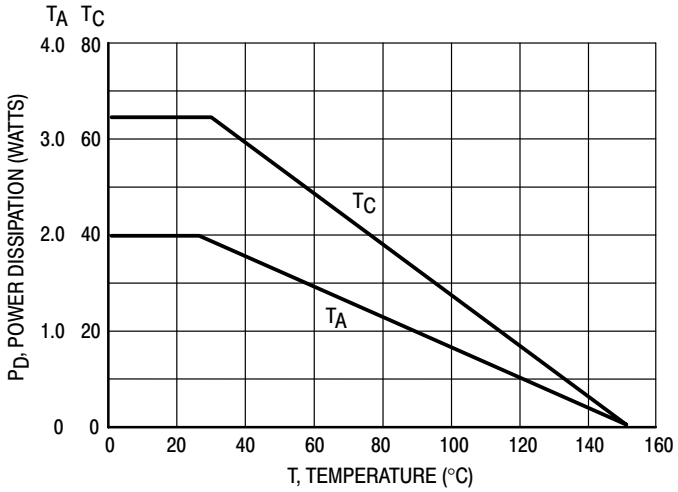


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	TIP120, TIP125		60	—	
	TIP121, TIP126		80	—	
	TIP122, TIP127		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP120, TIP125		—	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	TIP121, TIP126		—	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	TIP122, TIP127		—	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP120, TIP125		—	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	TIP121, TIP126		—	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	TIP122, TIP127		—	0.2	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			1000	—	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			—	2.0	
(I_C = 5.0 Adc, I_B = 20 mAdc)			—	4.0	
Base−Emitter On Voltage		$V_{BE(on)}$	—	2.5	Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain		h_{fe}	4.0	—	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz	TIP125, TIP126, TIP127		—	300	
	TIP120, TIP121, TIP122		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

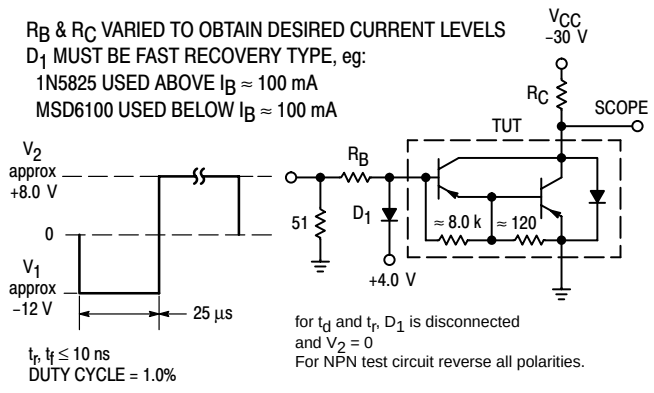


Figure 2. Switching Times Test Circuit

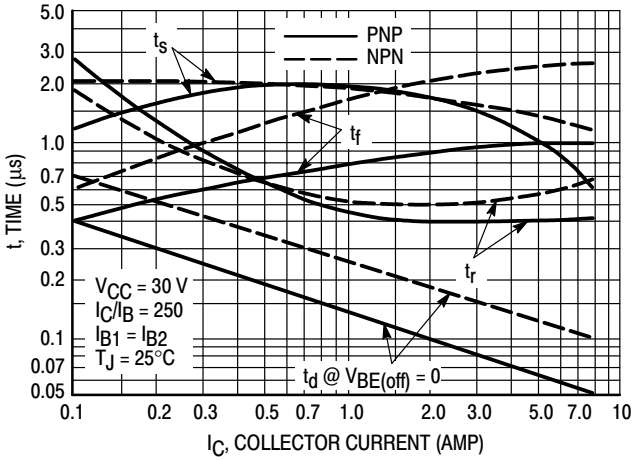


Figure 3. Switching Times

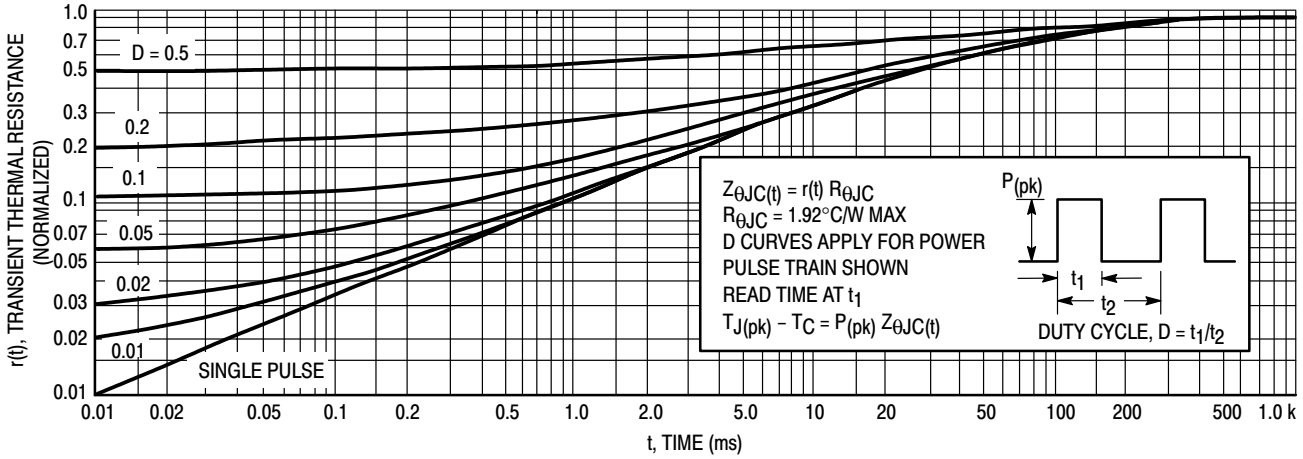


Figure 4. Thermal Response

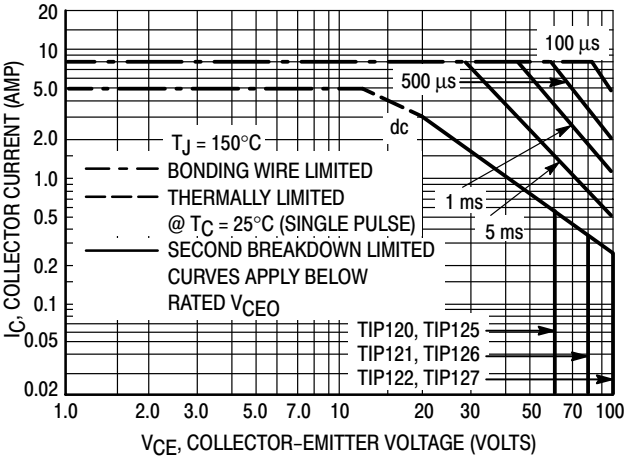


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

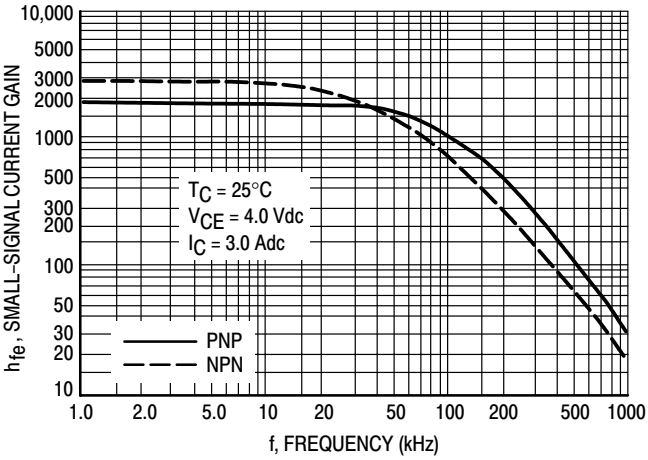


Figure 6. Small−Signal Current Gain

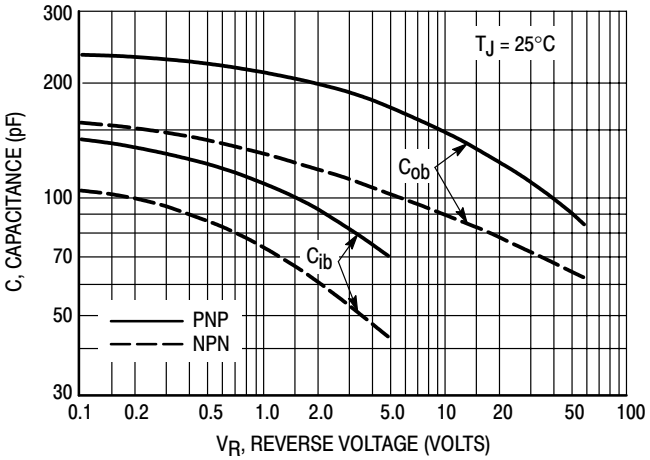
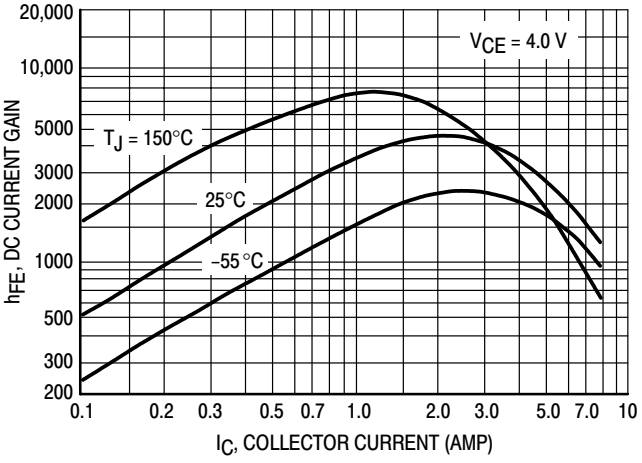


Figure 7. Capacitance

NPN
TIP120, TIP121, TIP122



PNP
TIP125, TIP126, TIP127

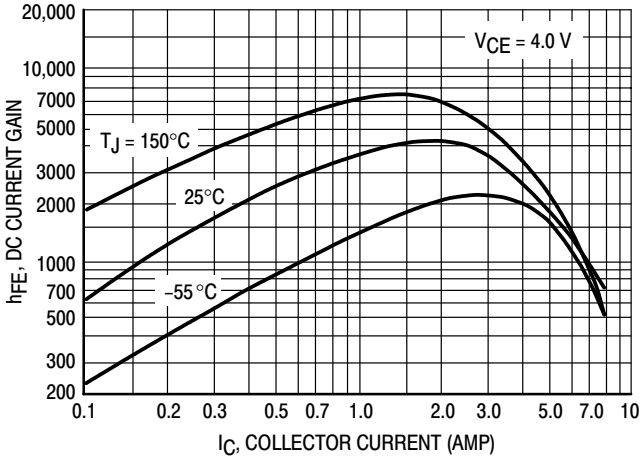
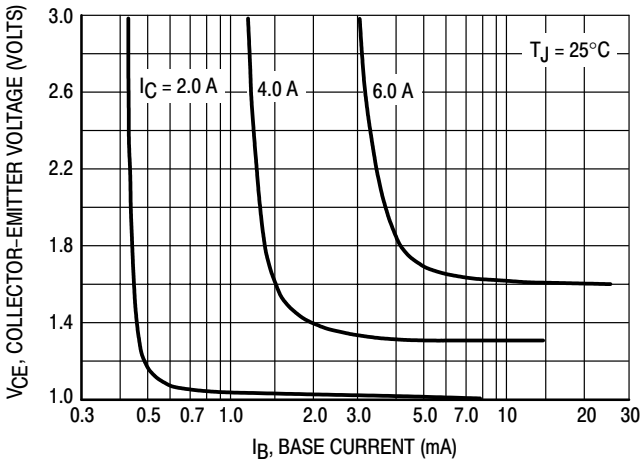


Figure 8. DC Current Gain



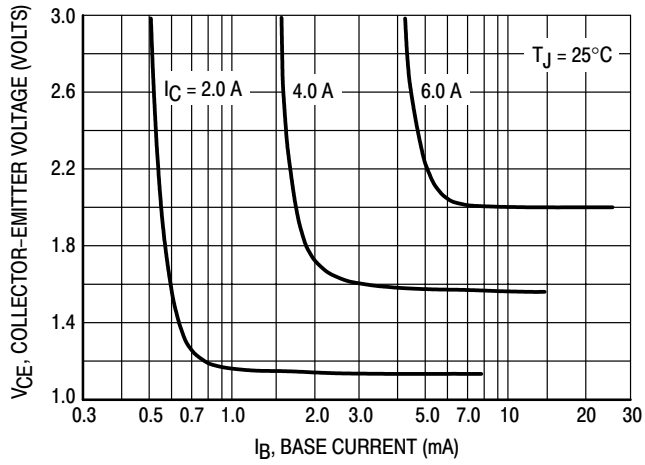
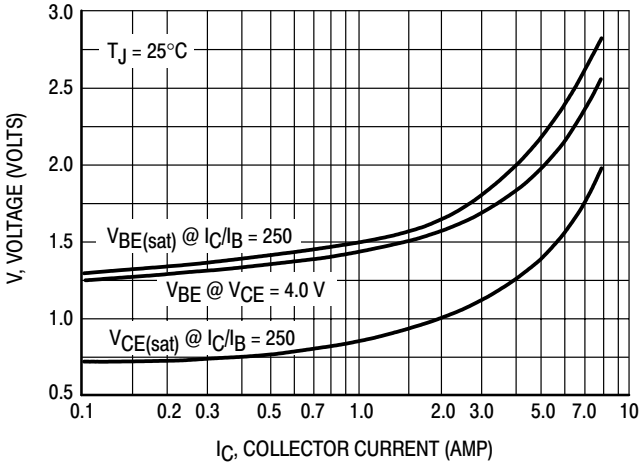


Figure 9. Collector Saturation Region



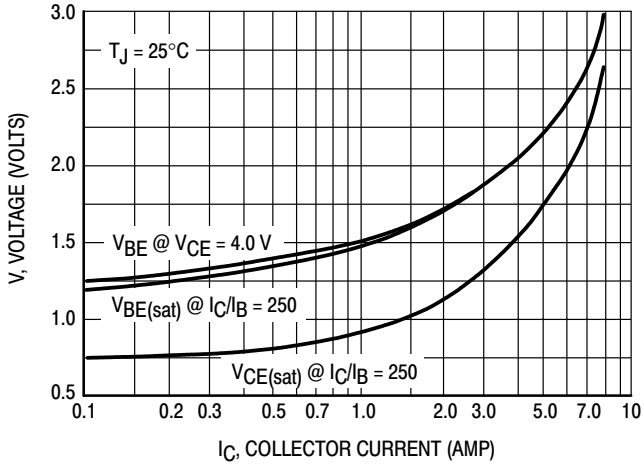


Figure 10. “On” Voltages

TIP131, TIP132 (NPN), TIP137 (PNP)

Preferred Devices

Darlington Complementary Silicon Power Transistors

Designed for general−purpose amplifier and low−speed switching applications.

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 30 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) − TIP131
  = 100 Vdc (Min) − TIP132, TIP137
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 6.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package

MAXIMUM RATINGS

Rating	Symbol	TIP131	TIP132, TIP137	Unit
Collector−Emitter Voltage	V_{CEO}	80	100	Vdc
Collector−Base Voltage	V_{CB}	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current − Continuous Peak	I_C	8.0 12		Adc
Base Current	I_B	300		mAdc
Total Power Dissipation @ T_C = 25°C	P_D	70		Watts
Total Power Dissipation @ T_A = 25°C	P_D	2.0		Watts
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	63.5	°C/W

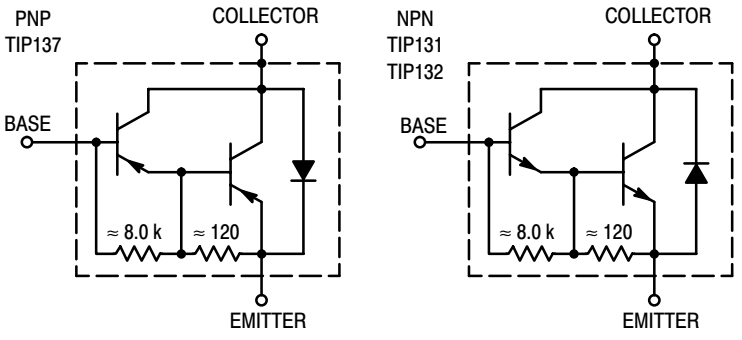
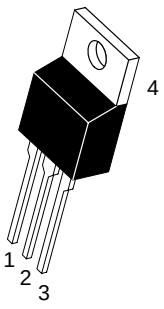


Figure 1. Darlington Circuit Schematic

ON Semiconductor®

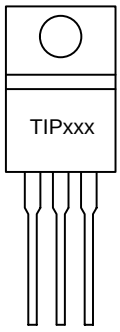
http://onsemi.com

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
80−100 VOLTS
70 WATTS



CASE 221A
TO−220AB

MARKING DIAGRAM



TIPxxx = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
TIP131	TO−220	50 Units/Rail
TIP132	TO−220	50 Units/Rail
TIP137	TO−220	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 30 mAdc, I_B = 0)	 TIP131 TIP132, TIP137	$V_{CEO(sus)}$	 80 100	 − −	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP131 TIP132, TIP137	I_{CEO}	 − −	 0.5 0.5	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP131 TIP132, TIP137	I_{CBO}	 − −	 0.2 0.2	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	5.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 500 1000	 − 15000	−
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc) (I_C = 6.0 Adc, I_B = 30 mAdc)		$V_{CE(sat)}$	 − −	 2.0 3.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	−	2.5	Vdc

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

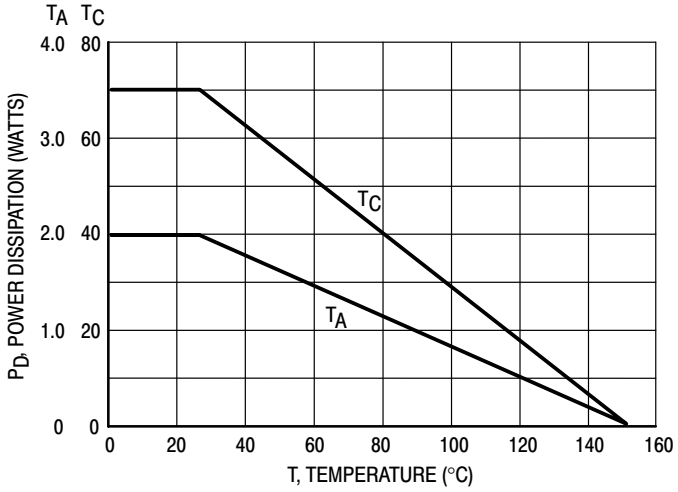


Figure 2. Power Derating

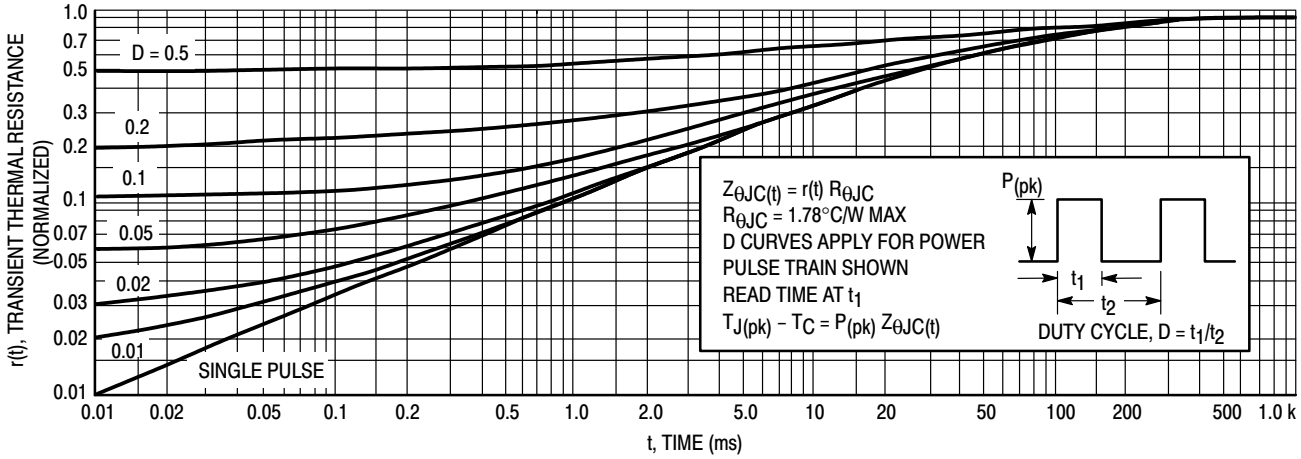


Figure 3. Thermal Response

Darlington Complementary Silicon Power Transistors

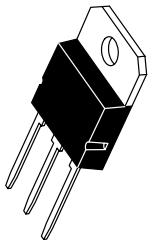
. . . designed for general−purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  Min h_{FE} = 1000 @ I_C
  = 5 A, V_{CE} = 4 V
- Collector−Emitter Sustaining Voltage — @ 30 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP140, TIP145
  80 Vdc (Min) — TIP141, TIP146
  100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built−In Base−Emitter Shunt Resistor

NPN
TIP140
TIP141*
TIP142*
PNP
TIP145
TIP146*
TIP147*

*ON Semiconductor Preferred Device

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 60−100 VOLTS 125 WATTS



CASE 340D−02

MAXIMUM RATINGS

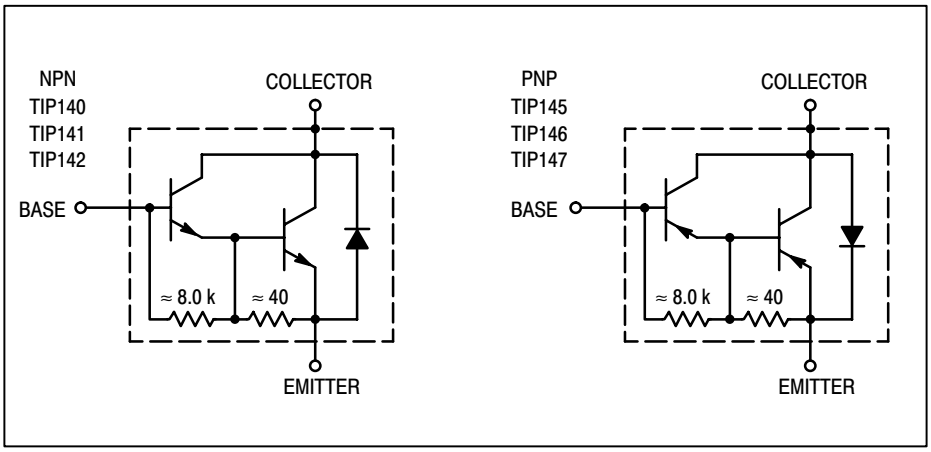
Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	10 15			Adc
Base Current — Continuous	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C	P_D	125			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	°C/W

(1) 5 ms, ≤ 10% Duty Cycle.

DARLINGTON SCHEMATICS



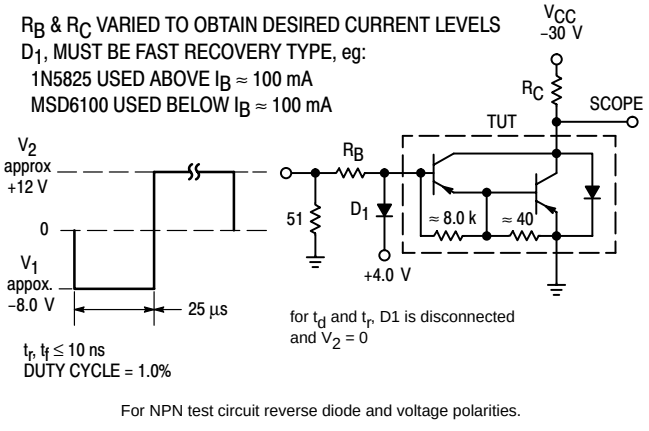
Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

January, 2002 − Rev. 4
Publication Order Number:
TIP140/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 30 mA, I_B = 0)	TIP140, TIP145		60	—	—	
	TIP141, TIP146		80	—	—	
	TIP142, TIP147		100	—	—	
Collector Cutoff Current		I_{CEO}				mA
(V_{CE} = 30 Vdc, I_B = 0)	TIP140, TIP145		—	—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP141, TIP146		—	—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP142, TIP147		—	—	2.0	
Collector Cutoff Current		I_{CBO}				mA
(V_{CB} = 60 V, I_E = 0)	TIP140, TIP145		—	—	1.0	
(V_{CB} = 80 V, I_E = 0)	TIP141, TIP146		—	—	1.0	
(V_{CB} = 100 V, I_E = 0)	TIP142, TIP147		—	—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 V)		I_{EBO}	—	—	2 0	mA
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 5.0 A, V_{CE} = 4.0 V)			1000	—	—	
(I_C = 10 A, V_{CE} = 4.0 V)			500	—	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 A, I_B = 10 mA)			—	—	2.0	
(I_C = 10 A, I_B = 40 mA)			—	—	3.0	
Base−Emitter Saturation Voltage		$V_{BE(sat)}$	—	—	3.5	Vdc
(I_C = 10 A, I_B = 40 mA)						
Base−Emitter On Voltage		$V_{BE(on)}$	—	—	3.0	Vdc
(I_C = 10 A, V_{CE} = 4.0 Vdc)						
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	(V_{CC} = 30 V, I_C = 5.0 A, I_B = 20 mA, Duty Cycle ≤ 2.0%, I_{B1} = I_{B2}, R_C & R_B Varied, T_J = 25°C)	t_d	—	0.15	—	μs
Rise Time		t_r	—	0.55	—	μs
Storage Time		t_s	—	2.5	—	μs
Fall Time		t_f	—	2.5	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 4. Switching Times Test Circuit

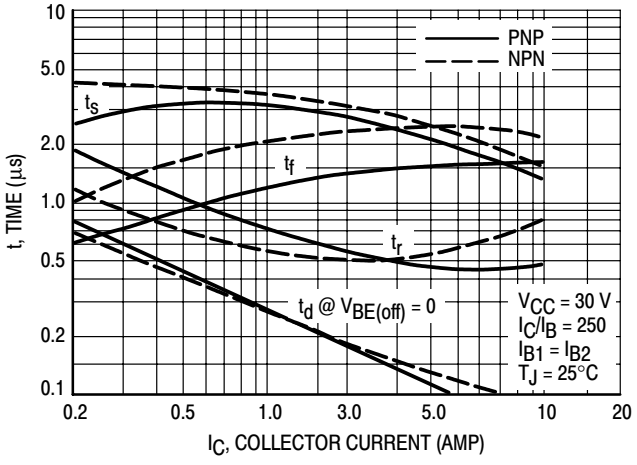
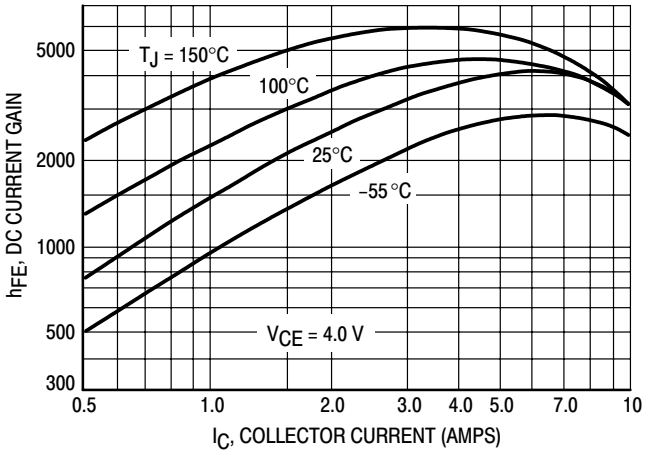


Figure 5. Switching Times

TYPICAL CHARACTERISTICS

NPN
TIP140, TIP141, TIP142



PNP
TIP145, TIP146, TIP147

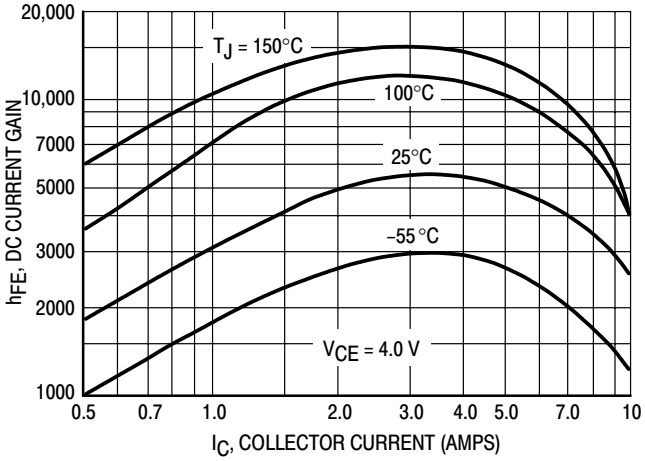
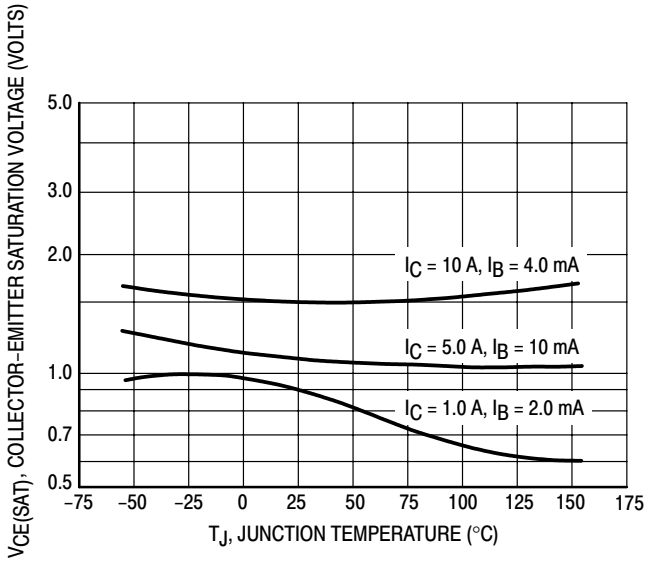


Figure 6. DC Current Gain versus Collector Current



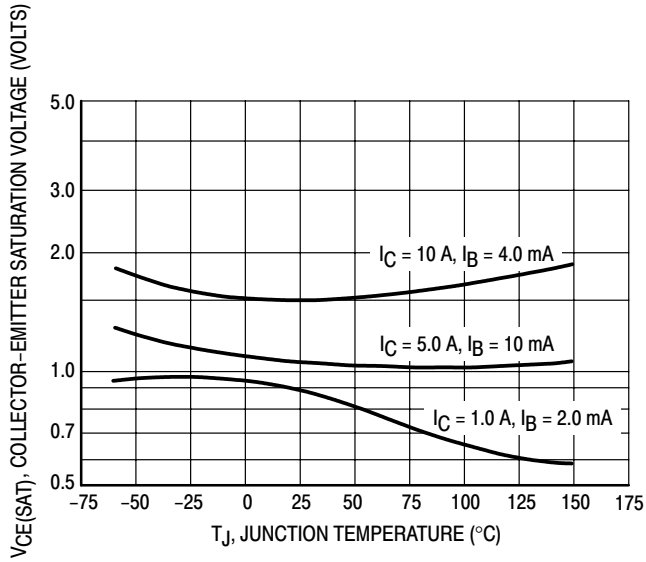
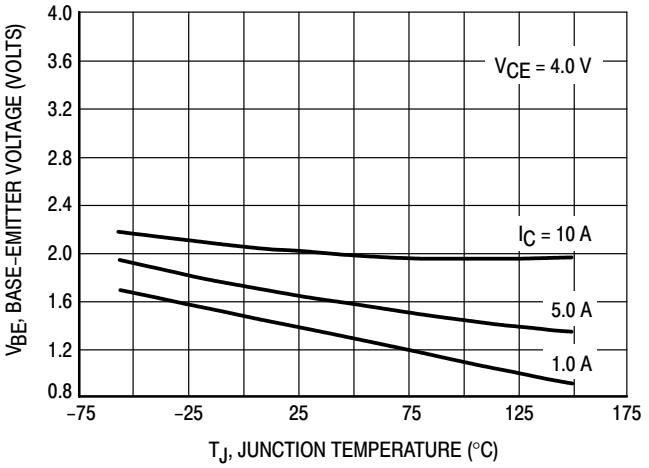


Figure 7. Collector−Emitter Saturation Voltage



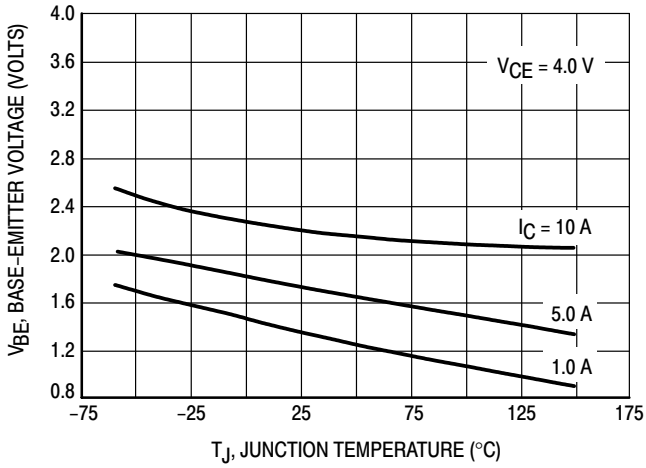


Figure 8. Base−Emitter Voltage

ACTIVE−REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

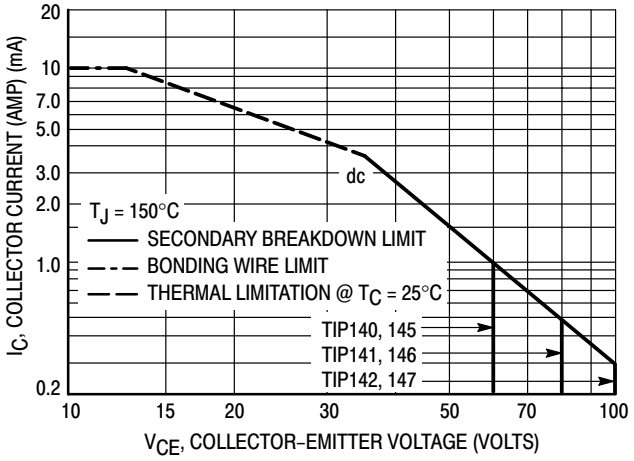


Figure 9. Active−Region Safe Operating Area

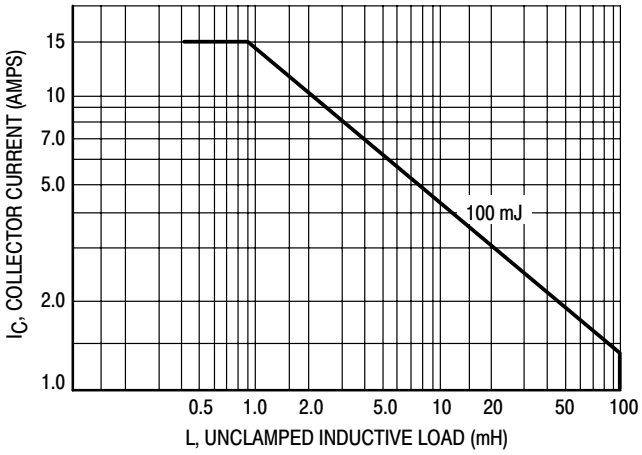
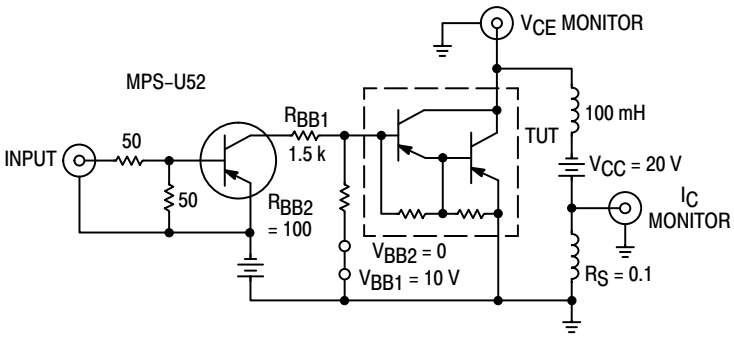
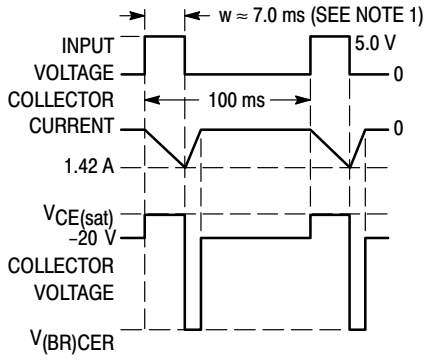


Figure 10. Unclamped Inductive Load



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE 1: Input pulse width is increased until I_{CM} = 1.42 A.
NOTE 2: For NPN test circuit reverse polarities.

Figure 11. Inductive Load

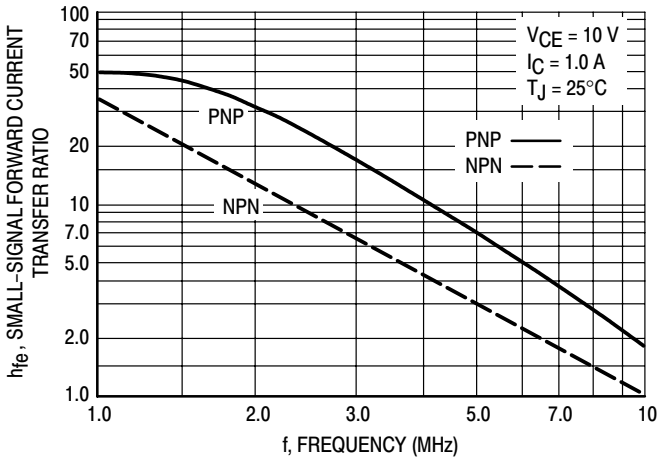


Figure 12. Magnitude of Common Emitter Small−Signal Short−Circuit Forward Current Transfer Ratio

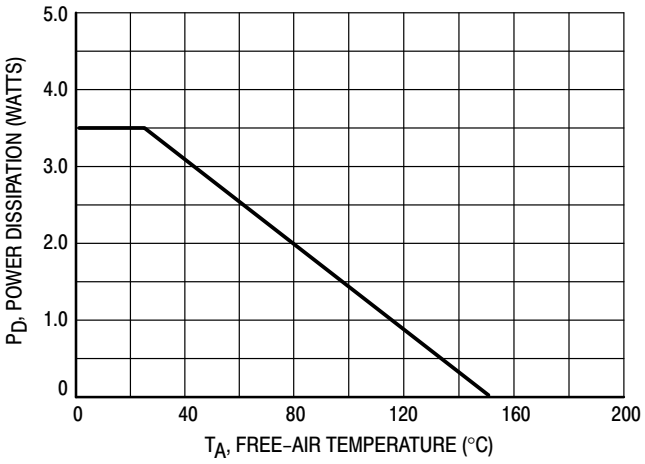


Figure 13. Free−Air Temperature Power Derating

TIP29, A, B, C (NPN), TIP30, A, B, C (PNP)

Complementary Silicon Plastic Power Transistors

. . . designed for use in general purpose amplifier and switching applications. Compact TO−220 AB package.

MAXIMUM RATINGS

Rating	Symbol	TIP29 TIP30	TIP29A TIP30A	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector−Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector−Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter−Base Voltage	V_{EB}	5.0				Vdc
Collector Current Continuous Peak	I_C	1.0 3.0				Adc
Base Current	I_B	0.4				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24				Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016				Watts W/°C
Unclamped Inductive Load Energy (Note 1)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	4.167	°C/W

1. This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F = 10 Hz.

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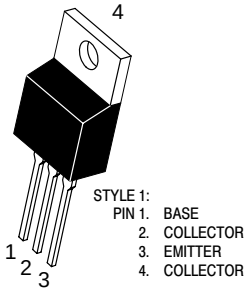
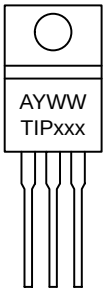
1 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 40, 60, 80−100 VOLTS 30 WATTS



TO−220AB
CASE 221A−09
STYLE 1

MARKING DIAGRAM



xxx = Specific Device Code:
29, 29A, 29B, 29C,
30, 30A, 30B, 30C
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 778 of this data sheet.

Publication Order Number:

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0) (Note 2)		$V_{CEO(sus)}$			Vdc
	TIP29, TIP30		40	−	
	TIP29A, TIP30A		60	−	
	TIP29B, TIP30B		80	−	
	TIP29C, TIP30C		100	−	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP29, TIP29A, TIP30, TIP30A		−	0.3	
(V_{CE} = 60 Vdc, I_B = 0)	TIP29B, TIP29C, TIP30B, TIP30C		−	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP29, TIP30		−	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP29A, TIP30A		−	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP29B, TIP30B		−	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP29C, TIP30C		−	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	40	−	−
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			15	75	
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$	−	0.7	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	−	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (Note 3) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	−	MHz
Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	−	−

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. $f_T = |h_{fe}| \bullet f_{test}$.

ORDERING INFORMATION

Device	Package	Shipping
TIP29	TO−220AB	50 Units/Rail
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TIP29B		
TIP29C		
TIP30		
TIP30A		
TIP30B		
TIP30C		

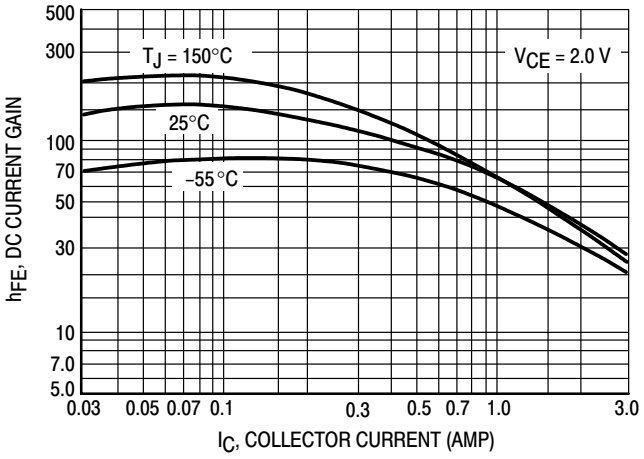


Figure 14. DC Current Gain

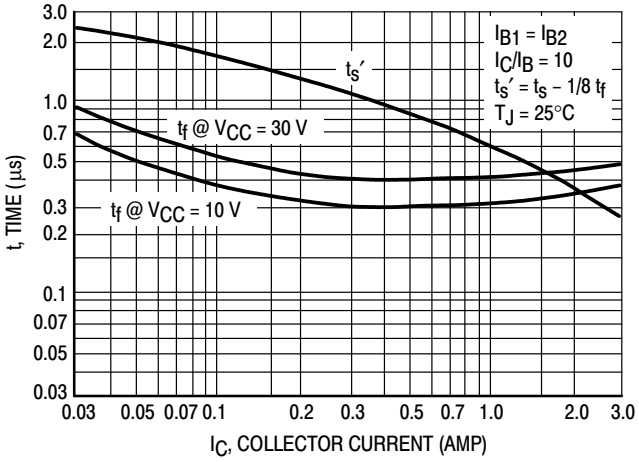


Figure 15. Turn−Off Time

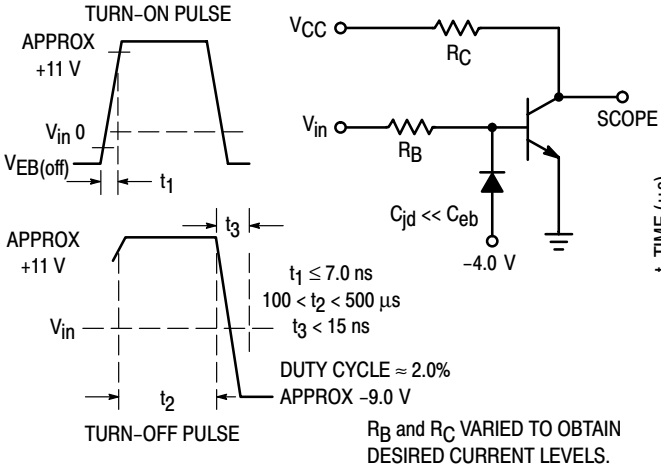


Figure 16. Switching Time Equivalent Circuit

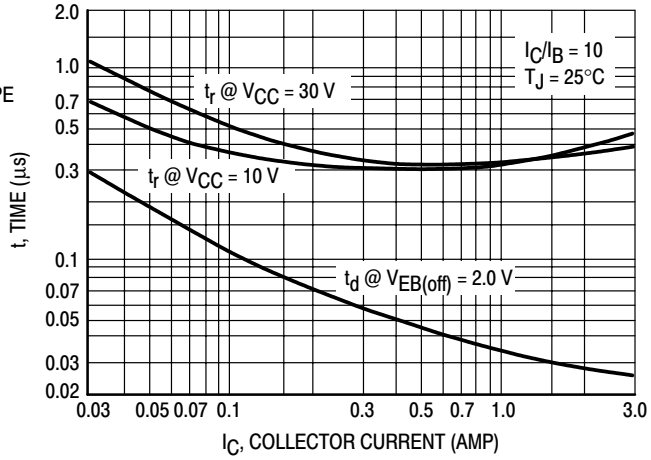


Figure 17. Turn−On Time

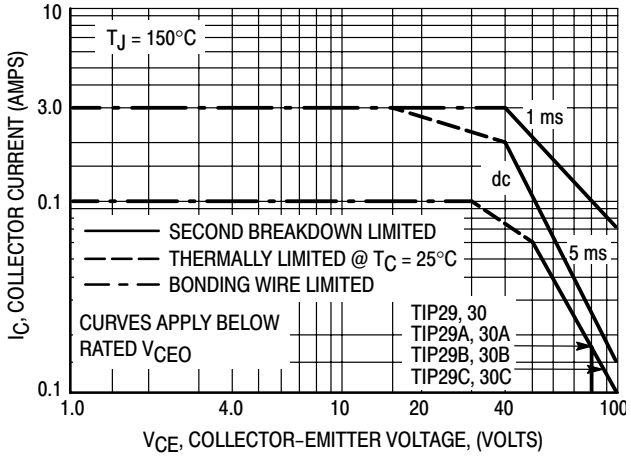


Figure 18. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 18 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

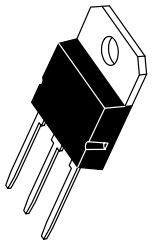
Complementary Silicon Power Transistors

. . . designed for general−purpose switching and amplifier applications.

- DC Current Gain —
  h_{FE} = 20−70 @ I_C
  = 4.0 Adc
- Collector−Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C
  = 4.0 Adc
- Excellent Safe Operating Area

NPN
TIP3055
PNP
TIP2955

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
90 WATTS



CASE 340D−02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Emitter Voltage	V_{CER}	70	Vdc
Collector−Base Voltage	V_{CB}	100	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	1 5	Adc
Base Current	I_B	7.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.72	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	°C/W

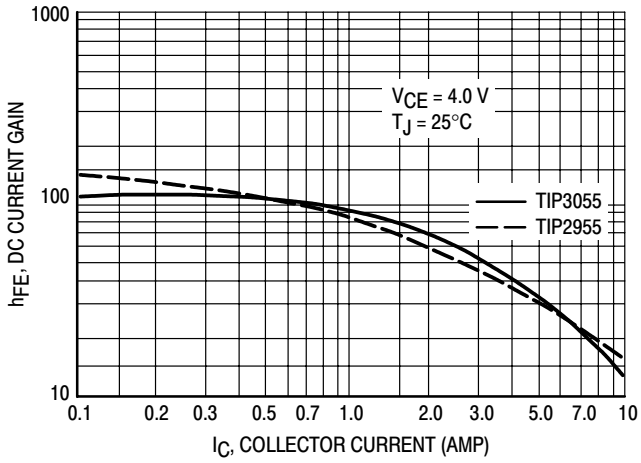


Figure 1. DC Current Gain

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, R_{BE} = 100 Ohms)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 —	—
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 3.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 30 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
Small−Signal Current Gain (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

NOTE: For additional design curves, refer to electrical characteristics curves of 2N3055.

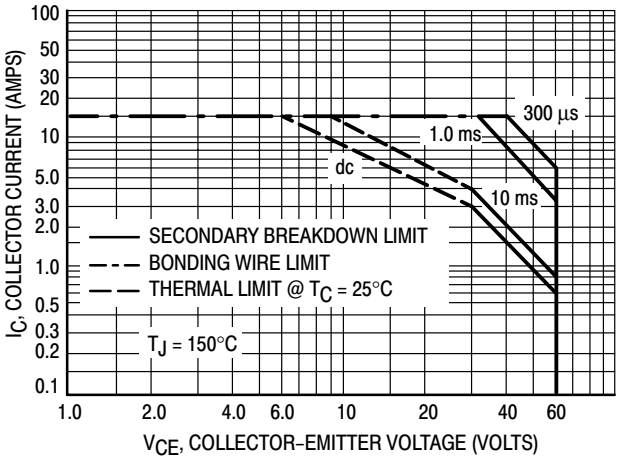


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

TIP31, TIP31A, TIP31B, TIP31C, (NPN), TIP32, TIP32A, TIP32B, TIP32C, (PNP)

Complementary Silicon Plastic Power Transistors

Designed for use in general purpose amplifier and switching applications.

- Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector−Emitter Sustaining Voltage −
  $V_{CEO(sus)}$ = 40 Vdc (Min) − TIP31, TIP32
  = 60 Vdc (Min) − TIP31A, TIP32A
  = 80 Vdc (Min) − TIP31B, TIP32B
  = 100 Vdc (Min) − TIP31C, TIP32C
- High Current Gain − Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO−220 AB Package

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	V_{CEO}	40 60 80 100	Vdc
Collector−Base Voltage TIP31, TIP32 TIP31A, TIP32A TIP31B, TIP32B TIP31C, TIP32C	V_{CB}	40 60 80 100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current Continuous Peak	I_C	3.0 5.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 0.32	 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 Watts W/°C
Unclamped Inductive Load Energy (Note 1)	E	32	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

1. I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω..

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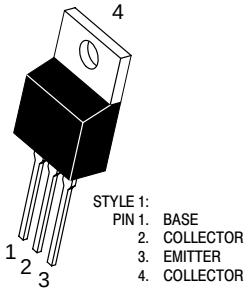
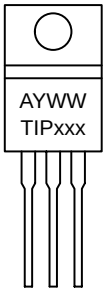
3 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 40−60−80−100 VOLTS 40 WATTS



TO−220AB
CASE 221A−09
STYLE 1

MARKING DIAGRAM



xxx = Specific Device Code:
31, 31A, 31B, 31C, 32, 32A, 32B, 32C
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 787 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2)	TIP31, TIP32	$V_{CEO(sus)}$	40	−	Vdc
(I_C = 30 mAdc, I_B = 0)	TIP31A, TIP32A		60	−	
	TIP31B, TIP32B		80	−	
	TIP31C, TIP32C		100	−	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	TIP31, TIP32, TIP31A, TIP32A	I_{CEO}	−	0.3	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C, TIP32B, TIP32C		−	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP31, TIP32		−	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		−	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		−	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		−	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	25	−	−
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	−	1.2	Vdc
Base−Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	−	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	−	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	−	−

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

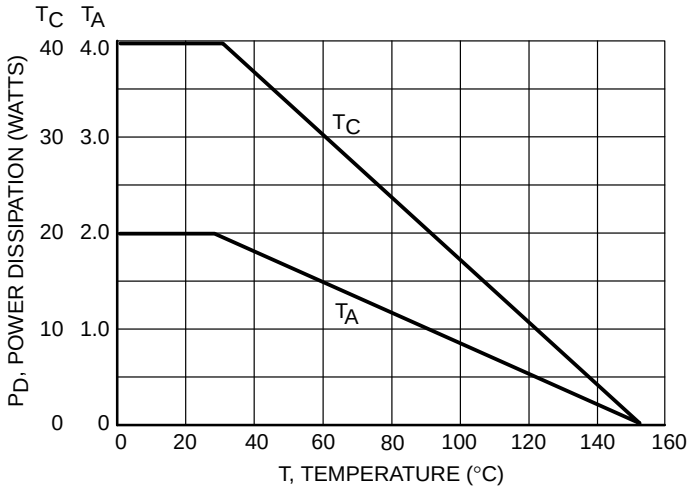
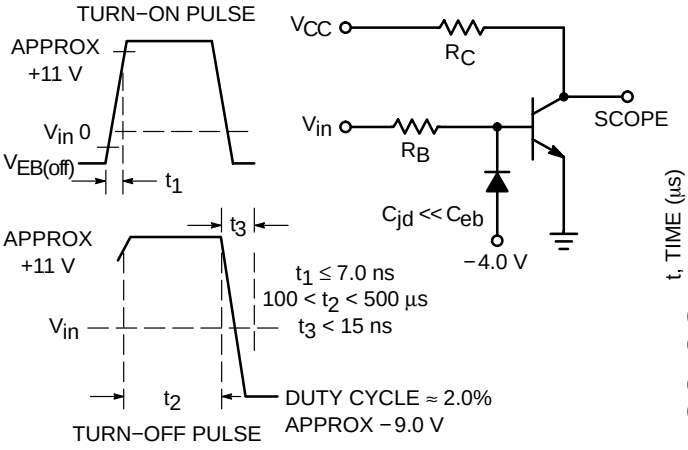


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.

Figure 2. Switching Time Equivalent Circuit

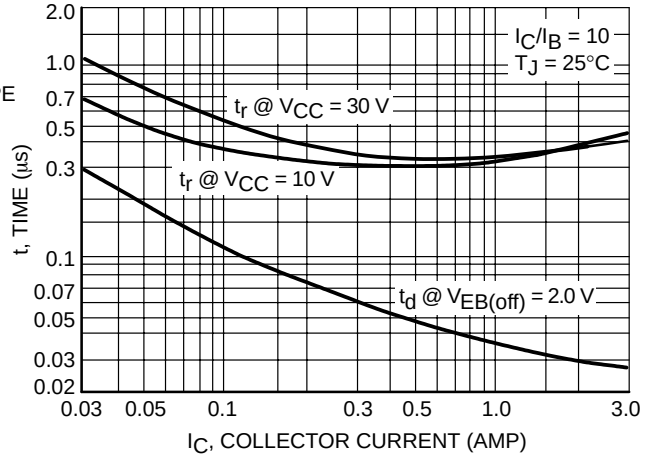


Figure 3. Turn−On Time

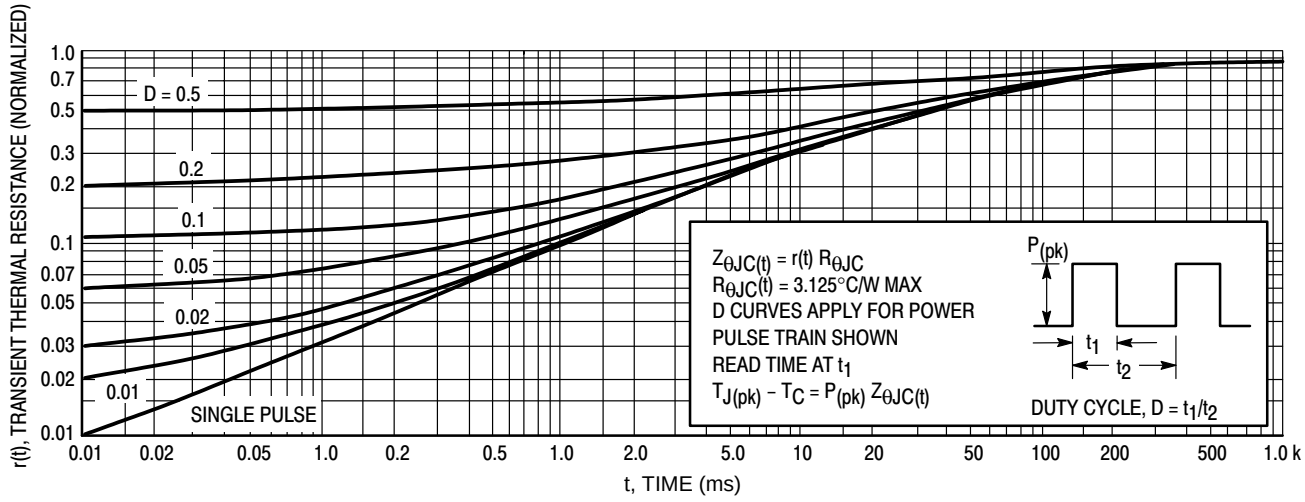


Figure 4. Thermal Response

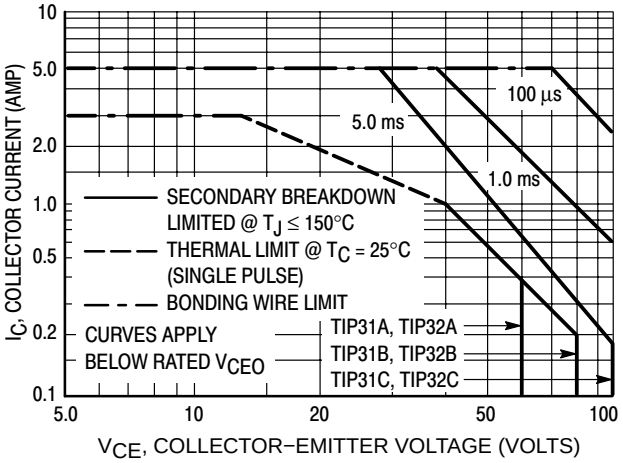


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

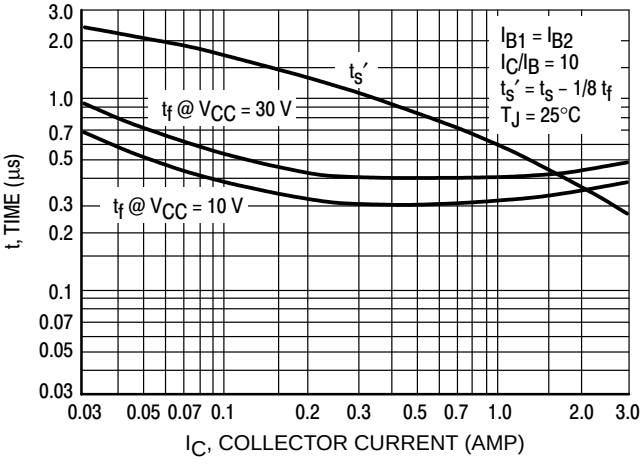


Figure 6. Turn−Off Time

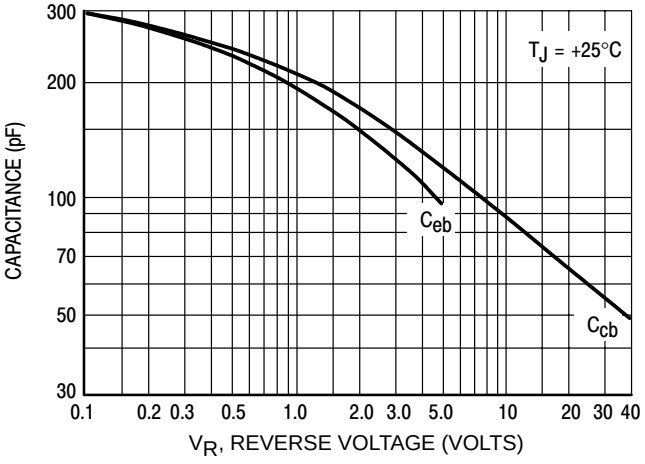


Figure 7. Capacitance

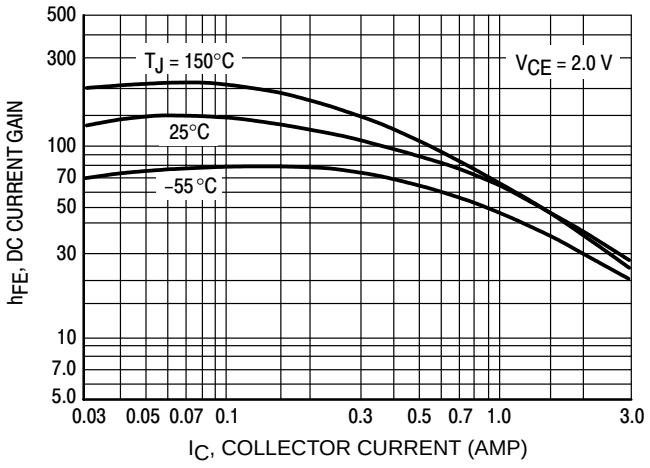


Figure 8. DC Current Gain

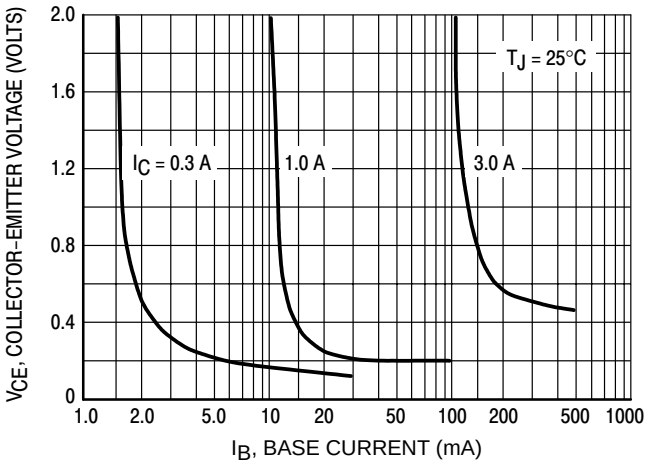


Figure 9. Collector Saturation Region

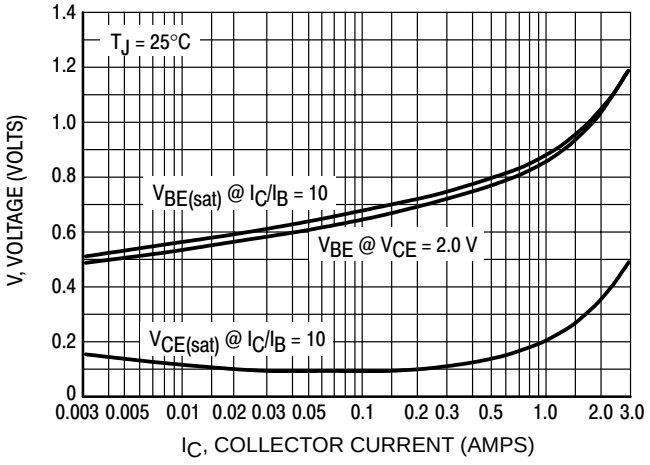


Figure 10. “On” Voltages

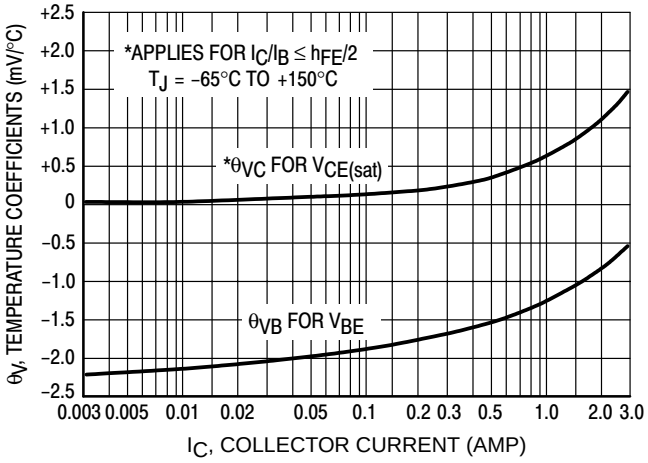


Figure 11. Temperature Coefficients

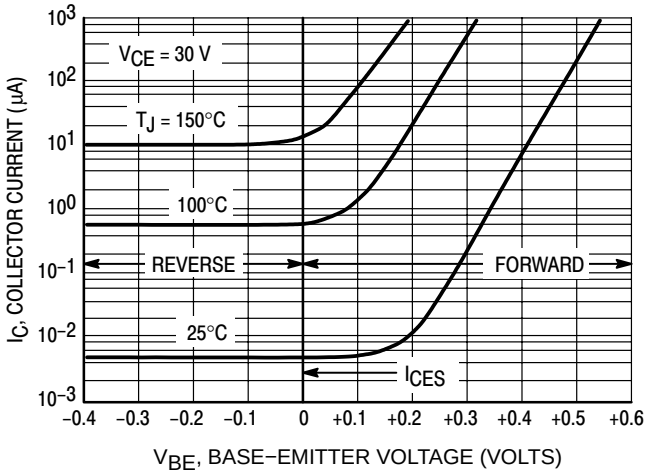


Figure 12. Collector Cut−Off Region

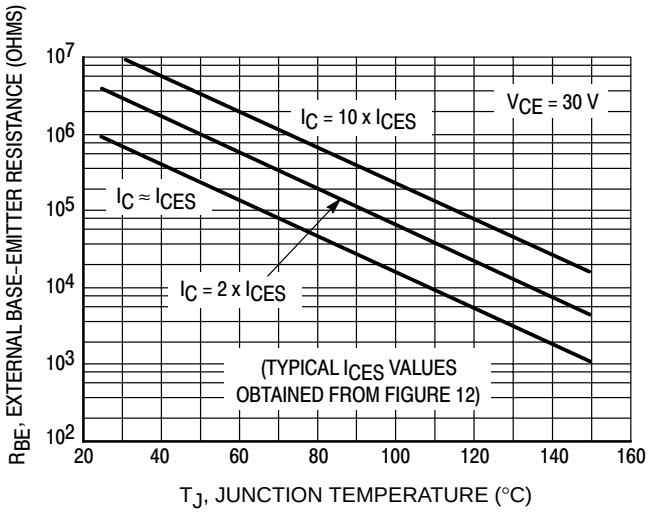


Figure 13. Effects of Base−Emitter Resistance

ORDERING INFORMATION

Device	Package	Shipping
TIP31	TO−220AB	50 Units/Rail
TIP31A	TO−220AB	50 Units/Rail
TIP31B	TO−220AB	50 Units/Rail
TIP31C	TO−220AB	50 Units/Rail
TIP32	TO−220AB	50 Units/Rail
TIP32A	TO−220AB	50 Units/Rail
TIP32B	TO−220AB	50 Units/Rail
TIP32C	TO−220AB	50 Units/Rail

TIP33A, TIP33C

NPN High-Power Transistors

. . . for general−purpose power amplifier and switching applications.

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V−0 @ 1/8”

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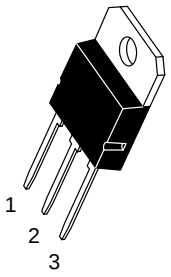
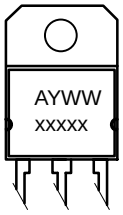
10 A, 60 & 100 V, 80 W
NPN SILICON
POWER TRANSISTORS



TO−218
CASE 340D
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	TIP33A TIP33C	V_{CEO}	60 100	Vdc
Collector−Base Voltage	TIP33A TIP33C	V_{CBO}	60 100	Vdc
Emitter−Base Voltage		V_{EBO}	5.0	Vdc
Collector Current − Continuous Peak (Note 1)		I_C	10 15	Adc Apk
Base Current − Continuous		I_B	3.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	80 0.64	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35.7	°C/W

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ORDERING INFORMATION

Device	Package	Shipping
TIP33A	TO−218	30 Units / Rail
TIP33C	TO−218	30 Units / Rail

Publication Order Number:

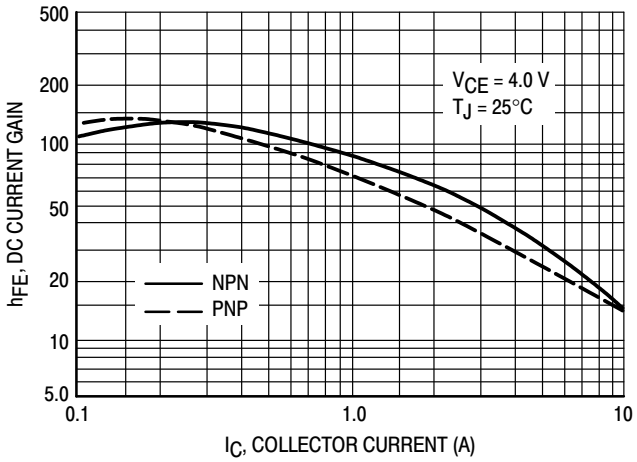


Figure 1. DC Current Gain

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mA, I_B = 0)	TIP33A TIP33C	$V_{CEO(sus)}$	60 100	— —	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) (V_{CE} = 60 V, I_B = 0)	 TIP33A TIP33C	I_{CEO}	—	0.7	mA
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.4	mA
Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (Note 1)					
DC Current Gain (I_C = 1.0 A, V_{CE} = 4.0 V) (I_C = 3.0 A, V_{CE} = 4.0 V)		h_{FE}	 40 20	 — 100	—
Collector−Emitter Saturation Voltage (I_C = 3.0 A, I_B = 0.3 A) (I_C = 10 A, I_B = 2.5 A)		$V_{CE(sat)}$	 — —	 1.0 4.0	Vdc
Base−Emitter On Voltage (I_C = 3.0 A, V_{CE} = 4.0 V) (I_C = 10 A, V_{CE} = 4.0 V)		$V_{BE(on)}$	 — —	 1.6 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	20	—	—
Current−Gain — Bandwidth Product (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

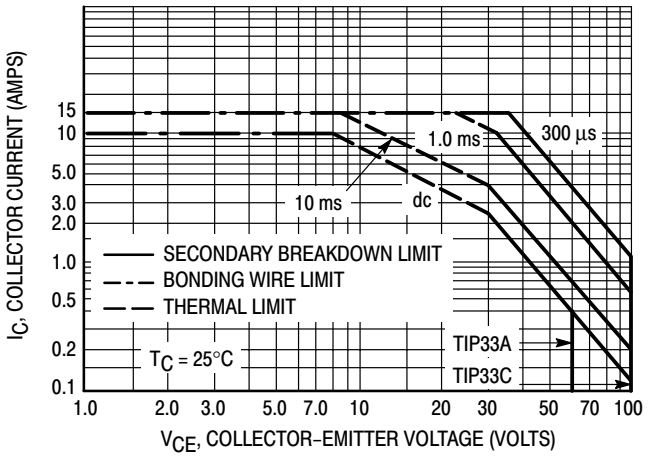


Figure 2. Maximum Rated Forward Bias Safe Operating Area

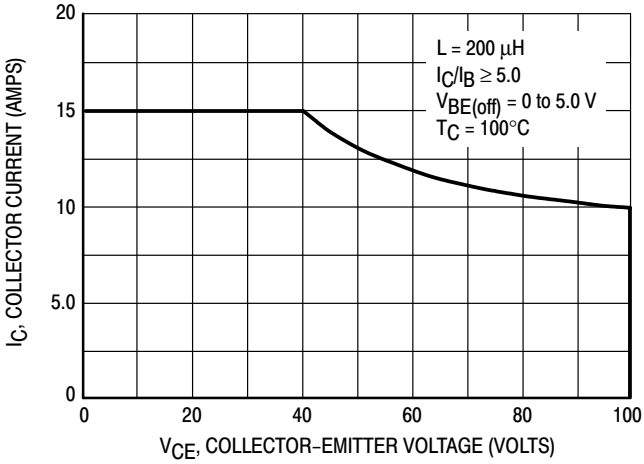


Figure 3. Maximum Rated Forward Bias Safe Operating Area

FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for $T_C > 25°C$.

REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn−off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

Complementary Silicon High-Power Transistors

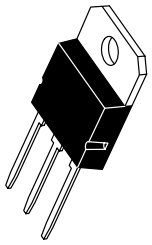
. . . for general−purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current —
  I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent DC Gain —
  h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product —
  $|h_{fe}|$ = 3.0 min @ I_C
  = 1.0 A, f = 1.0 MHz

NPN
TIP35A
TIP35B*
TIP35C*
PNP
TIP36A
TIP36B*
TIP36C*

*ON Semiconductor Preferred Device

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60−100 VOLTS 125 WATTS



CASE 340D−02 TO−218AC

MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector−Emitter Voltage	V_{CEO}	60 V	80 V	100 V	Vdc
Collector−Base Voltage	V_{CB}	60 V	80 V	100 V	Vdc
Emitter−Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	25 40			Adc
Base Current — Continuous	I_B	5.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C
Unclamped Inductive Load	E_{SB}	90			mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Junction−To−Free−Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

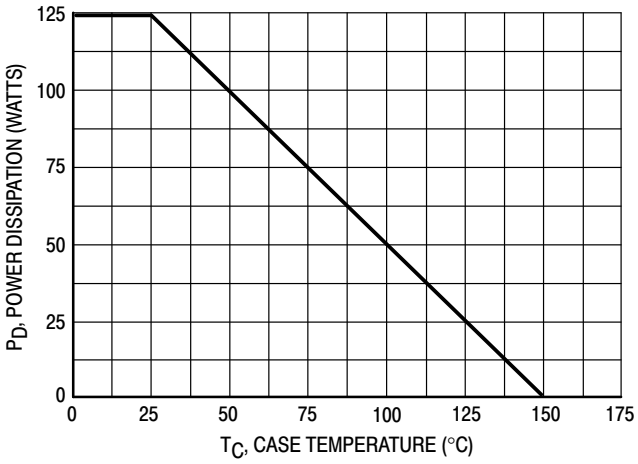


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	TIP35A, TIP36A TIP35B, TIP36B TIP35C, TIP36C	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) (V_{CE} = 60 V, I_B = 0)	 TIP35A, TIP36A TIP35B, TIP35C, TIP36B, TIP36C	I_{CEO}	 — —	 1.0 1.0	mA
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.7	mA
Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.5 A, V_{CE} = 4.0 V) (I_C = 15 A, V_{CE} = 4.0 V)		h_{FE}	 25 15	 — 75	—
Collector−Emitter Saturation Voltage (I_C = 15 A, I_B = 1.5 A) (I_C = 25 A, I_B = 5.0 A)		$V_{CE(sat)}$	 — —	 1.8 4.0	Vdc
Base−Emitter On Voltage (I_C = 15 A, V_{CE} = 4.0 V) (I_C = 25 A, V_{CE} = 4.0 V)		$V_{BE(on)}$	 — —	 2.0 4.0	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	25	—	—
Current−Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

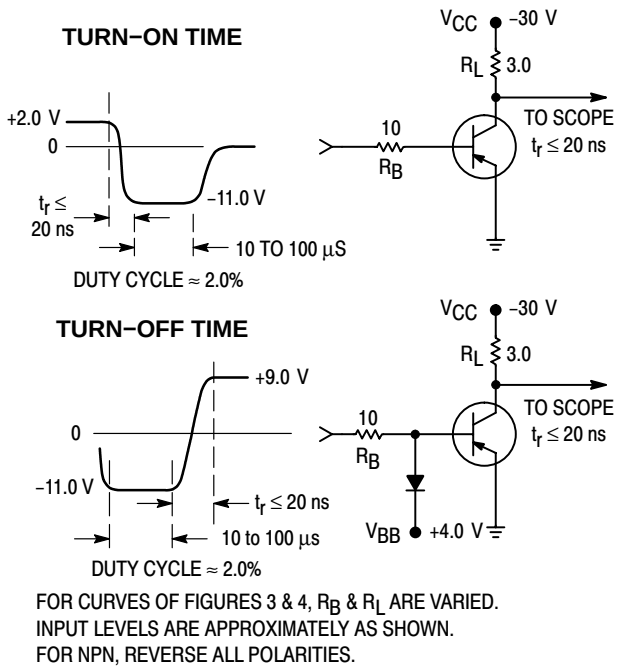


Figure 2. Switching Time Equivalent Test Circuits

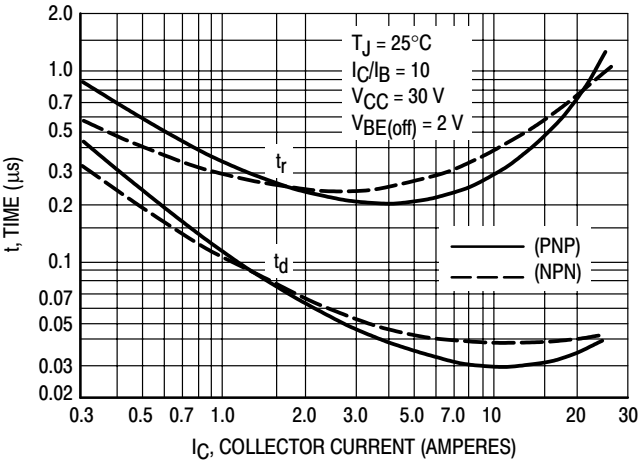


Figure 3. Turn−On Time

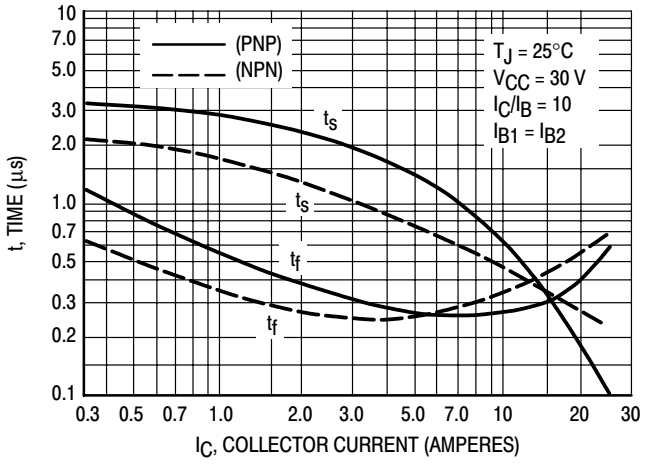


Figure 4. Turn−Off Time

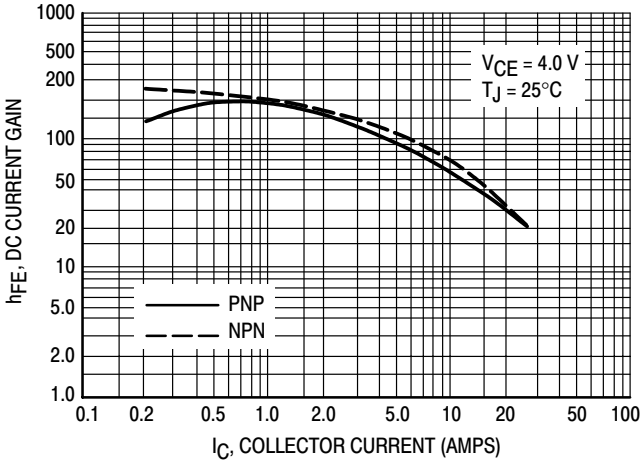


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

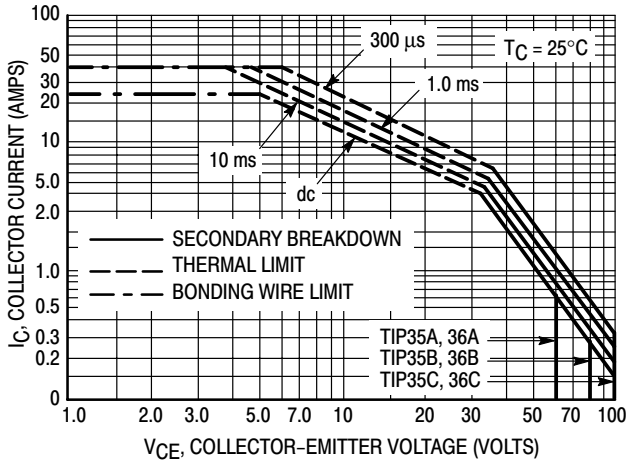


Figure 6. Maximum Rated Forward Bias Safe Operating Area

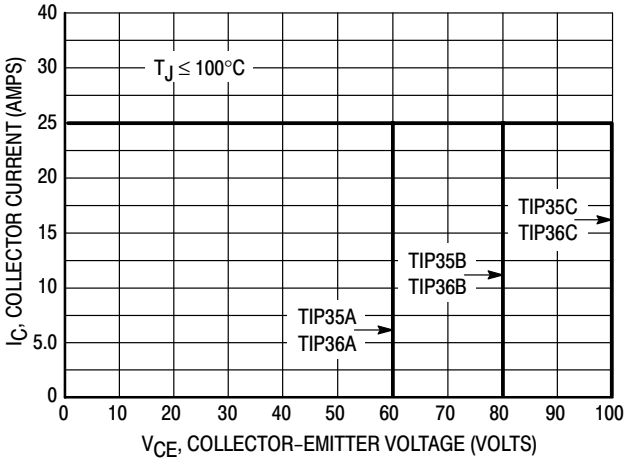
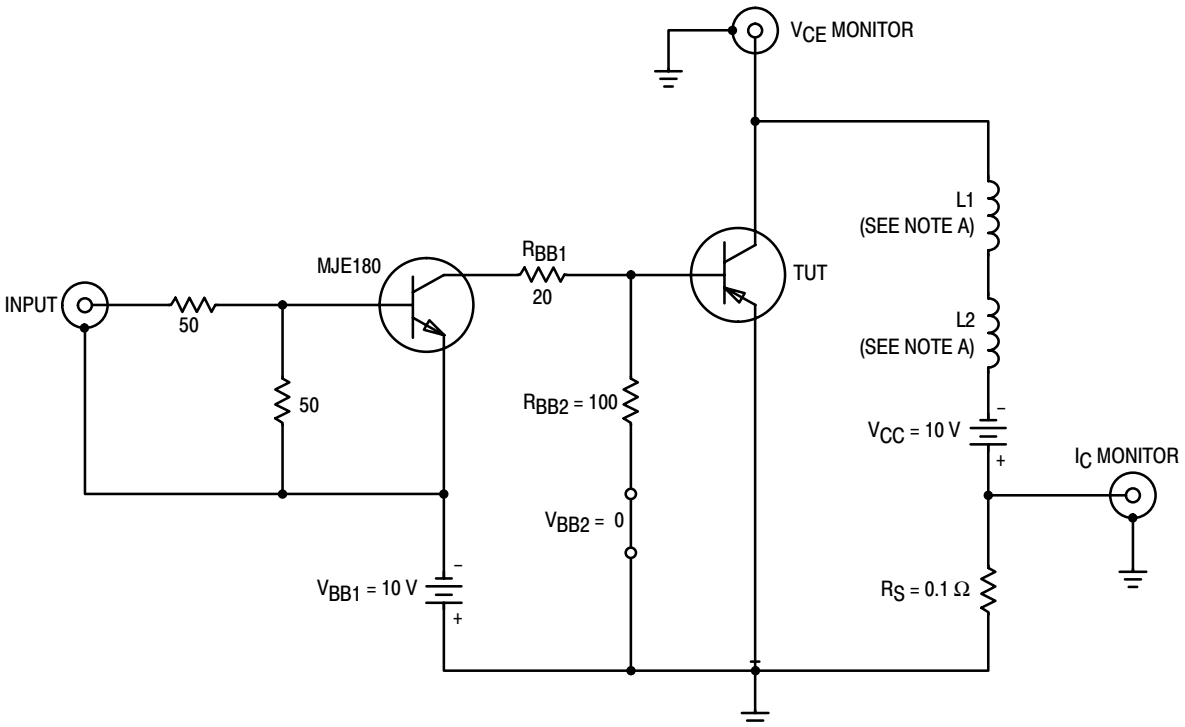
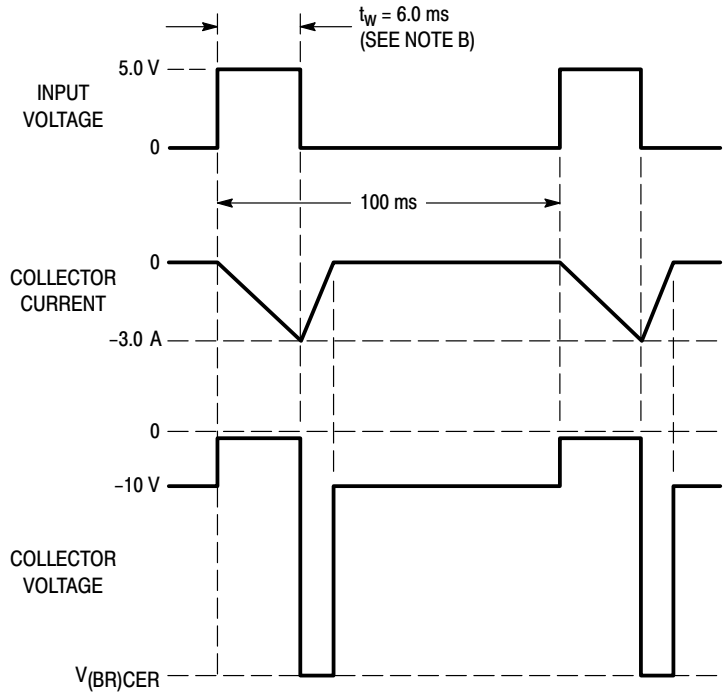


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C−2688, or equivalent.
B. Input pulse width is increased until I_{CM} = −3.0 A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

(NPN) TIP41, TIP41A, TIP41B, TIP41C
(PNP) TIP42, TIP42A, TIP42B, TIP42C

Complementary Silicon Plastic Power Transistors

. . . designed for use in general purpose amplifier and switching applications.

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V−0 @ 1/8”
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V_{CEO}	40 60 80 100	Vdc
Collector−Base Voltage TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	V_{CB}	40 60 80 100	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current− Continuous Peak	I_C	6.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Unclamped Inductive Load Energy (Note 2)	E	62.5	mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	57	°C/W

2. I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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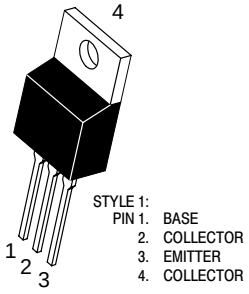
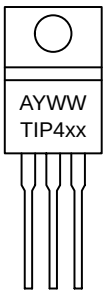
6 A
COMPLEMENTARY SILICON POWER TRANSISTORS
40 − 60 − 80 − 100 V, 65 W



TO−220AB
CASE 221A−09
STYLE 1

MARKING DIAGRAM



xx = Specific Device Code:
1, 2, 1A, 1B, 1C, 2A, 2B, 2C
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
TIP41	TO−220AB	50 Units / Rail
TIP41A	TO−220AB	50 Units / Rail
TIP41B	TO−220AB	50 Units / Rail
TIP41C	TO−220AB	50 Units / Rail
TIP41CG	TO−220AB (Pb−Free)	50 Units / Rail
TIP42	TO−220AB	50 Units / Rail
TIP42A	TO−220AB	50 Units / Rail
TIP42B	TO−220AB	50 Units / Rail
TIP42C	TO−220AB	50 Units / Rail
TIP42CG	TO−220AB (Pb−Free)	50 Units / Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 3)	TIP41, TIP42	$V_{CEO(sus)}$	40	−	Vdc
(I_C = 30 mAdc, I_B = 0)	TIP41A, TIP42A		60	−	
	TIP41B, TIP42B		80	−	
	TIP41C, TIP42C		100	−	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP41, TIP41A, TIP42, TIP42A		−	0.7	
(V_{CE} = 60 Vdc, I_B = 0)	TIP41B, TIP41C, TIP42B, TIP42C		−	0.7	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP41, TIP42		−	400	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP41A, TIP42A		−	400	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP41B, TIP42B		−	400	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41C, TIP42C		−	400	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30	−	−
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			15	75	
Collector−Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	−	1.5	Vdc
Base−Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	−	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	−	MHz
Small−Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	−	−

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

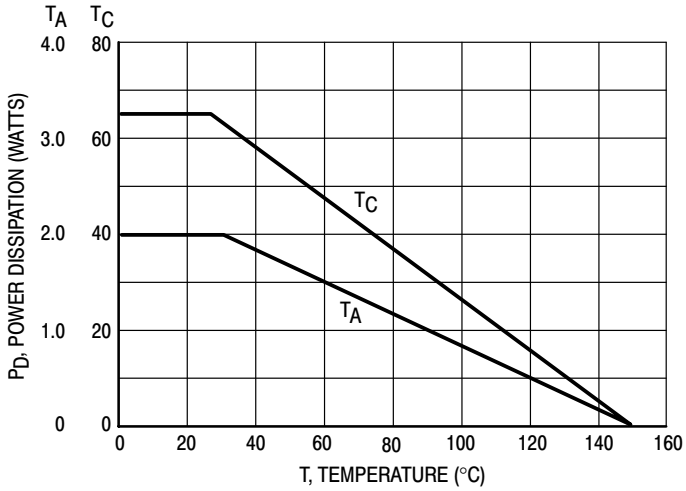
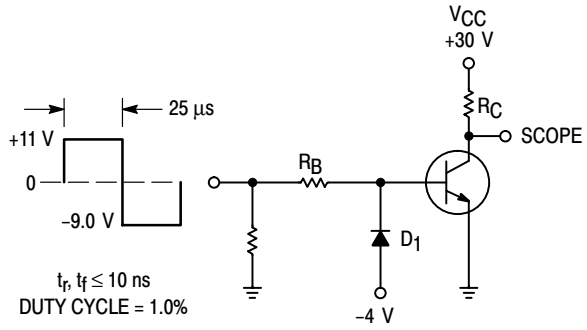


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Figure 2. Switching Time Test Circuit

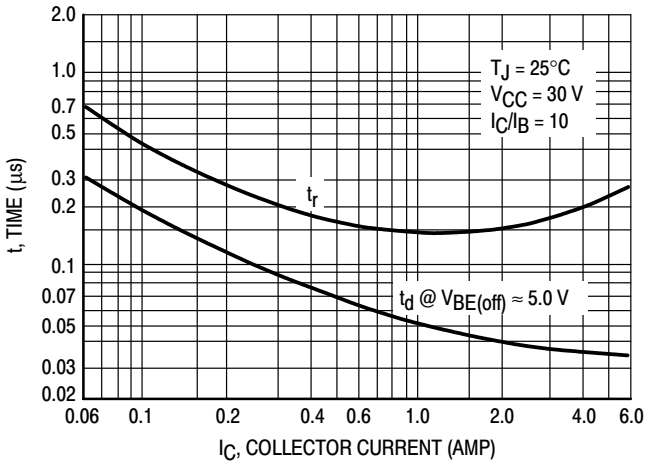


Figure 3. Turn−On Time

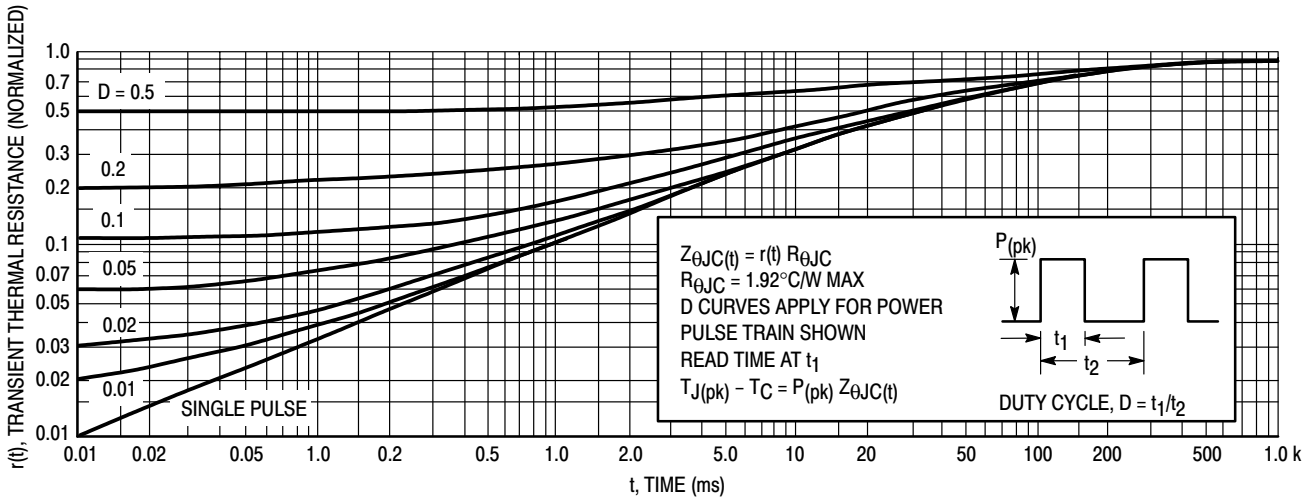


Figure 4. Thermal Response

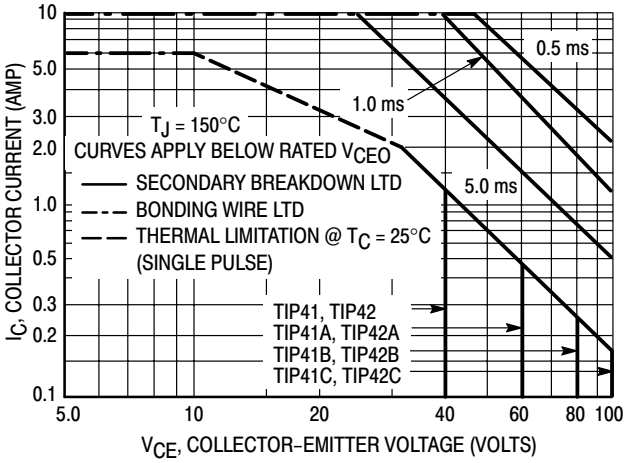


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

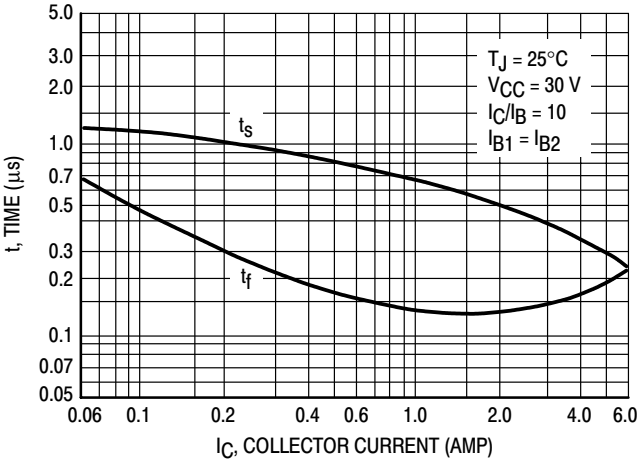


Figure 6. Turn−Off Time

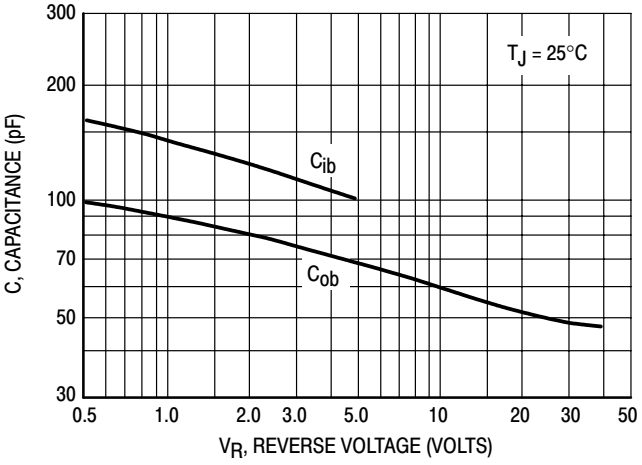


Figure 7. Capacitance

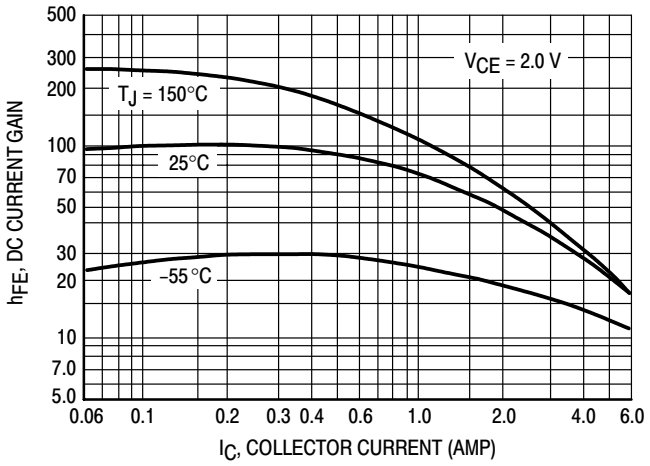


Figure 8. DC Current Gain

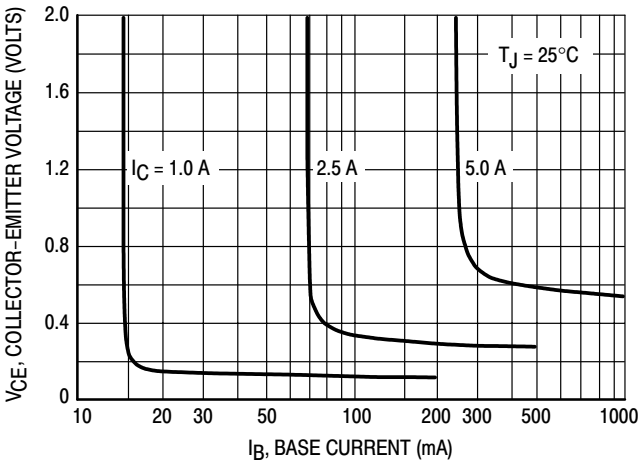


Figure 9. Collector Saturation Region

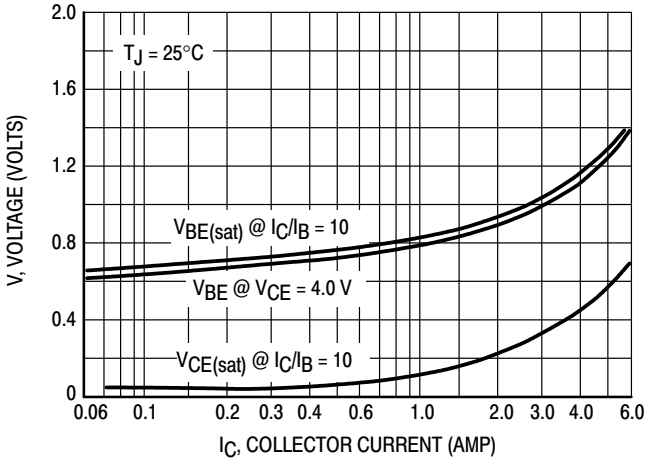


Figure 10. “On” Voltages

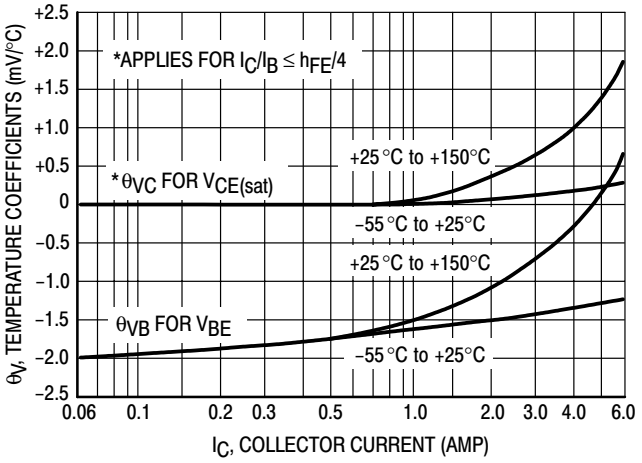


Figure 11. Temperature Coefficients

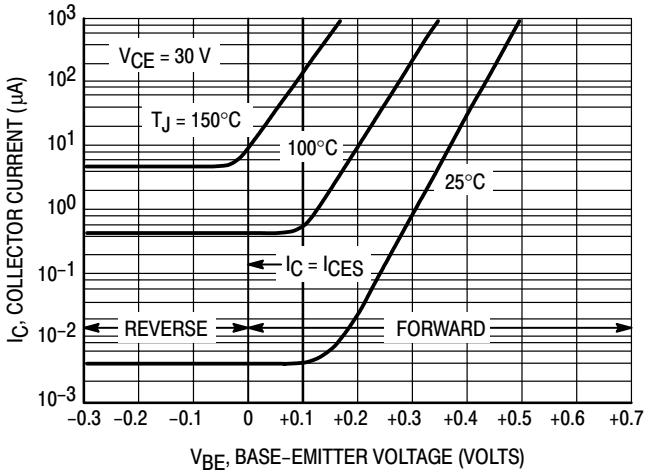


Figure 12. Collector Cut−Off Region

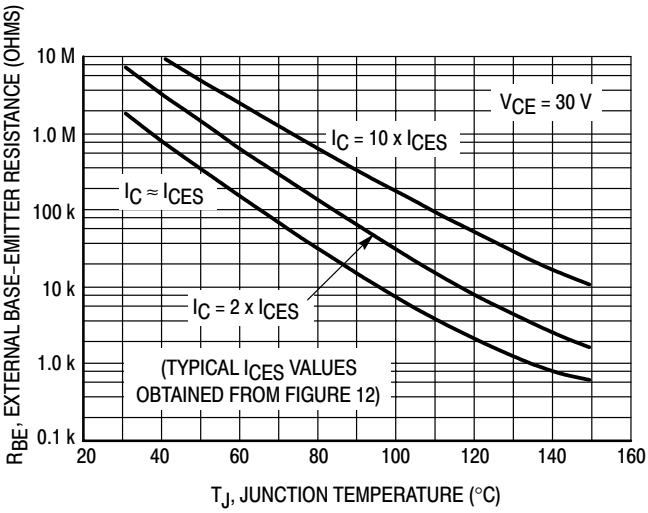


Figure 13. Effects of Base−Emitter Resistance

High Voltage NPN Silicon Power Transistors

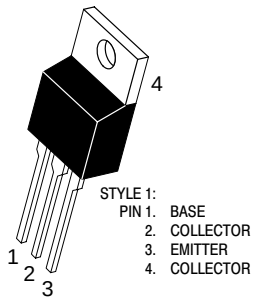
. . . designed for line operated audio output amplifier, SWITCHMODE™ power supply drivers and other switching applications.

- 250 V to 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO−220 Plastic Package

TIP47*
TIP48*
TIP50*

*ON Semiconductor Preferred Device

1.0 AMPERE
POWER TRANSISTORS
NPN SILICON
250−300−350−400 VOLTS
40 WATTS



CASE 221A−09
TO−220AB

MAXIMUM RATINGS

Rating	Symbol	TIP47	TIP48	TIP50	Unit
Collector−Emitter Voltage	V_{CEO}	250	300	400	Vdc
Collector−Base Voltage	V_{CB}	350	400	500	Vdc
Emitter−Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak	I_C		1.0 2.0		Adc
Base Current	I_B		0.6		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		40 0.32		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D		2.0 0.016		Watts W/°C
Unclamped Inducting Load Energy (See Figure 8)	E		20		mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}		−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

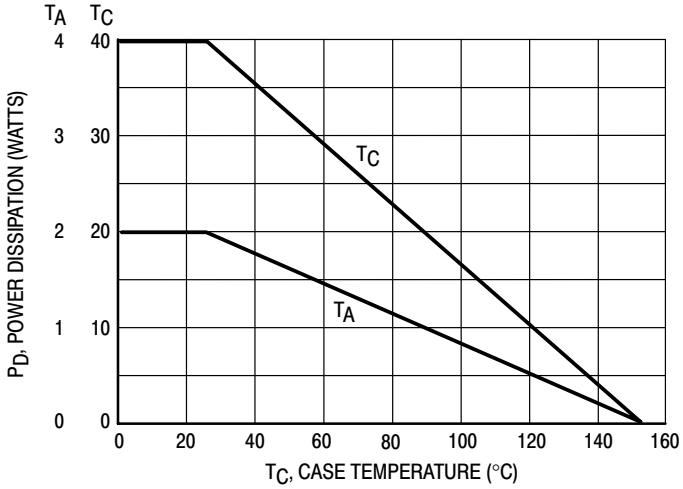


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP47 TIP48 TIP50	$V_{CEO(sus)}$	250 300 400	— — —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 TIP47 TIP48 TIP50	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 400 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	 TIP47 TIP48 TIP50	I_{CES}	 — — —	 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 —	—
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	—	MHz
Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2.0%.

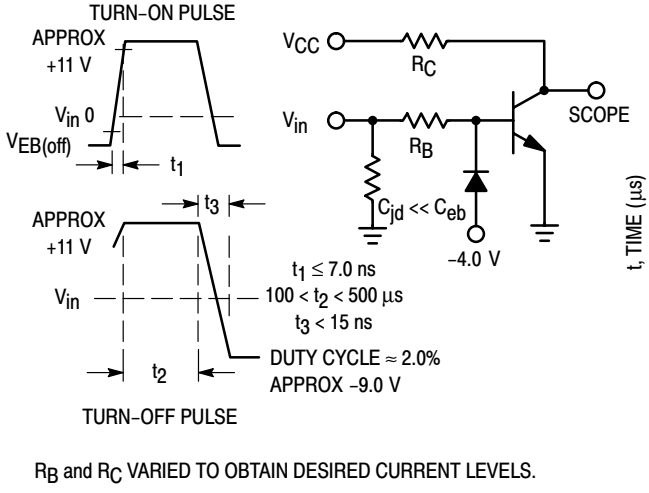


Figure 2. Switching Time Equivalent Circuit

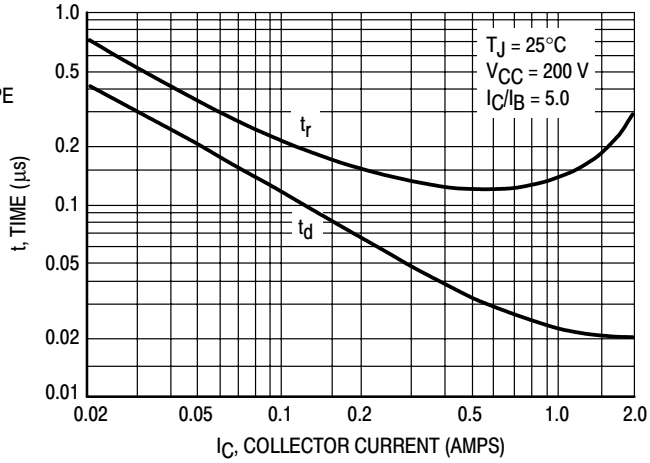


Figure 3. Turn−On Time

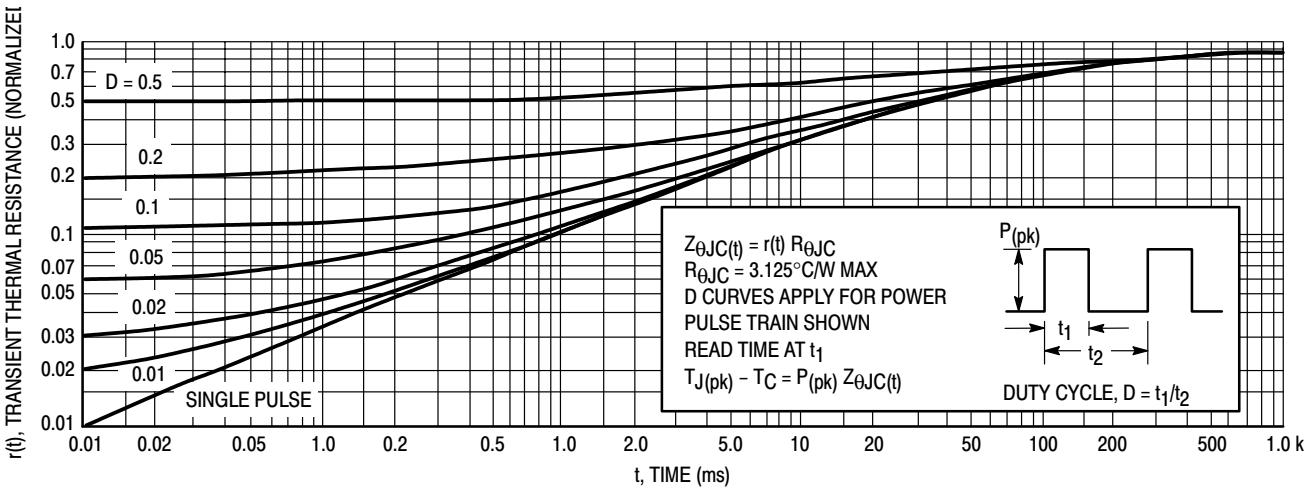


Figure 4. Thermal Response

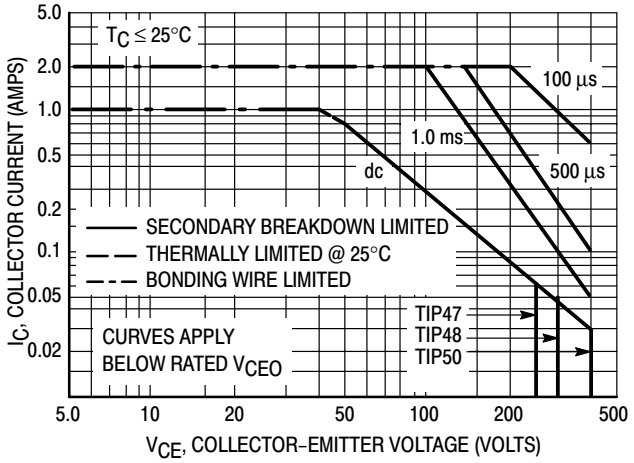


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

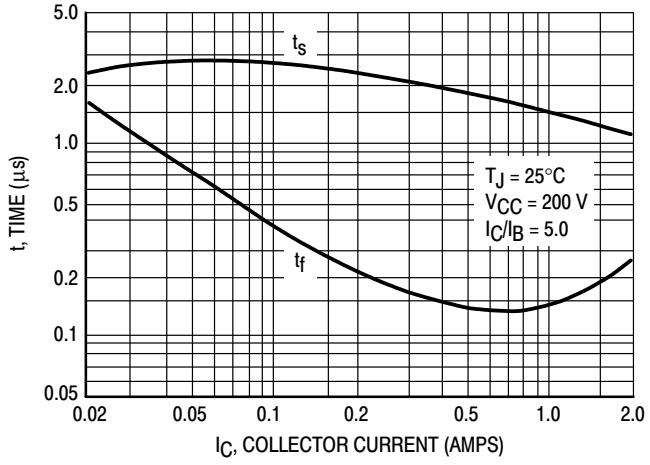


Figure 6. Turn−Off Time

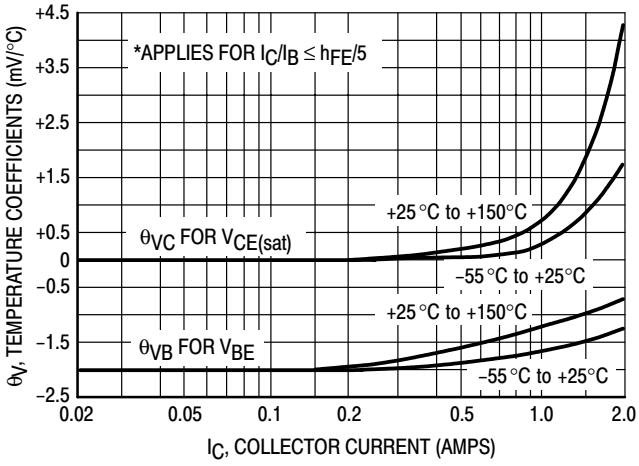
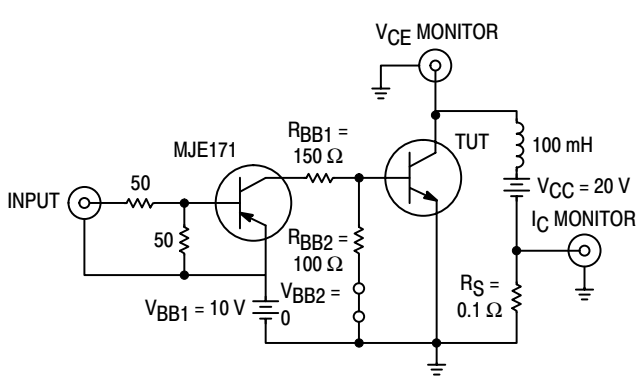
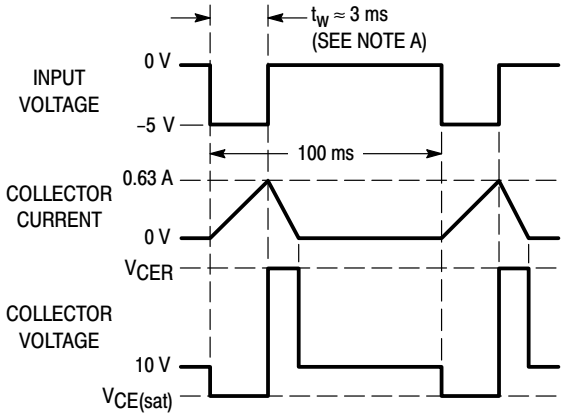


Figure 7. Temperature Coefficients





Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Figure 8. Inductive Load Switching

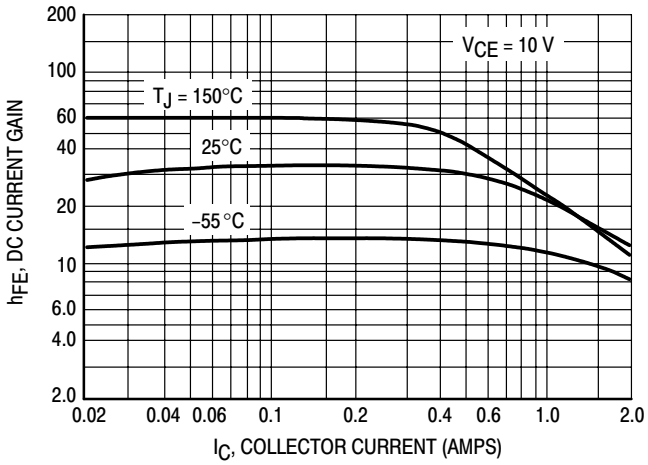


Figure 9. DC Current Gain

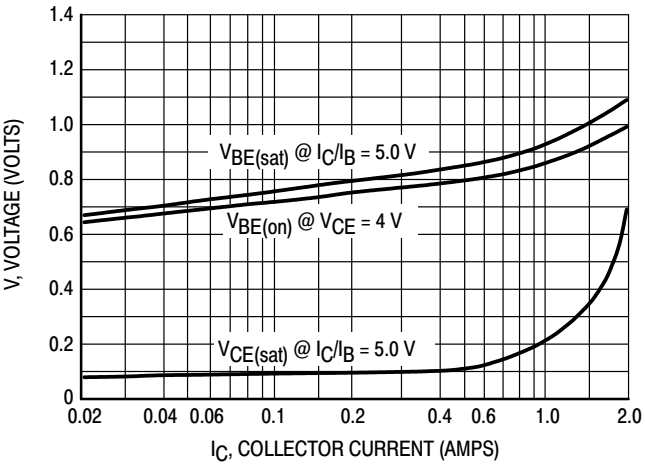


Figure 10. “On” Voltages

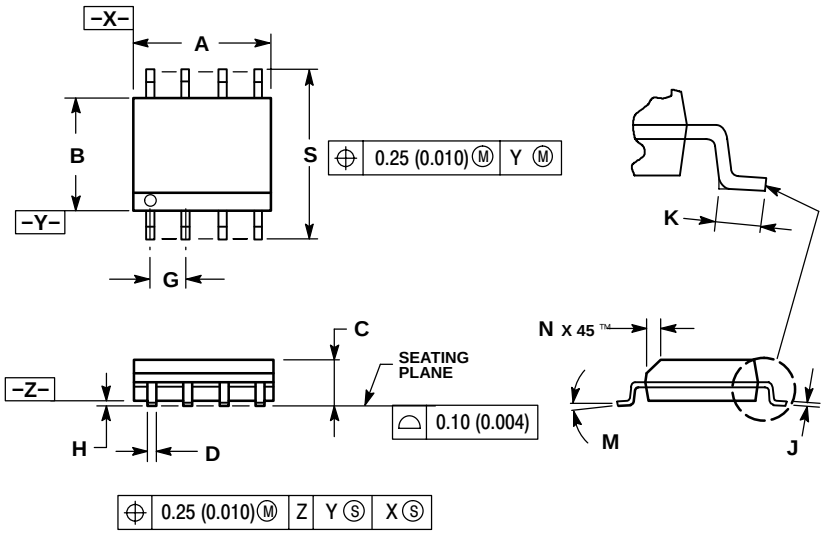
CHAPTER 3
Case Outlines and Package Dimensions

CASE OUTLINES AND PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AC

DATE 13 AUG 2004

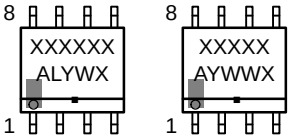
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 ™	8 ™	0 ™	8 ™
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W, WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

SOIC−8 NB
CASE 751−07
ISSUE AC

DATE 13 AUG 2004

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

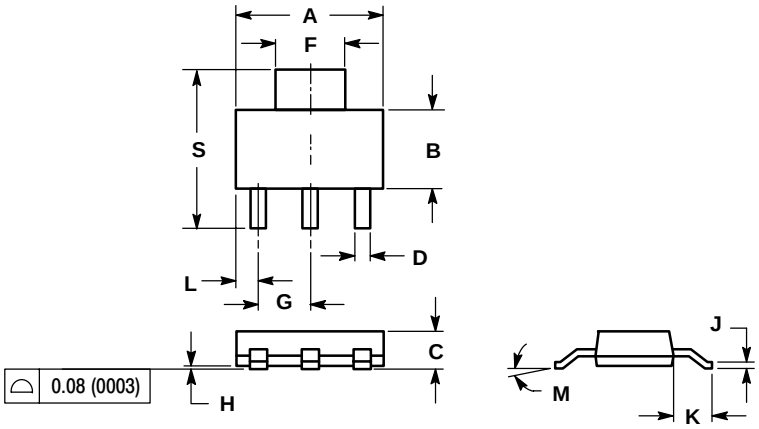
STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

SOT−223 (TO−261)
CASE 318E−04
ISSUE K

DATE 01/02/2000

SCA E



NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		I I ETERS	
DI	IN	A	IN	A
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
	0.009	0.014	0.24	0.35
	0.060	0.078	1.50	2.00
	0.033	0.041	0.85	1.05
	0 ™	10 ™	0 ™	10 ™
S	0.264	0.287	6.70	7.30

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

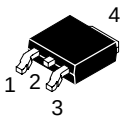
STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

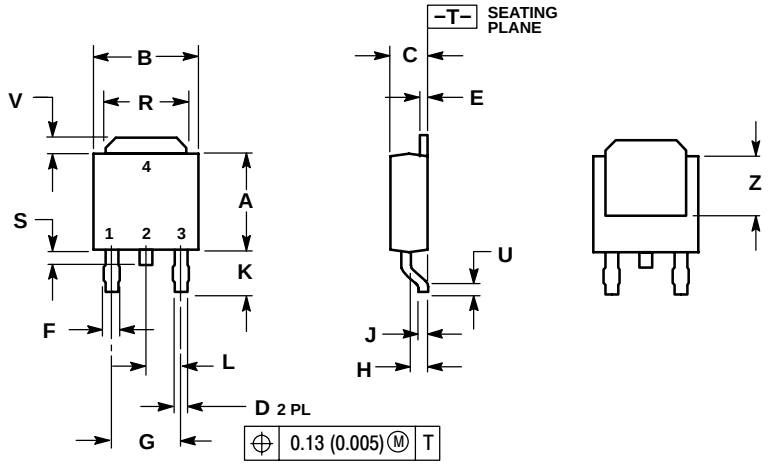
STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE O

DATE 24 SEP 2001



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

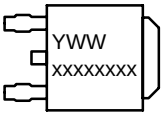
STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

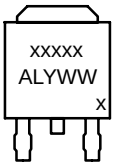
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

MARKING DIAGRAMS

Discrete

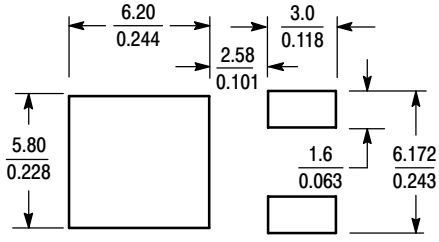


Integrated Circuits

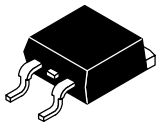


xxxxxxxxx = Device Code
A = Assembly Location
lL = Wafer Lot
Y = Year
WW = Work Week

RECOMMENDED FOOTPRINT



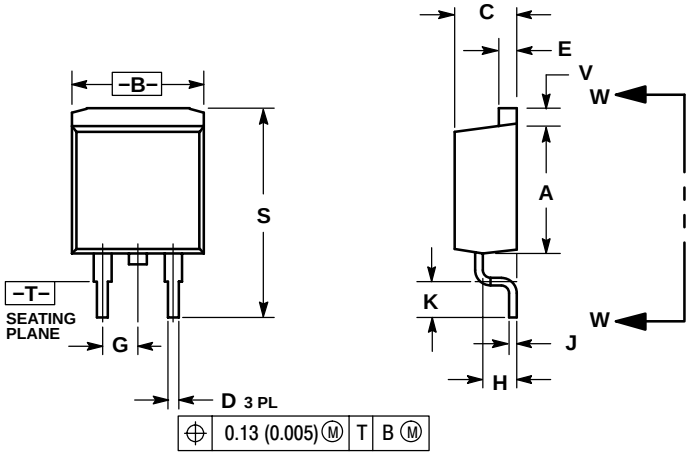
SCALE 3:1 $\frac{mm}{inches}$



SCALE 1:1

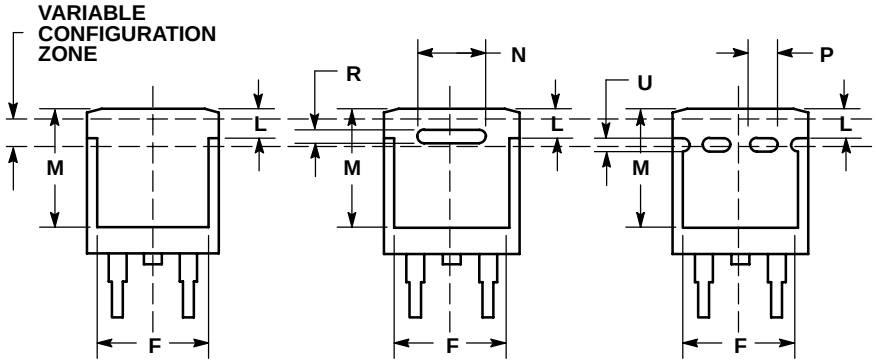
D²PAK 3
CASE 418B−04
ISSUE J

DATE 30 AUG 2004



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

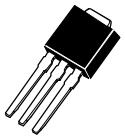
STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

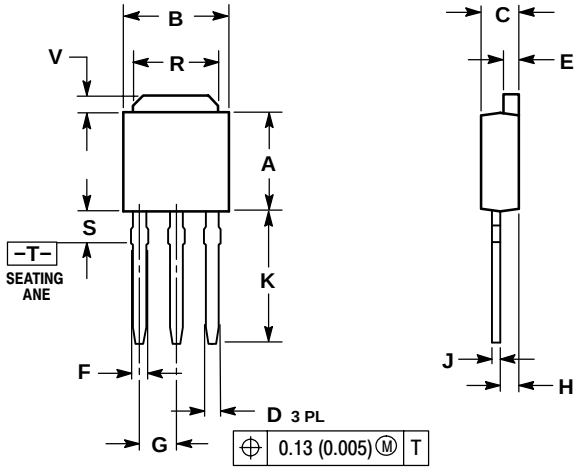
MARKING INFORMATION AND FOOTPRINT ON PAGE 2

DPAK
CASE 369−07
ISSUE M

DATE 01/02/2000



SCA E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		I I ETERS	
DI	IN	A	IN	A
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
	0.018	0.023	0.46	0.58
	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

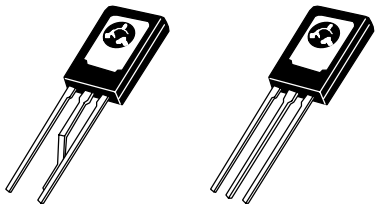
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

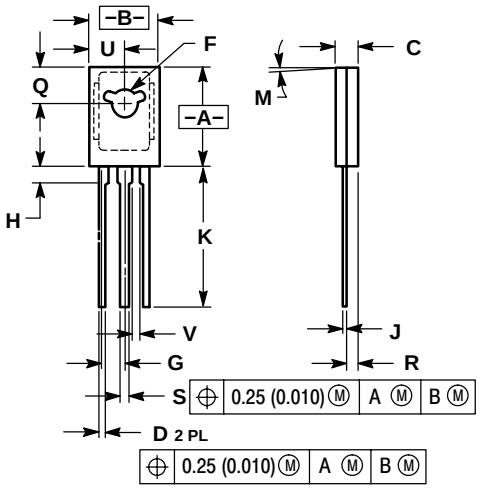
STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

TO−225
CASE 77−09
ISSUE Z

DATE 03/01/2002



SCA E



NOTES:
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. 077−01 THRU −08 OBSOLETE, NEW STANDARD 077−09.

	INCHES		I I ETERS	
DI	IN	A	IN	A
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
	0.015	0.025	0.39	0.63
	0.575	0.655	14.61	16.63
	5 TYP		5 TYP	
	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 4:
PIN 1. ANODE 1
2. ANODE 2
3. GATE

STYLE 5:
PIN 1. MT 1
2. MT 2
3. GATE

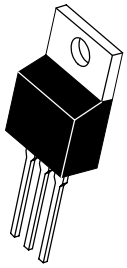
STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 7:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 9:
PIN 1. GATE
2. DRAIN
3. SOURCE

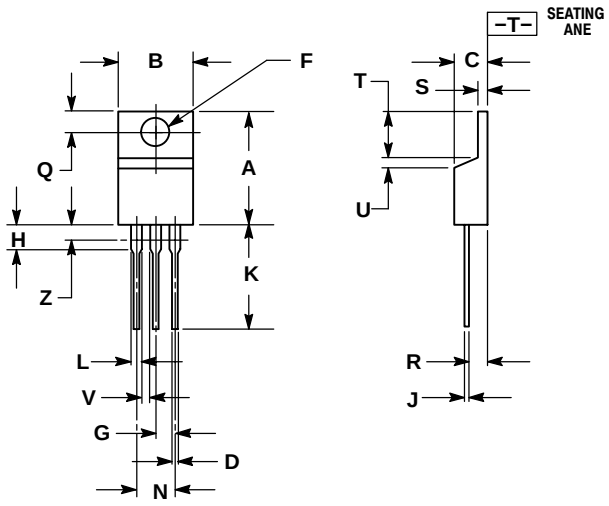
STYLE 10:
PIN 1. SOURCE
2. DRAIN
3. GATE



TO−220
CASE 221A−09
ISSUE AA

DATE 01/02/2000

SCA E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		I I ETERS	
DI	IN	A	IN	A
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
	0.018	0.025	0.46	0.64
	0.500	0.562	12.70	14.27
	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

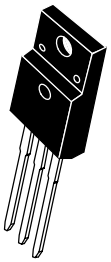
STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

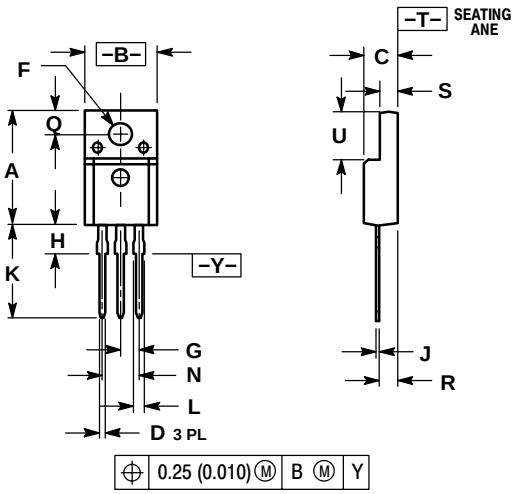
STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

TO−220 FULLPAK
CASE 221D−03
ISSUE G

DATE 03/19/2002



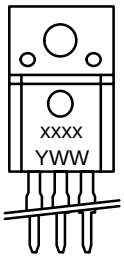
SCA E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

DI	INCHES		I I ETERS	
	IN	A	IN	A
A	0.625	0.635	15.88	16.12
B	0.408	0.418	10.37	10.63
C	0.180	0.190	4.57	4.83
D	0.026	0.031	0.65	0.78
	0.116	0.119	2.95	3.02
G	0.100 BSC		2.54 BSC	
H	0.125	0.135	3.18	3.43
	0.018	0.025	0.45	0.63
	0.530	0.540	13.47	13.73
	0.048	0.053	1.23	1.36
N	0.200 BSC		5.08 BSC	
	0.124	0.128	3.15	3.25
R	0.099	0.103	2.51	2.62
S	0.101	0.113	2.57	2.87
U	0.238	0.258	6.06	6.56

MARKING DIAGRAM



xx = Specific Device Code
Y = Year
WW = Work Week

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

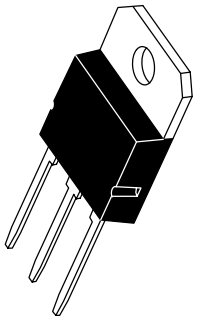
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

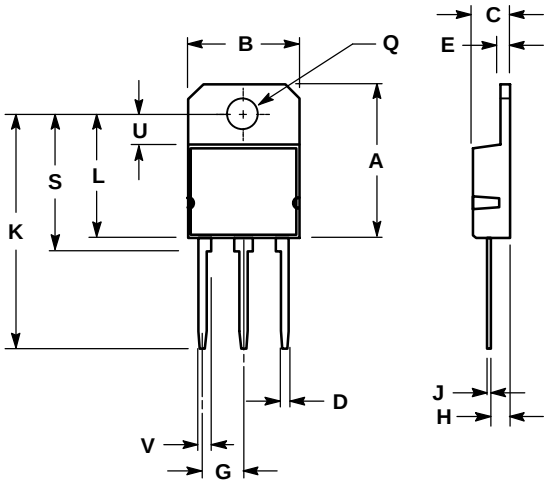
STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

SOT−93 (TO−218)
CASE 340D−02
ISSUE E

DATE 01/03/2002



SCA E



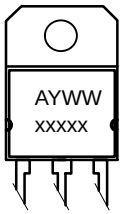
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	I I ETERS		INCHES	
DI	IN	A	IN	A
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
	0.50	0.78	0.020	0.031
	31.00 REF		1.220 REF	
	---	16.20	---	0.638
	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

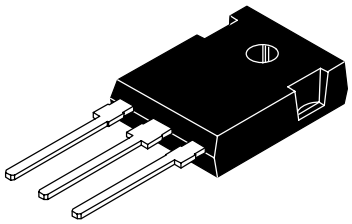
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

MARKING DIAGRAM



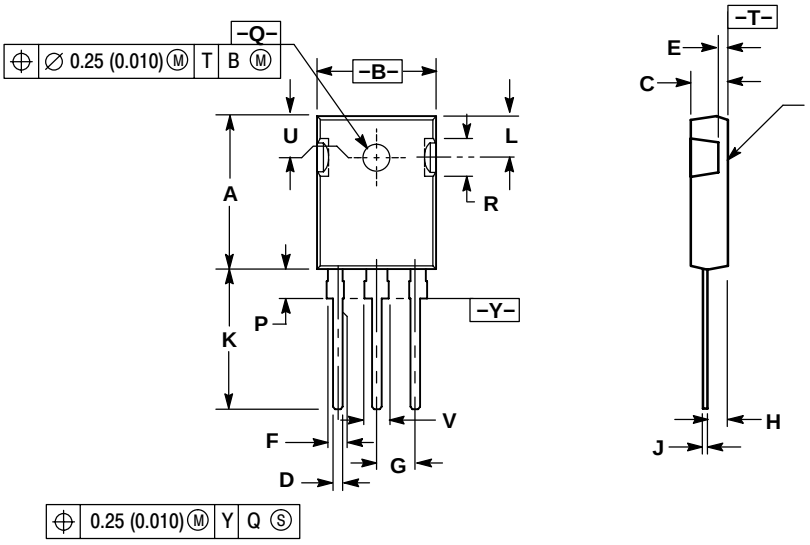
A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code



SCA E

TO−247
CASE 340K−01
ISSUE C

DATE 03/02/2000



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

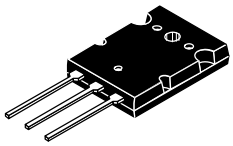
	I I ETERS		INCHES	
DI	IN	A	IN	A
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
	0.4	0.8	0.016	0.031
	14.2	14.8	0.559	0.583
	5.5 NOM		0.217 NOM	
	3.7	4.3	0.146	0.169
	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE 1
2. CATHODE(S)
3. ANODE 2
4. CATHODE(S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

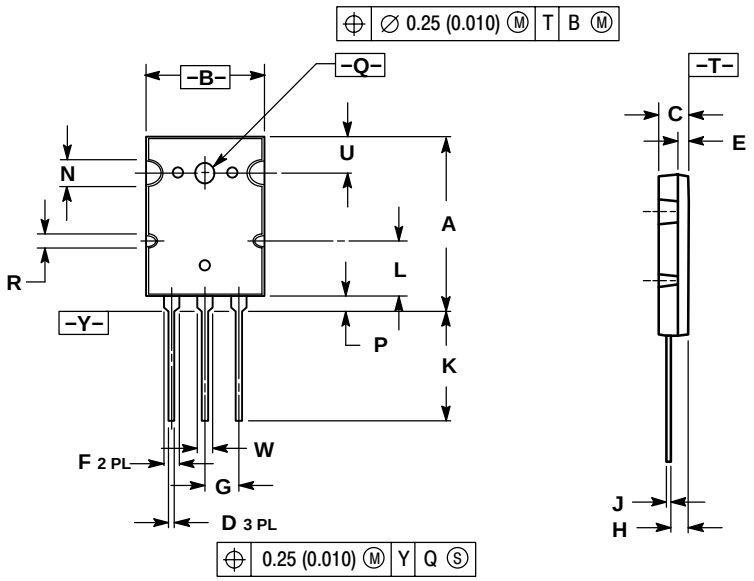
STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



TO−3PBL (TO−264)
CASE 340G−02
ISSUE H

DATE 08/08/2000

SCA E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	I I ETERS		INCHES	
DI	IN	A	IN	A
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
	0.43	0.78	0.017	0.031
	17.6	18.8	0.693	0.740
	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
	2.2	2.6	0.087	0.102
	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

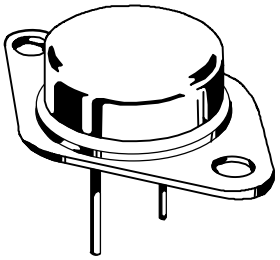
STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE

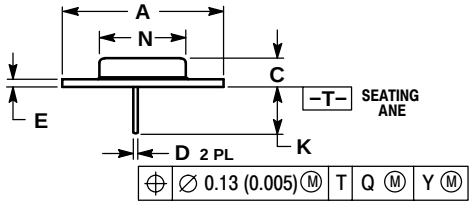
STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

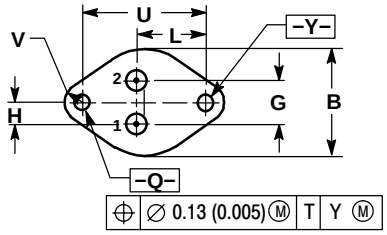
TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 05/18/1988



SCA E





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		I I ETERS	
DI	IN	A	IN	A
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
	0.440	0.480	11.18	12.19
	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

CHAPTER 4
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