National Semiconductor

April 2003

LMS75ALS176A
Differential Bus Transceivers

General Description

The LMS75ALS176A is a differential bus/line transceiver designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets ANSI Standards TIA/EIA RS422-B, TIA/EIA RS485-A and ITU recommendation V.11 and X.27. The LMS75ALS176A combines a TRI-STATE™ differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low enable, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments. The LMS75ALS176A is available in a 8-Pin SOIC package. It is a drop-in socket replacement to TI's SN75ALS176A.

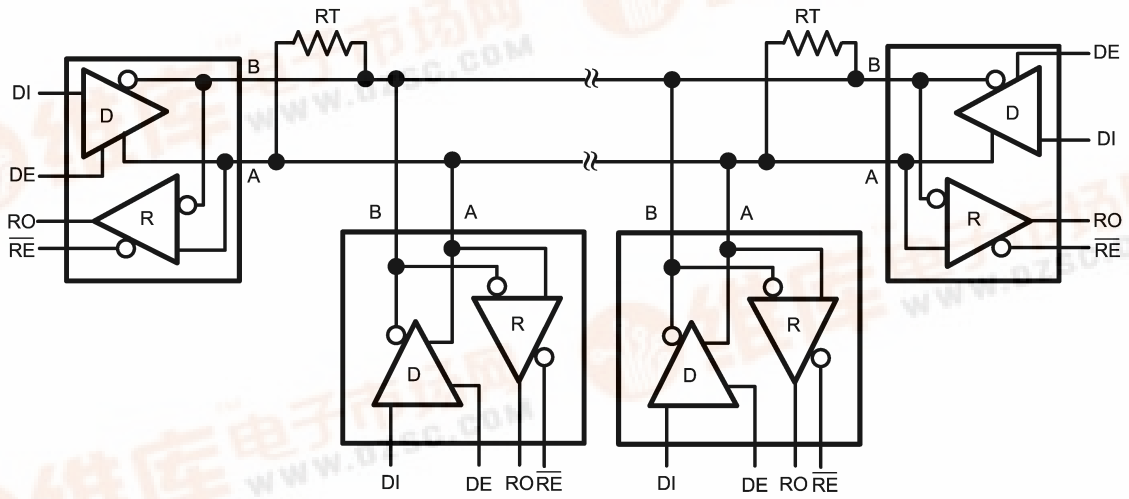
Features

- Bidirectional transceiver
- Meet ANSI standard RS-485-A and RS-422-B
- Low skew, 2ns
- Low supply current, 8mA (max.)
- Wide input and output voltage range
- High output drive capacity ±60mA
- Thermal shutdown protection
- Open circuit fail-safe for receiver
- Receiver input sensitivity ±200mV
- Receiver input hysteresis 10mV (min.)
- Single supply voltage operation, 5V
- Glitch free power-up and power-down operation
- Data rates up to 35 Mbaud
- Pin and functional compatible with TI's SN75ALS176A
- 8-Pin SOIC

Applications

- Network hubs, bridges, and routers
- Point of sales equipment (ATM, barcode readers,...)
- Industrial programmable logic controllers
- High speed parallel and serial applications
- Multipoint applications with noisy environment

Typical Application



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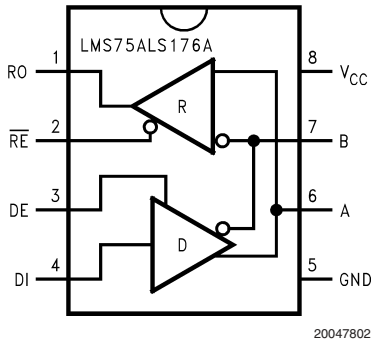
A Typical multipoint application is shown in the above figure. Terminating resistors, RT, are typically required but only located at the two ends of the cable. Pull up and pull down resistors maybe required at the end of the bus to provide failsafe biasing. The biasing resistors provide a bias to the cable when all drivers are in TRI-STATE, See National Application Note, AN-847 for further information.

Connection Diagram

8-Pin SOIC



Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMS75ALS176AM	LMS75LS176A	Rail	M08A
	LMS75ALS176AMX		2.5k Units Tape and Reel	

Truth Table

DRIVER SECTION				
$\overline{\text{RE}}$	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
$\overline{\text{RE}}$	**DE**	**A-B**		**RO**
L	L	≥ +0.2V		H
L	L	≤ −0.2V		L
H	X	X		Z
L	L	OPEN *		H

Note: * = Non Terminated, Open Input only

X = Irrelevant

Z = TRI-STATE

H = High level

L = Low level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 2)	7V
Voltage Range at Any Bus Terminal	−7V to 12V
Input Voltage, V_{IN} (DI, DE, or $\overline{RE}$)	−0.3V to V_{CC} + 0.3V
Package Thermal Impedance, θ_{JA}	125C/W
Junction Temperature (Note 3)	150˚C
Operating Free-Air Temperature Range, T_A	0˚C to 70˚C
Storage Temperature Range	−65˚C to 150˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
ESD Rating (Note 4)	2KV

Operating Ratings

	Min	Nom	Max	
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode) V_{IN} or V_{IC}			12 −7	V
High-Level Input Voltage, V_{IH} (Note 5)	2			V
Low-Level Input Voltage, V_{IL} (Note 5)			0.8	V
Differential Input Voltage, V_{ID} (Note 6)			±12	V
High-Level Output				
Driver, I_{OH}			−60	mA
Receiver, I_{OH}			−400	µA
Low-Level Output				
Driver, I_{OL}			60	mA
Receiver, I_{OL}			8	mA

Electrical Characteristics

V_{CC} = 5V, T_A = 0˚C to 70˚C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Driver Section							
V_{CL}	Input Clamp Voltage	I_I = −18mA				−1.5	V
V_O	Output Voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential Output Voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential Output Voltage	R_L = 100Ω,		2			V
		R_L = 54Ω		1.5	1.9	5	
V_{OD3}	Differential Output Voltage	V_{TEST} = −7V to 12 V		1.5		5	V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage (Note 7)	R_L = 54Ω or 100Ω				±0.2	V
V_{OC}	Common-Mode Output Voltage	R_L = 54Ω or 100Ω				3	V
						−1	
ΔV_{OC}	Change in Magnitude of Differential Output Voltage (Note 7)	R_L = 54Ω or 100Ω				±0.2	V
I_O	Output Current	Output Disabled (Note 8)	V_O = 12V			1	mA
			V_O = −7V			−0.8	
I_{IH}	High-Level Input Current	V_{IN} = 2.4V				20	µA
I_{IL}	Low-Level Input Current	V_{IN} = 0.4V				−400	µA
I_{OSD}	Short-Circuit Output Current	V_O = −7V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 8V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		4.8	8	mA
Switching Characteristics							
t_d (OD)	Differential Output Delay Time	R_L = 54Ω , C_L = 50pF		3	7	14	ns

Electrical Characteristics (Continued)

V_{CC} = 5V, T_A = 0˚C to 70˚C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_t (OD)	Differential Output Transition Time	R_L = 54Ω, C_L = 50pF			8		ns
$t_{sk(p)}$	Pulse Skew, ($\|t_{d(ODH}$ - $t_{d(ODL}\|$)	R_L = 54Ω, C_L = 50pF			0	3	ns
$t_{sk(lim)}$	Pulse Skew	R_L = 54Ω, C_L = 50pF (Note 9)			4		ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, C_L = 50pF			18	50	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, C_L = 50pF			18	35	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, C_L = 50pF			9	35	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, C_L = 50pF			10	17	ns
Receiver Section							
V_{TH+}	Positive-Going Input Threshold Voltage	V_O = 2.7V, I_O = −0.4mA				0.2	V
V_{TH-}	Negative-Going Input Threshold Voltage	V_O = 0.5V, I_O = 8mA		−0.2			V
ΔV_{TH}	Hysteresis Voltage (V_{TH+} - V_{TH-})			10			mV
V_{CL}	Enable-Input Clamp Voltage	I_I = −18mA				1.5	V
V_{OH}	High-Level Output Voltage	V_{ID} = 200mV, I_{OH} = −400µA		2.7			V
V_{OL}	Low-Level Output Voltage	V_{ID} = −200mV, I_{OL} = 8mA				0.45	V
I_{OZ}	High-Impedance-State Output Current	V_O = 0.4V to 2.4V				±20	µA
I_{IN}	Line Input Current	Other Input = 0V, (Note 5)	V_{IN} = 12V			1	mA
			V_{IN} = −7V			−0.8	
I_{IH}	High-Level Enable-Input Current	V_{IH} = 2.7V				20	µA
I_{IL}	Low-Level Enable-Input Current	V_{IL} = 0.4V				−100	µA
R_{IN}	Input Resistance			12	20		kΩ
I_{OSR}	Short-Circuit Output Current	V_{ID} = 200mV, V_O = 0V		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		4.8	8	mA
Switching Characteristics							
t_{PD}	Propagation Delay Time	V_{ID} = −1.5V to 1.5V, C_L = 15pF		8	18	30	ns
$t_{sk(p)}$	Pulse Skew ($\|t_{PLH}$ - $t_{PHL}\|$)	V_{ID} = −1.5V to 1.5V, C_L = 15pF			2		ns
$t_{sk(lim)}$	Pulse Skew	R_L = 54Ω , C_L = 50pF (Note 9)			7.5		ns
t_{PZH}	Output Enable Time to High Level	C_L = 15pF			5	35	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 15pF			5	35	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 15pF			20	35	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 15pF			10	17	ns

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics

Note 2: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: ESD rating based upon human body model, 100pF discharged through 1.5kΩ.

Note 5: Voltage limits apply to DI, DE, $\overline{RE}$ pins.

Note 6: Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

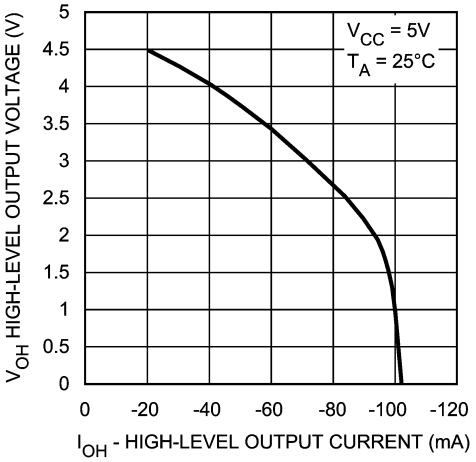
Note 7: $|\Delta V_{OD}|$ and $|\Delta V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively when the input changes from high to low levels.

Note 8: Applies to both power on and off (ANSI Standard RS-485 conditions). Does not apply to TIA/EIA-422-B for a combined driver and receiver combination.

Note 9: Skew limit is the maximum difference in propagation delay between any two channels of any two devices.

Typical Performance Characteristics

Driver High-Level Output Voltage vs. High-Level Output Current



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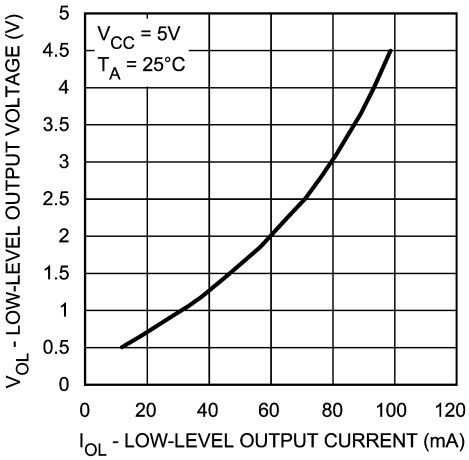
Driver Low-Level Output Voltage vs. Low-Level Output Current



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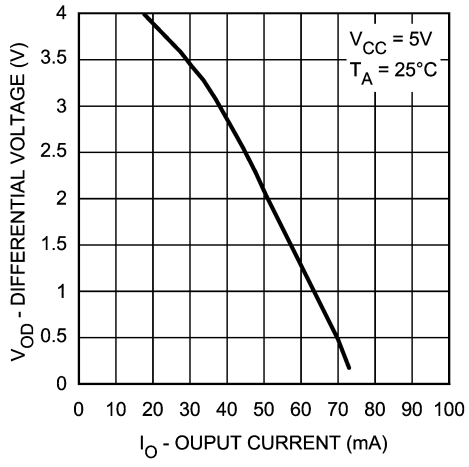
Driver Differential Output Voltage vs. Output Current



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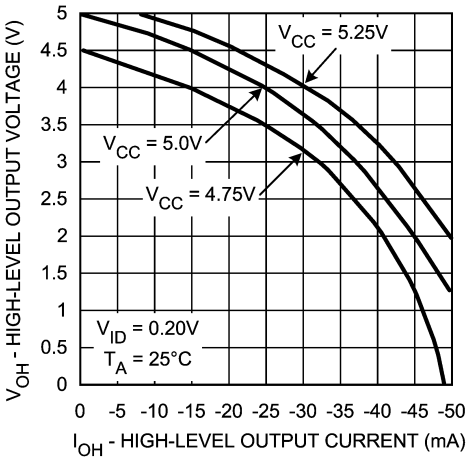
Receiver High-Level Output Voltage vs. High-Level Output Current



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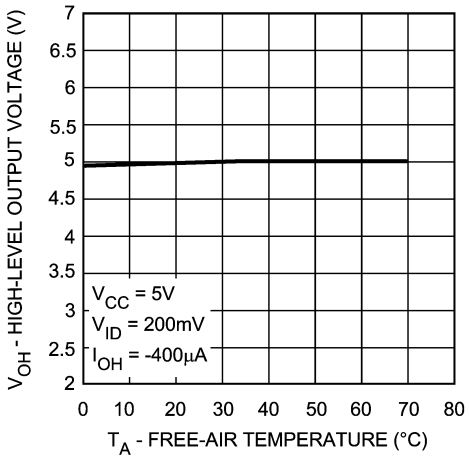
Typical Performance Characteristics (Continued)

Receiver High-Level Output Voltage vs. Free-Air Temperature



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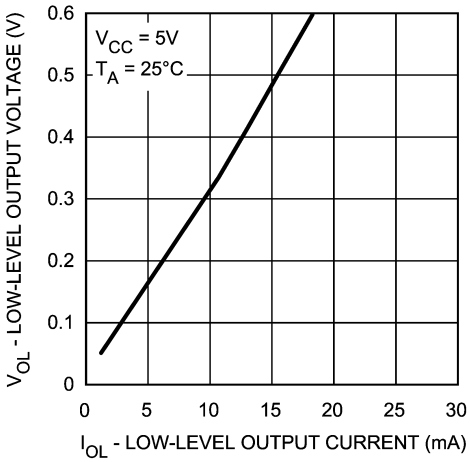
Receiver Low-Level Output Voltage vs. Low-Level Output Current



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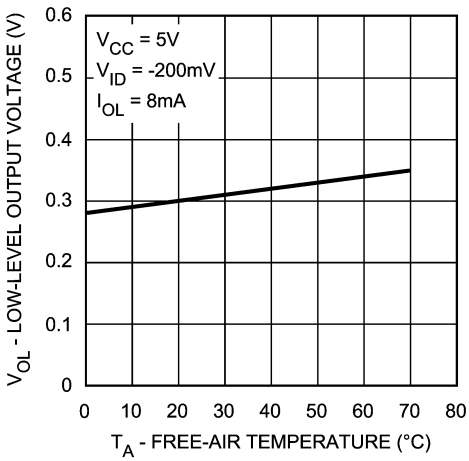
Receiver Low-Level Output Voltage vs. Free-Air Temperature



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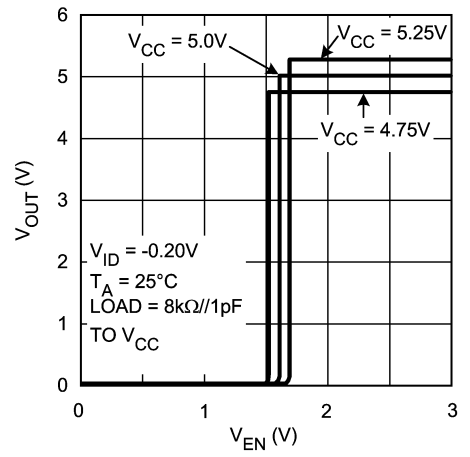
Receiver Output Voltage vs. Enable Voltage



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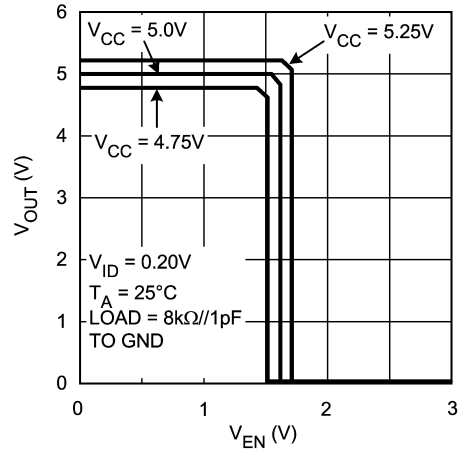
Receiver Output Voltage vs. Enable Voltage



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Parameter Measuring Information

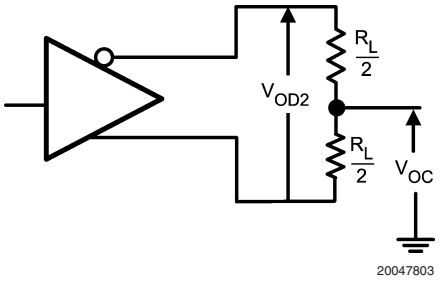


FIGURE 1. Test Circuit for V_{OD2} and V_{OC}

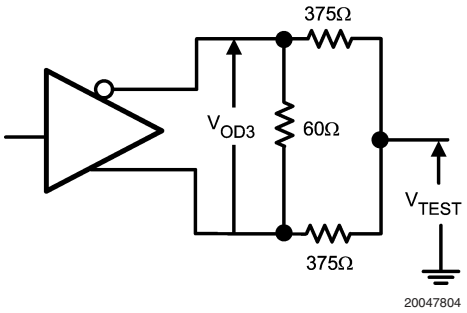


FIGURE 2. Test Circuit for V_{OD3}

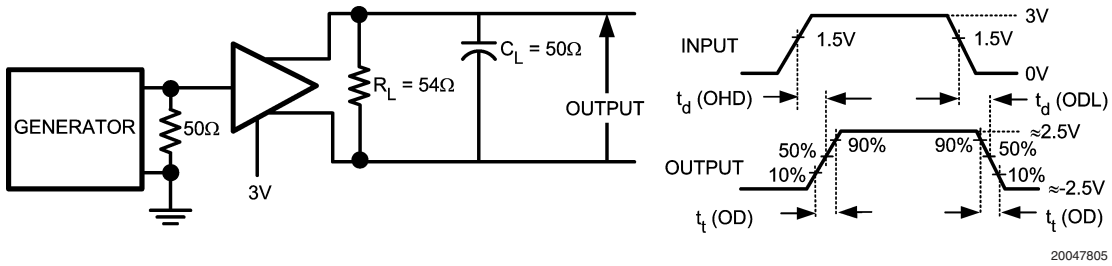


FIGURE 3. Test Circuit for Driver Differential Output Delay and Transition Times

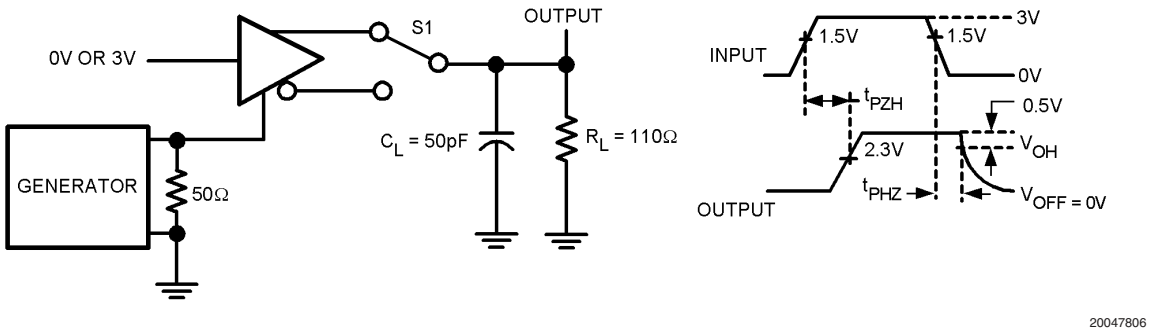


FIGURE 4. Test Circuit for Driver T_{PZH} and T_{PHZ}

Parameter Measuring Information (Continued)

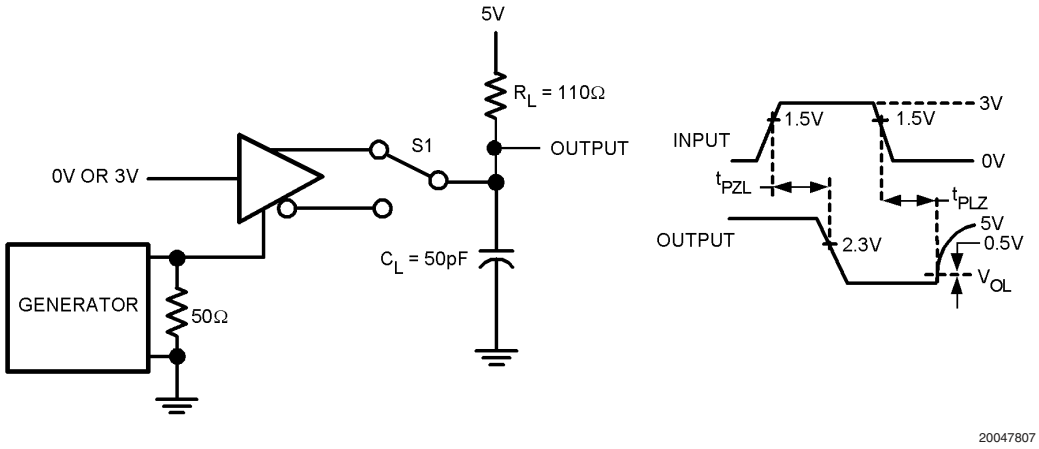


FIGURE 5. Test Circuit for T_{PZL} and T_{PLZ}

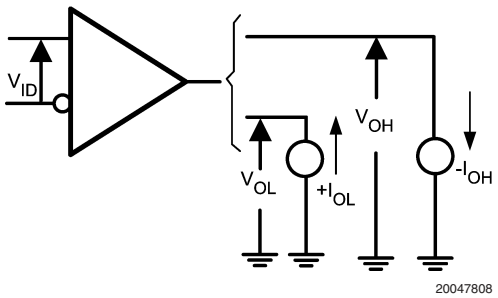


FIGURE 6. Test Circuit for Receiver V_{OH} and V_{OL}

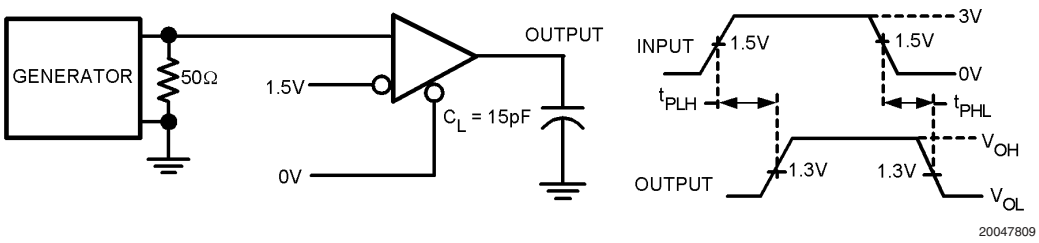
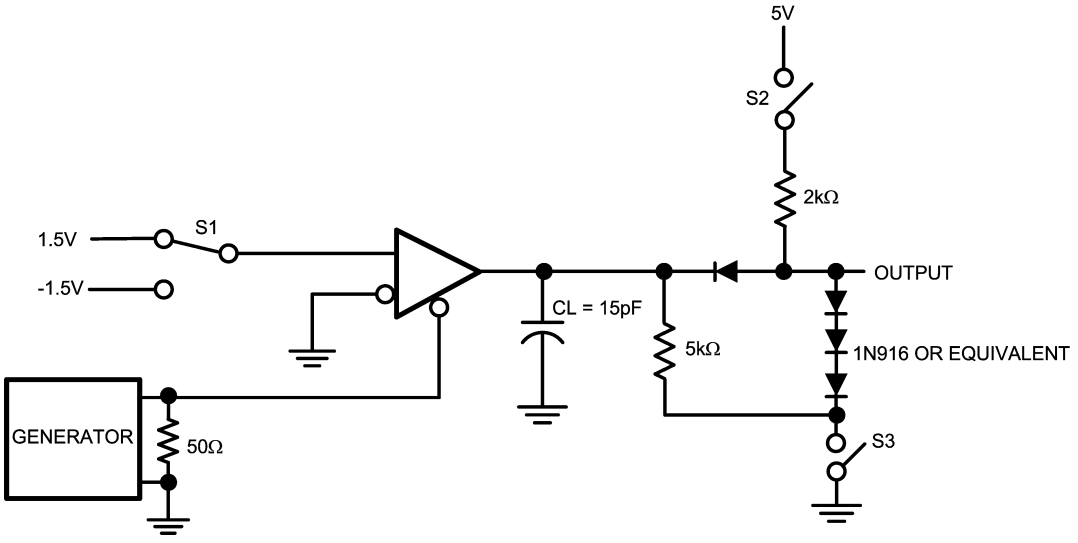


FIGURE 7. Test Circuit for T_{PLH} and T_{PHL}

Parameter Measuring Information (Continued)

Test Circuit



Voltage Waveforms

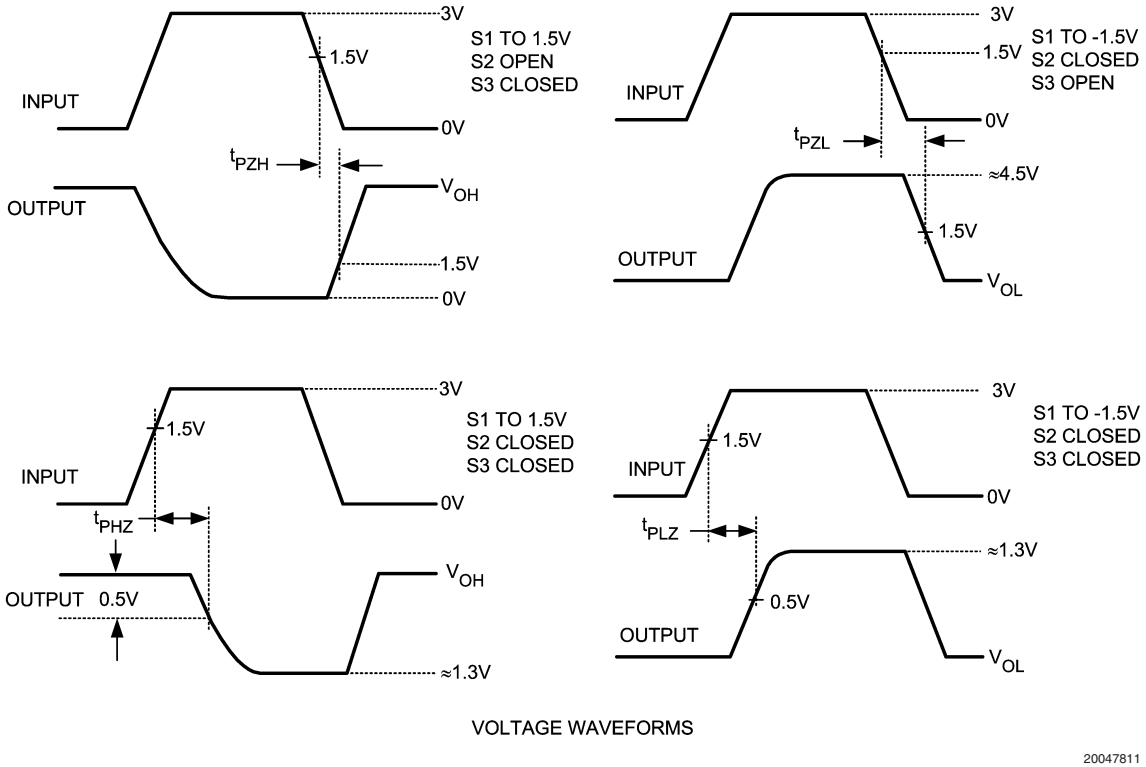


FIGURE 8. Test Circuit for Receiver T_{PZH}/ T_{PZL} and T_{PHZ}/T_{PLZ}

Application Information

POWER LINE NOISE FILTERING

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not ideal, they may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as 10µF, between the power supply pin and ground to filter out low frequencies and a 0.1µF to filter out high frequencies.

By pass-capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounted chip capacitors are the best solution because they have lower inductance.

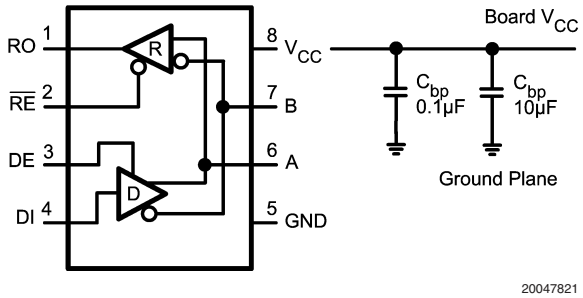
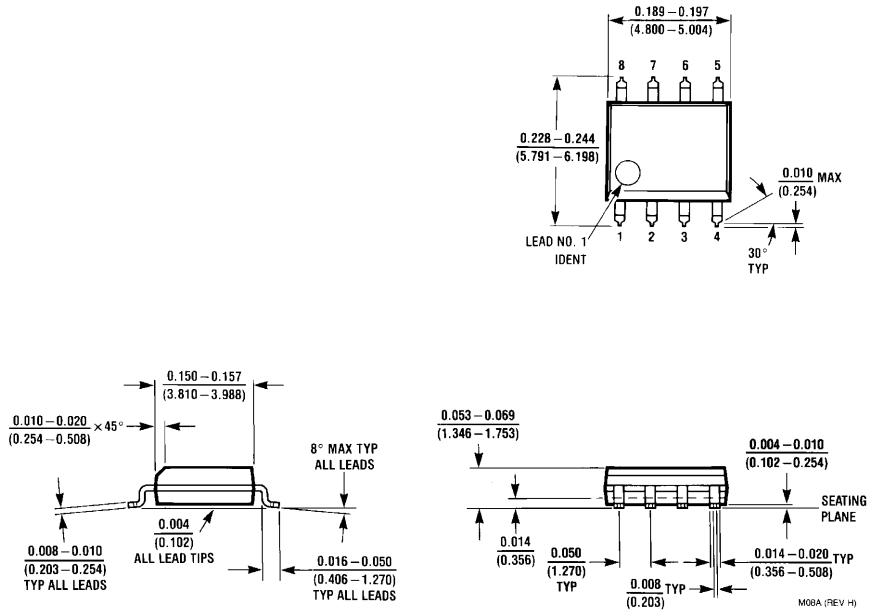


FIGURE 9. Placement of by-pass Capacitors, C_{bp}

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A

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