National Semiconductor

March 2005

LM5100A/LM5101A
3.0 Amp High Voltage High Side and Low Side Driver

General Description

The LM5100A/LM5101A High Voltage Gate Drivers are designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The outputs are independently controlled with CMOS input thresholds (LM5100A) or TTL input thresholds (LM5101A). An integrated high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC-8 pin and the LLP-10 pin packages.

Features

- 3.0A Sink/Source current gate drive
- Drives both a high side and low side N-Channel MOSFET
- Independent high and low driver logic inputs (TTL for LM5101A or CMOS for LM5100A)
- Bootstrap supply voltage range up to 118V DC
- Fast propagation times (25 ns typical)
- Drives 1000 pF load with 8 ns rise and fall times
- Excellent propagation delay matching (3 ns typical)
- Supply rail under-voltage lockouts
- Low power consumption
- Pin compatible with HIP2100/HIP2101 and LM5100/LM5101

Typical Applications

- Current Fed push-pull converters
- Half and Full Bridge power converters
- Synchronous buck converters
- Two switch forward power converters
- Forward with Active Clamp converters

Package

- SOIC-8
- LLP-10 (4 mm x 4 mm)

Simplified Block Diagram

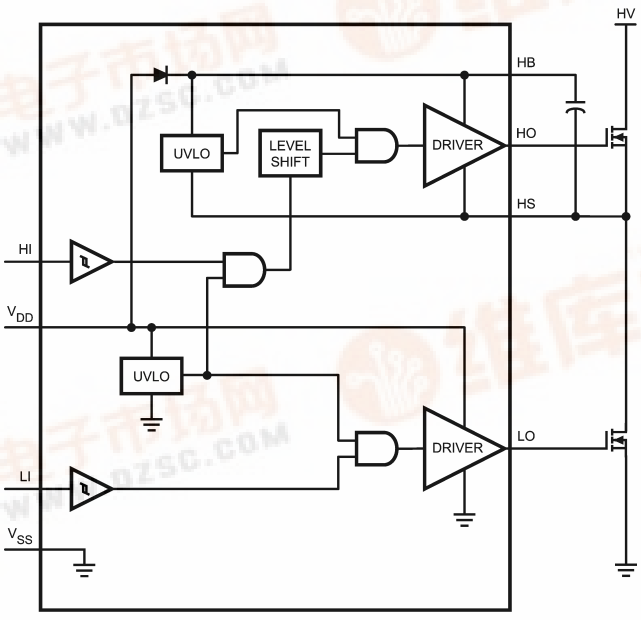
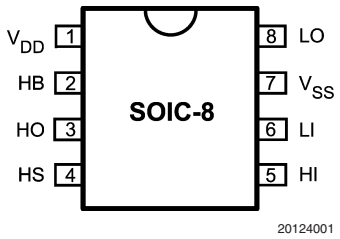


FIGURE 1.

Connection Diagrams



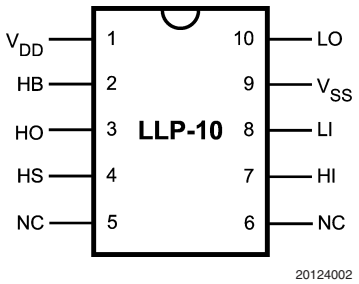


FIGURE 2.

Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5100A/01A M	SOIC-8	M08A	Shipped in anti static rails
LM5100A/01A MX	SOIC-8	M08A	2500 shipped as Tape & Reel
LM5100A/01A SD	LLP-10	SDC10A	1000 shipped as Tape & Reel
LM5100A/01A SDX	LLP-10	SDC10A	4500 shipped as Tape & Reel

Pin Description

Pin #		Name	Description	Application Information
SO-8	LLP-10			
1	1	V_{DD}	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	2	HB	High side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The Bootstrap capacitor should be place as close to IC as possible.
3	3	HO	High side gate driver output	Connect to gate of high side MOSFET with a short low inductance path.
4	4	HS	High side MOSFET source connection	Connect to bootstrap capacitor negative terminal and the source of the high side MOSFET.
5	7	HI	High side driver control input	The LM5100A inputs have CMOS type thresholds. The LM5101A inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	8	LI	Low side driver control input	The LM5100A inputs have CMOS type thresholds. The LM5101A inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	9	V_{SS}	Ground return	All signals are referenced to this ground.
8	10	LO	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.

Note: For LLP-10 package, it is recommended that the exposed pad on the bottom of the LM5100A / LM5101A be soldered to ground plane on the PC board, and the ground plane should extend out from beneath the IC to help dissipate the heat. Pins 5 and 6 have no connection.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{DD} to V_{SS}	−0.3V to +18V
V_{HB} to V_{HS}	−0.3V to +18V
LI or HI Inputs	−0.3V to V_{DD} +0.3V
LO Output	−0.3V to V_{DD} +0.3V
HO Output	V_{HS} −0.3V to V_{HB} +0.3V
V_{HS} to V_{SS}	−1V to +100V
V_{HB} to V_{SS}	118V
Junction Temperature	+150˚C
Storage Temperature Range	−55˚C to +150˚C
ESD Rating HBM (Note 2)	2 KV

Recommended Operating Conditions

V_{DD}	+9V to +14V
HS	−1V to 100V
HB	V_{HS} +8V to V_{HS} +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40˚C to +125˚C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V (LM5100A)		0.1	**0.2**	mA
		LI = HI = 0V (LM5101A)		0.25	**0.4**	
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		2.0	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.6	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.1	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.4		mA
INPUT PINS						
V_{IL}	Input Voltage Threshold (LM5100A)	Rising Edge	**4.5**	5.4	**6.3**	V
V_{IL}	Input Voltage Threshold (LM5101A)	Rising Edge	**1.3**	1.8	**2.3**	V
V_{IHYS}	Input Voltage Hysteresis (LM5101A)			50		mV
V_{IHYS}	Input Voltage Hysteresis (LM5100A)			500		mV
R_I	Input Pulldown Resistance		**100**	200	**400**	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.8	**7.4**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.52	**0.85**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.80	**1.0**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		1.0	**1.65**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.12	**0.25**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD}−V_{LO}		0.24	**0.45**	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		3.0		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		3.0		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.12	**0.25**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = −100 mA V_{OHH} = V_{HB}−V_{HO}		0.24	**0.45**	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		3.0		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		3.0		A

Electrical Characteristics (Continued)

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HO GATE DRIVER						
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOIC-8		170		˚C/W
		LLP-10 (Note 3)		40		

Switching Characteristics

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LM5100A						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			20	**45**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			20	**45**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			20	**45**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			20	**45**	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			1	**10**	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			1	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		8		ns
t_R, t_F	Either Output Fall Time (3V to 9V)	C_L = 0.1 µF		0.26		µs
	Either Output Rise Time (3V to 9V)	C_L = 0.1 µF		0.43		
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 100 mA, I_R = 100 mA		38		ns
LM5101A						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			22	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			22	**56**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			26	**56**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			26	**56**	ns
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off			4	**10**	ns
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On			4	**10**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		8		ns
t_R, t_F	Either Output Fall Time (3V to 9V)	C_L = 0.1 µF		0.26		µs
	Either Output Rise Time (3V to 9V)	C_L = 0.1 µF		0.43		

Switching Characteristics (Continued)

Specifications in standard typeface are for T_J = +25˚C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LM5101A						
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 100 mA, I_R = 100 mA		38		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 KV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000V.

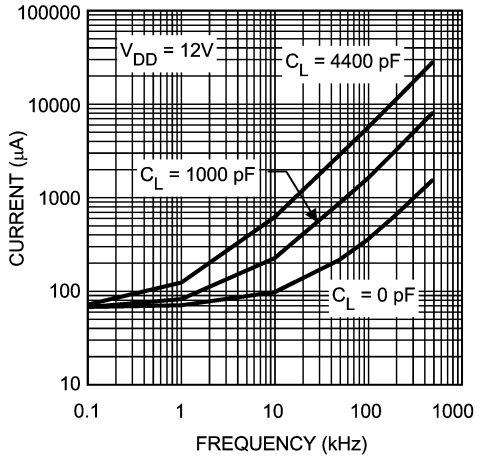
Note 3: 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Note 4: Min and Max limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

Typical performance Characteristics

LM5100A I_{DD} vs Frequency



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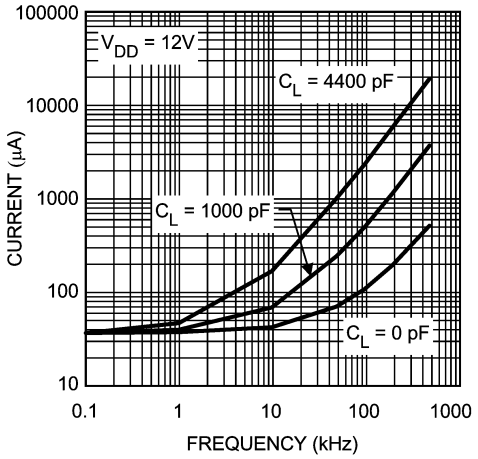
LM5101A I_{DD} vs Frequency



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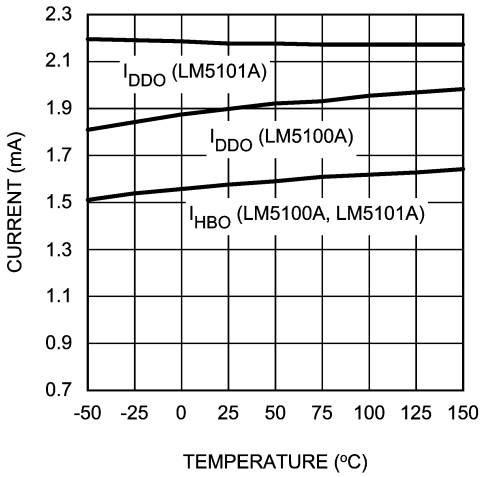
LM5100A/LM5101A Operating Current vs Temperature



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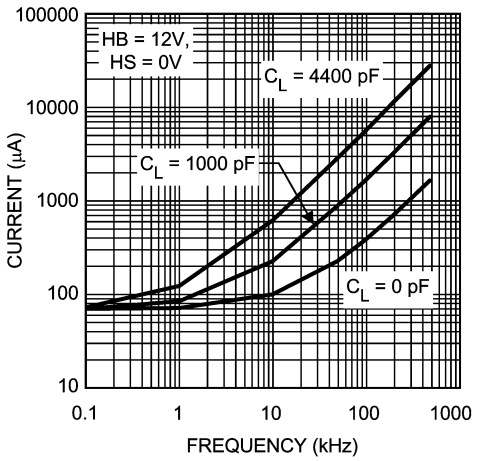
IHB vs Frequency



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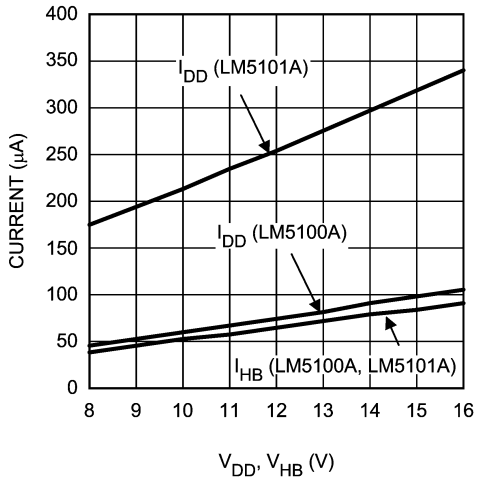
Quiescent Current vs Supply Voltage



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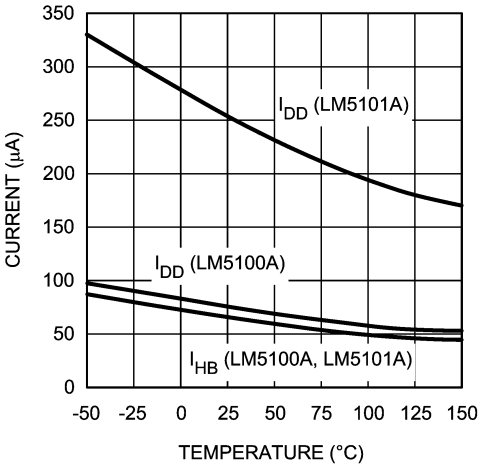
LM5100A/LM5101A Quiescent Current vs Temperature



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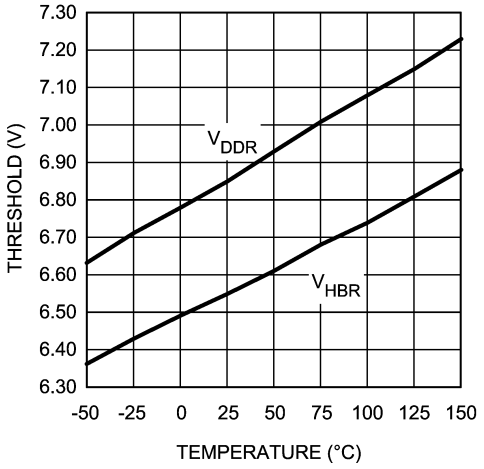
Typical performance Characteristics (Continued)

Undervoltage Rising Thresholds vs Temperature



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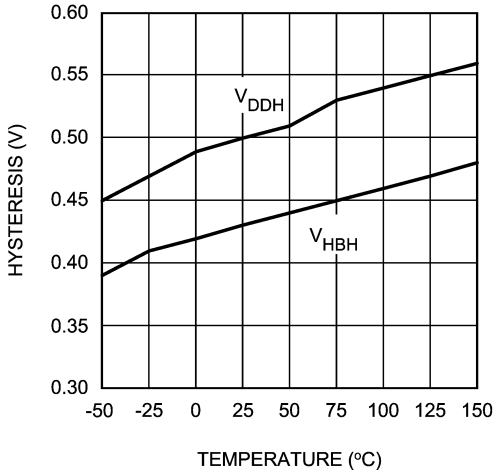
LM5100A Undervoltage Threshold Hysteresis vs Temperature



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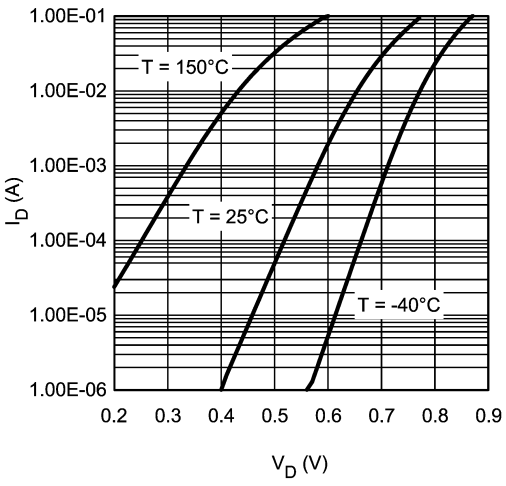
Bootstrap Diode Forward Voltage



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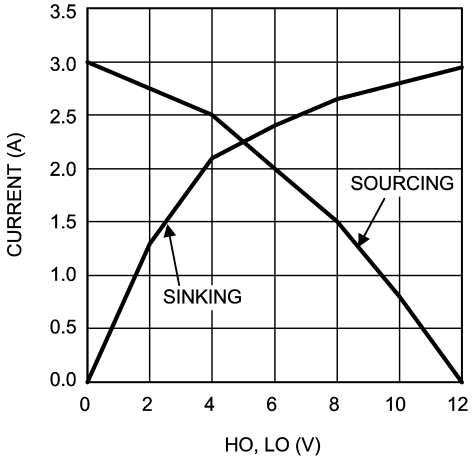
HO and LO Peak Output Current vs Output Voltage



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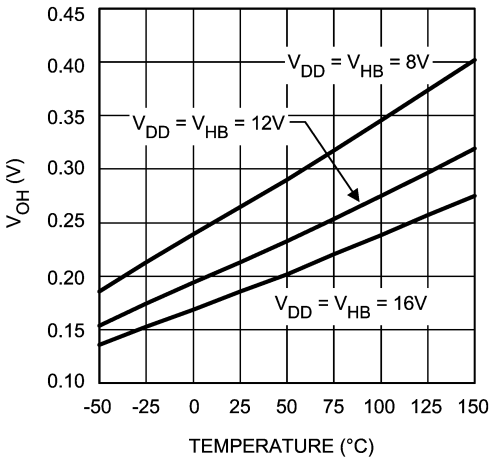
LO and HO Gate Drive—High Level Output Voltage vs Temperature



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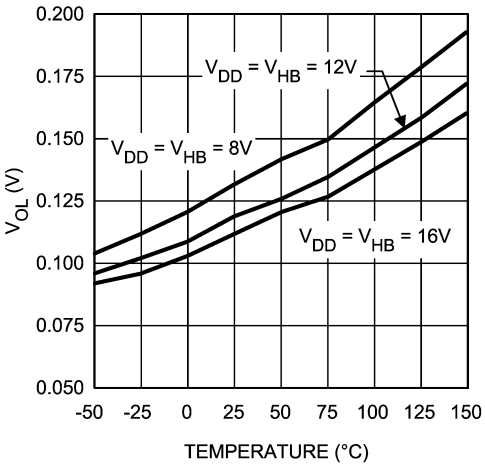
LO and HO Gate Drive—Low Level Output Voltage vs Temperature



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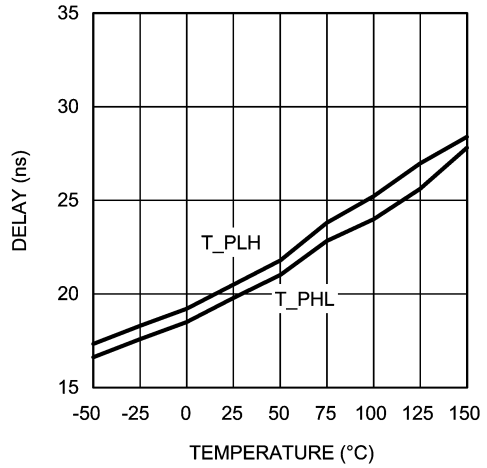
Typical performance Characteristics (Continued)

LM5100A Propagation Delay vs Temperature



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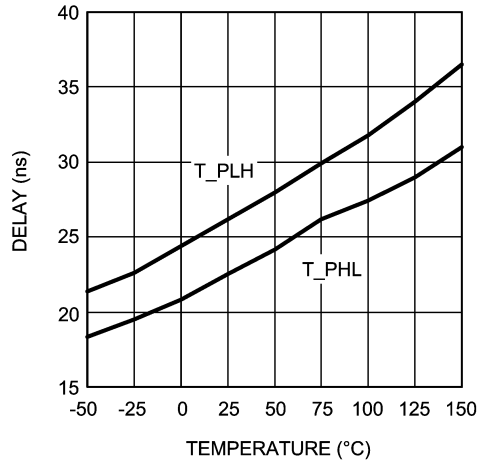
LM5101A Propagation Delay vs Temperature



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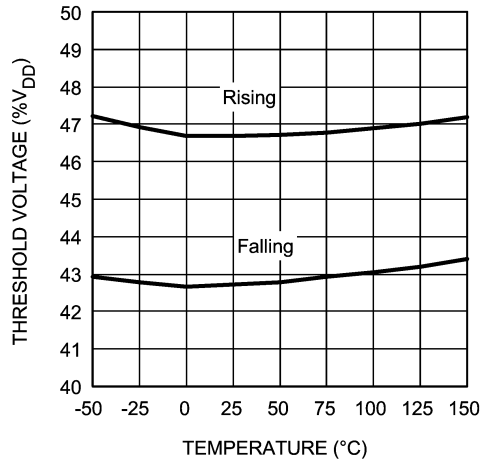
LM5100A Input Threshold vs Temperature



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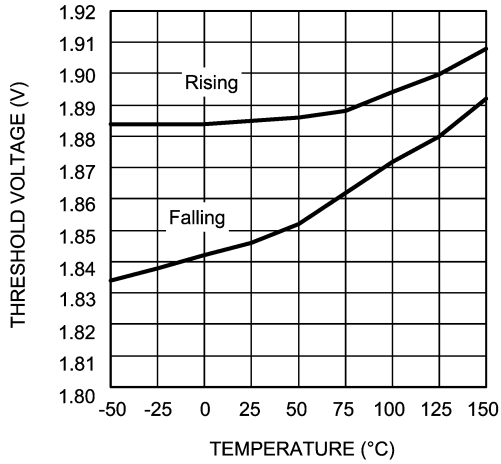
LM5101A Input Threshold vs Temperature



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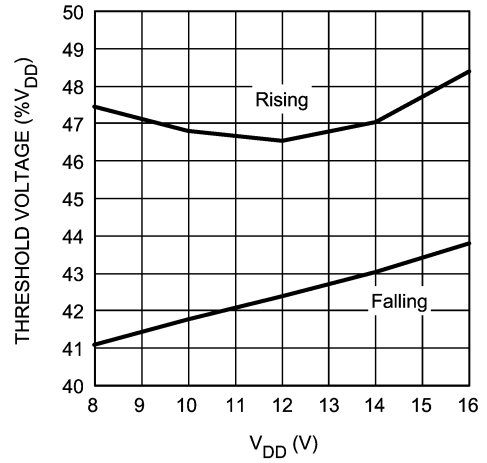
LM5100A Input Threshold vs V_{DD}



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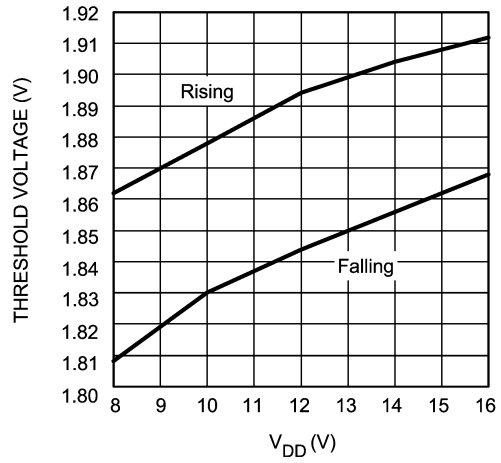
LM5101A Input Threshold vs V_{DD}



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Timing Diagram

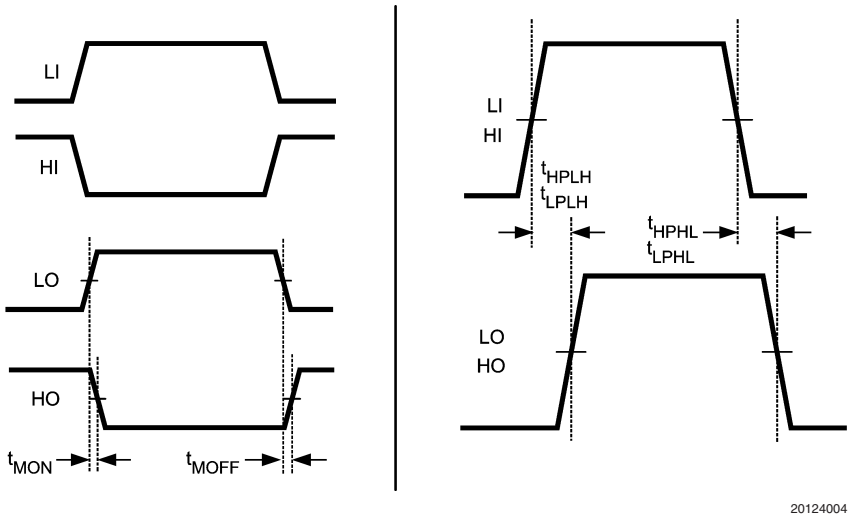


FIGURE 3.

Layout Considerations

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR / ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:

   a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.

   b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

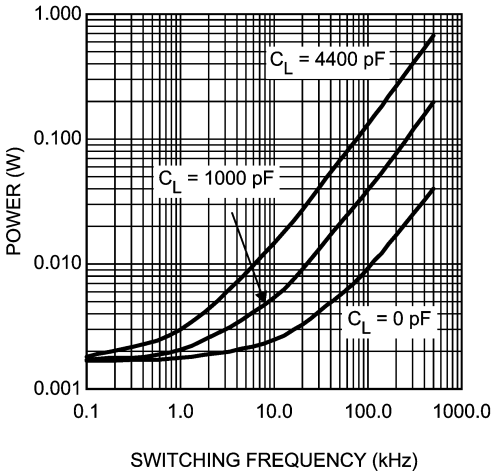
Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

Gate Driver Power Dissipation (LO + HO)
V_{DD} = 12V, Neglecting Diode Losses



The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency.

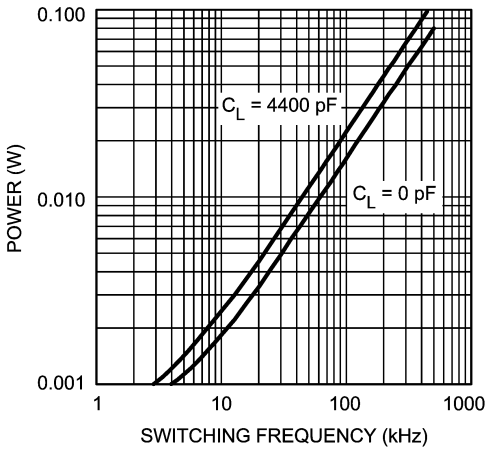
Power Dissipation Considerations

(Continued)

Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

Diode Power Dissipation V_{IN} = 50V



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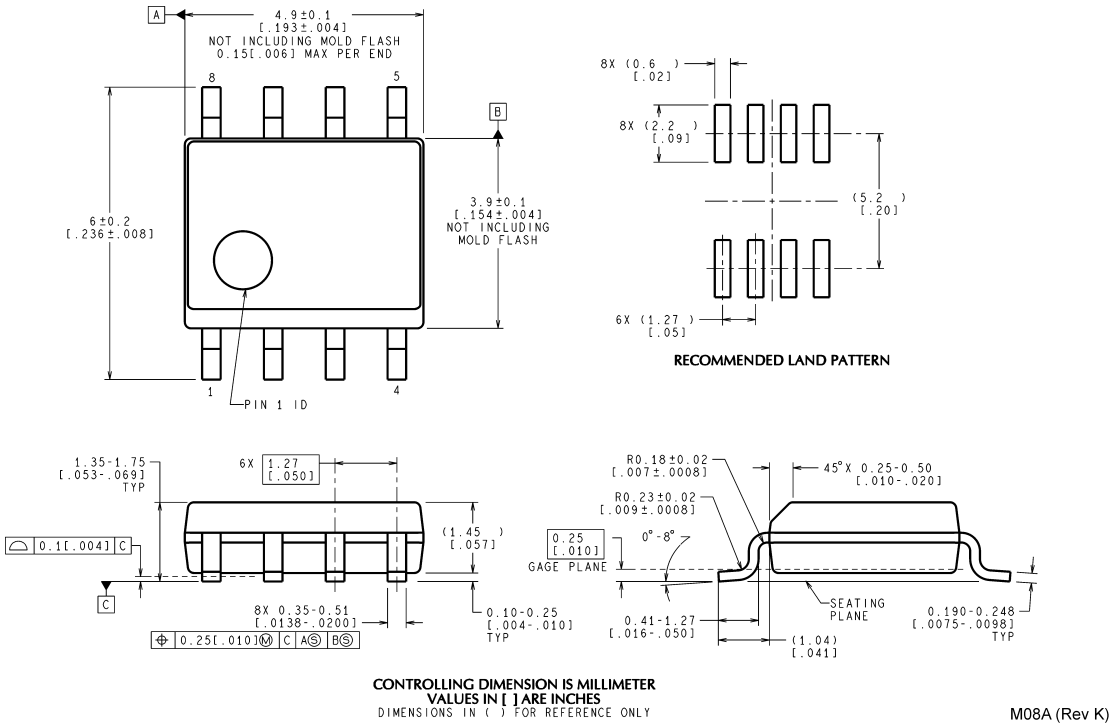
Physical Dimensions inches (millimeters) unless otherwise noted



M08A (Rev K)

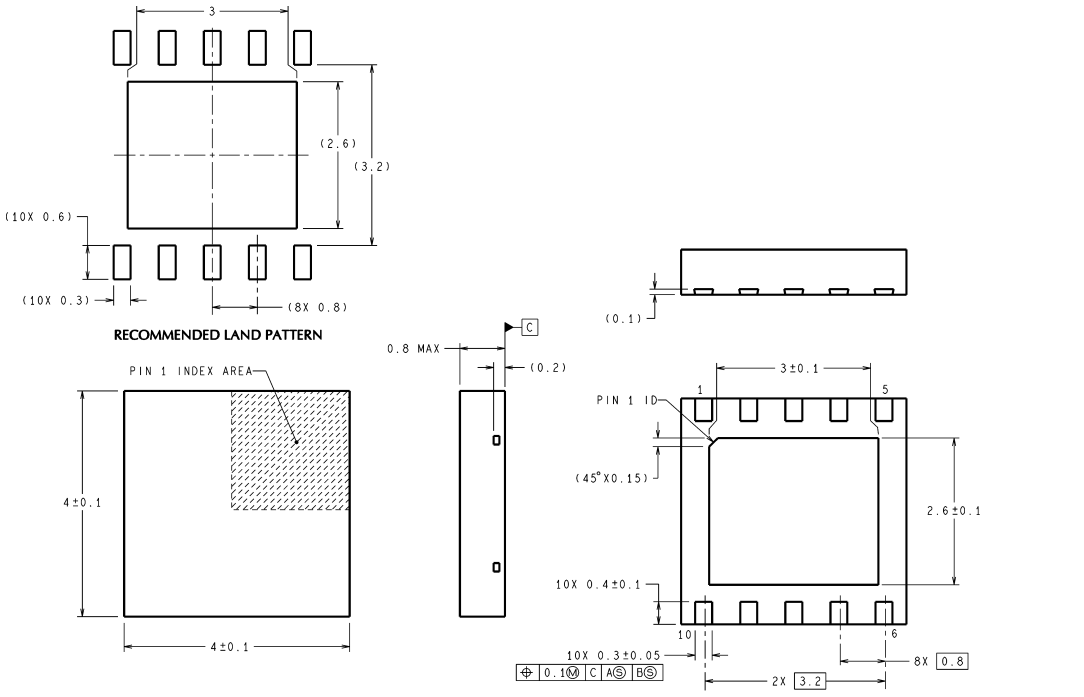
Controlling dimension is inch. Values in [ ] are millimeters.

Notes: Unless otherwise specified.

1. Standard lead finish to be 200 microinches/5.08 micrometers minimum lead/tin (solder) on copper.
2. Dimension does not include mold flash.
3. Reference JEDEC registration MS-012, Variation AA, dated May 1990.

SOIC-8 Outline Drawing
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes: Unless otherwise specified.

1. For solder thickness and composition, see “Solder Information” in the packaging section of the National Semiconductor web page (www.national.com).
2. Maximum allowable metal burr on lead tips at the package edges is 76 microns.
3. No JEDEC registration as of May 2003.

LLP-10 Outline Drawing
NS Package Number SDC10A

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