



April 2005

## LM4940 Boomer® Audio Power Amplifier Series

### 6W Stereo Audio Power Amplifier

#### General Description

The LM4940 is a dual audio power amplifier primarily designed for demanding applications in flat panel monitors and TV's. It is capable of delivering 6 watts per channel to a  $4\Omega$  load with less than 10% THD+N while operating on a  $14.4V_{DC}$  power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4940 does not require bootstrap capacitors or snubber circuits. Therefore, it is ideally suited for display applications requiring high power and minimal size.

The LM4940 features a low-power consumption active-low shutdown mode. Additionally, the LM4940 features an internal thermal shutdown protection mechanism along with short circuit protection.

The LM4940 contains advanced pop & click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4940 is a unity-gain stable and can be configured by external gain-setting resistors.

#### Key Specifications

|  |                  |
|--|------------------|
| ■ Quiescent Power Supply Current               | 40mA (max)       |
| ■ $P_{OUT}$ (SE)                               |                  |
| $V_{DD} = 14.4V$ , $R_L = 4\Omega$ , 10% THD+N | 6W (typ)         |
| ■ Shutdown current                             | 40 $\mu$ A (typ) |

#### Features

- Pop & click circuitry eliminates noise during turn-on and turn-off transitions
- Low current, active-low shutdown mode
- Low quiescent current
- Stereo 6W output,  $R_L = 4\Omega$
- Short circuit protection
- Unity-gain stable
- External gain configuration capability

#### Applications

- Flat Panel Monitors
- Flat Panel TV's
- Computer Sound Cards

#### Typical Application

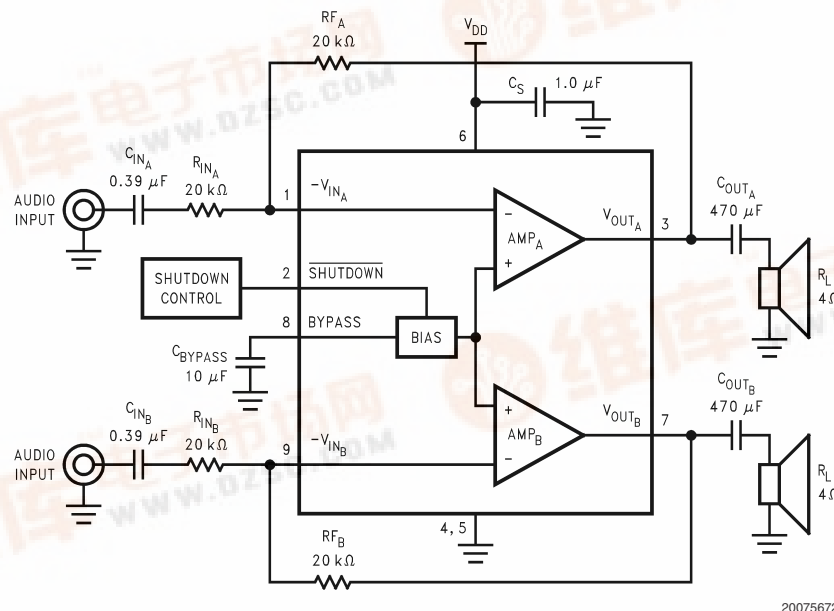
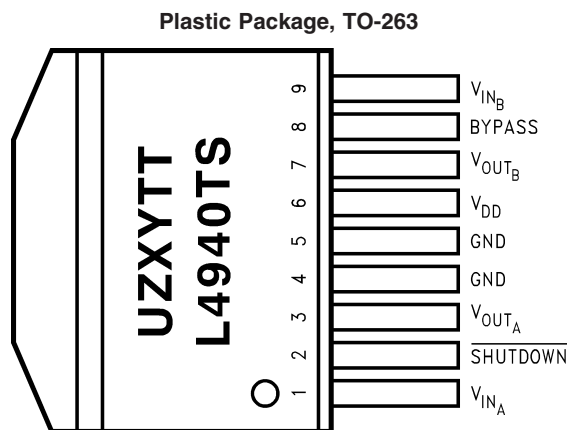


FIGURE 1. Typical Stereo Audio Amplifier Application Circuit

LM4940 6W Stereo Audio Power Amplifier



## Connection Diagram



200756E7

**Top View**  
**U = Wafer Fab Code**  
**Z = Assembly Plant Code**  
**XY = Date Code**  
**TT = Die Traceability**  
**Order Number LM4940TS**  
**See NS Package Number TS9A**

**Absolute Maximum Ratings** (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|   |                          |
|---|--------------------------|
| Supply Voltage (pin 6, referenced to GND, pins 4 and 5) | 18.0V                    |
| Storage Temperature                                     | –65°C to +150°C          |
| Input Voltage   |                          |
| pins 3 and 7  | –0.3V to $V_{DD} + 0.3V$ |
| pins 1, 2, 8, and 9                                     | –0.3V to 9.5V            |
| Power Dissipation (Note 3)                              | Internally limited       |
| ESD Susceptibility (Note 4)                             | 2000V                    |
| ESD Susceptibility (Note 5)                             | 200V                     |

|                             |        |
|-----------------------------|--------|
| Junction Temperature        | 150°C  |
| Thermal Resistance          |        |
| $\theta_{JC}$ (TS)          | 4°C/W  |
| $\theta_{JA}$ (TS) (Note 3) | 20°C/W |
| $\theta_{JC}$ (TA)          | 4°C/W  |
| $\theta_{JA}$ (TA) (Note 3) | 20°C/W |

**Operating Ratings**

|                   |                                 |                            |
|-------------------|---------------------------------|----------------------------|
| Temperature Range | $T_{MIN} \leq T_A \leq T_{MAX}$ | –40°C $\leq T_A \leq$ 85°C |
| Supply Voltage    |                                 | 10V $\leq V_{DD} \leq$ 16V |

**Electrical Characteristics**  $V_{DD} = 12V$  (Notes 1, 2)

The following specifications apply for  $V_{DD} = 12V$ ,  $A_V = 10$ ,  $R_L = 4\Omega$ ,  $f = 1kHz$  unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

| Symbol          | Parameter                         | Conditions   | LM4940              |                       | Units<br>(Limits)  |
|-----------------|-----------------------------------|--|---------------------|-----------------------|--------------------|
|                 |                                   |  | Typical<br>(Note 6) | Limit<br>(Notes 7, 8) |                    |
| $I_{DD}$        | Quiescent Power Supply Current    | $V_{IN} = 0V$ , $I_O = 0A$ , No Load                 | 16                  | 40                    | mA (max)           |
| $I_{SD}$        | Shutdown Current                  | $V_{SHUTDOWN} = GND$ (Note 9)                        | 40                  | 100                   | $\mu A$ (max)      |
| $V_{SDIH}$      | Shutdown Voltage Input High       |  |                     | 2.0<br>$V_{DD}/2$     | V (min)<br>V (max) |
| $V_{SDIL}$      | Shutdown Voltage Input Low        |  |                     | 0.4                   | V (max)            |
| $P_O$           | Output Power                      | Single Channel                                       |                     |                       | W (min)            |
|                 |                                   | THD+N = 1%   | 3.1                 | 2.8                   |                    |
|                 |                                   | THD+N = 10%  | 4.2                 |                       |                    |
|                 |                                   | $V_{DD} = 14.4V$ , THD+N = 10%                       | 6.0                 |                       |                    |
| THD+N           | Total Harmonic Distortion + Noise | $P_O = 1W_{rms}$ , $A_V = 10$ , $f = 1kHz$           | 0.15                |                       | %                  |
| $\epsilon_{OS}$ | Output Noise                      | A-Weighted Filter, $V_{IN} = 0V$ ,<br>Input Referred | 10                  |                       | $\mu V$            |
| $X_{TALK}$      | Channel Separation                | $P_O = 1W$   | 70                  |                       | dB                 |
| PSRR            | Power Supply Rejection Ratio      | $V_{RIPPLE} = 200mV_{P-P}$ , $f_{RIPPLE} = 1kHz$     | 56                  |                       | dB                 |

**Note 1:** All voltages are measured with respect to the GND pin, unless otherwise specified.

**Note 2:** *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$  or the given in Absolute Maximum Ratings, whichever is lower. For the LM4940 typical application (shown in Figure 1) with  $V_{DD} = 12V$ ,  $R_L = 4\Omega$  stereo operation the total power dissipation is 3.65W.  $\theta_{JA} = 20^\circ C/W$  for both TO263 and TO220 packages mounted to 16in<sup>2</sup> heatsink surface area.

**Note 4:** Human body model, 100pF discharged through a 1.5 k $\Omega$  resistor.

**Note 5:** Machine Model, 220pF–240pF discharged through all pins.

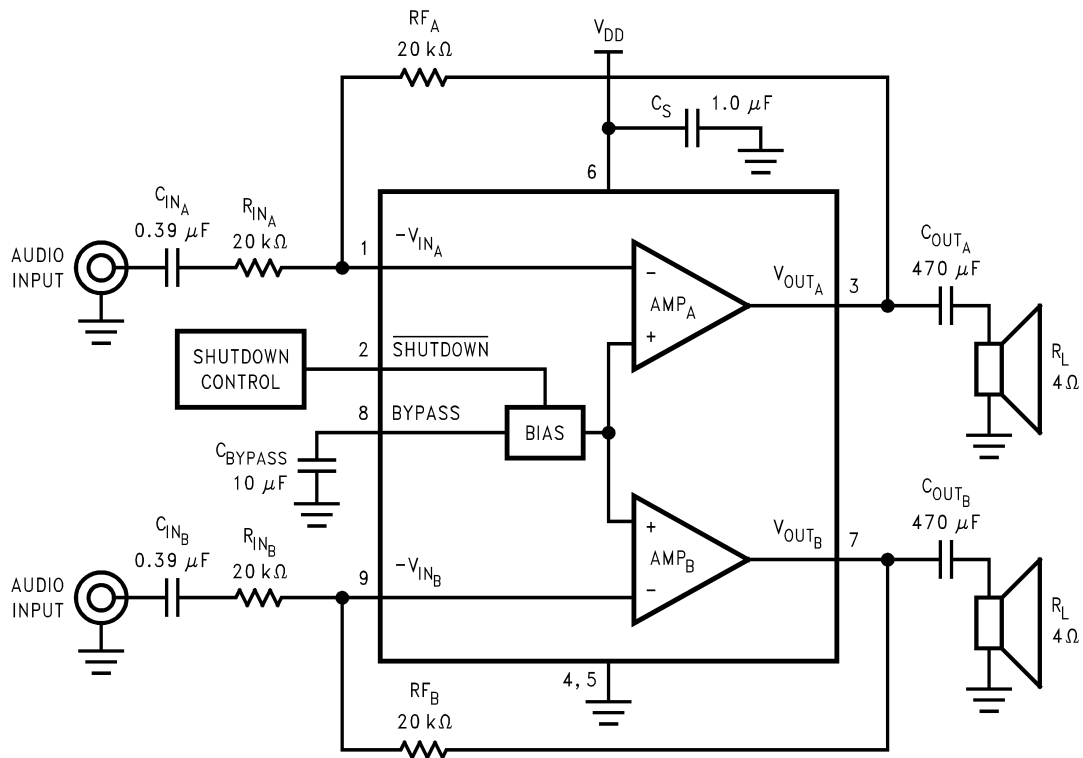
**Note 6:** Typicals are measured at 25°C and represent the parametric norm.

**Note 7:** Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 8:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

**Note 9:** Shutdown current is measured in a normal room environment. The Shutdown pin should be driven as close as possible to GND for minimum shutdown current.

## Typical Application



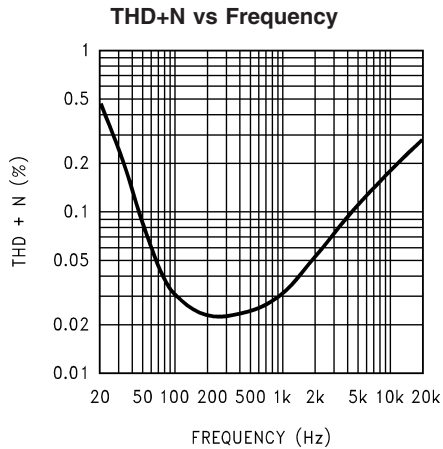
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FIGURE 2. Typical Stereo Audio Amplifier Application Circuit

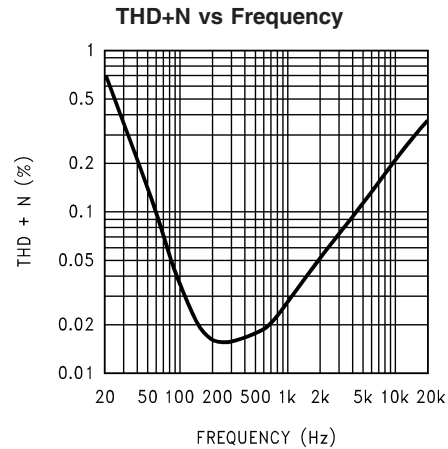
## External Components Description Refer to (Figure 1.)

| Components |              | Functional Description   |
|------------|--------------|--|
| 1.         | $R_{IN}$     | This is the inverting input resistance that, along with $R_F$ , sets the closed-loop gain. Input resistance $R_{IN}$ and input capacitance $C_{IN}$ form a high pass filter. The filter's cutoff frequency is $f_C = 1/(2\pi R_{IN} C_{IN})$ .   |
| 2.         | $C_{IN}$     | This is the input coupling capacitor. It blocks DC voltage at the amplifier's inverting input. $C_{IN}$ and $R_{IN}$ create a highpass filter. The filter's cutoff frequency is $f_C = 1/(2\pi R_{IN} C_{IN})$ . Refer to the <b>SELECTING EXTERNAL COMPONENTS</b> section for an explanation of determining $C_{IN}$ 's value.                                    |
| 3.         | $R_F$        | This is the feedback resistance that, along with $R_i$ , sets closed-loop gain.  |
| 4.         | $C_S$        | The supply bypass capacitor. Refer to the <b>POWER SUPPLY BYPASSING</b> section for information about properly placing, and selecting the value of, this capacitor.  |
| 5.         | $C_{BYPASS}$ | This capacitor filters the half-supply voltage present on the BYPASS pin. Refer to the Application section, <b>SELECTING EXTERNAL COMPONENTS</b> , for information about properly placing, and selecting the value of, this capacitor.   |
| 6.         | $C_{OUT}$    | This is the output coupling capacitor. It blocks the nominal $V_{DD}/2$ voltage present at the output and prevents it from reaching the load. $C_{OUT}$ and $R_L$ form a high pass filter whose cutoff frequency is $f_C = 1/(2\pi R_L C_{OUT})$ . Refer to the <b>SELECTING EXTERNAL COMPONENTS</b> section for an explanation of determining $C_{OUT}$ 's value. |

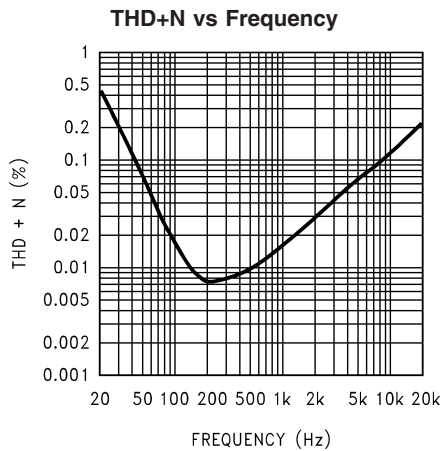
## Typical Performance Characteristics



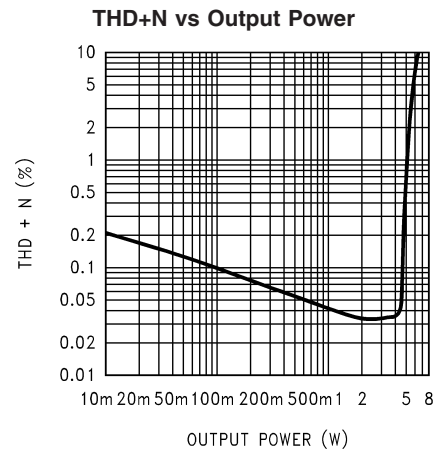
$V_{DD} = 12V$ ,  $R_L = 4\Omega$ , SE operation,  
both channels driven and loaded (average shown),  
 $P_{OUT} = 1W$ ,  $A_V = 1$



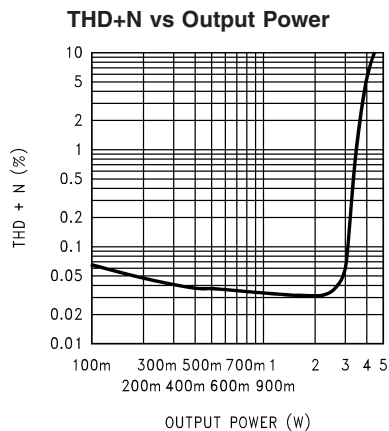
$V_{DD} = 12V$ ,  $R_L = 4\Omega$ , SE operation,  
both channels driven and loaded (average shown),  
 $P_{OUT} = 2.5W$ ,  $A_V = 1$



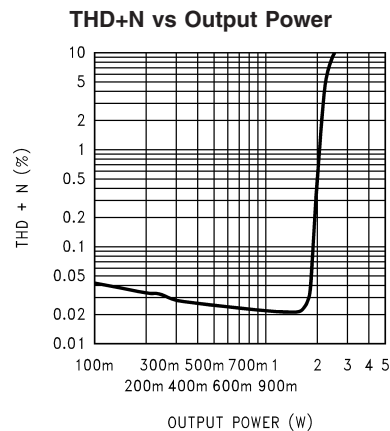
$V_{DD} = 12V$ ,  $R_L = 8\Omega$ , SE operation,  
both channels driven and loaded (average shown),  
 $P_{OUT} = 1W$ ,  $A_V = 1$



$V_{DD} = 14.4V$ ,  $R_L = 4\Omega$ , SE operation,  $A_V = 1$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$

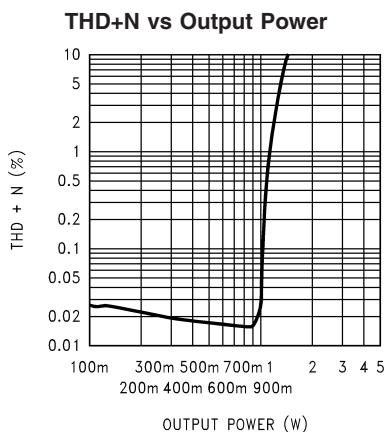


$V_{DD} = 12V$ ,  $R_L = 4\Omega$ , SE operation,  $A_V = 1$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$

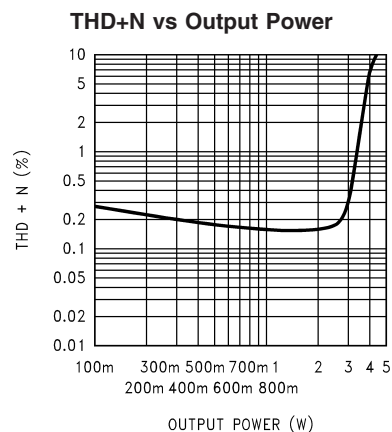


$V_{DD} = 12V$ ,  $R_L = 8\Omega$ , SE operation,  $A_V = 1$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$

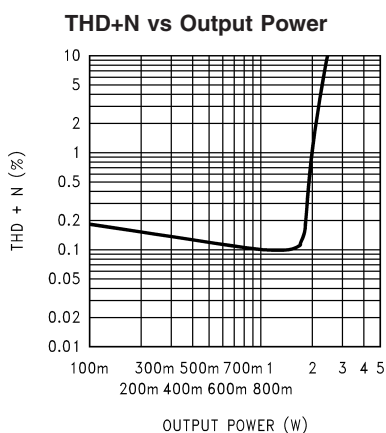
# Typical Performance Characteristics (Continued)



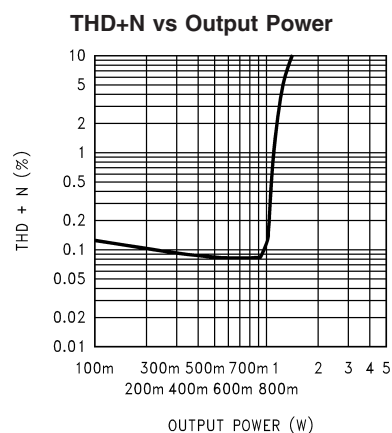
$V_{DD} = 12V$ ,  $R_L = 16\Omega$ , SE operation,  $A_V = 1$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$



$V_{DD} = 12V$ ,  $R_L = 4\Omega$ , SE operation,  $A_V = 10$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$

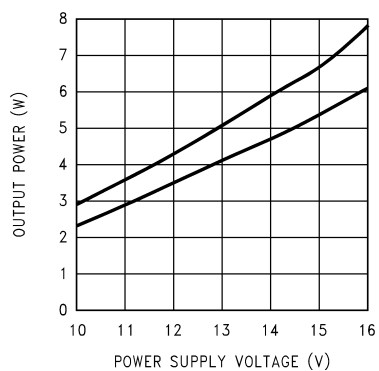


$V_{DD} = 12V$ ,  $R_L = 8\Omega$ , SE operation,  $A_V = 10$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$



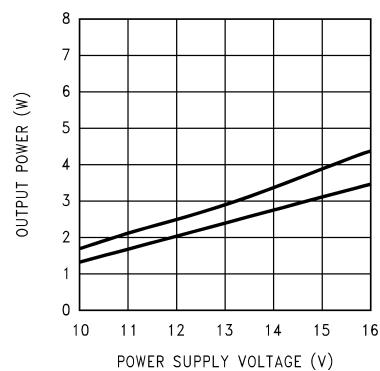
$V_{DD} = 12V$ ,  $R_L = 16\Omega$ , SE operation,  $A_V = 10$   
single channel driven/single channel measured,  
 $f_{IN} = 1kHz$

## Output Power vs Power Supply Voltage



$R_L = 4\Omega$ , SE operation,  $f_{IN} = 1kHz$ ,  
both channels driven and loaded (average shown),  
at (from top to bottom at 12V): THD+N = 10%,  
THD+N = 1%

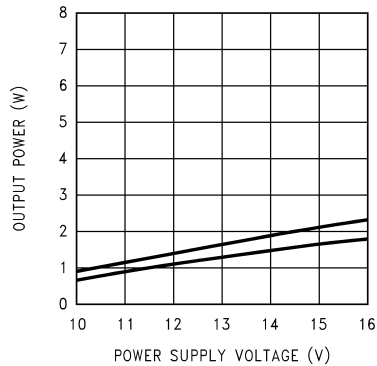
## Output Power vs Power Supply Voltage



$R_L = 8\Omega$ , SE operation,  $f_{IN} = 1kHz$ ,  
both channels driven and loaded (average shown),  
at (from top to bottom at 12V): THD+N = 10%,  
THD+N = 1%

# Typical Performance Characteristics (Continued)

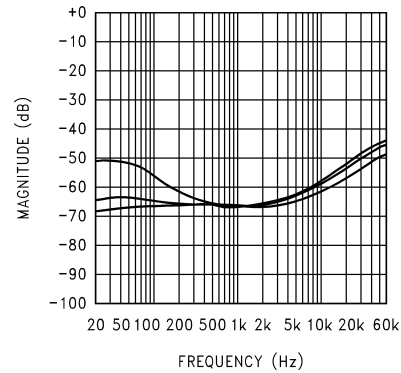
## Output Power vs Power Supply Voltage



20075667

$R_L = 16\Omega$ , SE operation,  $f_{IN} = 1\text{kHz}$ ,  
both channels driven and loaded (average shown),  
at (from top to bottom at 12V): THD+N = 10%,  
THD+N = 1%

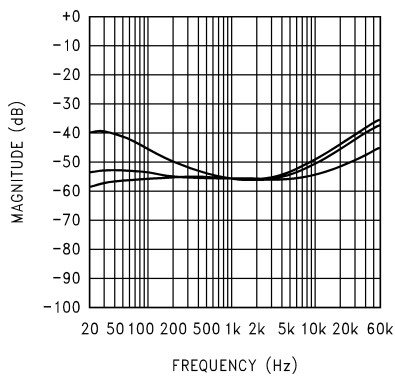
## Power Supply Rejection vs Frequency



200756B8

$V_{DD} = 12\text{V}$ ,  $R_L = 8\Omega$ , SE operation,  
 $V_{RIPPLE} = 200\text{mV}_{p-p}$ , at (from top to bottom at 60Hz):  
 $C_{BYPASS} = 1\mu\text{F}$ ,  $C_{BYPASS} = 4.7\mu\text{F}$ ,  $C_{BYPASS} = 10\mu\text{F}$ ,

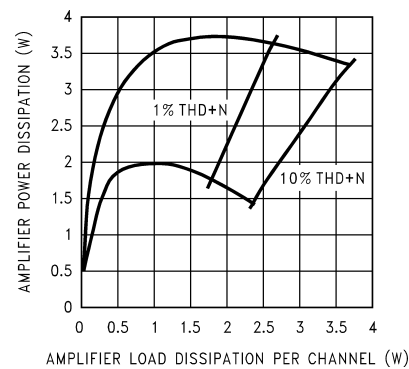
## Power Supply Rejection vs Frequency



200756D8

$V_{DD} = 12\text{V}$ ,  $R_L = 8\Omega$ , SE operation,  $V_{RIPPLE} = 200\text{mV}_{p-p}$ ,  
 $A_V = 10$ , at (from top to bottom at 60Hz):  
 $C_{BYPASS} = 1\mu\text{F}$ ,  $C_{BYPASS} = 4.7\mu\text{F}$ ,  $C_{BYPASS} = 10\mu\text{F}$

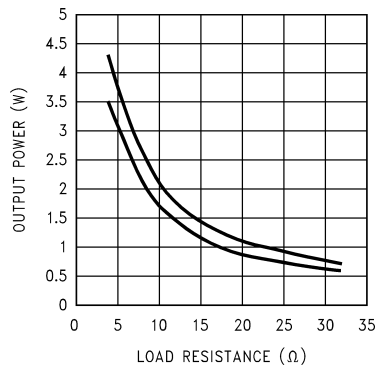
## Total Power Dissipation vs Load Dissipation



20075681

$V_{DD} = 12\text{V}$ , SE operation,  $f_{IN} = 1\text{kHz}$ ,  
at (from top to bottom at 1W):  
 $R_L = 4\Omega$ ,  $R_L = 8\Omega$

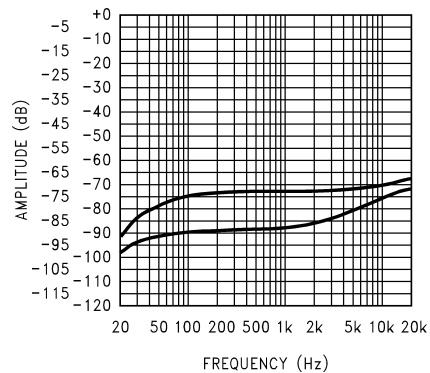
## Output Power vs Load Resistance



20075691

$V_{DD} = 12\text{V}$ , SE operation,  $f_{IN} = 1\text{kHz}$ ,  
both channels driven and loaded,  
at (from top to bottom at 15Ω):  
THD+N = 10%, THD+N = 1%

## Channel-to-Channel Crosstalk vs Frequency

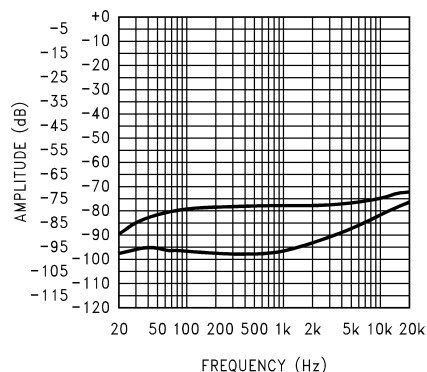


20075698

$V_{DD} = 12\text{V}$ ,  $R_L = 4\Omega$ ,  $P_{OUT} = 1\text{W}$ , SE operation,  
at (from top to bottom at 1kHz):  $V_{INB}$  driven,  
 $V_{OUTA}$  measured;  $V_{INA}$  driven,  $V_{OUTB}$  measured

## Typical Performance Characteristics (Continued)

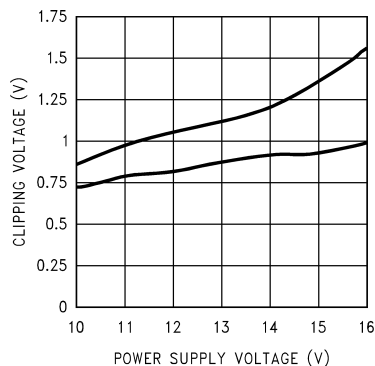
### Channel-to-Channel Crosstalk vs Frequency



200756A3

$V_{DD} = 12V$ ,  $R_L = 8\Omega$ ,  $P_{OUT} = 1W$ , SE operation,  
at (from top to bottom at 1kHz):  $V_{INB}$  driven,  
 $V_{OUTA}$  measured;  $V_{INA}$  driven,  $V_{OUTB}$  measured

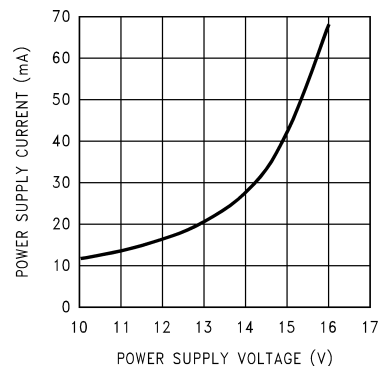
### Clipping Voltage vs Power Supply Voltage



200756F1

$R_L = 4\Omega$ , SE operation,  $f_{IN} = 1kHz$   
both channels driven and loaded,  
at (from top to bottom at 13V):  
negative signal swing, positive signal swing

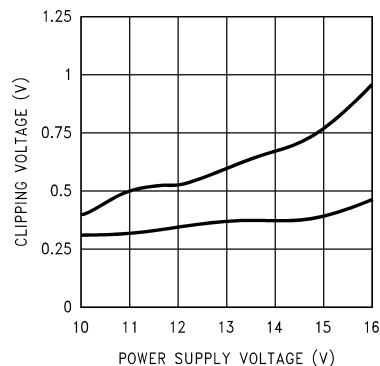
### Power Supply Current vs Power Supply Voltage



200756F0

$R_L = 4\Omega$ , SE operation  
 $V_{IN} = 0V$ ,  $R_{SOURCE} = 50\Omega$

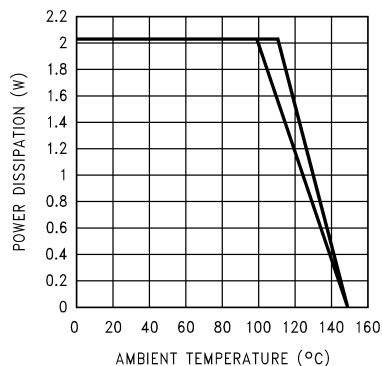
### Clipping Voltage vs Power Supply Voltage



200756F2

$R_L = 8\Omega$ , SE operation,  $f_{IN} = 1kHz$   
both channels driven and loaded, at (from top to bottom  
at 13V):  
negative signal swing, positive signal swing

### Power Dissipation vs Ambient Temperature



200756E4

$V_{DD} = 12V$ ,  $R_L = 8\Omega$  (SE),  $f_{IN} = 1kHz$ ,  
(from top to bottom at 120°C): 16in<sup>2</sup> copper plane  
heatsink area,  
8in<sup>2</sup> copper plane heatsink area



## Application Information

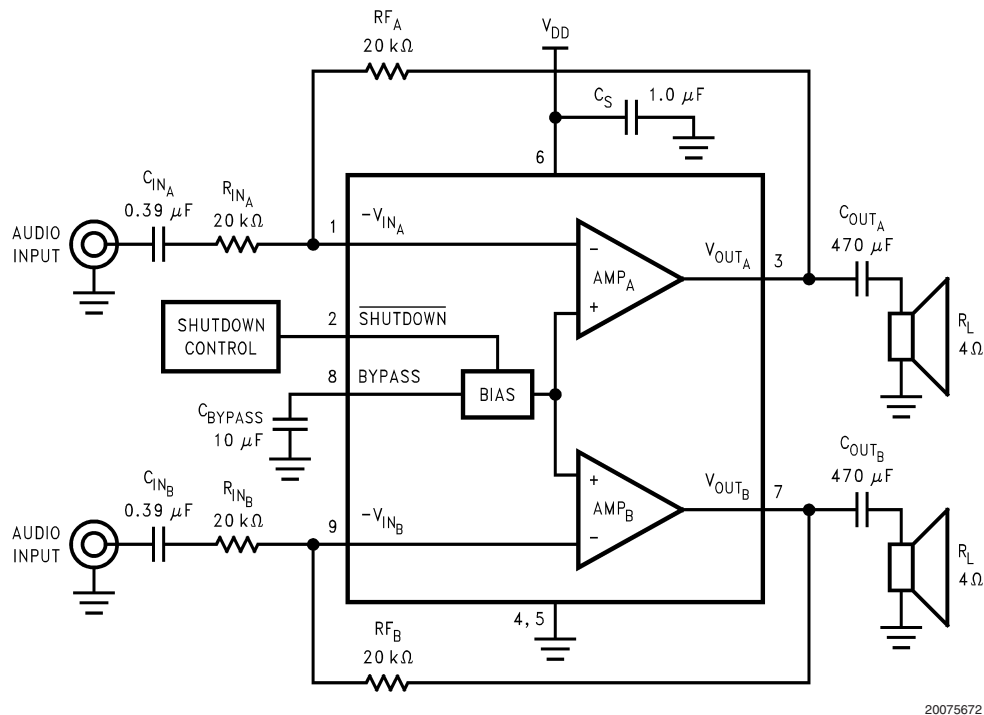


FIGURE 3. Typical LM4940 Stereo Amplifier Application Circuit

### HIGH VOLTAGE BOOMER WITH INCREASED OUTPUT POWER

Unlike previous 5V Boomer® amplifiers, the LM4940 is designed to operate over a power supply voltages range of 10V to 15V. Operating on a 12V power supply, the LM4940 will deliver 3.1W per channel into 4Ω loads with no more than 1% THD+N.

### POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended amplifier. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{\text{DMAX-SE}} = (V_{\text{DD}})^2 / (2\pi^2 R_L): \text{ Single Ended} \quad (1)$$

The LM4940's dissipation is twice the value given by Equation (2) when driving two SE loads. For a 12V supply and two 8Ω SE loads, the LM4940's dissipation is 1.82W.

The maximum power dissipation point (twice the value given by Equation (2)) must not exceed the power dissipation given by Equation (4):

$$P_{\text{DMAX}}' = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (2)$$

The LM4940's  $T_{\text{JMAX}} = 150^\circ\text{C}$ . In the TS package, the LM4940's  $\theta_{\text{JA}}$  is  $20^\circ\text{C/W}$  when the metal tab is soldered to a copper plane of at least  $16\text{in}^2$ . This plane can be split between the top and bottom layers of a two-sided PCB. Con-

nect the two layers together under the tab with a 5x5 array of vias. For the TA package, use an external heatsink with a thermal impedance that is less than  $20^\circ\text{C/W}$ . At any given ambient temperature  $T_A$ , use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting  $P_{\text{DMAX}}$  for  $P_{\text{DMAX}}'$  results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4940's maximum junction temperature.

$$T_A = T_{\text{JMAX}} - P_{\text{DMAX-SE}}\theta_{\text{JA}} \quad (3)$$

For a typical application with a 12V power supply and two 4Ω SE loads, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately  $113^\circ\text{C}$  for the TS package.

$$T_{\text{JMAX}} = P_{\text{DMAX-SE}}\theta_{\text{JA}} + T_A \quad (4)$$

Equation (6) gives the maximum junction temperature  $T_{\text{JMAX}}$ . If the result violates the LM4940's  $150^\circ\text{C}$ , reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures. The above examples assume that a device is operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

## Application Information (Continued)

If the result of Equation (3) is greater than that of Equation (4), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. Further, ensure that speakers rated at a nominal  $4\Omega$  do not fall below  $3\Omega$ . If these measures are insufficient, a heat sink can be added to reduce  $\theta_{JA}$ . The heat sink can be created using additional copper area around the package, with connections to the ground pins, supply pin and amplifier output pins. Refer to the **Typical Performance Characteristics** curves for power dissipation information at lower output power levels.

### POWER SUPPLY VOLTAGE LIMITS

Continuous proper operation is ensured by never exceeding the voltage applied to any pin, with respect to ground, as listed in the Absolute Maximum Ratings section.

### POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a voltage regulator typically use a  $10\mu\text{F}$  in parallel with a  $0.1\mu\text{F}$  filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local  $1.0\mu\text{F}$  tantalum bypass capacitance connected between the LM4940's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4940's power supply pin and ground as short as possible. Connecting a  $10\mu\text{F}$  capacitor,  $C_{\text{BYPASS}}$ , between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially  $C_{\text{BYPASS}}$ , depends on desired PSRR requirements, click and pop performance (as explained in the section, **SELECTING EXTERNAL COMPONENTS**), system cost, and size constraints.

### MICRO-POWER SHUTDOWN

The LM4940 features an active-low micro-power shutdown mode. When active, the LM4940's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low  $40\mu\text{A}$  typical shutdown current is achieved by applying a voltage to the SHUTDOWN pin that is as near to GND as possible. A voltage that is greater than GND may increase the shutdown current.

There are a few methods to control the micro-power shutdown. These include using a single-pole, single-throw switch (SPST), a microprocessor, or a microcontroller. When using a switch, connect a  $100\text{k}\Omega$  pull-up resistor between the SHUTDOWN pin and  $V_{DD}$  and the SPST switch between the SHUTDOWN pin and GND. Select normal amplifier operation by opening the switch. Closing the switch applies GND to the SHUTDOWN pin, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the active-state voltage to the SHUTDOWN pin.

## SELECTING EXTERNAL COMPONENTS

### Input Capacitor Value Selection

Two quantities determine the value of the input coupling capacitor: the lowest audio frequency that requires amplification and desired output transient suppression.

As shown in Figure 3, the input resistor ( $R_{\text{IN}}$ ) and the input capacitor ( $C_{\text{IN}}$ ) produce a high pass filter cutoff frequency that is found using Equation (7).

$$f_c = 1/2\pi R_{\text{IN}} C_{\text{IN}} \quad (5)$$

As an example when using a speaker with a low frequency limit of  $50\text{Hz}$ ,  $C_{\text{IN}}$  using Equation (7) is  $0.159\mu\text{F}$ . The  $0.39\mu\text{F}$   $C_{\text{INA}}$  shown in Figure 3 allows the LM4940 to drive high efficiency, full range speaker whose response extends below  $30\text{Hz}$ .

### Output Coupling Capacitor Value Selection

The capacitors  $C_{\text{OUTA}}$  and  $C_{\text{OUTB}}$  that block the  $V_{DD}/2$  output DC bias voltage and couple the output AC signal to the amplifier loads also determine low frequency response. These capacitors, combined with their respective loads create a highpass filter cutoff frequency. The frequency is also given by Equation (6).

Using the same conditions as above, with a  $4\Omega$  speaker,  $C_{\text{OUT}}$  is  $820\mu\text{F}$  (nearest common value).

### Bypass Capacitor Value

Besides minimizing the input capacitor size, careful consideration should be paid to value of  $C_{\text{BYPASS}}$ , the capacitor connected to the BYPASS pin. Since  $C_{\text{BYPASS}}$  determines how fast the LM4940 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4940's outputs ramp to their quiescent DC voltage (nominally  $V_{DD}/2$ ), the smaller the turn-on pop. Choosing  $C_{\text{BYPASS}}$  equal to  $10\mu\text{F}$  along with a small value of  $C_{\text{IN}}$  (in the range of  $0.1\mu\text{F}$  to  $0.39\mu\text{F}$ ), produces a click-less and pop-less shutdown function. As discussed above, choosing  $C_{\text{IN}}$  no larger than necessary for the desired bandwidth helps minimize clicks and pops.

### OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4940 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the  $V_{DD}/2$  voltage present at the BYPASS pin ramps to its final value, the LM4940's internal amplifiers are configured as unity gain buffers and are disconnected from the  $\text{AMP}_A$  and  $\text{AMP}_B$  pins. An internal current source charges the capacitor connected between the BYPASS pin and GND in a controlled manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage applied to the BYPASS pin.

The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches  $V_{DD}/2$ . As soon as the voltage on the bypass pin is stable, the device becomes fully operational and the amplifier outputs are reconnected to their respective output pins. Although the BYPASS pin current cannot be modified, changing the size of  $C_{\text{BYPASS}}$  alters the device's turn-on time. Here are some typical turn-on times for various values of  $C_{\text{BYPASS}}$ :

## Application Information (Continued)

| C <sub>B</sub> (μF) | T <sub>ON</sub> (ms) |
|---------------------|----------------------|
| 1.0                 | 120                  |
| 2.2                 | 120                  |
| 4.7                 | 200                  |
| 10                  | 440                  |

In order to eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V<sub>DD</sub> may not allow the capacitors to fully discharge, which may cause "clicks and pops".

There is a relationship between the value of C<sub>IN</sub> and C<sub>BYPASS</sub> that ensures minimum output transient when power is applied or the shutdown mode is deactivated. Best performance is achieved by setting the time constant created by C<sub>IN</sub> and R<sub>i</sub> + R<sub>f</sub> to a value less than the turn-on time for a given value of C<sub>BYPASS</sub> as shown in the table above.

### AUDIO POWER AMPLIFIER DESIGN

#### Audio Amplifier Design: Driving 3W into a 4Ω load

The following are the desired operational parameters:

|                 |                           |
|-----------------|---------------------------|
| Power Output    | 3W <sub>RMS</sub>         |
| Load Impedance  | 4Ω                        |
| Input Level     | 0.3V <sub>RMS</sub> (max) |
| Input Impedance | 20kΩ                      |
| Bandwidth       | 100Hz–20kHz ± 0.25dB      |

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the *Output Power vs Power Supply Voltage* curve in the **Typical Performance Characteristics** section. Another way, using Equation (8), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the *Clipping Dropout Voltage vs Power Supply Voltage* in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (8). The result is Equation (9).

$$V_{\text{opeak}} = \sqrt{(2R_L P_O)} \quad (6)$$

$$V_{DD} = V_{\text{OUTPEAK}} + V_{\text{ODTOP}} + V_{\text{ODBOT}} \quad (7)$$

The *Output Power vs. Power Supply Voltage* graph for an 8Ω load indicates a minimum supply voltage of 11.8V. The commonly used 12V supply voltage easily meets this. The additional voltage creates the benefit of headroom, allowing the LM4940 to produce an output power of 3W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates the maximum power dissipation as explained above in the Power Dissipation section. After satisfying the LM4940's power dissipation requirements, the minimum differential gain needed to achieve 3W dissipation in a 4Ω BTL load is found using Equation (10).

$$A_V \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{\text{orms}} / V_{\text{inrms}} \quad (8)$$

Thus, a minimum gain of 11.6 allows the LM4940's to reach full output swing and maintain low noise and THD+N performance. For this example, let A<sub>V</sub> = 12. The amplifier's overall BTL gain is set using the input (R<sub>IN<sub>A</sub></sub>) and feedback (R) resistors of the first amplifier in the series BTL configuration. Additionally, A<sub>V,BTL</sub> is twice the gain set by the first amplifier's R<sub>IN</sub> and R<sub>f</sub>. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_f / R_{IN} = A_V \quad (9)$$

The value of R<sub>f</sub> is 240kΩ. The nominal output power is 3W.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB-desired limit. The results are an

$$f_L = 100\text{Hz} / 5 = 20\text{Hz} \quad (10)$$

and an

$$f_H = 20\text{kHz} \times 5 = 100\text{kHz} \quad (11)$$

As mentioned in the **SELECTING EXTERNAL COMPONENTS** section, R<sub>INA</sub> and C<sub>INA</sub>, as well as C<sub>OUT</sub> and R<sub>L</sub>, create a highpass filter that sets the amplifier's lower band-pass frequency limit. Find the coupling capacitor's value using Equation (14).

$$C_{IN} = 1 / 2\pi R_{IN} f_L \quad (12)$$

The result is

$$1 / (2\pi \times 20\text{k}\Omega \times 20\text{Hz}) = 0.398\mu\text{F} = C_{IN}$$

and

$$1 / (2\pi \times 4\Omega \times 20\text{Hz}) = 1989\mu\text{F} = C_{OUT}$$

Use a 0.39μF capacitor for C<sub>IN</sub> and a 2000μF capacitor for C<sub>OUT</sub>, the closest standard values.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A<sub>V</sub>, determines the upper passband response limit. With A<sub>V</sub> = 12 and f<sub>H</sub> = 100kHz, the closed-loop gain bandwidth product (GBWP) is 1.2mHz. This is less than the LM4940's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.

## Application Information (Continued)

### RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 5 through Figure 7 show the recommended two-layer PC board layout that is optimized for the TO263-packaged LM4940 and associated external components. This circuit board is designed for use with an external 12V supply and 4Ω(min) speakers.

This circuit board is easy to use. Apply 12V and ground to the board's  $V_{DD}$  and GND pads, respectively. Connect a speaker between the board's  $OUT_A$  and  $OUT_B$  outputs and their respective GND terminals.

### Demonstration Board Layout

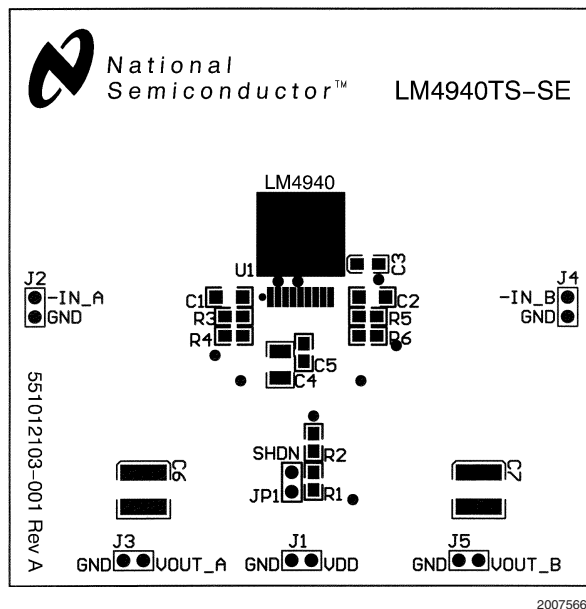


FIGURE 4. Recommended TS PCB Layout:  
Top Silkscreen

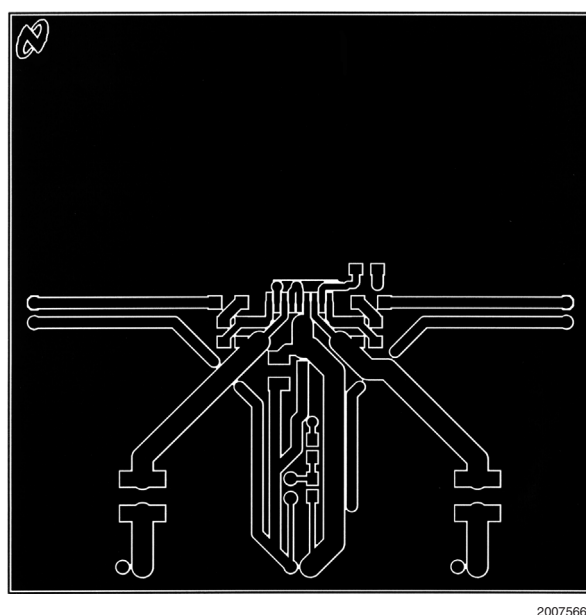
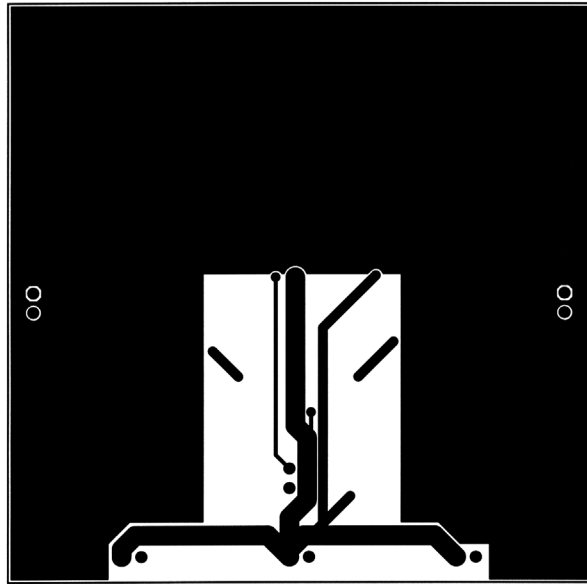


FIGURE 5. Recommended TS PCB Layout:  
Top Layer

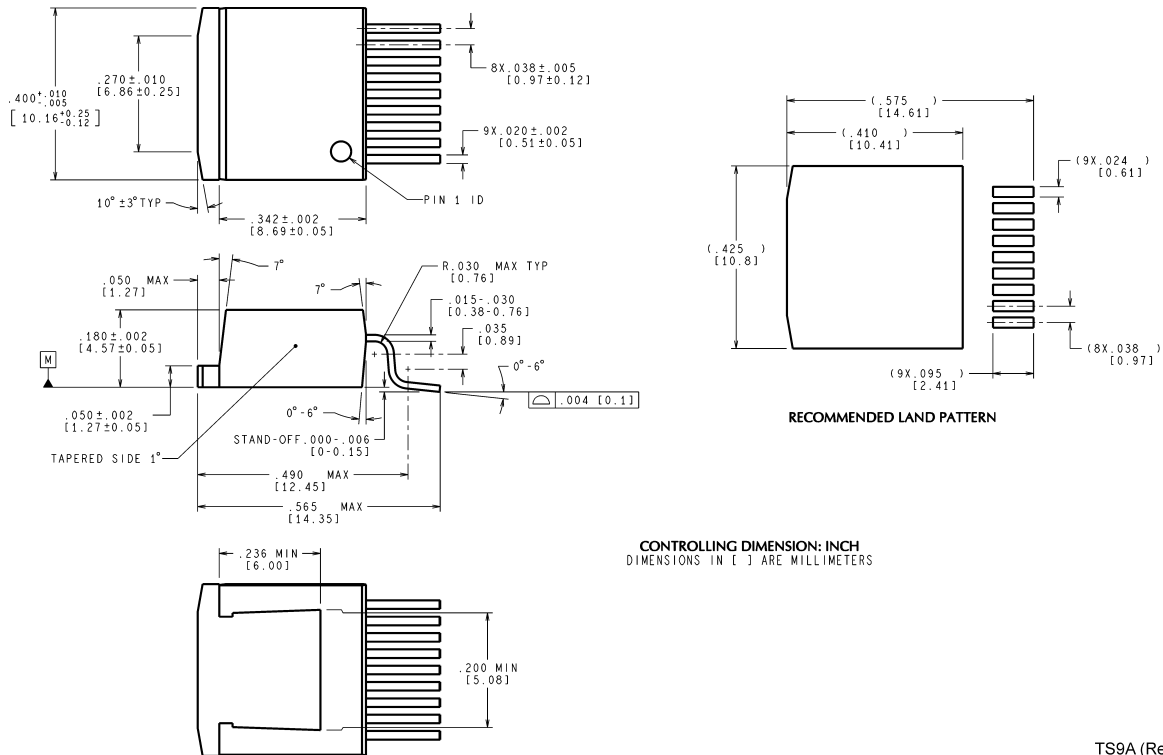
## Demonstration Board Layout (Continued)



20075665

**FIGURE 6. Recommended TS PCB Layout:  
Bottom Layer**

## Physical Dimensions inches (millimeters) unless otherwise noted



Plastic Package,  
Order Number LM4940TS  
NS Package Number TS9A

TS9A (Rev B)

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